

Optimal Integration and Characteristics of Vertical Array Devices for Ultra-High Density, Bit-Cost Scalable Flash Memory

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Abstract

Optimal process integration for array devices of Bit-Cost Scalable (BiCS) flash memory is successfully developed. We adopt SiN-based gate dielectrics for the consistency with the 'gate-first' process which is unique to BiCS flash technology, and 'macaroni' body FETs for better controllability over the sub-threshold characteristics of depletion-mode poly-silicon transistors. With these technologies and newly devised $4F^2$ cell array, BiCS flash becomes a promising candidate for future ultra-high density memory.

Introduction

Three-dimensional memories are gathering increasing attention as future ultra-high density memory technologies to keep a trend of increasing bit density and reducing bit cost. Among several proposals, including stacked two-dimensional array structures as reported in previous papers (1,2), one of the promising candidates is Bit-Cost Scalable (BiCS) flash technology (3).

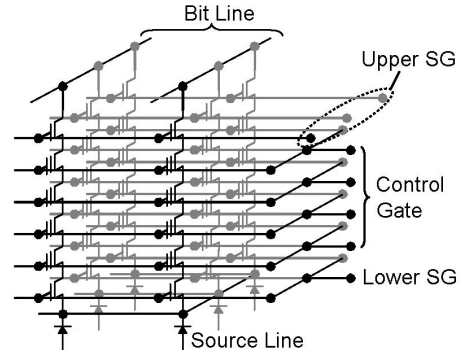


Figure 2: Equivalent circuit of BiCS Flash memory.

Concept of BiCS flash is explained in Figs.1-2. Whole stack of electrode plates are punched through and plugged with poly-silicon at one time, forming a series of vertical FETs which act as a NAND string of SONOS-type memories. The memory FETs work in depletion-mode with the body poly-silicon being undoped or lightly n-doped uniformly, to avoid the process complexity of forming p-n junctions within the plug. Each plate acts as a control gate except the lowest plate, functioning as the lower select gate. A single bit is accessed at the intersection of a control gate plate and a string, which is selected by a bit line and an upper select gate. The bottom of memory string is connected to the common source diffusion formed on the silicon substrate. For the erase operation, hole current generated by GIDL near the lower select gate is used to raise the body potential as shown in Fig.3.

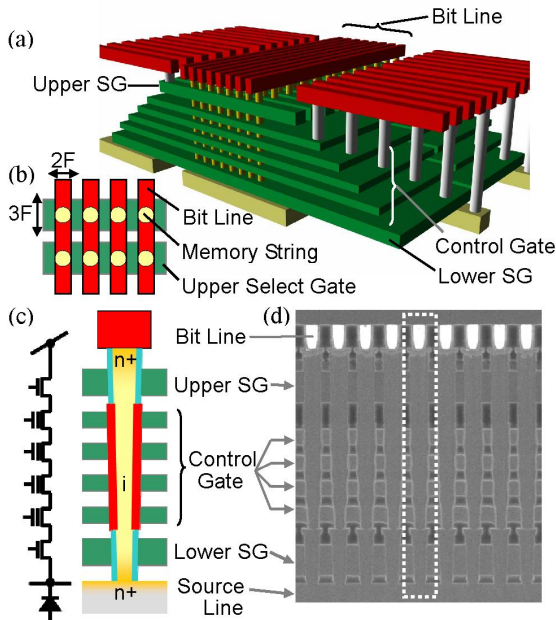


Figure 1: (a) Birds-eye view of BiCS Flash memory. (b) Top-down view of BiCS Flash memory array. (c) Enlarged view of the memory string. (d) Cross sectional SEM image of BiCS Flash memory array.

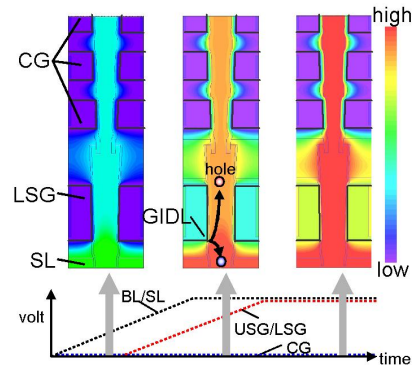


Figure 3: Simulated potential profile at erase operation.

One of the most essential technologies for BiCS flash memory is well-controlled poly-silicon channel vertical FET, which has to be consistent with the above mentioned 'punch-and-plug' process as well. In this paper, we propose novel SiN-based gate dielectrics for better process compatibility, and 'macaroni' body FET for better controllability over sub-threshold characteristics. Extendability of BiCS flash memory is also discussed.

SiN-based Gate Dielectric

In the 'punch-and-plug' process, the order of forming body, gate dielectric film and gate electrode is opposite to the case in conventional FET. As shown in Fig.4, this 'gate-first' process forces the gate dielectric surface to be exposed to diluted-HF prior to the poly-silicon deposition for good silicon-silicon contact at the bottom of the plug. Although there is an option to utilize SiO₂-based gate dielectric with some additional process steps for the protection, in order to minimize the process cost, we have developed SiN-based gate dielectric FETs compatible with the simplest and yet the most effective diluted-HF treatment.

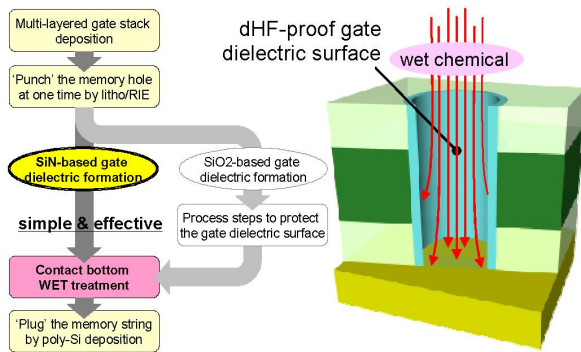


Figure 4: Process to form memory string. Compatibility to the bottom wet treatment for good contact is essential for simple low-cost process.

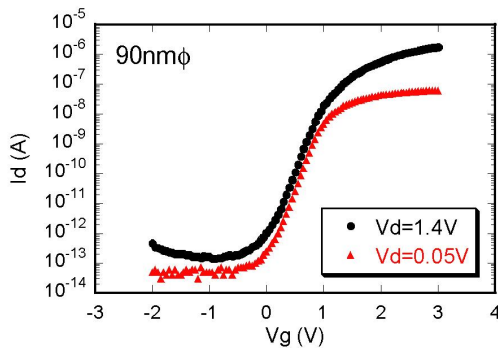


Figure 5: Id-Vg characteristics of select gate vertical FET with SiN-gate dielectric.

Fig.5 shows the Id-Vg characteristics of the select gate FET. The gate dielectric is 7nm SiN which is deposited by LPCVD. Good Ion/Ioff ratio of more than 6 orders with sub-threshold slope of ~190mV/dec is obtained.

As for the memory element, we propose vertical SONS FETs, so that the surface of the gate dielectric is covered not by SiO₂ as is the case of SONOS, but by SiN which is durable against the diluted-HF treatment. The program/erase, endurance, and retention characteristics are shown in Figs.6-8, respectively. Reasonable operational window is obtainable after 10 years.

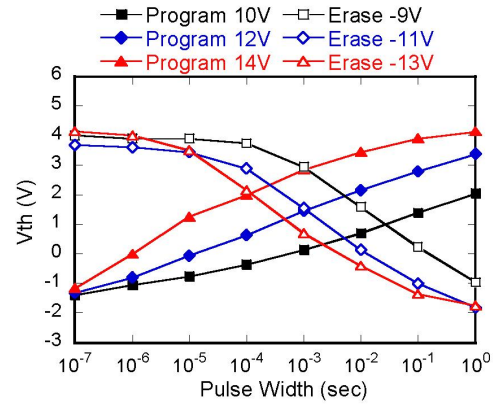


Figure 6: Program/erase characteristics of vertical SONS memory.

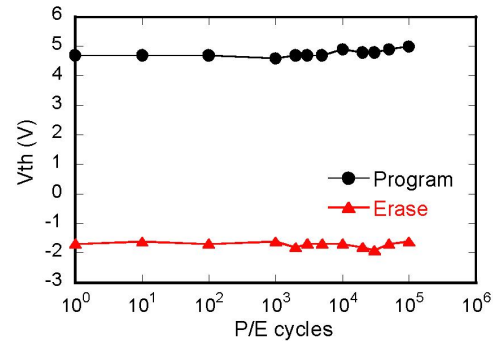


Figure 7: Program/erase cycle endurance of vertical SONS memory.

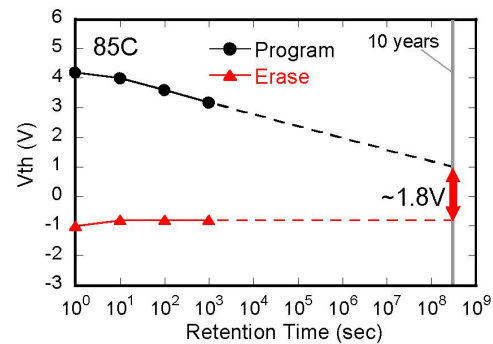


Figure 8: Retention characteristics of vertical SONS memory at 85C.

'Macaroni' Body Vertical FET

Making full use of poly-silicon as transistor body material is essential for BiCS technology, because the aspect ratio of the punched holes for the memory string is so high that non-selective conformal deposition method is preferable for reasonable production yield. However, sub-threshold characteristics of poly-silicon FETs are quite dependent on trap density at grain boundary, which is out of control in most cases. Based on the model described in Fig.9, our approach to achieve better controllability is making the body silicon much thinner than the depletion width (W_d), in order to reduce the volume of poly-silicon and total number of traps, and to make threshold voltage less sensitive to the trap density fluctuation.

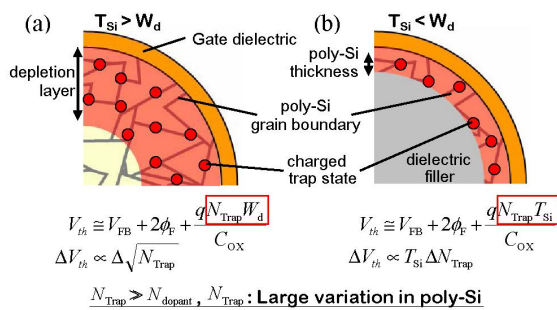


Figure 9: Schematics of V_{th} dependence on trap density at poly-silicon grain boundaries when (a) $T_{Si} > W_d$, and (b) $T_{Si} < W_d$. (For simplicity, V_{th} expression above is not the one for cylindrical coordinates (4), but for planer system.) If poly-Si is thinner than depletion layer width, ΔV_{th} becomes dependent on total number of traps, and thus becomes smaller with thinner body thickness.

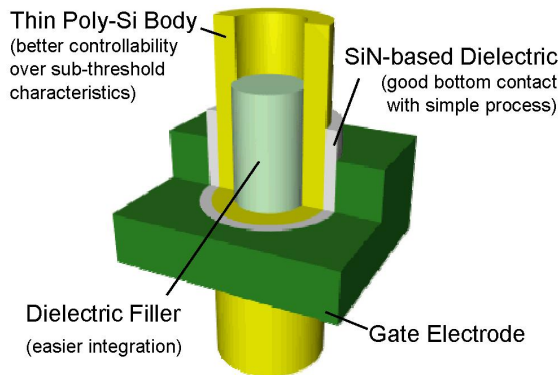


Figure 10: Concept of 'Macaroni' Body Vertical FET.

Concept of the 'macaroni' body vertical FET is described in Fig.10. Very thin poly-silicon is deposited on the gate dielectric to form macaroni-shaped body. Hollow center of the body is filled with dielectric film to make process integration easier. Thinner body thickness makes channel potential better controlled by gate electrode as simulated in Fig.11.

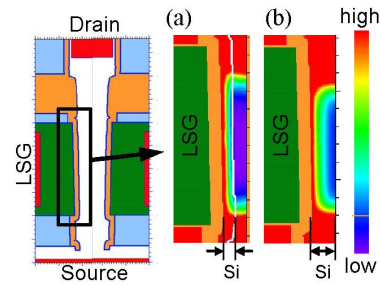


Figure 11: Simulated electric field in (a) 'Macaroni' body vertical FET, and (b) Conventional vertical FET.

Fig.12 shows I_d - V_g characteristics of the 'macaroni' body vertical FET. The reduced but sufficient amount of poly-silicon results in better control of sub-threshold characteristics with increased drive current. V_{th} variation in 300mm wafer is well trimmed by the new device design as shown in Fig.13. TEM images and corresponding I_d - V_g curves are shown in Fig.14. FET characteristics fall into almost the same curves regardless of the grain appearance.

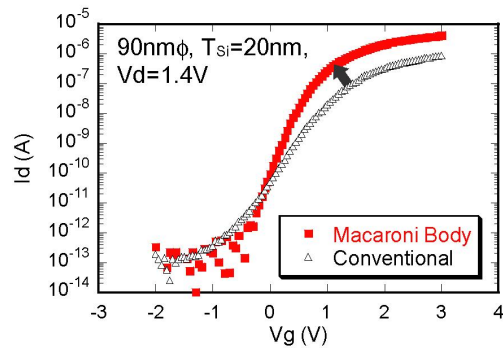


Figure 12: Typical I_d - V_g characteristics of conventional vertical FET and 'Macaroni' body vertical FET.

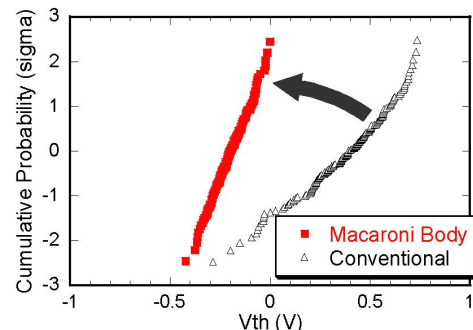


Figure 13: V_{th} distribution of conventional and 'Macaroni' body vertical FET.

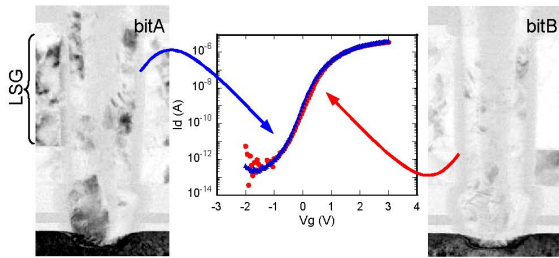


Figure 14: TEM images of 'Macaroni' body vertical FETs and corresponding Id-Vg curves. FET characteristics fall into the same curves regardless of the grain structure.

Extendability of BiCS Flash Memory

Measured V_{th} variations of several kinds of vertical FETs are plotted as a function of poly-silicon body radius or 'macaroni' thickness in Fig.15, showing good agreement with our model assuming $W_d \sim 35\text{nm}$ and $N_{trap} \sim 10^{18}\text{cm}^{-3}$, which is estimated from Id-Vg characteristics using field effect conductance method (5). 'Macaroni' body design offers better controllability until 30nm generation, and after that, diameter of the plug would be small enough to suppress V_{th} variation whether poly-silicon body has hollow center, i.e. a seam, or not.

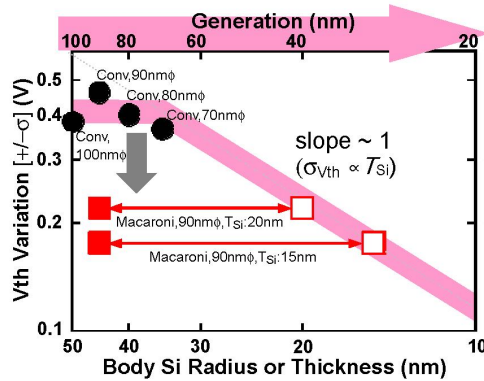


Figure 15: Extendability of 'Macaroni' body vertical FET. V_{th} variations in 300mm wafer are plotted as a function of body Si radius or thickness.

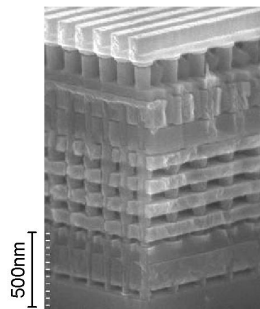


Figure 16: Birds-eye view SEM image of BiCS Flash memory.

Fig.16 shows a birds-eye view SEM image of the successfully fabricated 90nm $6F^2$ BiCS flash cell array. To pursue the bit cost efficiency more, we propose the novel $4F^2$ cell array structure with double layered, alternate select gate structure as described in Fig.17. Based on RIE & damascene process, critical lithography step is not required to be added. As plotted in Fig.18, BiCS flash technology keeps its bit cost superiority towards 8Tb generation.

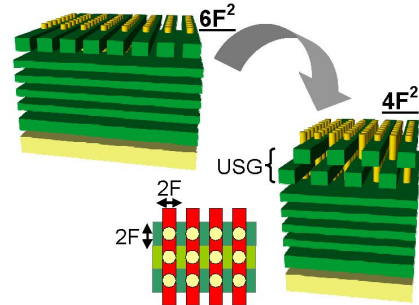


Figure 17: Concept of $4F^2$ memory string for further bit-cost efficiency.

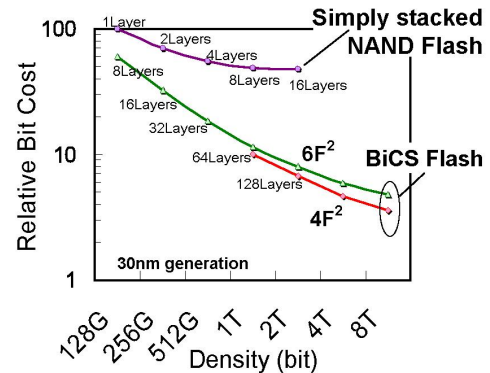


Figure 18: Extendability of BiCS Flash memory.

Conclusion

We have achieved the well-controlled poly-silicon channel vertical array devices with newly developed SiN-based gate dielectric and 'macaroni' body vertical FET, which are best suited for BiCS flash. By these technologies and the novel $4F^2$ string structure, BiCS flash becomes a promising solution for the future ultra-high density memory.

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