Universality of Short-Channel Effects in Undoped-Body Silicon Nanowire MOSFETs

Sarunya Bangsaruntip, Guy M. Cohen, Amlan Majumdar, and Jeffrey W. Sleight

***Abstract*—Experimental data from undoped-body gate-all-around (GAA) silicon nanowire (NW) MOSFETs with different sizes demonstrate the universality of short-channel effects as a function of L_{EFF}/λ, where L_{EFF} is the effective channel length and λ is the electrostatic scaling length. Data from undoped-body single-gate extremely thin SOI (ETSOI) devices additionally show that the universality of short-channel effects is valid for any undoped-body fully depleted SOI MOSFET. Our data indicate that L_{EFF} of undoped GAA NW MOSFETs can be scaled down by $\sim$2.5 times compared with undoped single-gate ETSOI MOSFETs while maintaining equivalent short-channel control.**

***Index Terms*—Fully depleted SOI (FDSOI), gate-all-around (GAA), MOSFETs, short-channel effects, silicon nanowire (NW).**

I. INTRODUCTION

FULLY depleted SOI (FDSOI) MOSFETs are attractive candidates for the 15-nm technology node and beyond because their thin body dimensions provide geometric electrostatic confinement for controlling short-channel effects as well as less stringent requirements of gate-oxide thickness scaling over conventional bulk Si or partially depleted SOI MOSFETs [1]. FDSOI architectures include single-gate extremely thin SOI (ETSOI) FETs, FinFETs, trigate FETs, and gate-all-around (GAA) nanowire (NW) FETs. Scaling theories for FDSOI MOSFETs predict that the short-channel effects improve when the relevant body dimensions are shrunk [2]–[6]. For the same body dimensions, GAA NW FETs have the best short-channel control among all the FDSOI architectures [4], [6]. Many groups have investigated the short-channel characteristics of Si NW FETs [7]–[10]. However, there are no experimental reports on the improvement in scalability of Si NW FETs as the body size is reduced. On the contrary, the data in [9] show degraded short-channel control at small NW diameters.

In this letter, we show that the short-channel effects of undoped-body GAA Si NW MOSFETs improve upon shrinking the body dimensions. Furthermore, data from NW FETs and undoped-body ETSOI MOSFETs with different SOI thicknesses [11] demonstrate the universality of short-channel effects in undoped-body FDSOI MOSFETs as a function of L_{EFF}/λ, where L_{EFF} is the effective channel length and λ is the relevant electrostatic scaling length. We also show that undoped GAA NW devices provide $\sim$2.5 times better L_{EFF} scaling compared with undoped single-gate ETSOI devices at constant short-channel effects.

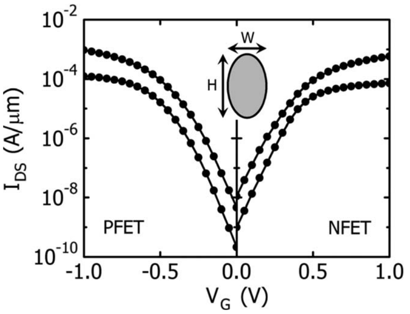

Fig. 1. Drain current I_{DS} versus gate voltage V_G characteristics of undoped-body GAA Si NW (left) PFETs and (right) NFETs at drain bias $|V_{\mathrm{DS}}| =$ 0.05 and 1 V. Both devices have gate length $L_G = 25$ nm, width $W = 9$ nm, and height $H = 13.9$ nm. Inset: Schematic cross section of an elliptical NW.

II. NW MOSFET SCALING

The device-fabrication scheme for the Si NW FETs is described in detail in [12]. Briefly, the NW devices have an undoped body, TaN metal gate, and Hf-based gate dielectric. The inversion oxide thickness $T_{\mathrm{INV}} = 1.7$ nm was obtained from capacitance–voltage measurements at 1 MHz. Therefore, we estimate an equivalent oxide thickness EOT $\sim$ 1.4 nm. Various sizes of NWs were patterned on the same wafer using electron-beam lithography and reactive ion etching. A combination of H_2 annealing and high-temperature oxidation processes was used to obtain ultrasmooth NWs down to $\sim$5 nm in size. NFETs and PFETs were fabricated on the same wafer with their source/drain contacts formed by As and B implantation, respectively, followed by a single activation anneal. Due to our smoothening process, the NW cross sections are elliptical with width W and height H, as shown in the inset of Fig. 1. The W and H, as well as the physical gate lengths L_G of the devices were obtained by transmission electron microscopy and scanning electron microscopy (SEM).

The undoped-body GAA Si NW devices have excellent short-channel control down to $L_G \sim 25$ nm, as shown in the transfer characteristics in Fig. 1, with drain-induced barrier lowering (DIBL) of $\sim$100 mV/V and saturated subthreshold slope $\mathrm{SS}_{\mathrm{SAT}} \sim 90$ mV/decade. We define DIBL as $|V_{\mathrm{TLIN}} - V_{\mathrm{TSAT}}|/0.95$ V, where V_{TLIN} and V_{TSAT} are threshold voltages at drain bias $|V_{\mathrm{DS}}| = 0.05$ and 1 V, respectively, and extract $\mathrm{SS}_{\mathrm{SAT}}$ at $|V_{\mathrm{DS}}| = 1$ V. The L_G dependence of DIBL and $\mathrm{SS}_{\mathrm{SAT}}$ of NW FETs with different body dimensions is

---

Manuscript received February 1, 2010; revised May 11, 2010; accepted May 24, 2010. Date of publication July 19, 2010; date of current version August 25, 2010. The review of this letter was arranged by Editor B.-G. Park.

The authors are with IBM Research Division, T. J. Watson Research Center, Yorktown Heights, NY 10598 USA (e-mail: amajumd@us.ibm.com).

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LED.2010.2052231

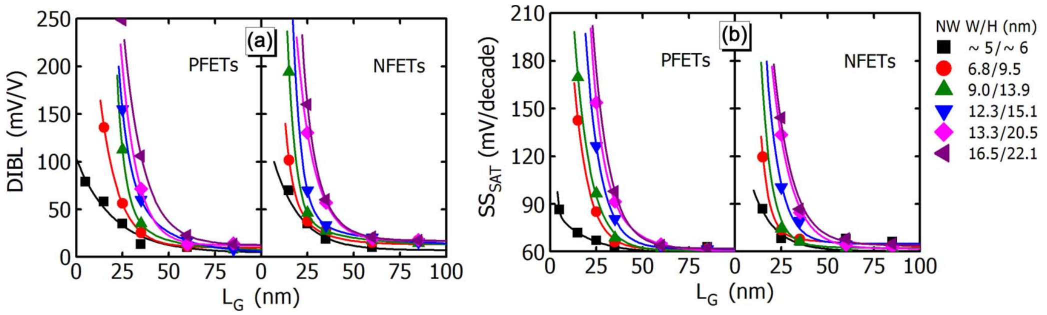

Fig. 2. (a) DIBL and (b) saturated subthreshold slope SS_{SAT} versus gate length L_G of undoped-body GAA Si NW (left panel) PFETs and (right panel) NFETs with different width W and height H. DIBL is defined as $|V_{TLIN} - V_{TSAT}|/0.95$ V, where V_{TLIN} and V_{TSAT} are threshold voltages at drain bias $|V_{DS}| = 0.05$ and 1 V, respectively. SS_{SAT} is extracted at $|V_{DS}| = 1$ V. Estimated error in L_G by SEM is on the order of ±5 nm. The lines are guides to the eye.

shown in Fig. 2. The short-channel control of NW FETs clearly improves upon shrinking the body dimensions.

In order to investigate the L_{EFF} scaling properties of NW FETs, we use the electrostatic scaling length of rectangular NWs as an approximation to our elliptical NWs. For rectangular NWs, the scaling length λ is given by

$$\lambda_{RNW} = \frac{\lambda_H \lambda_W}{\sqrt{\lambda_H^2 + \lambda_W^2}} \quad (1)$$

where

$$\lambda_H = \sqrt{\frac{1}{2}\frac{\varepsilon_{SI}}{\varepsilon_{OX}} T_{OX} H + \frac{1}{8} H^2} \quad (2)$$

$$\lambda_W = \sqrt{\frac{1}{2}\frac{\varepsilon_{SI}}{\varepsilon_{OX}} T_{OX} W + \frac{1}{8} W^2} \quad (3)$$

where T_{OX} is the gate-oxide thickness and ε_{SI} and ε_{OX} are the dielectric constants of Si and SiO_2, respectively [13]. One should note that these scaling lengths were derived under the assumption that maximum subthreshold leakage occurs at the center of the FDSOI body, which implies that quantum mechanics has been taken into account to the first order. We define $L_{EFF} = L_G - \Delta L$, where ΔL represents the net overlap of the source/drain extensions with the gate. Using ΔL as a fitting parameter and T_{OX} = EOT = 1.4 nm, we find that the DIBL and SS_{SAT} of NW NFETs and PFETs of all sizes collapse on to the same curve as a function of L_{EFF}/λ_{RNW} for $\Delta L = -4$ nm for NFETs and 0 nm for PFETs, as shown in Fig. 3. This clearly demonstrates that the short-channel effects of undoped-body GAA NW FETs are universal, as expected from scaling theory [4], [6]. The extracted values of ΔL indicate that the NW NFETs are less overlapped than the NW PFETs, which is consistent with the slower diffusion rate of As than B [14].

III. UNIVERSAL FDSOI MOSFET SCALING

A similar analysis was performed previously for undoped-body single-gate ETSOI MOSFETs with SOI thickness T_{SOI} in the 8.6–19.2-nm range and T_{OX} = EOT = 1.1 nm [11]. The scaling length used in [11] for undoped-body ETSOI devices with no back gate bias was

$$\lambda_{ETSOI} = \sqrt{\frac{\varepsilon_{SI}}{\varepsilon_{OX}} T_{OX} T_{SOI} + \frac{1}{2} T_{SOI}^2}. \quad (4)$$

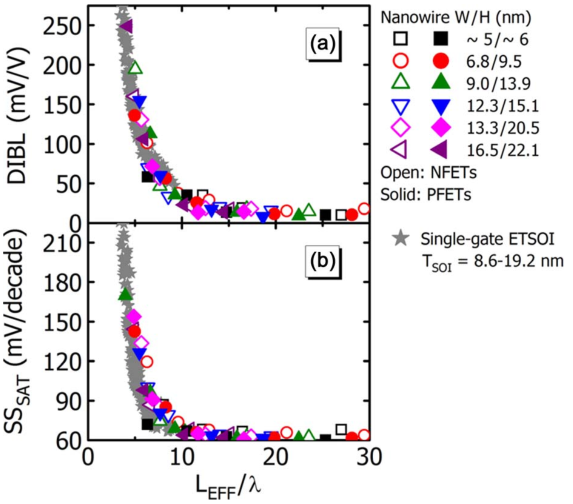

Fig. 3. (a) DIBL and (b) saturated subthreshold slope SS_{SAT} versus L_{EFF}/λ of undoped-body GAA Si NW (open symbols) NFETs and (solid symbols) PFETs with different width W and height H. L_{EFF} is the effective channel length, and λ is the electrostatic scaling length. Also, shown are data for undoped-body single-gate ETSOI MOSFETs with SOI thickness $T_{SOI} = 8.6-19.2$ nm [11]. We use $\lambda = \lambda_{RNW}$ for NW devices (1) and λ_{ETSOI} for ETSOI devices (4), as described in the text.

In Fig. 3, we also show the ETSOI scaling data from [11]. What is interesting is that the NW data fall on top of the ETSOI data on both DIBL and SS_{SAT} versus L_{EFF}/λ plots. Therefore, the experimental data in Fig. 3 clearly demonstrate that the short-channel effects of FDSOI devices are universal as a function of L_{EFF}/λ when one uses the appropriate λ for each FDSOI architecture. This universality, while heartening to observe in the experimental data, is not surprising. This is because scaling theories for undoped-body FDSOI devices lead to the same Laplace equation for electrostatic potential along the lateral (source/drain) direction for all FDSOI architectures with a different scaling length for each FDSOI geometry [2]–[6]. Therefore, short-channel effects are expected to be a universal

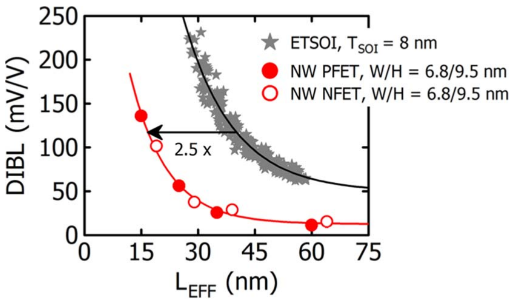

Fig. 4. Comparison of DIBL of GAA NW FETs (width $W = 6.8$ nm and height $H = 9.5$ nm) and single-gate ETSOI FETs (SOI thickness $T_{\mathrm{SOI}} = 8$ nm) [15] with similar body dimensions.

function of L_{EFF}/λ for all FDSOI architectures. We also note that the usefulness of the data in Fig. 3 is manifold. One can use this data to extract overlap ΔL when ΔL is not known, as we did. One can also use this data to verify if their estimate of body dimensions of any FDSOI device is correct, as short-channel-effect data with incorrect body dimensions will not fall on the universal curves for DIBL and $\mathrm{SS}_{\mathrm{SAT}}$.

Finally, we compare short-channel control in GAA NW FETs and single-gate ETSOI FETs with similar body dimensions and EOT in Fig. 4. We observe that, at constant short-channel effects, the NW devices have ∼2.5 times smaller L_{EFF} compared with the single-gate ETSOI devices, which is in good agreement with the ratio of their respective scaling lengths ($\lambda_{\mathrm{RNW}} = 3$ nm and $\lambda_{\mathrm{ETSOI}} = 7.7$ nm). In the thin T_{OX} limit, $\lambda_{\mathrm{ETSOI}}/\lambda_{\mathrm{NW}} = 2\sqrt{2} = 2.8$ using the parabolic potential approximation [4], and $2 \times 4.81/\pi = 3.06$ using the evanescent-mode analysis [6]. These theoretical ratios are somewhat higher than our observed value of ∼2.5. This is primarily due to the fact that our NW devices have slightly thicker T_{OX} than the ETSOI devices and also because the thin T_{OX} condition is not satisfied in our devices.

IV. CONCLUSION

In conclusion, we have shown that short-channel control in undoped-body GAA Si NW MOSFETs improves upon shrinking the body dimensions, as expected from scaling theories for FDSOI devices. Using the NW data and previously published data for single-gate ETSOI devices, we have demonstrated that short-channel effects in undoped-body FDSOI devices are a universal function of L_{EFF}/λ when the appropriate λ for each FDSOI architecture is used. Furthermore, we have shown that, compared with the single-gate ETSOI devices, the GAA NW geometry leads to ∼2.5 times smaller L_{EFF} with similar short-channel control.

ACKNOWLEDGMENT

The authors would like to thank W. Haensch, S. Guha, S. Koester, Q. Ouyang, J. Silverman, and the staff of IBM Yorktown Microelectronics Research Laboratory facility for their support.

REFERENCES

[1] W. Haensch, E. J. Nowak, R. H. Dennard, P. M. Solomon, A. Bryant, O. H. Dokumaci, A. Kumar, X. Wang, J. B. Johnson, and M. V. Fischetti, "Silicon CMOS devices beyond scaling," *IBM J. Res. Develop.*, vol. 50, no. 4/5, pp. 339–361, Jul. 2006.

[2] K. K. Young, "Short-channel effect in fully depleted SOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 36, no. 2, pp. 399–402, Feb. 1989.

[3] K. Suzuki, T. Tanaka, Y. Tosaka, H. Horie, and Y. Arimoto, "Scaling theory for double-gate MOSFETs," *IEEE Trans. Electron Devices*, vol. 40, no. 12, pp. 2326–2329, Dec. 1993.

[4] C. P. Auth and J. D. Plummer, "Scaling theory for cylindrical fully depleted, surrounding-gate MOSFETs," *IEEE Electron Device Lett.*, vol. 18, no. 2, pp. 74–76, Feb. 1997.

[5] D. J. Frank, Y. Taur, and H. S. P. Wong, "Generalized scale length for two-dimensional effects in MOSFETs," *IEEE Electron Device Lett.*, vol. 19, no. 10, pp. 385–387, Oct. 1998.

[6] S.-H. Oh, D. Monroe, and J. M. Hergenrother, "Analytical description of short-channel effects in fully depleted double-gate and cylindrical surrounding-gate MOSFETs," *IEEE Electron Device Lett.*, vol. 21, no. 9, pp. 445–447, Sep. 2000.

[7] S. D. Suk, S.-Y. Lee, S.-M. Kim, E.-J. Yoon, M.-S. Kim, M. Li, C. W. Oh, K. H. Yeo, S. H. Kim, D.-S. Shin, K.-H. Lee, H. S. Park, J. N. Han, C. J. Park, J.-B. Park, D.-W. Kim, D. Park, and B.-I. Ryu, "High performance 5 nm radius twin silicon nanowire MOSFET (TSNWFET): Fabrication on bulk Si wafer, characteristics, and reliability," in *IEDM Tech. Dig.*, 2005, pp. 717–720.

[8] K. H. Yeo, S. D. Suk, M. Li, Y.-Y. Yeoh, K. H. Cho, K.-H. Hong, S. K. Yun, M. S. Lee, N. Cho, K. Lee, D. Hwang, B. Park, D.-W. Kim, D. Park, and B.-I. Ryu, "Gate-all-around (GAA) twin silicon nanowire MOSFET (TSNWFET) with 15 nm length gate and 4 nm radius nanowires," in *IEDM Tech. Dig.*, 2006, pp. 539–542.

[9] S. D. Suk, M. Li, Y. Y. Yeoh, K. H. Yeo, K. H. Cho, I. K. Ku, H. Cho, W. J. Jang, D.-W. Kim, D. Park, and W.-S. Lee, "Investigation of nanowire size dependency on TSNWFET," in *IEDM Tech. Dig.*, 2007, pp. 891–894.

[10] D.-W. Kim, M. Li, K. H. Yeo, Y. Y. Yeoh, S. D. Suk, K. H. Cho, K. Oh, and W.-S. Lee, "Twin silicon nanowire FET (TSNWFET) on SOI with 8 nm silicon nanowires and 25 nm surrounding TiN gate," in *Proc. IEEE SOI Conf.*, 2008, pp. 117–118.

[11] A. Majumdar, Z. Ren, S. J. Koester, and W. Haensch, "Undoped-body, extremely thin SOI MOSFETs with back gates," *IEEE Trans. Electron Devices*, vol. 56, no. 10, pp. 2270–2276, Oct. 2009.

[12] S. Bangsaruntip, G. M. Cohen, A. Majumdar, Y. Zhang, S. U. Engelmann, N. C. M. Fuller, L. M. Gignac, S. Mittal, J. S. Newbury, M. Guillorn, T. Barwicz, L. Sekaric, M. M. Frank, and J. W. Sleight, "High performance and highly uniform gate-all-around silicon nanowire MOSFETs with wire size dependent scaling," in *IEDM Tech. Dig.*, 2009, pp. 297–300.

[13] C.-H. Lin, "Compact modeling of nanoscale CMOS," Ph.D. dissertation, Dept. Elect. Eng. Comput. Sci., Univ. California, Berkeley, CA, 2007.

[14] S. Wolf and R. N. Tauber, *Silicon Processing for the VLSI Era, Vol. 1: Process Technology*. Sunset Beach, CA: Lattice Press, 1999.

[15] A. Majumdar, X. Wang, A. Kumar, J. R. Holt, D. Dobuzinsky, R. Venigalla, C. Ouyang, S. J. Koester, and W. Haensch, "Gate length and performance scaling of undoped-body, extremely thin SOI MOSFETs," *IEEE Electron Device Lett.*, vol. 30, no. 4, pp. 413–415, Apr. 2009.