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9

10 UNITED STATES DISTRICT COURT  
11 NORTHERN DISTRICT OF CALIFORNIA  
12 SAN FRANCISCO DIVISION

13 YANGTZE MEMORY TECHNOLOGIES  
14 COMPANY, LTD.,

15 Plaintiff,

16 v.

17 MICRON TECHNOLOGY, INC., et al.,

18 Defendants.

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22 MICRON TECHNOLOGY, INC.,

23 Counterclaim Plaintiff,

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v.

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26 YANGTZE MEMORY TECHNOLOGIES  
COMPANY, LTD., and YANGTZE  
MEMORY TECHNOLOGIES, INC.,

27

Counterclaim Defendants.

28

Case No. 3:23-cv-05792-RFL

**COUNTERCLAIM PLAINTIFF  
MICRON TECHNOLOGY'S  
DISCLOSURE OF ASSERTED CLAIMS  
AND INFRINGEMENT  
CONTENTIONS AND DOCUMENT  
PRODUCTION ACCOMPANYING  
DISCLOSURE (PATENT LOCAL  
RULES 3-1 AND 3-2)**

Honorable Rita F. Lin

1 Pursuant to Patent Local Rules 3-1 and 3-2, Counterclaim Plaintiff Micron Technology, Inc.  
2 (“MTI”) hereby submits this Disclosure of Asserted Claims and Infringement Contentions for U.S.  
3 Patent Nos. 10,475,737 (the “737 patent”), 8,945,996 (the “996 patent”), 8,803,214 (the “214  
4 patent”), 10,872,903 (the “903 patent”), and 10,373,974 (the “974 patent”) (collectively, the  
5 “Asserted Patents”) asserted against counterclaim defendants Yangtze Memory Technologies  
6 Company, Ltd. (“YMTCL”), and Yangtze Memory Technologies, Inc. (“YMTI”) (collectively  
7 “YMTC”).

8 MTI bases these contentions on its current knowledge, understanding, and belief as to the  
9 facts and information available as of the date of these contentions. MTI has not yet completed its  
10 investigation, collection of information, discovery, or analysis relating to this action, and additional  
11 discovery, including discovery from YMTC and third parties, may lead MTI to further amend,  
12 revise, and/or supplement these contentions. Indeed, the accused functionalities relate to  
13 microscopic features, and the precise designs and fabrications methods thereof are held secret, at  
14 least in part, and are not publicly available in their entirety. As such, an analysis of non-publicly-  
15 available documentation and source code, including that of YMTC and/or third-parties may be  
16 necessary to fully and accurately describe every infringing functionality.

17 However, merits discovery in this action has barely begun and, as of the date of service of  
18 these contentions, is not scheduled to close until March 8, 2025. To date, YMTC has not produced  
19 documents responsive to MTI’s outstanding document requests, no depositions have been taken,  
20 and there has been no third-party discovery.

21 For at least these reasons, MTI specifically reserves the right to amend, revise and/or  
22 supplement these contentions and/or accompanying exhibits in accordance with any orders in this  
23 matter, Patent L.R. 3-6, and Federal Rule of Civil Procedure 26(e), as additional documents and  
24 information become available and as discovery and investigation proceed. MTI also reserves the  
25 right to supplement, modify, or amend these contentions to include additional products or services  
26 made, used, sold, or offered for sale in or imported into the United States by YMTC. The  
27 information in these contentions is not an admission regarding the scope of any claims or the proper  
28 construction of those claims or any terms contained therein, and MTI further reserves the right to

1 revise and/or supplement these contentions to address any claim constructions advanced as the case  
2 proceeds.

3 **I. Disclosure of Asserted Claims and Infringement Contentions**

4 **A. Identification of Accused Products Pursuant to Patent L.R. 3-1(b)**

5 Based on the information currently in its possession, MTI contends that the following  
6 YMTC products (and methods of making such products) (individually, “**Accused Product**” or  
7 collectively, “**Accused Products**”) infringe the Asserted Patents:

8 YMTC’s 64-layer 3D NAND storage technologies and products containing the same  
9 (collectively, the “YMTC 64L Accused Products”), including the X1-9050 and X2-9060, any  
10 YMTC 64-layer 3D NAND product, and other memory chips (and memory products containing  
11 the same) that have the same or similar structures, features, or functionalities, and/or are made by  
12 the same or similar Xtacking® technology manufacturing processes as the aforementioned  
13 exemplary products.

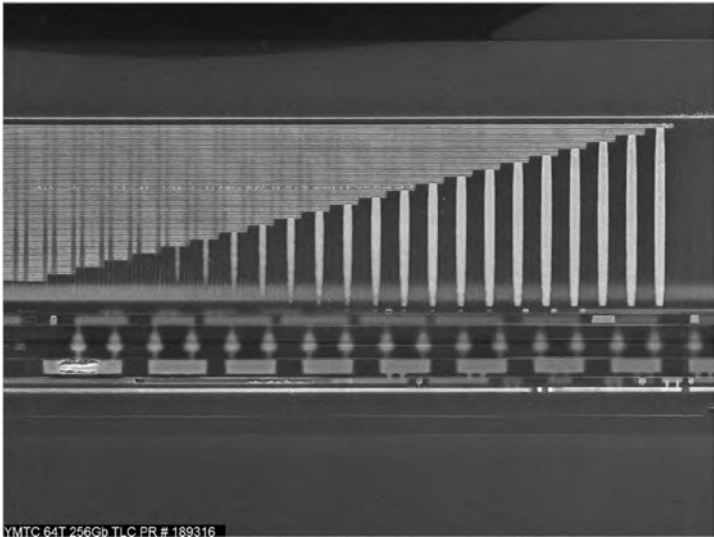
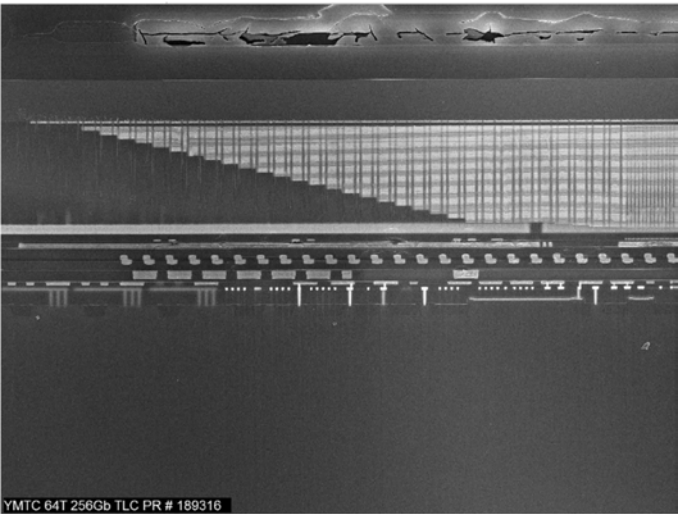
14 YMTC’s 128-layer 3D NAND storage technologies and products containing the same  
15 (collectively, the “YMTC 128L Accused Products”), including the X2-6070, any YMTC 128-  
16 layer 3D NAND product, and other memory chips (and memory products containing the same)  
17 that have the same or similar structures, features, or functionalities, and/or are made by the same  
18 or similar Xtacking® technology manufacturing processes as the aforementioned exemplary  
19 product.

20 YMTC’s 232-layer 3D NAND storage technologies and products containing the same  
21 (collectively, the “YMTC 232L Accused Products”), including the X3-9060, X3-9070, and X3-  
22 6070, any YMTC 232-layer 3D NAND product, and other memory chips (and memory products  
23 containing the same) that have the same or similar structures, features, or functionalities, and/or  
24 are made by the same or similar Xtacking® technology manufacturing processes as the  
25 aforementioned exemplary product.

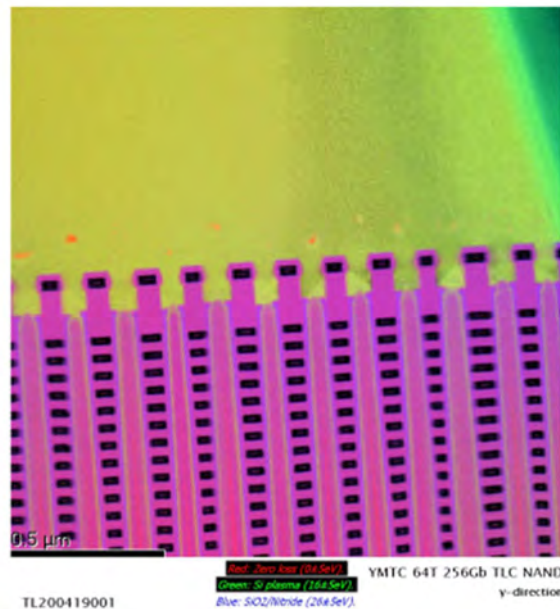
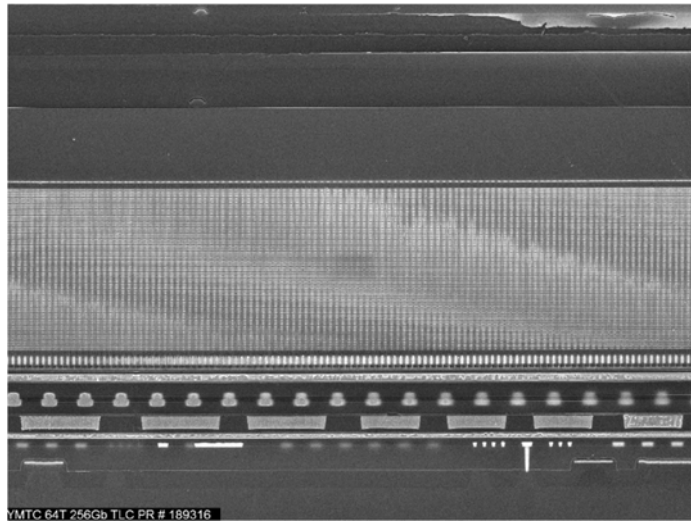
26 Upon information and belief, each of the YMTC 64L Accused Products, YMTC 128L  
27 Accused Products, and YMTC 232L Accused Products have the same or similar structures,  
28 features, or functionalities, and/or are made by the same or similar manufacturing processes

1 insofar as the structures, features, functionalities, and/or manufacturing processes of the Accused  
2 Products relate to the MTI Asserted Patents. Claim charts mapping a YMTC 1T 232L TLC  
3 product to the Asserted Claims of the Asserted Patents are provided as exhibits A-1, B-1, C-1,  
4 and E-1, and claim charts mapping the YMTC 512G 128L TLC product to the Asserted Claims of  
5 the Asserted Patents is provided as exhibits A-2, B-2, C-2, D-2, and E-2.

6 The YMTC 128L is representative of the YMTC 64L for the purposes of the Asserted  
7 patents. For example, the YMTC 256G 64L TLC product contains staircase regions with contacts  
8 and dummy structures that extend through word lines of the memory array structure in the same  
9 way as in the YMTC 512G 128L TLC product as shown in the images below:

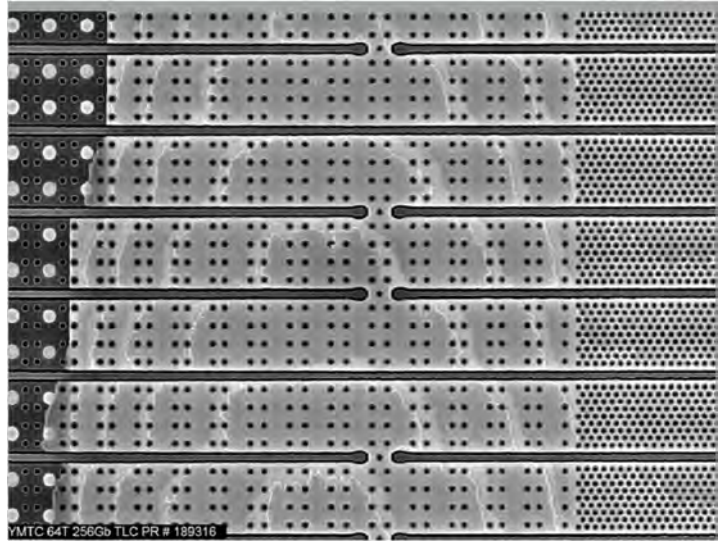


1 Further, the YMTC 256G 64L TLC product contains a memory storage array portion that  
2 is configured in the same way as the memory storage array portion of the YMTC 512G 128L  
3 TLC product:

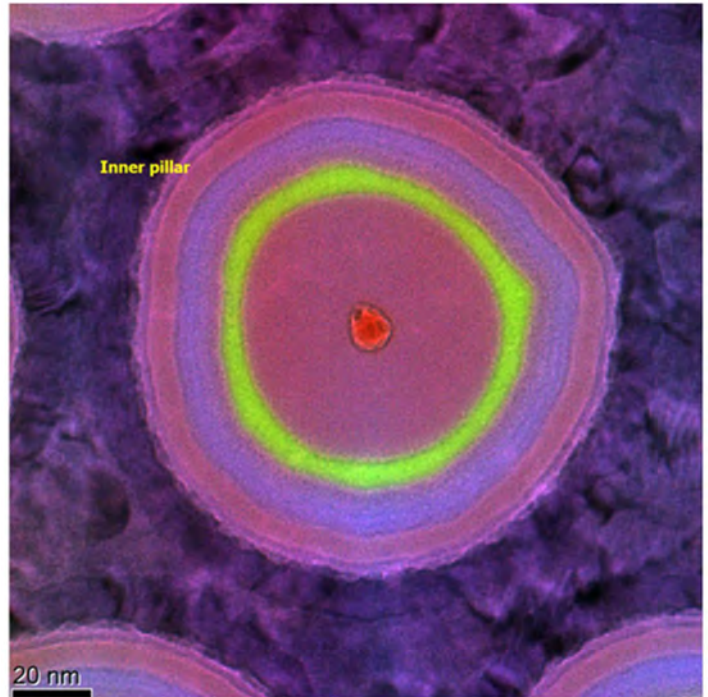


25 Further, the staircase contact regions, select gate regions, and array regions in the YMTC  
26 256G 64L TLC product are configured the same way as they are in the YMTC 512G 128L TLC  
27 product. For example, both have elongated slots that extend from the array portion to the  
28 staircase portion and that are used to remove sacrificial material prior to forming word lines:

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Lastly, the cell structure of the memory cells in the YBTC 256G 64L TLC product is identical, at least for the purposes of the Asserted Patents, to the cell structure of the memory cells in the YBTC 512G 128L TLC product:



TL200419001 Red: Zero loss (0±5eV) YBTC 64T 256Gb TLC NAND  
Green: Si plasma (16±5eV) planar, middle of pillar  
Blue: SiO<sub>2</sub>/Nitride (26±5eV)

1 Further, some product lines such as the YMTC 232L may include products that use, for  
2 example, triple level cells (TLC) or quad level cells (QLC); however, for the purpose of the  
3 Asserted Patents, such differences are immaterial.

4 **B. Identification of Asserted Claims Pursuant to Patent L.R. 3-1(a)**

5 Based on the information currently in its possession, MTI contends that YMTC infringes  
6 the following claims (collectively, the “Asserted Claims”). MTI expressly reserves the right to  
7 amend and/or supplement its identification of Asserted Claims should discovery (including  
8 YMTC’s technical documentation, source code, and witnesses) reveal additional, relevant  
9 information.

U.S. Patent No.	Asserted Claims
10,475,737	1-7, 9, 10-12, 14, 15, 18, 20, 21, and 22
8,945,996	1-4, 6-10, 12, 13, 16, 17, 18, 22-26, 28, 30, and 32
8,803,214	1-12 and 14-20
10,872,903	1-3, 5, 7-9, and 17-20
10,373,974	1, 4, 5, 7, 9, and 11-19

15  
16 **i. Direct Infringement Under 35 U.S.C. § 271(a) & § 271(g)**

17 MTI contends that YMTCL and YMTI have directly infringed, and continue to directly  
18 infringe, the Asserted Claims of the Asserted Patents, both individually and as a single enterprise,  
19 and literally or under the doctrine of equivalents, at least by offering to sell, selling, using, and/or  
20 importing into the United States the YMTC 64L Accused Products and the 128L Accused  
21 Products.

22 MTI contends that YMTCL and YMTI have directly infringed, and continue to directly  
23 infringe, the Asserted Claims of the ’717, ’996, ’214, and ’974 Patents, both individually and as a  
24 single enterprise, and literally or under the doctrine of equivalents, at least by offering to sell,  
25 selling, using, and/or importing into the United States the YMTC 232L Accused Products.

26 Further, MTI contend that the ’996 Patent and ’974 Patent are directly infringed, both  
27 individually and as a single enterprise, and literally or under the doctrine of equivalents, under 35  
28 U.S.C. § 271(g) at least because the Accused Products are made overseas by a process covered by

1 the Asserted Claims of the Asserted Patents and are offered for sale, sold, and/or imported into  
2 the United States.

3 In addition to the detailed claims charts demonstrating YMTC's infringement attached as  
4 exhibits A-1 through C-1 and E-1, and A-2 through E-2, at least the following facts support  
5 YMTC's direct infringement of the Asserted Patents:

6 **Sale or Importation in the U.S.:** On May 22, 2020, YMTCL declared to the USPTO that  
7 it sold or transported 3D NAND chips in commerce regulated by U.S. Congress since at least as  
8 early as September 9, 2016. Counterclaims<sup>1</sup>, Ex. 36 at 4; 15 U.S.C. § 1127 (defining “use in  
9 commerce” as when “the goods are sold or transported in commerce” and “commerce” as “all  
10 commerce which may lawfully be regulated by Congress”); Trademark Manual of Examining  
11 Procedure § 901.03 (“Use of a mark in a foreign country does not give rise to rights in the United  
12 States if the goods or services are not sold or rendered in the United States.”). Specifically, in  
13 connection with YMTCL's trademark filing for its YMTC mark, YMTCL declared under penalty  
14 of perjury that “the mark is in use in commerce on or in connection with all the goods/services in  
15 the application” and that “[t]he specimen(s) shows the mark as used on in connection with the  
16 goods ... in commerce.” Counterclaims, Ex. 36 at 6. YMTCL attached specimens showing its  
17 Xtacking® chips (Counterclaims, Ex. 6 at 8-9), which are 3D NAND memory chips that Micron  
18 accuses of infringement (*id.*, Ex. 37 at 2). Thus for these reasons, MTI, on information and  
19 belief, contends that YMTC has sold, offered for sale, or imported 3D NAND memory chips in  
20 the U.S. or between the U.S. and a foreign nation (*i.e.* imported from China).<sup>2</sup>

21 **Sales in California:** Mr. David Duffin identifies himself as “US General Manager and  
22 Head of International Customer Sales at Yangtze Memory Technologies,” in Santa Clara and San  
23 Jose, California, since March 2019. Counterclaims ¶¶ 24-26, Ex. 31 at 2. In his description of  
24 that role, he states that he is “responsible for \$5B+ in shipments per year” and that he is “used to  
25 regularly and directly interacting with customers,” among other things. *Id.* Although he does not

26 <sup>1</sup> “Counterclaims” as used herein refers to Defendants’ Answer to First Amended Complaint and  
27 Counterclaims (Dkt. 35).

28 <sup>2</sup> Micron did not allege that YMTC makes the accused products in the U.S. Thus, it is plausible  
to infer that acts of transportation in the U.S. must begin with an infringing importation.

1 specify which YMTC entity is his current employer, he states that at least from 2016-2019, he  
2 worked for “Yangtze Memory Technologies Co.” (*i.e.* YMTCL), which is the Chinese parent  
3 company of YMTI. *Id.* And YMTI identifies Mr. Duffin as its Chief Executive Officer and  
4 Secretary in its California Secretary of State filings. *Id.*, Ex. 32 at 2. It is proper to infer that he  
5 holds a role with both YMTC entities. Thus, YMTC’s Head of International Customer Sales,  
6 responsible for billions of dollars of shipments and customer interaction, operates in this District.  
7 Therefore, MTI contends, on information and belief, that YMTC sells, offers for sale, and  
8 provides customer support for accused products in the U.S. *Id.* ¶¶ 16-18.

9 **Use and Importation in California:** Mr. Duffin states that he worked at YMTCL as  
10 “Vice President Product & Test Engineering” from May 2016 to March 2019. Counterclaims,  
11 Ex. 31 at 2-3. He led “all product, test and assembly engineering for YMTC” in San Jose,  
12 California. Based on this description, it is reasonable to infer that YMTC has imported products  
13 into the U.S. for testing and used those products (e.g., tested them) in the U.S. Thus, on  
14 information and belief, MTI has concluded that the Accused Products are used and imported into  
15 the United States.

16 **YMTC Launched and Showed Accused Products in California:** “In August 2018,  
17 YMTC officially launched its ground-breaking Xtacking® architecture at the Flash Memory  
18 Summit, and won the ‘Best of Show’ award” in Santa Clara, California. Counterclaims Ex. 37 at  
19 7; Ex. 25 at 4 (“In 2018, [CEO Simon Yang] showed off the company’s technology at the Flash  
20 Memory Summit in California.”); *see also* Dkt. 29 (“YMTCL’s FAC”) ¶¶ 7, 25, Exs. 38, 39.  
21 Based on these representations regarding product launch, trade show attendance, and technology  
22 demonstration, MTI believes that YMTC has imported and used the Accused Products to solicit  
23 customers in the U.S.

24 **YMTC Participates in a Global Market of 3D NAND Sales:** YMTC participates in the  
25 global 3D NAND market, which includes the U.S.:

- 26 • In YMTCL’s own Complaint, “YMTC admits that it is ‘dedicated to the development of  
27 memory products for the *global market*’ and that it ‘*maintains ties to Silicon Valley*  
28 through a wholly-owned subsidiary, Yangtze Memory Technologies, Inc.’” Counterclaims

- 1 ¶ 29 (emphasis added); YMTCL’s FAC ¶¶ 8, 24, Ex. 36 (YMTC’s office in Santa Clara,  
2 California is one of its “Globalized R&D System and Market Locations”).
- 3 • “YMTC has become the world’s sixth-biggest maker of NAND flash memory by output,  
4 with about *5% of the global market*[,]” as of 2021. Counterclaims, Ex. 25 at 4.
  - 5 • “CEO [Simon Yang] worked to bring *YMTC to the global stage*.” *Id.*, Ex. 25 at 4.
  - 6 • “Yangtze Memory Technologies” Deputy General Counsel and Head of IP Department,  
7 Daniel (Tuenlap) Chan sits in Richardson, Texas, from where he helps “navigate through  
8 complex issues for advancing *YMTC’s competitive position in the global memory supply*  
9 *chain*.” *Id.*, Ex. 35 at 2. Mr. Chan stated that YMTC’s “patent portfolio is designed to  
10 protect our innovations in *markets that matter to YMTC* and its partners.” *Id.* ¶ 29, Ex.  
11 34 at 3. In suing Micron in California, YMTC “allege[s] that its *rival* was using its  
12 patented innovations to *force YMTC out of the 3D NAND flash memory market*.” *Id.*

13 Based on these representations about YMTC’s position in the global market, MTI believes that  
14 YMTC sells, offers for sale, and uses the Accused Products in, and imports the Accused Products  
15 into, the U.S.

16 **ii. Induced Infringement Under 35 U.S.C. § 271(b)**

17 MTI contends that each Accused Product infringes each Asserted Claim of the Asserted  
18 Patents, and that YMTC has actively, knowingly, and intentionally induced (and continues to  
19 actively, knowingly, and intentionally induce) others to directly infringe the Asserted Claims in  
20 various ways, at least by selling and importing devices containing the Accused Products in  
21 violation of 35 U.S.C. § 271(b). MTI incorporates its discussion of YMTC’s U.S. activities in  
22 Section I(B)(i) above. In addition to those facts, the following facts further support that YMTC  
23 has actively, knowingly, and intentionally induced (and continues to actively, knowingly, and  
24 intentionally induce) others to directly infringe the Asserted Claims:

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1           **Lexar Products Containing the Accused Products Are Available in the U.S.:** Before  
2 filing its Counterclaims, Micron purchased Lexar solid state memory devices that contain the  
3 YMTC accused products and shipped them to counsel’s offices in this District. Counterclaims,  
4 Ex. 28-30. Micron attached to the Counterclaims multiple articles demonstrating that the Lexar  
5 products contain YMTC accused products. *Id.* Thus, MTI is informed and believes that Lexar is  
6 a customer of YMTC and that products containing YMTC’s accused products are sold and  
7 imported into the U.S. *Id.*

8           **YMTC’s Website and Customer Support in the U.S.:** MTI is informed and believes  
9 that the YMTC Entities actively encourage others, such as their customers and distributors, to  
10 make, use, offer to sell, import, supply, or otherwise distribute into the United States the Accused  
11 Products and products containing the Accused Products. Counterclaims ¶ 22. YMTC describes  
12 the applications for which the accused products can be used, which include “enterprise servers,  
13 data centers, and other fields to meet the diversified needs for data storage in the era of 5G and  
14 AI,” and provides product specifications on the YMTC website, which is accessible in the U.S.  
15 (*id.*, Ex. 38); provides instructions and encouragement for such use (*id.* ¶ 22); designs its products  
16 to comply with U.S. safety standards (*id.* ¶ 23); and provides such materials in the English  
17 language (*id.*, Ex. 38). Based on this, the Court can infer that YMTC’s intended audience  
18 includes U.S. customers or potential customers. Indeed, YMTC’s website identifies its office in  
19 Santa Clara, California as one of its “Globalized R&D System *and Market Locations.*”  
20 YMTCL’s FAC ¶¶ 8, 24, Ex. 36 (emphasis added). And YMTC’s “US General Manager and  
21 Head of International Customer Sales” is located in California as discussed in greater detail  
22 above.

23           YMTCL and YMTI have had knowledge of their infringement at least since the filing of  
24 the MTI’s Counterclaims.

25           **C.     Infringement Claim Charts Pursuant to Patent L.R. 3-1(c)**

26           Based on the information currently in its possession, MTI contends that the following  
27 claim charts specify where each limitation of each Asserted Claim is found within each Accused  
28 Instrumentality (whether literally or under the Doctrine of Equivalents):

1           Exhibit A-1 & A-2: Infringement of '737 Patent

2           Exhibit B-1 & B-2: Infringement of '996 Patent

3           Exhibit C-1 & C-2: Infringement of '214 Patent

4           Exhibit D-2: Infringement of '903 Patent

5           Exhibit E-1 & E-2: Infringement of '974 Patent

6           YMTC has not provided MTI with full discovery regarding its products, including non-  
7 public documentation describing the Accused Instrumentalities, detailed written discovery  
8 responses, or testimony from YMTC's witnesses. Thus, MTI expressly reserves its right to amend  
9 and/or supplement these assertions or to asserted additional claims for infringement under Patent  
10 L.R. 3-6 as discovery in this case progresses or as otherwise permitted by the Court.

11           **D. Identification of Indirect Infringement Pursuant to Patent L.R. 3-1(d)**

12           Based on the information currently in its possession, MTI contends that YMTC is liable  
13 for indirect infringement of each of the Asserted Claims under 35 U.S.C. §§ 271(b). MTI has  
14 identified the acts of direct infringement and provided a description of YMTC's own acts that  
15 induce such direct infringement above (§ I(B)(i) & (ii)), as well as in MTI's Answer and  
16 Counterclaims (Dkt. No. 35), which are incorporated by reference in their entirety.

17           **E. Identification of Types of Infringement Pursuant to Patent L.R. 3-1(e)**

18           Based on the information currently in its possession, MTI contends that the Accused  
19 Products satisfy each limitation of each Asserted Claim both literally and under the doctrine of  
20 equivalents.

21           **F. Identification of Priority Dates Pursuant to Patent L.R. 3-1(f)**

22           With respect to claiming priority to an earlier application, MTI contends that: (a) each  
23 Asserted Claim of the '737 Patent is entitled to a priority date no later than April 12, 2011; (b)  
24 each Asserted Claim of the '966 Patent is entitled to a priority date no later than April 12, 2011;  
25 (c) each Asserted Claim of the '214 Patent is entitled to a priority date no later than June 28,  
26 2010; (d) each Asserted Claim of the '903 Patent is entitled to a priority date no later than June  
27 28, 2010; (e) each Asserted Claim of the '974 Patent is entitled to a priority date no later than  
28 Nov. 16, 2015.

1           **G. Identification of Practicing Instrumentalities Pursuant to Patent L.R. 3-1(g)**

2           Pursuant to L.R. 3-1(g), MTI states that MTI’s 130 series and beyond practice one or  
3 more claims of the ’996 patent.

4           MTI states that MTI’s 130 series and beyond practice one or more claims of the ’737  
5 patent.

6           MTI states that MTI’s 110 series and beyond practice one or more claims of the ’214  
7 patent.

8           MTI states that MTI’s 130 series and beyond practice one or more claims of the ’974  
9 patent.

10          The parties have been conferring about a protective order for this case that takes into  
11 account the fact that YMTC is a listed entity on the U.S. Department of Commerce Entity List.  
12 Once an appropriate protective order is in place, MTI will supplement its disclosure to identify  
13 particular claims, which will necessarily disclose technical information about the structure or  
14 fabrication of Micron’s products. Micron sent YMTC a final proposal on May 2, 2024 and  
15 indicated that it was prepared to submit the parties’ protective order proposal and remaining  
16 disputed issues to the Court. Micron is awaiting a further response from YMTC.

17           **H. Identification of First Infringement and Damages Period Pursuant to Patent  
18 L.R. 3-1(h)**

19          Based on the information currently in its possession, MTI contends that YMTC’s  
20 infringement of the Asserted Patents began at least as early as the dates set forth below. To MTI’s  
21 knowledge, YMTC’s infringement remains ongoing and the damages period likewise remains  
22 ongoing.

U.S. Patent No.	Date of First Infringement & Start of Damages Period
10,475,737	At least as early as November 2019
8,945,996	At least as early as 2018
8,803,214	At least as early as 2018
10,872,903	At least as early as December 2020
10,373,974	At least as early as August 2019

27          Discovery is ongoing and MTI has sought technical and sales information from YMTC

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1 regarding the Accused Products, as that information is in YMTC's possession, custody, or  
2 control. As of service of this document, MTI has not received substantive responses to its  
3 discovery requests from YMTC. MTI reserves the right to supplement its Infringement  
4 Contentions based on YMTC's discovery responses, and other documents and information  
5 produced in discovery. MTI further reserves its right to amend and/or modify its Infringement  
6 Contentions as discovery in this case progresses, under Patent L.R. 3-6, or as the Court otherwise  
7 permits.

8 **I. Identification of Willful Infringement Bases Pursuant to Patent L.R. 3-1(i)**

9 MTI contends that YMTC has willfully infringed each Asserted Claim of each Asserted  
10 Patent at least since the filing of the counterclaims in this action. Since at least the filing of  
11 MTI's Counterclaims, which identified the Asserted Patents and attached detailed charts  
12 demonstrating infringement, YMTC has been on notice of MTI's patents and claims of  
13 infringement. Moreover, YMTC had knowledge of Micron's 3D NAND patents from the large  
14 number of YMTC 3D NAND engineers who previously worked on 3D NAND development at  
15 Micron among other facts. Counterclaims ¶¶ 31, 32, 39, 50, 60, 70, 80. Thus, MTI expects that  
16 discovery will reveal that YMTC knew of the Asserted Patents and YMTC's unauthorized use  
17 thereof before filing of the Counterclaims. YMTC's infringement remains ongoing.

18 Moreover, discovery that YMTC has not yet produced may provide additional evidence  
19 which shows that YMTC has willfully infringed the Asserted Patents. MTI therefore reserves its  
20 right to amend and/or modify its willful infringement contentions as discovery in this case  
21 progresses, under Patent L.R. 3-6, or as the Court otherwise permits.

22 **II. Document Production & Accompanying Disclosure**

23 **A. Documents Pursuant to Patent L.R. 3-2(a)**

24 MTI is not currently aware of any documents responsive to Patent L.R. 3-2(a). MTI's  
25 discovery and investigation are ongoing.

26 **B. Documents Pursuant to Patent L.R. 3-2(b)**

27 The parties have been conferring about a protective order for this case that takes into  
28 account the fact that YMTC is a listed entity on the U.S. Department of Commerce Entity List.

1 Once an appropriate protective order is in place, MTI will supplement its document production  
2 with excerpts of technical lab notebooks. Micron sent YMTC a final proposal on May 2, 2024,  
3 and indicated that it was prepared to submit the parties' protective order proposal and remaining  
4 disputed issues to the Court. Micron is awaiting a further response from YMTC.

5 **C. Documents Pursuant to Patent L.R. 3-2(c)**

6 Pursuant to Patent L.R. 3-2(c), MTI has produced documents bearing production numbers  
7 MYM0000048 - MYM0000429; MYM0004678 - MYM0004915; MYM0004943 -  
8 MYM0005111; MYM0005714 - MYM0005899; and MYM0006291 - MYM0006448; *see*  
9 *generally* MYM0000001 - MYM0006448.

10 **D. Documents Pursuant to Patent L.R. 3-2(d)**

11 Pursuant to Patent L.R. 3-2(d), MTI has produced documents bearing production numbers  
12 MYM0006449 - MYM0020687.

13 **E. Documents Pursuant to Patent L.R. 3-2(e)**

14 As noted above, the parties have been conferring about a protective order for this case that  
15 takes into account the fact that YMTC is a listed entity on the U.S. Department of Commerce  
16 Entity List. Once an appropriate protective order is in place, MTI will supplement its technical  
17 document production. MTI will also make available for inspection MTI source code materials  
18 that demonstrates the structure and fabrication of the MTI products identified above pursuant to  
19 L.R. 3-1(g) pursuant to the source code inspection procedures that the parties are negotiating in  
20 connection with the protective order.

21 **F. Documents Pursuant to Patent L.R. 3-2(f)**

22 Although MTI is not aware of any agreements that transfer any ownership interest in the  
23 Asserted Patents, for the avoidance of doubt, MTI has produced the assignment records filed with  
24 the USPTO for each asserted patent bearing production numbers MYM0006449 - MYM0020687

25 **G. Documents Pursuant to Patent L.R. 3-2(g)**

26 MTI is currently not aware of any documents responsive to Patent L.R. 3-2(g). Micron's  
27 discovery and investigation are ongoing.

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**CERTIFICATE OF SERVICE**

I am employed in the County of San Mateo, State of California. I am over the age of 18 years old and not a party to this action. My business address is Orrick, Herrington & Sutcliffe LLP, 1000 Marsh Road, Menlo Park, California 94025. On May 6, 2024, I served the **DEFENDANT AND COUNTERCLAIM PLAINTIFF MICRON TECHNOLOGY’S DISCLOSURE OF ASSERTED CLAIMS AND INFRINGEMENT CONTENTIONS** on all interested parties to this action in the manner described as follows:

- (VIA U.S. MAIL)** On May 6, 2024, by placing a true copy of the document(s) listed above in an envelope, with postage thereon fully prepaid, addressed as set forth below and then sealing the envelope and depositing it in the U.S. mail at Menlo Park, California.
- (VIA EMAIL)** On May 6, 2024, via electronic mail in Adobe PDF format the document(s) listed above to the electronic address(es) set forth below.
- (VIA OVERNIGHT-FED EX)** I caused the within document(s) to be delivered by overnight courier to the address(es) set forth below.

Allen S. Cross (Bar. No. 303665) allen.cross@ropesgray.com James R. Batchelder (Bar No. 136347) james.batchelder@ropesgray.com Andrew T. Radsch (Bar No. 303665) andrew.radsch@ropesgray.com James F. Mack (Bar No. 322056) james.mack@ropesgray.com Nancy N. Attalla (Bar No. 341070) nancy.attalla@ropesgray.com Rachel Bacha (NYB No. 4817938) rachael.bacha@ropesgray.com ymtc-micron-ropes-service@ropesgray.com <b>ROPES &amp; GRAY LLP</b> 1900 University Avenue, 6th Floor East Palo Alto, CA 94303-2284 Telephone: (650) 617-4000
<b><i>Counsel for Plaintiff, Yangtze Memory Technologies Company, Ltd.</i></b>

I declare under penalty of perjury under the laws of the State of California and the United States that the foregoing is true and correct.

Executed on May 6, 2024, at San Mateo, California.

/s/Matthew Bonini  
Matthew Bonini

EXHIBIT C-2

**Infringement Chart for U.S. Patent No. 8,803,214 (the “’214 patent”)**

The following chart provides non-limiting examples, without the benefit of claim construction or discovery, of how YMTC’s Accused Products (as that term is defined in the accompanying cover pleading) meet every limitation, literally or under the doctrine of equivalents, of claims of U.S. Patent No. 8,803,214. The referenced images are images from a 128L YMTC 512G TLC part. Micron re-serves the right to amend, correct, supplement, or otherwise change its explanation of how YMTC’s Accused Products meet the following claim limitations, including as the claims are construed, as discovery progresses, or as Micron’s investigation continues. Micron takes no position on claim interpretation or scope at this time.

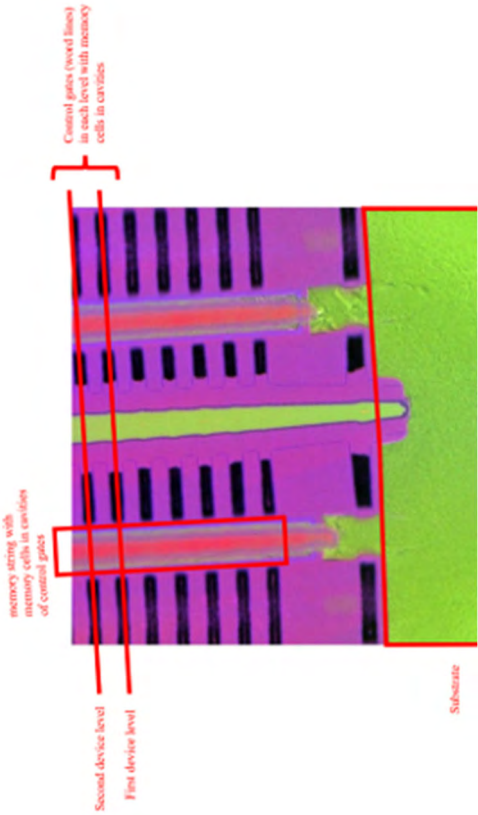
’214 Patent Claim	YMTC 128L 3D NAND MEMORY (“YMTC 128L”)
[1.PRE] An apparatus comprising:	<p>YMTC 128L is an apparatus. Specifically, as shown below, the YMTC 128L includes a semiconductor apparatus:</p> 
[1.A] a substrate of a memory device;	YMTC 128L has a substrate of a memory device. Specifically, as shown below, the YMTC 128L includes a substrate that supports multiple memory strings:

EXHIBIT C-2

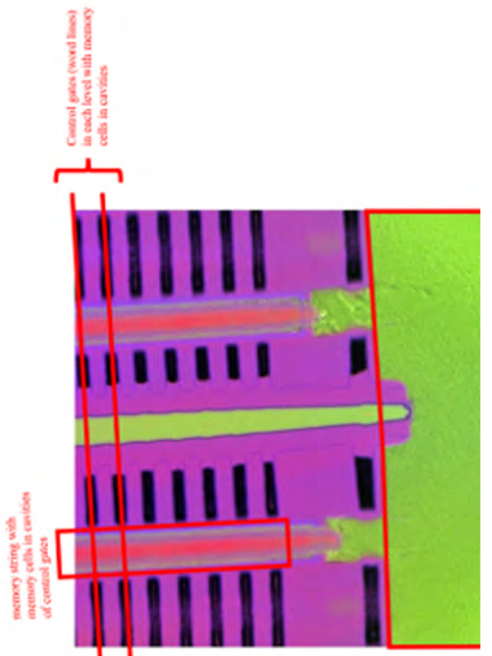
'214 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
<p>[1.B] a plurality of first memory cells located in a first device level of the memory device over the substrate. Specifically, as shown below, the YMTC 128L includes multiple device levels (each control gate (e.g., word line) with memory cells in the cavities):</p>	 <p>The diagram illustrates a cross-section of the YMTC 128L 3D NAND memory. It shows a substrate at the bottom with multiple device levels stacked on top. The first device level is highlighted in purple, and the second device level is highlighted in green. Memory strings are shown as vertical structures with cavities containing memory cells. Control gates (word lines) are shown as horizontal lines in each device level. Labels indicate the memory strings, control gates, and the substrate.</p>

EXHIBIT C-2

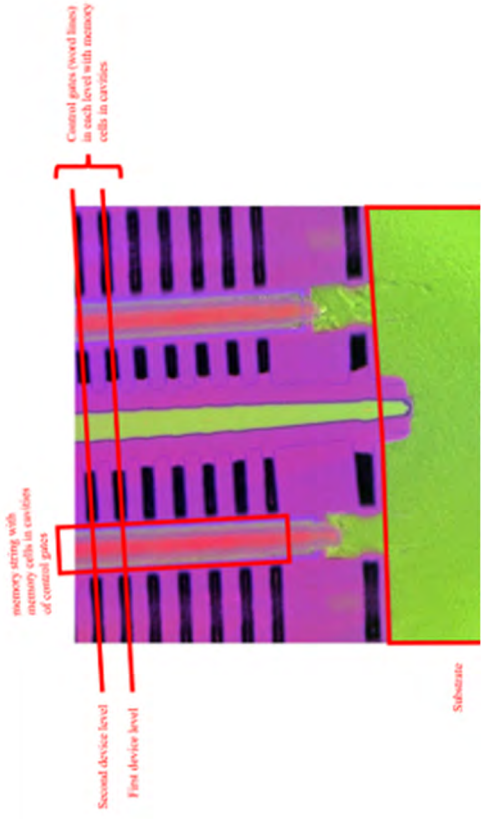
'214 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
<p>[1.C] a plurality of second memory cells located in a second device level over the first device level and over the substrate, wherein the first device level is different from the second device level. Specifically, as shown below, the YMTC 128L includes multiple device levels (each control gate (e.g., word line) with memory cells in the cavities):</p>	 <p>Note that the '214 Patent explains that: "The term 'on', 'over', or 'overlying' does not imply any directionality as used herein unless otherwise explicitly stated as such." 8,803,214 Patent at 5:30-38.</p>
<p>[1.C] a plurality of second memory cells located in a second device level over the first device level and over the substrate, wherein the first device level is different from the second device level;</p>	<p>YMTC 128L has a plurality of second memory cells located in a second device level of the memory device over the first device level and over the substrate, wherein the first device level is different from the second device level. Specifically, as shown below, the YMTC 128L includes multiple device levels (each control gate (e.g., word line) with memory cells in the cavities):</p>

EXHIBIT C-2

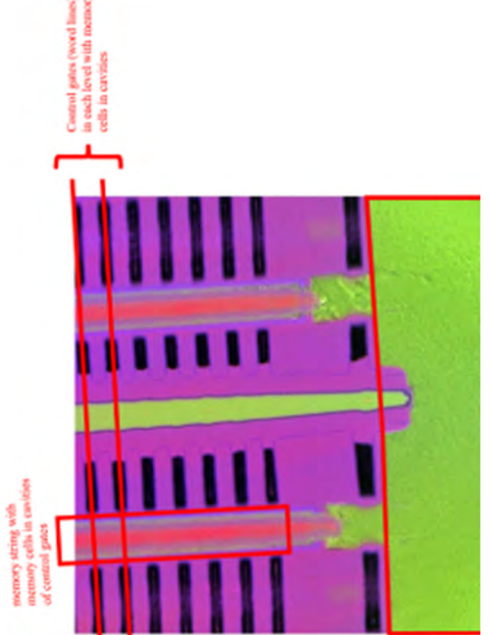
<p><b>'214 Patent Claim</b></p>	<p><b>YMTC 128L 3D NAND MEMORY ("YMTC 128L")</b></p>
<p>[1.D] a first control gate formed in the first device level, the first control gate to control access to the first memory cells, wherein each of the first memory cells includes a memory element formed in a cavity of the first control gate. Specifically, as shown below, the YMTC 128L includes in each device level, a control gate (e.g., word line) that is used to select memory cells, wherein in cavities of the control gate (e.g., word line) are memory elements (e.g., respective memory cells for that level of the memory strings):</p>	 <p>Note that the '214 Patent explains that: "The term 'on', 'over', or 'overlying' does not imply any directionality as used herein unless otherwise explicitly stated as such." 8,803,214 Patent at 5:30-38.</p>
<p>[1.D] a first control gate formed in the first device level, the first control gate to control access to the first memory cells, wherein each of the first memory cells includes a memory element formed in a cavity of the first control gate. Specifically, as shown below, the YMTC 128L includes in each device level, a control gate (e.g., word line) that is used to select memory cells, wherein in cavities of the control gate (e.g., word line) are memory elements (e.g., respective memory cells for that level of the memory strings):</p>	<p>YMTC 128L has a first control gate formed in the first device level, the first control gate to control access to the first memory cells, wherein each of the first memory cells includes a memory element formed in a cavity of the first control gate. Specifically, as shown below, the YMTC 128L includes in each device level, a control gate (e.g., word line) that is used to select memory cells, wherein in cavities of the control gate (e.g., word line) are memory elements (e.g., respective memory cells for that level of the memory strings):</p>

EXHIBIT C-2

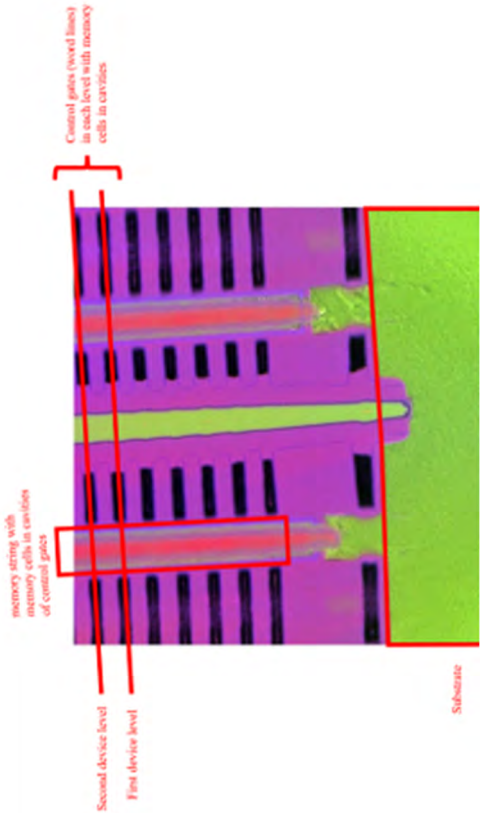
'214 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
<p>[1.E] a second control gate formed in the second device level, the second control gate to control access to the second memory cells, wherein each of the second memory cells includes a memory element formed in a cavity of the second control gate. Specifically, as shown below, the YMTC 128L includes in each device level, a control gate (e.g., word line) that is used to select memory cells, wherein in cavities of the control gate (e.g., word line) are memory elements (e.g., respective memory cells for that level of the memory strings):</p>	
<p>[1.E] a second control gate formed in the second device level, the second control gate to control access to the second memory cells, wherein each of the second memory cells includes a memory element formed in a cavity of the second control gate; and</p>	<p>YMTC 128L has a second control gate formed in the second device level, the second control gate to control access to the second memory cells, wherein each of the second memory cells includes a memory element formed in a cavity of the second control gate. Specifically, as shown below, the YMTC 128L includes in each device level, a control gate (e.g., word line) that is used to select memory cells, wherein in cavities of the control gate (e.g., word line) are memory elements (e.g., respective memory cells for that level of the memory strings):</p>

EXHIBIT C-2

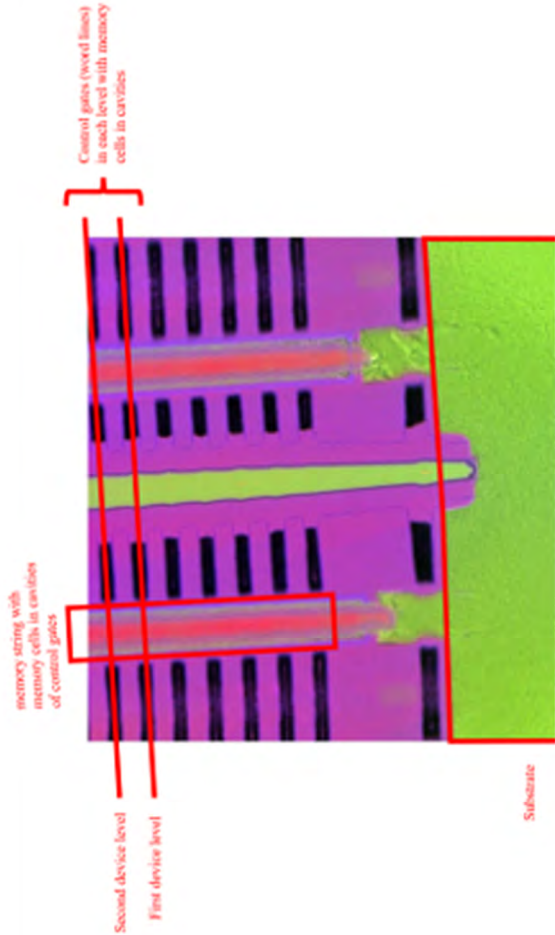
'214 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
<p>[1.F] data lines configured to be selectively coupled to a common source and the memory cells through conductive material. Specifically, as shown below, the YMTC 128L includes data lines that selectively couples, e.g., through select gate transistor devices (e.g., shown below on top and bottom of stack), through conductive material (e.g., semiconductor pillar and metal material interconnects) to both a common source and memory cells, e.g., during accesses to the memory cells:</p>	
	<p>YMTC 128L has data lines configured to be selectively coupled to a common source and the memory cells through conductive material. Specifically, as shown below, the YMTC 128L includes data lines that selectively couples, e.g., through select gate transistor devices (e.g., shown below on top and bottom of stack), through conductive material (e.g., semiconductor pillar and metal material interconnects) to both a common source and memory cells, e.g., during accesses to the memory cells:</p>

EXHIBIT C-2

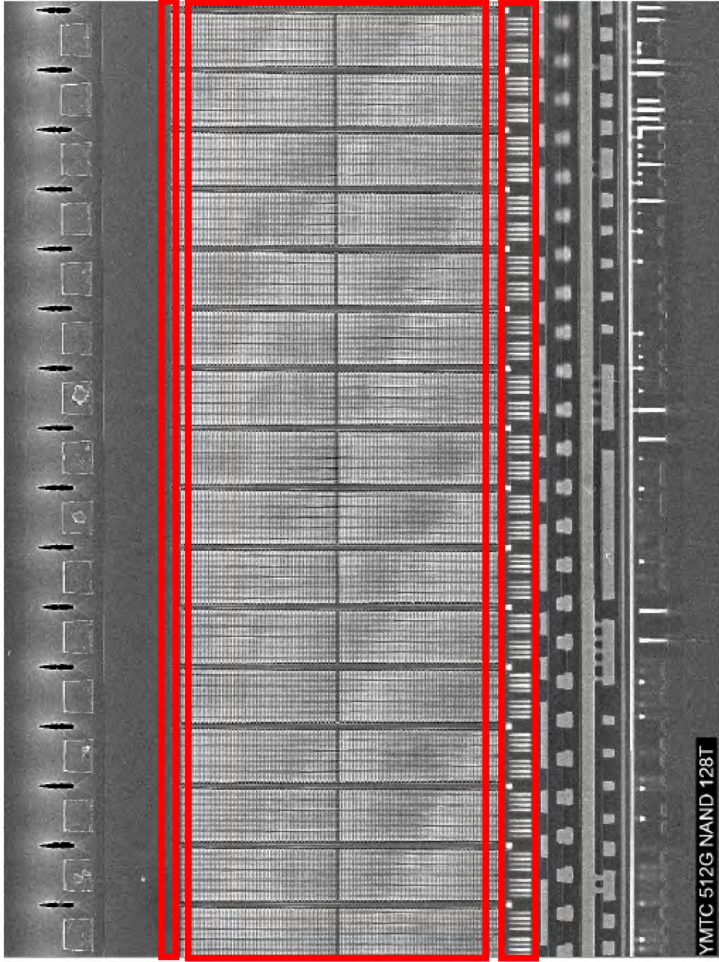
'214 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
	 <p>Common source</p> <p>Memory cells of memory cell strings containing conductive material</p> <p>Data lines</p> <p>YMTC 512G NAND 128T</p>
[2.A] The apparatus of claim 1, wherein the first and second memory cells include multiple memory cells arranged in a first direction and multiple memory cells arranged in a second direction and multiple	<p>YMTC describes the connections between the data lines, common source, and memory array in U.S. Pat. No. 10,937,806 at 6:36-56.</p> <p>YMTC 128L has the apparatus of claim 1, wherein the first and second memory cells include multiple memory cells arranged in a first direction and multiple memory cells arranged in a second direction.</p>

EXHIBIT C-2

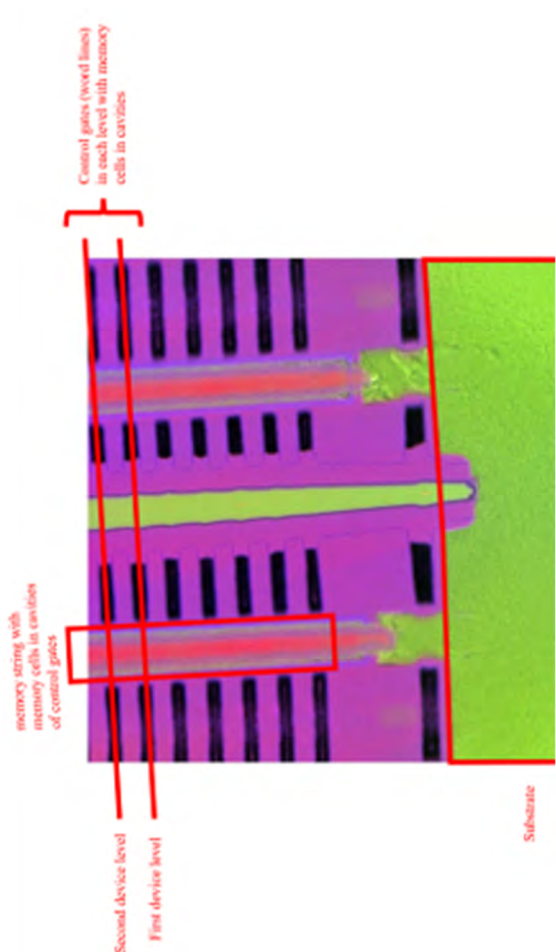
	<p>YMTC 128L 3D NAND MEMORY (“YMTC 128L”)</p>
<p><b>'214 Patent Claim</b> memory cells arranged in a second direction,</p>	 <p>The diagram shows a cross-section of a 3D NAND memory array. It features a substrate at the bottom. Two device levels are shown: the 'First device level' and the 'Second device level'. Memory cells are arranged in a grid. Control gates are located in cavities between the memory cells. Labels include: 'memory array with memory cells in cavities of control gates', 'Second device level', 'First device level', 'Control gates (word lines) in each level with memory cells in cavities', and 'Substrate'.</p> <p>YMTC's NAND memory array is three-dimensional and therefore for a given level memory cells will be arranged in a plane. As such, there will be multiple memory cells in any two planar directions.</p>

EXHIBIT C-2

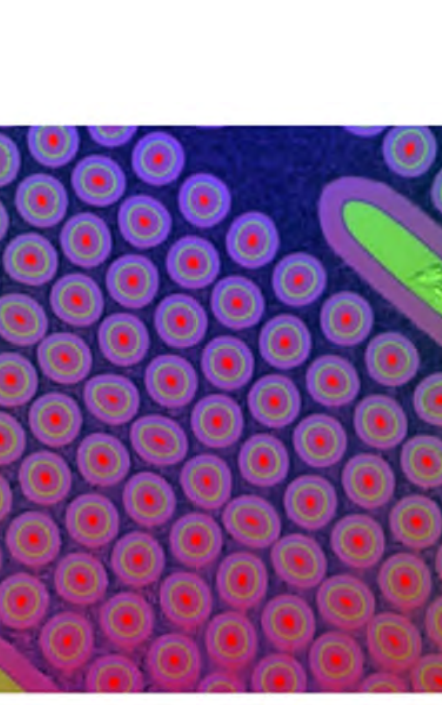
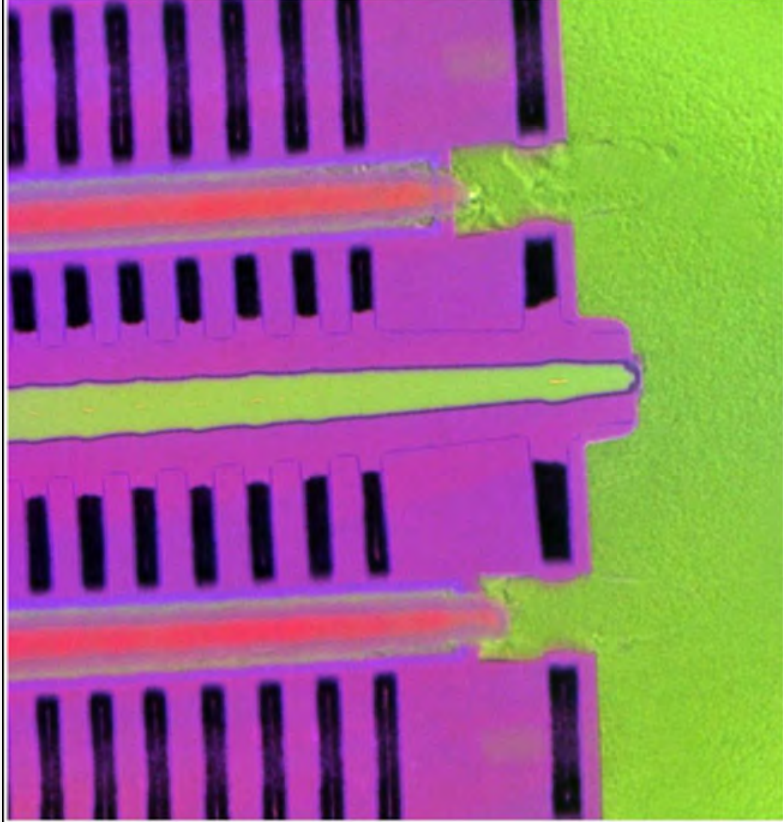
'214 Patent Claim	YMTC 128L 3D NAND MEMORY ('YMTC 128L')
<p>[2.B] the conductive material extending through the first and second memory cells in a third direction, the third direction being substantially perpendicular to the first and second directions.</p>	 <p>YMTC 128L has the conductive material extending through the first and second memory cells in a third direction, the third direction being substantially perpendicular to the first and second directions.</p> <p>The conductive material of the memory cell strings is substantially perpendicular to any horizontal cross-section of the memory array.</p>

EXHIBIT C-2

<p>'214 Patent Claim</p>	<p>YMTC 128L 3D NAND MEMORY ("YMTC 128L")</p>
	

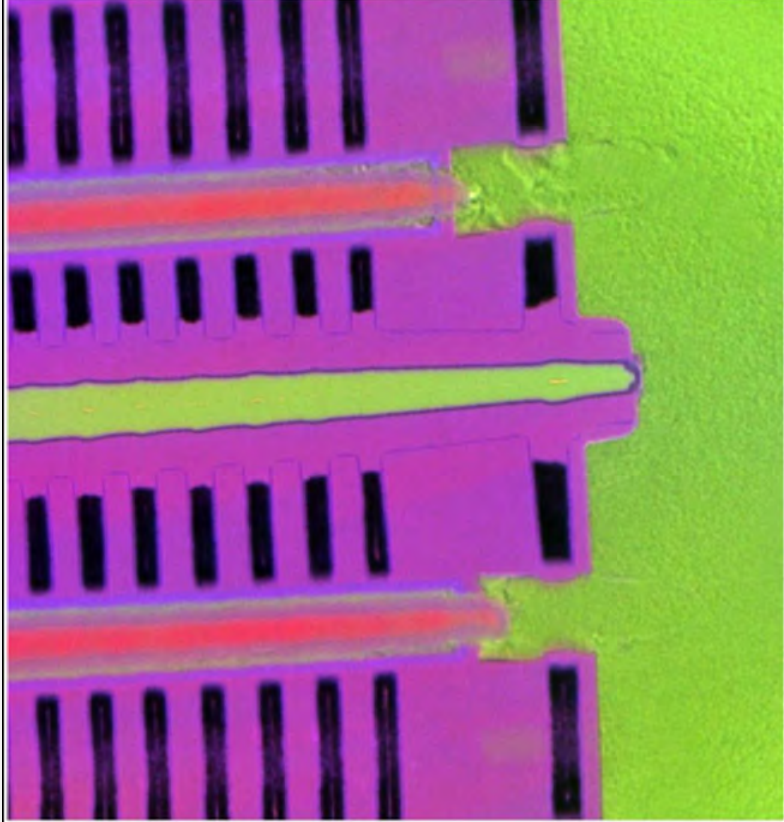


EXHIBIT C-2

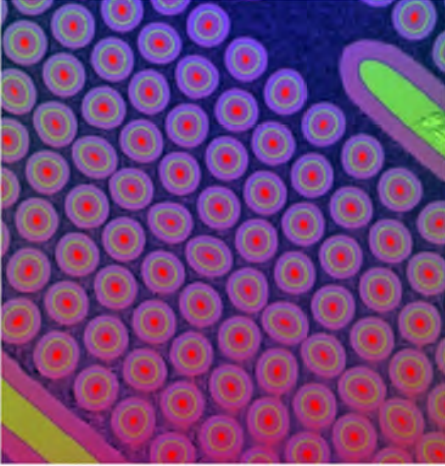
'214 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
<p>[3] The apparatus of claim 2, wherein the common source is formed over a substrate of the memory device, such that the common source is between the first and second memory cells and the substrate to allow electrons from the memory element of at least one of the first and second memory cells to move to the common source during an erase operation.</p>	 <p>YMTC 128L has the apparatus of claim 2, wherein the common source is formed over a substrate of the memory device, such that the common source is between the first and second memory cells and the substrate to allow electrons from the memory element of at least one of the first and second memory cells to move to the common source during an erase operation.</p> <p>One ordinary skill in the art understands that during, an erase operation, electrons are allowed to flow from programmed memory cells to the common source to allow erasing of the memory cells.</p>
<p>[3] The apparatus of claim 2, wherein the common source is formed over a substrate of the memory device, such that the common source is between the first and second memory cells and the substrate to allow electrons from the memory element of at least one of the first and second memory cells to move to the common source during an erase operation.</p>	

EXHIBIT C-2

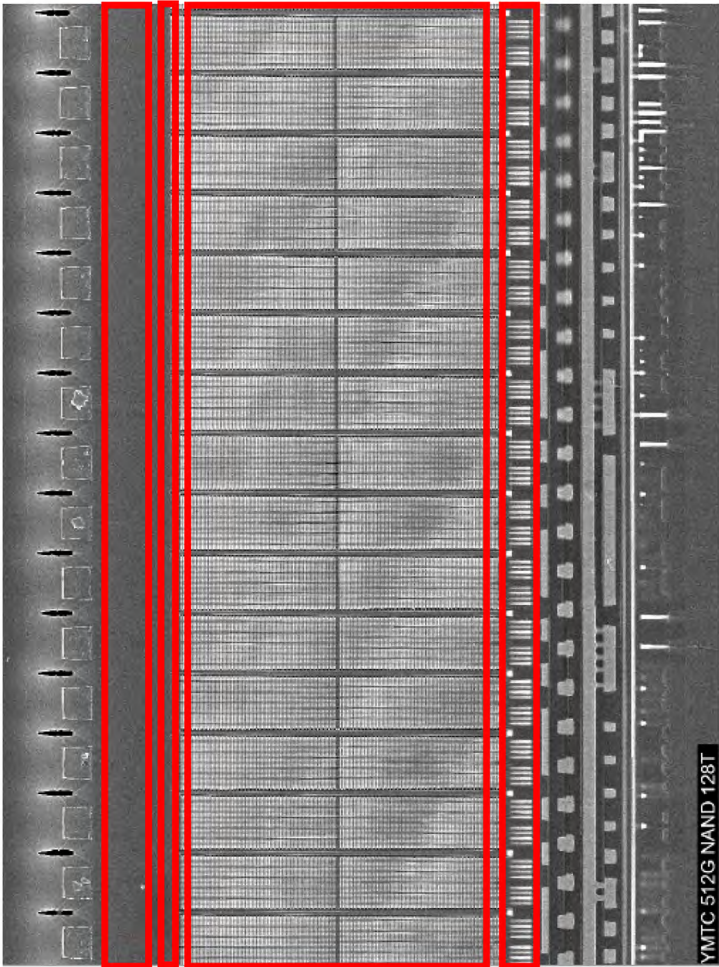
<p>'214 Patent Claim</p>	<p>YMTC 128L 3D NAND MEMORY ("YMTC 128L")</p>
<p>Substrate</p> <p>Common source</p> <p>Memory cells of memory cell strings containing conductive material</p> <p>Data lines</p>  <p>YMTC 512G NAND 128T</p>	<p>YMTC 128L has the apparatus of claim 1, wherein the first memory cells are substantially vertically aligned with the second memory cells. Specifically, as shown below, numerous of the memory cells are substantially vertically aligned with numerous of the other memory cells.</p>
<p>[4] The apparatus of claim 1, wherein the first memory cells are substantially vertically aligned with the second memory cells.</p>	<p>YMTC 128L has the apparatus of claim 1, wherein the first memory cells are substantially vertically aligned with the second memory cells. Specifically, as shown below, numerous of the memory cells are substantially vertically aligned with numerous of the other memory cells.</p>

EXHIBIT C-2

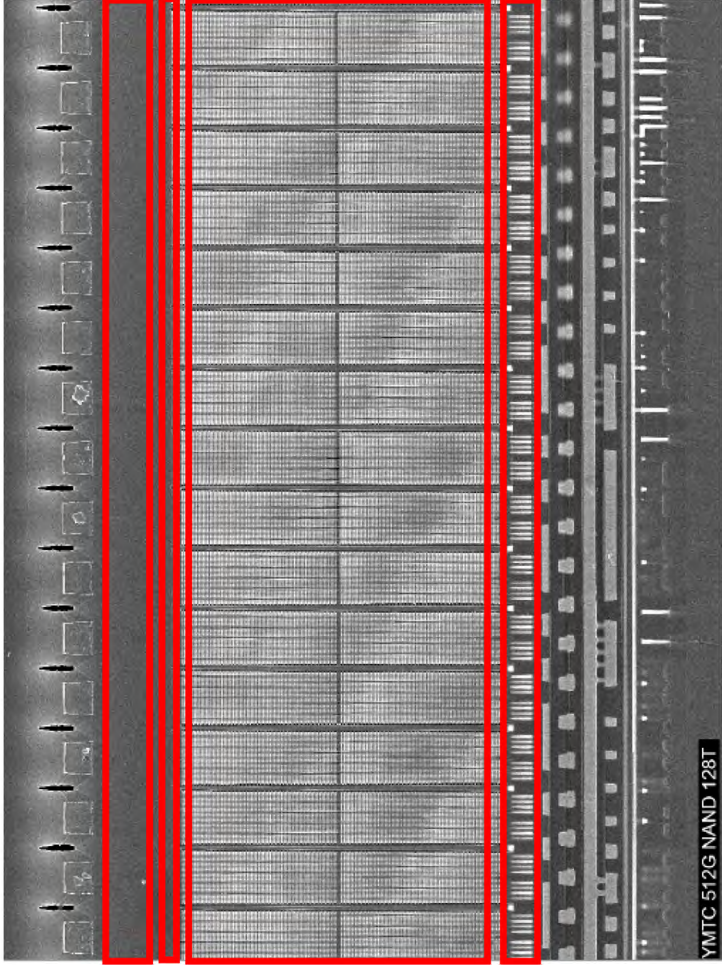
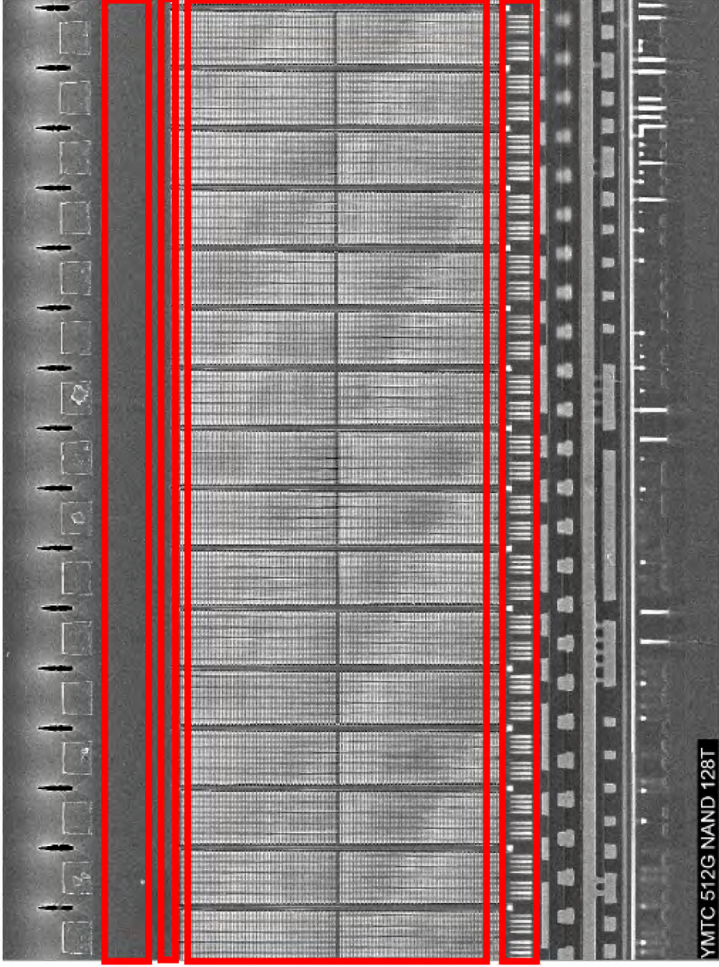
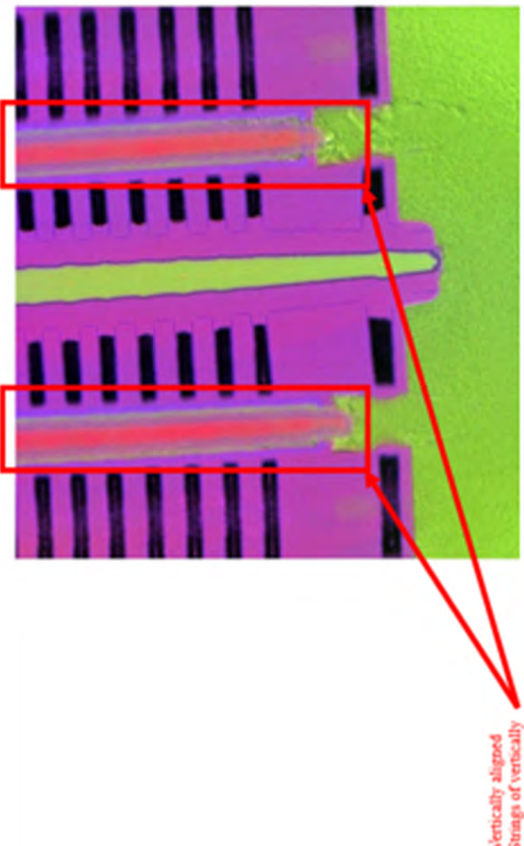
'214 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
	 <p>Substrate</p> <p>Common source</p> <p>Memory cells of memory cell strings containing conductive material</p> <p>Data lines</p> <p>YMTC 512G NAND 128T</p>
<p>[5] The apparatus of claim 1, wherein the memory element of each of the first memory cells is substantially vertically aligned with the memory element of one of the second memory cells. Specifically, each element, including the memory elements of the substantially vertically aligned memory cells is also substantially vertically aligned.</p>	<p>YMTC 128L has the apparatus of claim 1, wherein the memory element of each of the first memory cells is substantially vertically aligned with the memory element of one of the second memory cells. Specifically, each element, including the memory elements of the substantially vertically aligned memory cells is also substantially vertically aligned.</p>

EXHIBIT C-2

'214 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
	 <p>Substrate</p> <p>Common source</p> <p>Memory cells of memory cell strings containing conductive material</p> <p>Data lines</p> <p>YMTC 512G NAND 128T</p>

'214 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
	
<p>[6] The apparatus of claim 1, further comprising transistors to selectively couple the first and second memory cells to the data lines associated with the first and second memory cells during a memory operation of the memory device, wherein at least one of the transistors comprises a double-gate.</p>	<p>On information and belief, YMTC 128L has the apparatus of claim 1, upon information and belief, further comprising transistors to selectively couple the first and second memory cells to the data lines associated with the first and second memory cells during a memory operation of the memory device, wherein at least one of the transistors comprises a double-gate.</p> <p>For example, YMTC discusses the use of “double-gate” transistors in its memory peripheral in US20220367505, [0091].</p>
<p>[7] The apparatus of claim 1, further comprising transistors to selectively couple the first</p>	<p>On information and belief, YMTC 128L has the apparatus of claim 1, upon information and belief, further comprising transistors to selectively couple the first and second memory cells to the data</p>

<p><b>'214 Patent Claim</b></p>	<p><b>YMTC 128L 3D NAND MEMORY (“YMTC 128L”)</b></p>
<p>and second memory cells to the data lines associated with the first and second memory cells during a memory operation of the memory device, wherein at least one of the transistors comprises a surrounded gate.</p>	<p>lines associated with the first and second memory cells during a memory operation of the memory device, wherein at least one of the transistors comprises a surrounded gate.</p> <p>For example, YMTC discusses the use of “gate all around” transistors in its memory peripheral in US20220367505, [0091].</p>
<p>[8.PRE] An apparatus comprising:</p>	<p>YMTC 128L is an apparatus.</p> <p>See [1.PRE], <i>supra</i>.</p>
<p>[8.A] a plurality of first memory cells located in a first device level of a memory device;</p>	<p>YMTC 128L has a plurality of first memory cells located in a first device level of a memory device.</p> <p>See [1.B], <i>supra</i>.</p>
<p>[8.B] a plurality of second memory cells located in a second device level of the memory device;</p>	<p>YMTC 128L has a plurality of second memory cells located in a second device level of the memory device.</p> <p>See [1.C], <i>supra</i>.</p>
<p>[8.C] a first control gate formed in the first device level, the first control gate to control access to the first memory cells, wherein each of the first memory cells includes a memory element formed in a cavity of the first control gate;</p>	<p>YMTC 128L has a first control gate formed in the first device level, the first control gate to control access to the first memory cells, wherein each of the first memory cells includes a memory element formed in a cavity of the first control gate.</p> <p>See [1.D], <i>supra</i>.</p> <p>Each identified memory cell has a memory element for storing information in the form of electrical charge.</p>

EXHIBIT C-2

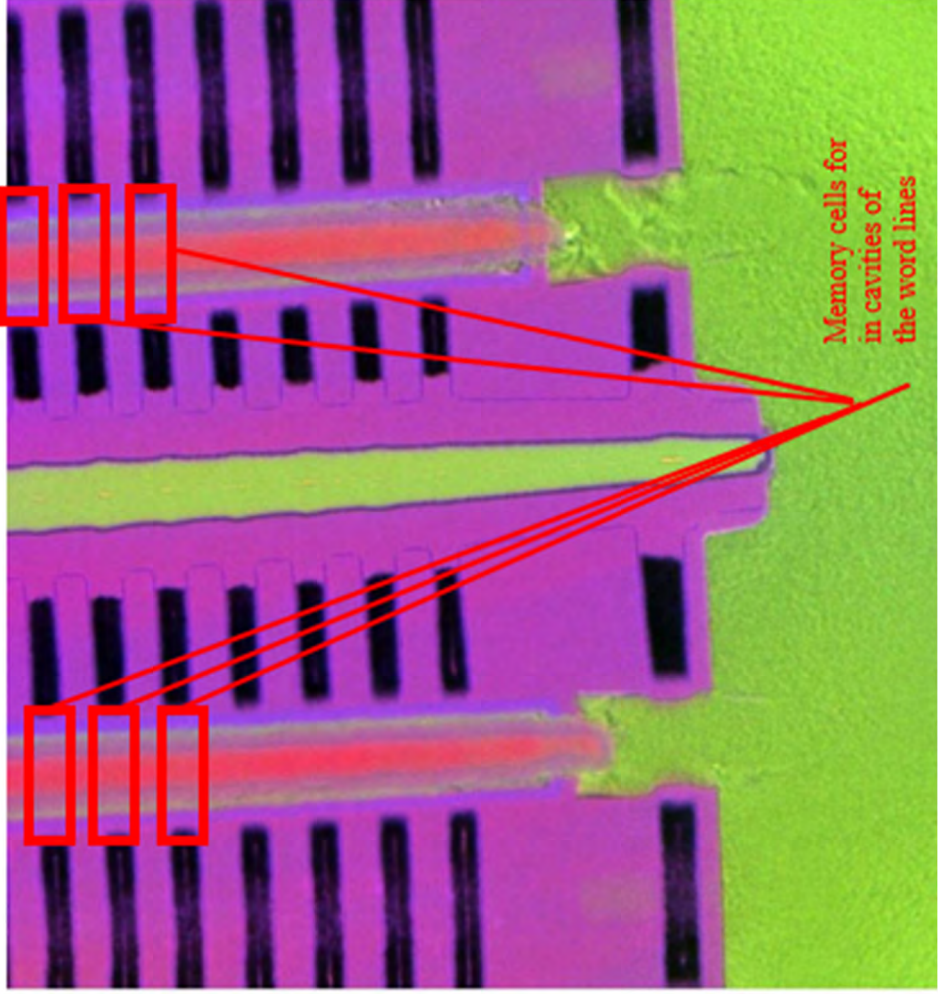
'214 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
 <p>Memory cells for in cavities of the word lines</p>	<p>YMTC 128L has a second control gate formed in the second device level, the second control gate to control access to the second memory cells, wherein each of the second memory cells includes a memory element formed in a cavity of the second control gate, wherein the first and second</p>
<p>[8.D] a second control gate formed in the second device level, the second control gate to control access to the second memory cells, wherein each of the second memory cells includes a memory element formed in a cavity of the second control gate, wherein the first and second</p>	<p>memory cells, wherein each of</p>

EXHIBIT C-2

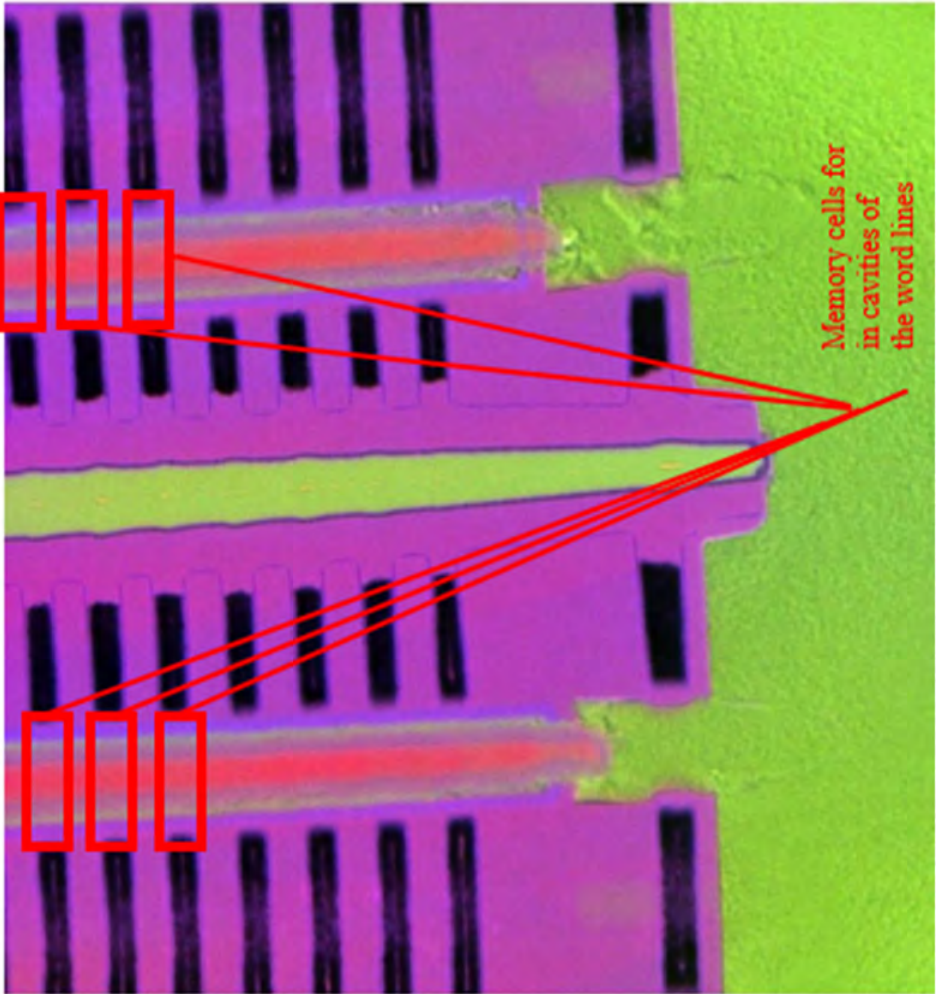
<p><b>'214 Patent Claim</b></p> <p>the second memory cells includes a memory element formed in a cavity of the second control gate, wherein the first and second memory cells include multiple memory cells arranged in a first direction and multiple memory cells arranged in a second direction;</p>	<p><b>YMTC 128L 3D NAND MEMORY ("YMTC 128L")</b></p>
<p>memory cells include multiple memory cells arranged in a first direction and multiple memory cells arranged in a second direction.</p> <p>See [2.A], <i>supra</i>, regarding multiple memory cells arranged in multiple directions.</p>	 <p>The image is a false-color scanning electron micrograph (SEM) of a 3D NAND memory array. It shows a grid of memory cells. The cells are arranged in a first direction (vertical) and a second direction (horizontal). Red boxes highlight specific cells in both directions. Red lines connect these boxes to a magnified view of the cells, which shows the cavities of the word lines. A red text label points to these cavities, stating: "Memory cells for in cavities of the word lines".</p>

EXHIBIT C-2

'214 Patent Claim	YMTC 128L 3D NAND MEMORY (“YMTC 128L”)
[8.E] a common source; and	YMTC 128L has a common source.  <i>See</i> [1.F], <i>supra</i> .
[8.F] data lines configured to be selectively coupled to the common source and the first and second memory cells through conductive material, the conductive material extending through the first and second memory cells in a third direction, the third direction being substantially perpendicular to the first and second directions, wherein the common source is formed over a substrate of the memory device, such that the first and second memory cells are between the common source and the substrate.	YMTC 128L has data lines configured to be selectively coupled to the common source and the first and second memory cells through conductive material, the conductive material extending through the first and second memory cells in a third direction, the third direction being substantially perpendicular to the first and second directions, wherein the common source is formed over a substrate of the memory device, such that the first and second memory cells are between the common source and the substrate.  <i>See</i> [1.F], [2.B], [3], <i>supra</i> .
[9.PRE] An apparatus comprising:	YMTC 128L is an apparatus.  <i>See</i> [1.PRE], <i>supra</i> .
[9.A] a first non-volatile memory cell including a first memory element, the first memory element having a ring shape, the first memory element located in a first device level of a memory device, the first memory element located in a first device level of a memory device. The YMTC 128L is NAND flash memory and the memory cells thereof are non-	YMTC 128L has a first non-volatile memory cell including a first memory element, the first memory element having a ring shape, the first memory element located in a first device level of a memory device. The YMTC 128L is NAND flash memory and the memory cells thereof are non-

EXHIBIT C-2

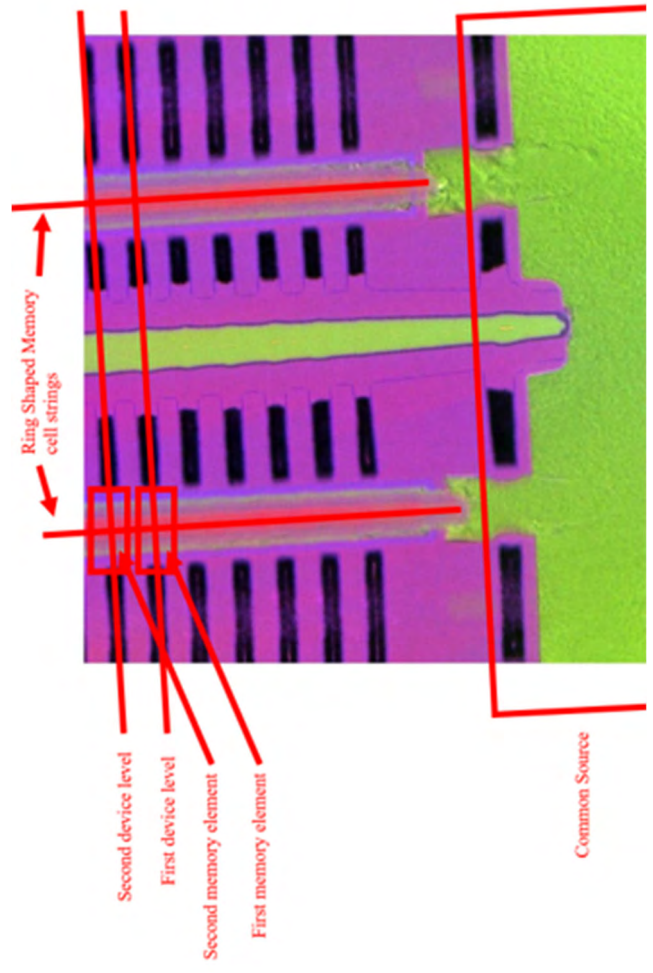
<p><b>'214 Patent Claim</b></p> <p>memory element having a ring shape, the first memory element located in a first device level of a memory device;</p>	<p><b>YMTC 128L 3D NAND MEMORY (“YMTC 128L”)</b></p> <p>volatile because they are designed to store information even when the memory device is not powered.</p>  <p>Below is a cross-section of the ring-shaped memory cell strings above:</p>
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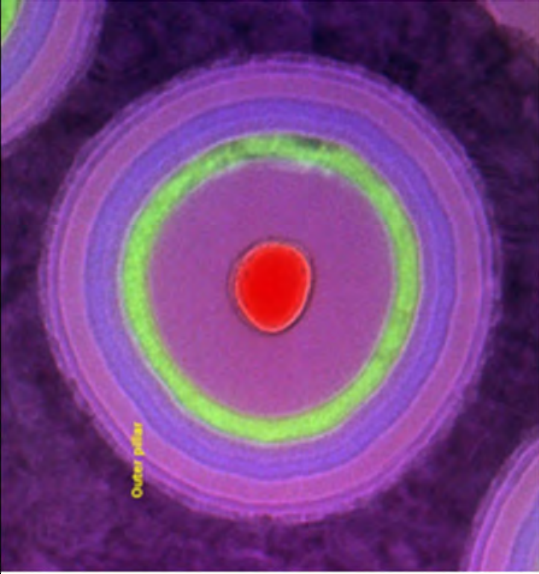
'214 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
<p>[9.B] a second non-volatile memory cell including a second memory element, the second memory element having a ring shape, the second memory element located in a second device level of the memory device, wherein the first device level is different from the second device level;</p>	 <p>YMTC 128L has a second non-volatile memory cell including a second memory element, the second memory element having a ring shape, the second memory element located in a second device level of the memory device, wherein the first device level is different from the second device level.</p>

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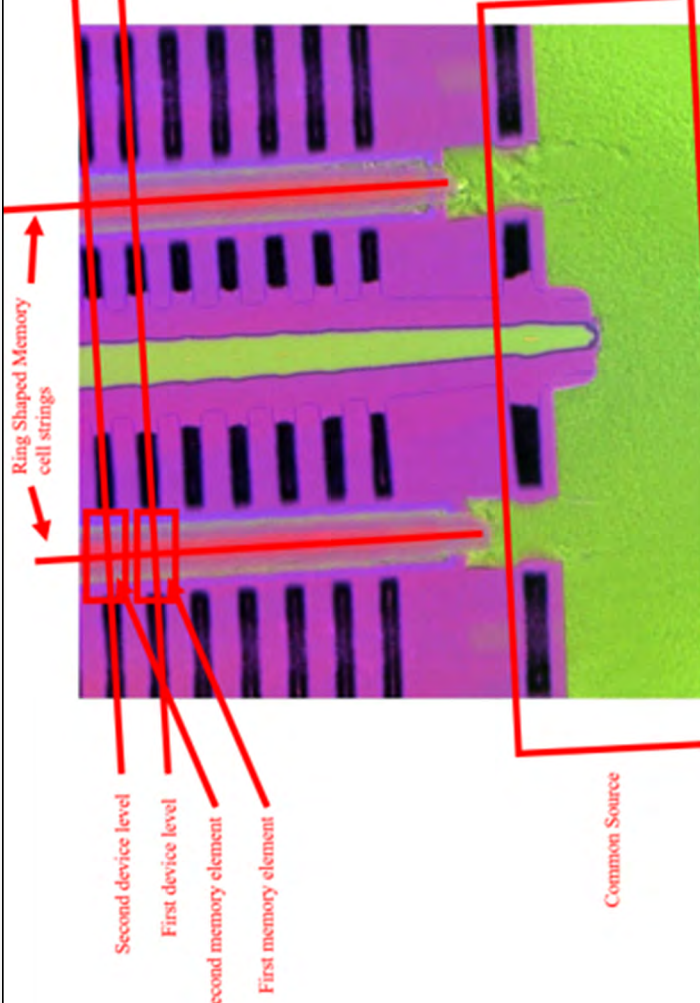
<b>'214 Patent Claim</b>	<b>YMTC 128L 3D NAND MEMORY ("YMTC 128L")</b>
	 <p>Below is a cross-section of the ring-shaped memory cell strings above:</p>

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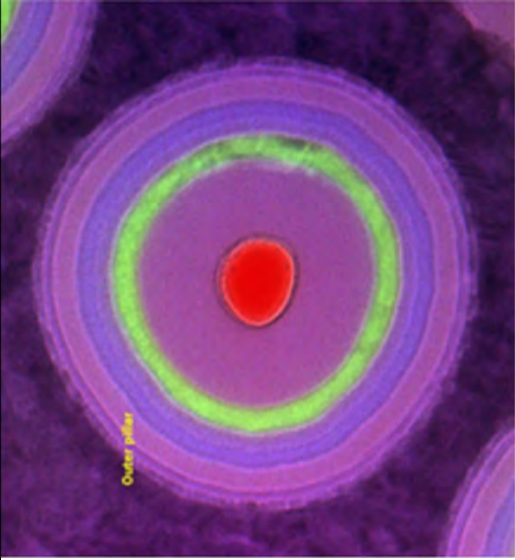
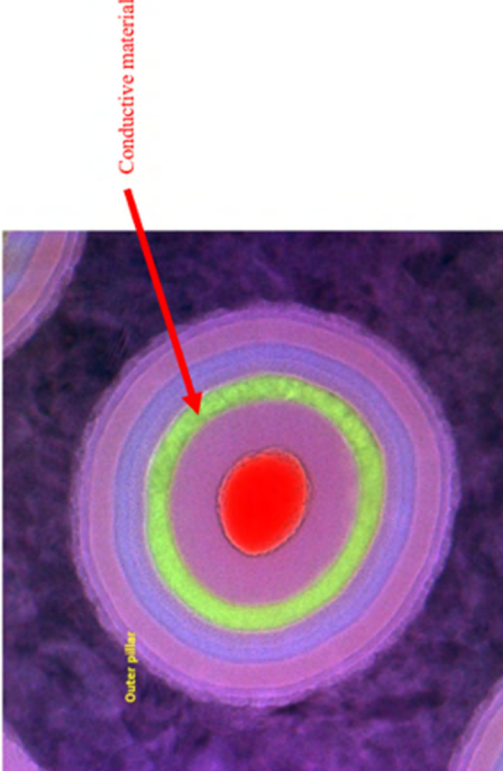
<b>'214 Patent Claim</b>	<b>YMTC 128L 3D NAND MEMORY ("YMTC 128L")</b>
	
<p>[9.C] a conductive material extending through the first and second memory elements; and</p>	<p>YMTC 128L has a conductive material extending through the first and second memory elements.</p> 

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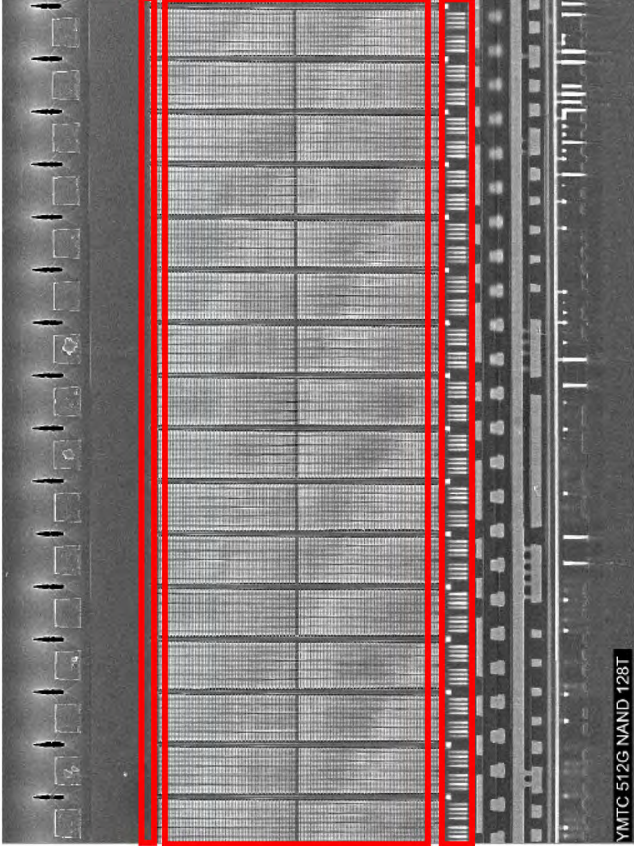
'214 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
<p>[9.D] a data line configured to be selectively coupled to a common source and the first and second memory cells through the conductive material.</p>	<p>YMTC 128L has a data line configured to be selectively coupled to a common source and the first and second memory cells through the conductive material.</p> <p><i>See [1.F], supra.</i></p>  <p>Common source</p> <p>Memory cells of memory cell strings containing conductive material</p> <p>Data lines</p> <p>YMTC 512G NAND 128T</p>
<p>[10.A] The apparatus of claim 9, further comprising: a first</p>	<p>YMTC 128L has the apparatus of claim 9, further comprising: a first additional conductive material configured to operate as a control gate to access the first memory cell, wherein the first memory</p>

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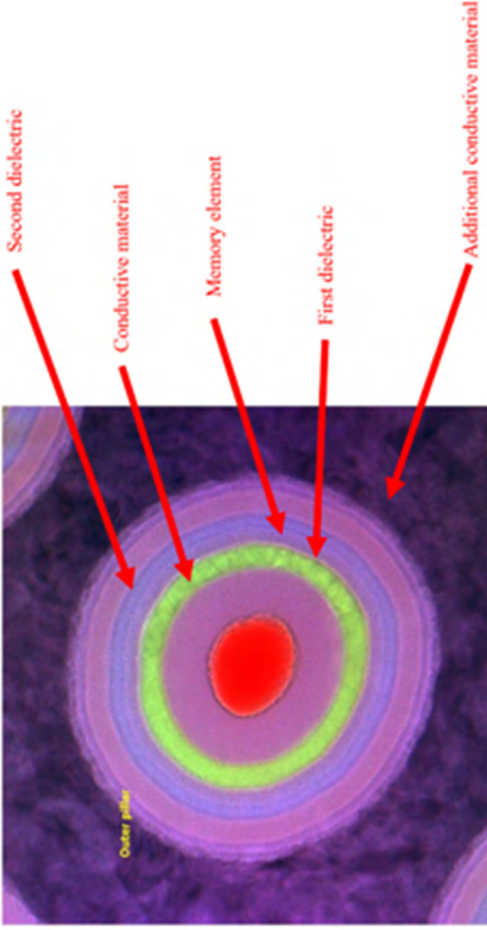
<p><b>'214 Patent Claim</b></p>	<p><b>YMTC 128L 3D NAND MEMORY ("YMTC 128L")</b></p>
<p>additional conductive material configured to operate as a control gate to access the first memory cell, wherein the first memory element and the first additional conductive material are located in the first device level of the memory device; and</p>	<p>element and the first additional conductive material are located in the first device level of the memory device. Specifically, the identified additional conductive material is the gate line or word line for a given level of the array, and the gate line or word line is configured to operate as a control gate as claimed.</p>  <p>The diagram shows a cross-section of a memory cell. At the center is a red 'Memory element'. It is surrounded by a green 'Conductive material' layer. This is followed by a purple 'First dielectric' layer, then a blue 'Second dielectric' layer, and finally an outermost purple 'Outer pillar' layer. A red arrow points to the 'Additional conductive material' located between the first and second dielectric layers.</p>
<p>[10.B] a second additional conductive material configured to operate as a control gate to access the second memory cell, wherein the second memory element and the second additional conductive material are located in the second device level of the memory device.</p>	<p>YMTC 128L has a second additional conductive material configured to operate as a control gate to access the second memory cell, wherein the second memory element and the second additional conductive material are located in the second device level of the memory device. Specifically, the identified additional conductive material is the gate line or word line for a given level of the array, and the gate line or word line is configured to operate as a control gate as claimed.</p>

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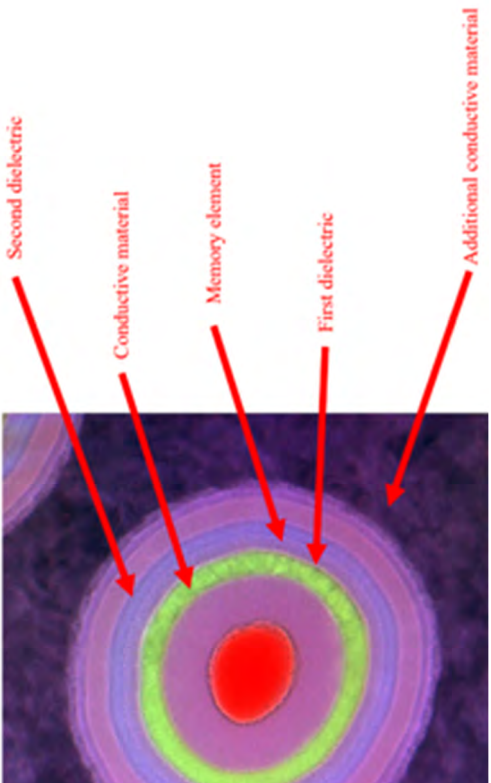
'214 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
<p>[11] The apparatus of claim 10, wherein each of the first and second memory cells further includes a first dielectric between the respective memory element and the conductive material.</p>	 <p>The diagram shows a cross-section of a memory cell with a central red core labeled 'Memory element'. This core is surrounded by a green ring labeled 'First dielectric'. The next layer is a purple ring labeled 'Conductive material'. The outermost layer is a light blue ring labeled 'Second dielectric'. A yellow label 'Outer pillar' points to the entire structure. A red arrow labeled 'Additional conductive material' points to a layer below the 'Conductive material' layer.</p>
<p>[11] The apparatus of claim 10, wherein each of the first and second memory cells further includes a first dielectric between the respective memory element and the conductive material.</p>	<p>YMTC 128L has the apparatus of claim 10, wherein each of the first and second memory cells further includes a first dielectric between the respective memory element and the conductive material.</p>

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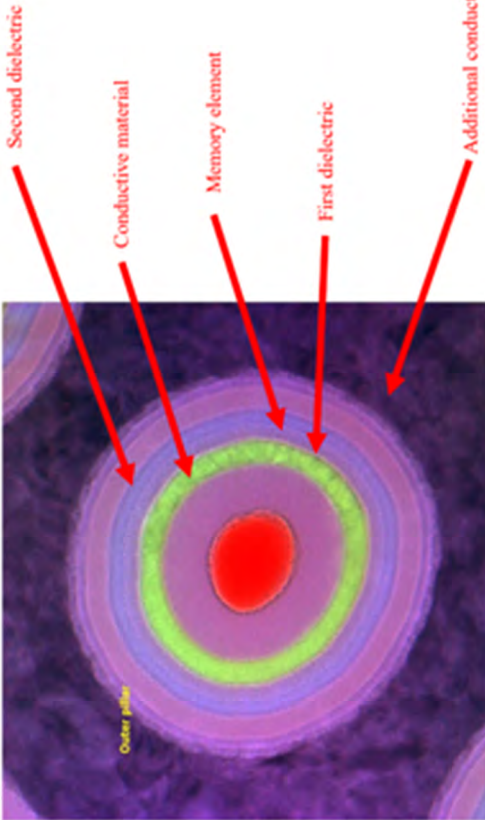
<p><b>'214 Patent Claim</b></p>	<p><b>YMTC 128L 3D NAND MEMORY ("YMTC 128L")</b></p> 
<p>[12] The apparatus of claim 11, wherein each of the first and second memory cells further includes a second dielectric between the respective memory element and the respective additional conductive material.</p>	<p>YMTC 128L has the apparatus of claim 11, wherein each of the first and second memory cells further includes a second dielectric between the respective memory element and the respective additional conductive material.</p>

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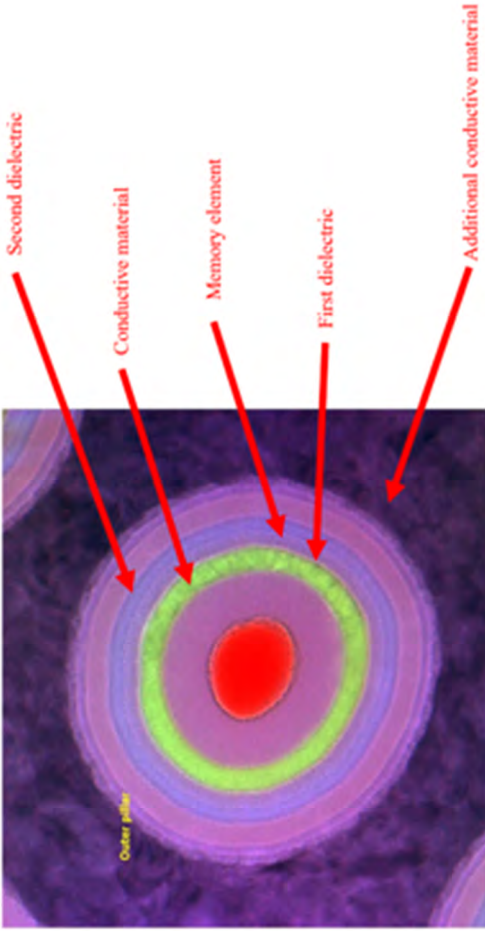
<p><b>'214 Patent Claim</b></p>	<p><b>YMTC 128L 3D NAND MEMORY ("YMTC 128L")</b></p>
<p>[14] The apparatus of claim 9, wherein the first and second memory cells are located between the substrate and the data line.</p>	 <p>Second dielectric Conductive material Memory element First dielectric Additional conductive material Outer pillar</p>
<p>[14] The apparatus of claim 9, wherein the first and second memory cells are located between the substrate and the data line.</p>	<p>YMTC 128L has the apparatus of claim 9, wherein the first and second memory cells are located between the substrate and the data line.</p>

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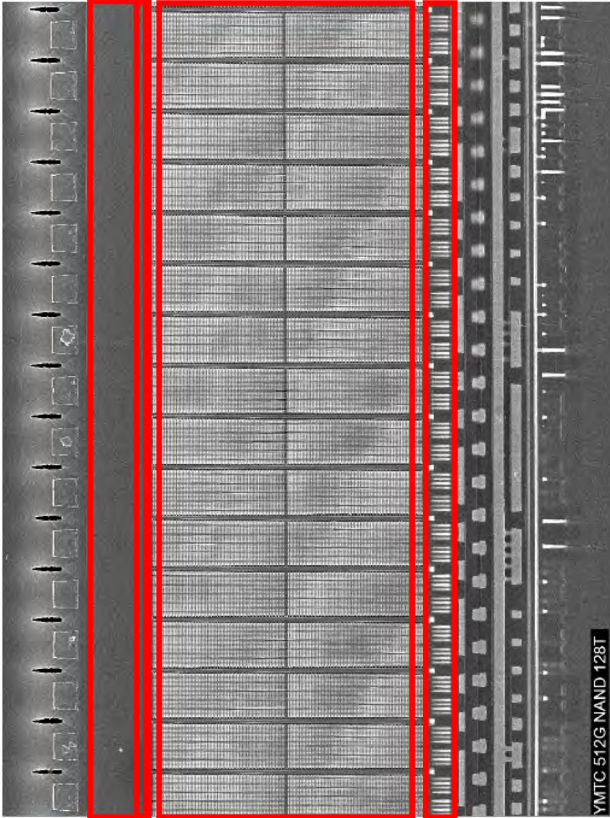
'214 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
	 <p>Substrate Common source</p> <p>Memory cells of memory cell strings containing conductive material</p> <p>Data lines</p> <p>YMTC 512G NAND 128L</p>
[15.PRE] An apparatus comprising:	YMTC 128L is an apparatus. <i>See [1.PRE], supra.</i>
[15.A] a substrate of a memory device;	YMTC 128L has a substrate of a memory device.

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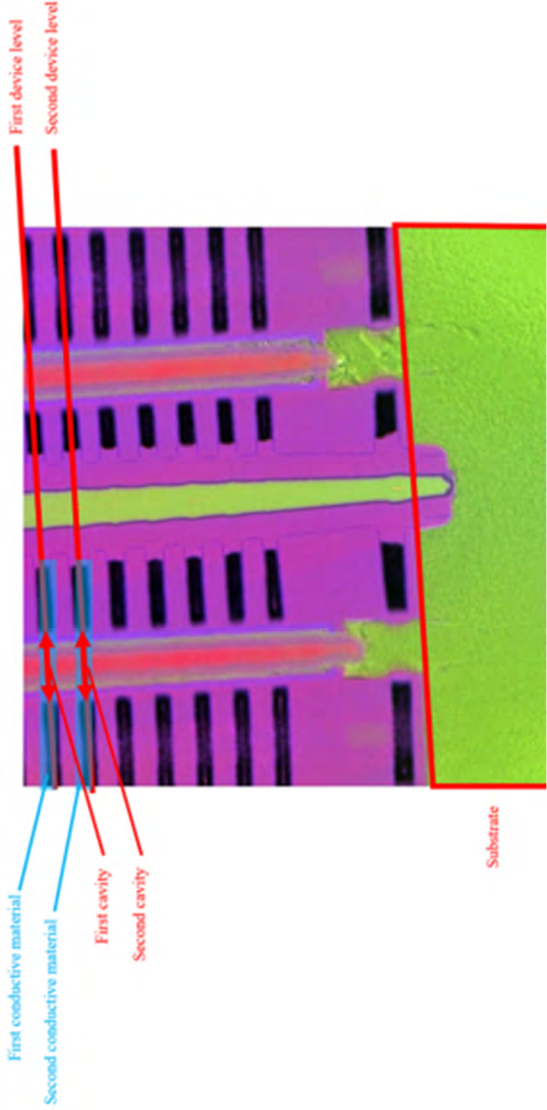
<p><b>'214 Patent Claim</b></p>	<p><b>YMTC 128L 3D NAND MEMORY ("YMTC 128L")</b></p>  <p>The diagram shows a cross-section of a 3D NAND memory stack. It features two device levels, each with a conductive material layer and a cavity. The first device level is on top, and the second is below it. The substrate is at the bottom. Labels with arrows point to the 'First device level', 'Second device level', 'First conductive material', 'Second conductive material', 'First cavity', 'Second cavity', and 'Substrate'.</p>
<p>[15.B] a first conductive material located in a first device level of the memory device over the substrate, the first conductive material including a first cavity, the first cavity having a first sidewall;</p>	<p>YMTC 128L has a first conductive material located in a first device level of the memory device over the substrate, the first conductive material including a first cavity, the first cavity having a first sidewall.</p>

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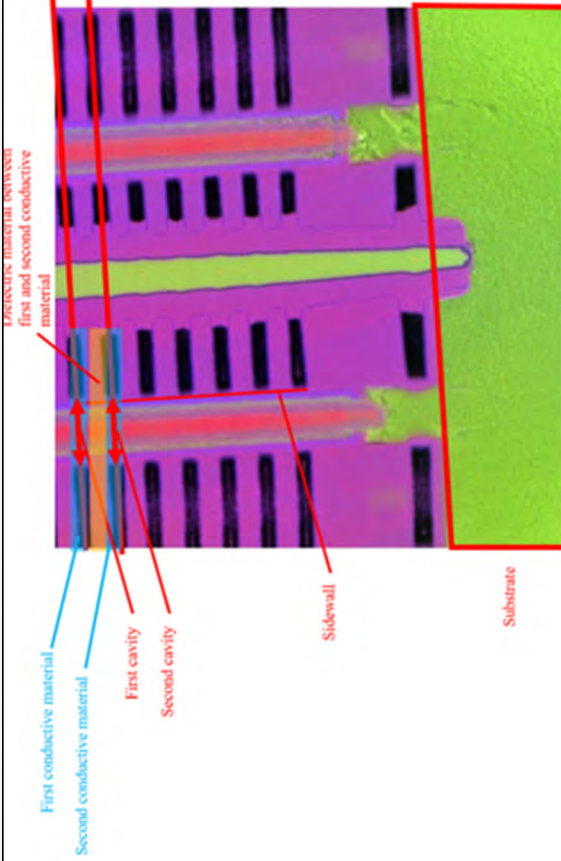
<p>'214 Patent Claim</p>	<p>YMTC 128L 3D NAND MEMORY ("YMTC 128L")</p>
<p>[15.C] a second conductive material located in a second device level of the memory device over the first device level and over the substrate, the second conductive material including a second cavity, wherein the first device level is different from the second device level;</p>	 <p>The diagram shows a cross-section of a 3D NAND memory stack. At the bottom is a green substrate. Above it is a purple layer representing the first device level, containing a blue layer (first conductive material) with a blue cavity (first cavity). Above this is a red layer representing the second device level, containing a red layer (second conductive material) with a red cavity (second cavity). A purple sidewall is shown between the two device levels. A grey layer (insulating material) is located between the first and second conductive material layers. Labels with arrows point to: First conductive material, Second conductive material, First cavity, Second cavity, Sidewall, Substrate, First device level, Second device level, and Insulating material between first and second conductive material.</p>
<p>[15.C] a second conductive material located in a second device level of the memory device over the first device level and over the substrate, the second conductive material including a second cavity, wherein the first device level is different from the second device level.</p>	<p>YMTC 128L has a second conductive material located in a second device level of the memory device over the first device level and over the substrate, the second conductive material including a second cavity, the second cavity having a second sidewall, wherein the first device level is different from the second device level.</p>

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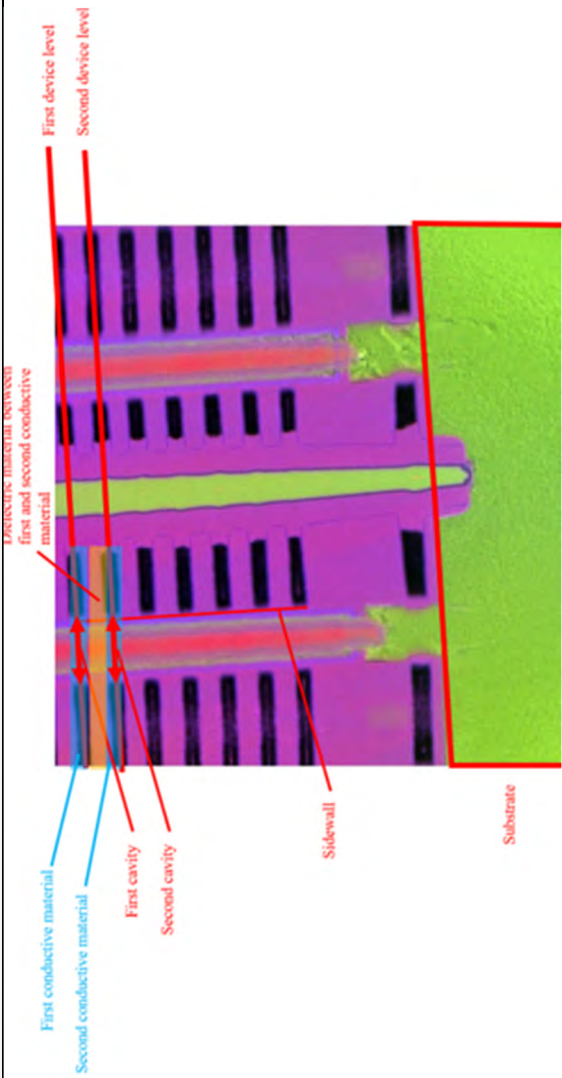
<p><b>'214 Patent Claim</b></p>	<p><b>YMTC 128L 3D NAND MEMORY ("YMTC 128L")</b></p>  <p>The diagram illustrates a cross-section of a 3D NAND memory stack. It features a substrate at the bottom, followed by a series of alternating layers of conductive material and cavities. The first conductive material layer is shown in blue, and the second conductive material layer is shown in purple. The first cavity is shown in orange, and the second cavity is shown in red. The sidewall is shown in green. The first device level is shown in black, and the second device level is shown in white. The first and second conductive material layers are shown in yellow.</p>
<p>[15.D] a first dielectric formed on the first sidewall and the second sidewall;</p>	<p>YMTC 128L has a first dielectric formed on the first sidewall and the second sidewall.</p>

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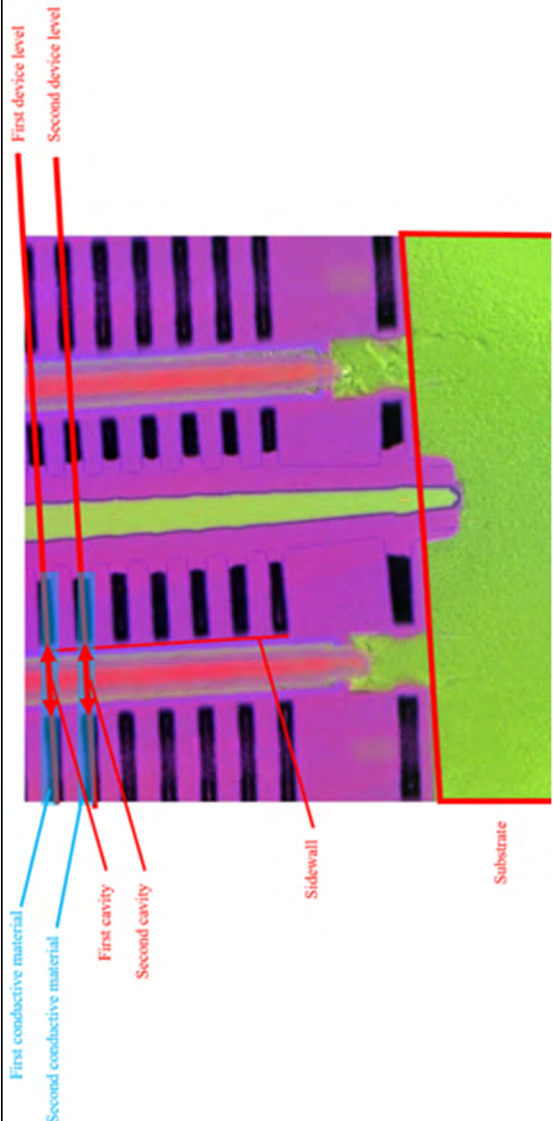
<p><b>'214 Patent Claim</b></p>	<p style="text-align: center;"><b>YMTC 128L 3D NAND MEMORY ("YMTC 128L")</b></p>  <p>The diagram shows a cross-section of a 3D NAND memory stack. It features two device levels, each with a conductive material layer and a cavity. The layers are separated by sidewalls. The entire structure is built on a substrate. Labels with arrows point to the following components: First device level (top), Second device level (middle), First conductive material (blue arrows), Second conductive material (purple arrows), First cavity (red arrows), Second cavity (red arrows), Sidewall (red arrow), and Substrate (green area at the bottom).</p> <p>Note that the '214 Patent explains that: "The term 'on', 'over', or 'overlying' does not imply any directionality as used herein unless otherwise explicitly stated as such." 8,803,214 Patent at 5:30-38.</p>
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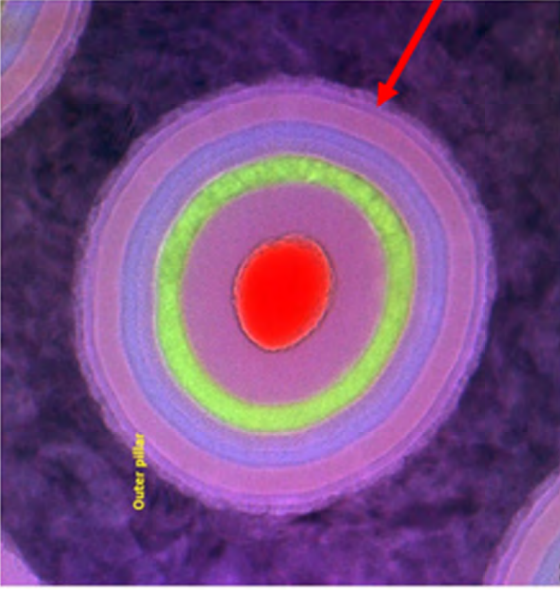
'214 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
<p>[15.E] a first memory element located in the first cavity and electrically isolated from the first conductive material by a first dielectric;</p>	 <p>Dielectric formed on sidewalls the different device levels</p> <p>Outer pillar</p>
<p>[15.E] a first memory element located in the first cavity and electrically isolated from the first conductive material by a first dielectric;</p>	<p>YMTC 128L has a first memory element located in the first cavity and electrically isolated from the first conductive material by a first portion of the first dielectric.</p>

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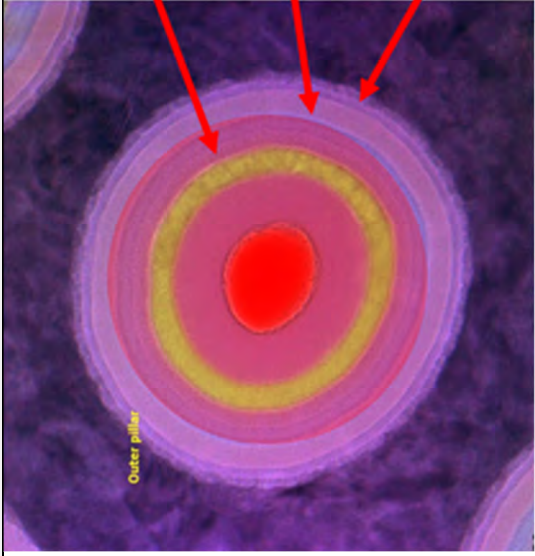
'214 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
<p>[15.F] a second memory element located in the second cavity and electrically isolated from the second conductive material by a second portion of the first dielectric;</p>	 <p>The diagram shows a cross-section of a memory cell. At the center is a red 'Memory element'. It is surrounded by a yellow 'Second dielectric' layer. This is further enclosed by a purple 'Dielectric formed on sidewalls the different device levels' layer. The entire structure is within a larger purple 'Outer pillar'.</p>
<p>[15.F] a second memory element located in the second cavity and electrically isolated from the second conductive material by a second portion of the first dielectric.</p>	<p>YMTC 128L has a second memory element located in the second cavity and electrically isolated from the second conductive material by a second portion of the first dielectric.</p>

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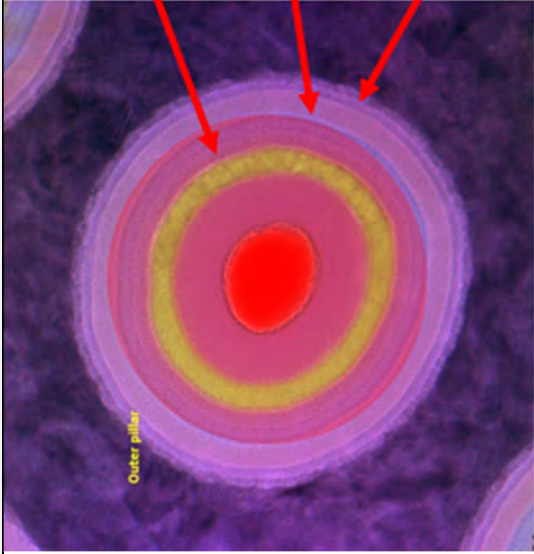
<p><b>'214 Patent Claim</b></p>	<p><b>YMTC 128L 3D NAND MEMORY ('YMTC 128L')</b></p>
	<p>YMTC 128L has a second dielectric formed on a side of the first memory element and on a side of the second memory element.</p>
<p>[15.G] a second dielectric formed on a side of the first memory element and on a side of the second memory element; and</p>	<p>YMTC 128L has a second dielectric formed on a side of the first memory element and on a side of the second memory element.</p>

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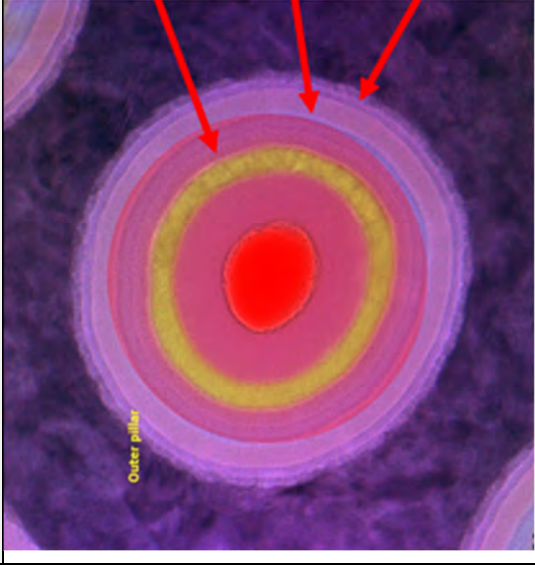
<p>'214 Patent Claim</p>	<p>YMTC 128L 3D NAND MEMORY ("YMTC 128L")</p>
<p>[15.H] a conductive channel extending from the first device level to the second device level and facing the first and second memory elements, such that the conductive channel is electrically isolated from the first and second memory elements by at least a respective portion of the second dielectric.</p>	 <p>Note that the '214 Patent explains that: "The term 'on', 'over', or 'overlying' does not imply any directionality as used herein unless otherwise explicitly stated as such." 8,803,214 Patent at 5:30-38.</p>
<p>[15.H] a conductive channel extending from the first device level to the second device level and facing the first and second memory elements, such that the conductive channel is electrically isolated from the first and second memory elements by at least a respective portion of the second dielectric.</p>	<p>YMTC 128L has a conductive channel extending from the first device level to the second device level and facing the first and second memory elements, such that the conductive channel is electrically isolated from the first and second memory elements by at least a respective portion of the second dielectric.</p>

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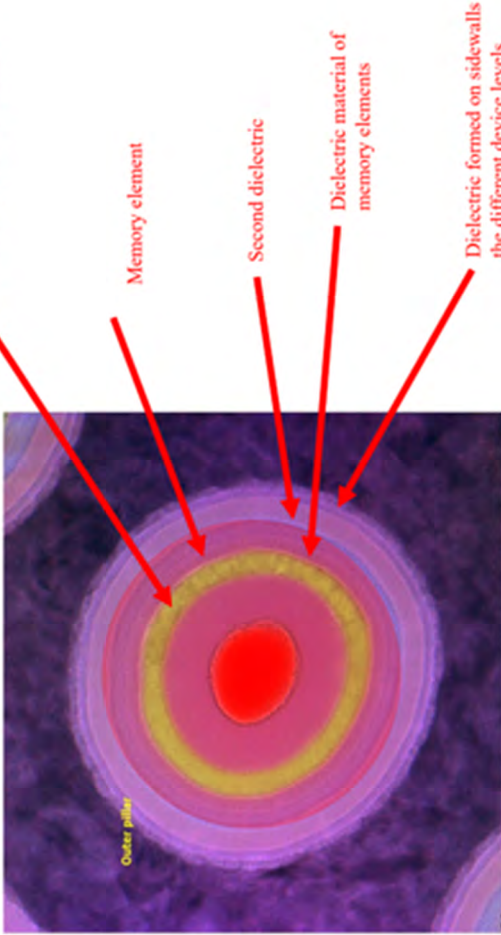
<p>'214 Patent Claim</p>	<p>YMTC 128L 3D NAND MEMORY ("YMTC 128L")</p>  <p>The diagram shows a cross-section of a 3D NAND memory cell. It features a central red core labeled "Memory element". This core is surrounded by a yellow ring labeled "Conductive polysilicon channel". The next layer is a purple ring labeled "Second dielectric". This is followed by a blue ring labeled "Dielectric material of memory elements". The outermost layer is a light blue ring labeled "Dielectric formed on sidewalls the different device levels". A yellow label "Outer pillar" points to the entire structure. Red arrows point from the text labels to the corresponding layers in the diagram.</p>
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EXHIBIT C-2

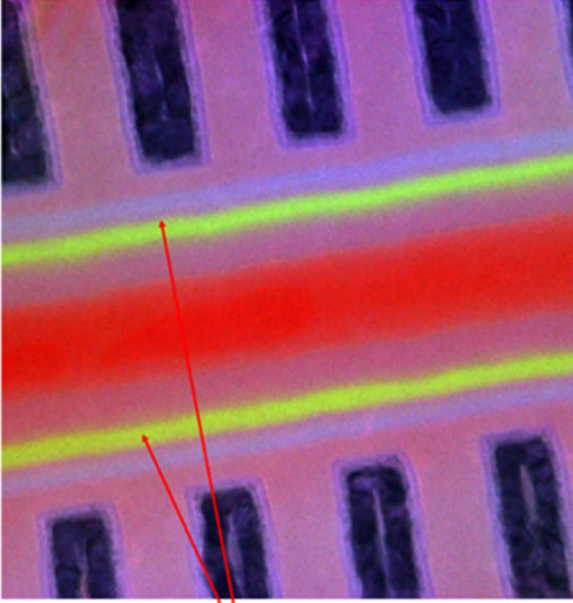
'214 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
	 <p data-bbox="519 1060 673 1186">Conductive polysilicon channel isolated from memory elements</p>
[16] The apparatus of claim 15, wherein the first and second memory elements comprise polysilicon.	YMTC 128L has the apparatus of claim 15, wherein the first and second memory elements comprise polysilicon.

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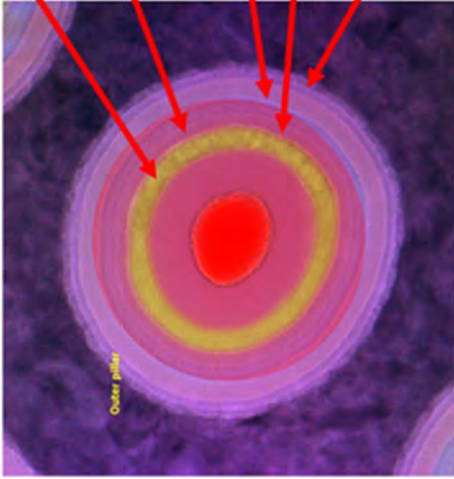
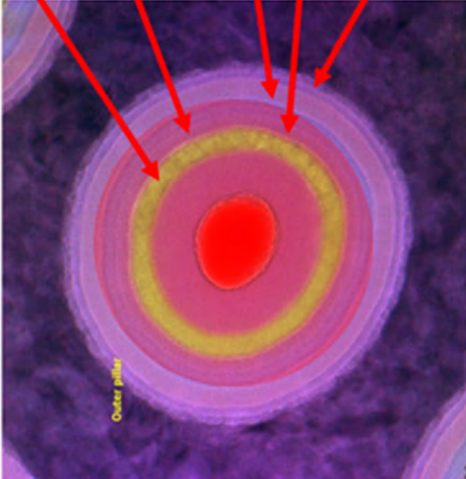
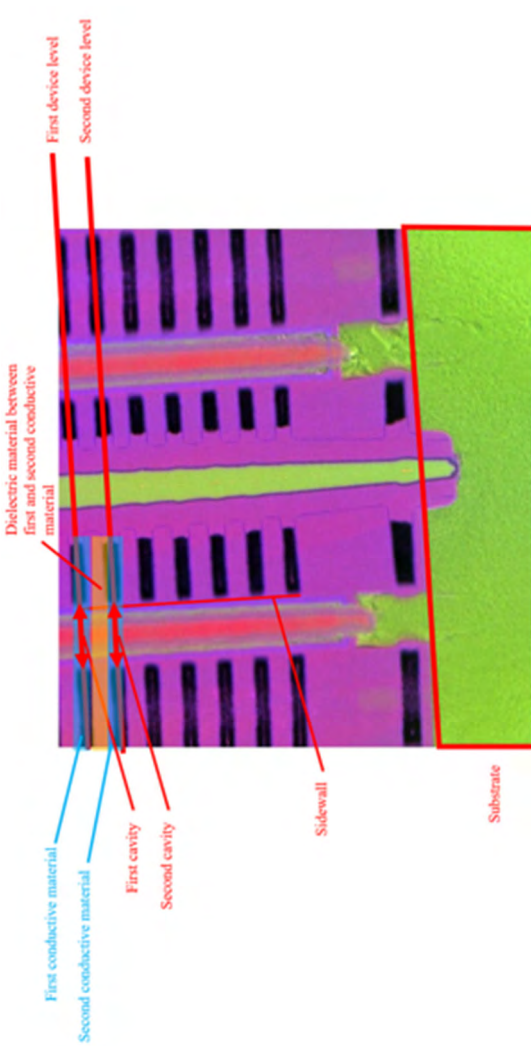
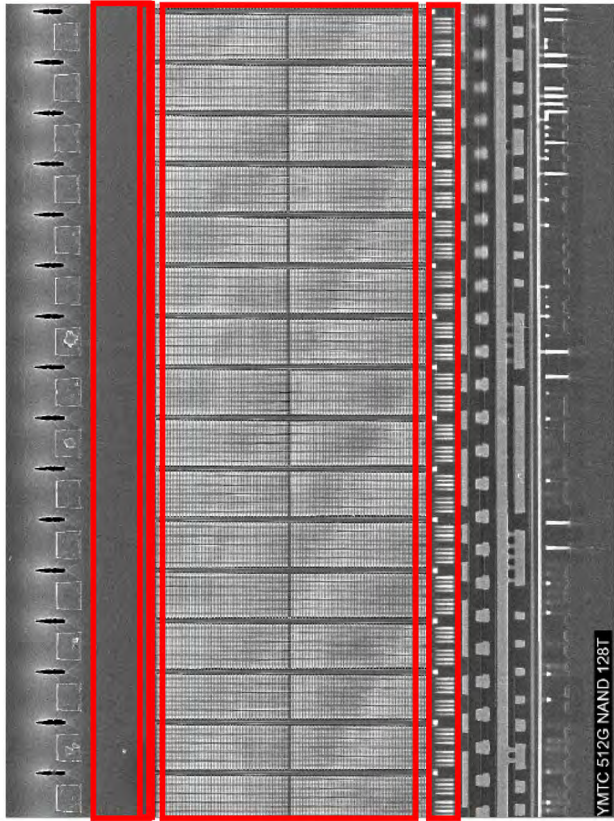
'214 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
	
<p>[17] The apparatus of claim 15, wherein the first and second memory elements comprise a dielectric material.</p>	

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'214 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
<p>[18] The apparatus of claim 17, wherein the dielectric material comprises silicon nitride.</p> <p>The charge trap of the memory element is a silicon nitride material.</p>	<p>YMTC 128L has the apparatus of claim 17, wherein the dielectric material comprises silicon nitride.</p> <p>The charge trap of the memory element is a silicon nitride material.</p>
<p>[19] The apparatus of claim 15, further comprising dielectric material between the first and second conductive materials.</p>	<p>YMTC 128L has the apparatus of claim 15, further comprising dielectric material between the first and second conductive materials.</p> 

<p><b>'214 Patent Claim</b></p>	<p><b>YMTC 128L 3D NAND MEMORY ("YMTC 128L")</b></p>
<p>[20.A] The apparatus of claim 15, further comprising: a data line configured to be selectively coupled to the conductive channel, wherein the first and second memory elements are located between the data line and the substrate.</p>	<p>YMTC 128L has the apparatus of claim 15, further comprising: a data line configured to be selectively coupled to the conductive channel, wherein the first and second memory elements are located between the data line and the substrate.</p>  <p>Substrate Common source</p> <p>Memory cells of memory cell strings containing conductive material</p> <p>Data lines</p> <p>YMTC 512G NAND 128T</p>

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