

Novel Transition Layer Engineered Si Nanocrystal Flash Memory with MHSOS Structure Featuring Large V_{th} Window and Fast P/E speed.

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Abstract

In this work, we propose a MHSOS (metal gate/high-k/SRO(silicon-rich oxide)/SiO₂/Si) structure showing large memory window (> 4V) with fast P/E speed (± 18 V, 200 μ s). The erase speed is featuring faster than that of Si₃N₄ and has a retention time of 10 years for 10 % charge loss. These excellent properties were obtained through the modification of the transition layer between Si-NC and SiO₂ matrix in an SRO medium, as well as tunneling/blocking dielectric material optimization.

Introduction

To achieve a good trade-off between reliability and good program/erase property in nonvolatile memory, we propose SRO as a charge trap medium. There have been several reports on SRO based Flash memory, but not much attention has been given to its microstructure and corresponding electrical features (1). In this study, we attempted to identify relative merits of SRO as a charge trap layer with specific consideration to the nano-scale environment. Precipitation of silicon nanocrystal (Si-NC) in the SRO medium builds up a sub-oxide transition layer (TL) between the Si-NC and SiO₂ matrix, which has been proven experimentally (2-3). This TL can provide certain advantages in memory window and P/E speed to overcome the shortcomings of conventional Si-NC (small memory window) (4) or Si₃N₄ (slow erase speed) (5), which are summarized in Table. I. These features are verified by obtained electrical data in this paper showing high performance memory operation, and also by the conceptual interpretation of a graded energy band model proposed for SRO.

TABLE. I. COMPARISON OF VARIOUS CHARGE STORAGE LAYERS

Charge Storage Medium	Si-NC	Si ₃ N ₄	TL engineered Si-NC
Coverage Ratio	<<1	~1	≤1
V _{th} Shift	Small	Large	Large
P/E Speed	Fast	Relatively Slow (E speed)	Fast
Endurance	Good	Poor	Good

Experimental

Thin SRO films (4 nm ~ 10 nm) were deposited by a novel pulse type HDP-CVD, named ‘flash deposition’ that forms denser non-stoichiometric film than conventional PECVD (6). The excess Si amount can be controlled by simple variation of a process variable i.e., OSR, as summarized in Table. II.

Si-nanocrystals precipitate from SRO film by appropriate annealing at 850~1050 °C, in N₂ or N₂/O₂ ambient. The presence of Si-nanocrystals in SRO medium was confirmed by TEM as well as PL (photo luminescence) (not shown in this article). Cross-sectional TEM (Fig. 1) shows that Si-nanocrystals of 2-3 nm precipitate from the SRO medium as a uniform single layer between tunnel and control oxide.

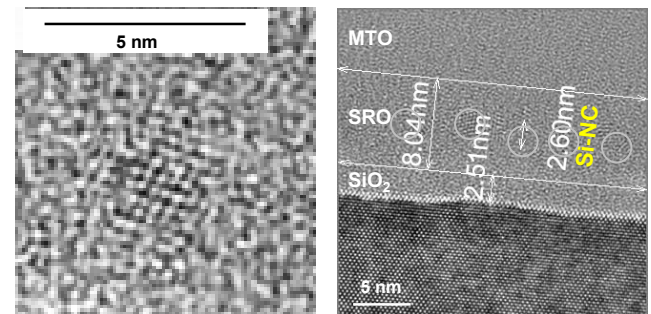


Fig. 1. Cross sectional TEM of gate oxide stack

TABLE. II. SUMMARY OF CHARACTERISTICS OF SRO FORMED BY FLASH DEPOSITION

#	OSR ¹	R.I. ²	x ³	Excess Si (%)
SRO_12	1.2	1.48	1.98	0
SRO_10	1.0	1.51	2.00	0
SRO_08	0.8	1.83	1.52	6.4
SRO_07	0.7	1.99	1.30	10.1
SRO_06	0.6	2.19	1.14	13.4
SRO_05 ⁴	0.5	2.33	0.91	19.3
SRO_04	0.4	2.52	0.75	25.0

¹ O₂ to SiH₄ gas flow rate ratio

² Refractive Index, measured by ellipsometry

³ x in SiO_x determined from XPS analysis

⁴ Most of the experiment was done with SRO_05 in this work.

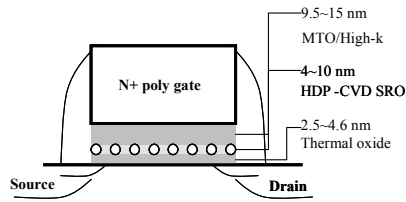


Fig. 2. Cross section of memory cell.

MOSFETs ($W/L = 80 \text{ nm}/100 \text{ nm}$) and MOS-type capacitors of $100 \times 100 \mu\text{m}$ were used for electrical characterization (Fig. 2). For devices with high-k control oxide, 20 nm TaN gate electrodes were used.

The control sample used in this work was fabricated by the same sequence except for the use of 8 nm ALD Si_3N_4 trap layer.

Results and Discussion

I-V curves of MOSFET (Fig. 3) and high frequency (100 kHz) C-V curves of MOS capacitor (Fig.4) show that large memory window greater than 5 V can be obtained with SRO memory cell.

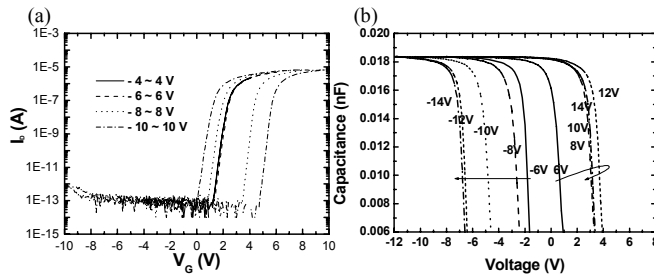


Fig. 3. (a) I-V curves of MOSFETs ($0.08 \times 0.1 \mu\text{m}$). (b) High-Frequency C-V curves of MOS capacitor ($100 \times 100 \mu\text{m}$). (Tunnel SiO_2 2.5 nm/SRO_07 8nm/MTO 9.5 nm.)

The memory window drastically increases with increasing Si concentration in the SRO layer, whereas degradation of ΔV_{FB} and retention is observed for highly Si-rich regime, probably due to agglomeration of Si-NC (Fig. 4).

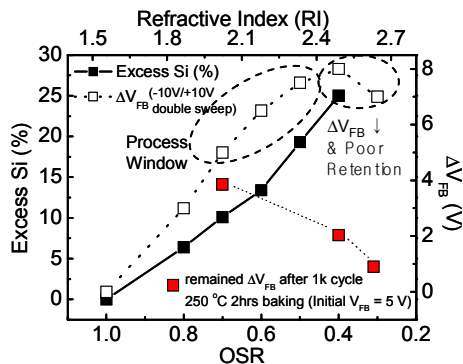


Fig. 4. Relationship of memory window with process variables. (Tunnel SiO_2 2.5 nm/SRO 8nm/MTO 9.5 nm)

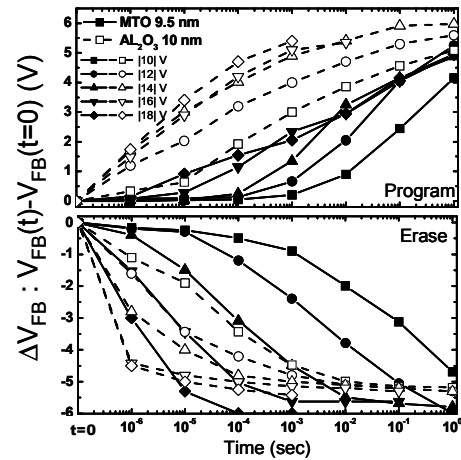


Fig. 5. Comparison of P/E speed of MTO with high-k control oxide. (Tunnel SiO_2 2.5 nm/SRO_05 8nm/MTO 9.5nm, ALO 10nm)

The program/erase transient characteristics are shown in Fig. 5. With MTO as a control oxide, ΔV_{FB} of programming saturates at a smaller voltage than that of erasing. This can be explained by the graded energy band model drawn in Fig. 6. In this model, TL is represented as a graded energy band regime with an assumption that Si-NC is formed in the middle of SRO. The barrier height of the tunnel oxide is reduced during the erase operation, resulting in fast erasing, while the barrier height of control oxide is reduced during programming, resulting in slow programming as illustrated in Fig. 7. To improve the program speed, this back-tunneling should be decreased during program/erase operation, thus a high-k dielectric of aluminum oxide (ALO) of 10 nm was adopted as a control oxide. As a result, the program/erase speed was much improved (dashed line in Fig. 5).

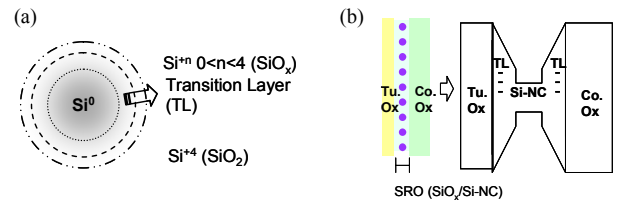


Fig. 6. Energy band diagram of SRO; (a) Transition layer between Si-NC and SiO_2 matrix, (b) Graded band proposed according to (a).

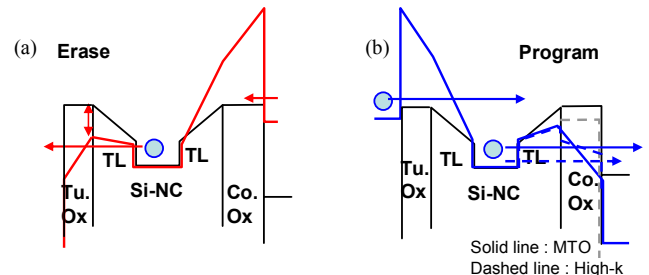


Fig. 7. Barrier height modulation due to transition layer results in (a) fast erase and (b) relatively slow program. Program speed can be improved by adopting a high-k control oxide.

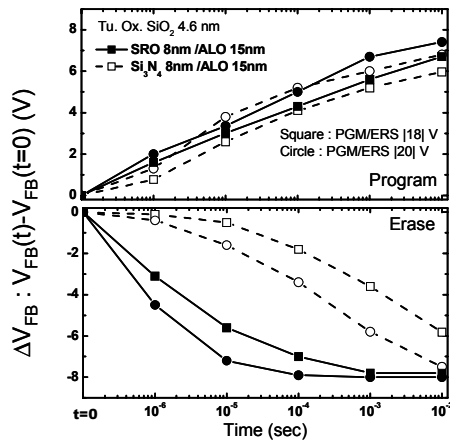


Fig. 8. Comparison of P/E speed of SRO with Si₃N₄. (Tunnel SiO₂ 4.6 nm/SRO_05, Si₃N₄ 8nm/ALO 15nm)

By comparing the P/E characteristics of SRO and SiN (Fig. 8) with the same control oxide of ALO 15 nm, SRO's notable advantage of fast erase speed is clearly observed. Owing to this fast erasing property, the endurance is better for SRO-based device as shown in Fig. 9. Room temperature retention is ensured with a thick tunnel SiO₂ of 4.6 nm requiring higher operation voltage than with thinner tunnel oxide (Fig.10).

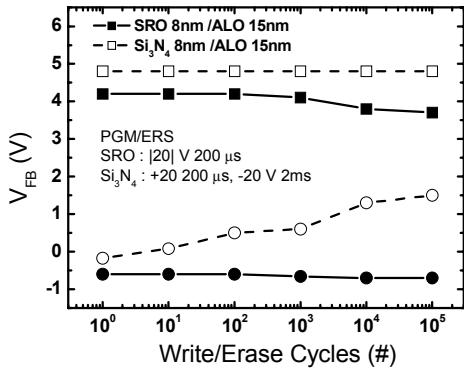


Fig. 9. Endurance of SRO_05 and Si₃N₄. (Tunnel SiO₂ 4.6 nm/SRO_05, Si₃N₄ 8nm/ALO 15nm)

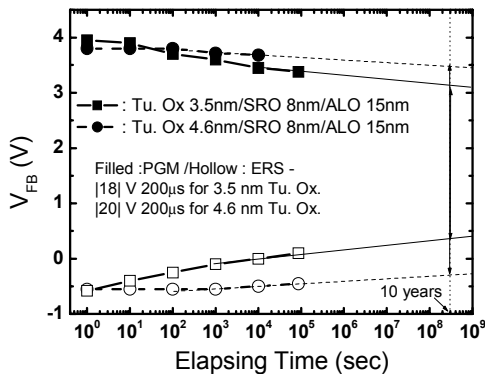


Fig. 10. Retention of SRO_05. (Tunnel SiO₂ 3.5 nm, 4.6 nm/SRO_05 8nm/ALO 15nm)

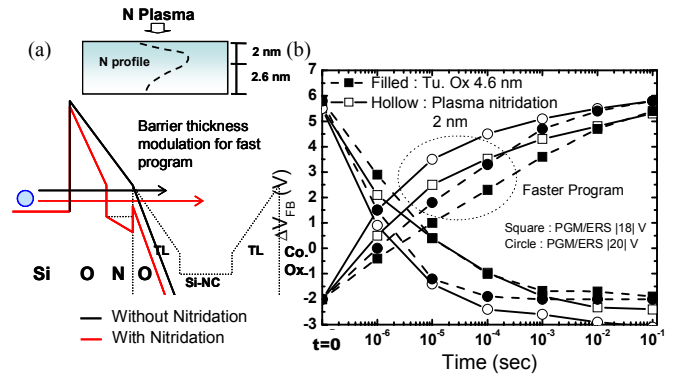


Fig. 11. (a) Schematics of plasma nitridation and energy band diagram for barrier thickness modulation. (b) Comparison of P/E speed; with/without nitridation. (Tunnel SiO₂ 4.6 nm/SRO_05 8nm/ALO 15nm.)

To improve the program speed with tunnel oxide of 4.6 nm, plasma nitridation on top of the tunnel SiO₂, was performed to make an ONO tunnel barrier. This is the kind of low-k/high-k/low-k VARIOT tunnel barrier proposed by B. Govoreanu et. al (7). The ONO structure in this work features a simple fabrication process in which the high-k layer is formed by plasma nitridation and top oxide in ONO is formed during SRO formation. The ONO tunnel barrier resulted in faster P speed as shown in Fig. 11.

Fig. 12 summarized the P/E characteristics of SRO-based device for various tunnel oxide and control oxide thickness.

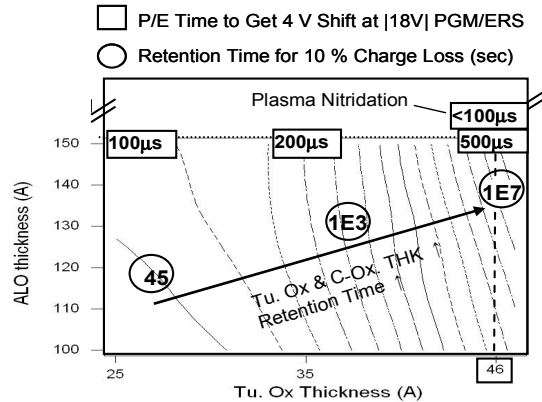


Fig. 12. P/E and retention characteristics for various tunnel oxide and control oxide combination with SRO_05.

Based on the graded band model suggested in this work, the electrical characteristics greatly depend on the SRO microstructure. SRO thickness or Si-NC size effect was investigated. With a thinner SRO layer, smaller Si-NC could be obtained, which was confirmed by blue shifted PL peak. From electrical data shown in Fig. 13(b) and (c), thinner SRO shows better retention with decreasing erase speed, which can be attributed to the band offset increase for smaller NCs with a reduced slope of graded band, as described in Fig. 13 (a).

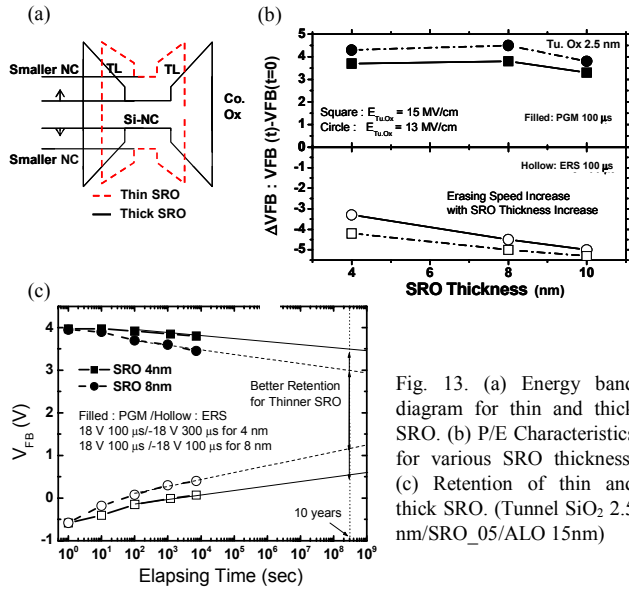


Fig. 13. (a) Energy band diagram for thin and thick SRO. (b) P/E Characteristics for various SRO thickness. (c) Retention of thin and thick SRO. (Tunnel SiO₂ 2.5 nm/SRO_05/ALO 15nm)

While the initial bonding configuration of as-deposited SRO consists of broad sub-oxide spectra from Si¹⁺ to Si⁴⁺, the annealed SRO shows the phase separation between Si-NC (Si⁰) and SiO₂ matrix (Si⁴⁺) as shown in Fig. 14(a). Moreover, in oxidizing ambient of N₂/O₂, a further reduction of sub-oxide and Si-NC bonding was observed, which signifies modification of the graded band as well as a decrease of nanocrystal size as shown in Fig. 14(b).

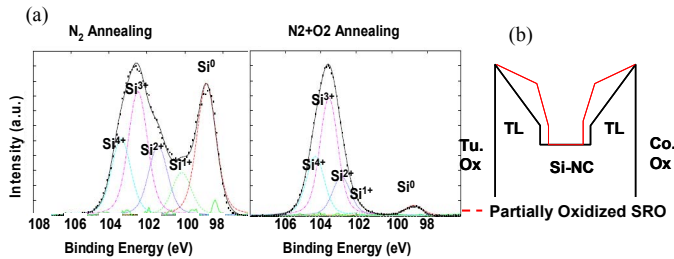


Fig. 14. (a) Si 2p XPS spectra showing increase of SiO₂-like Si⁴⁺, Si³⁺ peaks relative to Si²⁺, Si¹⁺ transition state after annealing at high temperature. (b) Corresponding band diagram.

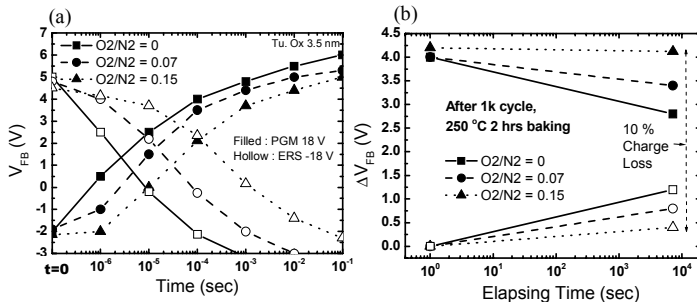


Fig. 15. (a) P/E characteristics according to partial oxygen pressure. (b) Corresponding retention. (Tunnel SiO₂ 3.5 nm/SRO_05 8nm/ALO 15nm)

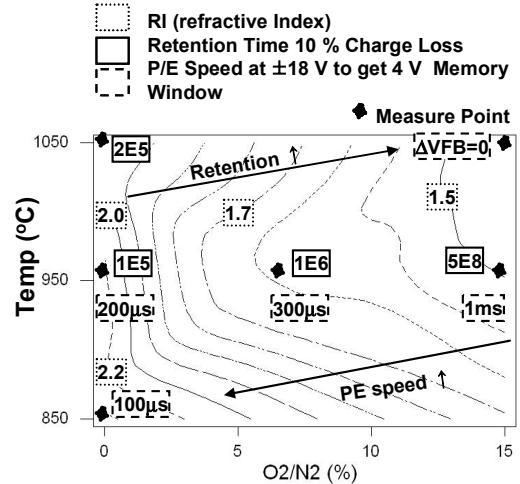


Fig. 16. Summary of P/E characteristics of SRO_05 for various partial oxygen pressures and annealing temperatures.

As shown in Figs.15 and 16, retention of 10 % charge loss for more than 10 years is obtained with a tunnel oxide of 3.5 nm through the modification of the transition layer rather than the increase in tunnel oxide thickness.

Conclusion

As a charge trap medium, SRO combines the advantages of Si₃N₄ and Si nanocrystals, which are large memory window and fast P/E, respectively. These properties are explained by the existence of a sub-oxide transition layer around the precipitated Si nanocrystals. The P/E speed, as well as retention, was further improved by employing a high-k control dielectric along with transition layer optimization.

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References

- (1) M. Rosmeulen, E Sleenckx, and K De Meyer., *Tech. Dig. of IEDM*, (2002) p.182.
- (2) M. Luppi, and S. Ossicini, *Physical Review*, B71 (2005) p.035340.
- (3) J. H. Oh et al., *Physical Review*, B63 (2001) p.205310.
- (4) S. Lombardo et al., *Microelectronic Engineering*, 72, (2004) p.411.
- (5) M. H. White, D. A. Adams, and J. Bu., *Circuits & Devices IEEE*, (2000) p. 22.
- (6) K.H. Joo et al., Korean Patent, P2005-0029290.
- (7) B. Govoreanu, P. Blomme, M. Rosmeulen, J. Van Houdt, K. De Meyer, *IEEE Electron Device Letters*, 24 (2003) p. 99.