

A New Operating Scheme by Switching the Polarity of Program/Erase Bias for Partially Oxidized Amorphous-Si-Based Charge-Trap Memory

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Abstract—In this brief, the authors propose a new program/erase (P/E) scheme for NAND-type partially oxidized amorphous-Si (a-Si)-based charge-trap memory in which the P/E voltages are interchanged into negative/positive ones, respectively. In the a-Si memory, the erasing speed was found to be faster than the programming speed, and therefore, the new scheme has been chosen to keep the program speed faster than the erase speed for the NAND operation. The P/E speeds in the new scheme increase at least ten times as those in the conventional P/E scheme. It is also shown that four-level memory states can be achieved via Fowler–Nordheim tunneling by applying programming voltage of -16 , -18 , and -20 V for each level during only 40 μ s together with erasing voltage pulse ($+20$ V, 1 ms). These results indicate that the new P/E scheme is more effective than the conventional scheme for operating the partially oxidized a-Si-based memories.

Index Terms—Charge-trap memory, NAND, partially oxidized amorphous Si (a-Si), program/erase (P/E) scheme, two-bit memory.

I. INTRODUCTION

A discrete-trap-type storage medium such as nitride and Si nanocrystals (NCs) [1], [2] has recently attracted much attention as an alternative approach to overcome the reliability issues of conventional polysilicon floating-gate Flash memory. Silicon–oxide–nitride–oxide–silicon (SONOS) has been widely studied as mainstream of discrete charge-trap memory due to several advantages over conventional devices such simple process, easy manufacturing, few erratic bits, insensitivity to oxide defects, and no floating-gate coupling effect [1]. Si NCs exhibit intrinsically amphoteric charge-trap behaviors; however, their memory window tends to be relatively smaller than that of silicon nitride [3], [4]. A transition layer has been employed between Si NC and SiO₂ to extend the memory window of the Si NC memory [5].

Several attempts have been made to achieve multilevel storage performance using a number of different storage media [2], [6], [7]. The key factors for obtaining multilevel operation are the memory window and program/erase (P/E) speeds. We have successfully extended the memory window by employing SiO₂/partially oxidized amorphous Si (a-Si)/HfO₂ structure as storage layer because the interface states of partially oxidized a-Si/SiO₂ tend to act as hole traps and the partially oxidized a-Si/HfO₂ interface has dominant electron trap centers [8]. The programming speed is known to be faster than the erasing speed in SONOS [9]. For conventional NAND Flash memory, fast programming is more essential than fast erasing because the P/E operations are generally performed in the block/page units, respectively. For our device, however, the erasing speed is faster than the programming

speed with the partially oxidized a-Si [8]. Hence, the conventional P/E scheme is not suitable for the NAND-type memory operations.

In this brief, we propose a new P/E scheme for the charge-trap memory based on the SiO₂/partially oxidized a-Si/HfO₂ structure, using reversed polarity as that of the conventional P/E scheme.

II. EXPERIMENTAL

Nonvolatile memory devices with SiO₂/partially oxidized a-Si/HfO₂ were prepared by sequential processes: formation of 3.5-nm SiO₂ on p-type Si using conventional thermal oxidation, atomic layer deposition (ALD) of 3-nm a-Si on SiO₂ at 350 °C, thermal oxidation of a-Si, and another ALD of 20 nm HfO₂ at 350 °C. The oxidation of a-Si was performed at 900 °C under a mixture of 10% O₂/90% N₂ for 1 min. Under this process, the a-Si layer is partially oxidized, which forms an oxygen-rich a-Si film. It is well known that the fully oxidized high-quality silicon dioxide (SiO₂) contains no charge-trapping sites; thus, it will not exhibit a hysteresis under capacitance–voltage (C – V) sweeping. Since dangling bonds or defects exist in the partially oxidized a-Si layer, the electrons that tunneled into the a-Si film can be trapped both in the bulk and the interfaces of partially oxidized a-Si/SiO₂ or partially oxidized a-Si/HfO₂. It has been reported that Si NCs can be formed by the oxidation of a-Si [10]. The high-resolution transmission electron microscopy image shows no discrete Si dots within the a-Si layer, which signifies the nonexistence of Si NCs. Therefore, it has been suggested that the memory effect is mainly not caused by Si NCs but by defect states such as dangling bonds in the partially oxidized a-Si or its interface with the HfO₂ or SiO₂ layer [8].

Two percent Nd-doped Al electrodes with a diameter of 100 μ m were deposited on the samples in vacuum for high-frequency C – V measurements, which were carried out by using an Agilent 4288A CV meter with a frequency of 1 MHz and a modulation signal amplitude of 100 mV. The P/E operations were performed via Fowler–Nordheim (FN) tunneling method by applying a voltage pulse on the gate electrode.

III. RESULTS AND DISCUSSION

Memory devices with a structure of SiO₂/partially oxidized a-Si/HfO₂ offer a hybrid type of charge memory: the interface states of partially oxidized a-Si/SiO₂ tend to act as hole traps, resulting in a negative shift of flatband voltage in (C – V) curve, and the partially oxidized a-Si/HfO₂ interface has electron trap centers leading to a positive voltage shift [8]. The memory window of the device is estimated to be 12 V from the flatband voltage (V_{FB}) shift of -5 to $+7$ V, obtained through C – V measurements swept from 20 to -20 V. The erasing speed was observed to be faster than the programming speed [8]. Using these characteristics, we introduce a new P/E scheme in which the P/E polarity is reversed because the erasing speed is faster than the programming speed in the conventional scheme. Fig. 1 compares the memory properties between the new and the conventional P/E schemes. In the new scheme, a positive gate pulse (20 V, 1 ms) switches the device to its fully erased state at 4.5 V V_{FB} . With a short programming pulse (-20 V, 1 μ s), the V_{FB} drops as much as 3 V from ~ 4.5 to ~ 1.5 V. The V_{FB} shift is linearly proportional to the programming time, and the fully erased state is almost invariant even after repeated P/E operations.

In the conventional P/E scheme, a fully erased state would be obtained by a negative gate pulse (-20 V, 1 ms). However, in the partially oxidized a-Si device, there is almost no change in V_{FB} even by a ten times longer positive gate pulse (20 V, 10 μ s). These results

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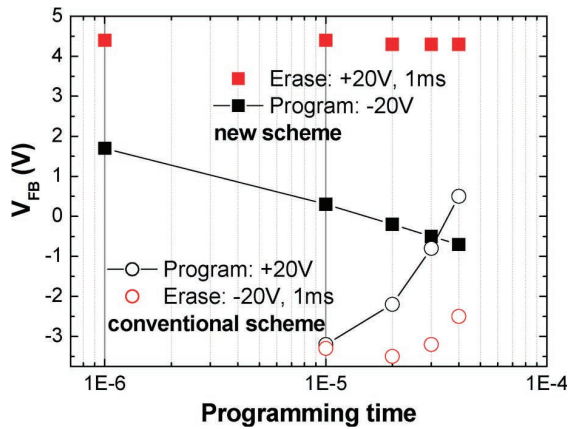


Fig. 1. Comparison of the P/E characteristics between the new and the conventional P/E schemes.

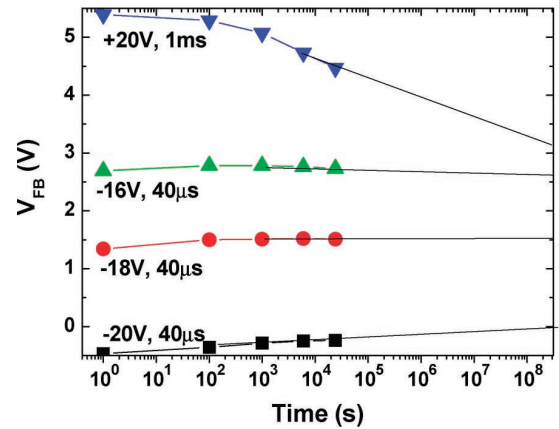


Fig. 3. Retention characteristics of the multilevel memory at room temperature in the new P/E scheme.

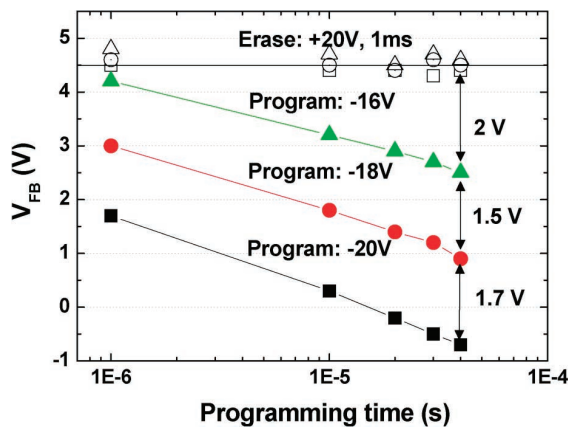


Fig. 2. V_{FB} shift as a function of programming time at each negative programming voltage for multilevel memory operation in the new P/E scheme.

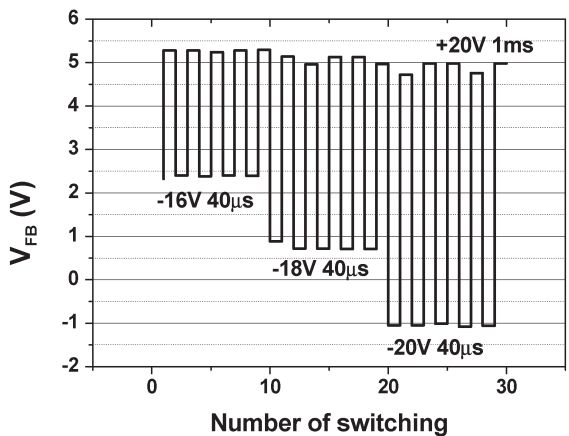


Fig. 4. Four-level V_{FB} response of device during the P/E testing cycle.

indicate that the new reversed polarity P/E scheme is more effective than the conventional scheme for operating the partially oxidized a-Si-based memories.

Fig. 2 shows the V_{FB} shift as a function of programming time at each negative programming voltage. A wide memory window of ~ 5.5 V is obtained by applying a programming pulse (-20 V, 40 μ s), which makes the device potentially promising for multilevel memory cell application. For successful multilevel operations, the spread in V_{FB} for each state should be within 0.5 V, and the voltage gap between the states should be at least 0.5 V. Hence, a minimum of 1 -V margin in V_{FB} is required between each state. As shown in Fig. 2, this device can reach four different states with interstate V_{FB} margin exceeding 1.5 V, using the erasing pulse (20 V 1 ms) and three 40 - μ s programming pulses (-16 , -18 , and -20 V).

Fig. 3 presents retention characteristics of the multilevel memory at room temperature. By extrapolating the retention data up to ten years, the voltage drops at each programming level are within 0.5 V, and the margin between the levels remains over 1 V, which satisfies the requirement for multilevel storage. In contrast, the fully erased state degrades faster than the programmed states, which is thought to be due to the high internal field ($V_{FB} \sim 5$ V) over the programmed states ($V_{FB} \sim -0.5 - 2.5$ V) induced by the trapped charge. The device retains its respective states up to 10^7 s. These results indicate that four levels (i.e., 00, 01, 10, and 11) can be stored up to 10^7 s in a single device by applying $+20$, -16 , -18 , and -20 V, respectively, which

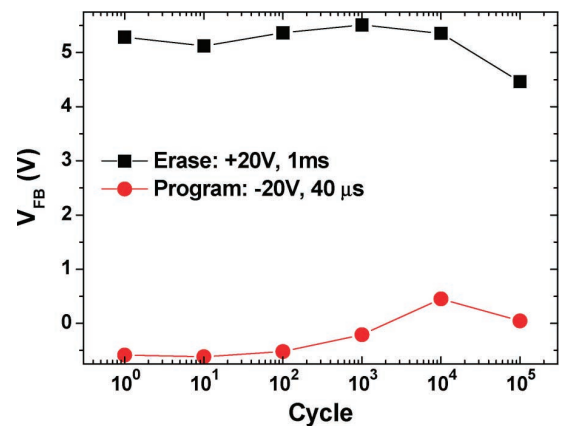


Fig. 5. P/E cycling characteristics of the device in the new P/E scheme. Pulses (-20 V, 40 μ s) and ($+20$ V, 1 ms) were applied to evaluate endurance characteristics for the P/E operations, respectively.

allows the use of the partially oxidized a-Si in high-density Flash memory applications.

The stability of the four-level P/E characteristics was checked by measuring the V_{FB} shift corresponding to applied voltage sequence as a function of time for the three programmed and one erased states, as shown in Fig. 4. The four states were very stable with little variation in

V_{FB} after five P/E cycling. Fig. 5 shows the P/E cycling characteristics of the device. Pulses of (-20 V, $40 \mu\text{s}$) and ($+20$ V, 1 ms) were applied to evaluate endurance characteristics for the P/E operation. Both the programmed and erased state V_{FB} increase almost in a parallel manner up to 10^3 cycles probably due to the accumulation of trap charges, but degradation of the P/E window occurs rapidly after 10^4 cycles.

IV. CONCLUSION

A new P/E scheme was proposed for faster P/E operations in partially oxidized a-Si-based NAND-type nonvolatile memory. The P/E speed using the reversed polarity scheme is at least ten times faster than the conventional P/E scheme in our device. It was shown that four-level memory states can be achieved by applying programming pulses of -16 , -18 , and -20 V for $40 \mu\text{s}$, together with an erase pulse of $+20$ V for 1 ms. This is very promising for multilevel memory cell application because the P/E speed is comparable to that of multilevel polysilicon Flash memory.

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Improved Noniterative Method for the Synthesis of Convergent Pierce Electron Guns

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Abstract—Iterative and noniterative synthesis techniques are widely employed for the preliminary design of Pierce electron guns, depending on four commonly used input design beam parameters. In this brief, an improved noniterative approach is proposed. This approach results in much closer agreement with the measured values of the same, except the anode-cathode spacing, when compared with 30 practical Pierce guns of different performances.

Index Terms—Pierce electron gun, Tiwary's noniterative method, Vaughan's iterative method.

I. INTRODUCTION

The iterative method of synthesizing a convergent Pierce electron gun was first proposed by Vaughan in 1981 [2]. In 2001, Sharma *et al.* made an improvement in synthesizing the anode aperture for Pierce guns [3], and in 2005, Yan *et al.* proposed another initial formula of a half-beam cone angle [5] so that the procedure can also give correct results in the case of relatively low convergence, which is programmed with languages such as Basic that do not have intrinsic support for negative square roots. Vaughan's iterative method is used to design a Pierce electron gun with a curved cathode that is described by output design parameters such as the radius of curvature of cathode R_c , the radius of curvature of the equivalent anode sphere R_a , the anode-cathode spacing z_a , the radius of the anode aperture r_a , and the "throw" z_w of the gun, which indicates the location of the "waist" of the beam from any gun electrode. The ancillary outputs are perveance P and the beam radius at anode plane $r_b(z_a)$. The input design parameters in this case are taken as those related to the circular-cylindrical electron beam to be "thrown" into the beam-wave interaction region of a device, for instance, a traveling-wave tube or klystron. The inputs are beam voltage U , current I , and waist radius r_w . The fourth input parameter is either the operating cathode current density J_c or the beam convergence ratio C , which is defined as the ratio of the radius of the cathode disc to that of the beam waist. Fig. 1 shows the parameters of the Pierce gun geometry.

The noniterative method was proposed by Tiwary and Basu [1], [4]. Like the iterative method, it also has the four aforementioned input design parameters and the same outputs. It is based on the logarithmic value of the ratio of the cathode-to-anode radii of curvature and is expressed in a power series directly in terms of the beam convergence ratio. This makes it possible to calculate the half-beam cone angle with the help of Langmuir–Blodgett's solution, which in turn facilitates the calculation of other output parameters. The throw of the gun is also expressed in a power series in terms of the ratio of the anode-aperture radius to the beam-waist radius. The accuracy of the results of Tiwary and Basu's noniterative method is comparatively good in the case of the gun's half-beam cone angle below 20° ; however, the accuracy of its

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