A HIGH-ENDURANCE (>100K) BE-SONOS NAND FLASH WITH A ROBUST NITRIDED TUNNEL OXIDE/SI INTERFACE

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ABSTRACT

For Solid-State Drive (SSD) applications cycling endurance of NAND flash is a critical challenge. In this work the endurance reliability of BE-SONOS NAND is thoroughly examined. Using dual *CV/IV* tests the impact of interface state (Dit) generation/annealing and real charge trapping (Q) on the endurance degradation has been clearly identified. For BE-SONOS with pure thermal oxide O1, the endurance degradation mainly comes from Dit generation at Si/O1 interface, while charge trapping in the thin ONO barrier is negligible even after 100K cycles of stressing. Meanwhile, the high-temperature V_T loss mainly comes from interface state annealing, while the real charge loss due to electron de-trapping is much smaller. This indicates that our nitride-trapping device has "deep" traps that well retain charges even after the tunnel barrier is damaged. Based on this understanding, we have introduced nitrided O1 to strengthen the Si/O1 interface, and both the endurance and retention are greatly improved. We demonstrate high-endurance BE-SONOS NAND devices of P/E > 5K for MLC and P/E > 100K for SLC operations with excellent retention, promising for solid-state drive (SSD) applications.

I. Introduction

Charge-trapping (CT) devices promise to continue the NAND Flash scaling and open the door for 3D NAND Flash. BE-SONOS [1, 2] is one of the promising solutions because it uses mature and mass-production proven materials of oxide, nitride and poly gate. These well understood materials help further improve the reliability.

Real charge loss (Q) and interface state (Dit) generation are two major causes for Flash memory device degradation. V_T will be impacted by both factors and the independent effects are difficult to be separated. Unlike the floating gate device, a large planar CT device can be operated in FN mode because there is no gate coupling ratio restrictions. This allows the measuring of *CV* and I_DVg on the same large-area device, where the V_{FB} is revealed from *CV* curve, and I_DVg provides the Vt. In this way both Q and Dit can be extracted separately by comparing V_{FB} and V_T, thus provides further understanding of endurance degradation.

II. Dual *CV/IV* Testing - Differentiating Charge Trapping (Q) from Interface State (Dit)

The schematic structure of BE-SONOS device is shown in Fig. 1. The O1 layer in this work was either a pure thermal oxide or thermally nitrided oxide with very well controlled thickness around 13Å. The dual *CV* and I_DVg testing is designed to differentiate the real charge trapping Q from interface state Dit. *CV* provides V_{FB} shift, which is related to the Q and is independent of Dit. On the other hand, I_DVg provides V_T shift, which is related to both Q and Dit. Thus by analyzing V_T and V_{FB} we can extract both Q and Dit. Moreover, the subthreshold swing (S.S.) change from I_DVg is directly related to Dit.

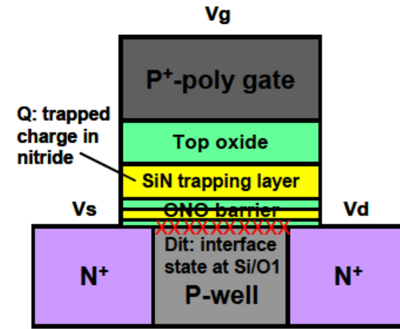

Fig. 1 Schematic structure of BE-SONOS device. Both the pure O1and the nitrided O1 are applied to evaluate the post-cycled real charge loss (Q) and interface state (Dit) generation.

The basic equations for the V_{FB} and V_T shifts are illustrated as followed:

V_{FB} equation:

$$V_{FB} = (\phi_{MS} - \frac{Q}{C_{OX}}) \quad (1)$$

V_T equation:

$$V_T = V_{FB} + 2\Psi_B + \frac{\sqrt{4\varepsilon_S q N_A (2\Psi_B + V_{BS})}}{C_{OX}} + \Delta V_T(Dit) \quad (2)$$

$$\Delta V_T(Dit) = S.S. \times [Log_{10}(I_D(@V_T)) - Log_{10}(I_D(@V_{MG}))] \sim \Delta S.S. \times 10 \quad (3)$$

According to the interface state model [3-6], interface state is neutral and inactive at mid-bandgap voltage (when surface band bending is at mid-bandgap, both acceptor and donor interface traps are neutral). The corresponding mid-bandgap current (I_{MG}) is unchanged after Dit generation. This is confirmed by simulation - the TCAD simulated I_{MG} is around 10^{-17}A for our device. Since the typical V_T is defined at 10^{-7}A, the V_T shift caused by S.S.

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degradation can be simply approximated by $\Delta V_T \sim 10\times\Delta S.S.$. This provides a way to estimate the contribution of S.S. changes to reliability degradation.

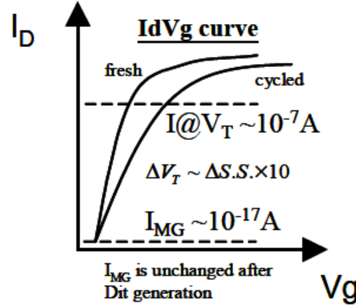

Fig. 2 Schematic diagram of I_DVg curves of fresh and P/E cycled devices. Midgap current (I_{MG}) is unchanged with Dit generation. However, S.S. is increased with Dit generation. Thus the IdVg curve rotates with respect to I_{MG}. Assuming $I_{MG}=10^{-17}$A, and Vt is defined at 10^{-7}A, a simple approximation gives $\Delta V_T - \Delta V_{FB} \sim 10\times\Delta S.S.$

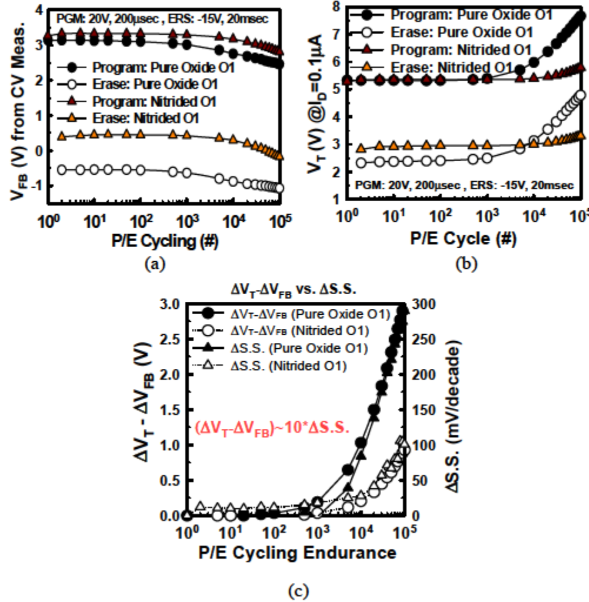

Fig. 3 Endurance comparison of two BE-SONOS devices with pure oxide O1 and nitrided O1. (a) V_{FB}'s during P/E cycling are relatively stable even after 100K cycling. The small V_{FB} roll-down is due to the interface state generation and *CV* distortion (in Fig. 5(a)). (b) The measured V_T during cycling. V_T roll-up happens severely for the pure oxide O1. On the other hand, the memory window is kept even V_T roll-up happens. Nitrided O1 shows significant improvement in endurance. (c) The subthreshold slope (S.S.) degradation (ΔS.S., right Y axis) is highly correlative with the V_T roll-up. $\Delta V_T - \Delta V_{FB} \sim 10\times\Delta S.S.$ is observed, consistent with the model in Fig. 2.

III. Reliability Study of BE-SONOS by Dual *CV/IV* Method

Figure 3 compares the endurance of BE-SONOS with pure oxide O1 and nitrided O1. In Fig. 3(a), the V_{FB} is very stable even after 100K cycling stressing. On the other hand, V_T in Fig. 3(b) shows very significant roll-up for pure oxide O1. Note that the cycling window is kept constant even with V_T roll up. This suggests that the FN tunneling speed is not degraded and the amount of stored charge remained the same even after 100K P/E cycles. On the other hand, Dit generation caused severe degradation of S.S. (Fig. 3(c)), leading to the V_T roll-up. It is interesting that the measured $\Delta V_T - \Delta V_{FB} \sim 10\times\Delta S.S.$, very consistent with our model.

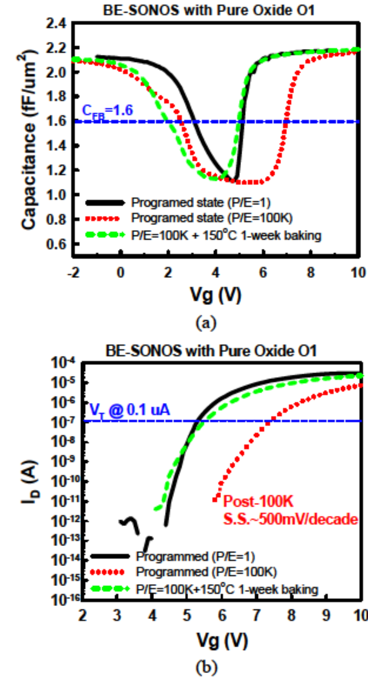

Fig. 4 (a) *CV* curves of post 100K P/E cycling and 150°C baking for BE-SONOS with **pure oxide O1**. *CV* curve has a large distortion and the inversion part is broadened after 100K PE cycling. At accumulation region, the *CV* curve is also distorted and V_{FB} shifts leftward. (b) I_DVg curves for the same device. *IV* curve shifts rightward, corresponding to the *CV* curve at the inversion region. Meanwhile, S.S. is strongly degraded. After 150°C 1-week baking, both *CV* and *IV* curves almost completely recover to fresh state. It should be noted that V_T and V_{FB} loss are different, which provides understanding of real charge loss (Q) and interface state generation (Dit).

Figure 4 compares the details of *CV* and I_DVg during P/E cycling for pure oxide O1. Dit generation is the major reason to the endurance degradation, which leads to *CV* stretch-out as well as V_T increase.

Note that the endurance degradation of BE-SONOS is quite different from the conventional floating gate device, where not only Dit is generated, but also memory window is gradually closed due to trapped electrons in tunnel oxide [5]. In BE-SONOS, both electron and hole tunneling happens during cycling, which neutralizes any charge trapped in the tunneling barrier. Thus the major endurance degradation of BE-SONOS comes from Dit generation instead of FN tunneling speed degradation.

The nitrided tunnel oxide is widely used in floating gate technology [5] to produce a stronger interface against Si dangling bond generation. For this work we have developed a very thin nitrided O1 to reduce Dit generation in BE-SONOS device. By comparing to pure oxide O1, great improvements of endurance to >100K are clearly shown with nitrided O1 (Fig. 3). Both *CV* and *IV* degradation are also much smaller, as shown in Fig. 5.

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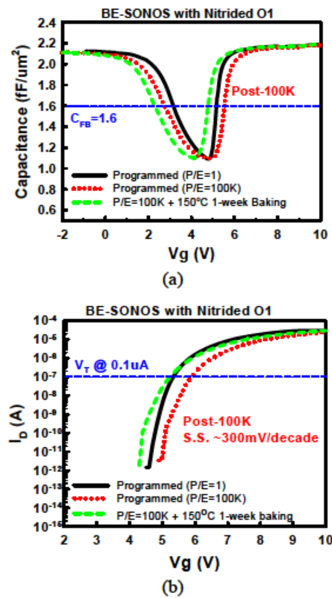

Fig. 5 (a) Detail *CV* curves during 100K P/E cycling and 150°C baking for BE-SONOS with **nitrided O1**. (b) Detail *IV* curve for the same device. Both *CV* and *IV* degradation are much smaller for nitrided O1. In *CV* curve, the *CV* stretching after cycling is suppressed. During baking, *CV* curves shift in parallel, thus V_T and V_{FB} loss are similar.

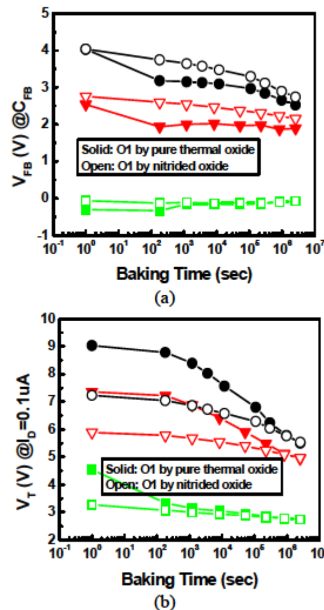

Fig. 6 (a) V_{FB} loss during 150°C baking after 100K P/E cycling. V_{FB} loss is small (<500mV) even after 100K cycling, indicating the real charge loss is very small even after 100K cycling. (b) V_T loss for the same device. V_T loss is much larger than V_{FB} loss for **pure oxide O1**, while the two values are quite similar for **nitrided O1**. Moreover, pure oxide O1 has much more V_T loss than nitrided O1 and less dependent on initial V_{FB} state, suggesting that the V_T loss is not dominated by real charge loss but Dit annealing. After 1-week baking, V_T loss of pure oxide O1 is about 2 V, while V_{FB} loss is ~500mV. Therefore, the estimated interface annealing effect contributes to ~1.5 V, which is approximately 10 times of S.S. recovery in Fig. 7.

The retention results are shown in Figs. 6-7. For pure oxide O1, the V_{FB} loss (real charge loss) is much smaller than V_T loss, indicating that the V_T loss mainly comes from interface annealing [5, 6], while real charge loss is much smaller. The annealing of interface state (Fig. 7(a)) is also observed from the S.S. recovery during baking (Fig. 7(b)). The total V_T loss can be approximated by real charge loss (V_{FB} loss) + interface anneal ($\sim 10\times\Delta S.S.$), or $\Delta V_T - \Delta V_{FB} \sim 10\times\Delta S.S.$ The experimental results show very good agreement with this model.

For nitrided O1, the suppressed S.S. degradation and V_T roll-up are shown (Fig. 3). Furthermore, V_T loss is comparable to V_{FB} loss during baking (Fig. 6), indicating the suppressed Dit generation after P/E cycling.

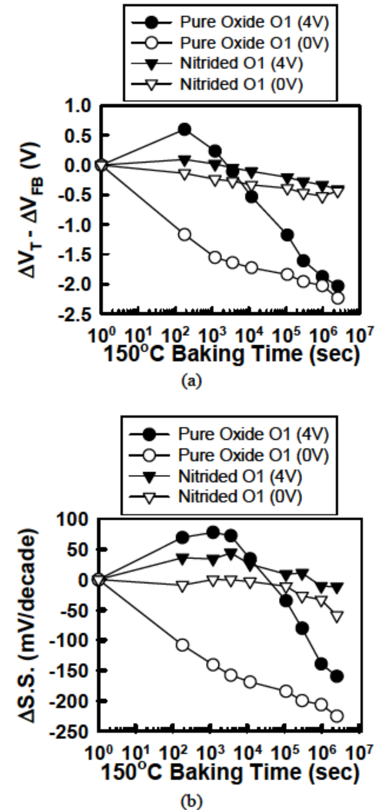

Fig. 7 (a) Interface-state annealing ($\Delta V_T - \Delta V_{FB}$) and (b) S.S. recovery (ΔS.S.) during 150°C baking for pure oxide O1 and nitrided O1 samples after 100K cycling. Significant suppression of interface-state annealing and S.S. recovery are revealed in the devices with nitrided O1. In addition, $\Delta V_T - \Delta V_{FB} \sim 10\times\Delta S.S.$ is also observed.

IV. Performances of BE-SONOS NAND Flash Using the Nitrided O1

(1) Cycling Endurance: The cycling endurance of BE-SONOS NAND cell is shown in Fig. 8. S.S. starts to degrade only after 10K cycling. After 100K cycling, S.S. only degrades by 100mV/decade, and the read current degradation is less than 20%. With suitable P/E conditions, more than 1M cycling endurance is achieved, as shown in Fig. 9.

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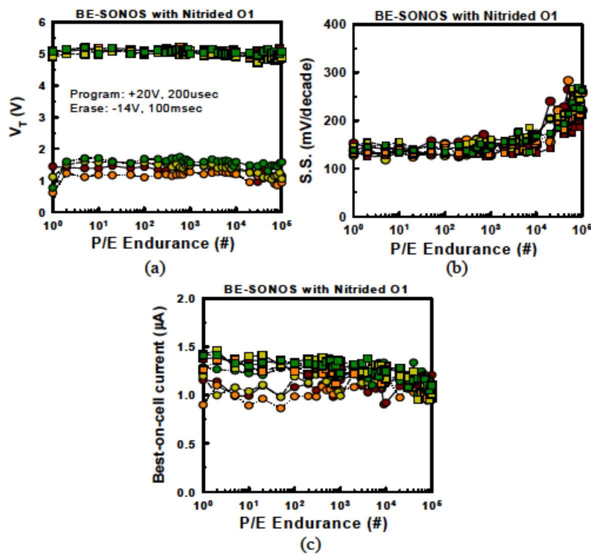

Fig. 8 (a) Endurance characteristics of BE-SONOS NAND device with **nitrided O1**. Several identical devices are collected. Dumb-mode P/E cycling (without any P/E verify) shows no degradation even after 100K cycling. (b) S.S. during 100K P/E cycling. S.S. shows no degradation below 10K cycling. After 100K, S.S. degradation is only about 100mV/decade. (c) the best-on-cell current under V_{pass}=7V, and read gate-overdrive (Vg-V_T) =1V.

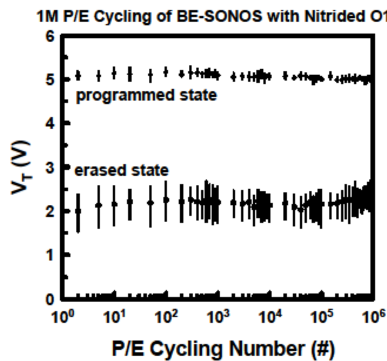

Fig. 9 1M PE cycling endurance distribution collected from many cells. With suitable P/E algorithms, 1M cycling can be achieved.

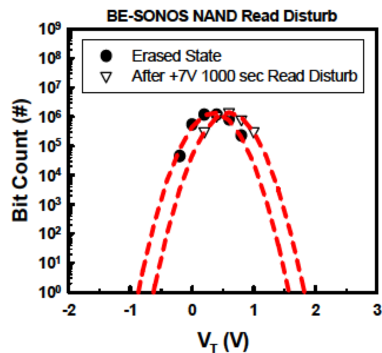

Fig. 10 Typical read disturb behavior at $V_{pass,read}$=7V and 1000 sec. The corresponding read cycle time is more than 10M.

(2) Read Disturb: Typical read disturb distribution analysis is shown in Fig. 10. More than 10M read is guaranteed.

(3) Self-Boosting Characteristics: The typical global self-boosting characteristics are shown in Fig. 11. More than 4V disturb-free window is achieved with V_{pass} = 10V. After 100K P/E cycling, self-boosting is only slightly degraded, allowing enough memory window design.

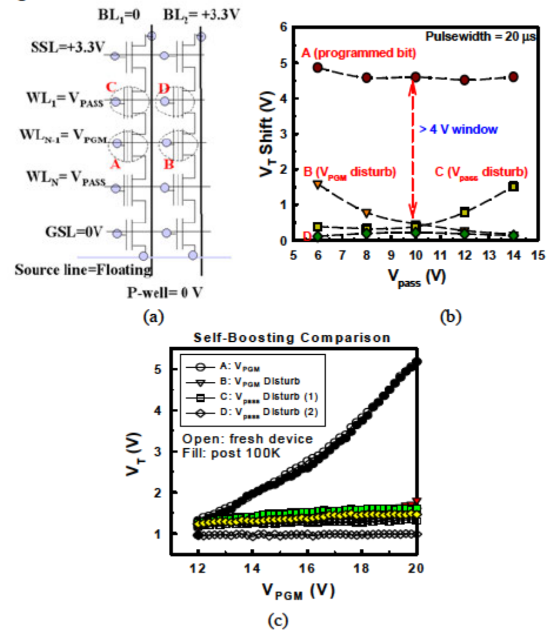

Fig. 11 (a) Self-boosting operation method. (b) Self-boosting V_{pass} disturb window. Increased V_{pass} shows suppressed V_{PGM} disturb, but increased V_{pass} disturb. V_{pass} ~ 10 V is the optimized condition. The disturb-free memory window is more than 4V. (c) Self-boosting operation before and after 100K cycling. Post 100K cycling still shows successful self-boosting disturb window.

(4) Data Retention: The memory window and post-cycling retention properties are shown in Figs. 12-13. Figure 12 shows that below 5K cycling the retention properties are quite enough for MLC design. After a strong P/E cycling (>100K) as shown in Fig. 13, the retention is still reasonable for SLC design.

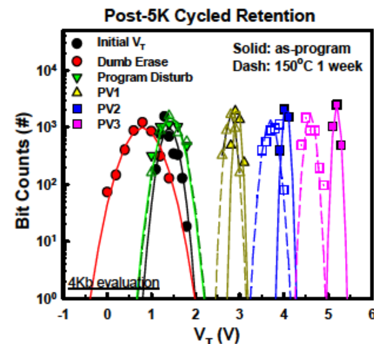

Fig. 12 The MLC distribution and post-5K cycled 150°C retention result for BE-SONOS with nitrided O1. Post 5K cycling and 150°C baking shows reasonable window for MLC operation.

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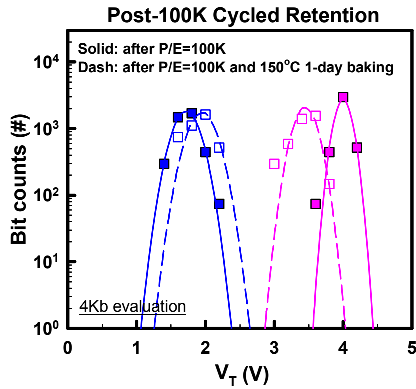

Fig. 13 The SLC distribution and post-100K cycled 150°C retention result for BE-SONOS with nitrided O1. Post 100K cycling and 150°C baking shows enough window for SLC operation.

V. Conclusions

We have clarified that the major endurance degradation mechanism of BE-SONOS NAND using pure oxide O1 is the interface state (Dit) generation/annealing. By developing a nitrided O1 that strengthens the Si/O1 interface, the endurance and retention are greatly improved. A high-performance BE-SONOS NAND Flash with P/E > 5K for MLC and P/E > 100K for SLC operation is developed.

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