UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Petitioner
v.

MICRON TECHNOLOGY, INC.,
Patent Owner

IPR2025-00498
U.S. Pat. 8,803,214

PATENT OWNER'S PRELIMINARY RESPONSE

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All emphases in quotations are added unless otherwise noted.

This paper includes color illustrations and should be viewed in color.

I. INTRODUCTION

Patent Owner Micron Technology, Inc. ("Micron" or "Patent Owner") submits this preliminary response to Yangtze Memory Technologies Company, Ltd.'s ("YMTC's" or "Petitioner's") Petition for *Inter Partes* Review (Paper 1, the "Petition") of U.S. Pat. 8,803,214 (the "'214 patent"). The Board should deny institution.[1]

First, YMTC—an entity created, owned, and controlled by the Chinese government—is not a statutorily authorized "person" entitled to file an IPR petition under the Supreme Court's holding in *Return Mail, Inc. v. U.S. Postal Service*, 587 U.S. 618 (2019). §IV.

Second, YMTC omitted the Chinese government as a real party-in-interest even though it has a substantial vested interest in the outcome of this proceeding, will benefit from any redress, and has an established relationship with YMTC.

[1] Micron's Discretionary Denial Brief (Paper 7) raised the first two arguments set forth below: (1) "Petitioner Is Not A 'Person' Entitled To File An IPR Petition" (§IV.A); (2) "Petitioner Failed To Identify All RPIs" (§IV.B). To the extent the Director finds that these arguments are non-discretionary and should be decided by the Board, Patent Owner repeats those arguments (and the underlying factual background) here.

This omission was not a good-faith mistake but a strategic maneuver to shield the Chinese government (and its other state-owned entities) from, e.g., the statutory estoppel provisions of Title 35. Even if YMTC moves to amend its RPI identification to add the Chinese government, doing so now would be beyond the §315(b) one-year bar. §V.

The Board also should deny institution because the Petition presents an insufficient number of challenges that meet the reasonable likelihood standard, rendering institution an inefficient use of resources. *Chevron Oronite Co. LLC v. Infineum USA L.P.*, IPR2018-00923, Paper 9 (PTAB Nov. 7, 2018) (informative). Petitioner takes a kitchen sink approach, challenging 18 claims in seven Grounds and hoping that one of them will stick. Petitioner advances two primary references: Kang and Fukuzumi. As summarized below, however, Kang is fundamentally different than the '214 patent, and all challenges involving Kang (Ground 1-3) have no chance to prevail on the merits. Similarly, for the vast majority of claims, Fukuzumi lacks a critical, express claim limitation.

A key component of the '214 patent is locating the "***memory elements***" in a ***cavity*** of the gate layer. The claims and specification make clear that this arrangement is central to the invention. The '214 patent accomplishes this by forming a stack of alternating gate layers and dielectric layers, then forming

cavities through the stack, and then forming the memory elements therein. Hence, the "memory elements" are located in cavities of the gate layers.

Petitioner relies on Kang (EX1004) as the primary reference for Grounds 1-3. But Kang's approach is fundamentally different than the '214 patent, and Petitioner either misread Kang or conveniently ignored a critical aspect of its structure. Kang teaches forming vertical pillars with memory elements directly from a bulk substrate. There is no stack of alternating and dielectric layers at this point in the Kang process. Thus, there is no stack (with gate layers) in which to form cavities and in which to locate the memory elements. Rather, after Kang forms the memory elements, Kang forms the stack to abut the memory elements.

For Grounds 4-7, Petitioner relies on Fukuzumi (EX1007) as the primary reference. These Grounds, just like the Kang grounds, have a fatal flaw. Of the three challenged independent claims, independent claims 1 and 9 of the '214 Patent recite a "common source." In another IPR proceeding, Petitioner expressly recognizes that not all 3D NAND devices employ a "common source." But here, Petitioner's claim mapping assumes that all 3D NAND devices, including Fukuzumi, employ a common source. Specifically, Petitioner assumes that Fukuzumi's disclosure of a "B***a1***" source refers to a single structure that must be "common" to all channel structures in Fukuzumi—even though in the same paragraph of that disclosure, Fukuzumi uses variables such as "***a1***" to denote one

structure of many. Put simply, Petitioner's assumption that "B***a1***" is a single structure that is common among all channel structures does not withstand scrutiny.

The Board should discretionarily deny institution because proceeding to trial on Petitioner's petition, which includes seven Grounds and challenges 18 claims, would be an inefficient use of the Board's limited time and resources (as well as those of the parties) given the fundamental flaws that permeate the petition. §XI.

II. FACTUAL BACKGROUND

A. Micron Is A Pioneer In NAND Flash Memory

NAND flash memory is a crucial component in the semiconductor ecosystem. It is a type of memory that does not lose data when it loses power. Conventional NAND stores data in memory cells laid out in an array of rows and columns. Historically, NAND arrays were laid out two-dimensionally in a single layer. But, as demand for data storage grew, the semiconductor industry developed multi-layer NAND devices, in which layers of NAND memory cells are stacked vertically on top of each other. This is 3D NAND. By stacking layers vertically, 3D NAND dramatically increases memory storage capacity compared to conventional NAND.

Micron began its pioneering work in developing 3D NAND products over a decade ago. Micron invested billions of dollars and years of effort towards researching, developing, and manufacturing 3D NAND technology. As part of this

effort, Micron filed for (and obtained) numerous U.S. patents on this technology no later than 2010. This culminated in Micron launching its first 3D NAND product on March 26, 2015. EX2001 (Micron "3D NAND Flash Memory" Press Release) at 1-2. Since then, Micron has continued to innovate its 3D NAND technology by developing memory products with more and more capacity and capabilities. Micron has received numerous awards and widespread recognition for its innovation (*see, e.g.*, EX2002 (Micron "Best of Show Award" Press Release) at 1), and it is a leading innovator—both in the U.S. and globally—of semiconductor memory devices, with over 57,000 patents (*see* EX2003 (Micron Form 10-K (2024)) at 2). In fact, Micron (headquartered in Boise, Idaho) remains the only U.S.-based manufacturer of semiconductor memory devices.

B. The Chinese Government's Control of Its Semiconductor Industry

A close examination of the Chinese government's strategic initiatives and investments in the semiconductor industry yields a clear understanding of Petitioner. For more than a decade, the Chinese government has invested heavily in the semiconductor industry within its borders and set policies for Chinese semiconductor companies. In June 2014, China's State Council announced its "National Integrated Circuit Industry Development Outline" with the "goal of establishing a world-leading semiconductor industry in all areas of the integrated circuit supply chain." *See* EX2005 (Translation of EX2004 (National IC

Development Promotion Outline)) at 1; EX2006 (Semiconductors and the CHIPS Act: The Global Context) at 19-20. It sought to "better play the role of the government," remove "bottleneck[s] of industrial development," establish "a national integrated circuit industry development leading group … for the overall coordination of the integrated circuit industry," and create "a financing platform and policy environment." EX2005 at 1-2; EX2006 at 19-23.

The Chinese government then created the "National Integrated Circuit Industry Investment Fund" (or "Big Fund") and raised 138.7 billion yuan from multiple government and state-owned enterprises,[2] including China's Ministry of Finance. EX2007 (Case Study: From Paper Tiger to Real Tiger?) at 5; *see id.* at 3-7. The Big Fund aimed to "***support[] the integrated circuit manufacturing field***," "implement mergers," and "***standardize corporate governance***." EX2005 at 2.

[2] According to China's State Council, the term "state-owned enterprise" includes "state-owned enterprises, state-owned companies and state-owned capital holding companies that the State Council and local people's governments respectively perform the duties of investors on behalf of the state, including enterprises supervised by central and local state-owned assets supervision and administration agencies and other departments at the same level and enterprises formed by their investment at each level." EX2009 (Translation of EX2008 (SASAC Definition)).

In May 2015, China's State Council launched its "Made in China 2025" initiative. EX2011 (Translation of EX2010 (Made In China 2025)). The initiative set an ambitious ten-year roadmap for China to become a global leader in high-tech industries and officially solidified the semiconductor industry as one of the Chinese government's targets. EX2011 at 1-13 (*e.g.*, "[W]e must seize the current rare strategic opportunities, actively respond to challenges, strengthen overall planning, highlight innovation-driven, formulate special policies, give full play to institutional advantages, mobilize the whole society to work hard, rely more on Chinese equipment and Chinese brands, … and complete the strategic task of transforming Chinese manufacturing from big to strong."), 30.

The "Made in China 2025" initiative also outlined a comprehensive set of strategic goals, emphasizing the government's central role in control and financing.[3] *Id.* at 8-9 (*e.g.*, "Market-led, ***government-guided***. Comprehensively deepen reform, give full play to the decisive role of the market in resource allocation, strengthen the dominant position of enterprises, and stimulate the

[3] *See also* EX2047 (Translation of EX2046 (State Council Notice on Policies to Promote Development of IC)) at 4-5 ("Strengthen services and guidance for the construction of major integrated circuit projects [and] orderly guide and regulate the development of the integrated circuit industry"), 8-9.

vitality and creativity of enterprises. ***Actively transform government functions, strengthen strategic research and planning guidance***, improve relevant support policies, and create a good environment for enterprise development."), 37, 39, 41-44 (*e.g.*, "***Deepen the reform of state-owned enterprises*** [and] ***improve the corporate governance structure***…."). Indeed, the U.S. Congressional Research Service (CRS) explained:

> ***China's policies feature a substantial and central role for the government in directing and financing Chinese businesses*** to obtain foreign IP related to semiconductors. The Chinese government uses production targets; subsidies; tax preferences; trade and investment barriers (including pressure to engage in joint ventures); and discriminatory antitrust, IP, procurement, and standards practices. The policies seek to leverage China's central role in global consumer electronics manufacturing and potential as a semiconductor production hub to incentivize and pressure foreign companies to localize production, share technology, and partner with the Chinese government and affiliated entities.

EX2012 (China's New Semiconductor Policies: Issues for Congress) at 6; *see also id.* at 7-11.

C. YMTC Is China's State-Owned NAND Memory Company

In pursuit of its "Made in China 2025" initiative, the Chinese government tasked Tsinghua Unigroup, a state-controlled company, with leading the country's

memory chip development. *See* EX2014 (Translation of EX2013 (*People's Paper* Article)) at 2; EX2017 (Stephen Ezell Testimony) at 7. On July 26, 2016, Tsinghua Unigroup—jointly with the Big Fund and municipal governments—founded YMTC to develop NAND memory. EX2016 (Translation of EX2015 (YMTC Press Release)) at 1. This joint venture initially invested more than $24 billion (USD) in YMTC. *See* EX2017 at 7. Since then, the Chinese government has continued to invest heavily in YMTC. In 2023, for example, the Chinese government invested another $7 billion (USD) through various investment vehicles, such as the second phase of its Big Fund. EX2018 (*Yahoo!* Article) at 1; EX2020 (Translation of EX2019 (*Baidu* Article)) at 1-2.

The Chinese government not only invests heavily in YMTC, but it also owns and controls YMTC. YMTC is wholly owned by one parent corporation: Yangtze Memory Technologies Holding Co., Ltd. ("YMTC Holding"). *See* EX2021 (YMTC's Corporate Disclosure Statement) at 2. And YMTC Holding is owned by the following state-owned enterprises (as of March 12, 2025):

Shareholder	**Ownership**
Hubei Changsheng Development Co., Ltd. (湖北长晟发展有限责任公司), a state-owned enterprise	~29%
Wuhan Xinfei Technology Investment Co., Ltd. (武汉芯飞科技投资有限公司), a state-owned enterprise	~27%
National IC Industry Investment Fund Co., Ltd.	~13%

Shareholder	Ownership
(国家集成电路产业投资基金股份有限公司), a state-owned enterprise	
National IC Industry Investment Fund Phase II Co., Ltd. (国家集成电路产业投资基金二期股份有限公司), a state-owned enterprise	~12%
Hubei Science & Technology Investment Group Co., Ltd. (湖北省科技投资集团有限公司), a state-owned enterprise	~10%
Hubei Guoxin Industry Investment Fund Partnership (L.P.) (湖北国芯产业投资基金合伙企业 (有限合伙)), a state-owned enterprise	~6%
Yangtze Industrial Investment Group Co., Ltd. (长江产业投资集团有限公司), a state-owned enterprise	~3%
Total	**100%**

See EX2023 (Translation of EX2022 (2024 Tracking Rating Report)) at 9-10; EX2027 (Translation of EX2026 (*Sina Finance* Article)) at 1 ("Yangtze Memory is a state-controlled enterprise … [where] all seven shareholders of Yangtze Memory Technologies Holdings Co., Ltd. are state-owned assets."); EX2020 at 1-2 ("Hubei Changsheng Development Co., Ltd. is held by Hubei Integrated Circuit Industry Investment Fund, Wuhan Optics Valley Finance and Yangtze River Industrial Investment Group"—with the actual "controller behind the scenes [being the governmental] Administration of Wuhan East Lake High-tech Development Zone…. [The] actual controller of Yangtze River Industrial Investment Group is

the Hubei Provincial State-owned Assets Supervision and Administration Commission…. [The] actual controller of Hubei Guoxin Industry Investment Fund Partnership (Limited Partnership) is the Wuhan State-owned Assets Supervision and Administration Commission, and the actual controller of Hubei Science [&] Technology Investment Group Co., Ltd. is the [governmental] Administration of Wuhan East Lake High-tech Development Zone."). All shareholders (listed above) are state-owned enterprises and, therefore, YMTC Holding and YMTC are state-owned. *See* EX2023 at 9-10; EX2027 at 1; EX2020 at 1-2.

This ownership structure and the Chinese government's significant investment (*i.e.*, tens of billions of U.S. dollars) clearly show that YMTC serves the Chinese government's semiconductor strategy and operates under the direction and control of the Chinese government. Indeed, China's State Council has described YMTC as a "state-owned enterprise." EX2025 (Translation of EX2024 (Statement of China's State Council)) at 2. And Chinese media outlets and Chinese universities identify YMTC as a "state-owned enterprise" or "state-controlled enterprise." EX2027 at 1 ("***Yangtze Memory [Technologies, Inc.] is a state-controlled enterprise***"); *see also, e.g.*, EX2029 (Translation of EX2028 (Southeast Univ., YMTC 2024 Campus Recruitment)) at 1 ("***Nature of [YMTC]: State-owned enterprise***"); EX2031 (Translation of EX2030 (Wuhan Univ. of Sci. and Tech., YMTC 2020 Campus Recruitment Introduction)) at 1 (same); EX2033

(Translation of EX2032 (China Univ. Of Petroleum, YMTC 2025 Campus Recruitment)) at 1 (same); EX2035 (Translation of EX2034 (*WSJ China* Article)) at 1-2 ("***China's state-owned enterprise Yangtze Memory Technologies Co. Ltd***…. ***Yangtze Memory is controlled by the Hubei Provincial Government and the China National Integrated Circuit Industry Investment Fund***.").

D. Bipartisan U.S. Policymakers And The U.S. Administration Agree That The Chinese Government Controls YMTC

U.S. policymakers consistently highlight the Chinese government's ownership and control over YMTC. In July 2021, U.S. Senator Bill Hagerty and U.S. Representative Michael McCaul urged the U.S. Commerce Secretary to add YMTC to the Department of Commerce's Entity List because it "has clear ties to the Party-state and military and plays a significant role in CCP plans to control the supply chain for a strategic dual-use sector." EX2036 (July 12, 2021 Letter from McCaul and Hagerty) at 1-2. They explained that:

> ***YMTC is the PRC's state-owned national champion for memory chips*** — a type of semiconductor with defense, artificial intelligence, and aerospace applications. YMTC was created as a joint-venture by the National Integrated Circuit (IC) Industry Investment Fund, Tsinghua Unigroup (a state investment firm that is one of the IC Fund's shareholders), the Hubei IC Industry Fund (a regional branch of the national IC Fund), and the Hubei Science and Technology Investment Group (an investment vehicle of the Wuhan Municipal Government

> that provides capital investment, infrastructure and services for the PRC's strategic industries, including semiconductors).

Id.; *see also* EX2037 (*Financial Times* Article) at 2 ("The White House has described YMTC as a Chinese 'national champion.'").

In April 2022, Mr. Stephen Ezell, Vice President of Global Innovation Policy at the Information Technology and Innovation Foundation, testified before the U.S.-China Economic and Security Review Commission (which is a bipartisan legislative commission created by the U.S. Congress) on "U.S.-China Innovation, Technology, and Intellectual Property Concern." EX2017 at 1, 3. In his testimony, he explained:

> ***[YMTC] is a Chinese state-controlled joint venture stood up from whole cloth by the National IC Industry Investment Fund***, the state university-controlled fabless semiconductor firm Tsinghua Unigroup, and the Hubei Science and Technology Investment Group, supported by $24 billion in initial government funding allocated for its initial Wuhan factory alone. ***In effect, YMTC is China's state-owned national champion for memory chips***.

Id. at 7. Similarly, in September 2022, U.S. Senator Mark Warner stated it "has been clear for some time now that YMTC is … a key part of the Chinese Communist party's goal of shifting control of global microelectronics to the PRC." EX2037 at 2. Similarly, in December 2022, U.S. Senator Charles E. Schumer

called YMTC a "CCP-backed technology compan[y]." EX2038 (Schumer Statement) at 1.

The U.S. Administration further corroborates that YMTC is state-controlled. For example, pursuant to Section 1260H of the William M. (Mac) Thornberry National Defense Authorization Act, the Secretary of Defense must identify entities that the Secretary "determines" to be a "Chinese military company" "based on the most recent information available." H.R. 6395, 116th Cong. §1260H(a), (d) (2021). A "Chinese military company" refers to any entity that is "directly or indirectly owned, controlled, or beneficially owned by, or in an official or unofficial capacity acting as an agent of or on behalf of, the People's Liberation Army or any other organization subordinate to the Central Military Commission of the Chinese Communist Party"—i.e., an entity that is owned and/or controlled by the Chinese government. *Id*., §1260H(d). On January 31, 2024, the Department of Defense identified YMTC as a "Chinese military compan[y]." EX2039 (DOD Press Release) at 1; EX2040 (List of Chinese Military Companies) at 1, 3; *see also* 90 Fed. Reg. 1105 (Jan. 7, 2025) (same).

III. PROCEDURAL BACKGROUND

YMTC sued Micron in the Northern District of California on November 9, 2023, alleging that certain Micron 3D NAND products infringe eight YMTC patents. C.A. No. 3:23-cv-05792, D.I. 1 (Nov. 9, 2023). YMTC concurrently filed

a "Corporate Disclosure Statement," in which YMTC represented that its sole parent corporation is YMTC Holding and that "no publicly held corporation owns 10 percent or more of its stock." EX2021 at 2. YMTC subsequently filed a First Amended Complaint, maintaining its original allegations of infringement across the same eight patents.[4] C.A. No. 3:23-cv-05792, D.I. 29 (Feb. 2, 2024).

On February 16, 2024, Micron served its Answer to the First Amended Complaint and Counterclaims against YMTC and Yangtze Memory Technologies, Inc. ("YMTI"), alleging infringement of the '214 patent and four other Micron patents.[5] *Id.*, D.I. 35 (Feb. 16, 2024). The §315(b) one-year period to file IPR petitions commenced on February 16, 2024 and expired February 16, 2025.

[4] YMTC filed a separate action against Micron on July 12, 2024, asserting an additional eleven patents. C.A. No. 5:24-cv-04223, D.I. 1 (July 12, 2024). The district court consolidated this second action with the first-filed action, bringing the total number of YMTC patents asserted against Micron to nineteen. C.A. No. 3:23-cv-05792-RFL, D.I. 106 (Aug. 21, 2024).

[5] The other asserted Micron patents are U.S. Patent Nos. 10,872,903 (the "'903 patent"), 8,945,996 (the "'996 patent"), 10,373,974 (the "'974 patent"), and 10,475,737 (the "'737 patent").

On February 14, 2025, YMTC filed two IPR petitions against the '214 patent. IPR2025-00498, Paper 1 ("Pet."); EX2052 (IPR2025-00499, Paper 1). YMTC identified itself and YMTI as the only real parties-in-interest. Pet., 1-2. Notably, in its Petition, YMTC chose not to add as real parties-in-interest its sole parent corporation (YMTC Holding) or the Chinese government, which owns and controls both YMTC Holding and YMTC. The PTAB accorded a filing date on April 17, 2025. IPR2025-00498, Paper 6. On April 21, 2025, Micron filed Patent Owner's Discretionary Denial Briefing, also making substantially identical arguments to those herein (*i.e.*, in §§IV and V). IPR2025-00498, Paper 7.

Separate from its challenge to the '214 patent, YMTC also filed IPR petitions against the other four patents that Micron asserted through counterclaims. *See* IPR2025-00098, -00099, -00500, -00501. Again, YMTC lists only itself and YMTI (a subsidiary) as real parties-in-interest for these IPR petitions. It chose not to list YMTC Holding or the Chinese government.

On March 12, 2025, Micron filed Patent Owner Preliminary Responses in IPR2025-00098 and -00099 (collectively, "POPRs"), making substantially identical arguments to those herein (*i.e.*, in §§IV and V). IPR2025-00098, Paper 8 (Mar. 12, 2025); IPR2025-00099, Paper 8 (Mar. 12, 2025). Thereafter, YMTC sought leave to file 10-page preliminary replies to address Micron's arguments "with the option to submit additional evidence" but ***not*** to "submit any additional

declarations."[6] EX2050 (Correspondence), 2. The Board granted YMTC's request. *Id.*, 1.

On April 11, 2025, YMTC filed its Preliminary Replies (collectively, "Replies") to Micron's POPRs. IPR2025-00098, Paper 12 (Apr. 11, 2025); IPR2025-00099, Paper 12 (Apr. 11, 2025). In its Replies, YMTC argued that it "is a private company with independent control over its actions"—without providing any declaration in support. Replies, 2.[7] Seven days later, on April 18, 2025, Micron filed its Preliminary Sur-replies (collectively, "Sur-replies"). IPR2025-00098, Paper 13 (Apr. 18, 2025); IPR2025-00099, Paper 13 (Apr. 18, 2025).

On June 10, 2025, the Board instituted an *inter partes* review in IPR2025-00098 and -00099. IPR2025-00098, Paper 15 (June 10, 2025); IPR2025-00099, Paper 15 (June 10, 2025).

On June 24, 2025, Micron filed Patent Owner's Requests for Director Review in response to the Board's Institution Decision. IPR2025-00098, Paper 17

[6] YMTC elected to forgo submitting a reply declaration shortly after Micron informed YMTC that it would seek leave to depose any fact declarant.

[7] YMTC filed identical Preliminary Replies in IPR2025-00098 and -00099, so Micron cites them herein collectively as "Replies."

(June 24, 2025); IPR2025-00099, Paper 17 (June 24, 2025). Thereafter, on June 30, 2025, YMTC filed Authorized Responses to Director Review Request. IPR2025-00098, Paper 18 (June 30, 2025); IPR2025-00099, Paper 18 (June 30, 2025).

The panel did not adopt Patent Owner's *Return Mail* and real-party-in-interest arguments in IPR2025-00098 and -00099 and instituted IPR in both proceedings. *See* IPR2025-00098, Paper 15 at 15-21 (June 10, 2025); IPR2025-00099, Paper 15 at 18-25 (June 10, 2025). When analyzing Patent Owner's *Return Mail* argument, the Board in the -098 and -099 proceedings relied on a panel ruling in *TikTok Inc. v. Cellspin Soft, Inc.*, IPR2024-00757, Paper 33 at 12 (PTAB June 2, 2025). *E.g.*, IPR2025-00098, Paper 15 at 18 (citing *TikTok*). The Director *sua sponte* ordered Director Review of the panel decision in *TikTok* (addressing similar *Return Mail* and real-party-in-interest arguments) and stayed the IPR proceedings. IPR2024-00757, Paper 34 (Order Initiating *Sua Sponte* Director Review). Director Review in the *TikTok* IPRs remains pending. Micron sought Director Review of the panel decisions instituting IPR in both the -098 and -099 proceedings. *See* IPR2025-00098, Paper 17 and IPR2025-00099, Paper 17. Director Review in the -098 and -099 proceedings remains pending.

IV. PETITIONER IS NOT A "PERSON" ENTITLED TO FILE AN IPR PETITION

The Board should deny institution because YMTC is not statutorily authorized to file an IPR petition. Title 35 U.S.C. §311(a) allows only "person[s]" (other than the patent owner) to file a petition for *inter partes* review. "The patent statutes do not define the term 'person,'" but in *Return Mail, Inc. v. U.S. Postal Service*, the U.S. Supreme Court held that the term "person" does not include the U.S. government based on "longstanding interpretive presumption[s]" that "the sovereign" is not a "person." 587 U.S. at 626. The Supreme Court pointed to the "Dictionary Act," which guides courts on "the meaning of any Act of Congress, unless the context indicates otherwise." *Id.* at 627. The Dictionary Act defines "person" as including "corporations, companies, associations, firms, partnerships, societies, and joint stock companies, as well as individuals"—***but notably omits*** any term suggesting that a government entity is a "person." *See id.* Thus, the Supreme Court held the U.S. Postal Service ("USPS")—a federal "agency"—was not a "person" and was not authorized to file an IPR petition. *Id.* at 626.

The Supreme Court's reasoning in *Return Mail* applies with equal (if not more) force to foreign governments—and government agencies and entities under government control. The Dictionary Act identifies a broad range of entities as persons but does not include foreign or domestic governments. *Return Mail*, 587 U.S. at 627. And nothing suggests that Congress created a patent review process

that prohibits U.S. federal agencies from challenging U.S. patents (as the Supreme Court held) but allows *foreign* governments (or government agencies) to do so. Thus, the Board should interpret this "express directive from Congress" to exclude foreign governments. *Id.*

Given the *Return Mail* reasoning, Petitioner is not an authorized "person." The USPS (with respect to the U.S. government) is analogous to YMTC (with respect to the Chinese government). Unlike most federal agencies, Congress transformed the postal service in 1970 from a cabinet-level department (i.e., the Post Office Department) into a self-sustaining "independent" enterprise (i.e., USPS), controlled by the U.S. government. *See* The Postal Reorganization Act, Pub. L. No. 91-375, 84 Stat. 720 §201 (1970). That means the USPS generally does not receive taxpayer dollars for operating expenses but relies instead on the services and products it provides to consumers. *See, e.g.*, EX2042 (USPS Postal Facts) at 1-2. It does, however, still receive investments from the U.S. government to, for example, upgrade its vehicle "infrastructure to support zero-emission delivery vehicles." *See* Inflation Reduction Act, Pub. L. No. 117-169, 136 Stat. 2087 (2022).

Moreover, like any other private company, the USPS can borrow money, issue bonds, and own property in its own name. *See* The Postal Reorganization Act, Pub. L. No. 91-375, 84 Stat. 722-23, 740 §§401, 2005. A "Board of

Governors," similar to a board of directors, oversees the USPS. *Id.*, 84 Stat. 720 §202. And, importantly, the USPS competes with private companies (like FedEx and UPS) in an open marketplace. While not incorporated, it is clear that the USPS closely resembles any other private enterprise owned and controlled by a government.

YMTC is no different than the USPS. The Chinese government heavily invests in, owns, and controls YMTC. *See supra* §II.A-D. At the same time, however, YMTC (a) relies on the sales of products to cover expenses, (b) presumably can borrow money, issue bonds, and own property, (c) is overseen by a board, and importantly, (d) competes against private companies in the semiconductor industry. In short, YMTC is the same type of government entity as the USPS.

In its Replies, YMTC faults Micron for relying "solely" on one case for its statutory interpretation argument. Replies, 5. But the case on which Micron relies—*Return Mail*—is controlling Supreme Court precedent and constitutes the best case on which Micron (or the Board) could rely. YMTC attempts to distinguish itself from the Postal Service in *Return Mail* because the Court noted that non-government actors "face greater and more uncertain risks" in litigation (*e.g.*, the possibility of punitive damages and injunctive relief) than government entities. *Id.*, (citing *Return Mail*). But the Supreme Court's decision did not turn

on this distinction, rendering irrelevant the fact that Micron counterclaimed against YMTC. *Id.*, 5-6. Moreover, given that YMTC sued Micron in district court, Micron's assertion of counterclaims against YMTC, rather than naming the Chinese government, is unsurprising.[8]

In its Replies, YMTC also contends that *Bozeman Fin. LLC v. Fed. Rsrv. Bank of Atlanta*, 955 F.3d 971, 975-976 (Fed. Cir. 2020), counsels for a different result (Replies, 6-7), but *Bozeman* is, if not inapposite, readily distinguishable. In *Bozeman*, the Federal Circuit held that various banks were "distinct from the government for purposes of the AIA" and thus qualified as "persons" authorized to file an IPR petition under the AIA. 955 F.3d at 975-976. But the Federal Circuit's rationale for this conclusion included that "[t]he Banks do not receive congressionally appropriated funds" and "are not government-owned," which is the opposite of YMTC's relationship with the Chinese government. *Id*. Moreover, the Federal Circuit expressly noted that the "issue [being decided] is narrow," and its decision "is limited to the status of the Banks and does not prejudice other

[8] This also disposes of YMTC's argument that Micron took a "contrary" position (*see* Replies, 10) in district court. Micron took no position in the district court on any RPI issue or privity of the Chinese government.

entities whose status as 'persons' under the AIA may separately be questioned." *Id*. at 975. Thus, YMTC's reliance on *Bozeman* is misplaced.

Accordingly, because the USPS is not an authorized "person" under *Return Mail*, neither is YMTC, and the Board should deny institution.

V. PETITIONER FAILED TO IDENTIFY ALL RPIs

The Board should deny institution because YMTC chose to omit the Chinese government as an RPI.[9] And YMTC cannot now add the Chinese government without losing its original filing date.

A. YMTC Did Not Identify the Chinese Government as an RPI

Title 35 U.S.C. §312(a)(2) requires that the petition identify "all real parties in interest" ("RPIs"). If a patent owner alleges that a petitioner omitted an RPI and produces *some* evidence in support, then the petitioner bears the ultimate burden of establishing that its petition names all RPIs and showing that the patent owner is incorrect. *Worlds Inc. v. Bungie, Inc.*, 903 F.3d 1237, 1242 (Fed. Cir. 2018).

[9] While this section focuses on YMTC's failure to name the Chinese government as an RPI, YMTC also failed to name its immediate parent company, YMTC Holding, as an RPI and similar arguments apply.

According to the Federal Circuit, "[d]etermining whether a non-party is [an RPI] demands a flexible approach that takes into account both equitable and practical considerations, with an eye toward determining whether the non-party is a clear beneficiary that has a preexisting, established relationship with the petitioner." *Applications in Internet Time, LLC v. RPX Corp.*, 897 F.3d 1336, 1351 (Fed. Cir. 2018) ("*AIT*"). The Board should ask "who, from a 'practical and equitable' standpoint, will benefit from the redress" that resolution of the IPR proceeding may provide and should inquire "whether [the petitioner] can be said to be representing [the non-party's] interest after examining its relationship." *Id.* at 1349, 1353.

One "common consideration is whether the non-party … could have exercised control over [the petitioner's] participation in a proceeding." Office Patent Trial Practice Guide, 84 Fed. Reg. 64,280 at 16 (Nov. 21, 2019) ("Trial Practice Guide"). Even without exercising actual control over the petitioner's preparation of the IPR petition or participation in the IPR proceeding, a non-party may still be an RPI if it has ***an opportunity*** to control based on a formal relationship with the petitioner. *Id.* The Board may also consider whether the non-party is funding or directing the proceeding. But the exact degree of funding or control necessary to support a finding that a non-party is an RPI depends on the totality of the evidence. *Id.* Indeed, the Trial Practice Guide indicates "that a non-

party may be a real party-in-interest even in the absence of control or an opportunity to control." *Cisco Sys., Inc. v. Hewlett Packard Enter. Co.*, IPR2017-01933, Paper 9 at 12 (PTAB Mar. 16, 2018). Ultimately, "Congress intended that the term 'real party in interest' have its expansive common-law meaning." *AIT*, 897 F.3d at 1351.

Here, YMTC has failed to identify all RPIs. YMTC lists only itself and YMTI. Pet., 1-2. But that identification intentionally omits the Chinese government, which is a "clear beneficiary" of any redress that resolution of this IPR proceeding may provide and has a "preexisting, established relationship" with YMTC.

First, the Chinese government is a "clear beneficiary" because resolution of this IPR proceeding may have a direct impact on the value of, and the significant financial investments in, its "national champion"—YMTC—because Micron is asserting the challenged patent against YMTC in the related district court litigation. As explained above, the Chinese government has set ambitious initiatives and policies to become a global leader in the semiconductor industry. *See supra* §II.B-C. It also owns and controls YMTC. *Id.* And it invested tens of billions of U.S. dollars in YMTC. *Id.*

The PTAB has determined that a non-party is an RPI on far less. For example, in *Ventex Co. v. Columbia Sportswear N. Am., Inc.*, the PTAB found that

a non-party was an RPI when the parties had "mutual interest in the continuing commercial and financial success of each other" and where the non-party was the "clear beneficiary." IPR2017-00651, Paper 152 at 7-8 (PTAB Jan. 24, 2019) (Precedential). In particular, the PTAB identified two agreements between the petitioner and non-party in which the petitioner agreed to exclusively manufacture products for the non-party in exchange for an exclusivity fee. *Id*. It is hard to imagine that two agreements would show that the non-party was a "clear beneficiary," but the following would not: a non-party that has invested tens of billions of U.S. dollars in a company that it owns, controls, and promotes as a "national champion" in pursuit of its ambitious plan to become a global leader in the semiconductor industry.

In short, from a practical and equitable standpoint, the Chinese government clearly benefits from the IPR petition if any claims are found unpatentable and has a strong interest in establishing the unpatentability of the challenged patent for both its financial and political gain. *See, e.g.*, *Ventex*, Paper 152 at 7-8; *AIT*, 897 F.3d at 1355 (finding "the evidence submitted indicates … that the very challenges to validity included in the IPR petitions were challenges [the non-party] would like to have made"); *Luminex Int'l Co. v. Signify Holdings B.V.*, IPR2024-00101, Paper 10 at 37-39 (PTAB May 9, 2024) (finding non-party "will benefit from the redress that the Board might provide" because a favorable determination "would relieve

[the non-party] from liability" and has an "interest in establishing unpatentability").

Second, the Chinese government has a "preexisting, established relationship" with Petitioner. The Chinese government created, funded, owns, and controls YMTC in pursuit of its ambitious semiconductor goals. *See supra* §II.B-C. Bipartisan U.S. policymakers agree that YMTC is a state-owned enterprise. *See supra* §II.D. The U.S. Administration has confirmed that YMTC is a state-owned enterprise. *Id.* China's State Council has described YMTC as a "state-owned enterprise." *See supra* §II.C. And Chinese media outlets and Chinese universities identify YMTC as "state-owned" or "state-controlled." *Id.*

Where, like here, the facts show that a non-party has at least an ***opportunity*** to control (if not actual control), the PTAB has repeatedly held that the non-party is an RPI that the petitioner must name. For example, in *Atlanta Gas Light Co. v. Bennett Regulator Guards, Inc.*, the petitioner only listed itself as an RPI, but the PTAB found that there was a significant amount of "corporate blurring" between the petitioner and its parent company. IPR2013-00453, Paper 88 at 3-6, 11 (PTAB Jan. 6, 2015). In particular, "[r]ather than maintaining well-defined corporate boundaries," the petitioner and its parent company "are so intertwined that it is difficult for both insiders and outsiders to determine precisely where one ends and another begins." *Id.* at 11-12. The PTAB also noted that a "parent-subsidiary

relationship[] … weighs heavily in favor of finding [the non-party parent] to be a real party in interest." *Id.*; *see also Copperweld Corp. v. Indep. Tube Corp.*, 467 U.S. 752, 771-72 (1984) (explaining "in reality a parent and a wholly owned subsidiary always have a 'unity of purpose or a common design.' They share a common purpose whether or not the parent keeps a tight rein over the subsidiary; the parent may assert full control at any moment if the subsidiary fails to act in the parent's best interests.").

In short, in view of YMTC's status as a state-owned enterprise, the totality of the evidence establishes that the Chinese government has a preexisting, established relationship with YMTC and could, at any point, exercise control over YMTC's participation in this IPR proceeding—or at the very least *has an opportunity to control*. *See Zoll Lifecor Corp. v. Philips Elecs. N.A. Corp.*, IPR2013-00606, Paper 13 at 9-11 (PTAB Mar. 20, 2014) (finding non-party is an RPI when it and the petitioner "have a very close parent and wholly-owned subsidiary relationship with aligned interests and sufficient opportunity [exists] for [the non-party] to control the challenge to the patentability of the patent-at-issue"); *Aceto Agric. Chems. Corp. v. Gowan Co.*, IPR2015-01016, Paper 15 at 8-9 (PTAB Oct. 2, 2015) (finding parent is an RPI when, inter alia, it owns the petitioner and "appears to have its own vested interest in challenging" the patent); *Amazon.com, Inc. v. Appistry, Inc.*, IPR2015-00480, Paper 18 at 4-6 (PTAB July 13, 2015)

(finding non-parties are RPIs when the evidence "strongly suggests that [the non-parties] … are involved and controlling corporations representing the unified interests of themselves and [p]etitioner").

In its Replies, YMTC alleges that Micron's evidence of Chinese government ownership and control of YMTC is "unreliable and inaccurate." Replies, §I. But, in doing so, YMTC does not dispute any of the following underlying facts supporting Micron's argument. *First*, YMTC does not dispute that the Chinese government both instigated and effectuated YMTC's formation in furtherance of Chinese government priorities. *See supra* §II.C. *Second*, YMTC does not dispute that the Chinese government has invested tens of billions of dollars into YMTC. *Id.* Indeed, YMTC provided no evidence to rebut Micron's showing (including the detailed ownership structure above), notwithstanding that YMTC is in the best position to provide such information. *Third*, YMTC does not dispute that its status as China's "national champion" for memory chips, established as part of the Chinese government's "Made in China 2025" initiative, which featured a "central role for the government in directing and financing Chinese businesses." *Id.*, §II.B, D.

Rather than dispute these facts, YMTC mischaracterizes the Chinese government's role as that of a mere "passive investor." *E.g.*, Replies, 2. But, as reflected by the dearth of citation to supporting evidence, this is nothing more than

attorney argument. "Attorney argument is not evidence." *Icon Health & Fitness, Inc. v. Strava, Inc.*, 849 F.3d 1034, 1043 (Fed. Cir. 2017); *Charter Comms., Inc., v. Iarnach Techs. Ltd.*, IPR2024-01287, Paper 12 at 33 (the "contrary argument is based on mere attorney argument, which is not evidence"). Indeed, despite Board authorization to submit additional evidence with its Replies (*see* EX2050) in the separate proceedings, YMTC chose not to provide a declaration contradicting Micron's showing. *Amazon.com, Inc. v. Appistry, Inc.*, IPR2015- 00480, Paper No. 18 at 5-6 (PTAB July 13, 2015) ("Petitioner was given the opportunity to provide additional evidence to rebut Patent Owner's evidence and meet its burden, but ***Petitioner chose not to provide any such evidence. As a result, we determine, based on the record before us, Petitioner has not sufficiently***" shown that it has identified all RPIs). This failure carries consequences as YMTC bears the burden of proving that it has named all RPIs. *See Worlds Inc.*, 903 F.3d at 1242.

YMTC's Replies also attempt to reframe Micron's argument as broadly applying to every instance where a petitioner merely "ha[s] investors," which would then purportedly extend IPR estoppel to "hundreds of other companies." Replies, 7-8. This framing fundamentally distorts Micron's position. YMTC incorrectly conflates its situation (*viz*. a state-owned entity formed at the behest of the Chinese government, which provides ongoing financial support) with situations where a government (or governmental entity) merely holds a small minority

ownership stake in, or provides grant awards to, a petitioner. Basic corporate law demands recognition of the distinction between majority and minority ownership, as that distinction determines the ability to control an entity. Here, Micron showed, and YMTC failed to rebut, that the Chinese government owns YMTC. This readily disposes of YMTC's slippery slope argument that "***every investor***"—or even every "major investor"—would necessarily be an RPI. *Id.* (emphasis by YMTC).

Citing *Uniloc 2017 LLC v. Facebook Inc.*, 989 F.3d 1018, 1027-28 (Fed. Cir. 2021), YMTC contends in its Replies that "Micron never explains how the Chinese government controlled or could have controlled this proceeding, or how this petition was 'filed at another party's behest.'" Replies, 7. YMTC's reliance on *Uniloc* is misplaced. *Uniloc* addressed a totally different fact pattern involving two otherwise unrelated entities—*viz*., whether LG Electronics, Inc. was an RPI of Facebook Inc. *Uniloc*, 989 F.3d at 1025. Here, by contrast, YMTC exists only because of the Chinese government, which owns YMTC and funds it (with tens of billions of dollars) for its own purposes. The most applicable guidance from *Uniloc* lies in its emphasis that the RPI determination "demands a flexible approach." *Id.*, 1027-28. In this respect, an important consideration is who would benefit from the IPR. *See supra* §IV.B (discussing *AIT*). Notably, YMTC does

not dispute that the Chinese government would "benefit from this proceeding" if it were instituted. *See* Replies, 7.

Finally, YMTC also attempts to distract with a lengthy discussion of the U.S. government's alleged investment in Micron,[10] which is wholly irrelevant to whether the Chinese government is an RPI vis-à-vis YMTC. *See* Replies, 1, 3, 7-9. Whether or not Micron has any RPIs is simply not at issue. Regardless, unlike the Chinese government's relationship with YMTC, the U.S. government does not own Micron.

Accordingly, because the Chinese government "is a clear beneficiary that has a preexisting, established relationship with the petitioner," it is an unnamed RPI. *AIT*, 897 F.3d at 1351; *see also Worlds Inc.*, 903 F.3d at 1242, 1246.

B. YMTC Is Not Entitled to Its Original Filing Date

If a petition fails to identify all RPIs, the PTAB may permit the petitioner an opportunity to amend, but the PTAB must decide whether the petition maintains or

[10] Of the seven exhibits YMTC submitted in its Replies, four (*E.g.*, IPR2025-00098, EX1028-1030 and EX1033) relate entirely to Micron, not YMTC. The other exhibit that mentions YMTC (EX1032) simply reflects that YMTC is on the entity list.

loses its original filing date. *See, e.g.*, *Adello Biologics LLC v. Amgen Inc.*, PGR2019-00001, Paper 11 at 2-3 (PTAB Feb. 14, 2019) (Precedential) ("*Adello*"); *Proppant Express Invs. LLC v. Oren Techs., LLC*, IPR2017-01917, Paper 86 at 6-8 (PTAB Feb. 13, 2019) (Precedential) ("*Proppant*"). The PTAB considers whether there have been: (1) attempts to circumvent §315(b) or the estoppel rules, (2) bad faith by the petitioner, (3) prejudice to the patent owner caused by the delay, or (4) gamesmanship by the petitioner. *Proppant*, Paper 86 at 6-7. In general, the PTAB maintains a petition's original filing date when the petitioner quickly corrects good-faith mistakes. *See, e.g.*, *Adello*, Paper 11 at 2-5; *Proppant*, Paper 86 at 6-8.

Here, YMTC asserts in its Replies that it "is a private company with independent control over its actions." Replies, 2. This is nothing more than attorney argument and "gamesmanship" because (a) the Chinese government owns and controls YMTC, and (b) the RPI analysis is not limited to parties that actually "control" the proceedings. RPIs also include non-parties that have *an opportunity to control* the petitioner in the proceeding. Indeed, YMTC chose not to provide any evidence or declaration contradicting Micron's showing that, for example, the Chinese government has an opportunity to control Petitioner in this proceeding.

YMTC intentionally made no attempt to add the Chinese government as an RPI so that the Chinese government can file additional IPR petitions through one of its many other state-owned semiconductor enterprises (e.g., Fujian Jinhua

Integrated Circuit Co., Ltd.) if this petition is denied or unsuccessful. EX2045 (DOJ Press Release) at 1 (identifying another state-owned enterprise focusing on semiconductor technology). The Board should not permit these tactics, as YMTC's actions are precisely what the rule requiring identification of all RPIs seeks to avoid. *See* Trial Practice Guide at 12-13 ("The core functions of the "real party-in-interest" [requirement] … are to assist members of the Board in identifying potential conflicts, and to assure proper application of the statutory estoppel provisions. The latter, in turn, seeks to protect patent owners from harassment via successive petitions by the same or related parties, to prevent parties from having a 'second bite at the apple[.]'").

Moreover, the conduct against which the PTAB consistently inveighs surely includes YMTC's conduct here. For example, in *Fasteners For Retail, Inc. v. RTC Industries, Inc.*, IPR2018-00742, Paper 32 at 2 (PTAB Nov. 15, 2018), the patent owner raised in its preliminary response that the petitioner had failed to identify a non-party as an RPI. Instead of adding the non-party as an RPI, the petitioner filed a reply brief arguing that the non-party was not an RPI. *Id.* Because the PTAB rejected the petitioner's argument, it denied institution and declined to give the petitioner another opportunity to amend because doing so "would be unfair to Patent Owner and would encourage gamesmanship by allowing petitioners to refrain from naming all RPIs until if and after such unnamed RPI is the cause for

denying institution." *Id.* at 5; *Cf. Atlanta Gas Light Co. v. Bennett Regulator Guards, Inc.*, IPR2015-00826, Paper 39 at 6-7 (PTAB Dec. 6, 2016) (finding the petitioner harmed the PO through its failure to amend to identify all RPIs, in that the PO was forced to take action "to ensure that estoppel provisions would be correctly applied").

At bottom, YMTC has known all along that it is a state-owned enterprise. And any argument to the contrary fails the red-face test. *See supra* §§II.A-D. Despite this, YMTC elected not to identify the entity that owns and controls YMTC (the Chinese government), hoping to avoid the estoppel effects that doing so would incur. While to date YMTC has made no attempt to add the Chinese government as an RPI, the Board should not allow YMTC to amend without losing its original filing date, which is the natural consequence of a calculated decision to name fewer than all RPIs. In turn, because Micron served YMTC with counterclaims alleging patent infringement of the challenged patent on February 16, 2024, any new filing date would be time-barred under §315(b). *See supra* §III.

VI. TECHNOLOGY BACKGROUND

At the time of the '214 patent, "3D memory devices [were] relatively new," and thus "manufacturing these devices can pose fabrication process challenges." '214 patent, 1:20-22. As this POPR demonstrates, the prior art in the IPR grounds discloses a vastly different approach than the '214 patent's unique approach to

forming cavities directly in the word line to form the memory strings, with each string coupled to a common source, which is an improvement set forth expressly in the ’214 patent claims. *Compare* §§VII *with* VIII.

A. Kang (EX1004)

Kang describes nonvolatile memory devices that use a 3D structure built on vertical active pillars. These pillars are formed by patterning and etching a single-crystal silicon substrate to create an array of these vertical pillars. (EX1004, [0002], [0024]; Fig. 2B). The memory cells are arranged along the sides of these vertical pillars, which function as the channel regions for the cells (*id.*, [0025]).

The fabrication process begins with patterning (etching) a bulk substrate to form the semiconductive substrate and vertical pillars. (*id.*, [0002], [0024]; Fig. 2B). After the pillars are defined, a charge storage layer—such as an oxide-nitride-oxide (ONO) stack—is deposited on the exposed sidewalls of each pillar (*id.*, [0066], [0067]; Figs. 2D–2E). The process then alternates between depositing sacrificial and conductive layers around the pillars to form stacked gate electrodes (*id.*, [0068], [0069]; Figs. 2F–2H). The gates are positioned to surround the pillars, with the ONO layer sandwiched between the pillar and each gate.

The ONO charge storage layer is not formed within a cavity in a gate electrode. Instead, the ONO is deposited directly onto the sidewall of each pre-formed vertical pillar, before the gate stack even exists (it is later formed to around

the pillar) (*id.*, [0066], [0067; Figs. 2D–2E). The result is a structure where the memory cell's channel runs vertically through the pillar, with the ONO charge storage layer sitting between the pillar and each surrounding gate.

The memory array connects to peripheral circuits and bit lines through conductive plugs or direct contacts to the vertical pillars (*id.*, [0107], [0108]; Figs. 2N–2O).

The ONO layer functions as a charge storage medium. Programming, reading, and erasing operations are performed by applying voltages to the gates and bit lines, which control the movement of charge into or out of the ONO layer at specific locations (*id.*, [0044], [0045]).

B. Fukuzumi (EX1007)

Fukuzumi describes a 3D nonvolatile semiconductor memory device with vertically stacked word lines and memory cells (EX1007, [0004]-[0009], Fig. 1). The device arranges memory strings (each a series of memory cells) along vertical "columnar semiconductor layers" (CLmn), which are formed by etching the memory stack. Each pillar acts as the channel for its memory cells (*id.*, [0083], [0127], Fig. 2).

Each memory string is built on a p-well region (Ba1) within an n+ region of the semiconductor substrate (Ba) (*id.*, [0086]). The memory cells are stacked along the columnar semiconductors, and each cell is defined by the intersection of

a word line and the channel (*id.*, [0087], Fig. 4). The word lines are flat, parallel layers stacked on top of each other. Each word line wraps around the pillar, with the pillar running through the stack.

Each memory string has a source-side selection transistor at one end and a drain-side selection transistor at the other (*id.*, [0095]–[0096]). The source and drain for each memory cell are formed within the columnar semiconductor itself (*id.*, [0087]: "A source and a drain of each of the memory cells MTrmn are formed in each of the columnar semiconductors CLmn."). The source-side selection transistor layer includes a source-side hole and a source-side columnar semiconductor region, so each column has its own individually defined source (*id.*, [0096]).

Fukuzumi describes each memory string landing on a source, Ba1, of the substrate, but does not state that this source region is common to multiple memory strings (*id.*, [0086]). As detailed in §X.A, Fukuzumi suggests that each columnar semiconductor and its associated source region operate independently, rather than sharing a single, common source across multiple strings.

VII. THE ’214 PATENT

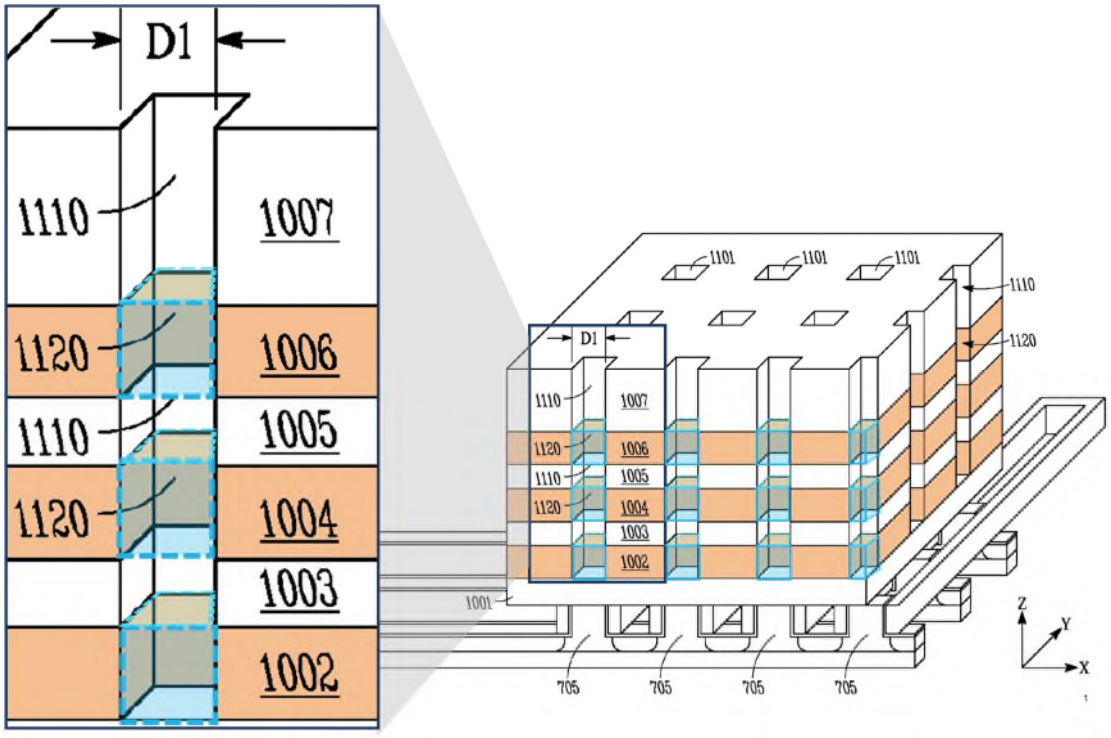
A. Overview

The ’214 patent relates to semiconductor memory devices and, in particular, to 3D non-volatile memory arrays with stacked device levels and memory elements located within the stack. *See* ’214 patent, Abstract; 1:41–44.

The patent discloses “a memory device and methods of forming the memory device” in which memory elements are formed in cavities of control gates located in distinct device levels. ’214 patent, Abstract. The invention describes a structure where each device level includes a conductive control gate with a cavity, a dielectric on the cavity sidewall, and a memory element—such as a polysilicon charge storage region—located within the cavity and electrically isolated from the control gate by the dielectric. *Id.*, 3:22–36; 7:32–8:2. A conductive channel extends vertically through the stack; the channel faces the memory elements in each device level and is electrically isolated from the memory elements by a second dielectric. *Id.*, 3:22–36; 7:66–8:10; Figs. 14–16.

The manufacturing process begins by forming a stack of alternating conductive (1002, 1004, 1006, orange) and dielectric layers (1003, 1005, 1007) on a substrate (1001). *See, e.g.*, ’214 patent, 6:25–7:18; Figs. 5–12. Holes (1101) are formed such that each hole (1101) can be aligned substantially directly over a corresponding pillar (705), as illustrated in Figure 11. Forming holes (1101)

results in forming cavities (1110) in each dielectric layer (1003, 1005, 1007) and cavities (1120, outlined in blue) in each conductive layer (1002, 1004, 1006, orange).



’214 patent, Fig. 11.

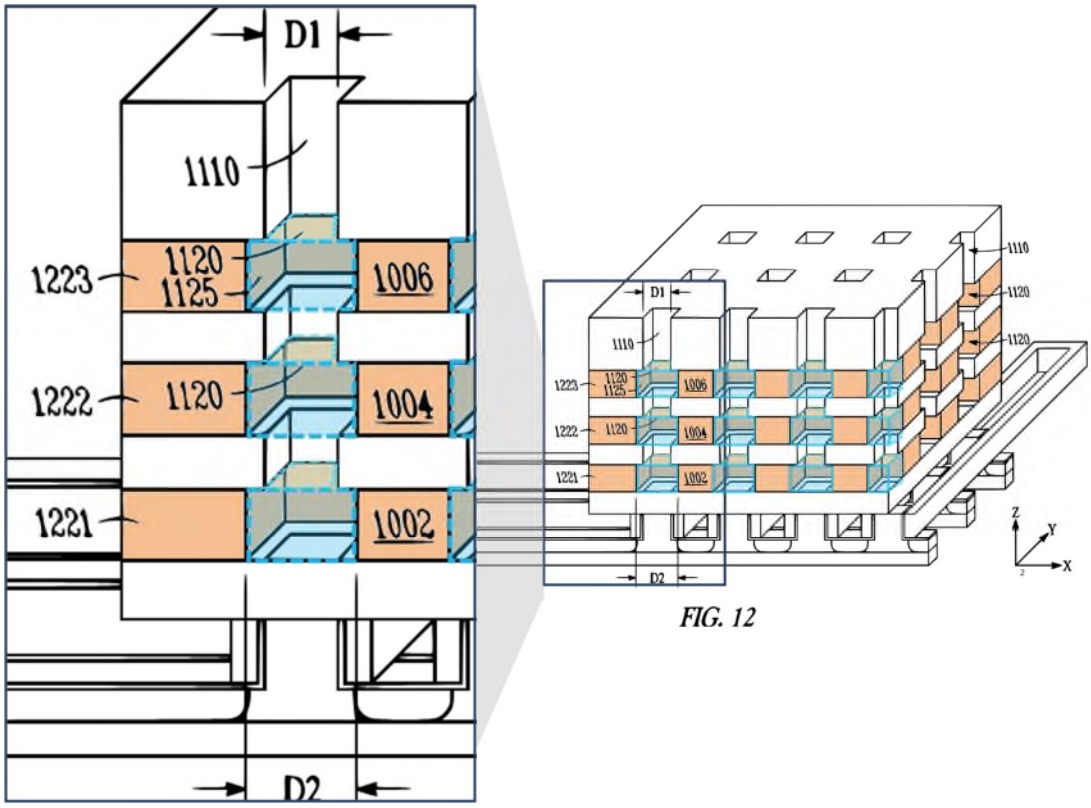


FIG. 12

’214 patent, Fig. 12.

Forming cavities (1220 (in Figure 14 below), outlined in blue) in the conductive layers (1002, 1004, 1006, orange) for the memory element can optionally include enlarging the size of cavities (1120, outlined in blue) while keeping the size of cavities (1110) in the dielectric layers substantially unchanged (e.g., remaining substantially at diameter D1). Specifically, cavities (1220 (in Figure 14 below), outlined in blue) are then etched into the conductive layers (1002, 1004, 1006, orange) at each device level. The conductive layers are used to form control gates (1221, 1222, 1223).

Memory elements (1430, red) are deposited or formed within the cavities (1220, outlined in blue), separated from the control gate by the first dielectric (1421).

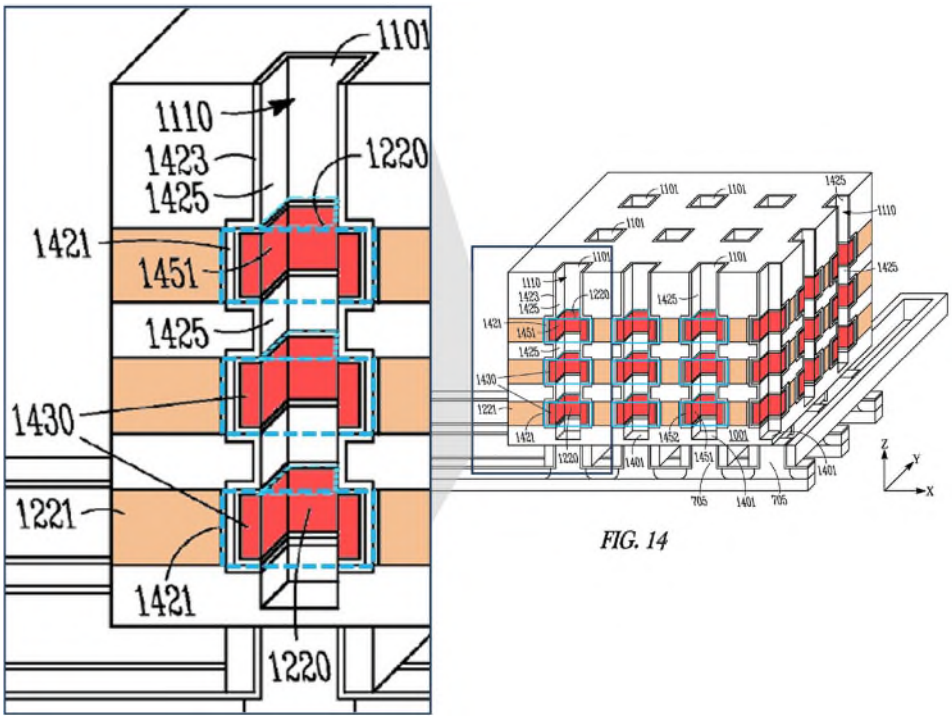


FIG. 14

’214 patent, Fig. 14.

A second dielectric is formed on the side (1451) of each memory element (1430, red), and a conductive channel (1841, pink) is created to extend vertically through the stack, facing and isolated from the memory elements (1430, red) by the second dielectric (1627). *See, e.g.*, *id.*, 6:25–7:17; Figs. 5–31.

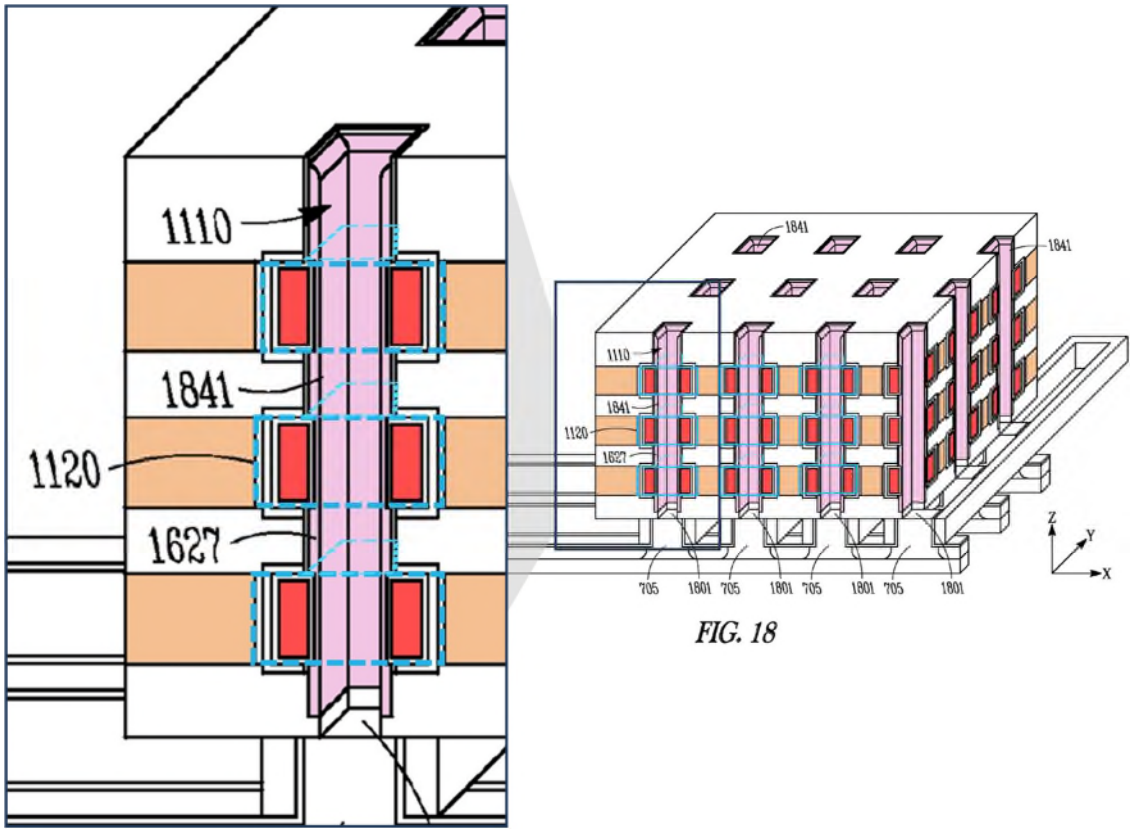


FIG. 18

’214 patent, Fig. 18.

Figures 11, 12, and 14 illustrate the formation of the stack, the etching of the cavities (1120, 1220, outlined in blue), and the formation of the memory elements (1430, red) within the cavities of the control gates.

Figure 18 shows the partially completed structure, where the vertical conductive channel (1841, pink) runs through the device, facing the memory elements (at each device level, with each memory element (1430, red) isolated from both the control gate (1221, 1222, 1223, orange) and the channel (1841, pink) by dedicated dielectric layers (1627). *Id.*, 7:17–8:10; 14:12–28.

In the device architecture, each vertical conductive channel (1841, pink) extends through the stack and terminates, at one end, at the common source (270, purple), which may be formed at the very top of the stack (or in other embodiments, at the bottom). *See*, e.g., ’214 patent, Figs. 2–4, 5, 12; 6:25–7:17; 11:19–12:11. As illustrated below, the common source (270, purple) sits above all memory cells and device levels, providing an electrical connection (a source) to every memory string in the array.

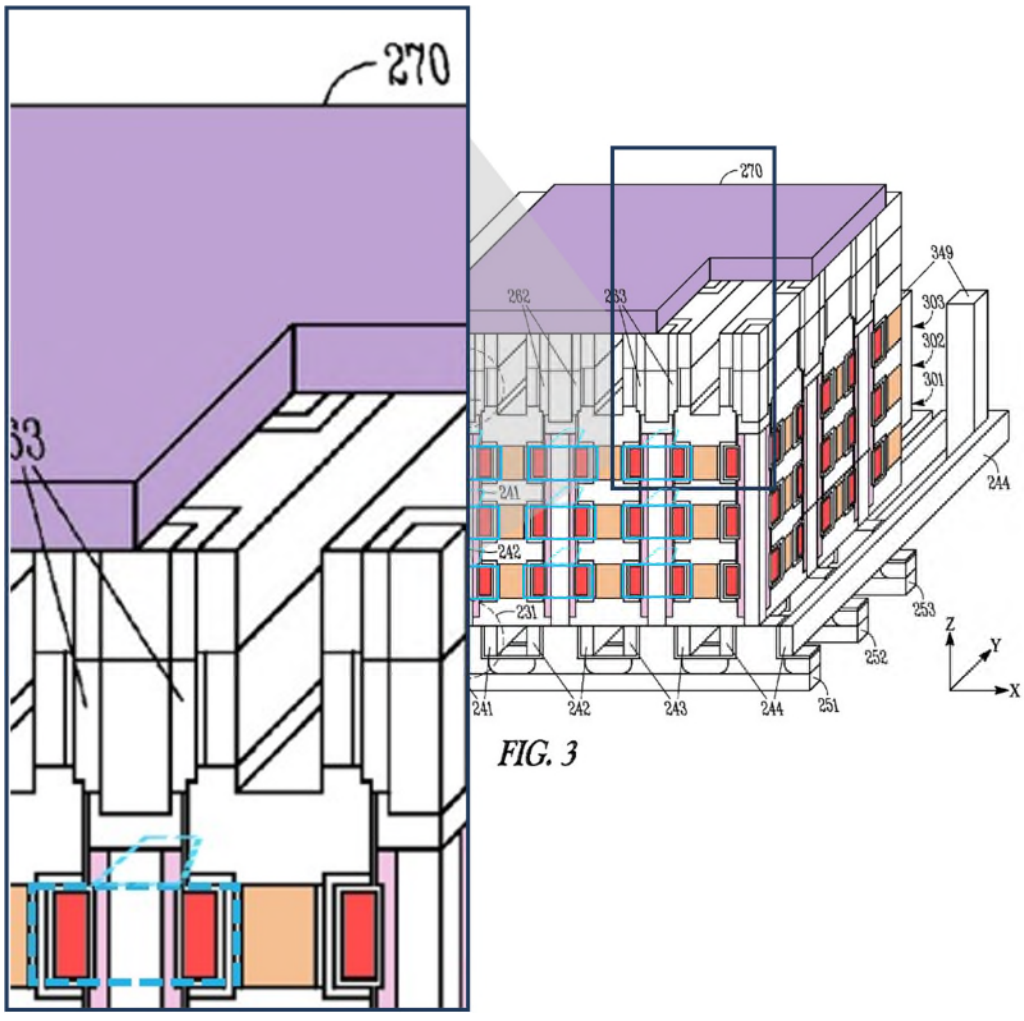


FIG. 3

’214 patent, Fig. 3.

The patent specification explains that this architecture enables each memory element to be individually addressed and electrically isolated, reducing the risk of charge leakage or cross-talk between cells. Forming memory elements in the cavities of the control gates allows for high-density stacking while maintaining robust electrical isolation and control. *Id.*, 2:27–44; 13:20–14:11.

The ’214 patent further teaches that the memory elements may comprise polysilicon (*see* claim 16), and that the arrangement of dielectric and conductive layers, memory elements, and the vertical channel supports efficient programming, reading, and erasing of memory cells. *Id.*, 3:37–45; 14:29–15:10.

In summary, the ’214 patent presents a 3D memory device architecture with stacked device levels with the option of a common source on top, each level featuring a control gate with a cavity, a dielectric, and a memory element formed within the cavity, all facing a vertically extending, electrically isolated conductive channel. The design supports high-density integration and reliable memory operation by ensuring each memory element is both physically and electrically isolated within its own cavity.

VIII. ’214 CLAIM CONSTRUCTION

Claim terms subject to IPR are construed in accordance with *Phillips v. AWH Corp*., 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc). *See* 37 C.F.R. § 42.100(b). Only terms necessary to resolve the controversy need construction.

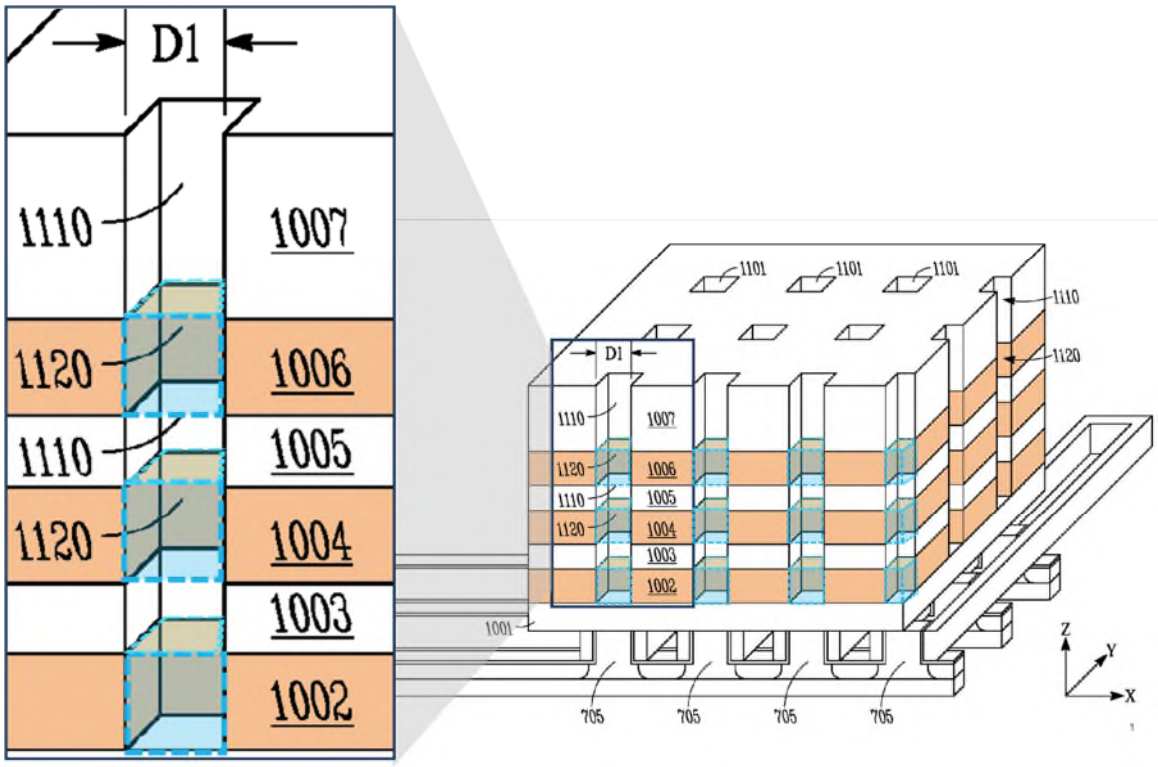
Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co. Ltd., 868 F.3d 1013, 1017 (Fed. Cir. 2017).

A. "memory element formed in a cavity of the first control gate" (Claim 1), "the first memory element located in a first device level of a memory device" (Claim 9), and "the first conductive material including a first cavity" and "a first memory element located in the first cavity" (Claim 15)

These terms should be given their plain and ordinary meaning. As detailed below, the plain claim language, consistent with the intrinsic evidence, establishes that these terms refer to a memory element that is located in a discrete, hollowed-out region formed within a conductive gate material at a given device level. Claims 1 and 15, for example, state that a "cavity" is in the "first control gate" (Claim 1) or "first conductive material (Claim 15), and that a "memory element" is within the "cavity." Similarly, Claim 9 refers to the "memory element" being "located in a first device level." In short, the "memory element" of these claims must be located within a cavity formed in the gate layer. The plain claim language does not include within its scope a "memory element" that is located next to gate layer (e.g., a gate layer that was formed after the memory element and contacts the memory element) because such a gate layer does not have a cavity in which to locate the memory element.

The specification is consistent with the plain claim language. The specification repeatedly describes the formation of cavities as openings etched into

the conductive gate layers (*see* ’214 patent, Fig. 12), with memory elements deposited or formed within these openings (*see id.*, Fig. 14) and at least partially surrounded by the gate material. *See, e.g.*, ’214 patent, 7:32–8:38 (“FIG. 14 and FIG. 15 shows memory device 500 after…memory elements 1430 have been formed ***in cavities*** 1220.”); Figs. 11, 12, 14. Indeed, the specification states that the “larger diameter” limitation in Petitioner’s proposed construction is an optional embodiment: “Forming cavities 1220 can include enlarging the size of cavities 1120 (FIG. 11) while keeping the size of cavities 1110 substantially unchanged (e.g., remaining substantially at diameter D1).” *Id.*, 7:27–38.



’214 patent, Fig. 11.

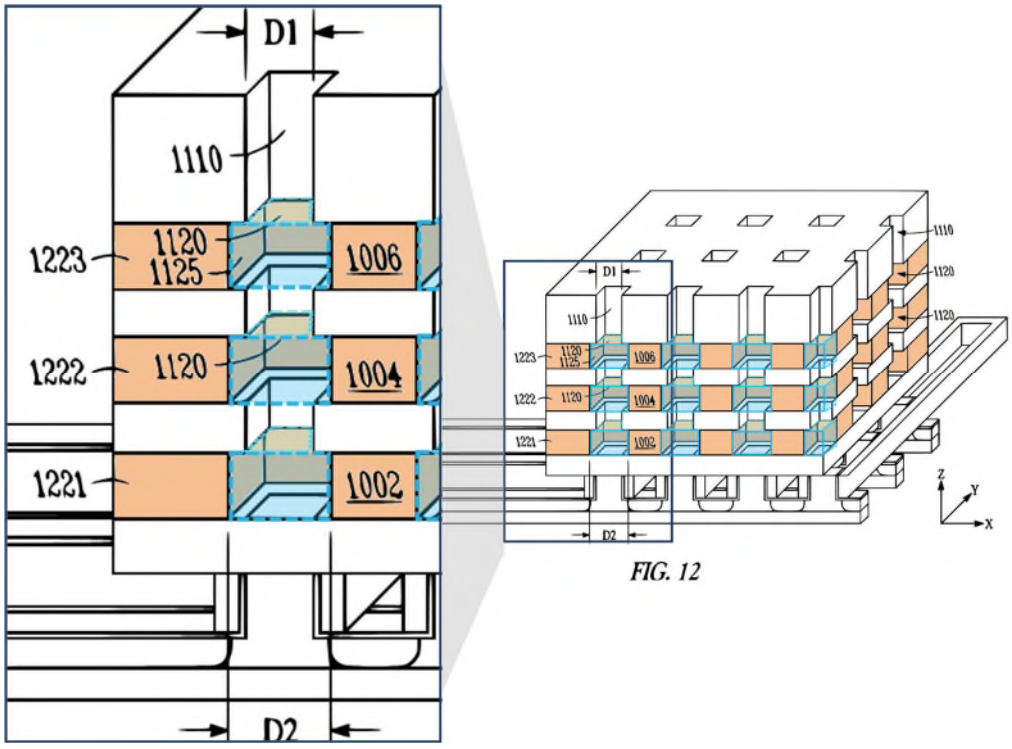


FIG. 12

’214 patent, Fig. 12.

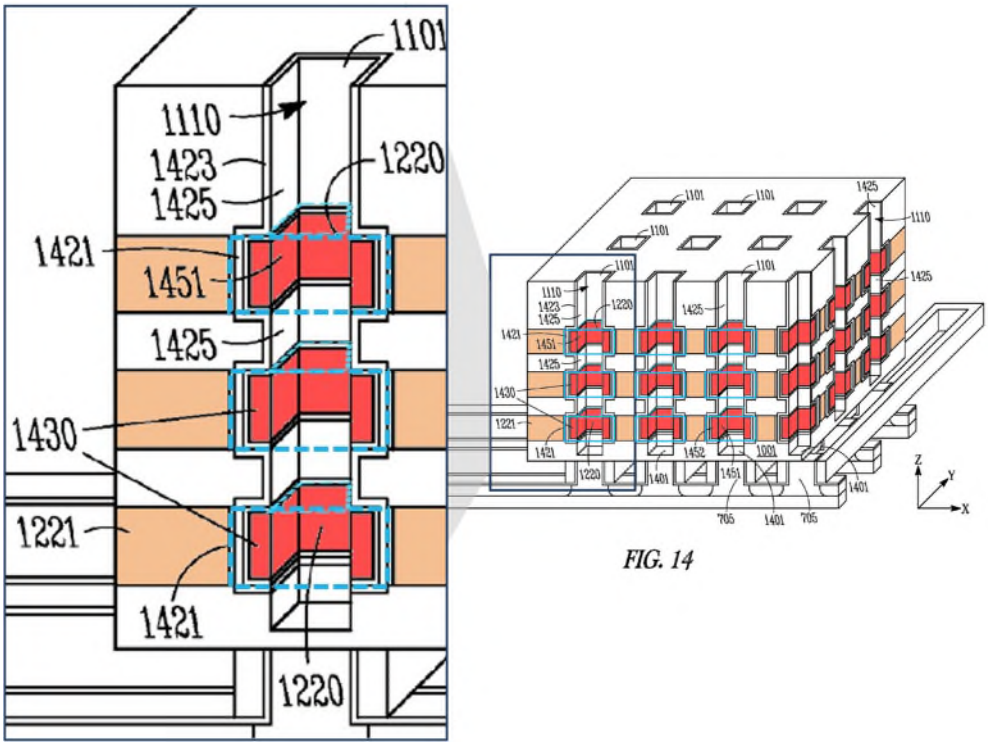


FIG. 14

’214 patent, Fig. 14.

The Board need not address Petitioner's proposed construction of "cavity" to determine whether to institute. Patent Owner's construction addresses "cavity" in the broader context of the claim language only to clarify where the "memory elements" must be located, i.e., located in an actual opening in the gate layer, which is dispositive of the Kang grounds. Patent Owner, however, notes that Petitioner's proposed construction is unduly narrow with respect to its size requirement. Petitioner proposes that "cavity" means: "a [first-fourth] hole with a larger diameter than holes in the layers immediately above and below the [first/second] control gate"). Pet., 8. This proposed construction improperly narrows the claim term by importing limitations not required by the claims or the specification. Nothing about the claim language requires that the cavity have a larger diameter than adjacent layers, nor does it restrict the cavity's shape or size to a particular comparative relationship. '214 patent, Claims 1, 8, 13, 15, 21 (no comparative size requirement); 7:26–8:34 (cavity described as an opening in the gate, not by relative diameter); Figs. 4–10, 11–16, 18–31 (no depiction of a required larger diameter). Indeed, the specification plainly states that "larger diameter" limitation in Petitioner's construction is an optional embodiment: "Forming cavities 1220 can include enlarging the size of cavities 1120 (FIG. 11) while keeping the size of cavities 1110 substantially unchanged (e.g., remaining substantially at diameter D1)." *Id.*, 7:27–38.

Nor does Petitioner cite a legal basis to rewrite the claim. The words of a claim are given their ordinary and customary meaning unless "a patentee sets out a definition and acts as his own lexicographer" or "the patentee disavows the full scope of a claim term either in the specification or during prosecution." *Thorner v. Sony Comput. Ent. Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012). Petitioner's construction violates this rule.

The Federal Circuit has cautioned against importing limitations from preferred embodiments or examples into the claims. *See Phillips*, 415 F.3d at 1323 ("[A]lthough the specification often describes very specific embodiments of the invention, we have repeatedly warned against confining the claims to those embodiments."). Here, no disclaimer or lexicography requires the "cavity" to be defined by a relative diameter or to be limited to a particular geometric relationship with adjacent layers.

IX. THE PETITION DOES NOT ESTABLISH A REASONABLE LIKELIHOOD OF SUCCESS ON GROUNDS 1-3

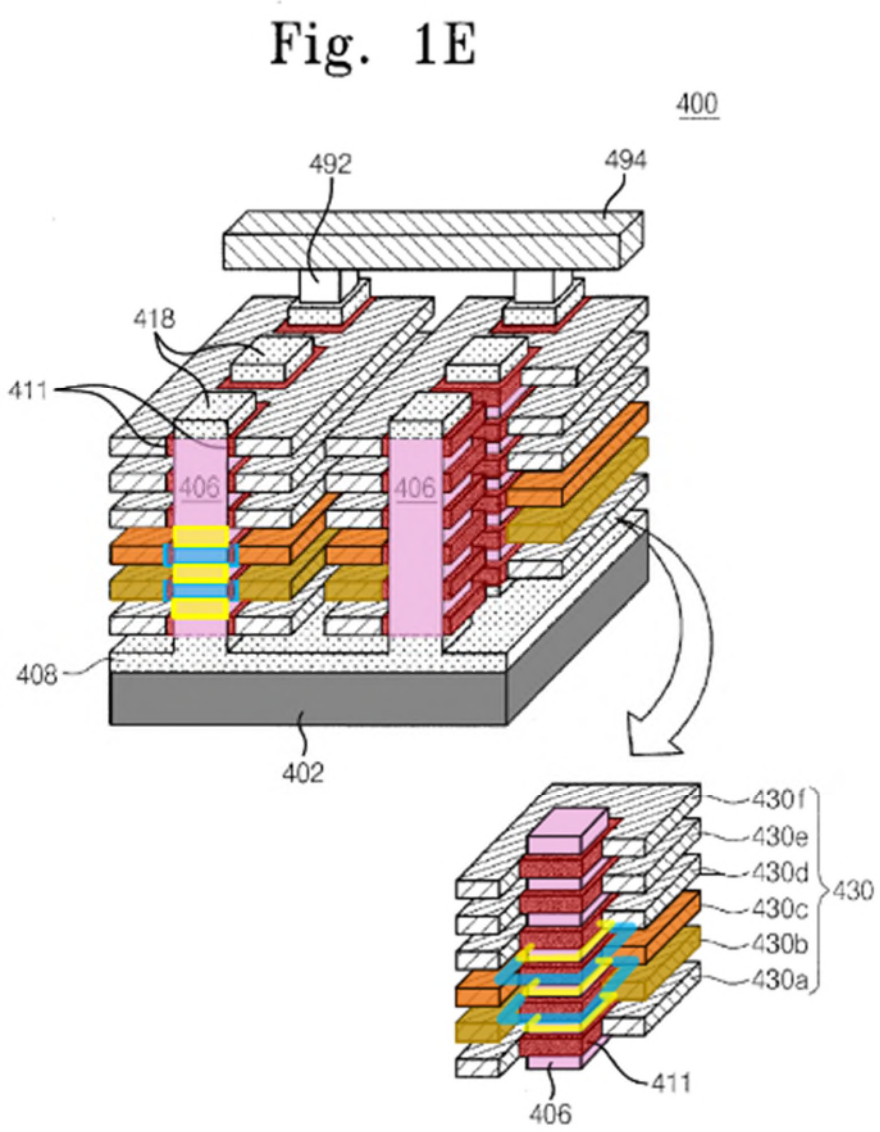
Claims 1, 9, and 15 are the only challenged independent claims in the Petition. The Petition's first three grounds all rely solely on Kang for the independent claims. Pet., 4, 9-43. As demonstrated below, Kang fails to disclose or suggest the critical requirement of the '214 patent that the memory elements are located in cavities of the gate layers. *See* §IX.

A. Kang Does Not Disclose or Suggest the Claimed "Located" Requirement (Grounds 1–3)

Sections VIII and IX detail that a critical aspect of the '214 patent—and independent claims 1, 9, and 15—is that the "memory elements" are located within cavities. Kang discloses a fundamentally different concept: forming memory pillars and then forming gate layers next to those pillars. Put another way, the "memory elements" are not located in cavities of, e.g., the gate layers, but instead, are located next to the gate layers. For this reason alone, Grounds 1-3 fail.

To start, Petitioner's allegations demonstrate that it misunderstands Kang. Petitioner states: "a POSITA would have understood that active pillar 406 and charge storage layers 411 create holes through gate group 430, respectively, in which active pillar 406 and charge storage layers 411 occupy. EX1004, [0060]-[0061]; EX1003, ¶97. Thus, Kang discloses 'a cavity of the first/second control gate' in which corresponding parts of active pillar 406 and charge storage layers 411 are positioned." Pet., 16. Petitioner alleges that Kang's "silicon nitride layer" and "charge storage layer" are the claimed "memory element" (i.e., an "ONO layer") and that these elements "are formed in two cavities (in blue) of two control gates." *Id.* Petitioner says these ONO layers (411, red) are formed in "cavities"—holes (in blue) within the gate group layers (430), specifically control gate 430b (brown) and control gate 430c (orange). Petitioner contends that a person of ordinary skill would see that the active pillar (106/406, pink) and charge storage

layers (411, red) together create these holes. In short, Petitioner claims the ONO layers are "located" in the "cavities" formed in the control gates:



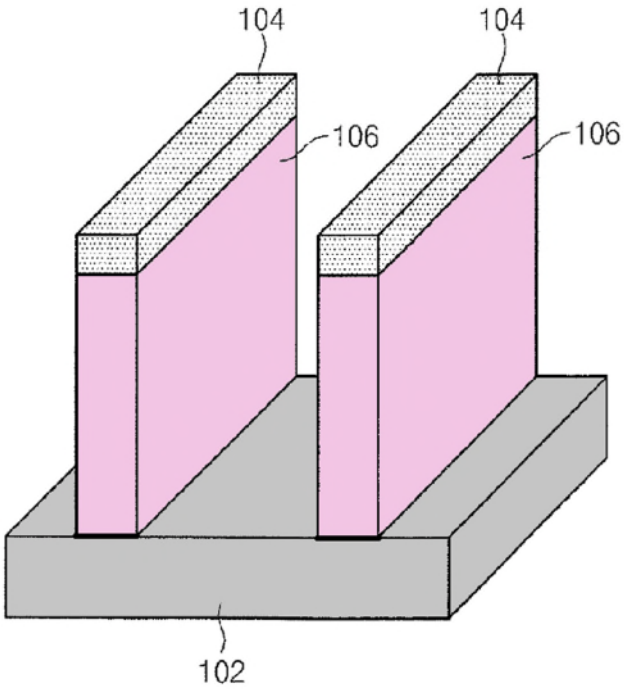
EX1003 — FIG. K

Pet., 14-16; *see also* Pet., 29–32, 35–38, 41–44.

Kang's fabrication sequence, however, does not form a cavity within the gate layers (430, 430b, brown; 430c, orange). Instead, Kang first etches the

vertical pillars (106/406, pink) from the silicon substrate, then deposits the ONO layer (411, red) on the sidewalls of the pillars. Only after these steps does Kang build up the gate stack (430) around the pillars (106/406, pink). *See* EX1004, [0063]–[0067]; Figs. 2B–2F. Specifically, Kang starts by creating the pillars (106/406, pink).

Fig. 2B

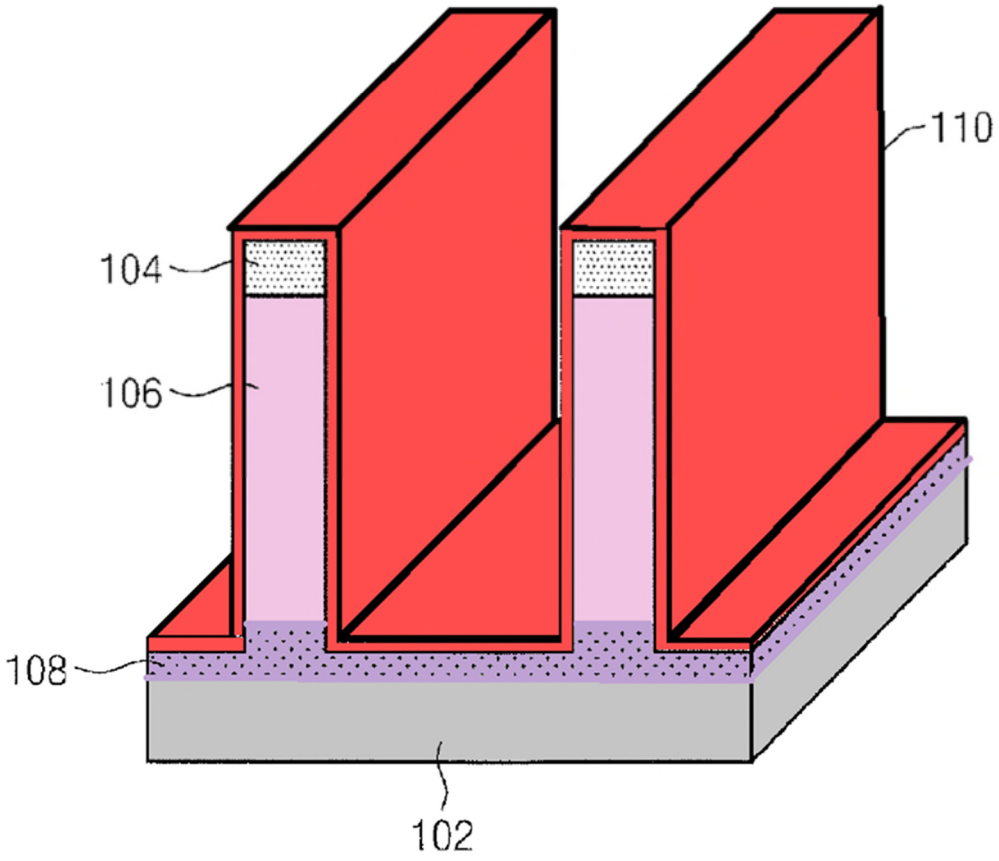


EX1004, Fig. 2B.

Then, the ONO layers (110/111[11], red) are added.

[11] The bottom portion of the ONO layer 110 contacting the substrate is removed (before forming the stack), and thus it is relabeled as 111 in Figure 2F. EX1004, [0067].

Fig. 2D

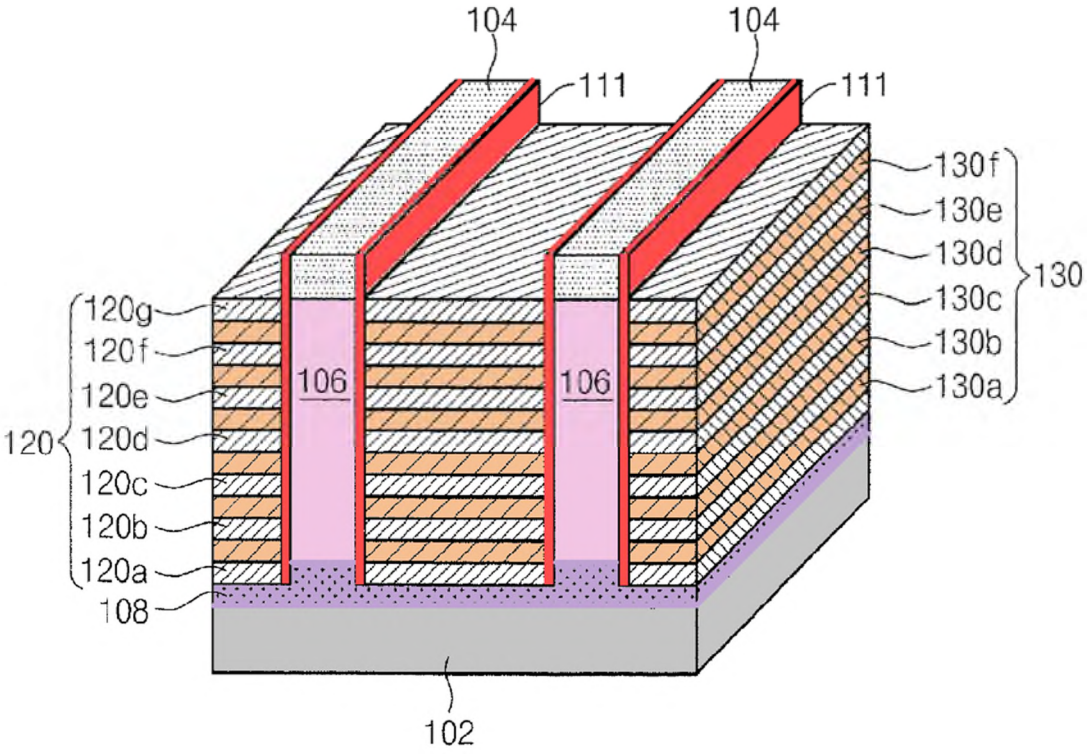


EX1004, Fig. 2D.

And finally, the alternating stack of gates (conductive layers (130a-f, orange) and sacrificial layers (120a-g) are added.[12]

[12] The sacrificial layers are replaced with insulating material, forming the final alternating stack of gate layer and dielectric layers. EX1004, [0074]-[0076].

Fig. 2F



EX1004, Fig. 2F.

In short, Kang forms the pillars (106, pink), coats them with ONO (110/111, red), and then adds the gate (130a-f, orange) and sacrificial layers (120a-g). The ONO layer (110/111, red) (the alleged "memory element") sits between the pillar (106, pink) and the gate layers (130a-f, orange). It is not formed or located in the gate layers (e.g., placed in a hollowed-out region within the gate). Rather, the gates (130a-f, orange) are formed as a shell around the pre-existing pillar and ONO coating (110/111, red). The resulting structure is a pillar with layers built up around it, not a gate with a cavity containing the ONO. *See id.*, Figs. 1A, 1E, 2F.

Petitioner's argument for Grounds 1-3 all fail because Kang's structure does not meet the claims' requirement that the memory element be located in a cavity. *See* §IX. Kang's ONO layer is continuous along the pillar's sidewall and is not formed in a discrete, gate-defined cavity. Kang simply locates the memory elements on the pillar, not in a cavity of the gate layers.

This alone disposes of Petitioner's Grounds 1-3. Grounds 1-2 rely entirely on Kang. Pet., 4, 9-42. While Ground 3 relies on the combination of Kang and Ahn, Petitioner proposes combining Kang with Ahn for claim 16 and relies on Ahn only for the material of the memory element, not for the structure of the cavity. Pet., 42–43. Thus, Petitioner's arguments also fail under Ground 3.

X. THE PETITION DOES NOT ESTABLISH A REASONABLE LIKELIHOOD OF SUCCESS ON THE MAJORITY OF CLAIMS IN GROUNDS 4-6

A. Petitioner Fails to Present Prima Facie Evidence that Fukuzumi Discloses a "Common" Source

Independent claims 1 and 9 of the '214 patent each require a "common source." *See* '214 patent, Claims 1, 9. The plain language of the claims, as well as the specification, makes clear that the source must be "common"—that is, shared among multiple memory cells. The '214 patent details this "common source": "FIG. 27 shows memory device 500 after material 2701 and ***a common source 2770*** have been formed. Forming material 2701 can include depositing a dielectric

material (e.g., silicon dioxide) over material 2101, such that the dielectric material fills trenches 2602. Then, a top portion of the dielectric material can be removed by, for example, etching back the dielectric material or by CMP. ***Forming common source 2770 can include depositing a conductive material (e.g., metal) over materials 2701 and 2101.***" *See* '214 patent, 9:56–64; 12:34–41. It, for example, "enable[s] global erase operation." *See* '214 patent, 10:35–49. An exemplary common source is shown in Figure 27:

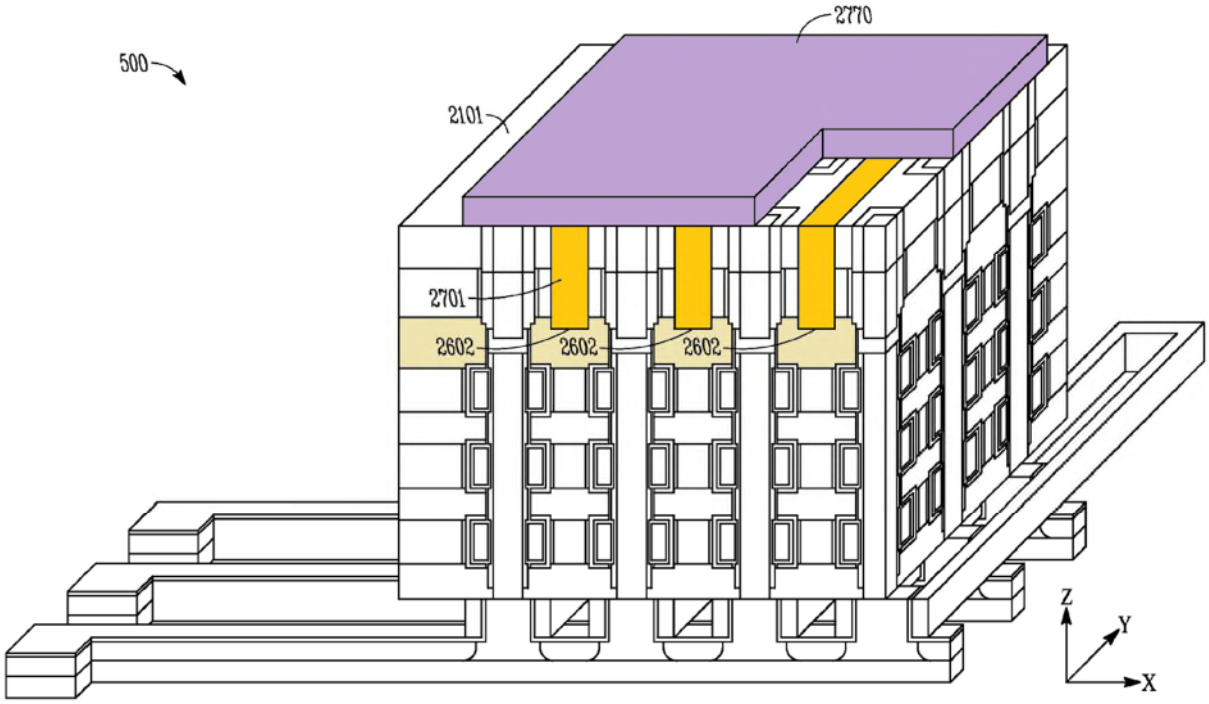


FIG. 27

'214 patent, Fig. 27.

Figure 27 shows a cross-section of the memory device after formation of the common source. Trenches (2602, beige) are etched for select line formation, and select lines are deposited. The common source (2770, purple) is formed as a

conductive layer over the dielectric (2701, gold), providing electrical connection to all vertical channels. *See* also §VIII.

Importantly, Petitioner itself was aware that 3D memory prior art may not always use a "common source." Specifically, in IPR2025-00499, Petitioner explains that Mokhlesi presents the option of either employing "source lines" or "replac[ing]" the source lines with a "common source." EX2052 (IPR2025-00499, Paper 1 (Feb. 14, 2025)), 35.

Petitioner relies on Fukuzumi for this element in Grounds 4–7, but fails to present any evidence that Fukuzumi actually discloses a "common" source as required by the claims. Pet., 4, 45-81. This is fatal to Grounds 4-7.

Petitioner's only support for this element is the assertion that "p-well region Ba1 is a 'common source' of multiple memory strings MS" because "each of the memory strings MS includes columnar semiconductors CLmn on a p-well region Ba1 formed in an n+ region of a semiconductor substrate Ba," and that "source means the n+-region formed in the p-well region Ba1 of the semiconductor substrate Ba." Pet., 54-55 (citing EX1007, [0081], [0086]). But this is not evidence that the alleged source, "Ba1," is "common"—it is only evidence that each column allegedly lands on a source. Specifically, the cited passage merely describes that each memory string is formed on a p-well region Ba1, which itself is formed in an n+ region of the substrate. There is no indication that this p-well

region, or the n+ region, is shared among multiple memory strings. To the contrary, Fukuzumi suggests that each columnar semiconductor (CLmn) has its own, separate source region at its base—consistent with Petitioner's concession of a prior art approach (the "source lines").

Before addressing Fukuzumi's specific disclosures, two aspects of Fukuzumi that Petitioner conveniently ignores are noteworthy. First, when Fukuzumi intends to describe something as "common," it does so explicitly. *See* EX1007, [0080] (describing that "each of the word lines WL1-WL4 are formed of the same conductive layer and are ***common*** in plane") The absence of such language here is telling. Second, Fukuzumi makes no reference to a global erase operation, which a common source enables. *See* '214 patent, 10:35-49.

Turning to Fukuzumi's source, Petitioner ignores the import of "a1" in "Ba1." The very paragraph that references "Ba1" makes clear that it is using the variable (a1) to indicate multiple instances of a structure. EX1007, [0081]. For example, Fukuzumi discloses "CLmn" and "m equals from 1 to 3 and n equals from 1 to 4." *Id.* It also discloses "WL1-WL4." Indeed, elsewhere Fukuzumi discloses: "As shown in FIG. 4, in the first embodiment of the memory strings MS, the columnar semiconductor CL***mn*** is formed on an n+-region formed in a p-type

region (p-Well region) B***a1*** of a semiconductor substrate B***a***."[13] *Id.*, [0086]. The plain meaning of this nomenclature is that respective columns (memory pillars) land on respective, discrete sources (e.g., Ba1, Ba2, Ba3, etc.), not a shared source. Petitioner intentionally turns a blind eye to this—which is particularly problematic given that Petitioner recognizes that the prior art discloses sources that are not common (*see supra*). Put simply, Petitioner has not met its burden for this reason alone.

Next, Fukuzumi describes individual sources and drains. For example, paragraph [0087] states: "A source and a drain of each of the memory cells MTrmn are formed in each of the columnar semiconductors CLmn." This shows that each memory string has its own source and drain.

Consistent with this, paragraph [0086] discloses connecting Fukuzumi's individual sources to individual memory strings in the substrate: "As shown in FIG. 4, in the first embodiment of the memory strings MS, the columnar semiconductor CL***mn*** is formed on an n+-region formed in a p-type region (p-Well region) B***a1*** of a semiconductor substrate B***a***." Here, "Ba" refers to a substrate,

[13] As was well known, a memory often includes multiple blocks or arrays within a single device. This use of variables allows for multiple blocks or arrays in the device, each block or array with its own substate (or doped portion of a substrate) (e.g., B1, B2, B3, etc.) and each substrate having separate sets of sources (for substrate B1: sources B11, B12, B13, etc., and for substrate B2: source B21, B22, B23, etc.).

while “Ba1” (and, by extension, Ba2, Ba3, etc.) refers to separate p-well regions—one for each memory string in that substrate. This structure connects each individual source to its own memory string, not to a shared, common source.

Fukuzumi Figures 2-4 reinforce this reading. Figures 2-3 are shown below:

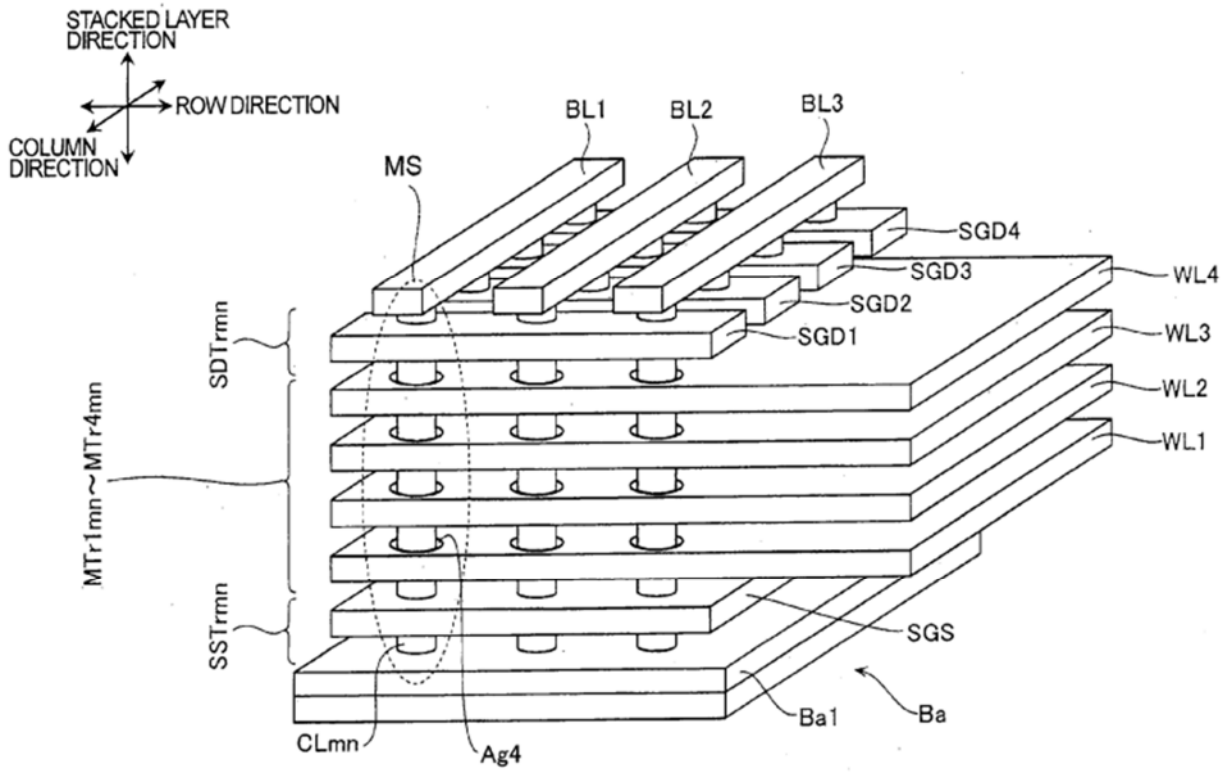


FIG. 2

EX1007, Fig. 2.

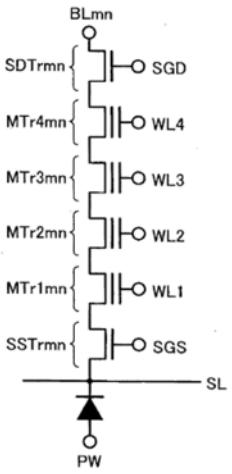


FIG. 3

EX1007, Fig. 3.

"FIG. 3 is a circuit diagram showing a memory string MS of the nonvolatile semiconductor memory device according to the first embodiment of the present invention." EX1007, [0034]. Notably, at the bottom of Figure 3, is a "source line," "SL." Recall that Petitioner itself cites to Mokhlesi, which presents the option of either employing "source lines" or "replac[ing]" the source lines with a "common source." EX2052 (IPR2025-00499, Paper 1 (Feb. 14, 2025)), 35. Thus, Fukuzumi suggests it is using the non-common source option.

Figure 2 is consistent with this interpretation. It shows "part of a perspective ***schematic view*** showing the memory cell region 12." (EX1007, [0078]). Each memory string (MS) is built on its own p-well region (Ba1) and n+ region of the substrate (Ba). Fukuzumi's use of the variable "Ba1" signals that each memory

string has a distinct p-well region—just as each columnar semiconductor (CLmn) is depicted as a separate structure. Fukuzumi's repeated use of variables ("CLmn" and "Ba1") throughout the text and figures reinforces that these are not shared, continuous regions, but individual areas assigned to each memory string. This supports the view that Fukuzumi describes separate, not common, sources for each string.

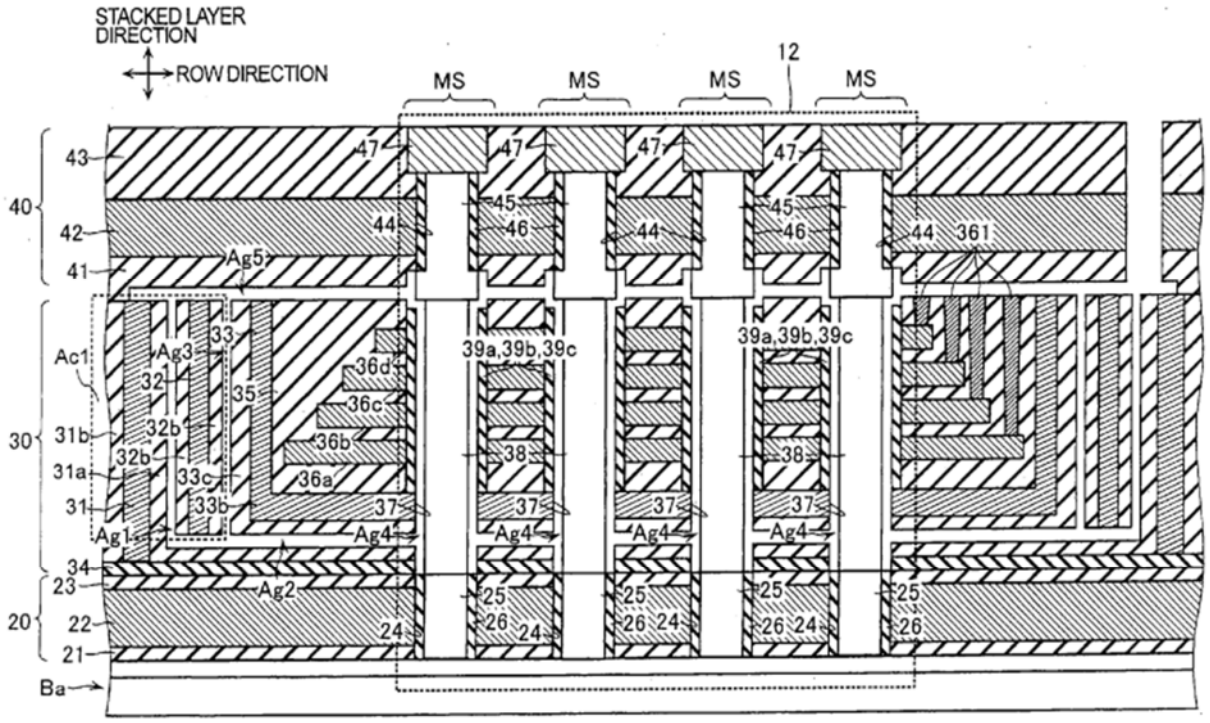


FIG. 4

EX1007, Fig. 4.

Figure 4 is "a cross-sectional schematic view showing a structure of the nonvolatile memory semiconductor device." EX1007, [0035]. The figure does not label any region as Ba1. If Ba1 were meant to be a "common" p-well region for all

memory strings, we would expect Figure 4 to show and label it as such. Instead, the description refers to "source lines," which it does not depict: "As shown in FIG. 4, in the first embodiment of the memory strings MS, the columnar semiconductor CLmn is formed on an n+-region formed in a p-type region (p-Well region) Ba1 of a semiconductor substrate Ba. Thus, source line SL is connected to a source of the source-side selection transistors SSTrmn." EX1007, [0086]. In summary, Petitioner has not presented a prima facie case that Fukuzumi discloses a "common" source as required by the claims. The Petition offers no analysis under 35 U.S.C. § 103 to bridge this gap.

XI. THE BOARD SHOULD EXERCISE ITS DISCRETION AND DENY INSTITUTION

As previously noted, Micron separately submitted discretionary denial briefing to the Director. *See* IPR2025-00498, Paper 7. Nevertheless, the Director has instructed the Board to consider discretionary denial "where the petition presents an insufficient number of challenges that meet the reasonable likelihood standard indicating that institution is an inefficient use of resources, as explained in *Chevron Oronite Co. LLC v. Infineum USA L.P.*, IPR2018-00923, Paper 9 (PTAB Nov. 7, 2018) (informative) ('*Chevron*') and *Deeper, UAB v. Vexilar, Inc.*, IPR2018-01310, Paper 7 (PTAB Jan. 24, 2019) (informative) ('*Deeper*')." FAQ No. 9, USPTO FAQs for Interim Processes for PTAB Workload Management,

available at http://www.uspto.gov/patents/ptab/faqs/interim-processes-workload-management.

In *Deeper*, the Board cited the Office's June 5, 2018 guidance that "the Board may consider the number of claims and grounds that meet the reasonable likelihood standard when deciding whether to institute *inter partes* review under 35 U.S.C. § 314(a)." *Deeper*, 42. The petitioner in *Deeper* asserted four grounds challenging 23 claims, but only showed a likelihood of prevailing on two claims and one ground. *Id*., 42-43. The Board denied institution because "instituting a trial with respect to all twenty-three claims and on all four grounds based on evidence and arguments directed to only two claims and one ground would not be an efficient use of the Board's time and resources." *Id*., 43.

Consistent with *Deeper*, the Board in *Chevron* denied institution "[e]ven when a petitioner demonstrates a reasonable likelihood of prevailing with respect to one or more claims," because "Petitioner demonstrates, at most, a reasonable likelihood of prevailing with respect to two dependent claims out of a total of twenty challenged claims. On this record, instituting a trial with respect to all twenty claims based on evidence and arguments directed to dependent claims 3 and 4 is not an efficient use of the Board's time and resources. Thus, we do not institute an *inter partes* review." *Chevron*, 10-11.

Here, YMTC has filed two separate petitions, presenting eleven grounds and challenging a total of 21 claims. In this Petition, YMTC advances seven grounds against 18 claims. Grounds 1-3, which rely on Kang to challenge eighteen claims (1-7, 9-12, and 14-20), do not warrant institution, because Kang fails to disclose that the "memory elements" are formed in cavities of the gate layers. *See* §IX. Ground 6, which relies on Fukuzumi to challenge Claim 6 (which depends upon claim 1 and requires a common source), also does not warrant institution, because Fukuzumi lacks a common source. *See* §X. Grounds 4 and 5, which also rely on Fukuzumi, challenge eleven claims (1-7 and 9-12) that all require a common source (only six do not, Claims 15-20). These Grounds, too, do not warrant institution. What's left is Ground 7—which challenges a single claim (Claim 16). This cannot warrant institution. As in *Deeper* and *Chevron*, Petitioner fails to show sufficient claims and grounds to warrant institution. Instituting trial across this many claims and grounds—when none meet the reasonable likelihood standard—would be an inefficient use of the Board's and the parties' resources. Instituting also would reward Petitioner's kitchen sink approach. The Board should deny institution, consistent with the guidance in *Deeper* and *Chevron*.

XII. CONCLUSION

Patent Owner respectfully requests that the Board deny institution.

Respectfully submitted,

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Dated: July 17, 2025,

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CERTIFICATE OF COMPLIANCE

The undersigned certifies that the foregoing PATENT OWNER'S PRELIMINARY RESPONSE complies with the type volume limitation in 37 C.F.R. §42.24(c)(1). According to the utilized word-processing system's word count, the Response—excluding the caption, table of contents, table of authorities, table of exhibits, certificate of word count, and certificate of service—contains 12,531words.

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CERTIFICATE OF SERVICE

The undersigned certifies that on July 17, 2025, a copy of the following was served in its entirety via electronic mail, upon the following attorneys of record for Petitioner:

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