EXTENDED DATA RETENTION PROCESS TECHNOLOGY FOR HIGHLY RELIABLE FLASH EEPROMs OF 10^6 TO 10^7 W/E CYCLES

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Abstract

Using 16Mbit flash memories, we clarified the relation between data retentivity and Si surface micro-defects just before the tunnel oxidation process. After 10^5 to 10^6 write/erase cycles, a small number of singular cells appear to have an anomalously large charge loss rate, when the Si surface defect density due to process damage exceeds $1.2x10^{20}/cm^3$. This anomalous charge loss phenomenon strongly depends on the electric field in the tunnel oxide, which is caused by the stored charge in the floating gate. Thus, an accelerated data retention test can be performed by means of the electric field in the tunnel oxide, by controlling the programmed Vt to be more than 2.4V just before the retention test (here, neutral Vt is adjusted to 0V). By using an accelerated test, it is clarified that controlling the number of surface micro-defects is important to obtain the extended data retention characteristics. By reducing the surface micro-defects to less than $1.2x10^{20}/cm^3$, the data retention reliability after 10^6 to 10^7 write/erase cycles can be guaranteed for conventional 2-level Flash memories, where programmed Vt is less than 2.4V.

I. Introduction

This paper studies data retention characteristics using 16M NAND EEPROM, and clarifies the influence of the process damage to data retention.

Section II describes the experimental conditions. Section III-a studies the phenomena of an anomalous cells which show a rapid charge loss after 10^6 write/erase, (W/E) cycles. Section III-b discusses the mechanism of this anomalous phenomena, and Section III-c proposes how to obtain extended data retention characteristics without anomalous cells.

II Experimental

In this study, 16Mbit NAND flash memories, a conventional simple stacked gate flash memory with 90 Å, 0.32 um^2 tunnel oxide, are used. A history of the NAND EEPROMs and studies of their reliability are reviewed in ref. 1. The voltage bias conditions during write and erase are shown in Fig. 1a and 1b. The write operation is executed by applying a programming pulse to the control gate while the source, drain and substrate are grounded and electrons are injected into the floating gate. The erase operation is executed by applying an erase pulse to the source, drain and substrate while the control gate is grounded and electrons are extracted from the floating gate[2]. A pulse wave form for W/E cycle endurance is shown in Fig. 2. For the write operation, a 22V, 3msec pulse is applied to the control gate. For the erase operation, 22V, 5msec pulse is applied to the source, drain and substrate. Those pulses are applied to all cells simultaneously. After 10^4 to 10^6 W/E cycles, the memory cells are programmed within 2.3V to 3.2V or 3.9V to 4.7V. After endurance cycles are applied, the chips are baked at room temperature or 125℃ and Vt of the cells is measured.

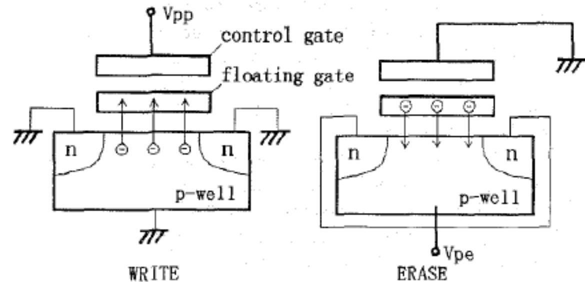

Fig. 1 Write/Erase operations of flash memory
Write pulse is applied to control gate, while drain, source and p-well are grounded. Erase pulse applied to drain, source and p-well, while control gate is grounded.

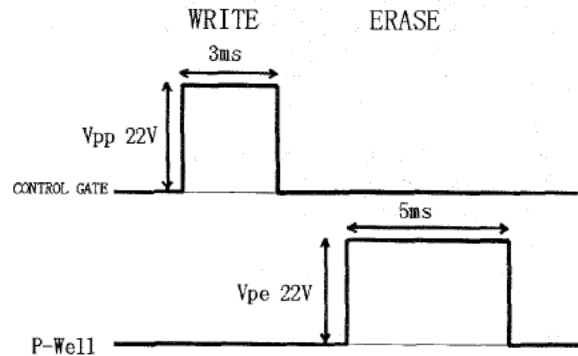

Fig. 2 Pulse wave form for W/E endurance.
Pulse is applied to all cells simultaneously.

III Results and Discussion

a) Anomalous leakage current

Figures 3-a and 3-b show the results of a 1000hr bake at room temperature after 10^5 and 10^6 W/E cycles. The initial Vt before baking in Fig.3-a exceeds 3.9V, and that in Fig. 3-b, 2.4V. As shown in Fig. 3-a, singular cells whose charge loss rates are very large appear; we call them tail bits. The number of tail bits in Fig. 3-b is much

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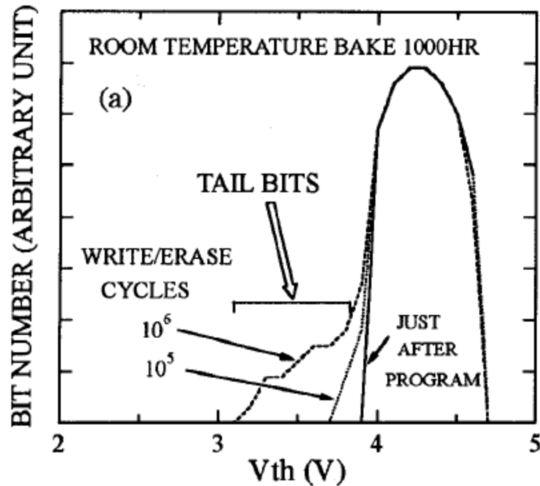

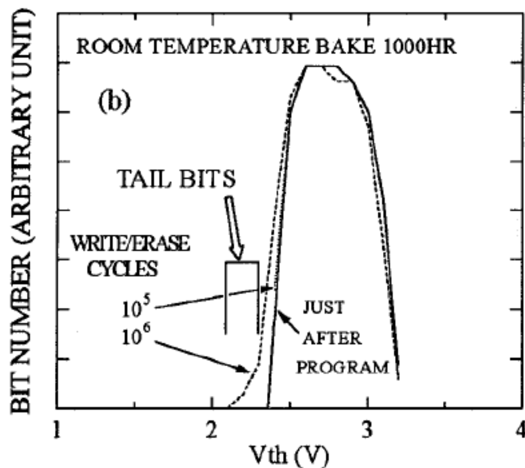

Fig. 3 Vt distrubution

Solid line indicates Vt just after programming. Dotted line and dashed line are Vt distributions after 1000hr bake. In programming, Vt is controlled to be more than 4.0V and 2.5V in (a), (b).

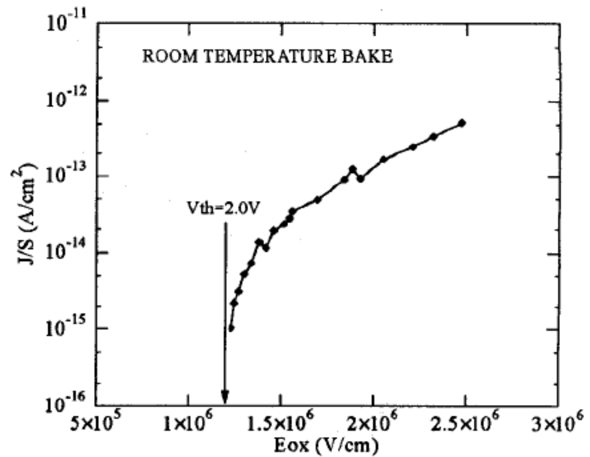

Fig. 4 Charge loss rate of a typical tail bit as a function of electric field.

Eox is the electric field inside tunnel oxide.

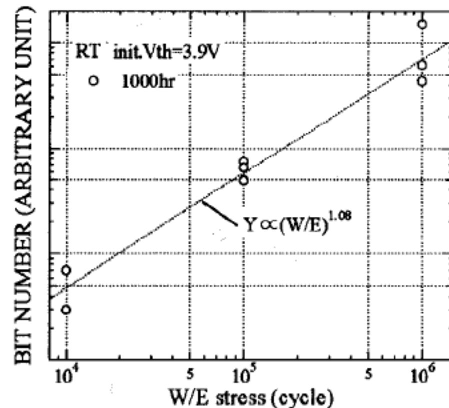

Fig. 5 W/E cycle dependence of tail bits

The initial Vt before baking exceeds 3.9V. Tail bits are defined as the cells whose Vt become less than 3.7V during baking.

smaller than in Fig. 3-a. This means that the tail bit generation rate depends largely on the electric field due to thefloating gate stored charge. The electric field dependence of charge loss rate is more clearly shown in Fig. 4, which shows the charge loss rate of a singular cell as a function of electric field in the tunnel oxide (Eox). J/S is leak current density. J is calculated by

$$J = C_{CG-FG} \cdot \Delta Vt/\Delta t$$

where C_{CG-FG} is the capacitance between a control gate and a floating gate.

The charge loss rate, when Eox is less than 1.2MV/cm, is very small. However, it rises sharply near Eox=1.4MV/cm, and increases exponentially with increasing Eox. The mechanism of this phenomena is not well known now. The tail bit generation rate also increases as the endurance cycles increases, as shown in Fig. 5. The number of tail bits increases in proportion to the endurance cycles.

b) Mechanism of the anomalous leakage

Tail bits reappear after reprogramming and one more retention bake as shown in Fig. 6. Tail bits behavior is split mainly into two groups. One group is transformed into normal cells during reprogramming and exhibits as high reliability as normal cells. The other is transformed into anomalous cells, which show almost the same charge loss characteristics in two measurements. After one more W/E operation, about 10% of the tail bits are transformed into normal cells. This fact indicates that cells which exhibit anomalous leakage have two states. In one state, a leakage current flows, in the other state, the mechanism of the leakage current vanishes or is inactive. Tail bits are then easily transformed from one into the other. In Fig. 6, an exceptional cell named "stop bit" here is identified, it does not belong to either group. By tracking the stop bits individually, we found that

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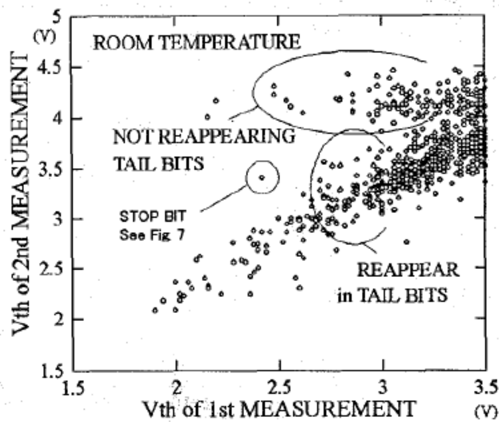

Fig. 6 Reappearence of the anomalous cells when retention characteristics are measured again.

After 10^6 write/erase cycles, chips were baked for 2500hr at room temperature. After that, all cells are erased, programmed and baked for 2000hr again.

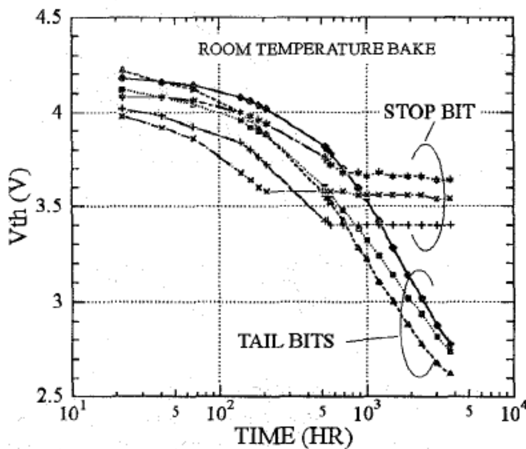

Fig. 7 Charge loss characteristics of the anomalous cells.

There are three bits whose rapid charge loss are suddenly and randomly stopped .

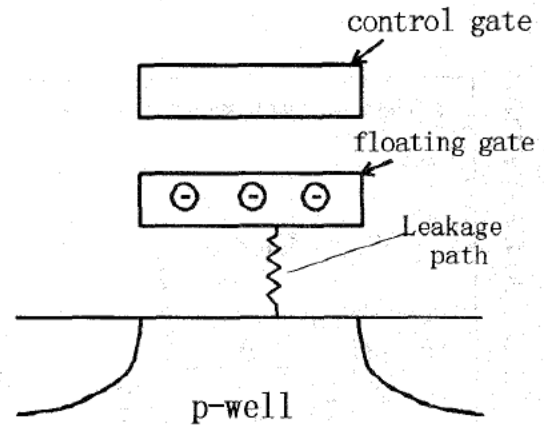

Fig. 8 Schemetic model of a leakage path

A leakage path is in a small area of the tunnel oxide. Charge stored in the floating gate passes throught the leakage path to the p-well.

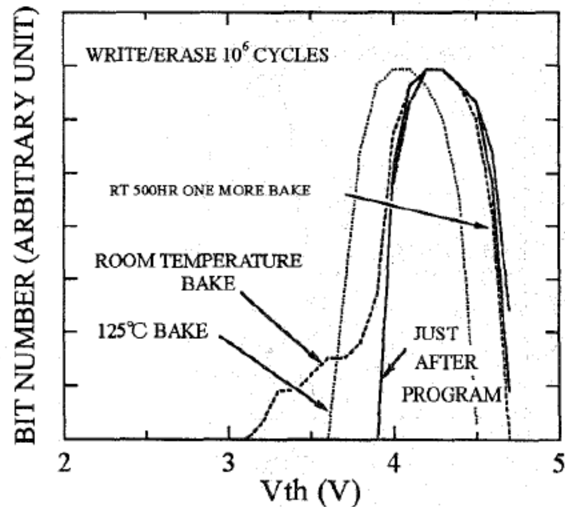

Fig. 9 Vt distribution after 25℃ and 125℃ baking.

Baking time is 1000hr. After 125℃ baking, Vt of all cells shifts about 0.3V.

the stop bits are suddenly transformed to normal cells during retention baking at room temperature, as shown in Fig. 7. Existence of the stop bits strongly supports the easy transformation between the two states.

These facts indicate that the anomalous leakage current of the tail bits flows only through one or a few spots, indicated as "leakage path" in Fig. 8. This leakage path can be easily inactivated or activated. A schematic model of the leakage path is shown in Fig. 8, where electrons can easily flow from the floating gate to the substrate through the leakage path. Leakage paths are generated with a constant probability per W/E cycles, as shown in Fig. 5. Vt will deviate due to detrapping of the charge in the oxide. However, in this model, Vt deviation due to detrapping of the trapped charges in the tunnel oxide does not play an important role for the following reason. Oxide charge trapping will occur over the whole channel area. Detrapping will also occur over the whole channel area, not just a few spots. Thus, the transformation between normal and anomalous cells can not be explained by the oxide charge detrapping model.

After 1000hr baking at 125℃, no tail bits can be observed. However, Vt of all cells shifts about 0.3V, as shown in Fig. 9. After 125℃ baking, 100hr baking at room temperature is performed. However, the Vt distribution, as shown in Fig. 9, is completely unchanged. Reprogramming and a room temperature baking are then done. No tail bits appear after 500hr room temperature baking. (In Fig. 9, the Vt distribution at RT 500hr baking almost overlaps with the distribution just after programming.) The Vt shift strongly depends on the initial Vt, as shown in Fig. 10. However, the tail bits disappear after

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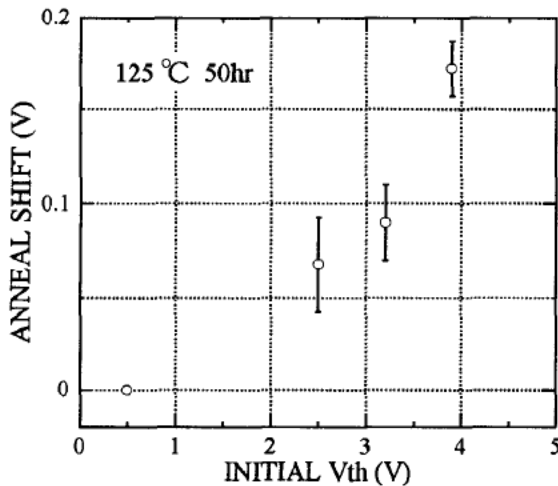

Fig. 10 Electric field dependence of anneal shift
Initial Vt is Vt just after programming. The chip is then baked 50hr at 125℃.

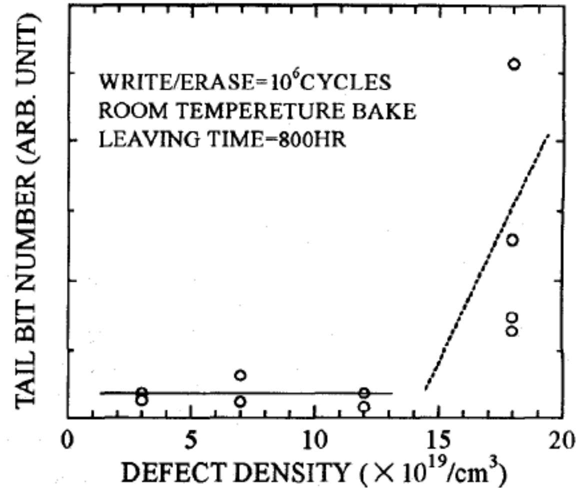

Fig. 11 Dependence of tail bit number on Si defect density
Small circles show experimental data. Initial Vt is more than 3.9V. Si defect density is obtained from process damage simulation.

125℃ baking independent of the initial Vt. This means that thermal energy (35meV) can inactivate or eliminate the leakage path. We obtain the same results after 24hr baking at 125℃. However, the tail bits don't disappear completely after 4hr baking.

c) Reduction of anomalous leakage current

The influence of the process damage on the tail bits is investigated, because process damage of the Si substrate may induce weak points in the tunnel oxide. For instance, when the oxidation temperature is not high enough, surface micro-defects may be built in the tunnel oxide. These defects may be related to the tail bits. As a result, the tail bit generation rate can be reduced by decreasing the Si surface micro-defects just before the tunnel oxidation process. In this experiment, the micro-defect density is intentionally controlled by adjusting the fabrication process, and the defect density is simulated by using a process damage simulator. As shown in Figures 11 and 12, the tail bit generation rate is drastically decreased when the Si surface defect density is less than $1.2\text{x}10^{20}/\text{cm}^3$. As shown in Fig. 11, the tail bit generation rate does not increase linearly, possibly because when the Si surface micro-defect density is less than $1.2\text{x}10^{20}/\text{cm}^3$, the oxidation process or some other thermal processes may anneal out the defect points in the Si surface. Thus, the Si defect density has a threshold of the tail bit generation, as shown in Fig. 11 and 12.

The effect of surface micro-defects on gate oxide reliability is clearly shown by measuring data retention characteristics. For actual NAND Flash memory, erased Vt is less than 0V, and programmed Vt is 0.6 to 1.6V. Thus, even if the micro-defect density exceeds $1.8\text{x}10^{20}/\text{cm}^3$, reliability after 10^6 W/E can be guaranteed. However, the micro-defect density must be controlled to less than $1.2\text{x}10^{20}/\text{cm}^3$ when reliability after 10^6 to 10^7 W/E is needed.

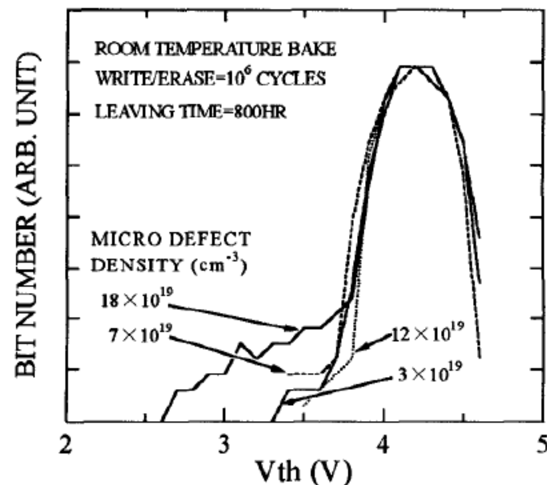

Fig. 12 Relation between tail bits and Si surface micro-defect density.

IV Conclusion

With experiments using 16Mbit flash memories, the relation between data retentivity and Si surface micro-defects has been clarified for the first time. The generation rate of singular cells with an anomalous charge loss rate can be reduced by decreasing the Si surface micro-defects just before the tunnel oxidation process. The Si surface micro-defects, derived from impurity implantation or RIE damage or stress, tend to increase with the scaling of the cell size. Therefore, this clear correlation provides a useful guideline for fabricating less than sub-half micron, highly reliable flash EEPROMs. It is also useful for multi level flash EEPROMs, because multi level flash memory is exposed to a large self-induced electric field in the tunnel oxide during baking[3].

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Acknowledgments

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