Silicon-Rich-Oxides as an Alternative Charge-Trapping Medium in Fowler-Nordheim and Hot Carrier Type Non-Volatile-Memory Cells

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Abstract

We present a study on memory cells consisting of a standard MOSFET with a Silicon-Rich-Oxide (SRO) charge-trapping layer incorporated in the gate-dielectric stack. The impact of excess-Silicon concentration and tunnel-oxide thickness on basic cell characteristics of both Fowler-Nordheim and hot-carrier type of devices is investigated. We employ a new technique for high-speed determination of the threshold voltage, demonstrate the possibility of 2-bit storage and analyze the Vt-fluctuations in matched transistor pairs.

Introduction

Memory devices based on localized charge-trapping recently experienced renewed interest because of their good scalability, low-cost process integration, high density and low voltage operation [2,3,4]. Obviously, the device characteristics critically depend on the properties of the charge-trapping medium. In the past, Si_3N_4 has been used almost exclusively for this purpose. The goal of this study is to investigate the possibility of using Silicon-Rich-Oxide (SRO) as an alternative charge-trapping medium [1].

Device fabrication

Memory cells have been fabricated using a standard nMOS 0.18μm process-flow with a modified gate-dielectric. No additional thermal cycling has been added to the flow. The gate-stack of the cells consists of a thermally grown bottom-oxide of 2, 2.5 and 5nm thickness respectively, a 6.5nm deposited SRO-layer using PECVD of SiH_4 and N_2O and a 5nm deposited High-Temperature top-oxide (HTO). Three SRO-layers with different amounts of excess-Silicon have been implemented by adjusting the gas-flow ratio. Characterization of the films by X-ray Photo-electron Spectroscopy (XPS) revealed the presence of ca. 20, 17 and 10 atomic% of excess-Silicon respectively, as well as ca. 10 atomic% of Nitrogen in all films. A cross-section of the device and a summary of the process splits are shown in fig. 1.

The TEM picture shown in fig. 2 reveals a fairly low density of nano-crystals, having sizes of 1nm and less. Since Silicon clusters can occur in the amorphous state and because of their small size, a considerable fraction of clusters might go undetected by TEM.

Memory action is apparent from conventional Id-Vg curves measured on a minimum size transistor (fig. 3). Functional cells with a physical gate-length of ca. 110nm have been observed, but suffer from punch-through (not shown). In the remainder of this text, the drawn gate length is indicated. A line-width loss of ca. 40nm has been measured by top-view SEM after gate-etch.

Electrical characterization

Similar to SONOS memory cells, the Fowler-Nordheim-type (FN) SRO-cells require a thin tunnel-oxide in order to achieve acceptable Program/Erase (P/E) times. As a consequence, a fast initial charge-loss after programming or erasing can be present in some cases. A correct measurement of the P/E-transients therefore requires reading of the threshold voltage immediately after programming or erasing. In the past, dedicated test-equipment has been developed for characterization of SONOS cells [3]. Our set-up employs off-the-shelf equipment only, as can be seen in fig. 4. The memory cell is used in a basic inverting amplifier stage. When sweeping the input-voltage Vgate of the invertor and recording it's output Vout, the threshold voltage Vt of the cell can be measured by determining Vgate at which the output switches (fig. 5). Measurements on a non-programming reference transistor show the set-up is capable of tracking input signals with slew-rates up till 1MV/s (fig. 5). Using this technique, the Vt is measured on the falling edge of a trapezoidal P/E pulse, effectively minimizing the read-delay. Note that extraction of the Id-Vg curve is straightforward, offering an elegant method for high-speed characterization of MOSFETs.

The P/E transients of a SRO3 cell with 2.5nm tunnel oxide and Lg=0.18μm is shown in fig. 6. The cell can be programmed/erased with ±8V/100ms gate pulses. Figures 8 and 9 compare the transients of different samples at $V_{P/E}$=±8V. Increasing excess-Silicon content or decreasing tunnel-oxide thickness improves P/E times by 0.5 to 1.5 orders of magnitude. For all samples, the as-programmed Vt after erasing is seen to increase again for higher erase-voltages (fig. 7). A similar, but smaller effect is present for programming. We believe this is due to injection of charge from –or de-trapping to– the gate-electrode. Seemingly a drawback, this effect could be used advantageously as a protection to over-erase. The retention characteristics shown

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in fig. 10 reveal a strong effect of both excess-Silicon content and tunnel-oxide thickness. Only the SRO3/2.5nm sample yields a 1V Vt-window extrapolated at 10 years. Cycling and high-temperature bakes are expected to further worsen the retention. Excellent endurance is obtained for all samples using ±8V $V_{P/E}$ (fig. 11).

Hot carrier programming/erasing allows for faster operation. Also, retention is improved because thicker bottom-oxides can be used. Figures 12 and 13 show the transients for channel hot-electron programming and band-to-band tunneling induced hot-hole erasing. Programming to Vt=4V can be achieved in 20μs using Vg=9V and Vd=4V. Erasing is considerably slower, partly because the device was not optimized. Storage of two bits in a single cell, as discussed in [2], is demonstrated in fig. 15. The difference in Vt between forward and reverse read (swapping role of source and drain) is monitored during programming. The attainable Vt-window is depending both on the drain read-voltage and program pulse-time. Samples containing a higher excess-Silicon concentration show a smaller nominal Vt shift (fig. 14) as well as smaller Vt-windows (fig. 16). We believe these effects are caused by charge moving laterally within the SRO-film.

Across-wafer Vt-tolerance and intrinsic Vt-fluctuation calculated from matched transistor pairs $(Vt-Vt')/\sqrt{2}$ is analyzed in figures 17 and 18. Cumulative probability distributions after programming and erasing are shown in fig. 17 (SRO3, 2.5nm bottom oxide, minimum size transistors). A comparison of the distribution's standard deviation σ is presented in fig. 18. The devices exhibit a moderate two-fold increase in matching with respect to a non-programming reference device.

Conclusion

The use of Silicon-Rich-Oxides in memory devices employing either Fowler-Nordheim or hot-carrier program-erase mechanisms can result in basic cell characteristics comparable to those reported for Si_3N_4 based devices [2,4]. Since excess-Silicon concentration has a strong impact on cell-performance, further exploration of the SiO_x design space might lead to further improvements.

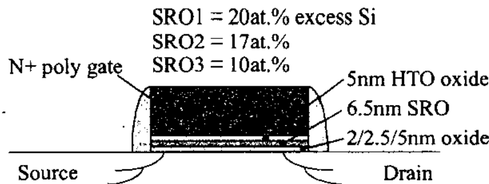

Fig. 1: Cross-section of the memory cell, indicating process splits.

Acknowledgments

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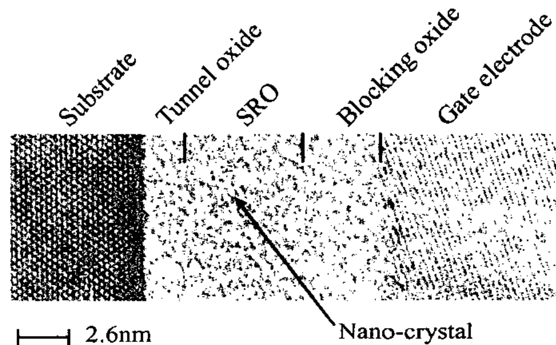

Fig. 2: TEM picture of the gate stack with SRO3. Similar results are obtained for SRO1 and 2.

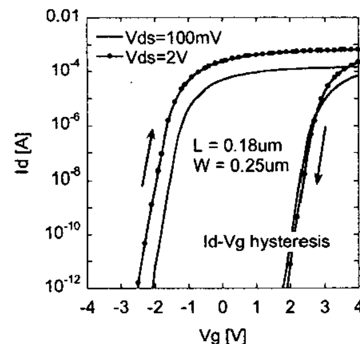

Fig. 3: Low-speed Id-Vg, scanning from −8V to +8V and back. Measured on SRO3 sample with 2.5nm tunnel oxide.

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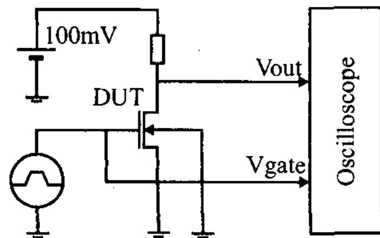

Fig. 4: Schematic of the measurement set-up for high-speed determination of Vt, based on a basic invertor circuit.

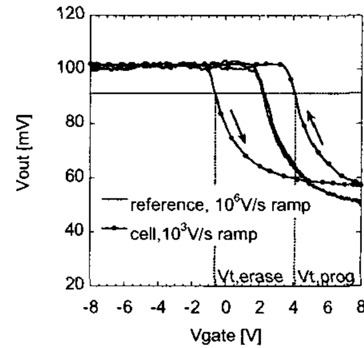

Fig. 5: Invertor Vout as a function of Vgate, measured on non-programming reference transistor and memory cell. Vt is determined at Vout = 90mV.

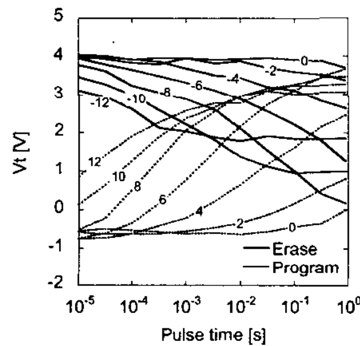

Fig. 6: Program and erase transients for SRO3 cell with 2.5nm tunnel oxide and L/W=0.18/10μm. Fowler-Nordheim tunneling used for both program and erase, voltages ranging till ±12V.

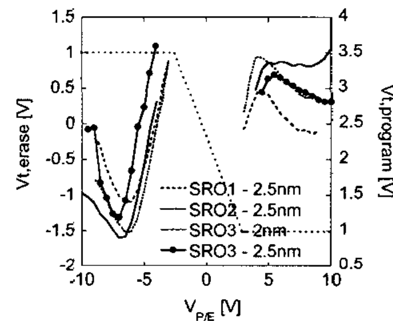

Fig. 7: Vt versus program/erase voltage measured immediately after a 10ms F-N programming/erasing pulse. Note the offset between left and right y-axis.

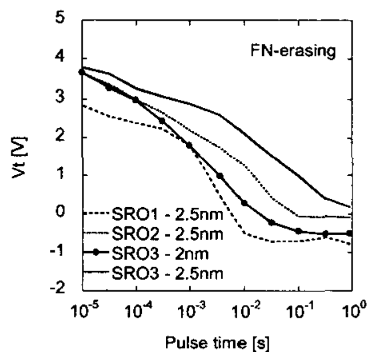

Fig. 8: Comparison of the F-N erase transient characteristic of different samples. Erase voltage is -8V.

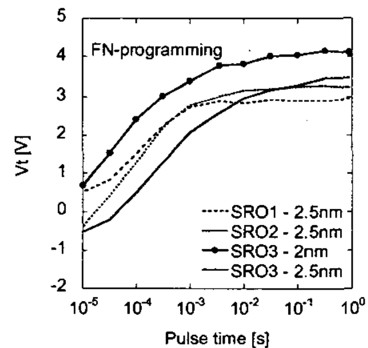

Fig. 9: Comparison of the F-N program transient characteristic of different samples. Program voltage is +8V.

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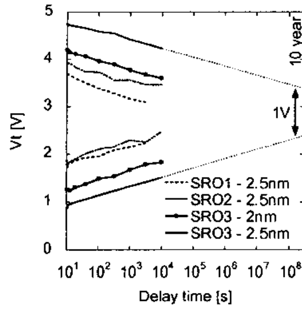

Fig. 10: Comparison of the Vt retention of different samples. A 1V window remains after 10 years for SRO3/2.5nm.

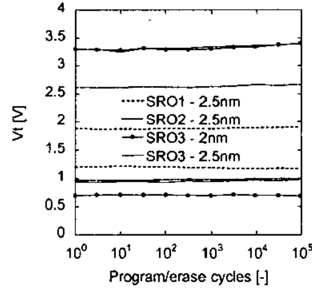

Fig. 11: Comparison of the F-N endurance characteristics of different samples. Program/erase voltage of ±8V (except SRO1 program at +6V). Pulse times depending on sample.

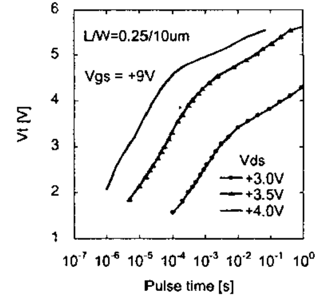

Fig. 12: Program transients for SRO3 with 5nm bottom oxide. Channel hot-electron programming used with 9V on gate and 3, 3.5 and 4V on drain.

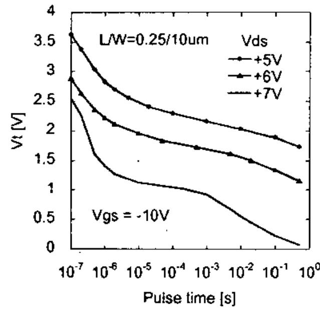

Fig. 13: Erase transients for SRO3 with 5nm bottom oxide. Band-to-band tunneling induced hot-hole injection used for erasing with −10V on gate and 5, 6 and 7V on drain.

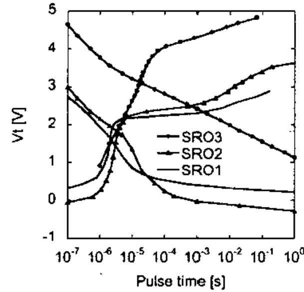

Fig. 14: Comparison of the hot-carrier program/erase transients of different samples. Erasing with Vg=-10V and Vd=6V, programming with Vg=9V and Vd=4V.

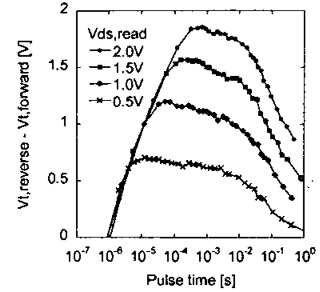

Fig. 15: Difference in forward- and reverse read as function of program pulse time (Vg=9V, Vd=4V), demonstrating 2-bit storage. Drain voltage during reading ranging from 0.5 till 2V. Measured on sample SRO3/5nm.

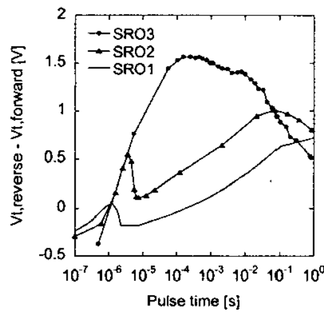

Fig. 16: Difference in forward and reverse read as function of program pulse time (Vg=9V, Vd=4V). Drain voltage during reading was 1.5V. Measured on SRO1, 2 and 3 with 5nm bottom oxide.

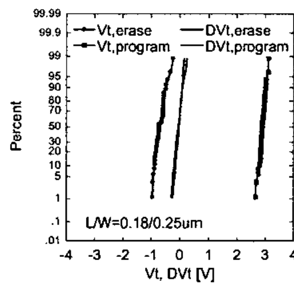

Fig. 17: Cumulative probability distribution of the linear Vt measured on 42 dies after F-N program/erase, as well as Vt-difference measured on matched transistor pairs, SRO3/2.5nm.

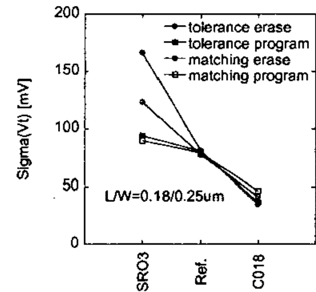

Fig. 18: Comparison of the Vt matching σ(Vt-Vt')/Sqrt(2) and tolerance σ(Vt).

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