A CMOS RF Bandpass Low Noise Amplifier for Multi-band Wireless Communication Applications

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Abstract

A new multi-band bandpass low noise amplifier was designed based on Charted Semiconductor Manufacturing (CSM) 0.25 m CMOS technology. The LNA is capable of a simultaneous operation at three different frequency bands: 900MHz-980MHz, 1.8GHz-2.5GHz and 5GHz-6GHz, with the corresponding peak gains to each band of 28.2dB, 25dB and 23.7dB respectively. The operating frequency range of this LNA covers almost all of the working bands of modern popular mobile/wireless communications, such as GSM900/1800, PCS/PHS, DECT, IMT-2000, the third-generation (3G) mobile communication, the Bluetooth, HiperLAN and some other bands indicated in IEEE 802.11a and 802.11b standards. The LNA also has the noise figure of no more than 5dB and the power consumption of 43mW at a low voltage supply of 1.5V. This design brings great convenience for modern multi-standard mobile/wireless communications and the system-on-chip (SoC) program.

1 Introduction

In the past few years, the wireless services industry has experienced a tremendous growth [1-2]. Mobile cellular and home cordless telephones are fast becoming a part of our daily lives. The wireless short-distance communication and the local area network communication (LAN) are becoming popular as well. The operating frequency bands of these communications range from 900MHz to about 6GHz. Table 1 lists part of the current communication standards.

Table 1. Some communication standards

Standard	GSM	PDC	IMT2000	Bluetooth
Frequency (GHz)	0.9/1.8/1.9	0.8/1.4	1.9-2.1	2.4
Standard	Wireless 1394	IEEE 802.1b	IEEE 802.11a	HiperLAN
Frequency (GHz)	5.2	2.4	5.2	5.15-5.35 5.47-5.725

With so many co-existing communication standards and at such high frequencies, these communication systems often consist of several ICs and many discrete components, which are bulky and power hungry in general. The highly competitive market demands low-cost, low-power and small form-factor devices. This calls for the development of a single-chip transceiver capable of adapting to the various communication standards in a low-cost CMOS technology [1].

Being the first stage in the receiving path, an LNA is an important building block of a single-chip transceiver. And one of the key bottlenecks for the multiple-standard applications is to design an LNA that can operate simultaneously in the different frequency bands. Recently, dual-band transceivers that use the conventional dual-band LNAs to cover several bands have been introduced [3-4]. This method will cause inevitable increase in the cost, footprint and power dissipation, because the conventional dual-band LNA uses two single-band LNAs, either one of which is selected according to the instantaneous band of operation [3], or both of which are designed to work in parallel using two separate input matching circuits and two separate resonant loads [4]. The former approach is non-concurrent while the latter consumes twice as much power. The other existing way is to use a wideband LNA, which will introduce strong unwanted bands and significantly degrade the receiver's sensitivity. In this work, a new concurrent multi-band CMOS LNA is proposed as one of the alternatives to alleviate these problems. The LNA can operate at multiple frequency bands of 900MHz-980MHz, 1.8GHz-2.5GHz and 5GHz-6GHz. It can satisfy the needs of almost all of the existent communication standards indicated above.

2 Design of the multi-band LNA

Traditional single-band LNA uses a single or cascode transistor stage with proper passive resonant circuits at the input and output to shape the frequency response and achieve the gain and matching at the single band of interest [5]. A very important observation here is that the transconductance of the transistor is still wideband and

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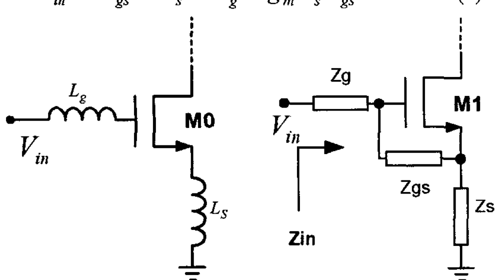
can be used to provide gains and matching at other frequencies of interest without any penalty in power consumption. This observation can be generalized to the designs of the dual-band/multi-band LNAs, which could provide simultaneous gains and matching at several bands of interest.

2.1 Input stage matching

In the design of an LNA, there are several common goals, including the minimum noise figure, the maximum gain with sufficient linearity, a stable 50 input impedance and the low power consumption which is very important for the portable systems. Recent research shows that the optimum topology, which could simultaneously fulfil all the above requirements is the inductively degenerated nMOS input stage [6] depicted in Figure 1(a). The analysis of noise and input matching has been presented in [5], where the optimum device size for minimum noise has also been defined. As known that the LNA described in [5] is a narrow band LNA, here some consideration about the input stage of the multiple-band LNAs will be given.

Figure 1(b) presents a general representation for the common-source configuration input stage, illustrated by the gate impedance Z_g, gate-source impedance Z_{gs} and source impedance Z_s. Note: the gate-source capacitance C_{gs1} is combined into Z_{gs}. Neglecting the effect of C_{gd}, the input impedance can be expressed as

$$Z_{in} = Z_{gs} + Z_s + Z_g + g_m Z_s Z_{gs} \qquad (1)$$



(a) (b)

Figure 1. The typical input stage of an LNA. (a) The inductive degeneration input stage; (b) a general representation of the common-source configuration

With the same analysis method presented in [5], the noise factor (F) can also be obtained:

$$F = 1 + \left|1 + \frac{1}{50}(Z_g + Z_{gs} + Z_s)\right|^2 \bullet \frac{1}{g_m^2 |Z_{gs}|^2} \bullet \frac{\overline{i_{nd}^2}}{\overline{i_s^2}} \qquad (2)$$

where $\overline{i_s^2}$ is the noise due to the 50 reference source impedance and $\overline{i_{nd}^2}$ is the channel noise of M1. The expression (2) indicates two messages: first, a larger g_m can improve the noise figure, which of course will cause more power consumption; second, the minimum noise figure (NF) occurs when

$$Z_g + Z_{gs} + Z_s = 0 \qquad (3)$$

Then to achieve the simultaneous minimum noise figure and input impedance matching at the input stage, the conditions as follows should be met at all frequencies of interest

$$\begin{cases} Z_{gs} + Z_s + Z_g = 0 \\ Z_{in} = g_m Z_s Z_{gs} = 50 \end{cases} \qquad (4)$$

The expression (4) can be regarded as the general constraint for the design of a concurrent dual-band/multi-band LNA.

2.2 The design of the multi-band LNA

The design criteria (4) can be satisfied with the combination of two parallel LC networks in series with the gate inductor and the degeneration source inductor. By tuning the passive components, the two parallel LCs of Z_g can resonate with $Z_{gs}+Z_s$ at all frequencies of interest. In addition, to minimize NF, one should maximize g_m as previously mentioned. Of course, there is a tradeoff between the noise figure and the power consumption. According to the above points, a multi-band LNA is designed.

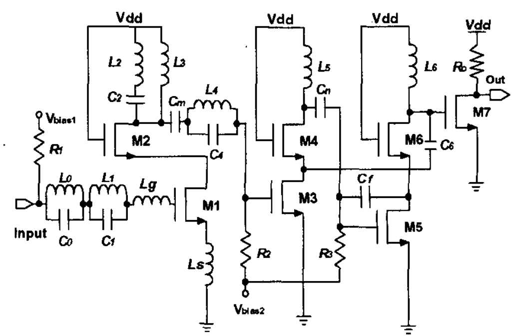


Figure 2. The schematic diagram of the multi-band LNA

Fig.2 is the schematic diagram of the proposed multi-band LNA. It's a three-stage amplifier with an additional buffer stage M7 and R_0. The LC tanks of L_0C_0 and L_1C_1, the inductors L_g and L_s, and the gate to source capacitance C_{gs1} form the input matching network (to 50). Transistors M1 and M2, M3 and M4, M5 and M6 form three cascode stages respectively.

In this design, great efforts have been made to shape the passbands of the LNA. The inductors L_g, L_3, L_5 and L_6 are designed to resonate at four different frequencies, the proper selection of which can determine the main frame of the gain transfer function curve. The L_2C_2 series branch in parallel with the inductor L_3 is used to shape the passband of the amplifier too. Each LC series branch can introduce a zero into the gain transfer function of the

LNA at its series resonant frequency. The frequencies of zeros determine the locations of the deep notches in the S_{21} curve. Tuning the resonant frequency of the LC series branch to the unwanted frequency band, such as the band of 3GHz-4.5GHz, there will be a notch between the second and third passbands of the gain transfer function (illustrated in the simulation result of S_{21}, shown in Figure 4). This leads to the LNA's band-selection function. The L_4C_4 parallel network between the first and second stages is a simple band-pass filter. The capacitor C_6 connected between the drain of M6 and the source of M4 is used to introduce a negative feedback so as to flatten the third passband in S_{21}.

The main objective of introducing the feedback capacitor C_f connected between the gate and drain of M5 is to provide a low resonant frequency ω for L_5 for the bandwidth extending purpose, while keeping the values of resonant components and the power consumption of the active device low. Figure 3(a) demonstrates the effect of C_f. According to the Miller theory, this capacitor is equivalent to two separate capacitors at the input port

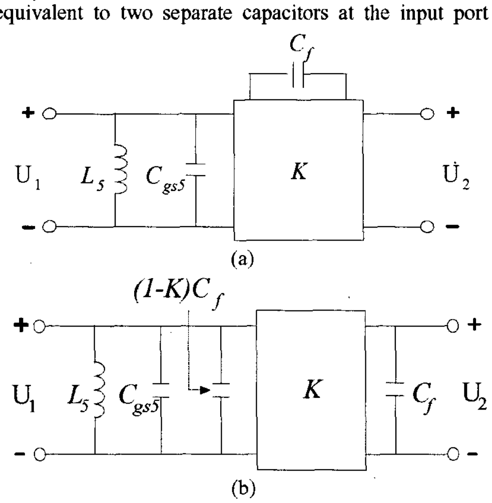


Figure 3. The Miller effect of C_f

and output port, $C_{in} = (1-K)C_f$ and $C_{out}=C_f$ respectively, shown in Figure 3(b). K is the gain of M5, which is negative. The required lower frequency is $\omega = \frac{1}{\sqrt{L_5 C_{gs5}}}$, in order to decrease this frequency, the value of L_5 or C_{gs5} must be increased. A large L_5 is prohibitive for on-chip fabrications. A large C_{gs5} can be obtained by increasing the width of the transistor M5, but this will cause higher power consumption. By adding C_f, the resonant frequency will change to $\omega = \frac{1}{\sqrt{L_5[C_{gs5} + (1-K)C_f]}}$. Hence, a lower resonant frequency ω can be obtained without increasing the inductor L_5 or the power consumption of M5.

3. Simulation results

The proposed LNA is simulated with Cadence's SpectreRF software using CSM 0.25 m CMOS RF models. The performance of the LNA is listed in Table 2. Some of the results are depicted in Figure 4-Figure 7. The results indicate that the input reflection coefficient (S_{11}), the output reflection coefficient (S_{22}) and S_{12} all match very well. Especially, the shape of the S_{21} shows that the LNA designed has the function of band-selection, which can be demonstrated by the notches of 1.0GHz-1.5GHz and 2.8GHz-4.3GHz, shown in Figure 4. This function reduces the responsibility of the subsequent band-pass filter.

Table 2. The multi-band LNA's performance

	1st band	2nd band	3rd band
Vdd (V)	1.5		
Pd (mW)*	43 (15)		
W_{-3dB} GHz)	N/A	1.8~2.5	5~6
NF (dB)	<3	<4	<5
S_{21} (dB)[1]	28.2	25	23.7
S_{11} (dB)[2]	-21	-32	-20
S_{22} (dB)	-29 ~ -15		
S_{12} (dB)	<-100		
IP_3 (dBm)	-16.3	-16.6	-19.8

*: The power dissipation excludes the consumption of the buffer stage, which is indicated in the bracket.
[1,2]:The value at the centre frequency.

The simulation result of the noise figure illustrated in Figure 7 has several high peaks. Since the peaks locate in the unwanted bands, there is no influence on the performance of the LNA at the wanted bands.

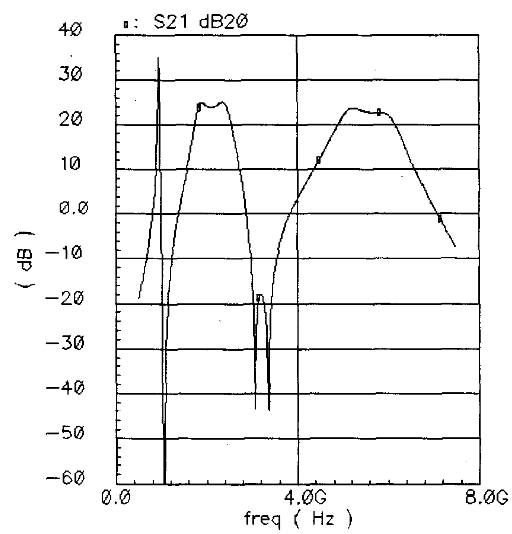


Figure 4. The simulation result of S_{21}

4. Conclusion

For the first time, a new CMOS multi-band bandpass LNA has been designed based on a CMOS technology. The LNA works at a low voltage supply of 1.5V and has three operating frequency bands: 900MHz-980MHz, 1.8GHz-2.5GHz and 5GHz-6GHz. The passbands cover most of the current wireless communication bands, such as GSM900/1800, PCS/PHS, DECT, IMT-2000, 3G, ISM, the Bluetooth, HiperLAN, wireless LAN and some of other communication bands. This design will bring great changes in modern wireless communications and the wireless local area networks communication.

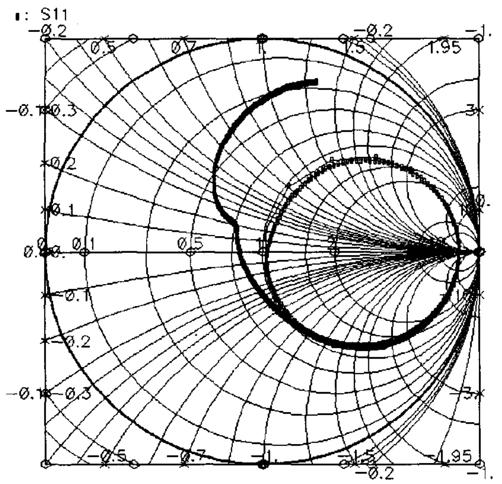


Figure 5. The simulation result of S_{11}

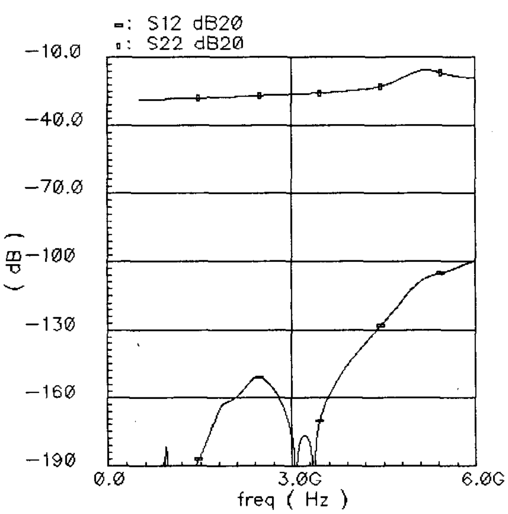


Figure 6. The simulation results of S_{12} and S_{22}

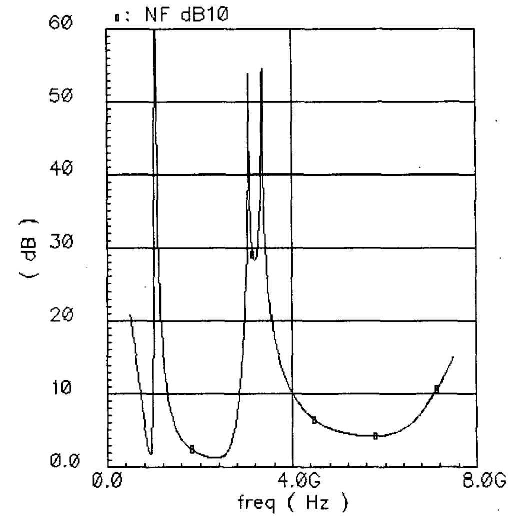


Figure 7. The simulation result of noise figure

Reference:

[1] Elwan H., Alzaher H., and Ismail M., "A New Generation of Global Wireless Compatibility", *IEEE Circuits & Devices Magazine,* vol.17, pp.7-19, January 2001.

[2] Akira Matsuzawa, "RF-SoC-Expectations and Required Conditions," *IEEE Trans. Microwave Theory Tech.*, vol.50, No.1, pp.245-253, January 2002.

[3] Jussi Ryynänen, Kalle Kivekäs, and Jarkko Jussila, "A Dual-Band RF Front-End for WCDMA and GSM Applications", *IEEE J. Solid-State Circuits,* vol.36, pp.1298-1204, August 2001.

[4] S.Wu and B.Razavi, "A 900MHz/1.8GHz CMOS Receiver for Dual Band Applications", *ISSCC Digest,* pp.124-125, February 1998.

[5] D. K. Shaeffer and T. H. Lee: "A 1.5-V 1.5-GHz CMOS low noise amplifier," *IEEE J.Solid-State Circuits,* vol. 32, pp. 45–759, March 1997.

[6] Hossein Hashemi and Ali Hajimiri: "Concurrent Dual-Band CMOS Low Noise Amplifiers and Receiver Architectures," *Symposium on VLSI Circuits Digest of Technical Papers*, pp.247-250, 2001.

[7] Franceso Gatta, Enrico Sacchi, Franceso Svelto, Paolo Vilmercati, and Rinaldo Castelloo, "A 2-dB Noise Figure 900-MHz Differential CMOS LNA," *IEEE J. Solid-State Circuits,* vol.36, No.10, pp.1444-1452, October 2001.