IV. A METHOD FOR MAKING " $H_{0...0}$ " Nonsingular

Suppose $H_{0...0}$ of (1) is singular with row rank q. Then there is a nonsingular matrix S_0 such that

$$\overline{H}(s_1,\cdots,s_p)=S_0H(s_1,s_2,\cdots,s_p)$$

(8)

where

$$\overline{H}_{0\cdots0} = \begin{bmatrix} H_{0\cdots0}^{*} \\ \hline 0 \end{bmatrix} \text{ with rank } [H_{0\cdots0}^{*}] = q$$

and

$$\overline{H}_{i_1\cdots i_p} = \begin{bmatrix} H_{i_1\cdots i_p}^* \\ -\overline{H}_{i_1\cdots i_p} \end{bmatrix}, \qquad i_m = 0, 1, \cdots, n_m \quad (m = 1, 2, \cdots, p).$$

Now, choose among $\tilde{H}_{0\cdots 0s,0\cdots 0}$ $(y=1,2,\cdots,p)$ the coefficient matrix which has the greatest rank and premultiply (8) by

$$M(s_y) = \begin{bmatrix} I_q & 0\\ 0 & \frac{1}{s_y} I_{r-q} \end{bmatrix}$$

Then we have

$$A(s_1,\cdots,s_p) = M(s_v)\overline{H}(s_1,\cdots,s_p)$$

which is generally a rational matrix of the form:

$$A(s_1, \cdots, s_p) = K(s_1, \cdots, s_p) + \sum_{i=1}^{n_1} A_{1i} \frac{s^i}{s_y} + \sum_{i=1}^{n_{y-1}} A_{y-1,i} \frac{s_{y-1}^i}{s_y} + \sum_{i=1}^{n_{y+1}} A_{y+1,i} \frac{s_{y+1}^i}{s_y} + \sum_{i=1}^{n_p} A_{pi} \frac{s_p^i}{s_y},$$

Now introducing auxiliary variables

$$x_i = \frac{s_i}{s_y} \qquad (i = 1, \cdots, y - 1, y + 1, \cdots, p)$$

in (9), we get

$$T(s_1, \dots, s_p, x_1, \dots, x_{y-1}, x_{y+1}, \dots, x_p) = T(s; x) = A(s_1, \dots, s_p)$$

where T(s; x) is a polynomial matrix of (2p-1) variables. Notice that the constant coefficient matrix of T(s; x) is

$$T_{0\cdots 0} \left[\frac{H_{0\cdots 0}^{*}}{\tilde{H}_{0\cdots 0i,0\cdots 0}} \right].$$

If $T_0 \cdots 0$ is full rank, then

$$H^{-1}(s) = T^{-1}(s; x) | M(s_y) S_0$$
(10)
$$x_i = s_i / s_y.$$

If $T_{0...0}$ is not full rank the procedure above may be repeated to get a new polynomial matrix of [2(2p-1)-1] variables until $T_{0\cdots 0}$ becomes full rank.

REFERENCES

- [1] Ö. Hüseyin, "Inversion of multidimensional polynomial matrices," J.
- O. Huseyin, "Inversion of multidimensional polynomial matrices," J. AEU, Band 33, Heft 11, pp. 457-462, Nov. 1979.
 C. S. Koo and C. Chen, "Fadeeva's algorithm for spatial dynamical equations," Proc. IEEE, vol. 65, pp. 975-976, June 1977.
 E. Emre, and Ö. Hüseyin, "Two computational algorithms for computer-aided design," in SSCT Conf., the Prague Czechoslavakia.
 E. Emre, O. Hüseyin, and K. Abdullah, "Author's reply on the com-ments on on the inversion of rational matrices" IEEE Trans. Circuits
- ments on, on the inversion of rational matrices," IEEE Trans. Circuits and Syst. pp. 375-376, Apr. 1975.

0098-4094/80/0300-0226\$00.75 ©1980 IEEE

A Switched-Capacitor High-Pass Filter

ROUBIK GREGORIAN AND WILLIAM E. NICHOLSON, JR.

Abstract-A high-pass switched-capacitor biquadratic filter section is described. It is economical and has sufficiently low sensitivities to element-value variations and parasitics to make it useful in a variety of applications. For analog input, it can be supplemented with a first-order filter section which prevents direct signal leakthrough.

I. INTRODUCTION

A number of recent publications [1]-[4] discussed the design of filters using only switches, capacitors, and operational amplifiers. In particular, [2] described second-order filter sections which could realize low-pass or bandpass transfer functions. The purpose of this letter is to present a related circuit which realizes a high-pass characteristic. It is economical, and both theory and experiments indicate that its sensitivities to element imperfections are sufficiently low for most practical applications.

II. FILTER CIRCUIT

The basic circuit is shown in Fig. 1(a); the timing diagram in Fig. 1(b). Denoting $v_1(t)$ at t = (n-1)T by $v_1(n-1)$, etc., the operation of the circuit can be described as follows. At $t = (n - 1)^{-1}$ 1)T, we have $v_1(n-1) = v_{in}(n-1)$. During the following $\phi = 1$ interval, v_1 is held at $v_{in}(n-1)$ by the capacitor C. Also, $\alpha_1 C_1$ and $\alpha_2 C_2$ are both charged to $v_0(n-1)$, while $\alpha'_1 C_1$ to $v_2(n-1)$. Next, when $\phi = 0$, $\alpha_1 C_1$ as well as $\alpha'_1 C_1$ are discharged into C_1 , while the charge in $\alpha_2 C_2$ enters C_2 . The corresponding chargeconservation equation is

(9)
$$C_1 v_0(n) = C_1 v_0(n-1) - \alpha_1 C_1 v_0(n-1) - \alpha_3 C_1 [v_{in}(n) - v_{in}(n-1)] \quad (1)$$

or, after taking the z-transforms of both sides

$$V_0(z) \left[1 - z^{-1} (1 - \alpha_1) \right] = -\alpha_1' z^{-1} V_2(z) - \alpha_3 (1 - z^{-1}) V_{in}(z).$$
(2)

A similar analysis performed for the stage containing the second amplifier gives

$$V_2(z)(1-z^{-1}) = \alpha_2 z^{-1} V_0(z).$$
(3)

Combining (2) and (3) gives the transfer function

$$H_0(z) \triangleq \frac{V_0(z)}{V_{\rm in}(z)} = \frac{-\alpha_3(z-1)^2}{z^2 - z(2-\alpha_1) + (1-\alpha_1 + \alpha_1'\alpha_2)}$$
(4)

Equation (4) describes a second-order high-pass filter characteristic, with two complex-conjugate poles and a double zero at dc (i.e., at z = 1). Note that $H_0(z)$ is similar in form to the bandpass and low-pass functions of the "version 1" filters discussed in [2].

The circuit of Fig. 1 is suitable as a self-contained filter only if the input signal is a sampled-and-held waveform, so that v_{in} does not change during the $\phi = 0$ half cycle. Otherwise, the output follows the input during this period, and hence there is a direct signal leakthrough, which affects the overall frequency response. To avoid this, a sample-and-hold stage can be cascaded with the

Manuscript received August 31, 1978; revised April 16, 1979. The authors are with American Microsystems Inc., Santa Clara, CA 959051.

IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS, VOL. CAS-27, NO. 3, MARCH 1980



Fig. 1. Second-order switched-capacitor high-pass filter. (a) Circuit diagram. (b) Timing diagrams.



Fig. 2. Third-order high-pass filter.

filter. A more efficient technique is, however, to cascade a first-order filter section with the original one (Fig. 2). Since the clocking of the added stage is the complement of that of the first, the leakthrough is blocked at all times. The overall transfer function is now

$$H_{01}(z) \stackrel{\scriptscriptstyle \triangle}{=} \frac{V_{01}(z)}{V_{in(z)}} = \frac{\alpha_3 \alpha_5 (z-1)^3}{[z-(1-\alpha_4)] [z^2 - z(2-\alpha_2) + (1-\alpha_1 + \alpha_1' \alpha_2)]} .$$
(5)

This has one real and two complex conjugate poles, and also three zeros at dc.

III. DESIGN EXAMPLE

Next, as an example, the bilinear z transformation [6], [7] will be used to derive the transfer function of a third-degree highpass filter with the following specifications:

Stopband loss: $\alpha \ge 25$ dB for $f \le 130$ Hz

Passband loss: $\alpha \leq 0.01$ dB for $f \geq 600$ Hz.

Prewarping these band-limit frequencies to account for the nonlinear scale distortion [6], [7] gives the transfer function of the analog prototype:

$$H(s) = \frac{5.207s^3}{(A+1.59s)(A^2+1.59As+3.28s^2)}$$
(6)

where $A = 1200\pi$. Using a clock frequency of 16 kHz, the bilinear transformation gives

$$H(z) = \frac{0.877(z-1)^3}{(z-0.862)(z^2-1.876z+0.892)}.$$
 (7)

Equating coefficients in (5) and (7) gives $\alpha_1 = \alpha'_1 = 0.124$, $\alpha_2 = 0.129$, $\alpha_3\alpha_5 = 0.877$, and $\alpha_4 = 0.138$. Note that only the product, not the individual values of α_3 and α_5 are defined.

A discrete-element experimental circuit was constructed to verify the above theoretical results. The operational amplifiers used were RCA CA-3140 units, the transmission gates Motorola MC 14066B integrated circuits. The measured results are shown in Fig. 3, which also illustrates the 0.2-dB droop due to the sample-and-hold effect.

IV. NONIDEAL EFFECTS

Next, the susceptibility of the circuit to nonideal effects will be discussed. The circuit will not function properly if either a dc bias in v_{in} or the inherent offset voltages of the amplifiers are amplified so much that they drive one or more of the amplifiers into saturation. Due to the presence of the transmission zeros at dc, any dc bias component in the input voltage is blocked, and cannot affect the output of any of the operational amplifier. Hence, only the dc offset voltages which originate in the amplifiers themselves are of concern. A detailed analysis shows that the largest worst-case dc offset voltage appears at the output of amplifiers 2. Its value is $2|v_{off_1}| + |v_{off_2}|$, where v_{off_i} denotes the equivalent dc input voltage of amplifier i (Fig. 4). This indicates that in order to avoid the saturation of amplifier 2, and to achieve the largest possible dynamic range, α_3 should be decreased. This will cause smaller values for v_0 and v_2 . Therefore, α_5 should be increased to enhance the gain of the last stage. The corresponding improvement in dc offset was observed experimentally.

The sensitivities of the frequency response to element-value variations are discussed next. The values of the grounded input capacitors C are unimportant, as long as their voltage droops due to leakage currents remain small during a half-clock period. The capacitance ratios α_3 and α_5 affect the flat gain only, and hence their exact values do not influence the selectivity properties of the filter. By contrast, α_1 , α'_1 , α_2 , and α_4 affect the values of the poles. In particular α_1 , α'_1 , and α_2 , determine the location of the complex pole-pair which is normally the dominant one.

A critical situation arises when the pole-Q is high, i.e., the poles are very close to the unit circle. If, as is usually the case, the clock-radian frequency is much higher than the angle θ_p of the poles $z_p = r_p \exp(\pm j\theta_p)$, then the demoninator polynomial of (4) can be written in the form $D(z) = z^2 - (2 - \Delta_1)z + (1 - \Delta_2)$, with $\Delta_1, \Delta_2 \ll 1$. The distance of z_p from the unit circle is determined solely by Δ_2 . Since in the given circuit the α_i determine directly the Δ_i (not $2 - \Delta_1$ and $1 - \Delta_2$) according to the relations

$$\Delta_1 = \alpha_1, \quad \Delta_2 = \alpha_1 - \alpha_1' \alpha_2 \tag{8}$$

it is to be expected that the sensitivity of the pole-Q to these parameters is reasonably low. In fact, let the desired analog natural-mode polynomial of the filter be

$$P(s) = s^2 + \frac{\omega_0}{Q}s + \omega_0^2.$$

iRhythm, Inc. / Welch Allyn, Inc. Exhibit 1051 Page 2



Fig. 3. Measured-loss response.



Fig. 4. Equivalent circuit for the calculation of offset-voltage effects.

Using the bilinear $s \rightarrow z$ transformation, P(s) can be transformed into the z-domain. The z-variable natural-mode polynomial thus obtained can be equated to the denominator of $H_0(z)$ in (4). Normalizing the time and frequency variables so that T = 1, this gives

$$\omega_0 = 2\sqrt{\frac{\alpha_1'\alpha_2}{4 - 2\alpha_1 + \alpha_1'\alpha_2}} \tag{9}$$

and

$$Q = \frac{\sqrt{\alpha_1' \alpha_2 (4 - 2\alpha_1 + \alpha_1' \alpha_2)}}{2(\alpha_1 - \alpha_1' \alpha_2)}.$$
 (10)

From (9) and (10), the logarithmic sensitivities of ω_0 and Q to the variables α_1 , α'_1 , and α_2 can readily be obtained. Defining the

usual way $S_x^y = x/y \partial y/\partial x$, the results are

$$S_{\alpha_1}^{\omega_0} = \frac{\alpha_1}{4 - 2\alpha_1 + \alpha_1' \alpha_2}.$$
 (11)

Since, as (8) shows, α_1 , α_2 , and $\alpha'_1 \leq 1$, in the worst case we have

$$S_{\alpha_1 \max}^{\omega_0} = \frac{\alpha_1}{4 - 2\alpha_1 + \alpha_1' \alpha_2} \bigg| \begin{array}{c} = 0.5 \\ \alpha_1 \rightarrow 1 \end{array}$$
(12)
$$\alpha_1' \alpha_2 \rightarrow 0$$

Also,

$$S_{\alpha_{1}}^{\omega_{0}} = \frac{2 - \alpha_{1}}{4 - 2\alpha_{1} + \alpha_{1}'\alpha_{2}}$$

$$S_{\alpha_{1}\max}^{\omega_{0}} = \frac{2 - \alpha_{1}}{4 - 2\alpha_{1} + \alpha_{1}\alpha_{2}} \Big|_{\alpha_{1}'\alpha_{2} \to 0} = \frac{2 - \alpha_{1}}{2(2 - \alpha_{1})} = 0.5 \quad (13)$$

$$S_{\alpha_{2}}^{\omega_{0}} = \frac{2 - \alpha_{1}}{4 - 2\alpha_{1} + \alpha_{1}'\alpha_{2}}$$

$$S_{\alpha_{2}\max}^{\omega_{0}} = \frac{2 - \alpha_{1}}{4 - 2\alpha_{1} + \alpha_{1}'\alpha_{2}} \Big|_{\alpha_{1}'\alpha_{2} \to 0} = 0.5.$$

Similarly,

$$S_{\alpha_{1}}^{Q} = -\frac{(4-\alpha_{1})(1+\omega_{0}Q)^{2}\omega_{0}}{4\alpha_{1}Q}$$
(14)

and

$$S_{\alpha_{1}'}^{Q} = S_{\alpha_{2}}^{Q} = \frac{2\alpha_{1} - \alpha_{1}^{2} + 2\alpha_{1}'\alpha_{2}}{\alpha_{1}(4 - 2\alpha_{1} + \alpha_{1}'\alpha_{2})}(1 + \omega_{0}Q).$$
(15)

For $\alpha_1 = \alpha'_1$, using (9) and (10),

$$S_{\alpha_1}^{\mathcal{Q}} = S_{\alpha_2}^{\mathcal{Q}} = \frac{1 - \alpha_1/2 + \alpha_2}{(2 - \alpha_1 + \alpha_1 \alpha_2/2)(1 - \alpha_2)}.$$
 (16)

In usual case when $\alpha_1, \alpha_2 \ll 1$, $S_{\alpha_1}^Q \approx 0.5$. It should be noted, however, that for $\alpha_2 \rightarrow 1$ (and hence $Q \rightarrow \infty$), $S_{\alpha_1}^Q \rightarrow \infty$. For the design example, $S_{\alpha_1}^Q \approx 0.642$ results.

Finally, the effect of the finite amplifier gain A will be discussed. It will be assumed that the signal frequencies are lower than the break-point of the amplifier gain characteristic,

iRhythm, Inc. / Welch Allyn, Inc. Exhibit 1051 Page 3 and hence $A(\omega)$ is constant in the frequency range of interest. For $A < \infty$, the negative input voltages of the two amplifiers in Fig. 1 will be $-v_0/A$ and $-v_2/A$, respectively. Hence, (2) will be replaced by

$$C_{1}\left[v_{0}(n) + \frac{v_{0}(n)}{A}\right] = C_{1}\left[v_{0}(n-1) + \frac{v_{0}(n-1)}{A}\right]$$
$$-\alpha_{1}C_{1}\left[v_{0}(n-1) + \frac{v_{0}(n)}{A}\right] - \alpha_{1}C_{1}\left[v_{2}(n-1) + \frac{v_{0}(n)}{A}\right]$$
$$-\alpha_{3}C_{1}\left[v_{in}(n) + \frac{v_{0}(n)}{A} - v_{in}(n-1) - \frac{v_{0}(n)}{A}\right].$$
(17)

Using z-transformation,

$$V_0(z) \Big[1 - z^{-1} (1 - \hat{\alpha}_1) \Big] = -\hat{\alpha}_1' z^{-1} V_2(z) - \hat{\alpha}_3 (1 - z^{-1}) V_{in}(z)$$
(18)

results, where

$$\hat{\alpha}_{1} = \frac{(A+1)\alpha_{1} + \alpha'_{1}}{A+1+\alpha_{1} + \alpha'_{1} + \alpha_{3}}$$

$$\hat{\alpha}_{1}' = \frac{A\alpha'_{1}}{A+1+\alpha_{1} + \alpha'_{1}}$$

$$\hat{\alpha}_{3} = \frac{A\alpha_{3}}{A+1+\alpha_{1} + \alpha'_{1}}.$$
(19)

For $\alpha_1 = \alpha'_1$ and $A \gg 1$, these expressions can be simplified. For example, $\hat{\alpha}_1 \simeq \alpha_1 [1 - (2\alpha_1 + \alpha_3 - 1)/A]$ is obtained.

Performing a similar analysis on the second stage, it turns out that (3) is replaced by

$$V_{2}(z)\left[1-\left(1+\frac{\hat{\alpha}_{2}}{A}\right)z^{-1}\right] = \hat{\alpha}_{2}z^{-1}V_{0}(z)$$
 (20)

where

$$\hat{\alpha}_2 = \frac{A\alpha_2}{A+1-\alpha_2}.$$
 (21)

Combining (18) and (20), the modified transfer function $\hat{H}_0(z)$ can be obtained and evaluated. Alternatively, (19) and (21) can be used to find the relative changes in the α_i due to the finite gain, and (11)–(16) applied to obtain the corresponding change in ω_0 and **Q**. For the amplifiers used in the filters designed by the authors, $A > 10^4$ in the low-frequency band, and the finite-gain effect was found to be negligible in all cases encountered.

References

- J. T. Caves et al., "Sampled analog filtering using switched capacitors as resistor equivalents," *IEEE J. Solid-State Circuits*, vol. SC-12, pp. 392-599, Dec. 1977.
- B. J. Hosticka et al., "MOS sampled-data recursive filters using switched capacitor integrators," *IEEE J. Solid-State Circuits*, vol. SC-12, pp. 600-608, Dec. 1977.
 G. C. Temes, "The derivation of switched-capacitor filters from active-
- [3] G. C. Temes, "The derivation of switched-capacitor filters from active-RC prototypes," Electron Lett., vol. 14, no. 12, pp. 361-362, June 8, 1978.
- [4] —, "Digital-filter design techniques for the synthesis of switchedcapacitor active circuits," in Proc. Int. Conf. on Digital Signal Processing (Florence, Italy), Aug. 1978.
- [5] J. Tow, "A step-by-step active filter design," IEEE Spectrum, vol. 6, pp. 64-68, Dec. 1969.
- [6] L. R. Rabiner and B. Gold, *Theory and Application of Digital Signal* Processing. Englewood Cliffs, NJ: Prentice Hall, 1975.
- [7] A. V. Oppenheim and R. W. Schafer, Digital Signal Processing. Englewood Cliffs, NJ: Prentice Hall, 1975.
- [8] G. C. Temes and J. W. LaParra, Introduction to Circuit Synthesis and Design. New York: McGraw-Hill, 1977.

New Results on the Ability of *LC* Networks to Realize Natural Frequencies

S. E. SUSSMAN-FORT

Abstract—A theorem proved by Lee states necessary and sufficient conditions for an LC network of a special structure to be able to realize an arbitrarily prescribed set of natural frequencies. A new proof of the sufficiency of these conditions is presented here. The proof is based upon a recent mathematical result and provides, in addition, bounds upon the element values in such an LC network realizing a given set of natural frequencies.

I. INTRODUCTION

The following definitions are given in [1].

- An LC network of complementary-tree structure is one in which both the capacitors and the inductors separately form a tree.
- 2) A *shunt-reducible LC* network is one which can be reduced to a single node by successively short-circuiting loops that contain only one inductor and one capacitor.

An example of the shunt-reduction of a complementary-treestructure LC network is shown in Fig. 1.

In [1], Lee proves that a necessary and sufficient condition for a complementary-tree structure LC network to be able to realize an arbitrary set of pure imaginary natural frequencies is that the network be, in addition, shunt-reducible. The necessity of the shunt-reducibility condition is proved by demonstrating the rather remarkable result that the maximum and minimum absolute values of natural frequency, ω_{max} and ω_{min} , of a nonshunt-reducible, complementary-tree structure LC network are constrained by the relation $\omega_{max} > 2\omega_{min}$ for all sets of positive element values. The proof of sufficiency, however, relies upon scaling the impedance levels of successive loops of inductors and capacitors so that the loops produce the natural frequencies with negligible interaction. We offer a new proof of the sufficiency condition which does not require that the network consist, in effect, of disjoint loops. This new result is based upon two interesting lemmas that we prove below, and a mathematical theorem recently proved by de Oliveira [2].

II. PRELIMINARY RESULTS

We first formulate the notation that will be used in the remainder of this paper. Consider an arbitrary, complementarytree structure LC network containing n capacitors and n inductors which are arbitrarily numbered C_1, C_2, \dots, C_n and L_1, L_2, \dots, L_n , respectively. The capacitors are designated as forming the tree for the network, with the inductors evidently forming links with this tree. The fundamental loop matrix of the network can then be written as

$$F \quad \mathbf{1}_n] \tag{1}$$

where F is $n \times n$, and l_n is the $n \times n$ identity matrix. We define the diagonal matrices

$$L = \operatorname{diag}(L_1, L_2, \cdots, L_n) \qquad C = \operatorname{diag}(C_1, C_2, \cdots, C_n)$$
$$D = \operatorname{diag}(d_1, d_2, \cdots, d_n) \qquad P = \operatorname{diag}(p_1, p_2, \cdots, p_n) \qquad (2)$$

Manuscript received January 16, 1979; revised April 19, 1979.

L

The author is with the Department of Electrical and Systems Engineering, Rensselaer Polytechnic Institute, Troy, NY 12181.

0098-4094/80/0300-0229\$00.75 ©1980 IEEE