

Single-Package Integration of RF Blocks for a 5 GHz WLAN Application

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Abstract—Transceivers for future digital telecommunications applications (third generation cellular, wireless LAN) need to be portable (compact), battery-powered and wireless. Today's single-chip solutions for RF front-ends do not yield complete system integration. For example, they typically still need external components for impedance matching, for antenna switches, for power amplifiers and for RF bandpass filters (BPFs). Furthermore, problems of substrate coupling (either manifesting as analog crosstalk or as noise coupling from the digital part to the analog part on mixed-signal chip) become more important with increasing integration.

A system-in-a-package (SiP) approach can address these problems. High quality components can be integrated in the package, avoiding lower quality on-chip passives or circumventing expensive chip technology adaptations. Virtually all external components can be integrated, as shown in this paper for the case of the bandpass filters and the impedance matching. Even the antenna is a candidate for integration in the package. Further, a clever chip partitioning can reduce the substrate coupling problem. Partitioning also allows using the best IC-technology for each component.

This paper reports on a fully integrated single-package RF prototype module for a 5 GHz WLAN receiver front-end, which is intended to demonstrate the concept of SiP integration. The approach, that is illustrated here with prototype RF blocks for a 5 GHz WLAN application, is implemented with a thin film multi-chip module (MCM-D) interconnect technology. This technology also allows the integration of high quality passive components. With these passives, low-loss filters can be implemented. The use of passives, filters and off-the-shelf, active, bare die components opens the way to successful system integration.

Index Terms—Bandpass filter, downconverter, low noise amplifier, MCM, RF front-end, single-package integration, system-in-a-package, transceiver, wireless LAN.

I. INTRODUCTION

IN THE booming market of wireless digital telecommunications, manufacturers of transceivers spend a lot of effort to lower the cost of their transceivers, with at the same time an increase of the performance and a reduction of the power consumption. Achieving a higher degree of integration for these transceivers is very helpful to obtain these goals. The ultimate goal would be a single-chip solution, often referred to as a system-on-a-chip (SoC). For cost reasons, this integration would make use of a silicon IC technology (CMOS or BiCMOS).

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Fig. 1. Block diagram of the single-package 5 GHz receiver front-end.

Silicon technologies, however, suffer from a limited performance. It is perhaps not the transistors performance itself that is a bottleneck, but rather the quality of interconnect and passive components. There are several reasons for the relatively low quality of passive components, as explained in Section III.

Only a limited amount of publications for 5 GHz applications in silicon technologies (e.g., [1], [2],) have been published. Other wireless applications, such as IEEE 802.11b (WLAN standard at 2.4 GHz) and Bluetooth, are often less demanding for the RF front-end than 5 GHz WLAN because they operate at lower frequencies, use smaller bandwidth, need smaller dynamic ranges, etc. In this paper, we concentrate on the realization of front-end blocks for 5 GHz WLAN. This application, together with some specifications for the front-end is discussed in Section II.

For the realization of the RF front-end for 5 GHz WLAN we propose an alternative for SoC with a much better performance of passive components: a single-package approach, often referred to as a system-in-a-package. This approach uses high-quality passive components that are realized in a thin-film MCM (MCM-D) interconnection technology. At the same time, the MCM substrate is a carrier for the integrated circuits that are mounted on this substrate preferably with a flip-chip technique. This technology is further explained in Section IV.

The high quality factor of passive components that are realized in the MCM-D technology enables a successful integration of RF filters with an acceptable insertion loss in the passband, which is not the case with an SoC approach. Some MCM-D designs of RF filters are discussed in Section V.

The integration of a front-end on an MCM-D module that uses high-quality passive components, enables the use of the proven-good superheterodyne architecture. Section VI describes the single-package integration of part of a superheterodyne receiver front-end. The front-end comprises two bandpass filters, a low noise amplifier (LNA) and a downconversion mixer, as shown in Fig. 1.

The active components are commercially available, "bare die" components, which are flip-chip mounted onto the MCM substrate. The MCM module integrates some passives for the active circuits, impedance matching for the LNA and

two lumped-element bandpass filters. The two integrated bandpass filters avoid the use of discrete RF filters, which are still required in “single-chip” solutions. This minimizes the number of components to be mounted. The 5.25 GHz RF input signal is downconverted to a fixed intermediate frequency (IF) of 500 MHz. The IF frequency is kept fixed by ranging the local oscillator (LO) frequency depending on which channel is to be received. The measurements are done for an LO frequency around 4.75 GHz. This means that the so-called image frequency for the mixer lies around 4.25 GHz, which is the difference of the (variable) LO frequency and the (fixed) IF frequency. Since the downconverter is as sensitive to the RF frequency as to the image frequency, the signal components at the image frequency must be rejected. This is accomplished with one or more bandpass filters, centered on the RF frequency. The RF bandwidth of WLAN and the required image-signal rejection yield filtering up to fifth-order or sixth-order, for the whole RF-part of the receiver chain.

II. SPECIFICATIONS FOR 5 GHz WLAN

Standardization activities for wireless local area networks (WLAN) in the 5 GHz ISM band have been evolving for a few years already. The American IEEE and European ETSI organizations are finalizing their respective standards for the 5 GHz band: IEEE 802.11a [3] and HIPERLAN/2 [4]. These two standards define nearly identical systems, based on orthogonal frequency division multiplexing (OFDM) modulation. OFDM is a multicarrier modulation technique that efficiently manages intersymbol interference and multipath distortions, making it very suited for indoor wireless communications. The standards foresee several data rates up to 54 Mbps, using different modulation schemes at different coding rates. The modulation schemes can be binary phase shift keying (BPSK), quadrature phase shift keying (QPSK) and quadrature amplitude modulation with 16 (16-QAM) and 64 points (64-QAM).

The IEEE 802.11a standard defines three frequency bands that can be used. A first band extends from 5.15 to 5.25 GHz, the second from 5.25 to 5.35 GHz and the third from 5.725 to 5.825 GHz. HIPERLAN/2 specifies two bands: from 5.15 to 5.35 GHz and from 5.470 to 5.725 GHz. Our design example only considers the frequency range from 5.15 to 5.35 GHz, which is common to both standards. This band is divided into eight channels with a nominal spacing of 20 MHz.

The IEEE 802.11a standard specifies further that the receiver should be able to receive a signal between -85 dBm and -30 dBm at the antenna and that the noise figure of the whole analog receiver chain should be less than 10 dB. Apart from that, the receiver must be able to withstand the effects of out-of-band blocking signals up to 0 dBm.

III. SiP VERSUS OTHER SOLUTIONS

For high-performance digital telecommunications a single-chip solution, which would serve the needs for low cost, small size and low power consumption, is very difficult or even impossible to obtain. An important reason for this is the inherent semiconductivity of the silicon substrate of an IC.

Substrate coupling between on-chip digital circuits and the RF blocks [5] becomes worse and induced eddy currents cause electrical losses, e.g., in interconnections [6] and passive components. Electrical losses are an important performance killer for SoC. They are the reason for low quality factors of on-chip passives, especially inductors. For example, in a $0.25 \mu\text{m}$ CMOS process with thick metal layers, quality factors in the order of 10 are reported [1]. Hence, it is impossible to make low-loss filters and matching networks, using on-chip inductors.

The frequency of self resonance of passive components also comes into play. This poses a limit to the useful frequency range of passives. Silicon on-chip realizations typically have lower self resonance frequencies, which is a natural consequence of the fact that these technologies and the used materials are not optimized for the passive devices, but for the active ones. Moreover, self resonance is an effect that is not always included in the models of on-chip passives that are provided by foundries of silicon technologies. Capacitors and resistors are often modeled with simple RC ladder networks, which do not model self resonance.

Some advanced adaptations of the IC technology partially overcome the limitations mentioned above. For example, thick metal layers and copper metallization are used more and more nowadays to lower the resistivity of the conductors. However, their enhancing effect is limited. Another adaptation is to implement local bulk etching, which partially replaces the lossy silicon with air, vacuum or another filler gas. This is the most effective adaptation, but it is an even more costly solution. And it is probably not going to be integrated in standard CMOS process flows, because it complicates processing significantly and probably also affects processing yield.

Therefore, today’s single-chip systems still require many off-chip components, such as the antenna, the RF bandpass filters, the antenna and the power amplifier.

Going to complete integration in GaAs is probably a good solution for performance, although quality factors of inductors are still lower than in our MCM-D technology. But this is a very costly solution.

The above considerations indicate that the largest problem of single-chip integration lies in the integration of the passives for high frequencies. Several architectures that eliminate the need for bandpass filters at intermediate frequencies (IF) in the range of a few tens of MHz up to a few hundreds of MHz, have been reported. Examples of such architectures are zero-IF and low-IF [7]. However these architectures still need off-chip filters at RF frequencies. The integration of the passives in technologies other than IC-technologies, that are still included in the same package, solves this. This leads to the concept of system-in-a-package (SiP) [8]. The integration of RF bandpass filters and impedance matching is discussed below.

Partitioning a system over a number of chips, which can still be mounted in a single package, also circumvents substrate coupling since the conductive silicon substrate is replaced by a glass substrate that is almost a perfect insulator. In addition, one does not have to stick to one IC-technology. Every component can be integrated in the best-fitted technology: e.g., CMOS for dig-

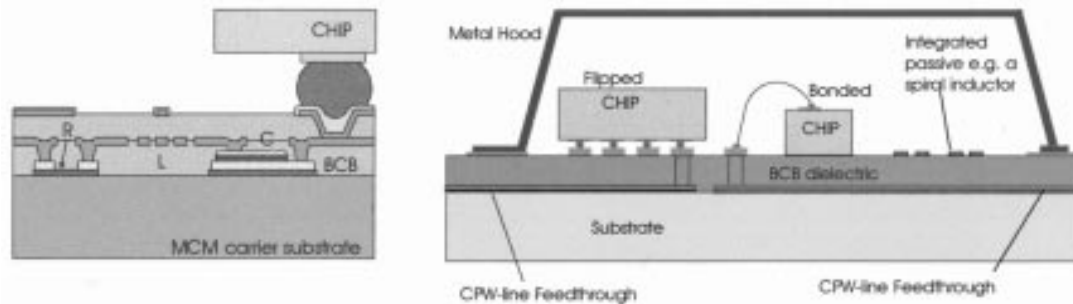


Fig. 2. Cross section of an MCM substrate with integrated passives and an indicative drawing of some supported mounting possibilities.

ital and BiCMOS for the low-frequency analog and the RF, except for the power amplifier. For the latter block, GaAs is probably required. This also leads to much more design freedom. An SoC approach for a high-end application would require the technology of the most demanding component for the whole chip. Otherwise, the performance might be jeopardized or the power consumption might become unacceptable.

Next to that, silicon-on-insulator (SOI) might be considered as an alternative solution. A lot of work has already been done in this area [9], [10]. SOI can also tackle the quality problem of the passives to some extent, if highly resistive substrates are used. However, SOI technologies have a much larger area cost than an MCM-D technology.

IV. AN MCM-D SUBSTRATE AS A CARRIER

The starting point for the presented SiP approach is a multi-chip module (MCM) technology. It is an interconnection technology on a common substrate. A substrate with low losses is required for RF applications. Here, a thin-film technology (MCM-D) with a glass substrate is used [11], [12]. Glass is a low-cost material with high resistivity and low microwave loss. The lithographic nature of a thin film technology guarantees lower component tolerances [13] in comparison with standard thick film or low temperature co-fired ceramic (LTCC) processes.

Several dielectric layers of benzocyclobutene (BCB, $\epsilon_r = 2.7$), alternating with copper metallization layers, are put on top of this glass substrate, forming the MCM-D. Fig. 2 shows a cross section of this technology. The top layer is gold-plated to ensure reliable mounting. High-quality inductors, BCB capacitors and coplanar waveguide (CPW) transmission lines can be embedded in this basic layer built-up.

The inductors are made in the metal 2 layer (3 μm thick copper). The inductor values range between 0.5 and 10 nH, with a maximum quality factor Q up to 100 at 10 GHz. The frequency of maximum Q and the maximum value of Q itself can be exchanged. Inductors with lower values have higher Q values, because they can be smaller (lower parasitics) or use wider metal tracks. An inductor with a larger inductance value using wider tracks would suffer a lower frequency of self-resonance due to higher parasitic capacitance. Therefore, inductors with lower inductance values can have higher Q -factors, given a certain technology and application (i.e., the required operation frequency). The maximum BCB capacitor value reaches 50 pF.

CPW transmission lines have some benefits over microstrip. They have one degree of freedom more, namely the spacing between the line itself and the ground plane. They also simplify the process from technological point of view. They use a ground plane in the same plane as the conductors such that an extra layer can be omitted. Moreover, via holes through the substrate for ground connections are not necessary.

Some extra processing steps allow the integration of tantalum nitride resistors and tantalum pentoxide (Ta_2O_5) capacitors in the technology. The resistors have a sheet resistance of 25 Ω per square. The plates of the Ta_2O_5 capacitors are formed between a split metal 1 layer. Electrically, they are complementary to the BCB-capacitors with values up to several nanofarads.

The technology can be used up to frequencies above 50 GHz. A library with fixed models for inductors and scalable models for capacitors, resistors and distributed CPW-elements has been developed and is implemented in Agilent's Advanced Design System [14]. The models are based on theoretical derivations and are confirmed with RF measurements up to 50 GHz.

An MCM-D module can host one or more chips, which can be mounted with bondwires or with a flip-chip technique. The latter technique is preferable, because it yields lower parasitic electrical effects. The principle of flip-chip is shown in Fig. 3. Solder bumps or gold-wire studs are placed on the substrate or on the chips. In this case 30 μm high gold-wire studs with a diameter of 50 μm are placed on the substrate. Subsequently, the chips are flipped and mounted on the substrate, with an IR-thermocompression step at 20 $^\circ\text{C}$. The mounted GaAs components have gold metallization layers.

V. INTEGRATION OF RF BANDPASS FILTERS IN MCM-D

This section explores the tradeoff between some different implementations of RF bandpass filters. It considers MCM-embedded, lumped element filters of two different orders, MCM-embedded filters using lumped capacitors with transmission line stubs, MCM-embedded distributed element filters and two commercial discrete filters. Since we are looking at the two lower frequency bands only, the passband of interest ranges from 5.15 to 5.35 GHz.

A discrete, custom-made LC-filter with six sections [15] could be used. Its passband (-1 dB) is between 5.075 and 5.425 GHz. The passband ripple is only 0.5 B. The insertion loss is 2.2 dB and the return losses at input and output are better than 14 dB. This discrete filter is called "miniature" but the

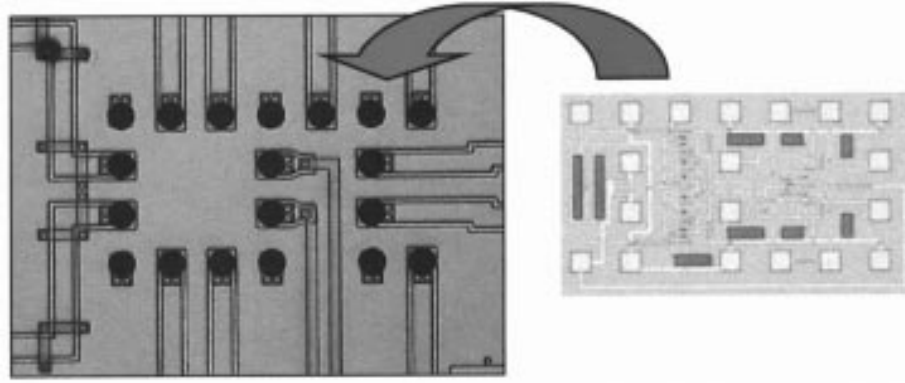


Fig. 3. Principle of flip-chip mounting. Left: detail of the MCM-D module with bumped pads. Right: chip, which is to be mounted upside-down on this module.

package still measures approximately $20 \times 10 \times 10 \text{ mm}^3$. The filter provides sufficient filtering for rejection of out-of-band signals. No further filtering in the RF chain is required. Another possibility is the use of ceramic filters such as the commercial 5.8 GHz ceramic filter of [16]. It is a three-section filter with an insertion loss of 2.5 dB. The bandwidth is 100 MHz. The filter provides a stopband rejection of 20 dB at 250 MHz offset from the center frequency. The size of this filter is $14 \times 20 \times 5 \text{ mm}^3$. Dielectric filters like [17] are probably the best choice considering size. The package of this filter measures $4.2 \times 3.4 \times 1.94 \text{ mm}^3$. It has a center frequency of 5.25 GHz and a bandwidth of 200 MHz. The insertion loss is smaller than 2 dB. Surface acoustic wave (SAW) filters for these frequencies currently do not exist.

Note that these filters are trimmed filters, with superior performance. They are useful as a point of reference to evaluate the designed filters. Also notice the dimensions of the filters, which are the kind of filter one would need in combination with a single-chip front-end.

Implementing this design in a planar technology such as MCM-D imposes some restrictions. For any device in front of the low noise amplifier (LNA), the insertion loss should be minimized, since the value of the insertion loss (expressed in dB) directly adds to the noise figure of the complete receiver with same amount. A sixth-order filter in MCM-D would have too much insertion loss, due to losses in the passives. Therefore, the RF bandpass filter for the receiver is split into two filters, one second-order filter in front of the low noise amplifier (LNA) and a second one after the LNA.

The first design is a second-order bandpass filter with lumped elements. The design actually consists of two parallel LC resonators, which are coupled to each other and to their input and output terminals with capacitors. The inductors must have a high quality factor for the filter to have low loss. The quality factor drops with increasing inductance. On the other hand, the inductor cannot be too small. The LC tank determines the center frequency, which needs to be kept constant (at 5.25 GHz). A smaller inductor implies a smaller capacitor, which in turn is related to the required coupling capacitance. To have a good reproducibility and robustness against process tolerances, this coupling capacitance may not become too low. The values of the LC-tank components are respectively 0.68 nH and 1.17 pF. The

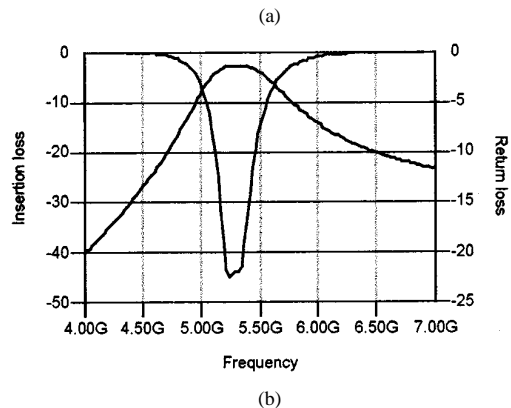
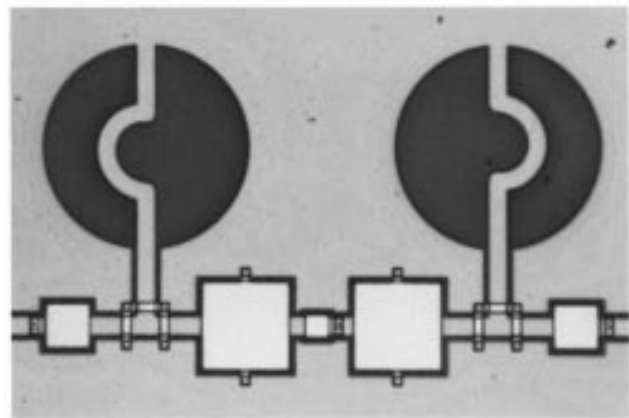
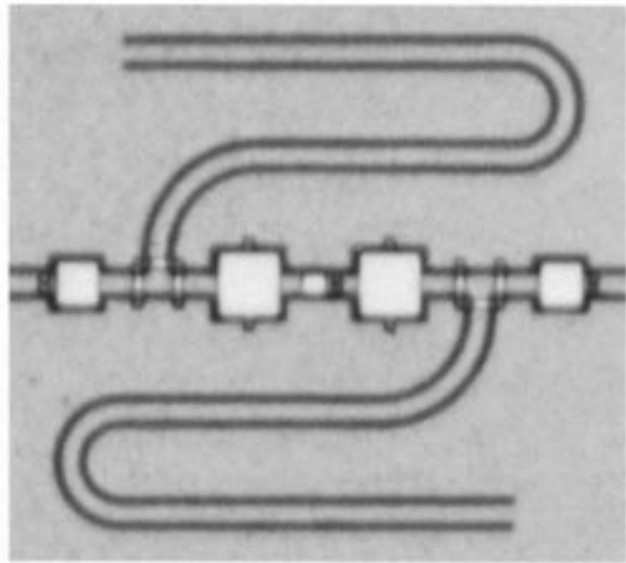


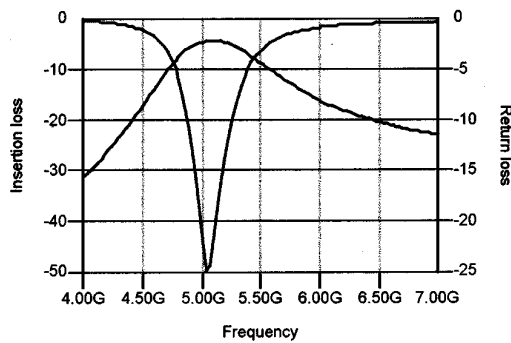
Fig. 4. (a) Microphotograph and (b) measurement data of the second-order, lumped-element bandpass filter, embedded in an MCM-D substrate. Notice the use of a coplanar waveguide approach.

capacitor that couples the two resonators has a value of 46 fF and the input and output coupling capacitances equal 156 fF. A microphotograph of the resulting MCM-D realization is shown in Fig. 4.

The measurements of the filter show an insertion loss of 2.5 dB. The stopband rejection at 500 MHz offset is about 10 dB for the upper side of the spectrum and 15 dB for the lower side of the spectrum. The -1 dB passband extends from 5.150 to 5.475 GHz. The return loss in this frequency band is better than 10 dB. The size of the planar structure is $2.4 \times 1.5 \text{ mm}^2$.



(a)



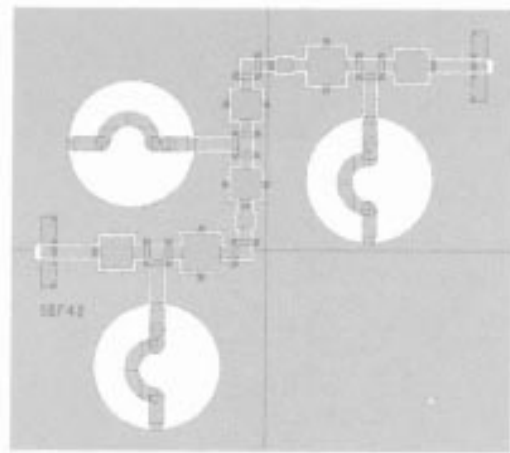
(b)

Fig. 5. (a) Microphotograph and (b) measurement data of the bandpass filter with transmission line stubs.

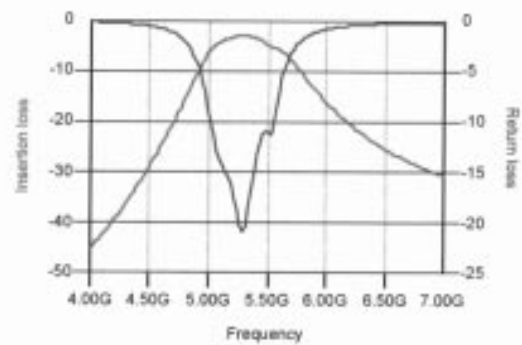
The center frequency has shifted a little bit upward because of process tolerances. The physical reason is a variation in the thickness of BCB layer, which forms the dielectric of the capacitors. This is due to the fact that our MCM-D process flow was not fully optimized yet at the time of production. When the simulation is redone with an adapted value for the changed parameter, the center frequencies of measurement and simulation are again in agreement. The deviation also causes a nonoptimal ratio between the coupling capacitors and the resonating capacitors, which explains a small deviation in the insertion loss. The simulated value was 2.2 dB. It was measured that a 3.5% shift on the center frequency was caused by a 12% shift on component. As the center-frequency is inversely proportional to the square-root of the capacitances, imposing a maximum allowable shift of 50 MHz yields required process tolerances smaller than 3.2%. This indicates that the MCM-D technology will allow us to design these filters without a need for tuning, once the process is frozen and characterized.

Another approach is to use transmission lines instead of inductors, while sticking to lumped capacitors. The design is shown in Fig. 5.

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(a)



(b)

Fig. 6. (a) Layout plot and (b) measurement data of the third-order bandpass filter.

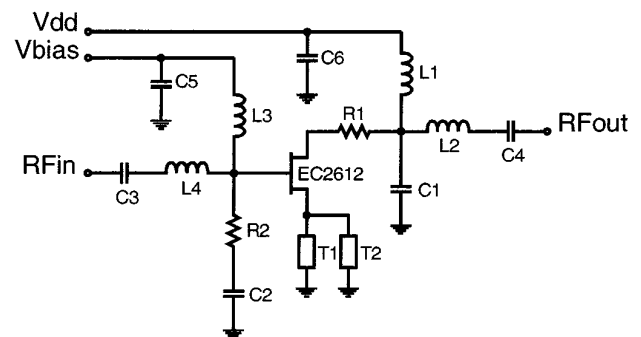


Fig. 7. Schematic of the low noise amplifier with EC2612 transistor.

The filter has an insertion loss of 4.3 dB and a -1 dB bandwidth of 350 MHz, ranging from 4.925 to 5.275 GHz. The return loss at input and output is better than 10 dB in the passband. The frequency shift of this filter is larger, originating from a larger shift of capacitance values, which also explains the bad figure for the insertion loss. The size of the structure is 2.4×2.2 mm².

The performance for these two second-order bandpass filter designs is comparable, taking abstraction from the different shift

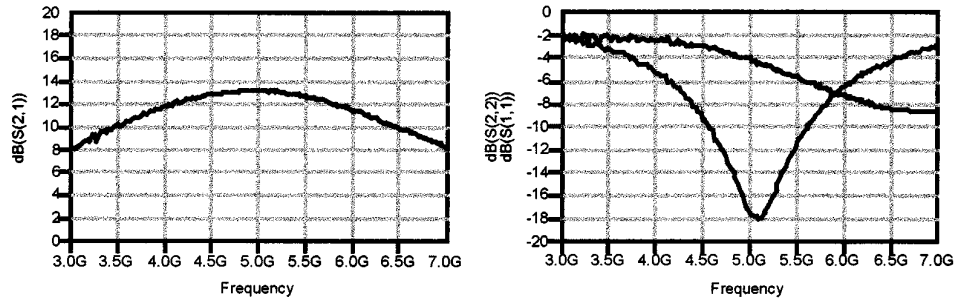


Fig. 8. S -parameter measurements of the LNA separately. S_{21} is the gain in a $50\ \Omega$ environment.

on the capacitors. Both simulations and measurements confirm this. The measured loss of the first filter on the same (off-spec) wafer as the second filter is 3.9 dB. The bandwidth of the second solution is somewhat larger, but the filtering is less steep. The second filter is also larger in size, because transmission line structures are wavelength-related and this wavelength is still rather big at 5 GHz.

Because two of these second-order filters used together do not provide enough out-of-band rejection, a third-order filter is also investigated. The measurement results are depicted in Fig. 6. The structure is similar to the other filters, but an extra section is added. This yields a structure with three capacitively coupled LC-tanks. The measurements show an insertion loss of 3 dB. This is probably too high for an input filter in front of the LNA, but it still can be used after an LNA with enough gain. The $-1\ \text{B}$ bandwidth is 325 MHz, from 5.125 to 5.450 MHz. The return loss is better than 12 dB in the whole band, both at the input and output. The size is $2.8 \times 3\ \text{mm}^2$.

VI. RECEIVER FRONT-END BLOCKS

As suggested in Section III, the presented integration demonstrator contains two bandpass filters, an LNA and a downconversion mixer. The prototype module is intended to demonstrate the concept of SiP. A lot of optimization work on the different blocks, especially on the LNA, is still possible.

All components are matched for $50\ \Omega$, which is not necessarily an optimum, but is often a requirement when using off-the-shelf components or when measurement of the separate functions is mandatory.

The low noise amplifier is built around a GaAs high electron mobility transistor [18] and is shown in Fig. 7.

It consists of a single class A stage. The transistor is available as bare die and is mounted on the MCM-D substrate with the flip-chip technique, explained in Section IV. All the passives are integrated in the MCM.

Inductor L1 (1.9 nH) serves as a load inductor for the amplifier. It is chosen such that the LNAs gain maximum is at 5.25 GHz. R1, R2, C2, and source degeneration in the form of transmission lines T1 and T2 are necessary to stabilize the amplifier. The RC network R2–C2 has a lowpass characteristic to stabilize the circuit at high frequencies. Transmission lines T1 and T2 serve the same stabilization purpose by degenerating the high frequencies. They also improve the linearity. The amplifier is designed to be unconditionally stable, which means that the amplifier is stable for every possible source and load

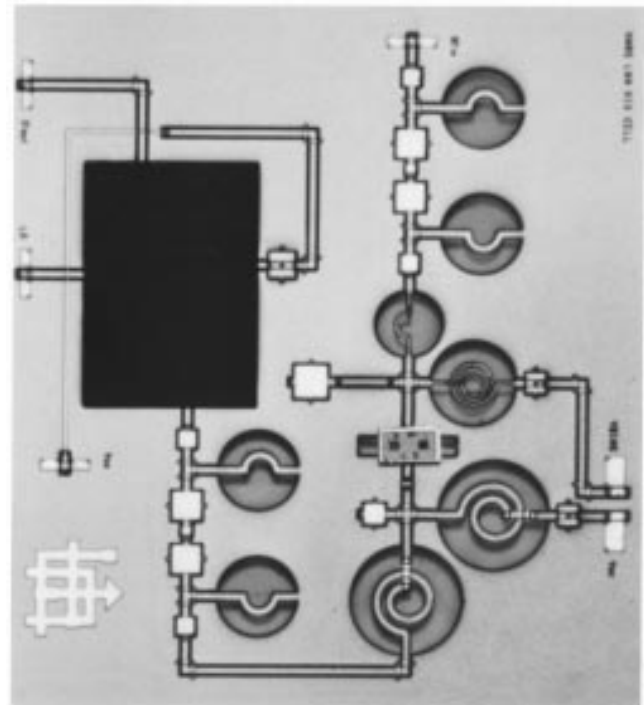


Fig. 9. Microphotograph of the single-package receiver module ($6.5 \times 7\ \text{mm}^2$).

impedance. The considerable measures, which had to be taken to get the design unconditionally stable up to 40 GHz, reduced the performance of the LNA significantly. The transistor was chosen for quick availability in low quantities as bare die component, yielding a component with a large overkill in frequency performance, which makes the instability risks broader. L2 (1.9 nH) and C1 (300 fF) provide impedance matching to $50\ \Omega$ at the output. Their values are determined with classical techniques [19]. L3 (3.4 nH) mainly serves to bias the transistor. L4 (0.6 nH) provides impedance matching for optimal noise performance at the input. Capacitors C5 and C6 are supply-decoupling capacitors, whereas C3 and C4 provide a DC-blocking function. They are omitted when the amplifier is combined with the bandpass filters, since the latter ones inherently provide DC-blocking.

The amplifier consumes 14 mA for a 2 V power supply. Measurements on the LNA separately are shown in Fig. 8: the gain is 12.9 dB and the noise figure is 2.5 dB. The output return loss

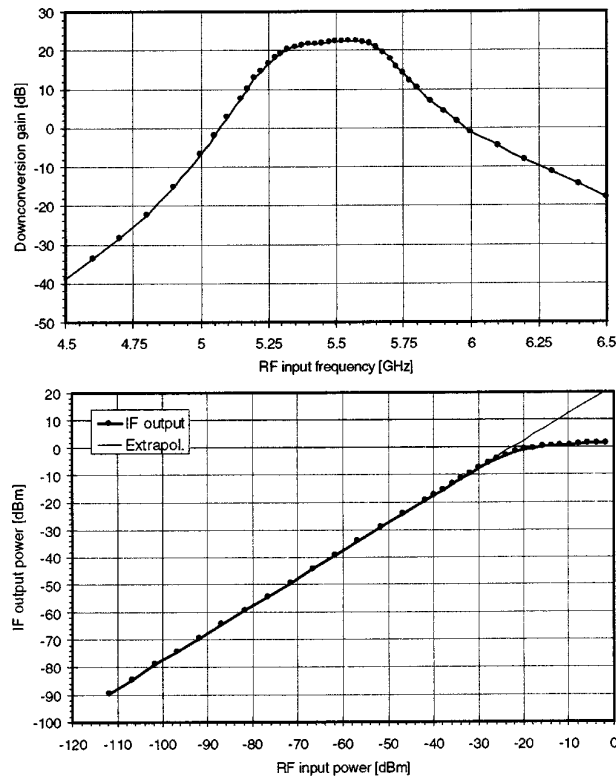


Fig. 10. Measurements on the receiver front-end: (top) downconversion gain, showing a bandpass characteristic, and (bottom) linearity measurement, revealing the compression point.

is better than 14 dB over the whole band. The input is matched for optimal noise performance. The measured 1 dB compression point is -5 dBm at the input.

The downconverter is a GaAs MMIC [20]. The device has a minimum specified gain of 12 dB. It consumes 26 mA at 3.3 V. The two 5-GHz bandpass filters, which filter out neighboring distortions in the frequency spectrum efficiently, were described in Section V. They are located in front of the LNA and between the LNA and downconverter.

A microphotograph of the receiver front-end is shown in Fig. 9. The whole structure measures 6.5 mm by 7 mm.

The complete receiver has a measured conversion gain of 22 dB and a noise figure of 7.5 dB. The measured 1 dB compression point is -3.6 dBm, referenced to the output. It is limited by the mixer. The passband extends from 5.4 to 5.65 GHz. The measured transfer for a swept RF input frequency and fixed-IF operation is shown in Fig. 10.

VII. CONCLUSION

In this paper, we have shown that SiP has benefits over single-chip solutions. Single-chip solutions do not provide a complete system integration. A single package approach with an MCM-D technology is a more complete solution that is compact and that is more flexible than a single-chip approach.

Furthermore we have demonstrated that high-quality passive components can be embedded on an MCM-D substrate. These passives can be used together with mounted active components as well as for the design of integrated RF bandpass filters and

matching networks. We have built prototype SiP-integrated RF module of a receiver front-end with commercial bare-die components to demonstrate this concept. This receiver has a measured gain of 22 dB and a total noise figure of 7.5 dB, making it suitable to serve as a part of a 5 GHz Wireless LAN system.

In a second step, we will further develop the receiver front-end by combining the MCM-D passives with custom designed ICs for the active circuitry, preferably in silicon, due to its lower cost compared to GaAs [8], [11]. We can then do real chip-package co-design by making a good trade-off between on-chip realization or embedding in the MCM. A single-package approach is neither limited to one certain technology, nor to the availability or limits of commercial components, thus creating more degrees of freedom for design.

Also the antenna is a candidate for future integration in the MCM-D module. It has been shown that this is possible [21].

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