

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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KANGXI COMMUNICATION TECHNOLOGIES (SHANGHAI) CO., LTD.  
Petitioner,

v.

SKYWORKS SOLUTIONS, INC.,  
Patent Owner.

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U.S. Patent 8,717,101

Title: APPARATUS AND METHODS FOR BIASING POWER AMPLIFIERS

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*Inter Partes* Review No.: 2025-00373

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**DECLARATION OF DAVID RICKETTS, PH.D. IN SUPPORT OF**  
**PETITIONS FOR INTER PARTES REVIEW OF**  
**U.S. PATENT NO. 8,717,101**

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I, David Ricketts, declare as follows:

## **I. INTRODUCTION**

1. I am over the age of eighteen (18) and otherwise competent to make this Declaration.

2. I have been retained by Kangxi Communication Technologies (Shangahi) Co., Ltd. (Petitioner) as an independent, technical expert consultant in this proceeding before the United States Patent and Trademark Office (USPTO). I am being compensated at my rate of \$725 per hour for my services. No part of my compensation is dependent on my opinions or on the outcome of this proceeding. I have no financial interest in any of the parties to this proceeding.

3. This Declaration is in support of the Petition for *inter partes* review involving U.S. Patent 8,717,101 (EX-1001), entitled “Apparatus and Methods for Biasing Power Amplifiers” and listing Ping Li and Paul T. DiCarlo as the inventors.

4. For the purposes of this *inter partes* review as I discuss later, I have been instructed to assume that the effective filing date of the Claims of the ’101 Patent challenged by the Petitioner in *inter partes* reviews is no earlier than May 13, 2011.

5. I understand that, according to USPTO records, the '101 Patent are currently assigned to Skyworks Solutions, Inc. ("Patent Owner"). I assume for purposes of this proceeding that Skyworks Solutions, Inc. is the patent owner.

6. The '101 Patent is generally directed to a power amplifiers and biasing circuits to correct for a variation in gain of a power amplifier. I am familiar with the technology described in the '101 Patent as of the earliest possible priority date of May 13, 2011, the filing date of Provisional Application No. 61/486,186.

7. In preparing this Declaration, I have reviewed the '101 Patent (EX-1001) its prosecution history (EX-1002), as well as the patents and documents cited herein, and I have considered these documents in light of the general knowledge in the art as of May 13, 2011. In formulating my opinions, I have relied upon my experience in the relevant art. I have also considered the viewpoint of a person of ordinary skill in the art ("POSITA") in the relevant field, as of May 13, 2011, who I describe below (§ V.D). For convenience, the materials I considered in arriving at my opinions are listed in Appendix A.

8. I have been asked to provide my technical expertise, analysis, insights and opinions regarding the '101 Patent and relevant references that form the basis of the arguments set forth in the accompanying Petition for *inter partes* review of the '101 Patent. As described in detail below, I offer the following opinions in this Declaration:

9. In my opinion, based on my experience, knowledge and consideration of a POSITA, and in view of the evidence I discuss herein, a POSITA would have found Claims 1-2, 10-11, 17-18, and 20-22 of the '101 Patent to be obvious over *Ishimaru* alone (Ground 1 below) or in view of *Harrison* (Ground 2 below) and a POSITA would have been motivated to combine the teachings of these references.

10. Unless otherwise indicated, the emphasis in quotations has been added.

## **II. QUALIFICATIONS**

11. My qualifications for forming the opinions set forth in this declaration are summarized here and explained in more detail in my *curriculum vitae*, which is included as Appendix B. Appendix B also includes a list of my publications and patents.

12. I am currently Full Professor of Electrical and Computer Engineering at the North Carolina State University. In my position I conduct research and teach undergraduate and graduate students in the area of electrical and computer engineering. The courses I teach include Advanced Analog Integrated Circuit (“IC”) Design, Radio System Design, Analog Circuit Laboratory and Power Management IC Design. I also lead a research group that conducts research and design of electrical and electronic circuits, including millimeter wave and microwave circuits and systems, wireless power transfer circuits, power electronics

and nano-electronic and nano-photonic devices. I lead research in power electronics and power conversion integrated circuits. I have served in my current position since 2012.

13. I have collaborated with numerous industries in power electronics, wireless power, radio frequency circuits and others. During this time, I worked with engineers of varying experience, including those with 2-20 years, including engineers with 5 years of experience.

14. Prior to my current position, I served as an Assistant Professor of Electrical and Computer Engineering and held a courtesy appointment in the Materials Science Department at Carnegie Mellon University from 2006 to 2012. I taught undergraduate and graduate device physics, which included photovoltaic devices.

15. I received my B.S. and M.S. in Electrical Engineering in 1995 and 1997, respectively, from Worcester Polytechnic Institute in Worcester, Massachusetts. I received my Ph.D. in Electrical Engineering from Harvard University in Cambridge, Massachusetts in 2006.

16. Prior to entering academia, I worked as an engineer in private industry holding several engineering and managerial positions where I developed and oversaw the development of electrical and electronic circuits, including those

related to power transfer, power conversion, and semiconductor design in wired and wireless circuits and systems.

17. From 1995 to 1999, I held a position as an engineer and senior engineer at American Power Conversion, where I designed uninterruptable power supplies (UPS), AC-DC and DC-DC converters. The AC-DC converters were originally developed for solar power grids to convert DC power from solar panels to AC energy to power homes. The technology also included methods to transfer energy from the solar panels directly to the grid, as well as microgrid, at home solar installations and voltage and current inverters. In addition, I worked on AC-DC and DC-DC converters as well as battery chargers.

18. From 1999 to 2001, I held a position as a Principal Consultant at Renaissance Design, Inc., where I designed power management ICs for DC-DC converters and DC-AC inverters.

19. From 2000 to 2002, I held a position as a Manager of New Product Development at ON Semiconductor Corp., where I was responsible for six product development teams including market analysis, business development, system design, integrated circuit design and testing. In that role I oversaw the development of over twenty power management ICs, also known as power ASICs, in bipolar, CMOS, and BiCMOS technologies. These ICs related to DC-DC converters among other power electronic circuits.

20. From 2002 to 2003, I held the position of Advanced System Engineering Manager at ON Semiconductor Corp., where I directed a team of system engineers to develop multi-phase power management ICs for Intel and AMD microprocessors.

21. In 2006 I received my PhD on the topic of advanced oscillator topologies and radio frequency integrated circuits. My work on integrated circuit oscillators was included in the 2008 McGraw-Hill Yearbook of Science and Technology and discussed in Nature, the pre-eminent science journal. In addition, my work on advanced materials for circuits included the first Si-Ge shell-core nanowire oscillator on plastic.

22. Since 2006, I have conducted research at the forefront of radio frequency power amplifier design. I have published numerous journal and conference papers on power amplifiers, with multiple designs being the best reported in the world at the date of publication. I have experience in design and testing of power amplifiers in various technologies, such as Silicon Germanium, complementary metal oxide semiconductor (CMOS), Silicon on Insulator, etc.

23. I have published two books, at least 50 academic journal papers and 78 conference papers, as shown in my curriculum vitae, in RF systems, wireless power transfer circuits, magnetic circuits and materials, analog circuits, RF circuits and nanoscale devices.

24. I am the recipient of the National Science Foundation CAREER award for work in emerging magnetic devices known as spin-torque oscillators. I also received the Defense Advanced Research Projects Young Faculty Award for my work in emerging magnetic devices.

25. Based on my above-described over three decades of experience in semiconductors and of radio frequency power amplifier design, and the acceptance of my publications and professional recognition by societies in my field, I believe that I am qualified to be an expert in the field of radio frequency electronics.

26. Based on my experience described above, and as indicated in my *curriculum vitae*, I am qualified to provide the following opinions with respect to the patents in this case. Additionally, I am at least a person having ordinary skill in the art as of the priority date of the '101 Patent.

### **III. RELEVANT LEGAL STANDARDS**

27. I do not provide any legal opinions in this Declaration. I have been informed and understand that certain legal standards are to be applied by technical experts in forming opinions regarding the meaning and validity of patent claims. I have been asked to provide my opinions regarding whether the claims of the '101 Patent would have been obvious to a person having ordinary skill in the art at the time of the alleged invention, in light of the prior art.

28. Further, I have been informed and understand that a patent claim is not patentable as obvious (a requirement I understand to be governed by a statute, 35 U.S.C. § 103) if the differences between the patent claim and the prior art are such that the claimed subject matter as a whole would have been obvious at the time the claimed invention was made to a person having ordinary skill in the relevant art. Obviousness, as I have been informed and understand, is based on the scope and content of the prior art, the differences between the prior art and the claim, the level of ordinary skill in the art, and, to the extent that they exist, certain objective indicia of non-obviousness.

29. I understand that objective indicia can be important evidence regarding whether a patent is obvious or nonobvious, if it has an appropriate nexus to the claimed invention, i.e., is a result of the merits of a claimed invention (rather than the result of design needs or market-pressure advertising or similar activities). Such indicia include: commercial success of products covered by the patent claims; a long-felt need for the invention; failed attempts by others to make the invention; copying of the invention by others in the field; unexpected results achieved by the invention as compared to the closest prior art; praise of the invention by the infringer or others in the field; the taking of licenses under the patent by others; expressions of surprise by experts and those skilled in the art at the making of the

invention; the patentee proceeded contrary to the accepted wisdom of the prior art, and, the contemporaneous development of the subject matter claimed by others.

30. I have been informed that whether there are any relevant differences between the prior art and the claimed invention is to be analyzed from the view of a person of ordinary skill in the relevant art at the time of the invention. As such, my opinions below as to a person of ordinary skill in the art are as of the time of the invention, even if not expressly stated as such; for example, even if stated in the present tense.

31. In analyzing the relevance of the differences between the claimed invention and the prior art, I have been informed that I must consider the impact, if any, of such differences on the obviousness or non-obviousness of the invention as a whole, not merely some portion of it. The person of ordinary skill faced with a problem is able to apply his or her experience and ability to solve the problem and also look to any available prior art to help solve the problem.

32. I have been informed that a precise teaching in the prior art directed to the subject matter of the claimed invention is not needed. I have been informed that one may take into account the inferences and creative steps that a person of ordinary skill in the art would have employed in reviewing the prior art at the time of the invention. For example, if the claimed invention combined elements known in the prior art and the combination yielded results that were predictable to a

person of ordinary skill in the art at the time of the invention, then this evidence would make it more likely that the claim was obvious. On the other hand, if the combination of known elements yielded unexpected or unpredictable results, or if the prior art teaches away from combining the known elements, then this evidence would make it more likely that the claim that successfully combined those elements was not obvious.

33. I have been informed and understand that there are recognized, exemplary, rationales for combining or modifying references to show obviousness of claimed subject matter. Some of the rationales include the following: combining prior art elements according to known methods to yield predictable results; simple substitution of one known element for another to yield predictable results; use of a known technique to improve a similar device (method or product) in the same way; applying a known technique to a known device (method or product) ready for improvement to yield predictable results; choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success; known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations are predictable to one of ordinary skill in the art; and some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill

to modify the prior art reference or to combine prior art teachings to arrive at the claimed invention.

#### IV. OVERVIEW

34. In my opinion, the Challenged Claims are obvious over the prior art. The '101 Patent is directed to a power amplifier ("PA") and biasing circuit that addresses the problem of PA gain variation at startup, *i.e.*, gain variation during the time period between when the PA is enabled (turned on) and when it reaches steady state operation. Thermal effects at startup that can cause the amplifier's gain to be lower than its steady-state gain until the circuitry heats up. This startup/warm-up phenomenon was known in the art at the time of the invention. The '101 Patent's proposed solution was to provide a current boost to the PA bias current to correct for variation of gain when the PA is activated/enabled, *i.e.*, during startup. EX-1001 4:28-43, 9:56-60; *see, e.g.*:

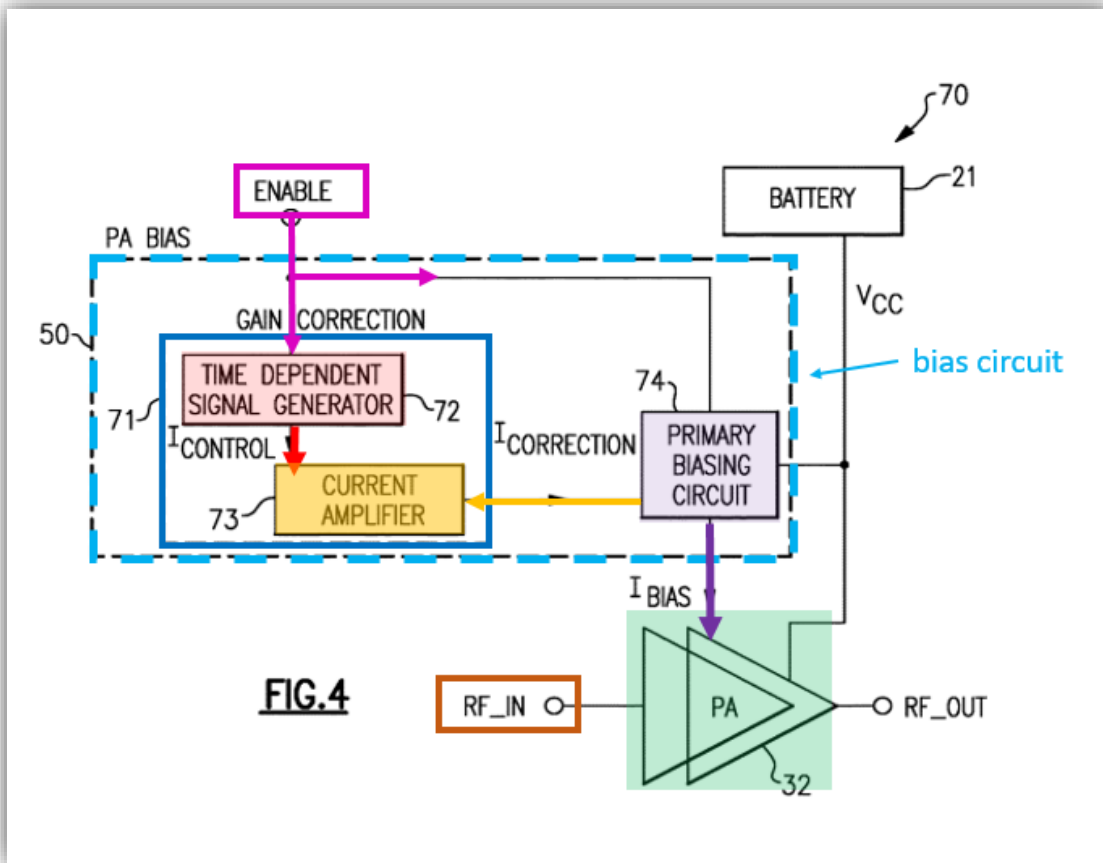
The correction current can be used to adjust the magnitude of the bias current so as to compensate for a variation in gain of the power amplifier over time when the power amplifier is transitioned from a disabled state to an enabled state. **For example, shortly after a power amplifier is enabled, absent compensation the current of a primary biasing circuit can come up slow due to thermal effects, and the power amplifier's gain can be low.** By including the time-dependent signal generator and the current amplifier, **a current boost can be provided to the power amplifier** so as to provide the power amplifier with a **substantially flat gain response versus time**. Correcting for

gain variation in the power amplifier can improve the power amplifier's performance, including, for example, the power amplifier's dynamic error vector magnitude (EVM).

EX-1001 4:28-43.

For example, shortly after the power amplifier 32 is enabled, absent compensation the current of the primary biasing circuit 74 can come up slow due to thermal effects, and the gain of the power amplifier 32 can be low.

EX-1001 9:56-60. Figure 4 of the '101 Patent illustrates a PA bias block that produces a bias current ( $I_{BIAS}$ ) (purple arrow) to the PA (green) including a current boost at startup:



EX-1001 Fig. 4 (Annotated).

35. The '101 Patent's enable signal (pink arrow) is activated at startup, causing a time-dependent signal generator (red) to generate a control current ( $I_{CONTROL}$ ) (red arrow) that is received by a current amplifier (gold) implemented as a current mirror. The current mirror replicates (*i.e.* mirrors) and amplifies the

$I_{CONTROL}$  (red arrow) to form the correction current ( $I_{CORRECTION}$ ) (gold arrow), which is pulled<sup>1</sup> from a primary biasing circuit (purple).

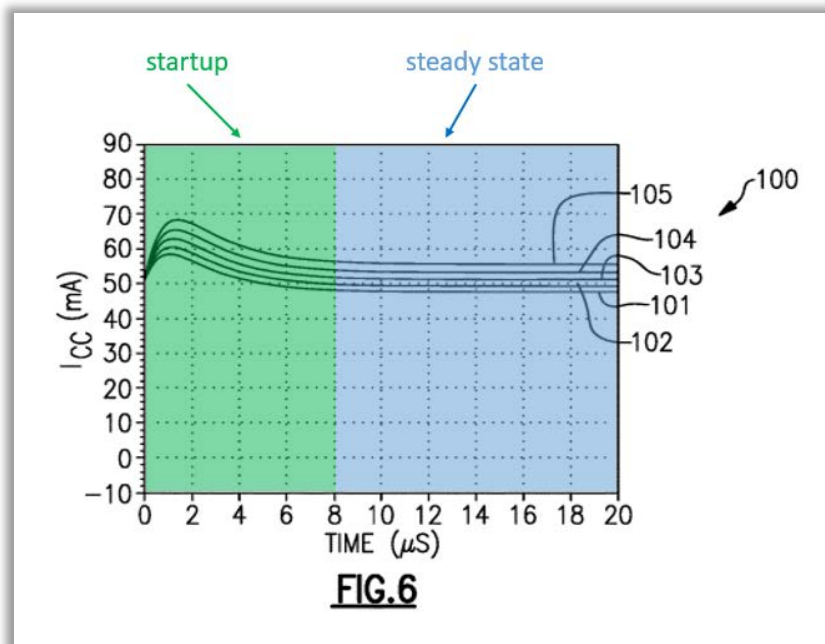
36. The '101 Patent's time-dependent signal generator and amplifier / current mirror together form a gain correction circuit (dark blue). The  $I_{CONTROL}$  (red arrow) and  $I_{CORRECTION}$  (gold arrow) are shaped to temporarily adjust current in the PA's primary biasing circuit (purple) in an amount and duration necessary to cause the primary biasing circuit to provide a corresponding temporary boost in  $I_{BIAS}$  to boost the PA's gain at startup, compensating for gain variations when the PA is enabled. The amount and duration of the  $I_{CORRECTION}$  is thus configured to

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<sup>1 1</sup> Although Figure 4 has an arrowhead suggesting that  $I_{CORRECTION}$  flows into the primary biasing circuit in some embodiments, that figure is directed to a generic current amplifier. All of the Challenged Claims, however, are directed to the embodiment where the amplifier includes, or is implemented as, a "current mirror." EX-1001 Fig. 5 (mirror 83), 10:23, 11:36-38; see §IV.F.2 (discussing current mirrors). In the current mirror disclosure,  $I_{CORRECTION}$  is pulled from the primary biasing circuit as shown in Figure 5. This ability to pull current in a desired amount is a conventional use of a current mirror. See §IV.F.2. Given that all of the Challenged Claims are directed to current mirror embodiments, we annotate the direction of  $I_{CORRECTION}$  in Figure 4 using the direction shown in Figure 5.

counteract and compensate for the thermal startup characteristics of a given PA, *i.e.*, the PA's gain over time absent compensation.

37. The resulting short “boost” in  $I_{BIAS}$  to the PA overcomes its low gain at startup, thereby reaching steady state sooner and providing a flatter gain response versus time, as illustrated by Fig. 6 of the '101 Patent:



EX-1001 Fig. 6 (annotated).

38. However, the use of biasing circuitry to generate a boost current to correct for low gain when a PA is enabled (*i.e.* at startup) was known in the prior art. For example, *Ishimaru* discloses a nearly identical architecture for a PA bias circuit that addresses the same PA gain variation arising from thermal effects at startup. EX-1004 ¶¶52-54; *see, e.g.*:

In the speedup circuit 122, with electric charge flowing into the capacitance element 121 at a rise time of the control voltage of the control voltage source 135 (at turn-on of the amplifier), a current transiently (temporarily) flows from the output terminal 118 into the fifth transistor 119, causing the voltage value of the output terminal 118 to lower. As a result, due to a change of the bias point of the third transistor 115, the voltage of a connecting terminal 117, which connects the collector of the third transistor 115 to the base of the bias transistor 107, transiently increases. Thus, at the rise time, the current fed to the amplifier transistor 103 by the bias transistor 107 transiently increases. Therefore, at the rise time, the power amplification factor of the amplifier transistor 103 transiently increases, so that the time elapsing until temperature variations due to heat generation of the amplifier transistor 103 come to an equilibrium on the whole circuit is shortened, with a result of reduced distortion

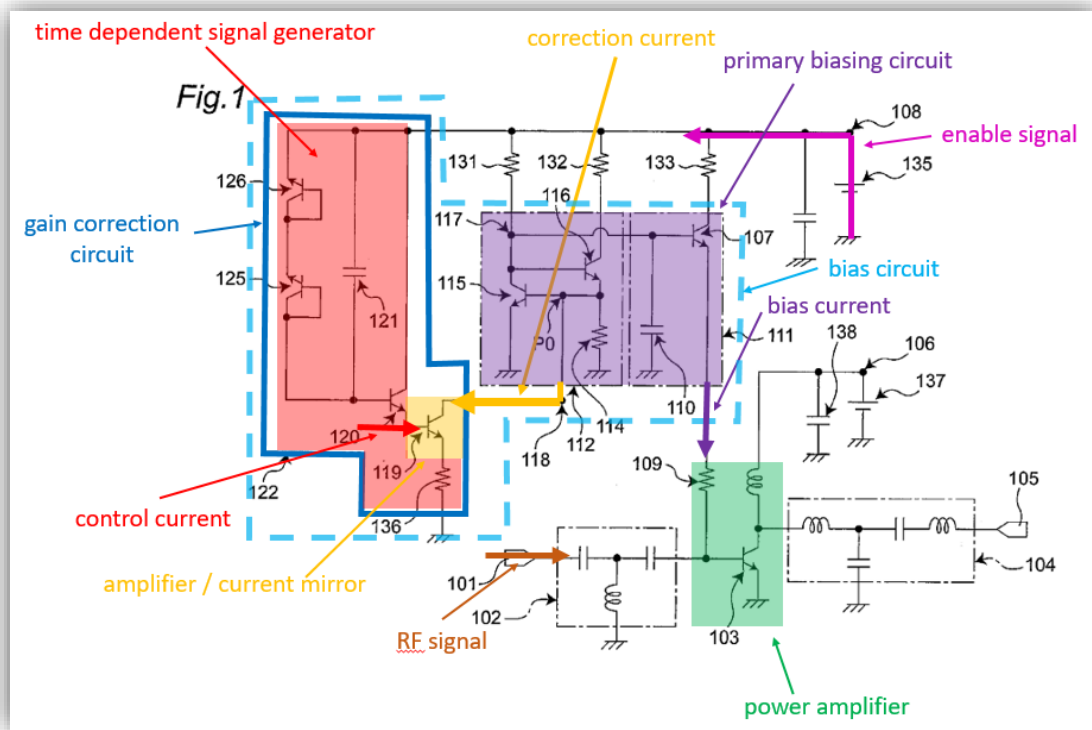
EX-1004 ¶52.

FIG. 2 shows an example of transient response of an operating current (collector current  $I_{c3}$ ) of the amplifier transistor 103 in a comparative example in which the speedup circuit 122 is removed in the circuit of FIG. 1. In this comparative example having no speedup circuit, due to the fact that a temperature increasing rate of the bias transistor 107 is slower than that of the amplifier transistor 103, the value of the current fed from the bias circuit 111 to the amplifier transistor 103 continues to vary, the variations in current value making a cause of signal distortion.

EX-1004 ¶53.

Next, FIG. 3 shows an example (simulation result) of transient response of the operating current (collector current  $I_{c3}$ ) of the amplifier transistor 103 in the power amplifier of this embodiment. In this embodiment, the current to be fed from the bias transistor 107 to the amplifier transistor 103 is forcibly increased at turn-on of the amplifier, with the result that the value of the operating current  $I_{c3}$  comes to a steady state in about 1/4 the time of transient response of the comparative example of FIG. 2. Thus, occurrence of distortions of the amplification signal due to temperature variations in the amplifier circuit is suppressed, so that the linearity of the circuit in burst operation is improved. That is, gain variations due to collector current variations of the power amplifier using a bipolar transistor can be compensated.

EX-1004 ¶54. *Ishimaru's* architecture is illustrated below (elements in common with the '101 Patent annotated in a common color):



EX-1004 Fig. 1 (annotated).

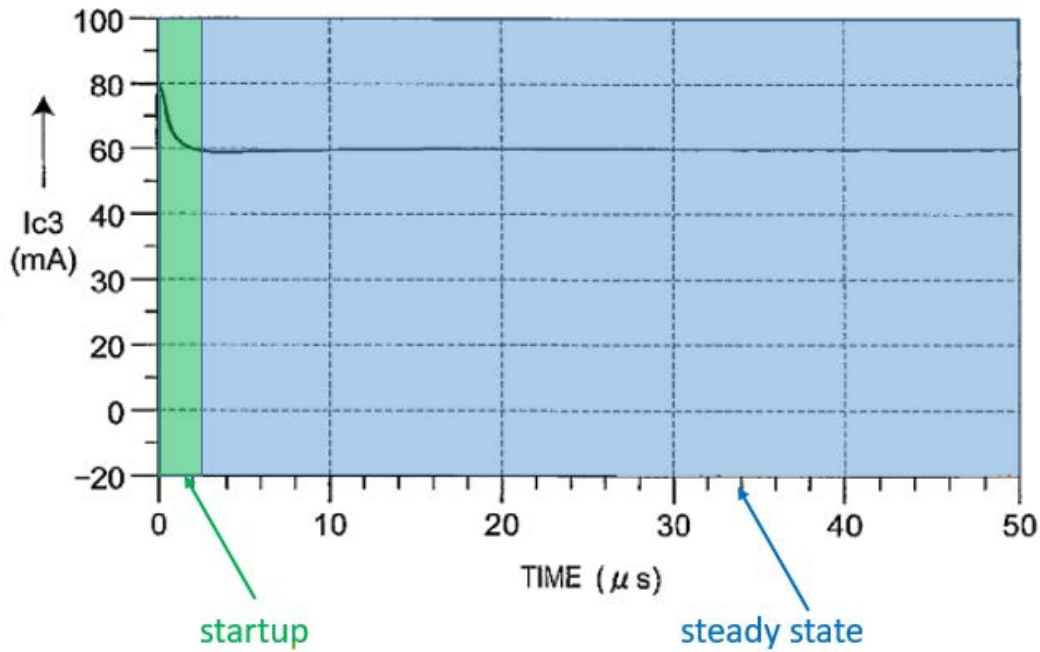
39. *Ishimaru's* enable signal (pink arrow) is activated at startup, causing a time-dependent signal generator (red) to generate a shaped control current ( $I_{CONTROL}$ ) (red arrow) that is received by a current amplifier (gold) implemented as a current mirror. The current mirror replicates (*i.e.* mirrors) and amplifies  $I_{CONTROL}$  (red arrow) to form a correction current ( $I_{CORRECTION}$ ) current (gold arrow), which is pulled from a primary biasing circuit (purple).

40. *Ishimaru's* time-dependent signal generator and amplifier/current mirror together form a gain correction circuit (dark blue), which *Ishimaru* calls a “speedup circuit.” The speedup circuit (dark blue) is a gain correction circuit in

that it is a circuit that generates  $I_{CONTROL}$  and  $I_{CORRECTION}$  (gold arrow) shaped for the purpose of correcting for the low gain of the PA (green) at startup. The  $I_{CONTROL}$  and  $I_{CORRECTION}$  (gold arrow) are shaped to temporarily pull current out of the PA's primary biasing circuit (purple) in an amount and duration necessary to cause the primary biasing circuit to provide a corresponding temporary boost in bias current ( $I_{BIAS}$ ) to the PA (green) to boost its gain during the startup period when its gain would otherwise be too low. The  $I_{CORRECTION}$  is thus configured to compensate for the thermal startup characteristics of a given PA, *i.e.*, the PA's gain over time absent compensation.

41. The resulting short “boost” in  $I_{BIAS}$  is provided to the PA to overcome its low gain at startup, thereby reaching steady state sooner and providing a flatter gain response versus time, as illustrated in Figure 3 of *Ishimaru*:

*Fig.3*



EX-1004 Fig. 3 (annotated).

42. Thus, *Ishimaru* is a parallel disclosure to the '101 Patent in that *Ishimaru* is directed to the same problem and proposes the same solution, but uses slightly different words to describe the same concepts.

43. In my opinion, based on my experience, knowledge, and consideration of a POSITA as described in Ground 1, the Challenged Claims are obvious over *Ishimaru*.

44. Ground 2 is provided to the extent that the Patent Owner asserts that the *current mirror* term of the Challenged Claims requires importing additional limitations from the specification, in which case the *Harrison* reference discloses these additional limitations.

## V. BACKGROUND

### A. Overview of the '101 Patent

45. The '101 Patent explains that “[t]here is a need for improving power amplifier biasing.” EX-1001 1:31-33. Biasing is the application of a suitable DC voltage or current (typically a DC offset applied to the base terminal of a transistor) to set or place the constituent PA transistor in an “on” state at a particular operating point so that it is ready to undertake AC signal amplification. EX-1023 141. Bias conditions of a PA can be thought of as “idling conditions” in that they are established when there is no AC signal at the input of the transistor, *i.e.* the conditions present when idling. EX-1024 218, 220-228; *see, e.g.:*

Transistor circuits are usually designed to amplify an ac input voltage rather than dc current. In this type of arrangement, the ac is superimposed on the dc. The dc is used to establish specific quiescent emitter and collector currents. These *bias currents* should set the idling voltage (voltage before ac is applied to the circuit) at the collector at one-half of  $E_{CC}$ . Because the collector voltage,  $V_C$ , is equal to  $E_{CC} - I_C R_C$ ,  $V_C$  should be idling at about  $E_{CC}/2$ .

EX-1024 218

Bias or idling conditions are established when there is no ac voltage at the input of the circuit, or  $E_{IN} = 0$ . At this time, only the dc emitter supply voltage less the base-emitter voltage is across  $R_C$  the only component in this circuit that is outside of the transistor.

EX-1024 220. The '101 Patent is directed to the problem that “shortly after a power amplifier is enabled, absent compensation, the current of a primary biasing circuit can come up slow due to thermal effects, and the power amplifier’s gain can be low.”

EX-1001 4:32-35.

46. The specification purports to solve that problem by providing “a current boost ... to the power amplifier [bias signal] so as to provide the power amplifier with a substantially flat gain response versus time.” EX-1001 4:28-40. Specifically, the specification describes “a power amplifier and a power amplifier bias block” where the bias block receives “an enable signal” to turn the PA on. *Id.* The bias block includes a “primary biasing circuit” and a “gain correction block”, which includes a “time-dependent signal generator” and “current amplifier.” The “time-dependent signal generator” shapes the enable signal to generate  $I_{CONTROL}$ , which is amplified to generate  $I_{CORRECTION}$ . The primary biasing circuit generates  $I_{BIAS}$  for the PA using  $I_{CORRECTION}$ .  $I_{CORRECTION}$  is used to adjust  $I_{BIAS}$  to compensate for a variation in gain of the PA over time when the PA is “transitioned from a disabled state to an enabled state.” Specifically,  $I_{BIAS}$  is temporarily “boosted” to overcome the PA’s “low” gain at startup, providing the PA “with a substantially flat gain response versus time.” *Id.* 4:10-39; *see, e.g.:*

Apparatus and methods for biasing power amplifiers are disclosed herein. In certain implementations, a power amplifier and a power amplifier bias block are provided. The power amplifier can be used to

amplify a radio frequency (RF) signal for transmission, and the power amplifier bias block can be used to bias the power amplifier. The power amplifier bias block can receive an enable signal that can be used to enable or disable the power amplifier so as to pulse the power amplifier's output.

In certain implementations, the power amplifier bias block includes a primary biasing circuit and a gain correction block including a time-dependent signal generator and a current amplifier. The time-dependent signal generator or control block can be used to shape the enable signal so as to generate a control current, which can be amplified by the current amplifier to generate a correction current. The power amplifier bias block can generate a bias current for the power amplifier using the primary biasing circuit and the correction current. The correction current can be used to adjust the magnitude of the bias current so as to compensate for a variation in gain of the power amplifier over time when the power amplifier is transitioned from a disabled state to an enabled state. For example, shortly after a power amplifier is enabled, absent compensation the current of a primary biasing circuit can come up slow due to thermal effects, and the power amplifier's gain can be low. By including the time dependent signal generator and the current amplifier, a current boost can be provided to the power amplifier so as to provide the power amplifier with a substantially flat gain response versus time.

*Id.* 4:10-39.

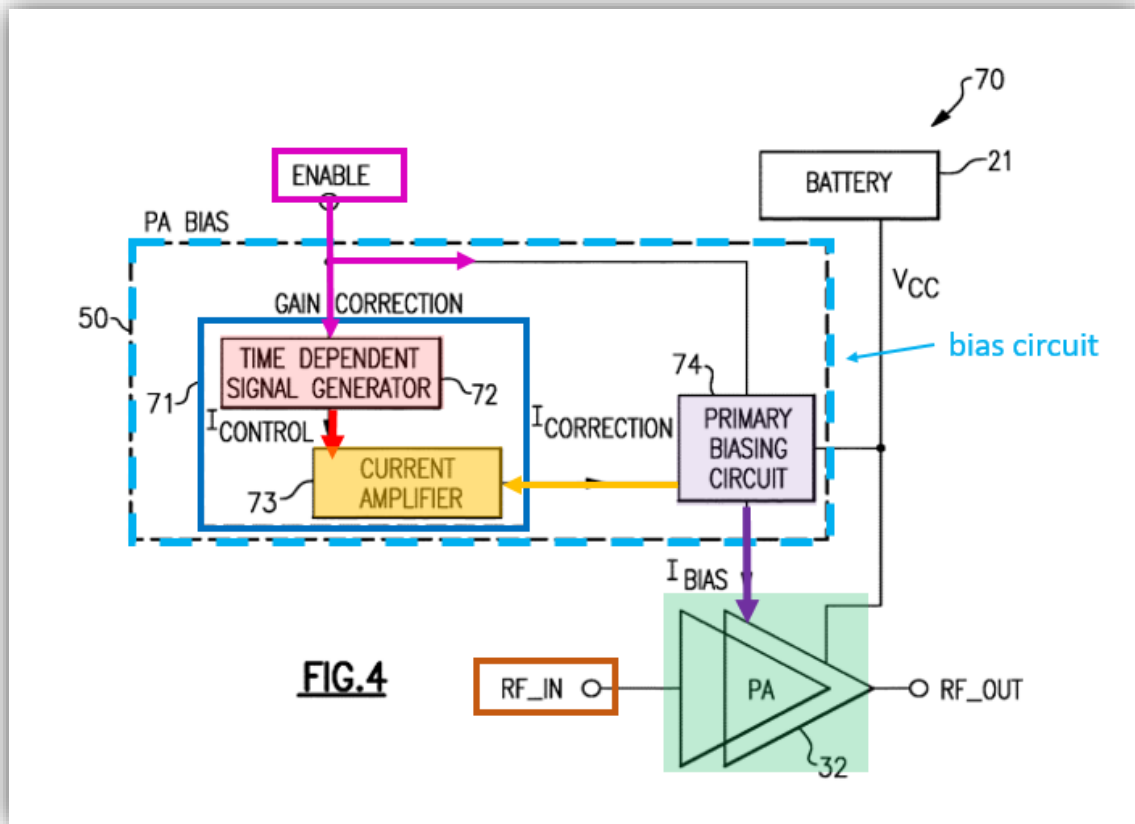
47. Figure 4 (below) illustrates the PA system with a PA bias block 50, battery 21, and PA 32 (green). EX-1001 8:64-9:1; *see, e.g.:*

FIG. 4 is a schematic block diagram of one example of a power amplifier system 70 including a power amplifier bias block 50 according to one embodiment. The illustrated power amplifier system 70 includes the power amplifier bias block 50, the battery 21, and the power amplifier 32.

EX-1001 8:64-9:1. The PA bias block includes both a gain correction block 71 (dark blue) and a primary biasing circuit 74 (purple). When the ENABLE signal is on, the bias block provides  $I_{BIAS}$  to the base of a bipolar transistor of PA 32. *Id.* 9:13-22; *see, e.g.:*

The power amplifier bias block 50 includes a gain correction block 71 and a primary biasing circuit 74. The gain correction block 71 includes a time-dependent signal generator or control block 72 and a current amplifier 73. The power amplifier bias block 50 can receive an enable signal ENABLE, and use the enable signal ENABLE to generate a bias current  $I_{BIAS}$  using charge stored on the battery 21. The bias current  $I_{BIAS}$  can be provided to, for example, a base of a bipolar transistor of the power amplifier 32, as was described earlier.

*Id.* 9:13-22.



Id. Fig. 4 (annotated).

48. The “bias circuit” (light blue) consists of a conventional “primary bias circuit” 74 (purple) driven by a conventional, unmodified “enable signal” (purple), plus a supplemental “gain correction circuit” (dark blue) that generates the supplemental  $I_{CORRECTION}$  to shape the  $I_{BIAS}$  that emerges from the primary bias circuit. The “time-dependent signal generator” (red) produces a small current signal  $I_{CONTROL}$  that varies in time with a desired shape and then the current amplifier (gold) scales up (*i.e.* amplifies) that shaped signal to an appropriate amplitude, creating  $I_{CORRECTION}$ . The current amplifier replicates (*i.e.* mirrors) and

amplifies  $I_{CONTROL}$  (red arrow) to form  $I_{CORRECTION}$  (gold arrow), which is pulled from the primary biasing circuit (purple). This replication of current is referred to as a “current mirror” as discussed in the State of the Art section. EX-1001 10:62-11:45, Figs 4-5; *see also* §IV.F.2; *see, e.g.*:

To aid in reducing the area of the RC network 82, **the current mirror 83 can be used to amplify the control current  $I_{CONTROL}$  to generate the correction current  $I_{CORRECTION}$ .** Thus, the amplifier 83 can be used to obtain a correction current  $I_{CORRECTION}$  of a suitable magnitude, while reducing the size of the components of the RC network 82 relative to a scheme omitting a current amplifier. By amplifying the control current  $I_{CONTROL}$  in this manner, the power amplifier bias block 80 can be integrated on-chip with a power amplifier without having to use a relatively large resistor, which may not provide enough current variation to provide suitable gain compensation.

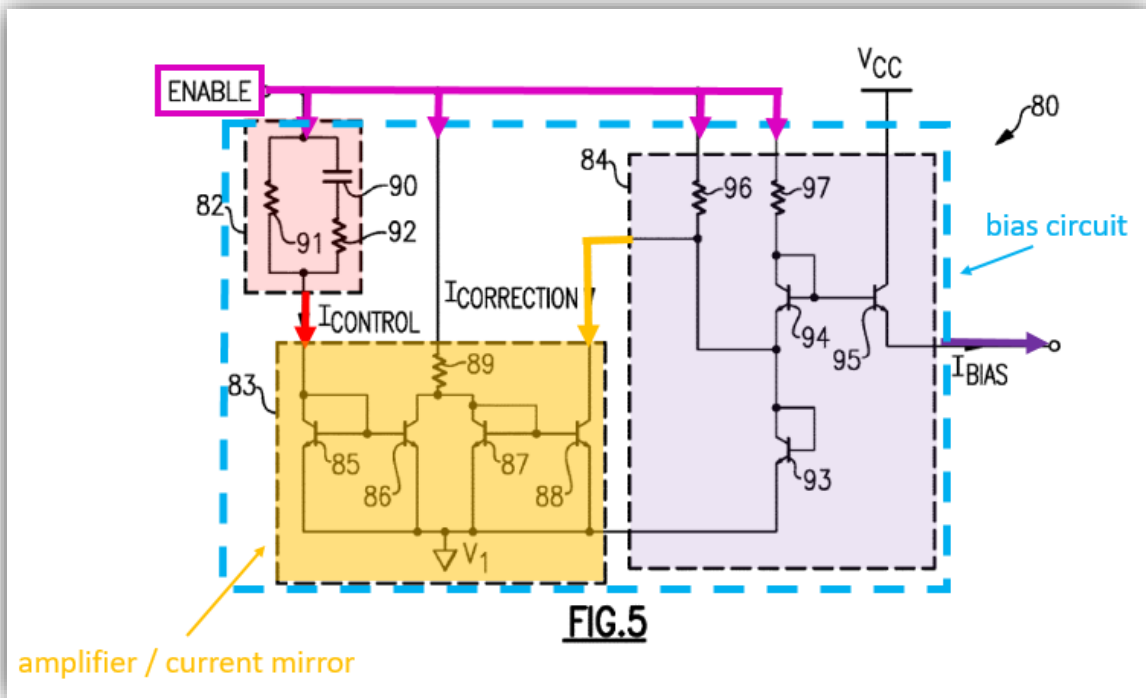
The illustrated current mirror 83 includes a first NPN bipolar transistor 85, a second NPN bipolar transistor 86, a third NPN bipolar transistor 87, a fourth NPN bipolar transistor 88, and a resistor 89. The first NPN bipolar transistor 85 includes an emitter electrically connected to the first or power low voltage  $V_{,,}$ , which can be, for example, ground, and a base and a collector electrically connected to a base of the second NPN bipolar transistor 86 at an input of the current mirror 83 configured to receive the control current  $I_{CONTROL}$ . The second NPN bipolar transistor 86 further includes an emitter electrically connected to the power low voltage  $V_1$ , and a collector electrically connected to a first end of the resistor 89, to a base of the fourth NPN bipolar transistor

88, and to a base and a collector of the third NPN bipolar transistor 87. The third and fourth NPN bipolar transistors 87, 88 each include an emitter electrically connected to the power low voltage  $V_1$ . The resistor 89 includes a second end configured to receive the enable signal ENABLE. The fourth NPN bipolar transistor 88 further includes a collector configured to generate the correction current  $I_{\text{CORRECTION}}$ .

The resistor 89 can have any suitable resistance, including, for example, a resistance selected based on the voltage level of power amplifier enable signal ENABLE and/or system requirements. In certain implementations, the resistor 89 has a resistance ranging between about 10 kQ to about 50 kQ, for example, about 20 kQ. By electrically connected the second end of the resistor 89 to the enable signal ENABLE, the power consumption of the power amplifier bias block 80 can be reduced when the enable signal ENABLE is low. **However, in other implementations, the current mirror 83 can be configured in other ways.**

**The current mirror 83 can have any suitable gain. In one implementation, the current mirror 83 is configured to amplify the control current  $I_{\text{CONTROL}}$ , by a factor ranging between about 5 to about 50, for example, about 10.** As used herein, the term current mirror can refer to current amplification circuits including a plurality of current mirrors combined (e.g., cascaded) to achieve a target gain.

EX-1001 10:62-11:45.



EX-1001 Fig. 5 (annotated).

49. In sum, in operation, the enable signal (pink arrow) is activated when the PA is enabled, switching from off to on. The time-dependent signal generator, in response, takes that flat “enable” signal and generates a shaped  $I_{CONTROL}$  (red arrow) that is received by the current amplifier (gold). The current amplifier (gold) scales up (amplifies)  $I_{CONTROL}$  (red arrow) to form  $I_{CORRECTION}$  (gold arrow). The primary biasing circuit (purple) receives the shaped  $I_{CORRECTION}$  and correspondingly adjusts the magnitude of the  $I_{BIAS}$  (purple arrow) to compensate for a variation in gain of the PA during startup. The short-term “boost” in  $I_{BIAS}$  helps overcome the PA’s low gain during startup, correcting for that gain variation of the PA. EX-1001 9:13-36; 9:47-56; see, e.g.:

The power amplifier bias block 50 includes a gain correction block 71 and a primary biasing circuit 74. The gain correction block 71 includes a time-dependent signal generator or control block 72 and a current amplifier 73.

EX-1001 9:13-36.

The power amplifier bias block 50 includes the time-dependent signal generator 72, which can be used to generate a control current  $I_{CONTROL}$  when the enable signal ENABLE is transitioned from a disabled state to an enabled state. The control current  $I_{CONTROL}$  can be provided to the current amplifier 73, which can amplify the control current  $I_{CONTROL}$  to generate a correction current  $I_{CORRECTION}$ . The correction current  $I_{CORRECTION}$  can be used by the primary biasing circuit 74 to correct for a variation in gain over time that can occur shortly after the power amplifier 32 is enabled.

EX-1001 9:47-56.

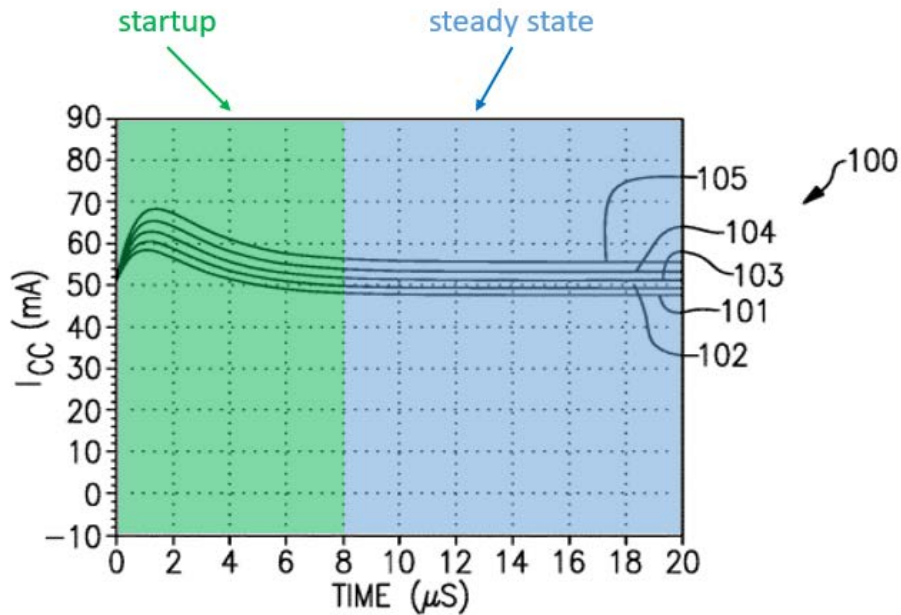
50. Figure 6 (below) is a graph of the collector current (of the PA transistor) versus time, where time zero is when the PA is enabled and where plots 101 through 105 correspond to different battery voltage values. The time-dependent signal generator generates  $I_{CONTROL}$  to adjust the PA's  $I_{BIAS}$  so that the PA's gain reaches steady state after about  $8\mu s$ . EX-1001 12:29-47; *see, e.g.:*

FIG. 6 is a graph 100 of one example of collector current versus time. The graph 100 begins at a time zero that is associated with enabling a power amplifier. The graph 100 includes a first plot 101, a second plot

102, a third plot 103, a fourth plot 104 and a fifth plot 105, which correspond to different battery voltage values. In particular, the first, second, third, fourth, and fifth plots 101-105 correspond to battery voltage values of about 3.2 V, about 3.4 V, about 3.6 V, about 3.8 V, and about 4.0 V, respectively.

In certain implementations described herein, a time-dependent signal generator is used to generate a signal that can be used to adjust a power amplifier's bias current during a time period within about 8  $\mu$ s after the power amplifier is enabled. Thereafter the power amplifier's bias current can be substantially constant until the power amplifier's enable signal is deactivated. In certain implementations, the power amplifier's bias current can vary by more than about 50% during the initial time period that the correction current is used to adjust the power amplifier's bias current.

EX-1001 12:29-47.



**FIG.6**

EX-1001 Fig. 6 (annotated).

**B. Priority Date of the Challenged Claims**

51. The '101 Patent claims priority to May 13, 2011. EX-1001 (60) (provisional application 61/486,186, filed on May 13, 2011. Solely for the purposes of this IPR, I have been instructed to assume the priority date for the Patent is May 13, 2011.

**C. Claim Construction**

52. I have been instructed to give each claim term in the Challenged Claims its plain and ordinary meaning in this proceeding. It is my opinion that the prior art I have relied upon meets each of the claim terms under any reasonable construction. Thus, I understand that no specific construction of any claim term is required.

#### **D. Person of Ordinary Skill in the Art**

53. With respect to the 101 Patent, a POSITA would have been someone knowledgeable and familiar with analog and RF circuit design. A POSITA would have gained knowledge of these concepts through a mixture of training and work experience, such as by having at least a Bachelor's degree in electrical engineering, or related field, and at least two to three years of training or additional work experience in the area of RF electronics, or a related field. Additional hands-on and design experience could compensate for less formal education, and vice versa, at the time of the priority date of each patent. The knowledge and skill of a POSITA is further reflected in the prior art references themselves, as well as the State of the Art, discussed below.

#### **E. State of the Art**

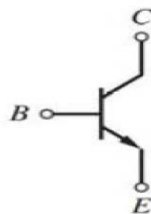
54. In the following section I describe the state of the art for power amplifier systems as of May 13, 2011. The prior art references, and the discussions of what was known to a POSITA, provide the factual support for the general description of the state of the art at the time of the invention, provide additional motivation to modify or combine the reference. Accordingly, these references should be considered by the Board.

##### **1. The Gain Variation of Power Amplifier at Startup Was Known**

55. A POSITA in May 2011 understood that a PA was commonly implemented using one or more transistors (such as a bipolar junction transistor (BJT)) to amplify an RF signal. EX-1008(*Johnson*)1605 (“bipolar transistors have evolved as the preferred choice” for wireless PAs due to “higher gain and current density at the frequencies employed”); *see, e.g.:*

Several device technologies have found use in the PA field. Historically, gated field-effect structures such as MOS and MESFET structures have found widespread use but, due to higher gain and current density at the frequencies employed, bipolar transistors have evolved as the preferred choice. GaAs HBTs have dominated such applications, however, bandgap-engineered SiGe heterostructure bipolar transistors (HBTs) are an emerging alternative due to their ability to provide high integration and to reduce cost.

EX-1008 1605. A BJT transistor has three terminals, “collector”, “base” and “emitter” as labelled, “C”, “B”, and “E”, respectively, in the figure below.



EX-1013(*Gray*) 92. The biasing and operation of such transistors to amplify a signal applied to the base of the transistor was well known. EX-1024(*Horowitz*) 218, 220-228; EX-1006 47-50, 52-55; EX-1015 38; *see, e.g.:*

Transistor circuits are usually designed to amplify an ac input voltage rather than dc current. In this type of arrangement, the ac is superimposed on the dc. The dc is used to establish specific quiescent emitter and collector currents. These *bias currents* should set the idling voltage (voltage before ac is applied to the circuit) at the collector at one-half of  $E_{CC}$ . Because the collector voltage,  $V_C$ , is equal to  $E_{CC} - I_C R_C$ ,  $V_C$  should be idling at about  $E_{CC}/2$ .

EX-1024 218

Bias or idling conditions are established when there is no ac voltage at the input of the circuit, or  $E_{IN} = 0$ . At this time, only the dc emitter supply voltage less the base-emitter voltage is across  $R_C$  the only component in this circuit that is outside of the transistor.

EX-1024 220.

As was true in the common-base circuit, it is also desirable here to let the voltage at the collector terminal in this circuit idle at  $E_{CC}/2$  volts. To do this, the idling voltage across  $R_C$  must be equal to half of the supply voltage, or  $I_C R_C = E_{CC}/2$ . Because  $I_C$  is related to  $I_B$ ,  $I_B$  is set by the designer of the circuit to equal the desired  $I_C$  divided by beta.  $I_B$  can, of course, be set by using the proper base resistor,  $R_B$ , in the circuit. Ac signal voltage is usually fed through a capacitor to the base and applied between the base and emitter to the transistor. The input voltage varies the base and hence collector current in step with the cyclic variations of the ac. A magnified version of the ac input voltage is developed across the collector resistor by the ac collector current flowing through it.

EX-1024 222-223.

The ac input signal adds a variable current to the dc idling current in the base. It is amplified by the transistor so that a magnified version of the ac input is across  $R_C$ . When the voltage at the base is at its peak in the cycle, the collector current is also at its peak. Because the voltage across  $R_C$  is the product of the collector current with  $R_C$ , this voltage is also at its maximum level.

EX-1024 222-224.

The bipolar transistor (both NPN and PNP) is a normally-off device until sufficient voltage ( $V_{BE}$ ) and base current ( $I_B$ ) are provided to turn it on, because it is a current-controlled device. The transistor can be biased into any one of three states: *cutoff* (off), *saturated* (full-on), or *active* (a predetermined state facilitated by biasing it halfway between saturation and cutoff) (Figure 4.4A). For example, in a 12-volt amplifier circuit, the transistor would normally be biased midway between the supply rails at 6 volts, to ensure a perfectly symmetrical AC signal swing (assuming that the input signal was also at the correct level) (Figure 4.48).

The BJT relies on a small forward base current ( $I_B$ ) and a small forward voltage ( $V_{BE}$ ) at its base, inducing and controlling a much larger forward current between the collector and the emitter. The base current ( $I_B$ ) is very small in comparison with the collector and emitter currents. For small-signal transistors switching a few milliamps, the base current will likely be in microamps.

EX-1006 52.

**bias** *Short for* bias voltage. A voltage applied to an electronic device to ensure that it operates on a particular portion of its ► characteristic curve.

EX-1015 38.

56. A POSITA in May 2011 was well aware that the gain response of a PA “varies with temperature” and that “at temperatures below the [PA’s] steady-state operating temperature,” the gain of a PA will be lower than it would be at the steady-state operating temperature (assuming the same bias signal). EX-1010(*Doherty*) ¶¶5-6; *see, e.g.:*

Although various fluctuations in physical characteristics caused by changing operating conditions can affect the gain or phase response of the PA, the temperature of the PA has a profound affect on its response.

EX-1010 ¶5.

The gain and phase response of a PA varies with temperature such that at temperatures below the steady-state operating temperature, the actual gain exhibited by the PA having a specific bias signal applied thereto will be less than the expected gain of the PA at steady-state operating temperatures in response to that same specific bias signal, and correspondingly, the actual phase response at a specific bias may be different from the expected phase response of the PA at steady-state operating temperatures. As the PA warms up, the actual gain of the PA increases to its expected value while the phase response of the PA

approaches an expected steady-state phase response. In order to achieve a desired target operating gain and phase response, a standard or steady-state bias level can be applied to the PA while the PA is operating at its steady-state operating temperature, but at temperatures below the steady-state operating temperature, the standard bias level is insufficient to achieve the target operating response.

EX-1010 ¶6. It was known that, as the PA warms up, the gain of the PA approaches its steady-state expected value. A POSITA was thus aware that “at temperatures below the steady-state operating temperature, the standard bias level is insufficient to achieve the target operating response.” EX-1010 ¶6. This problem existed in conditions where “the PA’s temperature fluctuates between idle temperatures and its steady-state operating temperature” and this fluctuation “causes variations in the gain and phase of the PA away from the target operating response.” EX-1010 ¶8; *see, e.g.:*

Due to its profound affect on the gain and phase response of the PA, one main contributor to unwanted changes in a PA's response and dynamic EVM is thermal changes of the PA caused by dynamic heating effects. Under pulsed conditions, the PA's temperature fluctuates between idle temperatures and its steady-state operating temperature, which in turn causes variations in the gain and phase of the PA away from the target operating response. One particular situation for which this can occur, is when the PA receives an RF signal data burst, after it has remained idle long enough that its temperature has fallen below its steady-state operating temperature. In one standard RF transmitter

application, a TX enable is received 500 ns to 1 us before the RF signal data to be transmitted is received. If the PA is sufficiently small, this time period is long enough to allow the PA to turn on and warm-up to its steady-state operating temperature. If the PA is large, the time period between receipt of the Tx enable and the receipt of RF signal data may be shorter than the time the PA needs to reach its steady-state operating temperature. In this case, some of the RF signal data may be received and amplified while the PA is in a thermally changing state during which the gain and phase response of the amplifier is also changing. This occurs primarily at the beginning of the pulse sequence, when the PA is coolest and hence at a temperature farthest from its steady-state operating temperature.

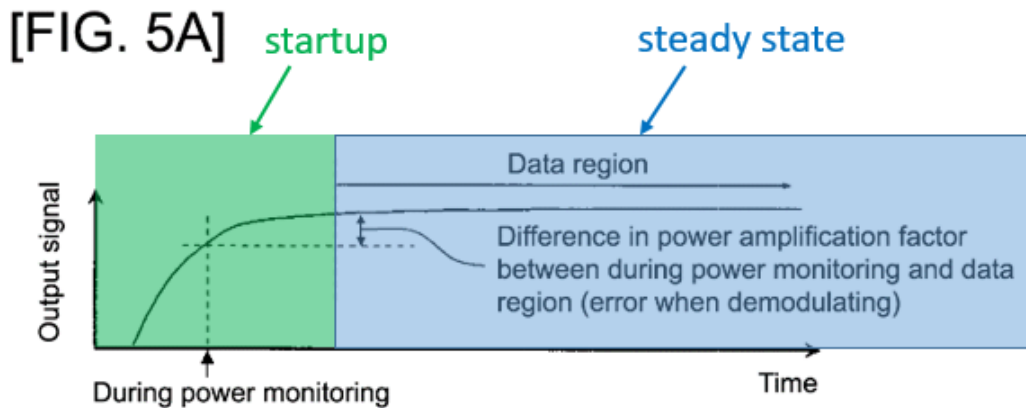
EX-1010 ¶8.

57. Further, it was known that a PA was conventionally operated in bursts, turning it on just before, and off just after, transmission of a signal, “in order to suppress power consumption” when not in use. EX-1018(*Akagi*) ¶4; *see, e.g.:*

In a communication device such as a wireless LAN, it is not such that an input signal is not always ON at the time of transmission in a system, but such that a burst operation is performed wherein an ON state in which the input signal is input and an OFF state in which the input signal is not input are repeated. In an off state in which an input signal is not input, a usage method in which a high-frequency power amplifier is turned off by being synchronized to a burst operation is often used in

order to suppress power consumption of a system. In the conventional high-frequency power amplifier in FIG. 4, the DC power source E1 is turned on and off by being synchronized to the burst operation, but the DC power source E2 is always on.

EX-1018 ¶4. Consistent with EX-1010 discussed above, it was well known that the gain (or “power amplification factor”) of the PA is lower at startup (green) than at steady state (blue), as shown below:



EX-1018 Fig. 5A (annotated), ¶6.

58. A POSITA also knew that this issue of the PA gain being too low on startup could be addressed using resistor-capacitor based “speedup” circuits to provide a temporary boost to the  $I_{BIAS}$  supplied to a PA. For example, *Doherty* described that a “common approach” to avoid “unwanted ... gain variations” in the PA was to “to speed up the gain ... response of the PA by applying an external resistor and speed-up capacitor to provide more forward [bias] current earlier to the PA.” EX-1010 ¶9; *see, e.g.:*

In order to ensure low dynamic EVM and an output signal that is not distorted by unwanted gain and phase variations, a PA is generally not used unless it is thermally stable. A common approach to avoid the problem of dynamic EVM is simply to wait until a PA is thermally stable before using it to amplify the signal. A second common approach is to speed up the gain and phase response of the PA by applying an external resistor and speed-up capacitor to provide more forward current earlier to the PA. Although the speed-up capacitor can improve the time response of the PA, as a passive mechanism it cannot provide the additional forward current until the RF input signal itself arrives. Consequently, the beginning of the RF signal data will suffer from some amount of dynamic EVM and the additional current may not be sufficient to bring the PA into a thermally stable state at a desired rate.

EX-1010 ¶9. Likewise, *Akagi* described that in “the conventional high-frequency power amplifier”, a resistor and capacitor circuit (EX-1018 Fig. 4, R1, C1) is generally used so that “immediately after the DC power source E1 is turned on, an instantaneous current flows into the bias circuit” to cause the PA’s “bias point” to be “set to be high, and the power amplification factor becomes high” to provide “power amplification factor correction” to compensate for the thermal properties of the PA. EX-1018 ¶7, Fig. 4 (R1, C1) ; *see, e.g.:*

Thus, in the conventional high-frequency power amplifier, as illustrated in FIG. 4, a method wherein a circuit in which the resistor R1 and the capacitor C1 as an example of a capacitance element are connected in parallel is inserted in series between the DC power source E1 and the

bias circuit 130 is generally used. In this case, immediately after the DC power source E1 is turned on, an instantaneous current flows into the bias circuit 130 via the capacitance 1, and the same voltage as the DC voltage of the DC power source E1 is applied to the bias circuit 130. The voltage value applied to the bias circuit 130 gradually decreases according to a time constant determined by the resistor R1 and the capacitor C1, and finally reaches a value corresponding to a voltage drop caused by the current flowing through the resistor R1. Thus, for the amplifier, the DC voltage of the DC power source E1 is applied immediately after the power source is turned on, the bias point is set to be high, and the power amplification factor becomes high, but, as time advances, current flows through the resistor R1, causing a voltage drop, and the amplifier operates at a low bias point and the power amplification factor becomes small by the amount of voltage drop. Thus, the power amplification factor correction is performed based on the thermal response.

EX-1018 ¶7. Thus, a POSITA had a well-developed understanding of using time-dependent current generation, including RC speedup circuits, to adapt a PA biasing circuit to boost a PA's  $I_{BIAS}$  in the period just after enablement of the PA.

## **2. Current Mirrors Were Widely Known**

59. Current mirrors were likewise commonplace and formed part of the general knowledge in the art long before May 2011. As discussed further below, a POSITA was well versed in their multiple and various structures, from single-transistor mirrors, to complicated, multi-transistor designs. A POSITA understood

how to use and include current mirrors in analog circuit designs, including RF PAs and their biasing circuits. Their behavior and benefits were predictable and well documented. They were pervasive in the literature.

60. For example, the current mirror had “become a familiar icon of modern analog design.” EX-1012(*Gilbert*) 239. They were “widely used in analog integrated circuits [] as biasing elements.” EX-1013(*Gray*) 251. Indeed, current mirrors were considered “particularly useful building blocks for analog circuit design” because “they provide a means of establishing the DC bias levels within the circuit.” EX-1014(*Grebene*) 170. Using current mirrors in biasing had advantages including “superior insensitivity of circuit performance to variations in power supply and temperature.” EX-1013 251.

61. As its name suggests, a current mirror is a circuit that “replicates” (in the sense of “reproduces”, “reflects”, “replicates”, “duplicates” *etc.*)—*i.e.* “mirrors”—an input current as its output current. EX-1014 170 (“the reference current” is “**reproduced or reflected**” and “because of this property” are “known as *current mirror* circuits.”); *see, e.g.:*

In a constant-current stage, the reference current in one branch of the circuit is accurately reproduced or reflected in a second branch, relatively independent of the absolute values of the device parameters. Because of this property, these subcircuits are also known as *current mirror* circuits. Such circuit configurations are particularly useful

building blocks for analog circuit design, since they provide a means of establishing the dc bias levels within the circuit, within the accuracy of the matching or tracking properties of the monolithic components.

EX-1014 170. EX-1012 240 (“an output node ... into which a **replication**” of “the input current flows in the same direction”); *see, e.g.:*

The simplest current mirror is a three-terminal device, Figure 6.1a, having an input node, N1, capable of accepting a current,  $I_1$ , of only one polarity, an output node, N2, into which a replication,  $I_2$ , of the input current flows in the same direction, and a common node, N0, in which the sum of the input and output currents flow.

EX-1012 240. EX-1013 251 (“[T]he input current is **reflected** to the output, **leading to the name *current mirror*.**”); *see, e.g.:*

A current mirror is an element with at least three terminals, as shown in Fig. 4.1. The common terminal is connected to a power supply, and the input current source is connected to the input terminal. Ideally, the output current is equal to the input current multiplied by a desired current gain. If the gain is unity, the input current is reflected to the output, leading to the name current mirror. Under ideal conditions, the current-mirror gain is independent of input frequency, and the output current is independent of the voltage between the output and common terminals.

EX-1013 251. EX-1006 70-71 (“*current mirrors* (aka current reflectors), where an input current is mirrored at the output, in either a matched 1:1 or other ratio.”); *see, e.g.:*

Some other devices, such as the JFET, the current regulator diode (CRD), and the power MOSFET, can result in a two-lead current source configuration, but any worthwhile BJT current source requires an input terminal, an output terminal, and a voltage bias point. In some configurations, four terminals are needed. As a result, virtually all BJT current sources are configured as *current mirrors* (aka current reflectors), where an input current is mirrored at the output, in either a matched 1 :1 or other ratio. This may be either a fraction or a multiple of the input, or scaled in some other manner.

EX-1006 70-71.

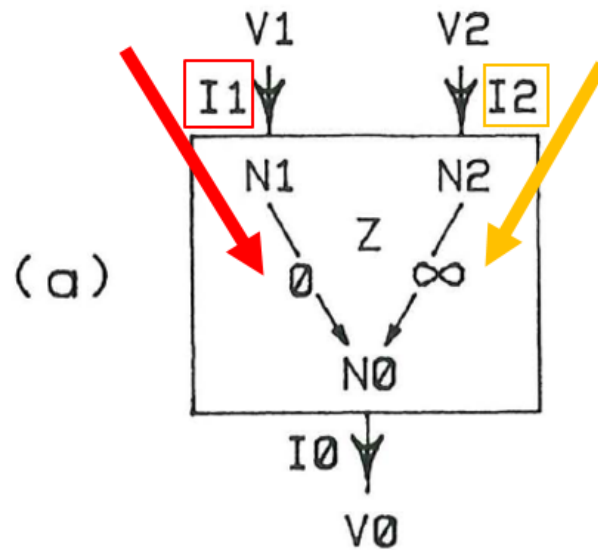
62. Barrie Gilbert started his textbook chapter on “Bipolar Current Mirrors” by observing that “[f]ew readers of this book will need to be introduced to the concept of the current mirror; it has become a familiar icon of modern analog design.” EX-1012 239. Barrie Gilbert was one of the pre-eminent industry leaders in analog circuit design. EX-1021(*Gilbert Biography*) (“Barrie was likely the most famous analog circuit designer in the world.”). Barrie Gilbert was featured, for example, on “the cover of the Fall 2007 IEEE Solid-State Circuits Society News issue and virtually the entire issue devoted to him.” EX-1021

(showing IEEE issue cover page titled “The Gears of Genius: Barrie Gilbert and Analog Circuits”).

63. *Gilbert* begins by describing the “generalized form” of a current mirror. He described the “simplest current mirror” was a three node device, with “an input node, N1, capable of accepting a current  $I_1$ ” (red arrow) of “only one polarity, an output node, N2, into which a **replication**  $I_2$ ” (gold arrow) of “the input current flows in the same direction, and a common node, N0, in which the sum of the input and output currents flow.” EX-1012 240; *see, e.g.:*

The simplest current mirror is a three-terminal device, Figure 6.1a, having an input node, N1, capable of accepting a current,  $I_1$ , of only one polarity, an output node, N2, into which a replication,  $I_2$ , of the input current flows in the same direction, and a common node, N0, in which the sum of the input and output currents flow.

EX-1012 240.



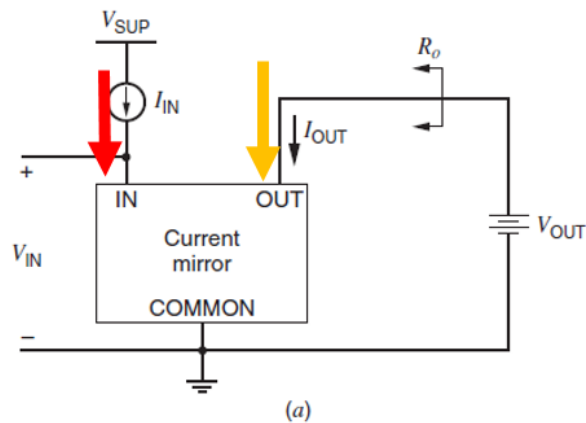
EX-1012 240, Fig. 6.1a (annotated); *accord* EX-1013 Fig. 4.1a.

64. In such current mirrors, the replicated current ( $I_2$ , gold arrow above) is pulled into the mirror, and is thus called a “current sink.” This arrangement is referred to as a “positive” current mirror. EX-1012 330; EX-1013 Fig. 4.1; *see, e.g.:*

There are many different types of current mirror and we begin by considering some definitions and terms commonly used. Current mirrors are firstly categorised as positive or negative. Positive current mirrors have an output in the form of a current sink (quiescent output current positive). Thus they require a power supply which is at a relatively negative potential. Negative current mirrors have a current source output (quiescent output current negative) and require a more positive power supply.

EX-1012 330.

65. Current mirrors having a common node at the more positive power supply, and replicate the input current as a current source flowing out of the output of the current mirror are referred to as “negative” current mirrors. see EX-1012 330; EX-1013 252, Fig. 4.1(b). *Gray* likewise depicts the same fundamental inputs and outputs of a current mirror:



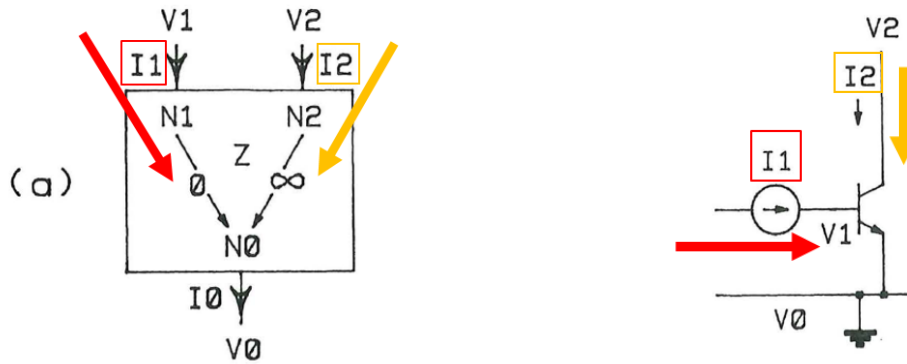
EX-1013 (*Gray*) Fig. 4.1(a) (annotated).

66. This ability of a current mirror to take an input current that is acting as a current source (*red*), and then replicate that same current *i.e. mirror* it, to create a current *sink* at the output node of the mirror, was well known to a POSITA. This was a common reason to include a current mirror in a circuit, *i.e.*, when one needed to couple a current source from one circuit as a current sink pulling a replicated amount of current from another circuit.

### Single Transistor Current Mirrors

67. Current mirrors were known to come in many forms. For example, it was well known to use a single transistor to take, *e.g.*, a current source as an input

current, and then replicate (*mirror*) it to an output terminal of the transistor as, *e.g.*, a current sink. For example, *Gilbert* provides a section on “One-transistor Mirrors”, describing how to arrange a single BJT transistor as a current mirror.



*Gilbert, 240, Fig. 6.1a (annotated)*    *Gilbert, 243, Fig. 6.2a (annotated)*

68. *Gilbert* explained that “[i]n the simplest possible scenario, a single BJT can be used as a mirror.” EX-1012 242 (section titled “One-transistor Mirrors”). With reference to the transistor in Fig. 6.2 (above), *Gilbert* explained that node N1 (of the general current mirror form shown in Figure 6. 1a) is the base of the transistor in Fig. 6.2a (*i.e.* the input of the current mirror), and likewise, N2 is the collector (*i.e.* the output of the current mirror), and N0 the emitter (*i.e.* the common node of the current mirror). EX-1012 242; *see, e.g.*:

In the simplest possible scenario, a single BJT can be used as a mirror: node N1 (of Figure 6. 1a) is the base, N2 the collector and N0 the emitter. Of course, the practical objection to this proposal is that the mirror ratio,  $M$ , is much higher than generally needed and poorly-controlled, being just the common-emitter current-gain,  $J3$ , and not

very linear. While these objections are all true, it is nevertheless useful to begin here, because we will discover that many of the properties of more familiar mirrors can be predicted from the behavior of the single transistor circuit.

EX-1012 242.

69. While “not very linear” and “poorly-controlled” compared to other current mirrors, the “mirror ratio,  $M$ ” of the single BJT mirror is the “common-emitter current-gain,  $\beta$ ”. EX-1012 242. The output is scaled by the amplification factor of the BJT, namely the common-emitter current-gain,  $\beta$ . That is because in a BJT biased into its active region, the collector current ( $I_C$ ) and base current ( $I_B$ ) are generally related by the equation:  $I_C = I_B * \beta$ . EX-1015 38; EX-1012 242-243; *see, e.g.:*

**beta current gain factor** *Syn.* common-emitter forward-current transfer ratio; forward current gain. Symbol:  $\beta$ . The short-circuit current-amplification factor in a bipolar transistor with ► common-emitter connection:  $\beta = \alpha I_c / \alpha I_B$   $V_{CE}$  constant where  $I_C$  is the collector current and  $I_B$  is the base current; the collector voltage,  $V_{CE}$ , is constant.  $\beta$  is always greater than unity and practical values up to 500 are used.

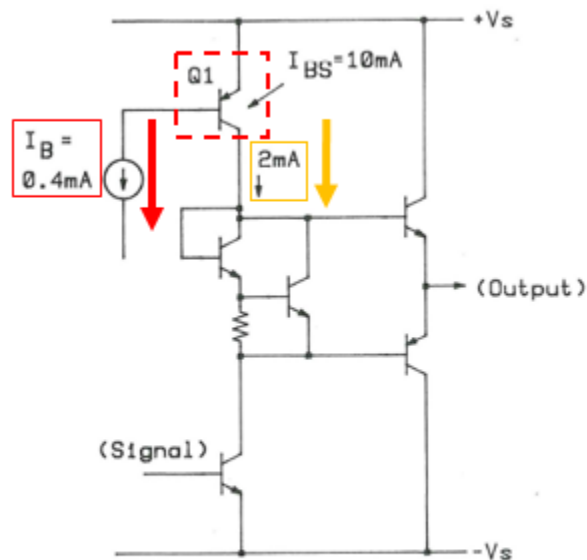
EX-1015 38.

It will be assumed that  $\beta$  is independent of current over the range of interest. If  $\beta$  were also independent of  $V_2$ , the output  $I_2$  would always be simply  $\beta I_1$  and the output resistance  $r_0$  would be infinite. In fact,  $\beta$  increases with  $V_2$  due to base-width modulation, and in the customary

BJT model would be exactly doubled when the collector bias voltage,  $V_{CB}$  (roughly,  $V_2$ ), is equal to the forward Early voltage,  $V_{AF}$ .

EX-1012 243.

70. Similarly, in the following example, *Gilbert* shows and describes a single transistor current mirror, “Q1”, to bias “an operational amplifier”.



*Gilbert*, Fig. 6.4 (annotated)

EX-1012 Fig. 6.4 (annotated).

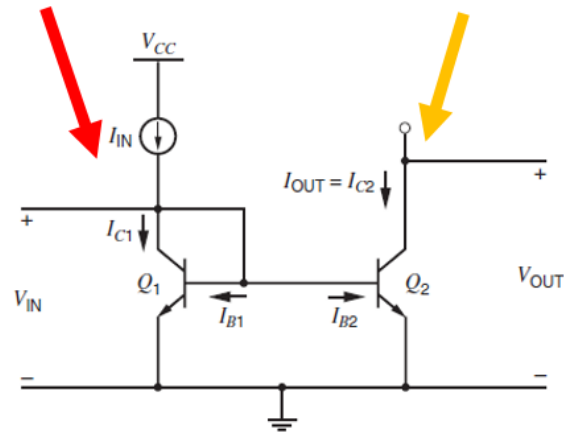
71. *Gilbert* described the transistor Q1 in the above figure as a “simple open-base PNP **current mirror**”, “used to bias an [operational amplifier] ... with improved efficiency.” EX-1012 248; *see, e.g.:*

Figure 6.4 A simple open-base PNP current mirror (Q1) used to bias an op-amp slewing node with improved efficiency; remaining components are for illustrative purposes only.

EX-1012 248.

### Two-Transistor Current Mirrors

72. Long before May 2011, undergraduate electrical engineering students were likewise conversant with the basic two-transistor current mirror form. EX-1013 253, Fig. 4.2; EX-1012 251, Fig. 6.7a. For example, a “simple bipolar current mirror” is shown in the annotated Figure 4.2 below, with the input current annotated in red and the mirrored output current in yellow.



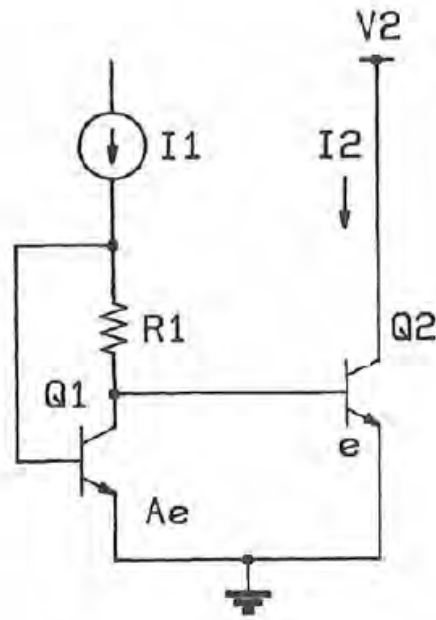
EX-1013 253, Fig. 4.2.

73. This two-transistor current mirror format was a heavily documented, staple of analog circuit design having highly predictable behaviors and advantages, readily known to undergraduate level students.

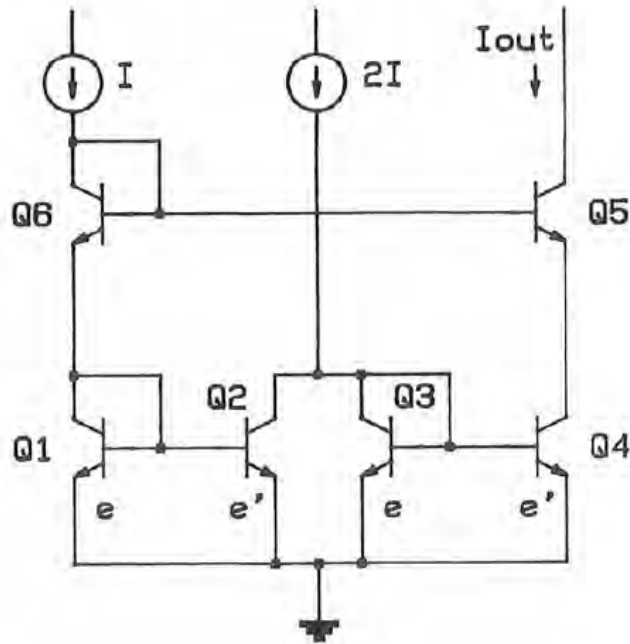
### Advanced Current Mirrors

74. Although a POSITA knew of simple single and two transistor current mirror designs, a POSITA also knew that “current mirrors” were not limited to any one configuration or arrangement.

75. More advanced, multi-transistor structures were likewise known for mirroring an input current to an output current, with various connections between the gates of the mirrors. EX-1012 261, Fig. 6.12b, 276-77, Fig. 6.25b; EX-1012 292, Fig. 6.42c.



EX-1012 261, Fig. 6.12b.



EX-1012 286, Fig. 6.36.

76. One well-known benefit of current mirrors was that they could be configured to provide a desired current amplification when mirroring the current, such that the “output current is equal to the input current multiplied by a desired current gain.” EX-1013 251; *see, e.g.:*

A current mirror is an element with at least three terminals, as shown in Fig. 4.1. The common terminal is connected to a power supply, and the input current source is connected to the input terminal. Ideally, the output current is equal to the input current multiplied by a desired current gain. If the gain is unity, the input current is reflected to the output, leading to the name current mirror. Under ideal conditions, the current-mirror gain is independent of input frequency, and the output current is independent of the voltage between the output and common terminals.

EX-1013 251. It was well known that one could advantageously set the gain by controlling the size of the transistors involved. EX-1013 254, 257; *see, e.g.:*

Thus for identical devices  $Q1$  and  $Q2$ , the gain of the current mirror is approximately unity... In practice, the devices need not be identical... Since the saturation current of a bipolar transistor is proportional to its emitter area, the first term in (4.6) shows that the gain of the current mirror can be larger or smaller than unity because the emitter areas can be ratioed. If the desired current-mirror gain is a rational number,  $M/N$ , the area ratio is usually set by connecting  $M$  identical devices called *units* in parallel to form  $Q2$  and  $N$  units in parallel to form  $Q1$  to minimize mismatch arising from lithographic effects in forming the emitter regions

EX-1013 254.

Equation 4.17 shows that the gain of the current mirror can be larger or smaller than unity because the transistor sizes can be ratioed. To ratio the transistor sizes, either the widths or the lengths can be made unequal in principle. In practice, however, the lengths of  $M1$  and  $M2$  are rarely made unequal.

EX-1013 257. In the case of bipolar transistors, this was done by scaling emitter area. EX-1012 280; EX-1014 172; *see, e.g.:*

There is no particular difficulty in achieving high mirror ratios. In many cases, simple emitter area ratios will suffice, supported by current gain if necessary (as in the EFA mirror, which is not limited to the use of a

single transistor for current boosting). In practical monolithic designs, emitter area ratios of up to 100: 1 are not hard to achieve.

EX-1012 280.

The basic current-voltage equations (4.1) through (4.8) hold over a broad temperature range (typically -60 to + 150°C) and over six orders of magnitude of current. Thus, the basic current mirror circuit of Figure 4.1 provides a means of obtaining a current reference level, independent of implicit device parameters, which can be "scaled" by proper choice of the emitter areas of the two transistors. Assuming typical  $V_{BE}$  mismatch of  $< \pm 1$  mV and  $\beta$  in the range of 100-200, the typical output current /2 would be within  $\pm 5\%$  of  $I_{ref}$  over a wide range of temperature and current levels.

EX-1014 172.

77. Thus, there was a robust state of the art in current mirrors at the time of the purported invention. A POSITA knew how to design and implement a wide variety of mirror circuits, from single transistor to complicated multi-transistor circuits, all achieving well understood, predictable behavior in replicating, *i.e.*, mirroring an input current to an output current.

### **3. BJT Power Amplifiers Were Commonly Implemented Using Heterojunction Bipolar Transistors (HBTs)**

78. By May 2011, it was well known to implement PAs using bipolar junction transistors (BJT). *Supra* §IV.F.1; EX-1008(*Johnson*) 1605 (explaining

that “bipolar transistors have evolved as the preferred choice” for wireless PAs due to “higher gain and current density at the frequencies employed” ; *see, e.g.*:

Several device technologies have found use in the PA field. Historically, gated field-effect structures such as MOS and MESFET structures have found widespread use but, due to higher gain and current density at the frequencies employed, bipolar transistors have evolved as the preferred choice. GaAs HBTs have dominated such applications, however, bandgap-engineered SiGe heterostructure bipolar transistors (HBTs) are an emerging alternative due to their ability to provide high integration and to reduce cost.

EX-1008 1605. Furthermore, it was well-known, general knowledge in the art that a high performing type of BJT for RF PAs was a BJT with a wide band gap emitter, known as a Heterojunction Bipolar Transistor (HBT). *See, e.g.*, EX-1015(*Illingworth*) 259 (defining HBT, including, *e.g.*, “A bipolar junction transistor that incorporates a wide band gap emitter” with the result of reduced base resistance, “maximizing the desired injection of carriers from emitter to base.... HBTs are used at radio- and microwave frequencies, in integrated circuit and power applications”). HBTs were known to be specifically adapted for high performance to meet the demands of RF power amplification applications. *See, e.g.*, EX-1015 259 (describing that the HBT properties “leads to **an improvement in the high-frequency performance** of the transistor. **HBTs are used at radio-**

**and microwave frequencies**, in integrated circuit and power applications, and in optoelectronic ICs.”); *see, e.g.*:

**heterojunction bipolar transistor (HBT)** A bipolar junction transistor that incorporates a wide band gap emitter. The emitter-base junction is a heterojunction between semiconductors of different energy band gap. The following are typical material systems: AlGaAs(emitter)/GaAs(base); AlInAs/InGaAs; Si/SiGe

The wider band gap of the emitter reduces significantly the injection of majority carriers from base to emitter, thus maximizing the desired injection of carriers from emitter to base. This eliminates the requirement for a heavily doped emitter to achieve the same result, and consequently allows the base doping to be increased. An increase in base doping is desirable from a device viewpoint as the base resistance can be reduced significantly. This leads to an improvement in the high-frequency performance of the transistor. HBTs are used at radio- and microwave frequencies, in integrated circuit and power applications, and in optoelectronic ICs.

EX-1015 259. In fact, HBTs were the dominant, market leading form for RF PAs implemented with BJTs, with well-documented advantages known to a POSITA.

EX-1017(*TriQuint*) 1 (“RF medium and high **power amplifiers realized with HBT technology are increasingly popular in telecommunications systems** due to the **inherently superior linearity and efficiency performance** compared to competing technologies. The **reliability of HBT RF devices is well known to be**

**excellent** from Highly Accelerated Stress Testing (HAST) and High Temperature Operating Lifetime (HTOL) testing.”); EX-1025(*Yanjun*) 1 (“In past years, **HBT PAs have dominated the medium power transmitter market due to their excellent linearity and PAE.**”); EX-1008 1605 (explaining advantages including “provid[ing] high integration and [] reduce[d] cost,” reduced chip area and increased chip robustness, temperature insensitive current gain, and well characterized reliability at high current densities enabling further reduction in device size).

79. It was known that HBTs came in a variety of advantageous forms, including Gallium Arsenide (GaAs) and Silicon Germanium (SiGe). EX-1015 259. For example, SiGe HBTs found “increasing use in wireless PA applications” due to “favorable thermal properties,” “volume manufacturing capability,” and “design automation support,” which had all “long been recognized.” EX-1008 1612. Such HBTs had “favorable device ruggedness for PA applications.” *Id.* HBT PA designs had been demonstrated to meet the needs of a range of wireless standards, including the robustness required at the high speed, output power and linearity called for by the GSM, GPRS, and EDGE wireless standards. *Id.* It was known that the “favorable thermal properties, lower cost of wafer processing, and the higher integration capabilities” of such HBTs “make them a compelling choice

for wireless applications” and provide a “very strong path for PA modules.” *Id.*;  
*see, e.g.:*

SiGe BiCMOS technology is finding increasing use in wireless PA applications. The favorable thermal properties, volume manufacturing capability, and design automation support of SiGe BiCMOS technology have long been recognized. Detailed investigation of the SOA analysis of SiGe HBTs reveals favorable device ruggedness for PA applications.

Device engineering with respect to SiGe HBT speed and ruggedness has been intensively studied. A roadmap of SiGe BiCMOS technologies targeting wireless PA applications will be constrained by the tradeoff between HBT ruggedness and speed discussed in this paper. SiGe HBTs that require high breakdown voltages will not strongly benefit from the vertical scaling trends that drive high-performance low-power HBT roadmaps due to the significant collector thickness required to support high levels of device ruggedness. Because of this, SiGe BiCMOS technologies targeting wireless PA applications will not be expected to show significant increases in from generation to generation unless PA ruggedness requirements are relaxed. However, it has been shown that high-breakdown SiGe BiCMOS HBTs engineered for wireless PA applications should benefit significantly from advances in lateral scaling and new device architectures, without detriment to device ruggedness, and can therefore be expected to show a significant generational progression in performance metrics related to power gain.

PA designs have been demonstrated for GSM, GPRS, and EDGE wireless standards using a SiGe HBT technology specifically tailored to meet the divergent requirements of high VSWR robustness at high output power and high linearity. The GPRS/EDGE FEM shown here exceeds the 15:1 VSWR requirement at 33 dBm with an overall efficiency of 37%. The SiGe HBT was optimized to simultaneously provide ruggedness and speed and is compatible with the base 0.5 m CMOS. The favorable thermal properties, lower cost of wafer processing, and the higher integration capabilities demonstrated by these SiGe PAs make them a compelling choice for wireless applications. A SiGe BiCMOS flip-chip together with LTCC is a very strong path for PA modules. The combined module exhibits superior performance and stability together with a low component count for the entire front-end solution.

EX-1008 1612.

80. Thus, the use of BJT transistors to form a PA, including the HBT form of BJTs and their advantages, formed part of the general knowledge in the art before the invention.

## **VI. IDENTIFICATION OF CHALLENGES**

### **A. Challenged Claims**

81. Claims 1, 2, 10-11, 17, 18, 20, 21, and 22 of the '101 Patent are challenged in the petition.

## B. Statutory Grounds for Challenges

Grounds	Claims	Basis	References
Ground 1	1, 2, 10-11, 17, 18, 20, 21, and 22	§103	<i>Ishimaru</i>
Ground 2	1, 2, 10-11, 17, 18, 20, 21, and 22	§103	<i>Ishimaru</i> in view of <i>Harrison</i>

## C. Prior Art Basis

82. I understand that U.S. Patent Publication 2009/0212863 (“Ishimaru”) (EX-1004) and Current Sources and Voltage References, A Design Reference for Electronics Engineers (Elsevier 2005) (“Harrison”) (EX-1006) qualify as prior art for purposes of this IPR.

## VII. IDENTIFICATION OF HOW THE CHALLENGED CLAIMS ARE UNPATENTABLE

### A. Ground 1: Claims 1-2, 10-11, 17-18, and 20-22 Are Obvious over *Ishimaru*

#### 1. *Ishimaru*

83. *Ishimaru* is titled “Power Amplifier” and relates to “a high frequency power amplifier to be used in radio communication devices or the like.” EX-1004 Abstract, ¶1; *see, e.g.*:

In the power amplifier of the invention, at a start of power amplification by an amplifier transistor 103 serving as an amplification section, a speedup circuit 122 transiently increases a bias which is fed to the amplifier transistor 103 via a bias power source section composed of a

bias circuit 111 and a power source circuit 112. As a result, the power amplification factor of the amplifier transistor 103 is transiently increased at the start of power amplification by the amplifier transistor 103. Thus, the time elapsing until temperature variations due to heat generation of the amplifier transistor 103 come to an equilibrium on the whole circuit is shortened, with a result of reduced distortion of the amplification signal such as a modulated-wave signal. Accordingly, in the invention, it becomes possible to suppress distortion increases of an amplification signal due to heat generation at the start time without using any temperature sensing element.

EX-1004 Abstract. *Ishimaru* explains that PAs in communication systems such as those using “Orthogonal Frequency Division Multiplex[ing]” have “such a circuit design for linearization that the system runs on a linear amplification range of enough smaller outputs than a maximum output of the power amplifier” so that the output RF signal “is not distorted in the power amplifier.” *Id.* ¶2; *see, e.g.:*

Conventionally, a power amplifier including a bipolar transistor is used as an amplifier for amplifying a signal or the like. Among others, a system that requires linear amplification such as a system using OFDM (Orthogonal Frequency Division Multiplex) modulated waves or the like has such a circuit design for linearization that the system runs on a linear amplification range of enough smaller outputs than a maximum output of the power amplifier so that the modulated wave signal is not distorted in the power amplifier.

*Id.* ¶2. *Ishimaru* further explains that “linear amplification” “means that even with input signal power changed, the output signal power is amplified at a constant ratio for output while the phase keeps unchanged.” Further, *Ishimaru* explains that in some communication systems, “slight changes of amplification gain as small as 0.2 to 0.3 dB may matter,” *i.e.*, affect a communication link. *Id.* ¶3; *see, e.g.*:

It should be noted here that the linear amplification mentioned above means that even with input signal power changed, the output signal power is amplified at a constant ratio for output while the phase keeps unchanged. In some communication systems, slight changes of amplification gain as small as 0.2 to 0.3 dB may matter

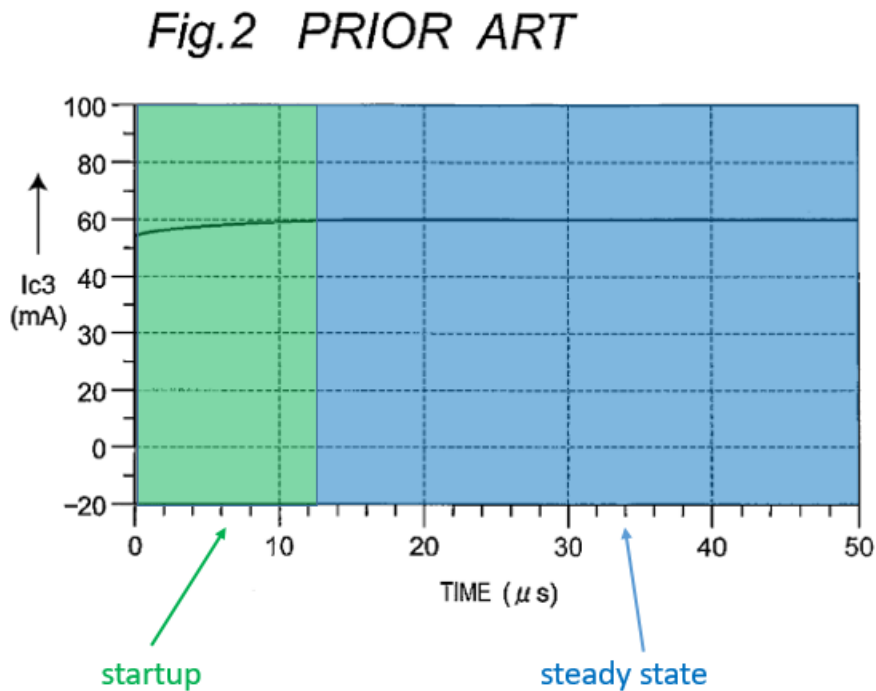
*Id.* ¶3. A POSITA would thus understand that *Ishimaru* is from the same field of art as the '101 Patent because it relates to the field of RF electronics generally, PAs specifically, and controlling/compensating gain in particular..

84. *Ishimaru* explains that thermal changes that occur slowly during startup can last for “tens to several hundreds of microseconds” and affect the “amplification ratio” of the PA during that time. EX-1004 ¶4; *see, e.g.*:

As another aspect of the linear amplification, there are some cases in which variations in amplification ratio or phase on the order of several tens to several hundreds of us caused by relatively slow temperature increases due to heat generation as an example do matter. As a circuit for correcting effects of such heat generation by the power amplifier's own, there has been shown, in U.S. Pat. No. 4,924, 194 (see FIG. 1), a circuit in which heat generation of an amplifier transistor is detected by

a temperature sensing element (PIN diode) thermally coupled to the amplifier transistor and the detection result is reflected on a bias voltage of the amplifier transistor.

*Id.* ¶4. In an example of such gain variation of the PA at startup, *Ishimaru* showed how collector current of the PA comes up slowly (~10 us in this example):



EX-1004 Fig. 2 (annotated).

85. *Ishimaru's* solution, shown in Figure 1 below, was a PA and bias circuit that included a “speedup circuit” that “transiently (temporarily) increases” the  $I_{BIAS}$  fed to the amplifier transistor by the bias circuit during the period after startup. EX-1004 ¶13; *see, e.g.:*

According to the power amplifier of this invention, at a start of power amplification by the first transistor of the amplification section, the speedup circuit transiently (temporarily) increases the bias fed to the first transistor by the bias power source section, so that the power amplification factor of the first transistor is transiently increased at the start of power amplification. Thus, the time elapsing until temperature variations due to heat generation of the first transistor (amplifier transistor) that performs the power amplification come to an equilibrium on the whole circuit is shortened, with a result of reduced distortion of the amplification signal (e.g., modulated-wave signal).

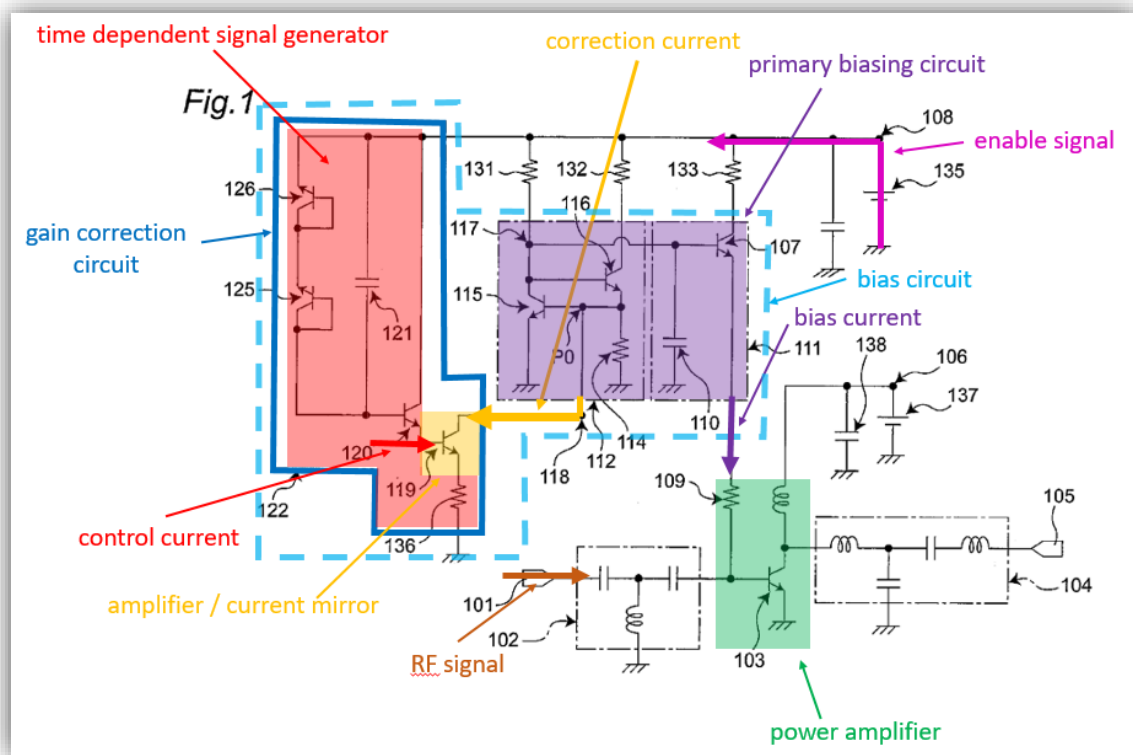
EX-1004 ¶13. Speedup circuit 122 includes transistors 119, 120, resistance element 136, as well as a capacitance element 121 connected between the base of transistor 120 and bias terminal 108. *Id.* ¶50-51; *see, e.g.:*

The speedup circuit 122 has a fifth transistor 119 whose collector is connected to the output terminal 118, and a sixth transistor 120 whose emitter is connected to a base of the fifth transistor 119. The emitter of the fifth transistor 119 is connected to the ground via a resistance element 136.

EX-1004 ¶50.

The speedup circuit 122 also has a capacitance element 121 which is connected between a base of the sixth transistor 120 and the bias terminal 108, and two diodes 125, 126 which are connected in series between the base of the sixth transistor 120 and the bias terminal 108.

EX-1004 ¶51.



EX-1004 Fig. 1 (annotated).

86. Figure 1 shows an input signal terminal 101 that receives a high-frequency signal (brown arrow) as an input signal, and this input signal passes through an input matching circuit 102, and is then amplified by amplifier transistor 103 (green). The amplifier transistor 103 outputs a signal through output matching circuit 104 to output signal terminal 105. Figure 1 also depicts a bias circuit 111 and a bias power source section 112, which together constitute a bias power source section (purple), and a speedup circuit 122 (dark blue). EX-1004 ¶¶43, 46, 49; *see, e.g.:*

Also, a bias transistor 107 as a second transistor is a transistor that supplies a base bias current to a base terminal of the amplifier transistor 103. An emitter of the bias transistor 107 is connected to a base terminal of the amplifier transistor 103 via a resistance element 109. The resistance element 109 is a ballast (stabilization) resistor which is inserted in a base bias channel to prevent thermal runaway of the amplifier transistor 103.

EX-1004 ¶43.

A power source circuit 112 is connected to the base terminal of the bias transistor 107 of the bias circuit 111. The bias circuit 111 and the power source circuit 112 constitute a bias power source section.

EX-1004 ¶46.

A connecting point P0 between the base of the third transistor 115 and the emitter of the fourth transistor 116 in the power source circuit 112 is connected to an output terminal 118 of a speedup circuit 122.

EX-1004 ¶49.

87. Bias circuit 111 includes a bias transistor 107 and capacitance element 110, where a collector of the bias transistor is connected to a bias terminal 108, which is in turn connected to a control voltage source 135. EX-1004 ¶44; *see, e.g.:*

The bias transistor 107 has its collector connected to a bias terminal 108 via a resistance element 133. The bias terminal 108 is connected to a control voltage source 135.

EX-1004 ¶44. The emitter of the bias transistor 107 is connected to the base of the amplifier transistor 103, and “supplies a base bias current” (purple arrow) to the base of the amplifier transistor (green). *Id.* ¶43; *see, e.g.:*

Also, a bias transistor 107 as a second transistor is a transistor that supplies a base bias current to a base terminal of the amplifier transistor 103. An emitter of the bias transistor 107 is connected to a base terminal of the amplifier transistor 103 via a resistance element 109. The resistance element 109 is a ballast (stabilization) resistor which is inserted in a base bias channel to prevent thermal runaway of the amplifier transistor 103.

*Id.* ¶43. Power source circuit 112 is connected to the base of the bias transistor 107. *Id.* ¶46; *see, e.g.:*

A power source circuit 112 is connected to the base terminal of the bias transistor 107 of the bias circuit 111. The bias circuit 111 and the power source circuit 112 constitute a bias power source section.

*Id.* ¶46. Power source circuit 112 has a connecting point P0, which is connected to an output terminal 118 of a speedup circuit 122. *Id.* ¶49; *see, e.g.:*

A connecting point P0 between the base of the third transistor 115 and the emitter of the fourth transistor 116 in the power source circuit 112 is connected to an output terminal 118 of a speedup circuit 122.

*Id.* ¶49.

88. The circuit used “capacitance element 121” “at turn-on of the amplifier” to generate an  $I_{CORRECTION}$  (gold arrow) that “transiently (temporarily)

flows” out of the biasing circuit from “output terminal 118.” That causes the voltage on the base of bias transistor 107 to “transiently increase[.]”, causing the bias “current fed to the amplifier transistor 103” to likewise “transiently increase[.]” EX-1004 ¶52; *see, e.g.*:

In the speedup circuit 122, with electric charge flowing into the capacitance element 121 at a rise time of the control voltage of the control voltage source 135 (at turn-on of the amplifier), a current transiently (temporarily) flows from the output terminal 118 into the fifth transistor 119, causing the voltage value of the output terminal 118 to lower. As a result, due to a change of the bias point of the third transistor 115, the voltage of a connecting terminal 117, which connects the collector of the third transistor 115 to the base of the bias transistor 107, transiently increases. Thus, at the rise time, the current fed to the amplifier transistor 103 by the bias transistor 107 transiently increases. Therefore, at the rise time, the power amplification factor of the amplifier transistor 103 transiently increases, so that the time elapsing until temperature variations due to heat generation of the amplifier transistor 103 come to an equilibrium on the whole circuit is shortened, with a result of reduced distortion of the amplification signal (e.g., modulated wave signal).

EX-1004 ¶52.

89. As illustrated in annotated Figure 1, a POSITA understood that the bias circuit (light blue) consists of a conventional “primary bias circuit” 111, 112 (purple) driven by a conventional, unmodified “enable signal” (pink), plus a gain

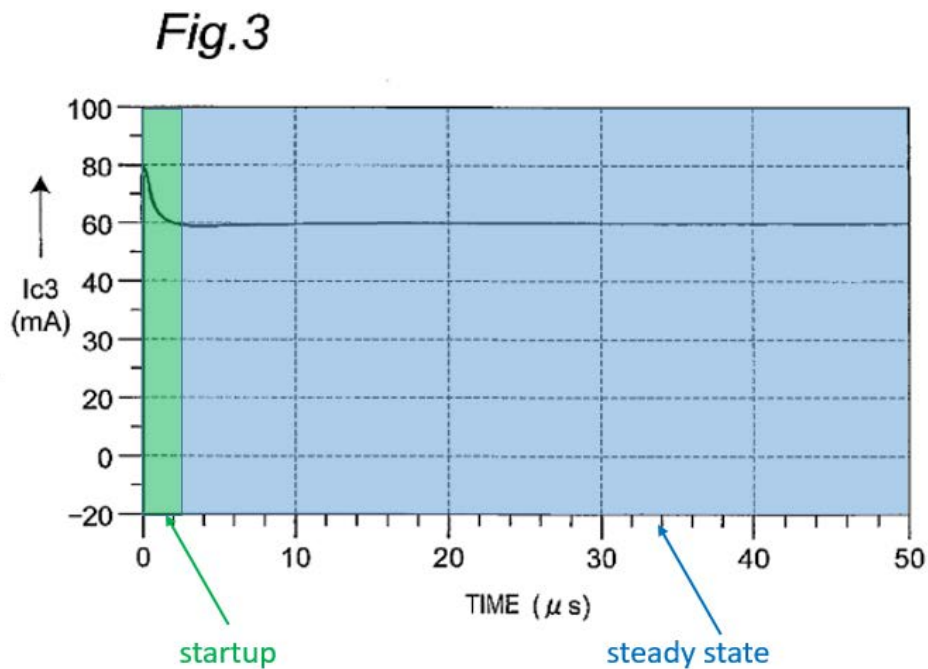
correction circuit (speedup circuit) (dark blue) that generates the  $I_{CORRECTION}$  (gold arrow) to shape the bias current (purple arrow) that emerges from the primary bias circuit. That  $I_{CORRECTION}$  is generated by the gain correction circuit using a time-dependent signal generator (red) to generate a small  $I_{CONTROL}$  (red arrow) with the desired shape, and then scaling up that shaped signal to an appropriate amplitude using a “current amplifier” (gold). The current amplifier replicates (*i.e.* mirrors) and amplifies  $I_{CONTROL}$  (red arrow) to form  $I_{CORRECTION}$  (gold arrow), which is pulled from the primary biasing circuit (purple).

90. *Ishimaru* explains that, at a rise time of control voltage source 135 (which is input to bias terminal 108 and is the enable signal), “with electric charge flowing into the capacitance element 121” “a current transiently (temporarily) flows from the output terminal 118 into the fifth transistor 119, causing the voltage value of the output terminal 118 to lower.” EX-1004 ¶52. The  $I_{BIAS}$  (purple arrow) fed “to the amplifier transistor 103 is forcedly increased at turn-on of the amplifier.” *Id.* ¶54. This means that “at the rise time, the current fed to the amplifier transistor 103 by the bias transistor 107 transiently increases.” *Id.* ¶52.

91. Accordingly, to compensate for the startup phenomenon shown in Figure 2 (above), *Ishimaru* disclosed simulation results of the transient boost in PA collector current at PA startup. EX-1004 ¶54, Fig. 3; *see, e.g.*:

Next, FIG. 3 shows an example (simulation result) of transient response of the operating current (collector current  $I_{c3}$ ) of the amplifier transistor 103 in the power amplifier of this embodiment. In this embodiment, the current to be fed from the bias transistor 107 to the amplifier transistor 103 is forcibly increased at turn-on of the amplifier, with the result that the value of the operating current  $I_{c3}$  comes to a steady state in about 1/4 the time of transient response of the comparative example of FIG. 2. Thus, occurrence of distortions of the amplification signal due to temperature variations in the amplifier circuit is suppressed, so that the linearity of the circuit in burst operation is improved. That is, gain variations due to collector current variations of the power amplifier using a bipolar transistor can be compensated.

EX-1004 ¶54.



EX-1004 Fig. 3 (annotated).

92. *Ishimaru* taught that the forced transient boost in current corrected for the startup gain variation of the PA:

Therefore, at the rise time, **the power amplification factor of the amplifier transistor 103 transiently increases**, so that the **time elapsing until temperature variations** due to heat generation of the amplifier transistor 103 **come to an equilibrium** on the whole circuit is shortened, with a result of **reduced distortion of the amplification signal** (e.g., modulated wave signal).

EX-1004 ¶52.

Thus, occurrence of **distortions of the amplification signal due to temperature variations in the amplifier circuit is suppressed**, so that the **linearity** of the circuit in burst operation is **improved**. That is, **gain variations** due to collector current variations **of the power amplifier** using a bipolar transistor **can be compensated**.

EX-1004 ¶54.

## 2. Detailed Application of *Ishimaru* to the Challenged Claims

### Claim 1

#### *[1.0] A power amplifier system comprising:*

93. To the extent that the preamble is limiting, the bias and PA circuitry in *Ishimaru's* Figure 1 is a power amplifier system for “a high-frequency power amplifier to be used in radio communication devices.” EX-1004 ¶¶1, 41, Fig. 1. The circuitry for the PA system includes “an amplification section having a first

transistor for performing power amplification”, as well as “a bias power source section”, “bias circuit,” and “a speedup circuit.” EX-1004 Abstract, ¶¶10-12, Fig.

1 (annotated below); *see, e.g.:*

In the power amplifier of the invention, at a start of power amplification by an amplifier transistor 103 serving as an amplification section, a speedup circuit 122 transiently increases a bias which is fed to the amplifier transistor 103 via a bias power source section composed of a bias circuit 111 and a power source circuit 112. As a result, the power amplification factor of the amplifier transistor 103 is transiently increased at the start of power amplification by the amplifier transistor 103. Thus, the time elapsing until temperature variations due to heat generation of the amplifier transistor 103 come to an equilibrium on the whole circuit is shortened, with a result of reduced distortion of the amplification signal such as a modulated-wave signal. Accordingly, in the invention, it becomes possible to suppress distortion increases of an amplification signal due to heat generation at the start time without using any temperature sensing element.

EX-1004 Abstract.

an amplification section having a first transistor for performing power amplification;

EX-1004 ¶10.

a bias power source section having a second transistor for feeding a bias to the first transistor; and

EX-1004 ¶11.



95. *Ishimaru* discloses “a high-frequency power amplifier to be used in radio communication devices.” EX-1004 ¶1. The circuitry for the PA includes “an amplification section having a first transistor for performing power amplification” (green) (*a power amplifier*). EX-1004 ¶¶10-12. As illustrated in Figure 1 (annotated below), *Ishimaru* further discloses that “a high-frequency signal as an input signal [is] inputted from an input signal terminal 101, ... is amplified by an amplifier transistor 103 serving as a first transistor, and then, ... outputted from an output signal terminal 105” (*power amplifier configured to amplify*). EX-1004 ¶42; *see, e.g.:*

In this power amplifier, a high-frequency signal as an input signal inputted from an input signal terminal 101, passing through an input matching circuit 102, is amplified by an amplifier transistor 103 serving as a first transistor, and then, after passing through an output matching circuit 104, outputted from an output signal terminal 105. In FIG. 1, reference sign 106 denotes a collector bias terminal of the amplifier transistor 103. Between the collector bias terminal 106 and the ground are connected a DC power source 137 and a capacitance element 138. The amplifier transistor 103 forms an amplification section.

EX-1004 ¶42.

96. Specifically, because *Ishimaru* is directed to a PA for a **radio** communications device, a POSITA reading *Ishimaru* understood that the high-frequency input signal at input terminal 101 is a *radio frequency (RF) signal*

(brown arrow) for amplification by amplifier transistor 103 (*a power amplifier configured to provide amplification*) to generate an amplified radio frequency signal at output terminal 105.

***[1.2] a bias block for biasing the power amplifier, the bias block including***

97. *Ishimaru* discloses this limitation. As shown in Figure 1, *Ishimaru* discloses a “speedup circuit 122,” “power source circuit 112,” and “bias circuit 111” (collectively, *a bias block*) (light blue) that receives a control voltage from voltage source 135 (enable signal) (pink arrow) and supplies a “base bias current” ( $I_{BIAS}$ ) (purple arrow) to the base terminal of amplifier transistor 103 (*biasing the power amplifier*) (green). EX-1004 Abstract, ¶¶24, 31, 43, 45, 49-52; *see, e.g.:*

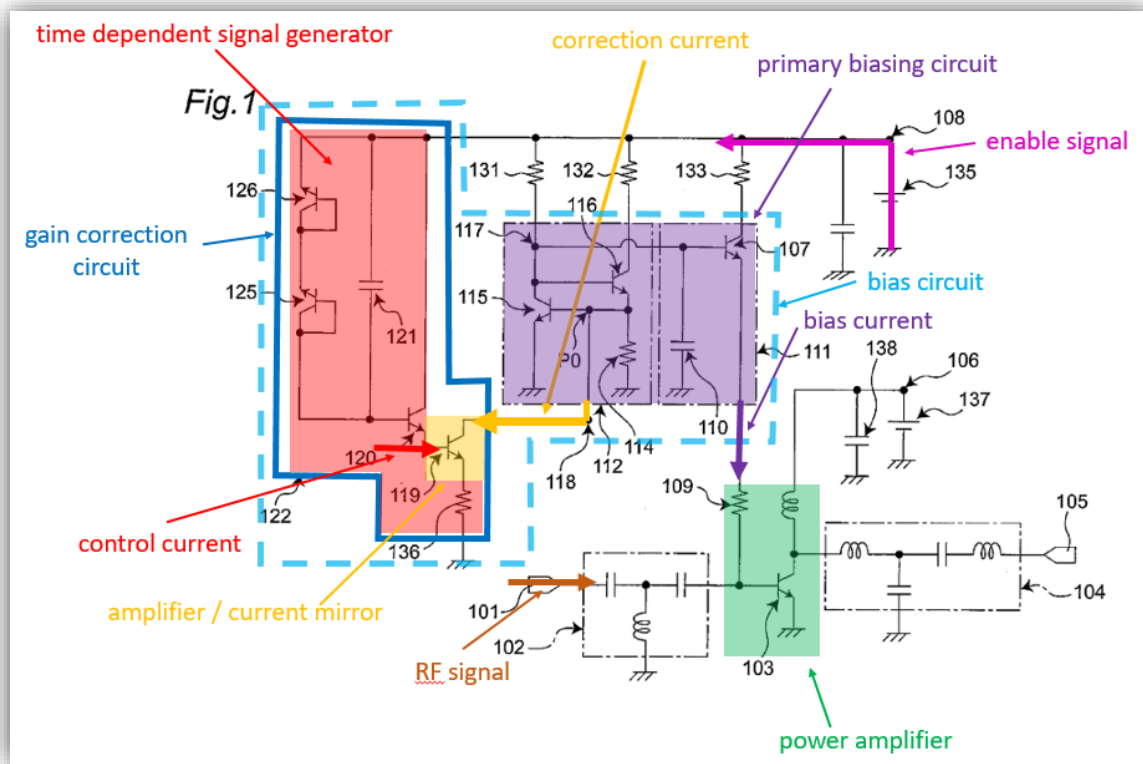
In the power amplifier of the invention, at a start of power amplification by an amplifier transistor 103 serving as an amplification section, a speedup circuit 122 transiently increases a bias which is fed to the amplifier transistor 103 via a bias power source section composed of a bias circuit 111 and a power source circuit 112. As a result, the power amplification factor of the amplifier transistor 103 is transiently increased at the start of power amplification by the amplifier transistor 103. Thus, the time elapsing until temperature variations due to heat generation of the amplifier transistor 103 come to an equilibrium on the whole circuit is shortened, with a result of reduced distortion of the amplification signal such as a modulated-wave signal. Accordingly, in the invention, it becomes possible to suppress distortion increases of an

amplification signal due to heat generation at the start time without using any temperature sensing element.

EX-1004 Abstract.

A bias circuit 111 composed of the bias transistor 107 and a capacitance element 110 connected to a base terminal of the bias transistor 107 has a function of increasing the base bias current in response to an increase in signal strength of the input signal, and functions to keep the amplification ratio of an output signal as well as its phase rotation after amplification constant even when the signal strength of the input signal has changed.

EX-1004 ¶45.



EX-1004 Fig. 1 (annotated).

***[1.2.1] a time-dependent signal generator configured to shape an enable signal of the power amplifier to generate a control current,***

98. *Ishimaru* discloses this limitation. *Ishimaru* discloses that the control voltage from control voltage source 135 at bias terminal 108 “controls turn-on and -off of power amplification.” EX-1004 ¶24; *see, e.g.*:

Accordingly, in this invention, at the start of power amplification, i.e., immediately after the control voltage source that controls turn-on and -off of the power amplification is turned on so that the bias voltage is applied from the control voltage source to the first transistor via the bias power source section, the current following into the base of the first transistor is transiently increased by the speedup circuit. As a result of this, variations in the operating current due to heat generation of the power amplifier or the like can be canceled, by which variations in amplification factor can be suppressed, and improvement of the linearity can be achieved. That is, without use of any temperature sensing element, since the speedup circuit enabled to adjust the transient response of the operating current is connected to the bias power source section, distortion increases of the amplification signal (modulated-wave signal) due to heat generation can be suppressed.

EX-1004 ¶24. Thus, *Ishimaru*'s control voltage is *an enable signal of the power amplifier* (pink) as the PA is only operable when the bias is active and the bias is only active when the terminal 108 is high.

99. With reference to Figure 1, *Ishimaru* discloses a speedup circuit 122 (dark blue) that includes a capacitance element 121, diodes 125 and 126, transistors 119 and 120, and resistance element 136 (*a time-dependent signal generator*) (red). EX-1004 ¶¶50-51; *see, e.g.:*

The speedup circuit 122 has a fifth transistor 119 whose collector is connected to the output terminal 118, and a sixth transistor 120 whose emitter is connected to a base of the fifth transistor 119. The emitter of the fifth transistor 119 is connected to the ground via a resistance element 136.

EX-1004 ¶50.

The speedup circuit 122 also has a capacitance element 121 which is connected between a base of the sixth transistor 120 and the bias terminal 108, and two diodes 125, 126 which are connected in series between the base of the sixth transistor 120 and the bias terminal 108.

EX-1004 ¶51. In response to the “rise time of the control voltage of the control voltage source 135 (at turn-on of the amplifier),” (*enable signal*) (pink arrow), the speedup circuit applies a transient or time-varying current to the base of transistor 119 (*control current*) (red arrow). EX-1004 ¶52; *see, e.g.:*

In the speedup circuit 122, with electric charge flowing into the capacitance element 121 at a rise time of the control voltage of the control voltage source 135 (at turn-on of the amplifier), a current transiently (temporarily) flows from the output terminal 118 into the fifth transistor 119, causing the voltage value of the output terminal 118

to lower. As a result, due to a change of the bias point of the third transistor 115, the voltage of a connecting terminal 117, which connects the collector of the third transistor 115 to the base of the bias transistor 107, transiently increases. Thus, at the rise time, the current fed to the amplifier transistor 103 by the bias transistor 107 transiently increases. Therefore, at the rise time, the power amplification factor of the amplifier transistor 103 transiently increases, so that the time elapsing until temperature variations due to heat generation of the amplifier transistor 103 come to an equilibrium on the whole circuit is shortened, with a result of reduced distortion of the amplification signal (e.g., modulated wave signal).

EX-1004 ¶52. This is a control current at least because it is used to control the correction to the biasing of *Ishimaru's* PA to compensate for gain variation, as discussed next.

100. *Ishimaru's* speedup circuit 122 (dark blue) includes a *time dependent signal generator* (red) in that it is a circuit configured to change an enable signal (pink arrow) of the PA to achieve a desired shape of ( $I_{CONTROL}$ ) (red arrow), where the control current changes based on time. The shaping eventually results in the corresponding time-dependent current shown in Figure 3. EX-1004 ¶¶ 8-12, 52-56, Fig. 3. As explained in more detail below with respect to limitation [1.2.2], the speedup circuit 112 (dark blue) shapes  $I_{CONTROL}$  (red arrow) and amplifies it to form a correction current ( $I_{CORRECTION}$ ) (gold arrow) as a “current that transiently (temporarily) flows” out of the PA’s primary biasing circuit (purple). EX-1004

¶52.; see [1.2.2]. The time-dependent shape of the  $I_{CONTROL}$  (red arrow) is thereby used to shape the  $I_{CORRECTION}$  (gold arrow) in an amount and duration necessary to cause the primary biasing circuit to send a corresponding temporary boost in  $I_{BIAS}$  to the PA (green) to boost its gain during the startup period when its gain would otherwise be too low, *i.e.* to correct for the gain variation of the PA. EX-1004 ¶¶ 8-12, 52-55, Figs. 2 and 3. The speed up circuit, and its capacitor 121, changes the flat nature of the enable/on signal into a signal that is not just “on”, but instead is made to have a desired time-varying shape for compensating PA gain variation. EX-1004 ¶¶ 49-52, 55-56; see, *e.g.*:

In the speedup circuit 122, with electric charge flowing into the capacitance element 121 at a rise time of the control voltage of the control voltage source 135 (at turn-on of the amplifier), a current transiently (temporarily) flows from the output terminal 118 into the fifth transistor 119, causing the voltage value of the output terminal 118 to lower. As a result, due to a change of the bias point of the third transistor 115, the voltage of a connecting terminal 117, which connects the collector of the third transistor 115 to the base of the bias transistor 107, transiently increases. Thus, at the rise time, the current fed to the amplifier transistor 103 by the bias transistor 107 transiently increases. Therefore, at the rise time, the power amplification factor of the amplifier transistor 103 transiently increases, so that the time elapsing until temperature variations due to heat generation of the amplifier transistor 103 come to an equilibrium on the whole circuit is shortened,

with a result of reduced distortion of the amplification signal (e.g., modulated wave signal).

EX-1004 ¶ 52.

Next, FIG. 3 shows an example (simulation result) of transient response of the operating current (collector current  $I_{c3}$ ) of the amplifier transistor 103 in the power amplifier of this embodiment. In this embodiment, the current to be fed from the bias transistor 107 to the amplifier transistor 103 is forcibly increased at turn-on of the amplifier, with the result that the value of the operating current  $I_{c3}$  comes to a steady state in about 1/4 the time of transient response of the comparative example of FIG. 2. Thus, occurrence of distortions of the amplification signal due to temperature variations in the amplifier circuit is suppressed, so that the linearity of the circuit in burst operation is improved. That is, gain variations due to collector current variations of the power amplifier using a bipolar transistor can be compensated.

EX-1004 ¶ 54.

***[1.2.2] a current amplifier configured to amplify the control current to generate a correction current, and***

101. *Ishimaru* discloses this limitation. The *control current* ( $I_{CONTROL}$ ) (red arrow) is amplified by transistor 119, (*current amplifier*) (gold) resulting in the transient *correction current* ( $I_{CORRECTION}$ ) (gold arrow) being pulled into the collector of transistor 119 from node 118. EX-1004 ¶52; *see also* [1.2.1]; *see, e.g.:*

In the speedup circuit 122, with electric charge flowing into the capacitance element 121 at a rise time of the control voltage of the control voltage source 135 (at turn-on of the amplifier), a current transiently (temporarily) flows from the output terminal 118 into the fifth transistor 119, causing the voltage value of the output terminal 118 to lower. As a result, due to a change of the bias point of the third transistor 115, the voltage of a connecting terminal 117, which connects the collector of the third transistor 115 to the base of the bias transistor 107, transiently increases. Thus, at the rise time, the current fed to the amplifier transistor 103 by the bias transistor 107 transiently increases. Therefore, at the rise time, the power amplification factor of the amplifier transistor 103 transiently increases, so that the time elapsing until temperature variations due to heat generation of the amplifier transistor 103 come to an equilibrium on the whole circuit is shortened, with a result of reduced distortion of the amplification signal (e.g., modulated wave signal).

EX-1004 ¶52.

102. A POSITA recognized that transistor 119 amplifies its base current by the beta factor,  $\beta$ , of transistor 119 to provide amplification, e.g., 60 to 150 or higher. EX-1006 53-55; EX-1015 38 (practical  $\beta$  values can be “up to 500”); *see, e.g.:*

**beta current gain factor** *Syn.* common-emitter forward-current transfer ratio; forward current gain. Symbol:  $\beta$ . The short-circuit current-amplification factor in a bipolar transistor with ► common-emitter connection:  $\beta = \alpha I_C / \alpha I_B$   $V_{CE}$  constant where  $I_C$  is the collector

current and  $I_B$  is the base current; the collector voltage,  $V_{CE}$ , is constant.  $\beta$  is always greater than unity and practical values up to 500 are used.

EX-1015 38. Thus, transistor 119 is a *current amplifier configured to amplify* the current at its base (red arrow) (*the control current*) to generate the amplified  $I_{CORRECTION}$  at its collector (gold arrow) (*to generate a correction current*).

$I_{CORRECTION}$  (gold arrow) is a “current that transiently (temporarily) flows” out of the PA’s primary biasing circuit (purple). EX-1004 ¶52.  $I_{CORRECTION}$  (gold arrow) is a correction current in that it is shaped in an amount and duration necessary to cause the primary biasing circuit (discussed below) to send a corresponding temporary boost in  $I_{BIAS}$  (purple arrow) to the PA (green) to boost its gain during the startup period when its gain would otherwise be too low, *i.e.* to correct for the gain variation of the PA. EX-1004 ¶¶ 8-12, 52, 55, Figs. 2 and 3. *See also, infra*, [1.2.4] (discussing amplifier implemented as a current mirror with amplification due to mirror ratio); *see, e.g.*:

an amplification section having a first transistor for performing power amplification;

EX-1004 ¶ 10.

a bias power source section having a second transistor for feeding a bias to the first transistor; and

EX-1004 ¶11.

a speedup circuit for transiently increasing the bias fed to the first transistor by bias power source section at a start of the power amplification.

EX-1004 ¶12.

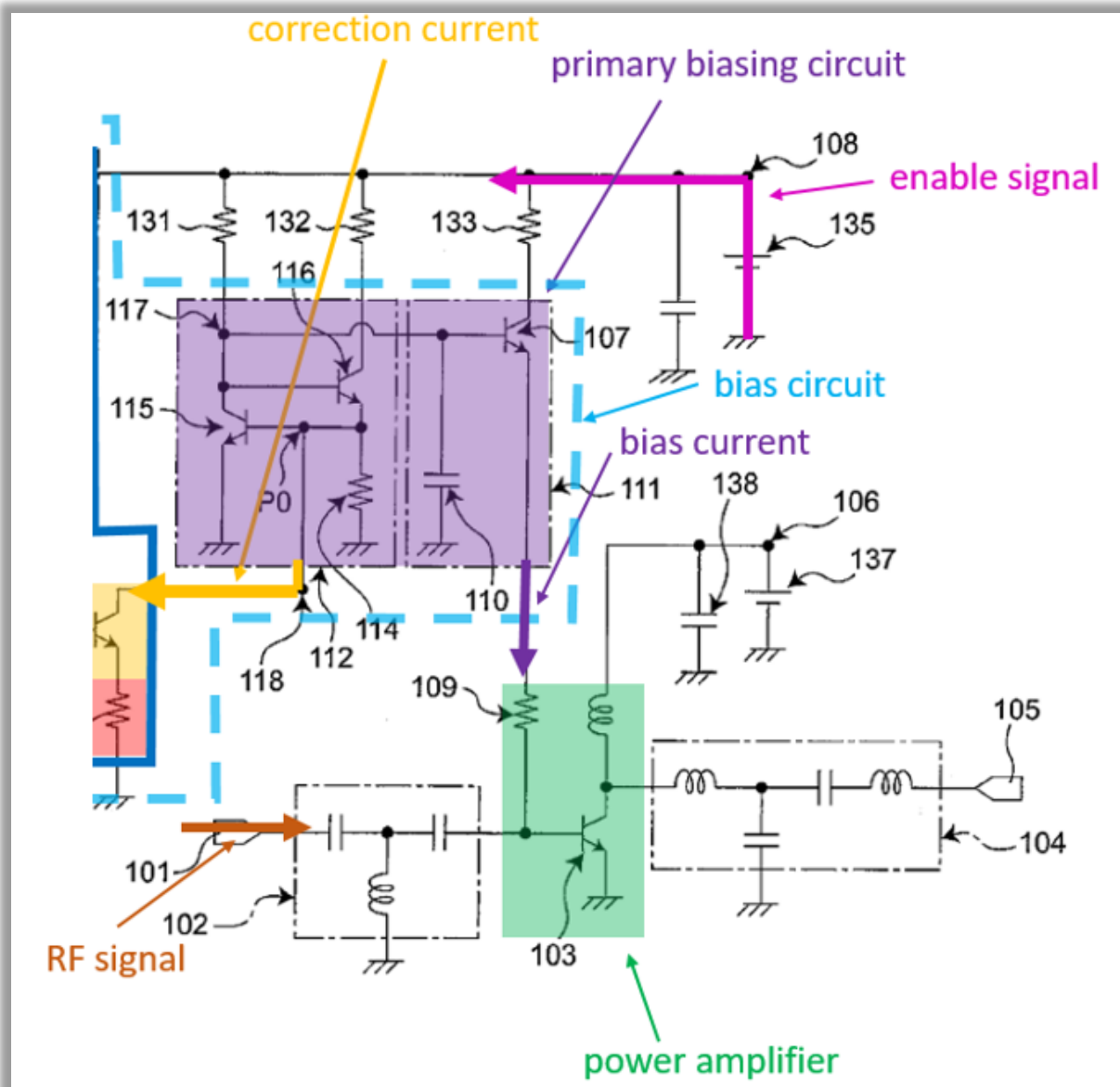
In the power amplifier of this embodiment also, the capacitance value of the capacitance element 121 of the speedup circuit 122 is adjusted so as to cancel transient variations in gain due to the temperature variations at a start of power amplification. As a result of this, deterioration of the linearity due to variations of amplification gain can be canceled so that the value of dynamic EVM (error vector magnitude) can be improved.

EX-1004 ¶55.

***[1.2.3] a primary biasing circuit configured to generate a bias current for the power amplifier based at least partly on the correction current, the bias current configured to correct for a variation in gain of the power amplifier when the power amplifier is enabled,***

103. *Ishimaru* discloses this limitation. As shown in the portion of Figure 1 reproduced below, *Ishimaru* discloses a power source circuit 112 and bias circuit 111, which constitute *the primary biasing circuit* (purple) which together supply a “base bias current” ( $I_{BIAS}$ , *a bias current for the power amplifier*) (purple arrow) to the amplifier transistor 103. As explained below, this boost  $I_{BIAS}$  is based on the current drawn out of node 118 ( $I_{CORRECTION}$ , *the correction current*) (gold arrow)

when the control voltage is applied (*the power amplifier is enabled*) (pink arrow) to correct for a variation in gain of the PA at startup.



EX-1004 Fig. 1 (partial) (annotated);

104. *Ishimaru* explains that “bias circuit 111 and the power source circuit 112 constitute a bias power source section.” EX-1004 ¶46; *see, e.g.*:

A power source circuit 112 is connected to the base terminal of the bias transistor 107 of the bias circuit 111. The bias circuit 111 and the power source circuit 112 constitute a bias power source section.

EX-1004 ¶46. The combination of this circuitry is a *primary biasing circuit* in that it is the main circuitry used to generate the  $I_{BIAS}$  that biases the operating point of the transistor of the PA (green) to its intended state (e.g. *enabled*, and biased to operate at its intended operating point, suitable for amplification). *See, e.g.*, EX-1024 218, 220, 222-228; EX-1006 Fig. 2.1; *see, e.g.*:

Transistor circuits are usually designed to amplify an ac input voltage rather than dc current. In this type of arrangement, the ac is superimposed on the dc. The dc is used to establish specific quiescent emitter and collector currents. These *bias currents* should set the idling voltage (voltage before ac is applied to the circuit) at the collector at one-half of  $E_{CC}$ . Because the collector voltage,  $V_C$ , is equal to  $E_{CC} - I_C R_C$ ,  $V_C$  should be idling at about  $E_{CC}/2$ .

EX-1024 218.

Bias or idling conditions are established when there is no ac voltage at the input of the circuit, or  $E_{IN} = 0$ . At this time, only the dc emitter supply voltage less the base-emitter voltage is across  $R_C$  the only component in this circuit that is outside of the transistor.

EX-1024 220.

As was true in the common-base circuit, it is also desirable here to let the voltage at the collector terminal in this circuit idle at  $E_{cc}/2$  volts. To

do this, the idling voltage across  $R_c$  must be equal to half of the supply voltage, or  $I_c R_c = E_{CC}/2$ . Because  $I_c$  is related to  $I_B$ ,  $I_B$  is set by the designer of the circuit to equal the desired  $I_c$  divided by beta.  $I_B$  can, of course, be set by using the proper base resistor,  $R_B$ , in the circuit. An ac signal voltage is usually fed through a capacitor to the base and applied between the base and emitter to the transistor. The input voltage varies the base and hence collector current in step with the cyclic variations of the ac. A magnified version of the ac input voltage is developed across the collector resistor by the ac collector current flowing through it.

EX-1024 223. More specifically, bias circuit 111 is “composed of the bias transistor 107 and a capacitance element 110” connected to the base of bias transistor 107. EX-1004 ¶45; *see, e.g.:*

A bias circuit 111 composed of the bias transistor 107 and a capacitance element 110 connected to a base terminal of the bias transistor 107 has a function of increasing the base bias current in response to an increase in signal strength of the input signal, and functions to keep the amplification ratio of an output signal as well as its phase rotation after amplification constant even when the signal strength of the input signal has changed.

EX-1004 ¶45. Bias transistor 107’s collector is connected to bias terminal 108 through a resistor 133, and the bias terminal 108 is connected to control voltage source 135 (*enable signal*) (pink arrow). EX-1004 ¶44; *see, e.g.:*

The bias transistor 107 has its collector connected to a bias terminal 108 via a resistance element 133. The bias terminal 108 is connected to a control voltage source 135.

EX-1004 ¶44. The emitter of bias transistor 107 is connected to a base terminal of the amplifier transistor 103 via resistance element 109 and “supplies a base bias current to the base of amplification transistor 103.” EX-1004 ¶43; *see, e.g.:*

Also, a bias transistor 107 as a second transistor is a transistor that supplies a base bias current to a base terminal of the amplifier transistor 103. An emitter of the bias transistor 107 is connected to a base terminal of the amplifier transistor 103 via a resistance element 109. The resistance element 109 is a ballast (stabilization) resistor which is inserted in a base bias channel to prevent thermal runaway of the amplifier transistor 103.

EX-1004 ¶43. The “base bias current” ( $I_{BIAS}$ ) is a *bias current*.

105. Bias transistor 107 in circuit 111 operates in conjunction with power source circuit 112 to generate  $I_{BIAS}$  that is applied to the amplifier transistor 103 and thus, circuit 111 and 112, collectively are a *primary biasing circuit* (purple).

106. More specifically, as shown in the portion of the annotated Figure 1 above, node 117 of circuit 112 is connected to the base terminal of the bias transistor 107 and, thus, controls the bias point of transistor 107 and, consequently, the transistor 107’s collector current. EX-1004 ¶¶46, 48; *see, e.g.:*

A power source circuit 112 is connected to the base terminal of the bias transistor 107 of the bias circuit 111. The bias circuit 111 and the power source circuit 112 constitute a bias power source section.

EX-1004 ¶46. Node P0 of power source circuit 112 (*i.e.*, the base of transistor 115 and emitter of transistor 116) is connected to output terminal 118 of speedup circuit 122. *Id.* ¶¶48-49; *see, e.g.*:

In this embodiment, as shown in FIG. 1, the power source circuit 112 has a third transistor 115, a fourth transistor 116, and a resistance element 114. The third transistor 115 has its collector connected to the base of the bias transistor 107 and its emitter connected to the ground. Also, a base of the third transistor 115 is connected to an emitter of the fourth transistor 116. The collector of the third transistor 115 is connected to the bias terminal 108 via a resistance element 131. Meanwhile, the fourth transistor 116 has its emitter connected to the ground via the resistance element 114 and its collector connected to the bias terminal 108 via a resistance element 132.

*Id.* ¶48.

107. *Ishimaru* explains that, at a rise time of the control voltage from the control voltage source 135, “a current transiently (temporarily) from the output terminal 118” flows into the speedup circuit 122. EX-1004 ¶52. As explained in [1.2.2] above, this current is  $I_{CORRECTION}$ . EX-1004 ¶52; *see, e.g.*:

In the speedup circuit 122, with electric charge flowing into the capacitance element 121 at a rise time of the control voltage of the

control voltage source 135 (at turn-on of the amplifier), a current transiently (temporarily) flows from the output terminal 118 into the fifth transistor 119, causing the voltage value of the output terminal 118 to lower. As a result, due to a change of the bias point of the third transistor 115, the voltage of a connecting terminal 117, which connects the collector of the third transistor 115 to the base of the bias transistor 107, transiently increases. Thus, at the rise time, the current fed to the amplifier transistor 103 by the bias transistor 107 transiently increases. Therefore, at the rise time, the power amplification factor of the amplifier transistor 103 transiently increases, so that the time elapsing until temperature variations due to heat generation of the amplifier transistor 103 come to an equilibrium on the whole circuit is shortened, with a result of reduced distortion of the amplification signal (e.g., modulated wave signal).

EX-1004 ¶52. The transient rise in  $I_{CORRECTION}$  causes the voltage at output terminal 118 to lower, which raises the voltage at the collector of transistor 115 (node 117), which controls the bias transistor 107, and this causes “the current fed to the amplifier transistor by the bias transistor 107” (*the bias signal*) to transiently increase to correct for a variation in gain of the PA when the PA is enabled. EX-1004 ¶52, *see also* ¶¶ 8-12, 31, 53-55, Figs. 2 and 3; *see, e.g.:*

According to the power amplifier of this embodiment, by electric charge flowing into the capacitance element at a rise time of the control voltage of the control voltage source (upon turn-on of the amplifier), a current transiently (temporarily) flows into the collector of the fifth

transistor, causing the voltage value of the collector to lower. As a result, due to a change of the bias point of the third transistor, the voltage of the connecting terminal at which the collector of the third transistor is connected to the base of the second transistor is temporarily increased. Thus, the current fed to the first transistor by the second transistor is transiently increased at the rise time. Therefore, the power amplification factor of the first transistor is transiently increased at the rise time, so that the time elapsing until temperature variations due to heat generation of the first transistor come to an equilibrium on the whole circuit is shortened, with a result of reduced distortion of the amplification signal (e.g., modulated wave signal).

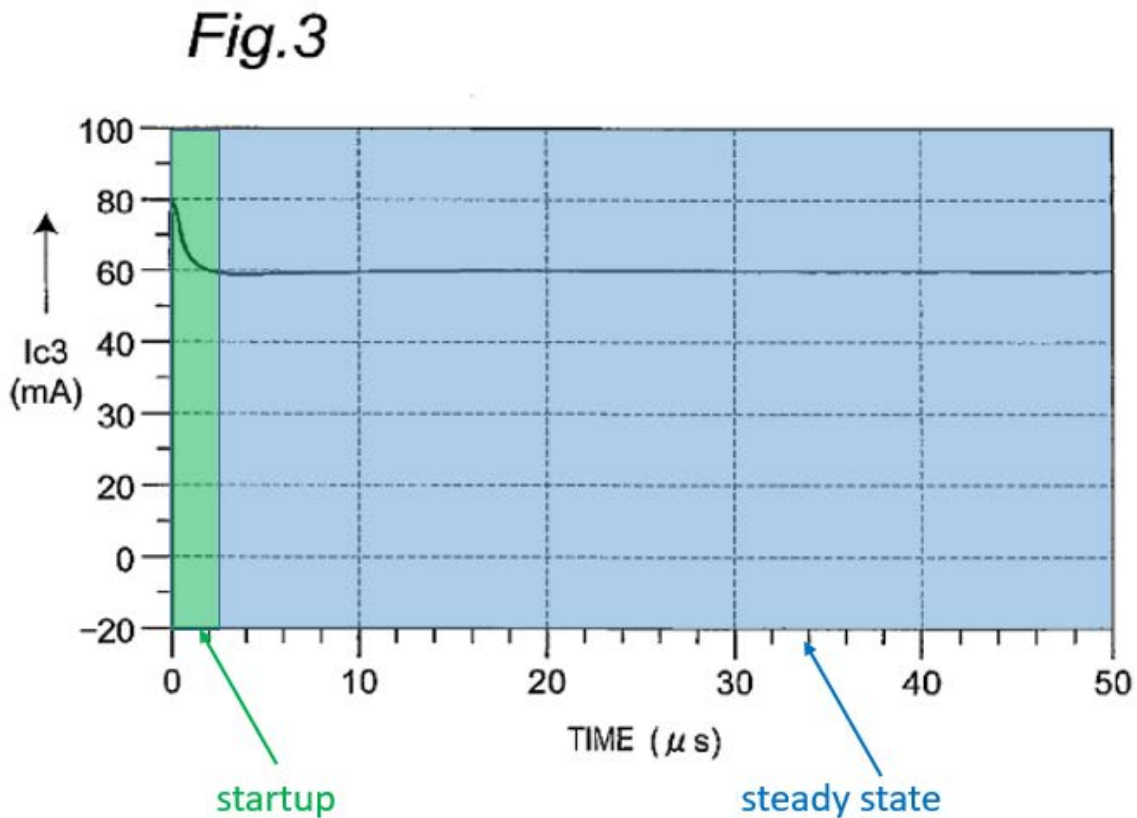
EX-1004 ¶ 31.

108. Figure 3, which shows the transient response of the collector current of the amplifier transistor 103, illustrates how the transient rise in  $I_{CORRECTION}$  causes the collector current of the amplifier transistor 103 to temporarily increase during startup to compensate for gain variations due to collector current variations of the PA using a bipolar transistor (*to correct for a variation in gain of the power amplifier when the power amplifier is enabled*). EX-1004 ¶54, Fig. 3; see, e.g.:

Next, FIG. 3 shows an example (simulation result) of transient response of the operating current (collector current  $I_{c3}$ ) of the amplifier transistor 103 in the power amplifier of this embodiment. In this embodiment, the current to be fed from the bias transistor 107 to the amplifier transistor 103 is forcedly increased at turn-on of the amplifier, with the result that the value of the operating current  $I_{c3}$  comes to a steady state in about

1/4 the time of transient response of the comparative example of FIG. 2. Thus, occurrence of distortions of the amplification signal due to temperature variations in the amplifier circuit is suppressed, so that the linearity of the circuit in burst operation is improved. That is, gain variations due to collector current variations of the power amplifier using a bipolar transistor can be compensated.

EX-1004 ¶54.



EX-1004 Fig. 3 (annotated), contrast Fig. 2, ¶ 53.

109. More specifically, the transient rise in  $I_{CORRECTION}$  causes the collector current of the amplifier transistor 103 to temporarily increase during startup to

*correct for a variation in gain of the power amplifier when the power amplifier is enabled:*

Thus, occurrence of **distortions of the amplification signal due to temperature variations in the amplifier circuit is suppressed**, so that the **linearity** of the circuit in burst operation **is improved**. That is, **gain variations** due to collector current variations **of the power amplifier using a bipolar transistor can be compensated**.

*Id.* ¶54.

110. This transient increase in the collector current of amplifier transistor 103 is due to a transient increase in  $I_{BIAS}$  (*a bias signal*) into amplifier transistor 103 because the collector current amplifies the base bias current via the amplifier transistor 103's amplification factor  $\beta$ . Further, *Ishimaru* explicitly explains that the collector current 103 (also called "operating current  $I_{c3}$ ") "comes to a steady state in about  $\frac{1}{4}$  of the time of transient response of the comparative example of Fig. 2," which is the transient response without speedup circuit 122. EX-1004 ¶¶53-54, Figs. 2 and 3; *see, e.g.:*

FIG. 2 shows an example of transient response of an operating current (collector current  $I_{c3}$ ) of the amplifier transistor 103 in a comparative example in which the speedup circuit 122 is removed in the circuit of FIG. 1. In this comparative example having no speedup circuit, due to the fact that a temperature increasing rate of the bias transistor 107 is slower than that of the amplifier transistor 103, the value of the current

fed from the bias circuit 111 to the amplifier transistor 103 continues to vary, the variations in current value making a cause of signal distortion.

EX-1004 ¶53

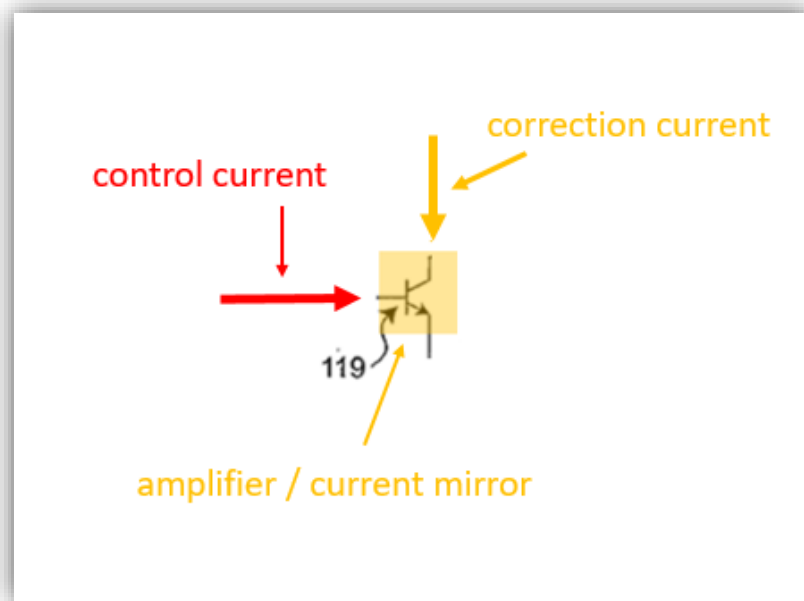
Next, FIG. 3 shows an example (simulation result) of transient response of the operating current (collector current  $I_{c3}$ ) of the amplifier transistor 103 in the power amplifier of this embodiment. In this embodiment, the current to be fed from the bias transistor 107 to the amplifier transistor 103 is forcedly increased at turn-on of the amplifier, with the result that the value of the operating current  $I_{c3}$  comes to a steady state in about 1/4 the time of transient response of the comparative example of FIG. 2. Thus, occurrence of distortions of the amplification signal due to temperature variations in the amplifier circuit is suppressed, so that the linearity of the circuit in burst operation is improved. That is, gain variations due to collector current variations of the power amplifier using a bipolar transistor can be compensated.

EX-1004 ¶54.

111. Accordingly, *Ishimaru* discloses a *primary biasing circuit* (purple) configured to generate a *bias current* (purple arrow) for the *power amplifier* (green) based at least partly on the *correction current* (gold arrow), the *bias current configured to correct for a variation in gain of the power amplifier* (purple arrow) at startup (*when the power amplifier is enabled*).

***[1.2.4] the current amplifier including a current mirror.***

112. *Ishimaru's* transistor 119 is a current amplifier. *See* [1.2.2]. Like the preferred embodiment of the '101 Patent, the current amplifier can constitute the current amplifier. *See* EX-1001 10:23. As shown in Fig. 1, partially reproduced below, *Ishimaru's* transistor 119 is a *current amplifier including a current mirror* (gold) in that transistor 119 is configured to replicate (*i.e. mirror*) and scale (amplify) the  $I_{CONTROL}$  (*red arrow*) to generate the  $I_{CORRECTION}$  (*gold arrow*).



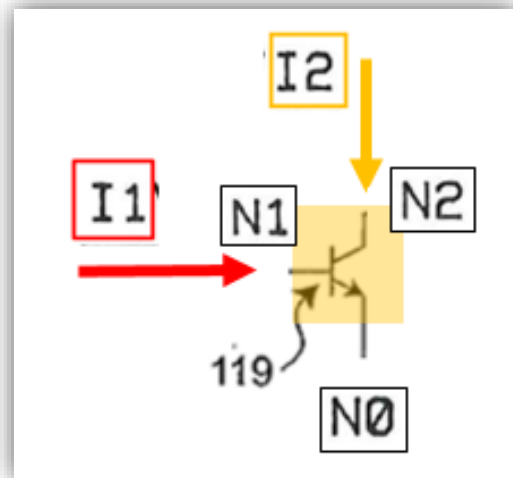
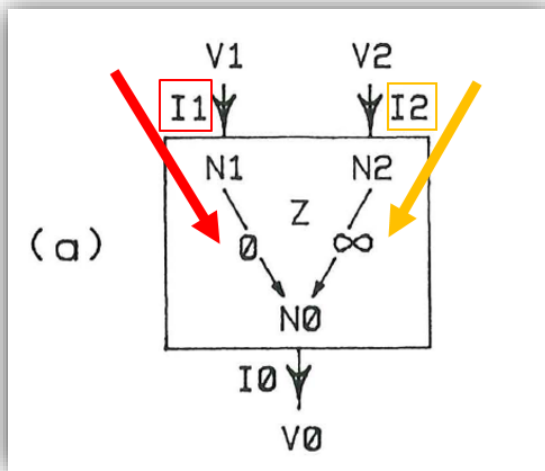
EX-1004 Fig. 1 (annotated) (partial).

113. Consistent with the discussion of current mirrors in the State of the Art section, transistor 119 as connected in *Ishimaru* is configured to mirror in that it is configured to replicate (reproduce, duplicate, reflect, etc.), *i.e., mirror* the current at its input (the base of transistor 119) to generate the current at its output (the collector of transistor 119). §IV.F.2; EX-1004 Fig. 1.

114. When connected as shown in *Ishimaru*, transistor 119 takes the general, three-node form set out by Barrie Gilbert and Gray for a *current mirror*. EX-1012 Fig. 6.1a; EX-1013 Fig. 4.1). Accordingly, in the side-by-side images below, *Ishimaru's* transistor 119 is used as a current mirror in that node N1 (of *Gilbert* Figure 6.1a showing a current mirror) is the base of transistor 119, N2 the collector of transistor 119, and N0 the emitter of transistor 119, with the circuit replicating (and scaling) current I1 to generate output current I2. EX-1012 242, Fig. 6.1a; EX-1013 Fig. 4.1; *see, e.g.:*

In the simplest possible scenario, a single BJT can be used as a mirror: node N1 (of Figure 6. 1a) is the base, N2 the collector and N0 the emitter. Of course, the practical objection to this proposal is that the mirror ratio,  $M$ , is much higher than generally needed and poorly-controlled, being just the common-emitter current-gain,  $\beta$ , and not very linear. While these objections are all true, it is nevertheless useful to begin here, because we will discover that many of the properties of more familiar mirrors can be predicted from the behavior of the single transistor circuit.

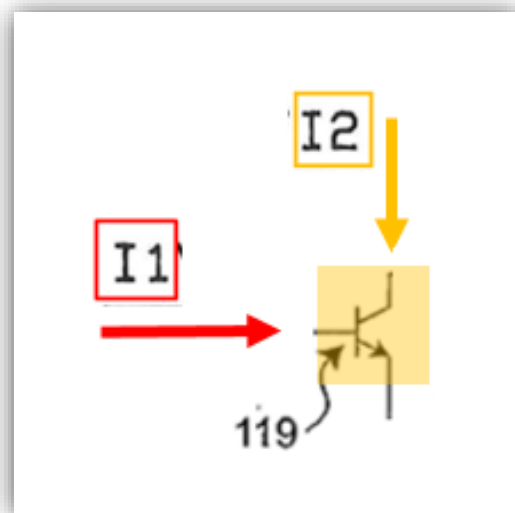
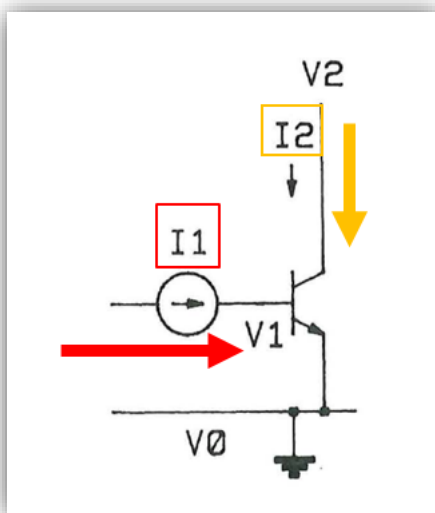
EX-1012 242.



EX-1012 240, Fig. 6.1a (annotated)

EX-1004 Fig. 1 (annotated)(partial)

115. Likewise, *Ishimaru's* transistor 119 is connected and used in the same way as *Gilbert's* single transistor current mirror shown of his Figure 6.2a:



EX-1012 243, Fig. 6.2a (annotated)

EX-1004 Fig. 1 (annotated)(partial)

116. In addition to the replication discussed above, *Ishimaru's* current mirror is further configured to **amplify** the  $I_{CONTROL}$ , scaling it up by the amplification factor, namely scaling by the common-emitter current-gain,  $\beta$ , of the

transistor 119, which quantifies the “mirror ratio” (discussed below) of *Ishimaru’s* current mirror. §IV.F.2, EX-1015 38; EX-1012 242-243; *see, e.g.:*

**beta current gain factor** *Syn.* common-emitter forward-current transfer ratio; forward current gain. Symbol:  $\beta$ . The short-circuit current-amplification factor in a bipolar transistor with ► common-emitter connection:  $\beta = \alpha I_c / \alpha I_B$   $V_{CE}$  constant where  $I_c$  is the collector current and  $I_B$  is the base current; the collector voltage,  $V_{CE}$ , is constant.  $\beta$  is always greater than unity and practical values up to 500 are used.

EX-1015 38.

In the simplest possible scenario, a single BJT can be used as a mirror: node N1 (of Figure 6. 1a) is the base, N2 the collector and N0 the emitter. Of course, the practical objection to this proposal is that the mirror ratio,  $M$ , is much higher than generally needed and poorly-controlled, being just the common-emitter current-gain,  $\beta$ , and not very linear. While these objections are all true, it is nevertheless useful to begin here, because we will discover that many of the properties of more familiar mirrors can be predicted from the behavior of the single transistor circuit.

Figure 6.2a shows the biasing for an NPN device. We wish to determine the input and output resistances. It will be assumed that  $\beta$  is independent of current over the range of interest. If  $\beta$  were also independent of  $V_2$ , the output  $I_2$  would always be simply  $\beta I_1$  and the output resistance  $r_o$  would be infinite. In fact,  $\beta$  increases with  $V_2$  due to base-width modulation, and in the customary BJT model would be exactly doubled

when the collector bias voltage,  $V_{CB}$  (roughly,  $V_2$ ), is equal to the forward Early voltage,  $V_{AF}$ .

EX-1012 242-243. The current at the collector ( $I_{C119}$ ) of transistor 119 (a transistor having  $\beta_{119}$ ) is generally related to the current at the transistor's base ( $I_{B119}$ ) by the equation:  $I_{C119} = \beta_{119} * I_{B119}$ . *Id.*; EX-1004 Fig. 1. Thus, the ratio of the input current  $I_{B119}$  to the output current  $I_{C119}$  is generally  $\beta_{119}$ . EX-1004 Fig. 1. The gain through the transistor is the “mirror ratio”, “M”, by which *Ishimaru's current mirror* scales the  $I_{CONTROL}$  to generate the  $I_{CORRECTION}$  EX-1012 242-243; EX-1004 Fig. 1. The gain of transistor 119 can be configured to a target value by designing the voltage and current biasing of the transistor 119 (within the constraints of the circuit), such that a  $\beta$  in a range, *e.g.*, of about 60 to 150 or more, can be achieved. The time constant of the transient can then be tuned through the choice of components, namely C121 and R136. EX-1004 ¶¶ 55-56. EX-1004 ¶¶ 55-56; *see also, infra*, Claim 2; *see, e.g.*:

In the power amplifier of this embodiment also, the capacitance value of the capacitance element 121 of the speedup circuit 122 is adjusted so as to cancel transient variations in gain due to the temperature variations at a start of power amplification. As a result of this, deterioration of the linearity due to variations of amplification gain can be canceled so that the value of dynamic EVM (error vector magnitude) can be improved.

EX-1004 ¶55.

In addition, the capacitance element 121 of the speedup circuit 122 may be a capacitance element whose capacitance value is changeable. In this case, changing the capacitance value of the capacitance element 121 makes it possible to adjust the time duration during which the bias fed to the amplifier transistor 103 at a start of amplification operation by the speedup circuit 122 via the bias power source section composed of the power source circuit 112 and the bias circuit 111 is kept increased.

EX-1004 ¶56.

117. Thus, transistor 119 as connected in *Ishimaru* is a *current mirror* in that it constitutes a circuit configured to mirror a current, which can be configured to achieve a target gain. Transistor 119 is a circuit that has electrical interconnections, including input, output, and other connections that permit current to flow through the circuit. EX-1020 2; *see, e.g.*:

Plain meaning, such as “one or more circuits configured to mirror a current, which can be configured to achieve a target gain”

EX-1020 2.

## **Claim 2**

***[2] The power amplifier system of claim 1 wherein the time-dependent signal generator includes a resistor-capacitor (RC) network.***

118. *Ishimaru* discloses this limitation. As illustrated in Figure 1, *Ishimaru*'s PA system includes a speedup circuit (dark blue) that includes a *time-dependent signal generator* (red) that “transiently (temporarily) increases” the  $I_{BIAS}$

fed to the amplifier transistor by the bias circuit during the period after startup.

EX-1004 ¶13; *see, e.g.:*

According to the power amplifier of this invention, at a start of power amplification by the first transistor of the amplification section, the speedup circuit transiently (temporarily) increases the bias fed to the first transistor by the bias power source section, so that the power amplification factor of the first transistor is transiently increased at the start of power amplification. Thus, the time elapsing until temperature variations due to heat generation of the first transistor (amplifier transistor) that performs the power amplification come to an equilibrium on the whole circuit is shortened, with a result of reduced distortion of the amplification signal (e.g., modulated-wave signal).

EX-1004 ¶13. Speedup circuit 122 includes transistors 119, 120, *resistor* 136, as well as a *capacitor* 121 connected between the base of transistor 120 and bias terminal 108. *Id.* ¶¶50-51, 55-56; *see, e.g.:*

The speedup circuit 122 has a fifth transistor 119 whose collector is connected to the output terminal 118, and a sixth transistor 120 whose emitter is connected to a base of the fifth transistor 119. The emitter of the fifth transistor 119 is connected to the ground via a resistance element 136.

EX-1004 ¶50.

The speedup circuit 122 also has a capacitance element 121 which is connected between a base of the sixth transistor 120 and the bias

terminal 108, and two diodes 125, 126 which are connected in series between the base of the sixth transistor 120 and the bias terminal 108.

EX-1004 ¶51. The charging time of capacitor 121 depends on the size of the capacitor and the resistance through R136 to ground, which sets the shape of the control current from the speedup circuit 122. *Id.* ¶¶55-56; *see, e.g.:*

In the power amplifier of this embodiment also, the capacitance value of the capacitance element 121 of the speedup circuit 122 is adjusted so as to cancel transient variations in gain due to the temperature variations at a start of power amplification. As a result of this, deterioration of the linearity due to variations of amplification gain can be canceled so that the value of dynamic EVM (error vector magnitude) can be improved.

EX-1004 ¶55

In addition, the capacitance element 121 of the speedup circuit 122 may be a capacitance element whose capacitance value is changeable. In this case, changing the capacitance value of the capacitance element 121 makes it possible to adjust the time duration during which the bias fed to the amplifier transistor 103 at a start of amplification operation by the speedup circuit 122 via the bias power source section composed of the power source circuit 112 and the bias circuit 111 is kept increased.

EX-1004 ¶56. A POSITA understands that this speedup circuit forms an *RC network*.

119. More specifically, a POSITA understands that *Ishimaru* applies a large current amplification (by virtue of transistors 119, and 120)<sup>2</sup> to the transient current controlled by “capacitance element 121.” EX-1004 ¶¶52, 55-56, Fig. 1 (capacitor 121, transistors 119 and 120, and resistor 136); *see, e.g.*:

In the speedup circuit 122, with electric charge flowing into the capacitance element 121 at a rise time of the control voltage of the control voltage source 135 (at turn-on of the amplifier), a current transiently (temporarily) flows from the output terminal 118 into the fifth transistor 119, causing the voltage value of the output terminal 118 to lower. As a result, due to a change of the bias point of the third transistor 115, the voltage of a connecting terminal 117, which connects the collector of the third transistor 115 to the base of the bias transistor 107, transiently increases. Thus, at the rise time, the current fed to the amplifier transistor 103 by the bias transistor 107 transiently increases. Therefore, at the rise time, the power amplification factor of the amplifier transistor 103 transiently increases, so that the time elapsing until temperature variations due to heat generation of the amplifier transistor 103 come to an equilibrium on the whole circuit is shortened, with a result of reduced distortion of the amplification signal (e.g., modulated wave signal).

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<sup>2</sup> Each transistor has an amplification factor, “ $\beta$ ” that relates the transistor’s base current to its collector current. (e.g. EX-1015 38).

EX-1004 ¶52. When the enable signal turns on, capacitor 121 charges by virtue of current flowing through transistor 119, transistor 120 and resistor 136 to ground. Owing to the very high gain of transistors 119 and 120, the current in the capacitor can be made very small, and therefore the capacitor 121 can be made small for a given time constant. Likewise, the size of resistor 136 can be small as the capacitor current ( $I_{C121}$ ) is generally the resistor current ( $I_{R136}$ ) divided by the gain of transistors 119 and 120. In *Ishimaru*, a physically small resistor can be used for R136 as its current when traced back to C121, will be greatly reduced by the gain of 119 and 120. Increasing the size of R136, or the size of C121, will slow the rate at which C121 charges, providing the circuit with a time-dependent signal that has a longer time constant. Conversely, a smaller C121 and/or R136 will allow the capacitor to charge more rapidly, providing a time-dependent signal that reaches steady state more quickly. Thus, *Ishimaru's time-dependent signal generator* includes a resistor-capacitor (RC) network that includes capacitor 121 and resistor 136.

### **Claim 10**

***[10] The power amplifier system of claim 1 wherein the power amplifier includes a bipolar transistor having an emitter, a base and a collector, the base configured to receive the RF signal and the bias current.***

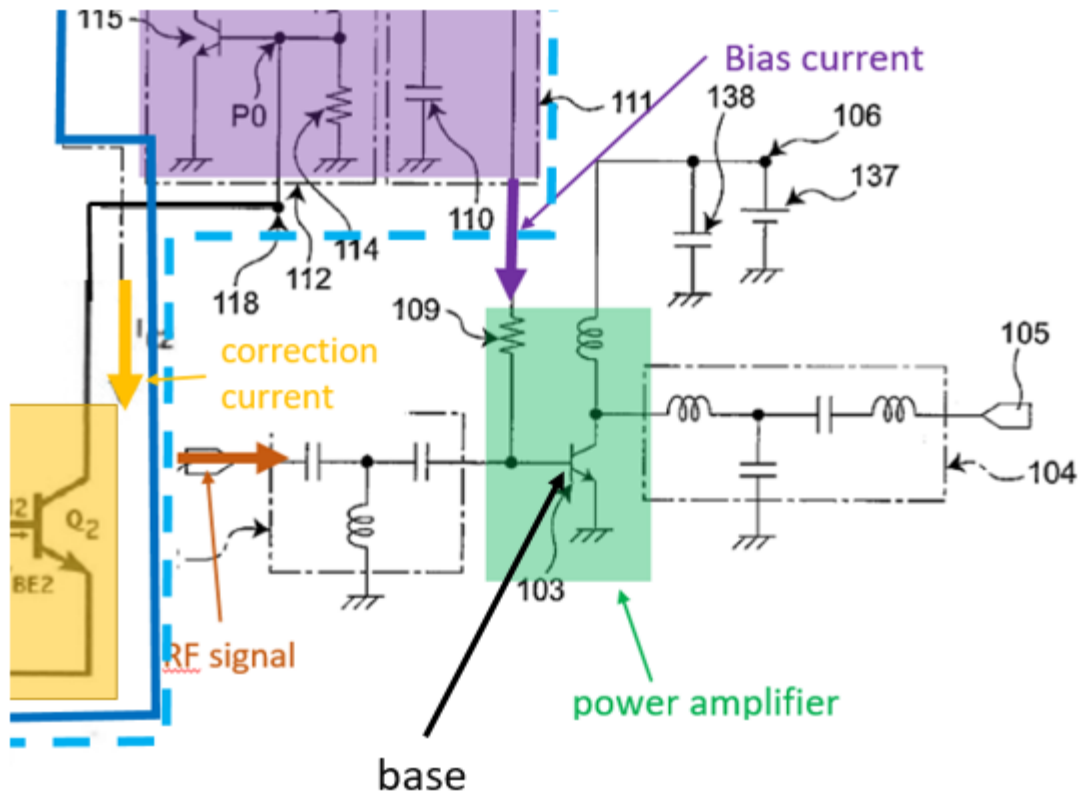
120. *Ishimaru* discloses this limitation. *Ishimaru* discloses that transistor 103 is a bipolar transistor. EX-1004 ¶¶54, 55. EX-1004 ¶¶54, 55. In *Ishimaru*,

the base of transistor 103 receives the “high-frequency signal” for “radio communication devices” from terminal 101 (*where the base is configured to receive the RF signal*) and bias transistor 107 “supplies a base bias current to a base terminal of the amplifier transistor 103” (*the base receives the bias current*).

EX-1004 ¶¶41-42; *see, e.g.:*

In this power amplifier, a high-frequency signal as an input signal inputted from an input signal terminal 101, passing through an input matching circuit 102, is amplified by an amplifier transistor 103 serving as a first transistor, and then, after passing through an output matching circuit 104, outputted from an output signal terminal 105. In FIG. 1, reference sign 106 denotes a collector bias terminal of the amplifier transistor 103. Between the collector bias terminal 106 and the ground are connected a DC power source 137 and a capacitance element 138. The amplifier transistor 103 forms an amplification section.

EX-1004 ¶42. As illustrated in the annotated portion of Figure 1 below, the base of transistor 103 receives *the RF signal* (brown arrow) and the *bias current* (purple arrow):



EX-1004, FIG 1 (partial) (annotated); see §IV.F.1 (showing BJT terminals).

**Claim 11**

*[11] The power amplifier system of claim 10 wherein the emitter is electrically connected to a power low voltage and the collector is configured to generate an amplified version of the RF signal.*

121. *Ishimaru* discloses this limitation. Figure 1 shows an input signal terminal 101 that receives a high-frequency signal (brown arrow) as an input signal, and this input signal passes through an input matching circuit 102, and is then amplified by amplifier transistor 103 (green). The amplifier transistor 103 outputs a signal through output matching circuit 104 to output signal terminal 105

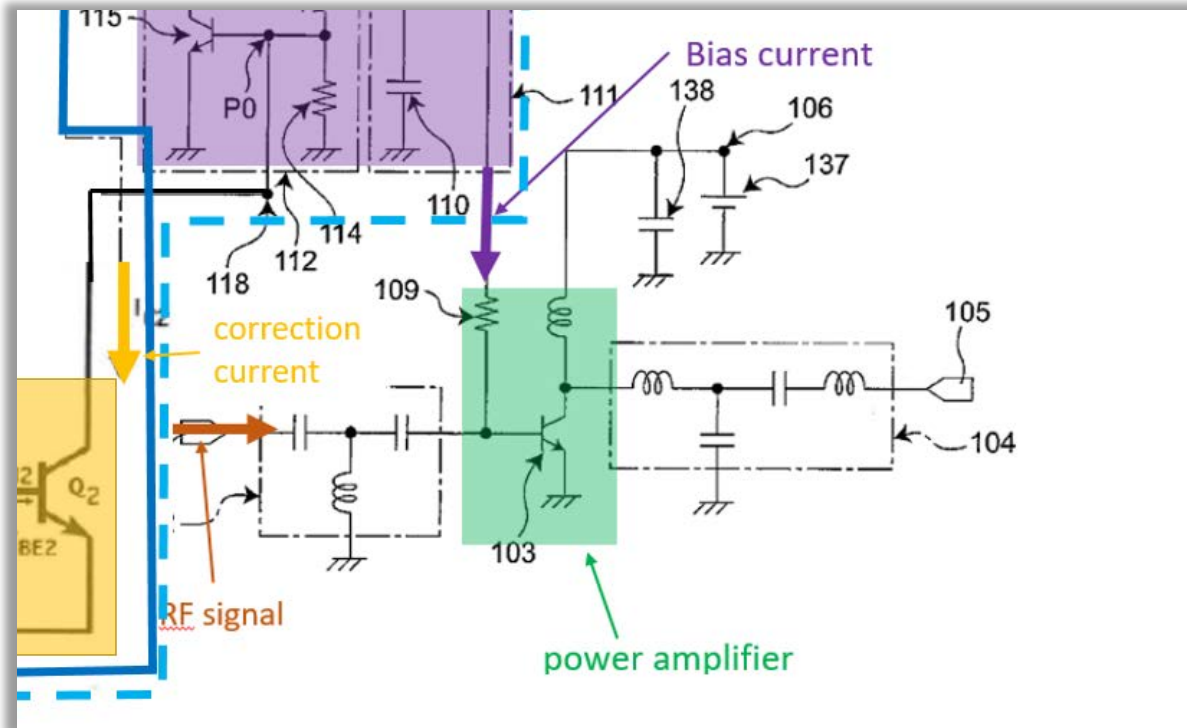
as an amplified version of the RF input signal (*the collector is configured to generate an amplified version of the RF signal*). EX-1004 ¶¶41-43, 46, 49; see, *e.g.*:

In this power amplifier, a high-frequency signal as an input signal inputted from an input signal terminal 101, passing through an input matching circuit 102, is amplified by an amplifier transistor 103 serving as a first transistor, and then, after passing through an output matching circuit 104, outputted from an output signal terminal 105. In FIG. 1, reference sign 106 denotes a collector bias terminal of the amplifier transistor 103. Between the collector bias terminal 106 and the ground are connected a DC power source 137 and a capacitance element 138. The amplifier transistor 103 forms an amplification section.

EX-1004 ¶42.

A power source circuit 112 is connected to the base terminal of the bias transistor 107 of the bias circuit 111. The bias circuit 111 and the power source circuit 112 constitute a bias power source section.

EX-1004 ¶46.



EX-1004, FIG 1 (partial) (annotated).

122. Figure 1 further illustrates that the emitter of transistor 103 is electrically connected to Ground which a POSITA understood was a *power low voltage*. *Ishimaru's* disclosure is consistent with the disclosure of the '101 Patent, in which the emitter of the bipolar transistor 61 is likewise connected to ground.

EX-1001 7:45-51, Fig. 3B; *see, e.g.:*

The illustrated power amplifier 32 includes a bipolar transistor 61 having an emitter, a base, and a collector. The emitter of the bipolar transistor 61 can be electrically connected to a first or power low voltage  $V_1$ , which can be, for example, ground, and a radio frequency input signal RF\_IN can be provided to the base of the bipolar transistor 61 through the first capacitor 42.

**Claim 17**

***[17.0] A method of biasing a power amplifier, the method comprising:***

123. To the extent the preamble is limiting, *Ishimaru* discloses this limitation for the same reasons as discussed with respect to limitation [1.2].

***[17.1] shaping an enable signal using a time-dependent signal generator to generate a control current;***

124. *Ishimaru* discloses this limitation for the same reasons as discussed with respect to limitation [1.2.1].

***[17.2] amplifying the control current using a current mirror of a current amplifier to generate a correction current; and***

125. *Ishimaru* discloses this limitation for the same reasons as discussed with respect to limitations [1.2.2] and [1.2.4].

***[17.3] generating a bias current for a power amplifier using a primary biasing circuit, the primary biasing circuit configured to use the correction current to correct for a variation in gain of the power amplifier when the power amplifier is enabled.***

126. *Ishimaru* discloses this limitation for the same reasons as discussed with respect to limitation [1.2.3].

**Claim 18**

***[18] The method of claim 17 wherein shaping the enable signal includes using a resistor-capacitor (RC) network of the time-dependent signal generator.***

127. *Ishimaru* discloses this limitation for the same reasons as discussed with respect to Claim 2.

### **Claim 20**

***[20]. The method of claim 17 wherein generating the bias current includes shaping the bias current so as to compensate for a gain variation of a heterojunction bipolar transistor (HBT).***

128. *Ishimaru* discloses this limitation for the reasons as discussed with respect to Claim 10 and [1.2.3], and further in view of the general knowledge in the art concerning HBT transistors. *See* §IV.F.3.

129. As discussed for claim 10 and [1.2.3], *Ishimaru* discloses shaping the bias current to compensate for a gain variation of the BJT used for its PA transistor 103 for radio communication devices. *See* Claim 10 and [1.2.3]; EX-1004 ¶¶ 1, 54, 55; *see, e.g.:*

Next, FIG. 3 shows an example (simulation result) of transient response of the operating current (collector current  $I_{c3}$ ) of the amplifier transistor 103 in the power amplifier of this embodiment. In this embodiment, the current to be fed from the bias transistor 107 to the amplifier transistor 103 is forcedly increased at turn-on of the amplifier, with the result that the value of the operating current  $I_{c3}$  comes to a steady state in about 1/4 the time of transient response of the comparative example of FIG. 2. Thus, occurrence of distortions of the amplification signal due to temperature variations in the amplifier circuit is suppressed, so that the linearity of the circuit in burst operation is improved. That is, gain

variations due to collector current variations of the power amplifier using a bipolar transistor can be compensated.

EX-1004 ¶ 54.

130. A POSITA would understand *Ishimaru*'s solution to apply to all types of BJT processes for PAs for such radio communications devices, of which heterojunction bipolar transistors (HBT) were a popular, market-leading form for RF PAs. *See* §IV.F.3. As explained in the State of the Art, it was part of the general knowledge in the art to use the HBT form of BJT, as was widely done and well documented, for bipolar junction transistor implementations of RF PAs. *Id.* This is because HBTs were an improved form of BJTs, with well-documented advantages for RF power amplification, including, *e.g.*, having the robustness, speed, density, and linearity necessary for such circuits. §IV.F.3.

131. While *Ishimaru* does not expressly refer to the use of HBTs, that is nonetheless understood by a POSITA for several reasons. First, *Ishimaru* expressly discloses a solution for RF PAs implemented as BJTs, and a POSITA would reasonably draw the inference that *Ishimaru* disclosed the use of its solution for the market leading forms of such BJTs, namely HBTs. §IV.F.3. Indeed, it was conventional to use HBTs in the context of radio communication devices having RF PAs using BJT transistors like *Ishimaru*'s. Second, *Ishimaru* is directed to an incremental improvement in the startup behavior of BJT-based RF PAs that is

directed at the margin of high performing devices, *i.e.*, the type of BJT-based RF PAs commonly implemented as HBTs. A POSITA understood that HBTs, as BJTs, suffer the same thermal effects described by *Ishimaru*, and would likewise benefit in the same way as other BJTs. For these reasons, a POSITA reading *Ishimaru* in 2011 understood that *Ishimaru's* “radio communication device” with its PA (green) and bias circuits (blue) would be implemented in *an integrated circuit attached to a package substrate in a packaged module* as claimed. Thus, while not explicitly stated, the HBT form claimed is nonetheless disclosed to a POSITA in view of the reasonable inferences that a skilled artisan would draw when reading *Ishimaru*.

132. To the extent that Patent Owner argues that a POSITA would not have drawn the reasonable inference that *Ishimaru's* PA would employ BJTs using the market-leading HBT form, that would have at minimum been obvious to a POSITA in view of the general knowledge in the art, for the same reasons discussed above and evidenced by the well-known advantages of HBTs for RF PAs. §IV.F.3. A POSITA would have been motivated to use an HBT for *Ishimaru's* BJT PA 103 to achieve any one of a host of known benefits such as their “improvement in the high frequency performance of the transistor” (EX-1015), their “inherently superior linearity and efficiency performance” (EX-1017), their “reliability [being] well known to be excellent” (EX-1017), and other

advantages in cost, size, robustness, *etc.* (EX-1008, EX-1025). §IV.F.3. A POSITA would have been motivated to implement at least the PA of *Ishimaru* as an HBT following these well-documented advantages. *Id.* Doing so would involve nothing more than using a market-leading prior art technique (using HBT type of BJT-based RF PAs) according to conventional wisdom for the benefits and successes confirmed by the market and reported by others. Finally, there would have been nothing technologically counterintuitive about implementing *Ishimaru*'s PA system with an HBT as compared to other forms of a BJT. Indeed, the '101 Patent references HBTs in passing, without any special significance, criticality, challenges, or counterintuitive concepts or properties. EX-1001 7:53-55; *see, e.g.:*

In one implementation, the bipolar transistor 61 is a heterojunction bipolar transistor (HBT).

EX-1001 7:53-55. This lack of detail is consistent with the well-developed state of the art for HBT RF PAs. §IV.F.3. Furthermore, given *Ishimaru*'s teachings, the selection of a market-leading BJT type (HBT) would have been viewed with a reasonable expectation of success with predictable benefits, all well within the skill of a POSITA as demonstrated by the popularity of HBTs in the marketplace.

§IV.F.3.

### **Claim 21**

***[21.0] A bias circuit for biasing a power amplifier, the bias circuit comprising:***

133. To the extent that the preamble is limiting, *Ishimaru* discloses a bias circuit (light blue) as illustrated in Figure 1, as discussed in limitation [1.2].

***[21.1] a time-dependent signal generator configured to shape an enable signal of the power amplifier to generate a control current;***

134. *Ishimaru* discloses this limitation for the same reasons as discussed with respect to limitation [1.2.1].

***[21.2] a current amplifier configured to amplify the control current to generate a correction current, the current amplifier including a current mirror; and***

135. *Ishimaru* discloses this limitation for the same reasons as discussed with respect to limitation [1.2.2] and [1.2.4].

***[21.3] a primary biasing block configured to generate a bias current for the power amplifier based at least partly on the correction current, the bias current configured to correct for a variation in gain of the power amplifier when the power amplifier is enabled.***

136. *Ishimaru* discloses this limitation for the same reasons as discussed with respect to limitation [1.2.3].

## **Claim 22**

***[22] The bias circuit of claim 21 wherein the time-dependent signal generator includes a resistor-capacitor (RC) network.***

137. *Ishimaru* discloses this limitation for the same reasons as discussed with respect to Claim 2.

**B. Ground 2: Claims 1-2, 10-11, 17-18, and 20-22 Are Obvious over *Ishimaru* in View of *Harrison***

138. Ground 2 is submitted to address Patent Owner’s claim construction of *current mirror* that differs from Petitioner’s plain meaning in that Patent Owner’s construction adds the limitations that the *current mirror* must have “at least two transistors with their base or gate terminals tied together.” While I maintain the State of the Art (§IV.F.2) demonstrates that a POSITA understood that a *current mirror* is not limited to any specific number or configuration of transistors, Ground 2 discloses a current mirror even under Patent Owner’s claim construction. In such circumstances, I understand from counsel that the Board need not construe a claim term.

139. Ground 2 is identical to Ground 1 except for limitations [1.2.4] and [21.2] which recite that *the current amplifier including a current mirror*, and limitation [17.2] that recites *amplifying the control current using an current mirror*. All other limitations are disclosed by *Ishimaru* as discussed with respect to Ground 1 set forth above.

**1. *Harrison***

140. *Harrison* is a book titled “Current Sources & Voltage References” and its Chapter 4 is titled “Using BJTs to Create Current Sources.” EX-1006 47. *Harrison* explains that a bipolar junction transistor (or “BJT”) is a “current-

operated semiconductor device” with “three terminals that are designated the base, the collector, and the emitter.” *Id.* 49.

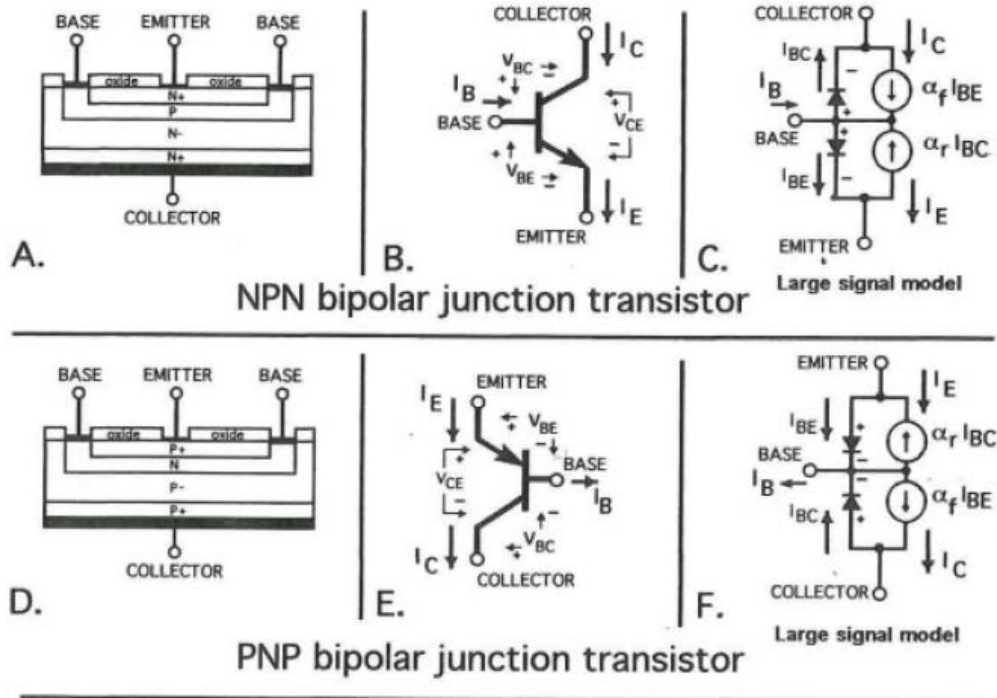


Figure 4.2. Showing the structure of the BJT, as well as its various voltages, currents, and polarities. Notice the two inherent diodes that provide forward and reverse bias.

EX-1006 50, Fig. 4.2.

141. *Harrison* explains that “simple current sources” using bipolar analog transistors were used starting in the late 1960s “for purposes of biasing and stability” and analog circuit designers “found a reliable method of biasing their circuits and thereby improving the overall quality and accuracy of their products.”

*Id.* 68; see, e.g.:

When the silicon bipolar analog IC became a practical reality in the late 1960s, simple current sources began to be used in their architectures for purposes of biasing and stability. Their performances far outperformed

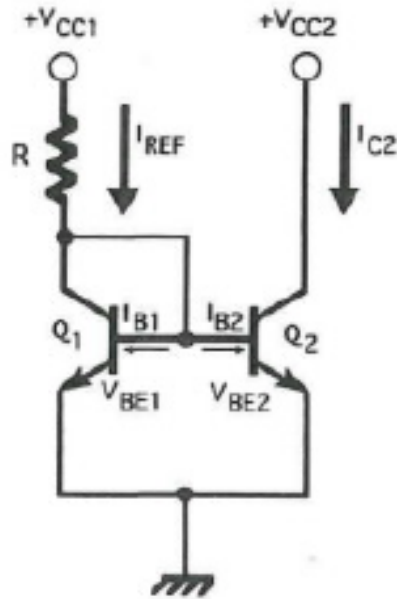
their discrete predecessors, because all of the necessary components were integrated into the chip's design. As a result, much development focused on creating current sources for bipolar circuits between the mid-60s and the early '80s. At last, analog designers had found a reliable method of biasing their circuits and thereby improving the overall quality and accuracy of their products. As other technologies have since evolved, such as complimentary-bipolar (CB), analog CMOS, and gallium arsenide (GaAs) RF amplifiers, current sources were used in them also, with similarly good results.

*Id.* 68. *Harrison* further explains that “virtually all BJT current sources are configured as *current mirrors* (aka current reflectors), where an input current is mirrored at the output, in either a matched 1:1 or other ratio.” *Id.* 70.

Some other devices, such as the JFET, the current regulator diode (CRD), and the power MOSFET, can result in a two-lead current source configuration, but any worthwhile BJT current source requires an input terminal, an output terminal, and a voltage bias point. In some configurations, four terminals are needed. As a result, virtually all BJT current sources are configured as *current mirrors* (aka current reflectors), where an input current is mirrored at the output, in either a matched 1 :1 or other ratio. This may be either a fraction or a multiple of the input, or scaled in some other manner.

*Id.* 70. *Harrison* is from the same field of art as the '101 Patent because it describes the operation of analog circuit components, such as bipolar junction transistors, that are used in RF electronics and PAs; *see, e.g.:*

142. *Harrison* illustrates simple two-transistor current source designs using BJT NPN transistors:

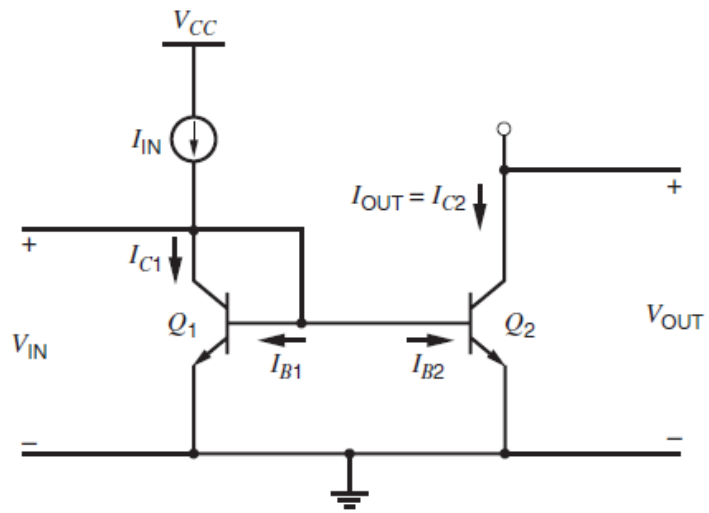


Basic NPN Current sink

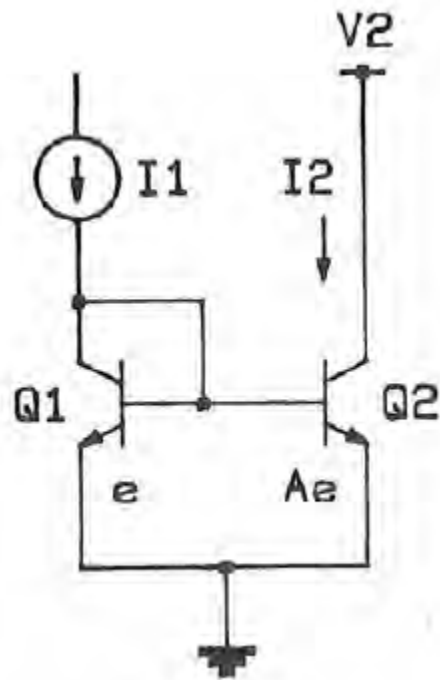
Figure 4.18. Basic BJT current mirrors.

EX-1006 Fig. 4.18 (reproduced in part), 71 (“reference current,  $I_{REF}$ , will be mirrored (duplicated)”).

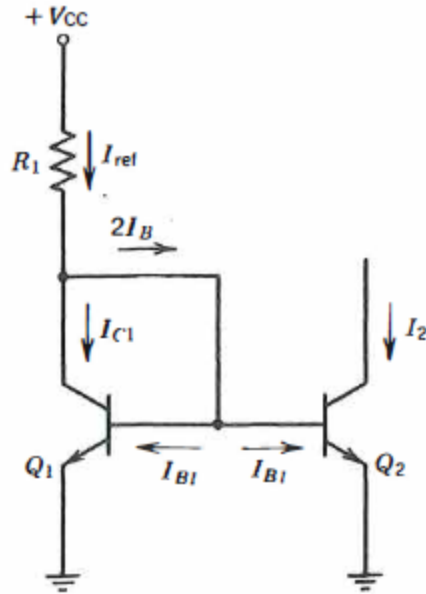
143. *Harrison's* two-transistor current mirror shown and described in Fig. 4.18 was a widely understood circuit, well established in the general knowledge of a POSITA. §IV.F.2; EX-1013 251-54, 257, Fig. 4.2; EX-1012 251, 280, Fig. 6.7(a); EX-1014 171. *Harrison* is exemplary of that general knowledge.



EX-1013 Figure 4.2.



EX-1012 Figure 6.7.



EX-1012 Figure 4.1.

2. Detailed Application of *Ishimaru* in View of *Harrison* to the Challenged Claims

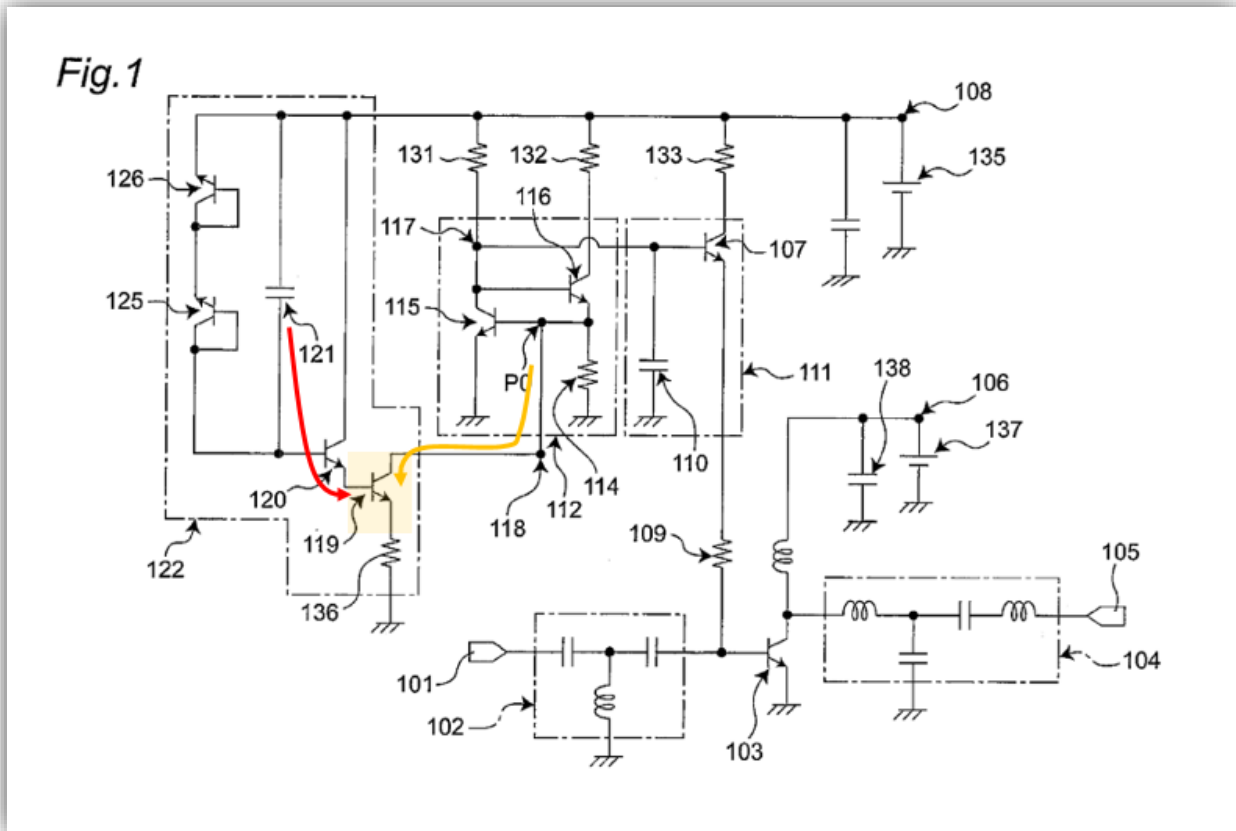
**Claim 1**

*[1.2.4] the current amplifier including a current mirror.*

144. To the extent Patent Owner argues that *Ishimaru* does not disclose a *current mirror*, *Ishimaru* in view *Harrison* discloses this limitation.

145. As discussed in Ground 1, *Ishimaru* discloses a speedup circuit 122 that responds at “a rise time of the control voltage of the control voltage source 135 (at turn-on of the amplifier)” to generate a time-varying current via capacitor 121 that is amplified by and 119 (*current amplifier*). §V.C. Furthermore, as illustrated in the annotated Figure 1, below, a POSITA recognizes that *Ishimaru* uses the

amplified version of the current (red arrow) as a current sink to pull a specifically shaped  $I_{CORRECTION}$  (gold arrow) out of the primary biasing circuit.



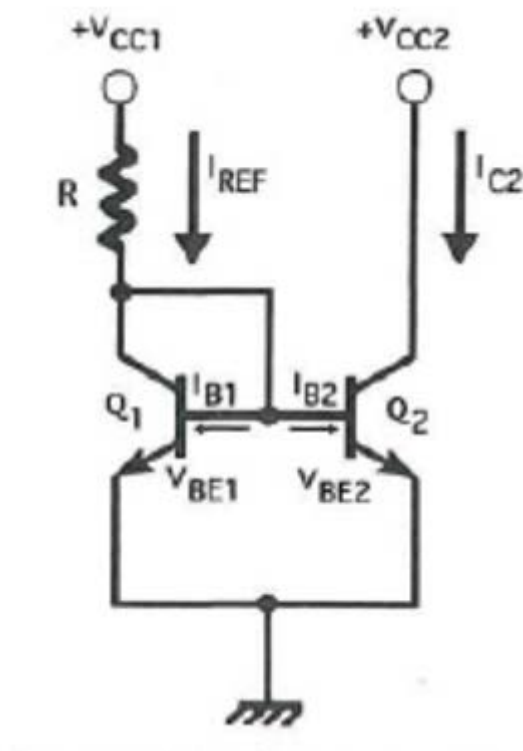
EX-1004 Fig. 1 (annotated).

146. A POSITA readily recognizes the coupling of the left and right sides of *Ishimaru's* circuit as involving a current source generated on the left side that is replicated as a current sink on the right side, which is a coupling that takes the general form of a *current mirror* (i.e. transistor 119 as discussed in Ground 1).

147. A POSITA further recognizes that the current source / current sink coupling of *Ishimaru* would be well suited for, and ready for improvement by, the

use of additional current mirror structures to couple the two sides of *Ishimaru's* circuit to achieve the well-known benefits of such current mirrors.

148. In that regard, *Harrison* teaches a well-known “basic” current mirror using NPN transistors that operates as a “mirror-sink,” as shown in the excerpt of Figure 4.18 below:



EX-1006 71; Fig. 4.18.

149. As can be seen in Figure 4.18 above, this current mirror also satisfies Patent Owner’s proposed construction of current mirror in that it has at least two transistors (Q1 and Q2) with their base terminals tied together. EX-1020 2; EX-1006 71, Fig. 4.18; *see, e.g.:*

In both current mirror circuits,  $Q_1$ 's base and collector are shorted together, while the base and emitter act as a diode. The series resistor,  $R_1$ , provides a fixed voltage and current to  $Q_1$ 's collector, as well as base current for  $Q_1$  and  $Q_2$ . In the NPN circuit, because  $Q_1$ 's collector and base are shorted, and its emitter is grounded, this clamps the  $V_{BE}$  at approximately 0.65 volt above ground.

EX-1006 71. Furthermore, the basic current mirror above is a circuit configured to mirror  $I_{REF}$  to  $I_{C2}$ , and is configurable to achieve a target gain that can be finely tuned by adjusting the ratio of the transistor sizes. EX-1006 95 (describing “current scaling” by setting the ratio of the emitter area); *see also* EX-1012 280; EX-1013 254, 257; EX-1014 172; *see, e.g.:*

With the exception of the Widlar and the Wyatt current sources, up until now we have looked at current sources that generate input-to-output currents in a 1:1 ratio, but it is often necessary to generate integer multiples or fractions on an initial current. For the IC designer this is accomplished in the design by creating transistors with multiple emitters, or with bulk emitter area ratioed in either greater or lesser amounts. In this way a current can be made, say, 10 times or one-tenth of the initial input current. It is sometimes depicted in a manufacturer's circuit schematic as a number written next to the particular emitter (see Figure 4.22D). It is sometimes shown, for example, as 10E or 10A.

For the board-level designer, generating multiples or fractions of an initial current can be accomplished in different ways. One way to do

this is by paralleling individual transistors as shown in the following circuits, in what is known as *current scaling*.

EX-1006 95.

There is no particular difficulty in achieving high mirror ratios. In many cases, simple emitter area ratios will suffice, supported by current gain if necessary (as in the EFA mirror, which is not limited to the use of a single transistor for current boosting). In practical monolithic designs, emitter area ratios of up to 100:1 are not hard to achieve.

EX-1012 280.

Since the saturation current of a bipolar transistor is proportional to its emitter area, the first term in (4.6) shows that the gain of the current mirror can be larger or smaller than unity because the emitter areas can be ratioed. If the desired current-mirror gain is a rational number,  $M/N$ , the area ratio is usually set by connecting  $M$  identical devices called *units* in parallel to form  $Q_2$  and  $N$  units in parallel to form  $Q_1$  to minimize mismatch arising from lithographic effects in forming the emitter regions.

EX-1013 254.

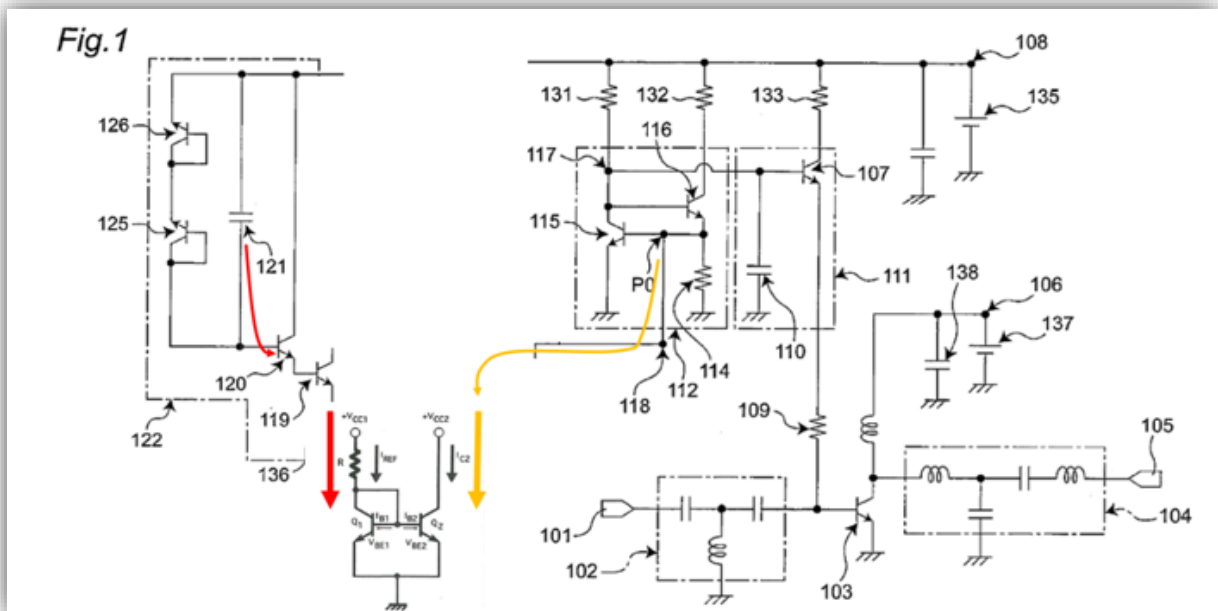
Equation 4.17 shows that the gain of the current mirror can be larger or smaller than unity because the transistor sizes can be ratioed. To ratio the transistor sizes, either the widths or the lengths can be made unequal in principle. In practice, however, the lengths of  $M_1$  and  $M_2$  are rarely made unequal.

EX-1013 257.

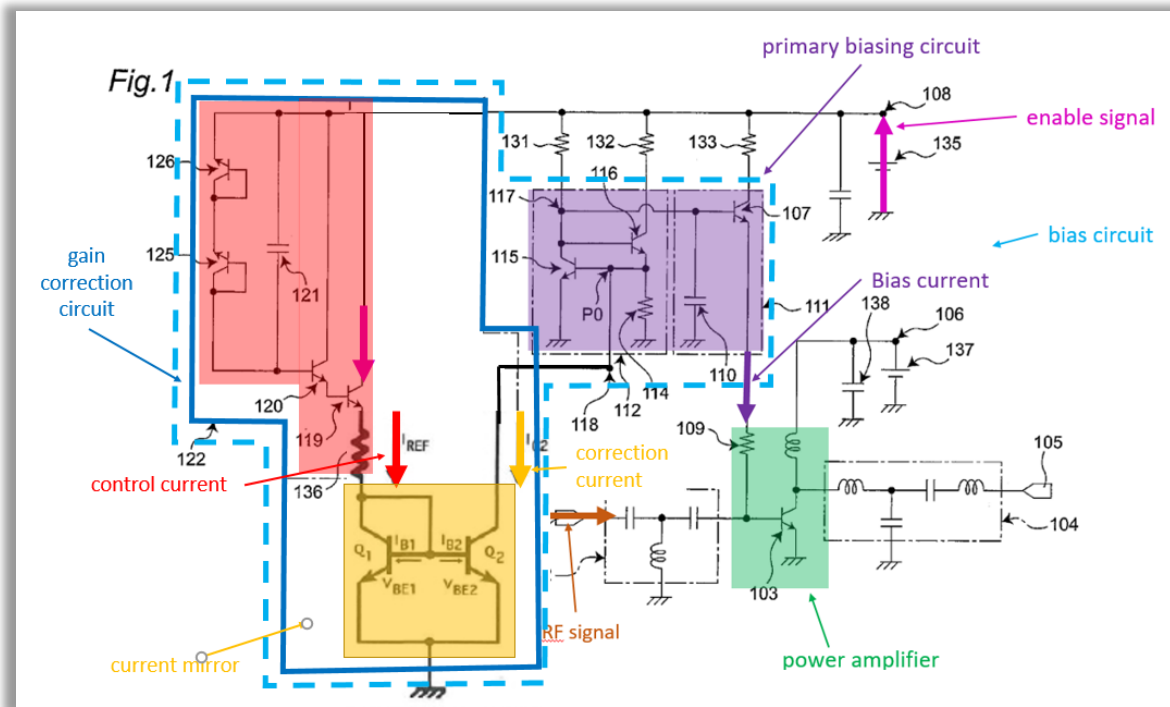
The basic current-voltage equations (4.1) through (4.8) hold over a broad temperature range (typically -60 to + 150°C) and over six orders of magnitude of current. Thus, the basic current mirror circuit of Figure 4.1 provides a means of obtaining a current reference level, independent of implicit device parameters, which can be "scaled" by proper choice of the emitter areas of the two transistors. Assuming typical  $V_{BE}$  mismatch of  $< \pm 1$  mV and  $\beta$  in the range of 100-200, the typical output current  $I_2$  would be within  $\pm 5\%$  of  $I_{ref}$  over a wide range of temperature and current levels.

EX-1014 172.

150. A POSITA would recognize modifying the speedup circuit as taught by *Ishimaru* to add a basic current mirror as taught by *Harrison* would be beneficial because it provides flexibility in allowing a broader range of voltages and a broader range of amplification due to the ability to achieve the desired current amplification by changing the ratios of transistor sizes in the basic current mirror. §IV.F.2. In my opinion, a POSITA would easily and advantageously apply *Harrison's* teaching to *Ishimaru* as illustrated below in the following annotated figures, derived from *Ishimaru's* Figure 1 and *Harrison's* Figure 4.18:



151. As illustrated above, a basic current mirror such as taught by *Harrison* can be advantageously added to *Ishimaru's* speedup circuit by interposing the basic current mirror at the emitter of transistor 119, and then connecting node P0/118 to the collector of current mirror transistor Q2. The collector of transistor 119 is then connected to the control voltage source (*the enable signal*).



152. As shown in the above annotations and simulation, *Ishimaru*' speedup circuit modified with *Harrison*'s basic current mirror is a gain correction circuit (dark blue) that responds to "a rise time of the control voltage of the control voltage source 135 (at turn-on of the amplifier)" in response to activation of the PA enable signal (pink) to generate a transient current signal via capacitor 121 that is amplified by transistors 120 and 119 and passed through resistor 136 to generate a control current (red arrow). *Ishimaru* modified with *Harrison* then takes this amplified time varying current signal (red arrow) and mirrors it using the basic *current mirror* to generate a time-varying  $I_{CORRECTION}$  (gold arrow) that is pulled from node 118.

153. A POSITA would have been highly motivated to combine *Ishimaru's* teaching of a bias circuit for a PA with *Harrison's* disclosure of a basic current mirror and have a reasonable expectation of success for at least the following reasons.

154. *Harrison* discloses a “basic” current mirror. EX-1006 71. Current mirrors were well-known in the art and were considered “a familiar icon of modern analog design.” EX-1012 239. Indeed, current mirrors were “widely used in analog integrated circuits” “as biasing elements” and were “particularly useful building blocks for analog circuit design.” EX-1013 251; EX-1014 170; *see, e.g.:*

Current mirrors made by using active devices have come to be widely used in analog integrated circuits both as biasing elements and as load devices for amplifier stages. The use of current mirrors in biasing can result in superior insensitivity of circuit performance to variations in power supply and temperature. Current mirrors are frequently more economical than resistors in terms of the die area required to provide bias current of a certain value, particularly when the required value of bias current is small.

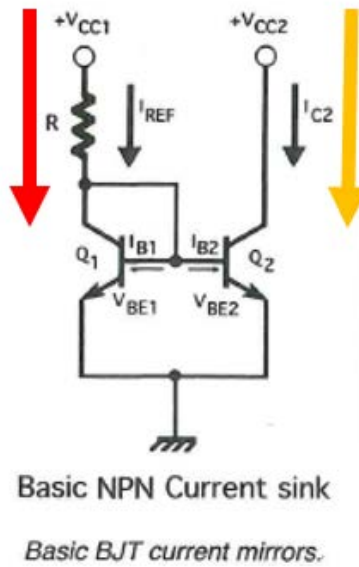
EX-1013 251.

In a constant-current stage, the reference current in one branch of the circuit is accurately reproduced or reflected in a second branch, relatively independent of the absolute values of the device parameters. Because of this property, these subcircuits are also known as *current mirror* circuits. Such circuit configurations are particularly useful

building blocks for analog circuit design, since they provide a means of establishing the de bias levels within the circuit, within the accuracy of the matching or tracking properties of the monolithic components.

EX-1014 170.

155. One of these advantages was that current mirrors take a reference current in one branch of a circuit and accurately reproduce or reflect that current in a second branch of that circuit, and can do so “relatively independent of the absolute values of the device parameters.” *Id.*; EX-1014 171. Thus, current mirrors were useful in coupling circuits together such that an input current could advantageously be provided into one branch of a circuit and the current mirror would then replicate (or *mirror*) that current such that the current mirror would pull a mirrored version of that current out of the second branch of the circuit. *Harrison* illustrates this configuration (called a current sink), where the input branch is annotated in red and the output branch is annotated in yellow. EX-1006 71.



EX-1006 (Fig. 4.18) (annotated).

156. Further, current mirrors were known to be useful in providing desired current scaling when mirroring a current (called **current mirror gain**) by changing the ratios of transistor sizes. EX-1006 95 (describing “current scaling” by setting the ratio of the emitter area); *see, e.g.:*

With the exception of the Widlar and the Wyatt current sources, up until now we have looked at current sources that generate input-to-output currents in a 1:1 ratio, but it is often necessary to generate integer multiples or fractions on an initial current. For the IC designer this is accomplished in the design by creating transistors with multiple emitters, or with bulk emitter area ratioed in either greater or lesser amounts. In this way a current can be made, say, 10 times or one-tenth of the initial input current. It is sometimes depicted in a manufacturer's

circuit schematic as a number written next to the particular emitter (see Figure 4.22D). It is sometimes shown, for example, as 10E or 10A.

For the board-level designer, generating multiples or fractions of an initial current can be accomplished in different ways. One way to do this is by paralleling individual transistors as shown in the following circuits, in what is known as *current scaling*.

EX-1006 95. In the case of bipolar junction transistors, this would be done by changing the relative sizes of the emitters of the current mirror transistors. EX-1013 25. Scaling transistor sizes in current mirrors to achieve granular, targeted levels of scaling that could (be fine-tuned was well understood as of the priority date of the '101 Patent, and described in multiple textbooks. EX-1013 251-257; EX-1014 172; EX-1012 252, 280; *see, e.g.:*

Since the saturation current of a bipolar transistor is proportional to its emitter area, the first term in (4.6) shows that the gain of the current mirror can be larger or smaller than unity because the emitter areas can be ratioed. If the desired current-mirror gain is a rational number,  $M/N$ , the area ratio is usually set by connecting  $M$  identical devices called *units* in parallel to form  $Q_2$  and  $N$  units in parallel to form  $Q_1$  to minimize mismatch arising from lithographic effects in forming the emitter regions.

EX-1013 254.

Equation 4.17 shows that the gain of the current mirror can be larger or smaller than unity because the transistor sizes can be ratioed. To ratio

the transistor sizes, either the widths or the lengths can be made unequal in principle. In practice, however, the lengths of  $M1$  and  $M2$  are rarely made unequal.

EX-1013 257.

The basic current-voltage equations (4.1) through (4.8) hold over a broad temperature range (typically  $-60$  to  $+150^{\circ}\text{C}$ ) and over six orders of magnitude of current. Thus, the basic current mirror circuit of Figure 4.1 provides a means of obtaining a current reference level, independent of implicit device parameters, which can be "scaled" by proper choice of the emitter areas of the two transistors. Assuming typical  $V_{BE}$  mismatch of  $< \pm 1$  mV and  $\beta$  in the range of 100-200, the typical output current  $I_2$  would be within  $\pm 5\%$  of  $I_{ref}$  over a wide range of temperature and current levels.

EX-1014 172.

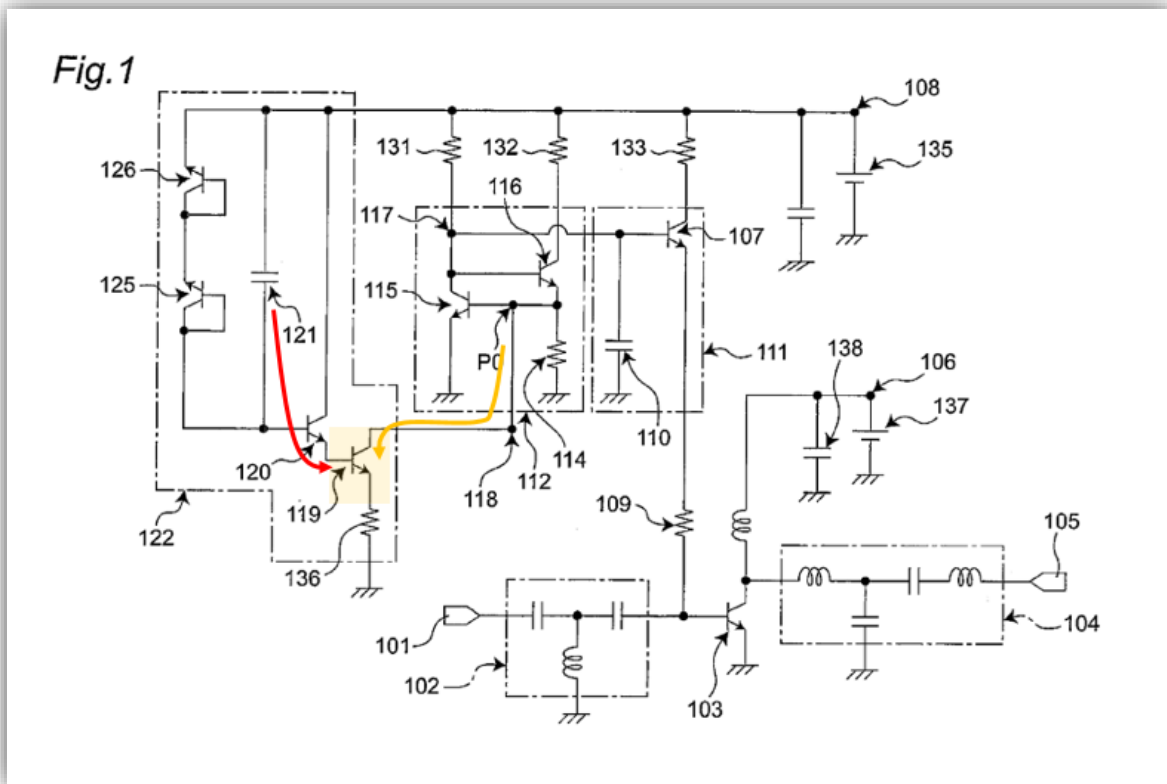
There is no particular difficulty in achieving high mirror ratios. In many cases, simple emitter area ratios will suffice, supported by current gain if necessary (as in the EFA mirror, which is not limited to the use of a single transistor for current boosting). In practical monolithic designs, emitter area ratios of up to 100:1 are not hard to achieve.

EX-1012 280.

157. In addition, a POSITA understood that *Harrison's* two-transistor current mirror would advantageously provide better isolation between the left side and the right side of *Ishimaru's* circuit. First, because there are separate emitter

currents and paths in the two-transistor mirror, there is a degree of separation between the left and right sides of the circuit. Second, it avoids the issue that using a single transistor like *Ishimaru's* 119 as the current mirror has coupling (parasitic) between its base and collector due to standard parasitic capacitance. This coupling across 119 can create unwanted coupling across the transistor, such that noise on one side of the circuit can pass to the other side. Adding *Harrison's* two-transistor current mirror does not have this limitation, providing better isolation between the input and output current signals than *Ishimaru* provides.

158. A POSITA would thus have been motivated to modify the teachings of *Ishimaru* to add a basic current mirror as taught by *Harrison* because a POSITA understood that *Ishimaru's* circuit is designed to amplify the current that flows through capacitor 121 (annotated in red below) to generate the current sink pulled from node 118 (annotated in yellow). EX-1004 ¶¶50-52, Fig. 1.



EX-1004 Fig. 1 (annotated).

159. A POSITA recognized that *Ishimaru* used a current source (red) from circuit 122 to generate a current sink (yellow) from 112, coupling the two circuits using the current mirroring provided by transistor 119. A POSITA readily understood that this coupling could be improved by use of the basic current mirror of *Harrison* because of multiple advantages of providing an additional stage of fine tuning the current amplification. The additional stage of fine tuning would give the designer an additional degree of freedom in designing the circuit, would provide better isolation between the two sides of the circuit, and allow fine tuning in a final amplification stage that had better linearity, better control, and higher

configurability of its mirror ratio,  $M$ , in scaling the mirrored current. *See also* §IV.F.2 (discussing two-transistor mirrors).

160. A POSITA would understand that, without the additional teachings of *Harrison, Ishimaru's* circuit is constrained by the limited configurability of the  $\beta$  (amplification factor) of transistors 119 and 120. EX-1006 53-55; *see, e.g.:*

Gain is a variable parameter that is difficult to control in processing and-manufacturing. As a result, manufacturers normally provide only a minimum gain specification. The particular process will yield a range of gains, where any one device's value may typically range from, say, 100 to 350.

EX-1006 55. A POSITA was aware that the  $\beta$  of transistors 119 and 120 would be, *e.g.*, 60 to 150 or more, meaning that the gain of *Ishimaru's* transistors 119 and 120 would be a relatively large and cumbersome gain (for example, x100 for transistor 120 and x100 for transistor 119 would result in a total gain of 10,000).

EX-1006 53-55; EX-1015 38 (practical  $\beta$  values can be “up to 500”). While the  $\beta$  values provide amplification, and, for transistor 119 provide a mirror ratio, that mirror ratio is “not very linear” and “poorly-controlled” compared to other current mirrors, such as the basic current mirror of *Harrison*. EX-1012 242; EX-1006 53-55; *see, e.g.:*

In the simplest possible scenario, a single BJT can be used as a mirror: node N1 (of Figure 6. 1a) is the base, N2 the collector and NO the emitter. Of course, the practical objection to this proposal is that the

mirror ratio,  $M$ , is much higher than generally needed and poorly-controlled, being just the common-emitter current-gain,  $J_3$ , and not very linear. While these objections are all true, it is nevertheless useful to begin here, because we will discover that many of the properties of more familiar mirrors can be predicted from the behavior of the single transistor circuit.

EX-1012 242. Thus, a POSITA readily understood that having to rely upon just the  $\beta$  gains of transistors 119 and 120 is another factor making tuning *Ishimaru's* circuit overly complicated and constrained.

161. Adding a basic current mirror similar to that taught by *Harrison*, however, allows for an additional stage of amplification that can be finely tuned, linear, tightly controlled and granular scaling of the current by adjusting the emitter area of the current mirror transistors, as discussed above. Being able to scale currents in this manner would be useful for a circuit designer wanting to establish a speedup control circuit that could advantageously be reused and adapted for different PA applications and product lines. That is because a POSITA understood that different PAs have different startup and steady state operating qualities, and that the gain variation in *Ishimaru's* Figure 2 is specific to a given PA in a given layout, in a specific operating point and use case. The corresponding corrective transient current thus has a specific amplitude and duration that is suitable for the application at issue.

162. For example, using different PA circuit layouts (*i.e.* where components are dimensionally closer or farther away from each other), different PA packaging, or different PA integrated circuits using a different semiconductor manufacturing process (*e.g.*, Gallium Arsenide (“GaAs”) Heterojunction Bipolar Transistors (“HBTs”) (together “GaAs HBTs”), or Silicon Germanium Bipolar CMOS HBTs (“SiGe BiCMOS HBTs”)), will result in different thermal behaviors and startup effects, and so the amount of correction required will vary. *Ishimaru* itself recognizes that temperature effects depend on the layout of the PA and the amount of correction required varies across applications. EX-1004 ¶23 (“[T]urn-on behavior of the control voltage source in the amplifier depends on the layout of the amplifier, particularly on the placement of transistors[.]”), ¶3 (“In some communication systems, slight changes of amplification gain as small as 0.2 to 0.3 dB may matter.”), ¶4 (“there are some cases in which variations in amplification ratio or phase on the order of several tens to several hundreds of  $\mu$ s caused by relatively slow temperature increases due to heat generation as an example do matter.”); *see, e.g.*:

That is, heat generation of transistors becomes larger in a transistor for signal amplification involving larger current consumption (first transistor), and smaller in a transistor for bias Supply (second transistor). Then, in stages before the temperature's reach to the equilibrium, the temperature is higher at around the signal-

amplification transistor and lower increasingly with increasing distance from the signal-amplification transistor, where these temperature differences cause the current value to vary, forming a cause of distortion of the modulated-wave signal. Therefore, turn-on behavior of the control voltage source in the amplifier depends on the layout of the amplifier, particularly on the placement of transistors, and amplifiers of the same layout result in the same characteristics as to turn-on and -off transient variations of the amplifiers.

EX-1004 ¶23.

It should be noted here that the linear amplification mentioned above means that even with input signal power changed, the output signal power is amplified at a constant ratio for output while the phase keeps unchanged. In some communication systems, slight changes of amplification gain as small as 0.2 to 0.3 dB may matter

EX-1004 ¶3.

As another aspect of the linear amplification, there are some cases in which variations in amplification ratio or phase on the order of several tens to several hundreds of us caused by relatively slow temperature increases due to heat generation as an example do matter. As a circuit for correcting effects of such heat generation by the power amplifier's own, there has been shown, in U.S. Pat. No. 4,924, 194 (see FIG. 1), a circuit in which heat generation of an amplifier transistor is detected by a temperature sensing element (PIN diode) thermally coupled to the amplifier transistor and the detection result is reflected on a bias voltage of the amplifier transistor

EX-1004 ¶4.

163. Thus, *Ishimaru* provides express motivation for a POSITA to add a current mirror of similar design to *Harrison's* for its intended purpose in order to provide flexibility in scaling *Ishimaru's* current, including allowing a designer to tune the operation of *Ishimaru's* corrective current transient in Figure 3 to a higher peak (such as for a PA having a larger gain variation). A POSITA understands that *Ishimaru's* circuit otherwise constrains the ability to tune  $I_{CORRECTION}$  at node 118 as a function of the current through capacitor 121 because of the common, fixed relationships caused by transistor 119 and resistor 136 and the design constraints that limit the configurability of the amplification factors  $\beta$  of transistors 119 and 120. A POSITA would have recognized that *Harrison's* two-transistor current mirror would advantageously provide an extra degree of freedom in tuning *Ishimaru's* circuit to compensate for the gain problems of a given PA.

164. Modifying the teachings of *Ishimaru* with the basic current mirror taught by *Harrison* would involve no more than combining prior art elements (*Ishimaru* and a conventional current mirror) according to known methods (coupling a current source through a positive current mirror to a current sink, while scaling the mirror's gain to provide tunable amplification) to yield predictable results. Adding a current mirror simply uses a known technique (scaling currents

between two branches of a current mirror) to improve *Ishimaru* by scaling its currents between the two branches of its circuits in the same way.

165. The combined teachings of *Ishimaru* and *Harrison* is consistent with the disclosure of the '101 Patent that the term *current mirror* can refer to current amplification circuits including a plurality of current mirrors combined (*e.g.*, cascaded) to achieve a target gain. EX-1001 11:42-45; *see, e.g.*:

As used herein, the term current mirror can refer to current amplification circuits including a plurality of current mirrors combined ( *e.g.* cascaded) to achieve a target gain.

EX-1001 11:42-45.

### **Claim 17**

***[17.2] amplifying the control current using a current mirror of a current amplifier to generate a correction current; and***

166. *Ishimaru* in view of *Harrison* discloses this limitation for the same reasons as discussed with respect to limitation [1.2.4].

### **Claim 21**

***[21.2] a current amplifier configured to amplify the control current to generate a correction current, the current amplifier including a current mirror; and***

167. *Ishimaru* in view of *Harrison* discloses this limitation for the same reasons as discussed with respect to limitation [1.2.4].

168. Thus, for Ground 2 *Ishimaru* in view of *Harrison* discloses each of the Challenged Claims.

## **CONCLUSION AND DECLARATION**

My findings and opinions set forth in this Declaration are based on my work and examination to date. I may continue my examinations in view of additional documents or other factual evidence over the course of this proceeding that may necessitate supplementing and/or refining my opinions. I reserve the right to add to, alter, or delete my opinions and my Declaration upon discovery of additional information. I reserve the right to make such changes as necessary.

In signing this Declaration, I understand that the Declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I acknowledge that I may be subject to cross-examination in this case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001, of Title 18 of the United States Code.

[SIGNATURE ON FOLLOWING PAGE]



Date: 1/14/2025

By: David S. Ricketts

## APPENDIX A – MATERIALS RELIED UPON

Exhibit	Brief Description
1001	U.S. Patent 8,717,101 (“the ’101 Patent”)
1002	Prosecution History for U.S. Patent 9,917,101
1003	Reserved
1004	U.S. Patent Publication 2009/0212863 (“ <i>Ishimaru</i> ”)
1005	U.S. Patent Publication 2004/0232982 (“ <i>Ichitsubo</i> ”)
1006	Excerpts of Linden T. Harrison, Current Sources and Voltage References, A Design Reference for Electronics Engineers (Elsevier 2005) (“ <i>Harrison</i> ”)
1007	U.S. Patent Publication 2011/0025422 (“ <i>Marra</i> ”)
1008	Johnson, “Silicon-Germanium BiCMOS HBT Technology for Wireless Power Amplifier Applications,” IEEE J. Solid State Circuits, Vol. 39, No. 10 (Oct. 2004) (“ <i>Johnson</i> ”)
1009	Excerpts of Laplante, Comprehensive Dictionary of Electrical Engineering (2d Ed. 2005) (“ <i>Laplante</i> ”)
1010	U.S. Patent Publication No. 2011/0128078 (“ <i>Doherty</i> ”)
1011	Christopher Bowick, “What’s in an RF Front End,” EE Times (Feb. 4, 2008) available at: <a href="https://www.eetimes.com/whats-in-an-rf-front-end/">https://www.eetimes.com/whats-in-an-rf-front-end/</a> (last accessed December 12, 2024) (“ <i>Bowick</i> ”)
1012	Barrie Gilbert, “Bipolar Current Mirrors”, Chapter 6 in Tomazou <i>et al.</i> , Analog IC Design: The Current Mode Approach (Reprinted 2008) (“ <i>Gilbert</i> ”)
1013	Excerpts of Gray <i>et al.</i> , Analysis and Design of Analog Integrated Circuits (5 <sup>th</sup> Ed. 2009) (“ <i>Gray</i> ”)
1014	Excerpts of Grebene, Bipolar and MOS Analog Integrated Circuit Design (2003) (“ <i>Grebene</i> ”)
1015	Excerpts of Illingworth, Dictionary of Electronics (3d Ed. 1998)
1016	Declaration of June Ann Munford
1017	TriQuint Semiconductor, Application Note TVS Protection and Bias Sequencing for HBT Amplifiers, p. 1 (June 2009) (“ <i>TriQuint</i> ”)

Exhibit	Brief Description
1018	Certified Translation of Japanese Patent Application Publication No. JP 2009-283991 (“ <i>Akagi</i> ”)
1019	U.S. Patent No. 6,831,517 (“ <i>Hedberg</i> ”)
1020	Joint Claim Construction Chart in ITC Inv. No. 337-TA-1413
1021	VintageTek biography, Barrie Gilbert, available at <a href="https://vintagetek.org/barrie-gilbert/">https://vintagetek.org/barrie-gilbert/</a> (“ <i>Gilbert Biography</i> ”)
1022	<i>Diels</i> , Single-Package Integration of RF Blocks for a 5 GHz WLAN Application, IEEE Transactions On Advanced Packaging, Vol. 24, No. 3, (August 2001) (“ <i>Diels</i> ”)
1023	<i>Scherz</i> , Practical Electronics for Inventors (2000) ( <i>Sherz</i> )
1024	<i>Horowitz</i> , Elementary Electricity and Electronics, Component by Component, (1986) (“ <i>Horowitz</i> ”)
1025	<i>Yanjun</i> , “A 2.4-GHz SiGe HBT power amplifier with bias current controlling circuit”, Chinese Institute of Electronics, Journal of Semiconductors, Vol. 30, No. 5, (May 2009), (“ <i>Yanjun</i> ”)
1026	Patent Owner’s Markman Briefs in ITC Inv. No. 337-TA-1413
1027	Petitioner’s Markman Briefs in ITC Inv. No. 337-TA-1413
1028	Commission Investigative Staff’s Markman Briefs in ITC Inv. No. 337-TA-1413

## **APPENDIX B – RÉSUMÉ**

## **1. David S. Ricketts - Expert Testimony Deposition & Trial (last 6 years)**

### **DuaneMorris (2024-)**

Case – In the Matter of Certain Wireless Front-End Modules and Devices Containing the Same  
Case No. No. 337-TA-1413  
Retained by Respondent Kangxi Communication Technologies (Shanghai) Co., Ltd. (“KCT”)

### **Bond, Schoeneck & King NY (2024-)**

Case – Signify North America Corporation et al. (Patent Owner) v. Lepro Innovation Inc. et al.  
Case No. 2:22-cv-02095-JAD-DJA (Patent Owner)  
Retained by Patent Owner

### **Bunsow De Mory CA (2024)**

Case – Tesla, INC vs. Relink US LLC (Patent Owner)  
Case No. IPR2024-00389  
Retained by Patent Owner

### **Nixon Peabody CA (2024-)**

Case - CogniPower LLC (Patent Owner) v. Anker Innovations LTD and Fantasia Trading LLC  
Case No. C.A. No. 19-cv-02293-CFC-SRF  
Retained by Patent Owner

Case - CogniPower LLC (Patent Owner) v. Samsung  
Case No. 2:23-cv-160 - JRG  
Retained by Patent Owner

### **Banner Witcoff DC (2024)**

Case – SMA Solar Technology AG (Junior Party) v. SolarEdge Technologies Ltd.(Senior Party)  
Case No. Patent Interference No. 106,144 (DK)  
Retained by Senior Party

### **Daignault Iyer LLP (2023-)**

Case – Parker Vision (Patent Owner) v. REALTEK SEMICONDUCTOR CORP.  
Case No. 6:22-cv-01162-ADA  
Retained by Patent Owner

Case – Parker Vision (Patent Owner) v. REALTEK SEMICONDUCTOR CORP.  
Case No. 6:22-cv-00375  
Retained by Patent Owner

Case – Parker Vision (Patent Owner) v. NXP SEMICONDUCTORS N.V., NXP B.V., NXP USA, INC. D/B/A NXP SEMICONDUCTORS USA, INC.,  
Case No. 6:23-cv-00389  
Retained by Patent Owner

Case – Parker Vision (Patent Owner) v. MEDIATEK INC. AND MEDIATEK USA INC.  
Case No. 6:22-cv-01163-ADA  
Retained by Patent Owner

Case – Parker Vision (Patent Owner) v. MEDIATEK INC. AND MEDIATEK USA INC.  
Case No. 6:23-cv-00375-ADA  
Retained by Patent Owner

Case – Parker Vision (Patent Owner) v. TEXAS INSTRUMENTS INCORPORATED  
USA INC.

Case No. 6:23-cv-00384

Retained by Patent Owner

**McKool Smith Tx (2023-2024)**

Case - Mojo Mobility (Patent Owner) v. Samsung

Case No. 2:22-cv-00398

Retained by Patent Owner

**Anderson Dailey LLP (2023-)**

Case – Joy Laskar, Ph.D. v. Phillip W. Hurd; and Patrick A. Jenkins

Case No. 1:18-cv-4570-WMR

Retained by Plaintiff

**Kramer Alberti CA (2023-2024)**

Case – Polaris Powered Tech LLC (Patent Owner) v. Samsung

Civil Action No. 2:22-cv-00469-JRG

Retained by Patent Owner

**King & Wood Mallesons, Melbourne, Victoria, Australia (2023-)**

Case — Federal Court of Australia

Proceeding No. VID 122/2023

Retained by Respondents

**Perkins Coie, San Francisco, CA (2023-)**

Case — The Noco Company, Inc. (Patent Owner) v. Shenzhen Gooloo E-Commerce Co., Ltd.

NDOH Case No. 1:20-cv-01171-PAB

Retained by Defendant

Case — SHENZHEN XINZEXING E-COMMERCE CO., LTD., (Petitioner) v. SHENZHEN CAR KU  
TECHNOLOGY CO., LTD.(Patent Owner)

IPR2024-00222

Retained by Patent Owner

Case — Shenzhen Chic Electrics Co., Ltd. (Petitioner) v. Pilot, Inc.(Patent Owner)

IPR2023-00810

Retained by Petitioner

Case — In the Matter of Certain Portable Battery Jump Starters and Components Thereof  
ITC Investigation No. 337-TA-1360

Retained by Respondents

Case — In the Matter of Certain Portable Battery Jump Starters and Components Thereof  
ITC Investigation No. 337-TA-1359

Retained by Respondents

**Heim, Payne & Chorush, Houston, Tx (2022)**

Case - Apple Inc. et al. (Petitioner) v. Arigna Technology Ltd (Patent Owner)

IPR2022-01037

Retained by Patent Owner

**Norton Rose Fulbright, Toronto, Canada (2022-2023 )**

Case – *Canadian Tire Corporation, Limited (Defendant) v. The Noco Company, Inc (Plaintiff)*

Court File No. T-343-20

Jurisdiction: Federal Court, Canada.  
Retained by Defendant

**Russ August & Kabat, Los Angeles, CA (2021-2023)**

Case - *APPLE INC.*, (Petitioner) v. *SCRAMOGE TECHNOLOGY LTD.*, (Patent Owner)  
IPR2022-00351  
IPR2022-00120  
IPR2022-00117  
Retained by Patent Owner

**Powell Gilbert, London (2022)**

Case – *Shenzhen Carku Technology Co., Ltd. (Claimant) and The NOCO Company (Defendant)*  
Claim No. HP-2020-000018  
Jurisdiction: The High Court of Justice Business and Property Courts of England and Wales.  
Retained by Claimant

**Kramer, Day, Burlingame (2020-2023)**

Case - *Garrity Power Services LLC vs. Samsung Electronics Ltd.*  
Case Number – Texas Eastern District Case No. 2:20-cv-00269  
EPR - 9,906,067 Control No. 90/014,746  
Retained by Patent Owner (Garrity)

**Perkins Coie, San Francisco, CA (2021-2022) Validity/Invalidity**

Case – *The NOCO Company vs. Shenzhen Carku Technology Co., Ltd. And others* (Respondents)  
Case Number - USITC 337-TA-1256  
Retained by Respondents

**Stern Kessler Goldstein & Fox, Washington, DC (2019-2020)**

Case - *Samsung Electronics Co., Ltd. et al. (Petitioner) v. NuCurrent, Inc.* (Patent Owner)  
Case Number - IPR2019-00858,  
Case Number - IPR2019-00859  
Case Number - IPR2019-00860  
Case Number - IPR2019-00861  
Case Number - IPR2019-00862  
Case Number - IPR2019-00863  
Case Number - IPR2019-01217  
Case Number – PGR2019-0049  
Case Number – PGR2019-0050  
Retained by Patent Owner (NuCurrent)

**Dr. David S. Ricketts**  
**Full Professor**

**I.B BRIEF RESUME**

**1. Education background:**

Ph.D., Electrical Engineering, 2006, Harvard University  
M.Sc., Electrical Engineering, 1997, Worcester Polytechnic Institute  
B.Sc., Electrical Engineering, 1995, Worcester Polytechnic Institute

**2. Professional experience:**

Full Professor, 2012 – present, Department of Electrical and Computer Engineering North Carolina State University, Raleigh, NC

Visiting Researcher (Research Scientist), 7/2012 – 8/2013, MTL-ECE Massachusetts Institute of Technology, Cambridge, MA

Visiting Associate Professor, 9/2012-12/2012, School of Engineering and Applied Science Harvard University, Cambridge, MA

Assistant Professor, 2006 – 2012, Department of Electrical and Computer Engineering Carnegie Mellon University, Pittsburgh, PA

Manager of New Product Development & Advanced System Engineering, 2001 – 2003, ON Semiconductor, East Greenwich, RI

Principal Consultant, 1999-2001, Renaissance Design, Inc., Warwick, RI

IC Technology Unit Manager, 1995-1999, American Power Conversion, Billerica, MA

**3. Scholarly and creative activities:**

<i>Type</i>	<i>Number</i>
<i>Books</i>	<u>3</u>
<i>Book Chapters</i>	<u>2</u>
<i>Refereed Journal Article</i>	<u>52</u>
<i>Other Journal Article (submitted)</i>	<u>0</u>
<i>Conference Paper, Refereed</i>	<u>82</u>
<i>Conference Presentation, (no paper)</i>	<u>7</u>
<i>Patent (filed)</i>	<u>2</u>
<i>Academic Workshops Chaired</i>	<u>20</u>
<i>Research Presentations, Invited</i>	<u>66</u>

**4. Membership in professional organizations:**

IEEE, 1997-present (senior member since 2015)

**5. Scholarly and professional honors:**

- 2022 Chancellors Innovation Fund
- 2021 William F. Lane Outstanding Teaching Award

- Best Paper Award, IEEE Asia-Pacific Microwave Conference 2016.
- IEEE Senior Member, 2015
- Certificate of Teaching Excellence, Derek Bok Center, Harvard University, 2013
- **NSF CAREER AWARD, 2011.**
- Wimmer Teaching Fellow, Carnegie Mellon University, 2009.
- George Tallman Ladd Research Award, Carnegie Mellon University, 2009.
- National Academy of Engineers Frontiers of Engineering Education Recipient, 2009.
- **DARPA Young Faculty Award, 2008.**
- McGraw Hill Yearbook of Science and Technology, 2008.

#### **6. Professional service on campus:**

Faculty Teaching Evaluation Committee (ECE Department) 2022-present  
Faculty Search Committee (ECE Department) – Fall/Spring 2021/22 & 2019/20  
Course Curricula Committee (ECE Department) - 2015-present  
Faculty Search Committee (ECE Department) – Fall/Spring 2016/2017  
Senior Design Director Search Committee (ECE Department) - 2014  
Participated in Engineering Open House (ECE Department), 2014

#### **7. Professional service off campus:**

**Advisor DARPA Commercialization Office** - 2023-24

**Topic Editor**, IEEE JMW 2022-2023

**Track Editor**, IEEE T-MTT Oct 2019-2022

**Chair**, IEEE Chapter ACME (Joint chapter of Antennas and Propagation (AP), Electronic Packaging Society (EP), Microwave Theory and Techniques (MTT), and Electron Devices (ED) 2019-

Technical Committee **Chair** for IEEE T-MTT 9 Society 2020-2022

Technical Committee **Vice-chair** for IEEE T-MTT 7 Society 2015-2019

Technical Program **Chair**: Enabling Nanomanufacturing for Rapid Innovation, TRC/NSF Workshop, Aug. 2013

Technical Program Committee (member) – IEEE International Microwave Symposium 2014-;

Technical Program Committee IEEE BioWireless 2012-2015.

Session Chair - Nanotechnology, CMOS Emerging Technologies Conf., Banff, Canada 2009; NANO-DDS, Chemically-Synthesized, Biomimetic Systems and Biologically-Inspired Architectures Session, August 2011.

## **II.B. INSTRUCTIONAL DEVELOPMENT**

Include innovations in courses and curricula.

Creation of a new STEM portal interactRF.org (supported by ONR research grant) to teach RF and microwave engineering. This portal supports national education workshops and a full semester online course using an e-learning platform.

ECE 592 Analog Laboratory (graduate). Introduced graduate version of ECE 426 to allow for more advanced hands-on projects.

ECE 426 Analog Laboratory. Re-booted a retired course with Dr. Besnoff (teaching professor). Developed 12 new lectures and an entirely new course project where students build a drone from scratch, making their own printed circuit boards and coding an Arduino for flight control

ECE 714 Advanced Analog IC Design (ADCs). CAF Completed S18. (NCSU) Fall 2015. Developing new course for advanced analog IC design. Includes ~ 35 online lectures, and 10 interactive labs/workshops for students to practice hands on design. Full course, including labs, are available online for the public.

ECE 424/524 – CAF completed S17- 492(592) Radio Systems Design: (NCSU) Spring 2014+. Developed new experiential undergraduate course in radio system design. Includes 34 online lectures, and 10 interactive labs/workshops for students to practice hands on design. Full course, including labs, are available online for the public.

ECE 592 Analog-to-digital Converters: (NCSU) Fall 2013. Developed new course for ADCs as part of ECS circuit's curriculum.

ES139/239 Innovation in Science and Technology (Harvard): Fall 2012. Co-developed new format, assignments and teaching materials for primarily undergraduate innovation course.

ECE 18-605/606 Innovation in Science and Technology (CMU): Fall 2009. Developed interdisciplinary course on innovation between ECE and CMU's Engineering Technology Innovation Management masters program.

ECE 18-513 RF Circuits and Antennas for Wireless Systems (CMU): Fall 2008. Co-developed w. D. Stancil a new capstone design course in RF circuits & antennas.

ECE 18-610 Fundamentals of Modern CMOS Devices (CMU): Spring 2008, Developed introductory graduate course in CMOS device physics.

ECE 18-310 Fundamentals of Semiconductor Devices (CMU): Spring 2007. Developed entirely new content for undergraduate device physics course.

## **II.C. MENTORING ACTIVITIES**

Include undergraduate academic advising and assessments thereof, if applicable, graduate committees, postdoctoral advising, advising student organizations, special projects with students, and Department of Public Instruction assessments of supervising student teaching.

Currently, member of   4   PhD and   0   MS committees.

1. Participated in 29 Masters/PhD graduate committees.
2. Advisor to 6 nonthesis MS students.

#### POST-DOCTORAL RESEARCHER SUPERVISION

1. Jordan Besnoff (F2020, now research Prof NCSU 2021-)
2. Morteza Abbasi (2013-2016, research Prof. NCSU, 2016-18)
3. Jordan Besnoff (2014, now at Oakridge National Labs)
4. Junfeng Xu (2013, now at SpaceX)
5. Mathew Trotter (2013, Disney Research)
6. Mathew Chabalko (2012, now at Disney Research)
7. Darmin Arumugum (2012, now at JPL)
8. Limin Cao (2010,2012)
9. Joshua Smith (2010-2012, now at NRL)
10. Shingo Tamaru (2008-2010, now at AIST, Japan)

#### GRADUATE STUDENT SUPERVISION NCSU

1. Prya Darshni (PhD Canddiate, 2026)
2. Hongtao Zhong (PhD Candidate, 2025)
3. Shian Su (PhD Candidate, 2025)
4. Joe Zhou (PhD Candiate 2023)
5. Karan Maru F20-S21 RA
6. Sriraj Kandala, Summer 2020 RA
7. Bhaumik Jain Summer-Fall 2020 RA
8. Matt Dwyer Summer-Fall 2020. RA
9. William Harris (PhD candidate, 2019)
10. Junyu Shen (PhD candidate, 2019)
11. Hangjin Liu (PhD Candidate, 2021)
12. You Zhou (PhD Candidate, 2021)
13. Deeksha Lal (PhD 2018)
14. Samyak Parakh (MS, 2018)
15. Rafael de Silva (PhD candidate, 2020)
16. Michael Aiken ( MS 2017, PhD Candidate)
17. Viswanath Ramesh (Initial PhD work 2015-2016)

#### GRADUATE STUDENT SUPERVISION CMU

1. Emre Karagozler, PhD 2013
2. Wei Tai, PhD 2012
3. Darmin Arumugam, PhD 2012
4. Weihua Hu, PhD 2012
5. Chongzhe Li, MS 2012
6. Zacherias George, MS 2012
7. En Shi, MS 2010
8. Qianyu Liu, MS 2009

#### GRADUATE COMMITTEES

1. Yongduk Oh (PhD Candidate 2023)
2. Jaewoo Kim (MS 2021)
3. Sarah Colebaugh

4. Weifu Li (PhD Candidate 2019)
5. Kirti Bhanushali (PhD candidate 2018)
6. Weihu Wang (PhD candidate 2018)
7. Yunjia Zhu (MS candidate Textiles 2017)
8. Junan Zhu (PhD candidate 2016)
9. Yunjia Zhu (MS candidate 2016)
10. Anirban Sarkar, (PhD candidate 2016)
11. Sandeep Hari, (PhD candidate 2018)
12. Kevin Green (PhD candidate 2016)
13. Ying Yi Tang, PhD 2015 (CMU)
14. Mohammad Noman, PhD 2013 (CMU)
15. Erkan Alpman, PhD 2007 (CMU)

#### UNDERGRADUATE STUDENT SUPERVISION

1. Bryan Wilson – S24
2. Jason Apsell F22-
3. Zander Sellesest F-22-
4. Jonathan Weeks – S32-
5. Yiyang Ye – S23/Summer
6. Maya Clinton F22-S23 (MechE)
7. Cole Contos F22
8. Jason Abell F22-S23
9. Landon Calton F22
10. Frank di Lustro S21
11. Alan Davila Summer 2020
12. Casey Crouse Spring 2020-Summer 2020
13. Jacob Abramow Spring 2020
14. Jeremy Peterson Spring 2020-Summer 2020
15. Laura Walker Spring 2020
16. Ryan Hardy REU Spring 2020-Spring 2021
17. Matt Dwyer Connor Walker REU Fall/Spring 2019
18. Matt Dwyer REU 2019 Summer.
19. Casey Crouse REU 2019 Summer.
20. Zack Miller, Felix Chamielec, Danny Krafft, Grason Humphrey, Sufian Ahmad (NCSU UG Senior Design: Qi Charger, 2019)
21. Matt Dwyer, S19 (NCSU, Undergrad Research)
22. Shakti Reddy, F18/S19 (NCSU, Undergrad Research)
23. Shane Reagan, Zach Cline, Daniel Robson, Andrew Cragg, (NCSU UG Senior Design: Pringles Radar 2017/18)
24. Christian Burke, F17/S18 (NCSU, Undergrad Research)
25. Bill Zhou (BSEE) Fall 2016 (NCSU, Undergrad Research)
26. Akshay Iyer, Stephen Kerr, William Stepp, Kirk Weston, (NCSU UG Senior Design: Magnetic Sports Tracking, 2015/16)
27. Shaunak Turaga (BSEE), Fall/Spring 2014/15 (NCSU, Undergrad Research)
28. Mathew Briley (BSEE), Fall/Spring 2014/15 (NCSU, Undergrad Research)
29. Adeola Salu (BS), Spring 2013 (Harvard, Independent Study )
30. Zackary Hamad (BS), Spring 2011 (Harvard, independent Study)
31. Andrew Hillenius (BS), Summer/Fall, 2011 (CMU, Independent Study)
32. Chongzhe Li (BS), Spring 2010 (CMU, Independent Study)

- 33. Christopher Heidelberger (BS), Summer 2009, (CMU) NSF REU
- 34. Yue Lu (BS), Summer 2007 (CMU Independent Study)

SPECIAL STUDENT ADVISING

- 1. Karan Maru, S20 (NCSU MSEE Research)
- 2. Bhaumik Jain, F19 (NCSU, MSEE Research)
- 3. Sriraj Kandala, F19 (NCSU, MSEE Research)
- 4. Sandesh Shanmukha, S19 (NCSU, MSEE Research)
- 5. Shubhankar Patwardham F17/S18/F18 (NCSU, Ind. Study)
- 6. Amrutha Anantha S18 (NCSU, Ind. Study)
- 7. David Philpott S2017 (NCSU, Ind. Study)
- 8. Shenoy Akshat S2017 (NCSU, Ind. Study)
- 9. Sayan Das Fall 2016 (NCSU, Ind. Study)
- 10. Rounak Lokare Spring 2016 (NCSU, Ind. Study)
- 11. Swaroop Mohapatra Spring 2016 (NCSU, Ind. Study)
- 12. Ganapati Pai Spring 2016 (NCSU, Ind. Study)
- 13. Mahmoud Metwally 2015 (NCSU, MS research)
- 14. Ashwin Thyagarajan Spring 2015 (NCSU Ind. Study)
- 15. Reza Chavoshisani 2015 (PhD – 1 year visiting scholar)
- 16. Abhishek Malhotra (MS), Spring/Summer, 2013 (NCSU, Independent Study)
- 17. Syed Saad (MS), Summer 2011 (CMU, Independent Study)
- 18. Brian Lee (MS), Summer 2011 (CMU, Independent Study)
- 19. Ashwath Krishnan (MS), Summer 2010 (CMU, Independent Study)
- 20. Akshat Gupta (MS), Fall 2009 (CMU, Independent Study)
- 21. Heer Ghandi (MS), Fall 2007 (CMU, Independent Study)

*GRADUATE COMMITTEES: 2023 ones listed*

<b>Student name</b>	<b>Degree [defense]</b>	<b>Chair</b>	<b>Member</b>	<b>Comment</b>
Shian Su	PhD	X		Qual S21
Hongtao Zhong	PhD	X		Qual S22

## II.D. MASTER'S AND DOCTORAL THESES DIRECTED AND BEING DIRECTED

Show numbers and dates in each category

I am actively directing the theses of   2   Ph.D. students and   0   Master with Thesis option (MST) students.

I have graduated   8   PhD and   4   MST students. I was the sole chair of   5   of the   7   PhD committees; I was the sole chair of   4   of the   4   MST committees.

### Master's and Doctoral Theses Currently under direction

Student name	Degree	Committee Approved	POW Approved	Qualifying Review (date)	Preliminary Exam (date)	Notes
Shian Su	PhD			S21		RA
Hongtao Zhong	PhD			S21		RA

### Doctoral Theses Directed

Student name	Degree [date]
Joe Zhou	May 2024
Carter Harris	May 2020
Junyu Shen	Aug 2019
Deeksha Lal	May 2019
Emre Karagozler	Jan 2013
Wei Tai	May 2012
Darmin Arumugam	Jan 2012
Weihua Hu	Aug 2012

### Master's Directed

Student name	Degree [date]
Samyak Parakh	Dec. 2017
Fenglan Yang	May 2015
Chongzhe Li (CMU)	Dec. 2012
Zacharias George (CMU)	Aug 2005
En Shi (CMU)	May 2010
Qianyu Liu (CMU)	May 2009

### III. SCHOLARSHIP

#### III.A. PUBLICATIONS, AWARDS, AND ED. BOARD/PROGRAM COMMITTEE

List items as applicable, e.g., original research articles and research review articles in peer-reviewed journals, refereed articles that are pedagogy or extension-related, research abstracts, books; interdisciplinary/multidisciplinary works; invited and contributed research presentations; appointments or election to study sections and editorial boards; creative or professional works; exhibitions; juried shows, honors; awards, fellowships, prizes, competitions, and other pertinent evidence.

##### BOOKS

1. Radio System Design, D. S. Ricketts, Igram Spark, 2015.
2. Electrical Solitons: Theory, Design and Applications, D. S. Ricketts and D. Ham, CRC Press, 2010.
3. The Designers Guide to Jitter in Ring Oscillators, J. A. McNeill and D. S. Ricketts, Springer Verlag, 2009.

##### BOOK CHAPTERS

1. D. S. Ricketts, Xiaofeng Li, and Donhee Ham, "Soliton Electronics," in Circuits for Emerging Technologies - CMOS and Beyond, CRC Press 2008.
2. X. Li, D. S. Ricketts, and D. Ham, "Solitons in electrical networks," McGraw-Hill 2008 Yearbook of Science and Technology, McGraw-Hill, 2008.

##### DISCUSSION PI'S WORK

1. Nature, News & Views article by Thomas H. Lee, "Electrical solitons come of age," Nature, vol. 440, 36-37, Mar. 2006.

##### JOURNAL PUBLICATIONS

###### **Graduate student author; undergraduate author**

1. J. Besnoff, H. Zhong, S. Su, R. Kaveti, N. Maiya, S. Krishna, N. Garland, A. Bandokar and D. S. Ricketts, "Sweat-powered, mm scale, continuous time sensor systems with Bluetooth Low Energy2 (BLE) Backscatter." *IEEE ACCESS*, accepted 2024.
2. W. C. Harris and D. S. Ricketts, "Maximum Gain Enhancement n Wireless Power Transfer using Anisotropic Metamaterials," Scientific Reports, Sci Rep 13, 7726 (2023). <https://doi.org/10.1038/s41598-023-32415-9>
3. J. Shen and D. S. Ricketts, "Compact W-Band "Swan Neck" Turnstile Junction Orthomode Transducer Implemented by 3-D Printing," in IEEE Transactions on Microwave Theory and Techniques, vol. 68, no. 8, pp. 3408-3417, Aug. 2020
4. **M. Dwyer** and D. S. Ricketts, "The North Carolina state university rabbit radar: Build a frequency-modulated continuous-wave radar in a day [application notes]," IEEE Microwave Magazine, vol. 21, no. 5, pp. 136–145, 2020..[Invited]
5. D. S. Ricketts, "A modern 16-qam digital radio you can design and build at home [application notes]," IEEE Microwave Magazine, vol. 21, no. 7, pp. 10–22, 2020.
6. **W. C. Harris**, D. D. Stancil, and David S. Ricketts, "Improved wireless power transfer efficiency with non-perfect lenses," Applied Physics Letters 114:14, April 2019.
7. D. S. Ricketts, E. Shi, X. Li, N. Sun, O.O.. Yildirim and D. Ham, "Electrical Solitons for Microwave Systems," IEEE Microwave Magazine, April 2019 [Invited].

8. **J. Shen** and D. S. Ricketts, "Additive Manufacturing of Complex Millimeter-Wave Waveguides Structures Using Digital Light Processing," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 67, no. 3, pp. 883-895, March 2019.
9. D. S. Ricketts, **J. Shen**, J. Dunn, "Expanding the Antenna Frontier With Antenna Synthesis and 3D Printing", (Cover article), *Microwave Engineering Europe*, Sept. 2018.
10. **D. Lal**, A. M. A. Ali and D. S. Ricketts, "Analysis and Comparison of High-Resolution GS/s Samplers in Advanced BiCMOS and CMOS," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 65, no. 5, pp. 532-536, May 2018.
11. J. Besnoff, M. Abbasi and D. S. Ricketts, "Ultrahigh-Data-Rate Communication and Efficient Wireless Power Transfer at 13.56 MHz," in *IEEE Antennas and Wireless Propagation Letters*, vol. 16, pp. 2634-2637, 2017.
12. M. Abbasi, B. Wang, S. Tamaru, H. Kubota, A. Fukushima and D. S. Ricketts, "Accurate De-Embedding and Measurement of Spin-Torque Oscillators," in *IEEE Transactions on Magnetics*, vol. 53, no. 11, pp. 1-4, Nov. 2017.
13. **V. Pasku** et al., "Magnetic Field-Based Positioning Systems," in *IEEE Communications Surveys & Tutorials*, vol. 19, no. 3, pp. 2003-2017, thirdquarter 2017.
14. W. Tai, M. Abbasi and D. S. Ricketts, "Analysis and design of high-power and efficient, millimeter-wave power amplifier systems using zero degree combiners," *IET J. of Electronics*, pp. 1-11, Jul. 2017.
15. M. Chabalko, J. Besnoff, M. Laifenfeld and D. S. Ricketts, "Resonantly Coupled Wireless Power Transfer for Non-Stationary Loads With Application in Automotive Environments," in *IEEE Transactions on Industrial Electronics*, vol. 64, no. 1, pp. 91-103, Jan. 2017.
16. Abbasi M, Ricketts DS. A high-power, broadband 245-285 GHz balanced frequency doubler in 45 nm SOI CMOS *Microwave and Optical Technology Letters*. 58: 423-426, 2016.
17. **M. E. Karagozler**, S. C. Goldstein and D. S. Ricketts, "Scalable self-assembly process for the fabrication of sub-millimetre three-dimensional cylindrical tubes," in *IET Micro & Nano Letters*, vol. 11, no. 1, pp. 4-8, 1 2016.
18. M. Abbasi, D.S. Ricketts, "A 275 GHz-285 GHz Balanced Frequency Quadrupler in 45nm SOI CMOS," *Electronic Letters*, vol.51, no.18, pp.1424-1426, Sept 2015.
19. J. Besnoff, M. Abbasi and D. S. Ricketts, "High Data-Rate Communication in Near-Field RFID and Wireless Power Using Higher Order Modulation," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 2, pp. 401-413, Feb. 2016.
20. J. Besnoff, M. Chabalko and D. S. Ricketts, "A Frequency-Selective Zero-Permeability Metamaterial Shield for Reduction of Near-Field Electromagnetic Energy," in *IEEE Antennas and Wireless Propagation Letters*, vol. 15, pp. 654-657, 2016.
21. M. J. Chabalko, J. Besnoff and D. S. Ricketts, "Magnetic Field Enhancement in Wireless Power With Metamaterials and Magnetic Resonant Couplers," in *IEEE Antennas and Wireless Propagation Letters*, vol. 15, pp. 452-455, 2016.
22. M. Chabalko and D. S. Ricketts, "Experimental characterization of Fabry-Perot resonances of magnetostatic volume waves in near-field metamaterials", *Applied Physics Letters*, 106, 062401 (2015).
23. **Ozcan, O.; Weihua Hu**; Sitti, M.; Bain, J.; Ricketts, D.S., "Investigation of tip current and normal force measured simultaneously during local oxidation of titanium using dual-mode scanning probe microscopy," *Micro & Nano Letters*, IET , vol.9, no.5, pp.332,336, May 2014
24. Ricketts, D.S.; Chabalko, M.; **Hillenius, A.**, "Tri-Loop Impedance and Frequency Matching With High- Q Resonators in Wireless Power Transfer," *Antennas and Wireless Propagation Letters*, IEEE , vol.13, no., pp.341,344, Jan. 2014.
25. **D. Arumugam**, J. Griffin, D. Stancil and D. S. Ricketts, "Three-Dimensional Position and Orientation Measurements using Magnetoquasistatic Fields and Complex Image Theory," *Antennas and Propagation Magazine*, IEEE, vol.56, no.1, pp.160,173, Feb. 2014
26. Williams, D.F.; Corson, P.; Sharma, J.; Krishnaswamy, H.; **Tai, W.**; George, Z.; Ricketts, D.S.; Watson, P.M.; Dacquay, E.; Voinigescu, S.P., "Calibrations for Millimeter-Wave Silicon Transistor Characterization," *Microwave Theory and Techniques*, IEEE Transactions on , vol.62, no.3, pp.658,668, Mar. 2014.
27. **Tai, W.**; Ricketts, D.S., "A compact, 36 to 72 GHz 15.8 dBm power amplifier with 66.7% fractional bandwidth in 45 nm SOI CMOS," *Microw. And Opt. Tech Lett.* ,vol. 56, pp.1098-2760, Nov. 2013.
28. J. Xu and D. S. Ricketts, "An Efficient, Watt-Level Microwave Rectifier Using an Impedance Compression Network (ICN) With Applications in Outphasing Energy Recovery Systems," *Microwave and Wireless Components Letters*, IEEE , vol.23, no.10, pp.542,544, Oct. 2013.

29. Arumugam, D.D.; Ricketts, D.S., "Passive orientation measurement using magnetoquasistatic fields and coupled magnetic resonances," *Electronics Letters*, vol.49, no.16, pp.999,1001, Aug. 2013.
30. Williams, D.F.; Corson, P.; Sharma, J.; Krishnaswamy, H.; **Wei Tai**; George, Z.; Ricketts, D.; Watson, P.; Dacquay, E.; Voinigescu, S.P., "Calibration-Kit Design for Millimeter-Wave Silicon Integrated Circuits," *Microwave Theory and Techniques, IEEE Transactions on*, vol.61, no.7, pp.2685,2694, July 2013.
31. **Tai, W.**; Ricketts, D.S., "74 GHz, 17.2 dBm power amplifier in 45 nm SOI CMOS," *Electronics Letters*, vol.49,no.12,pp.758,759, June 2013.
32. S. Tamaru and D. S. Ricketts, "Measurement of ultra-low power oscillators using adaptive drift cancellation with applications to nano-magnetic spin torque oscillators," *Rev. of Scien. Instr.*, vol. 84, p. 054704-7, May 2013.
33. **Arumugam, D.D.**; Ricketts, D.S., "Passive Magnetoquasistatic Position Measurement Using Coupled Magnetic Resonances," *Antennas and Wireless Propagation Letters, IEEE*, vol.12, no., pp.539,542, Apr. 2013
34. **Arumugam, D.D.**; Griffin, J.D.; Stancil, D.D.; Ricketts, D.S., "Magneto-Quasistatic Tracking of an American Football: A Goal-Line Measurement," *Antennas and Propagation Magazine, IEEE*, vol.55, no.1, pp.138,146, Feb. 2013.
35. D. S. Ricketts, M. Chabalko and **A. Hillenius**, "Experimental demonstration of the equivalence of inductive and strongly coupled magnetic resonance wireless power transfer," *Applied Physics Letters*, vol. 102, no. 5, Feb. 2013.
36. **C. Li** and D. S. Ricketts, "Loss minimization in  $\lambda/4$  impedance transformers using multiple  $\lambda/4$  segments," *Electronic Letters*, vol.49, no.4, pp.274,276, Feb. 14 2013
37. **W. Hu**, J. Bain and D. S. Ricketts, "An AFM/STM multi-mode nanofabrication approach allowing in situ surface modification and characterization," *Micro and Nano Letters*, Vol. 8, p. 43-46, Jan 2013.
38. **Arumugam, J.** Griffin, D. Stancil and D. S. Ricketts, "Error Reduction in Magnetoquasistatic Positioning Using Orthogonal Emitter Measurements," *Antennas and Wireless Propagation Letters, IEEE*, vol.11, no., pp.1462,1465, 2012
39. **R. Birt**, K. An, M. Tsoi, S. Tamaru, D. Ricketts, K. L. Wong, P. K. Amiri, K. L. Wang, and X. Li, "Deviation from exponential decay for spin waves excited with a coplanar waveguide antenna," *Applied Physics Letters*, vol. 101, no. 25, 2012.
40. S. Tamaru and D. S. Ricketts, "Experimental Study of the Variation in Oscillation Characteristics of Point-Contact-Based Spin-Torque Oscillators." *IEEE Trans. on Magnetics*, vol.3, no., pp.3000504, 2012
41. **M. E. Korogozlar**, S. Goldstein and D. S. Ricketts, "Analysis and modeling of capacitive power transfer in microsystems," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol.59, no.7, pp.1557,1566, July 2012
42. **W. Hu**, J. A. Bain and D. S. Ricketts "In-Situ quantification of electrical isolation in STM-fabricated TiOx nanostructures," *Micro and Nano Letters*, vol. 7, no. 4, pp. 334-36, Apr. 2012.
43. S. Tamaru, J. A. Bain, M. H. Kryder and D. S. Ricketts, "Theory for calculating the Green's function of magnetostatic surface waves and its application to the study of spatial diffraction patterns," *Physical Rev. B*, 84, pp.064437 (2011).
44. D.S. Ricketts, J. A. Bain, Y. Luo, S. Blanton, K. Mai and G. K. Fedder, "Enhancing CMOS using nanoelectronic devices, a perspective on hybrid integrated systems," *Proc. of the IEEE* vol.98, no.12, pp.2061,2075, Dec. 2010.
45. **R. Evarts**, L. Cao, D. S. Ricketts, N. D. Rizzo, J. A. Bain, and S. A. Majetich, "Characterization of conducting atomic force microscopy for use with magnetic tunnel junctions," *IEEE Trans. on Magnetics*, vol.46, no.6, pp.1741,1744, June 2010
46. **E.R. Evarts**, L. Cao, D. S. Ricketts, N. D. Rizzo, J. A. Bain, and S. A. Majetich, "Spin transfer torque switching of magnetic tunnel junctions using a conductive atomic force microscope," *Applied Physics Letters* 95, 132510 (2009).
47. **O. O. Yildirim**, D. S. Ricketts, and D. Ham, "Reflection soliton oscillator," *IEEE Transactions on Microwave Theory and Technique*, vol. 57, no. 10, pp. 2344-2353, Oct. 2009.
48. D. S. Ricketts, X. Li, N. Sun, K. Woo, and D. Ham, "On the self-generation of electrical soliton pulses," *IEEE J. Solid-State Circuits (JSSC)*, vol. 42, no. 8, pp. 1657-1668, Aug. 2007.
49. D. Ham, X. Li, S. A. Denenberg, T. H. Lee, and D. S. Ricketts, "Ordered and chaotic electrical solitons: communication perspectives," (**Invited**) *IEEE Communications Magazine*, vol. 44, no. 12, pp. 126-135, December 2006.
50. D. S. Ricketts, X. Li, and D. Ham, "Electrical Soliton Modelocking," (**Invited cover article**) *IEEE LEOS Newsletter*, vol. 20, no. 3, pp. 4-11, June 2006.

51. D. S. Ricketts, X. Li, and D. Ham, "Electrical Soliton Oscillator," *IEEE Trans. on Microwave Theory and Tech.*, vol. 54, no. 1, pp. 373-382, Jan. 2006.
52. R. S. Friedman, M. C. McAlpine, D. S. Ricketts, D. Ham, C. M. Lieber, "High-speed integrated nanowire circuits," *Nature*, vol. 434, p.1085, Apr. 2005.

### PEER-REVIEWED CONFERENCE/WORKSHOP PUBLICATIONS

#### **Graduate student author; undergraduate author**

1. H. Zhong and D. S. Ricketts, "14dB Active Gain Magnetic Negative Permeability Metamaterial Cell with Self-coupling Compensation," 2023 53rd European Microwave Conference (EuMC), Berlin, Germany, 2023, pp. 424-427, doi: 10.23919/EuMC58039.2023.10290148.
2. G. Garner, B. Byars, J. Wetherington, J. Besnoff and D. S. Ricketts, "Radio Disruption of Electronic Systems," GOMACTech, Charleston SC 2024
3. H. Zhong and D. S. Ricketts, "14dB Active Gain Magnetic Negative Permeability Metamaterial Cell with Self-coupling Compensation," 2023 53rd European Microwave Conference (EuMC), Berlin, Germany, 2023, pp. 424-427, doi: 10.23919/EuMC58039.2023.10290148.
4. J. Besnoff and D. S. Ricketts, "Teaching 100 remote students hands-on microwave design: Building a 16 QAM radio at home by hand," 2021 51st European Microwave Conference (EuMC), London, United Kingdom, 2022, pp. 1-4
5. J. Shen and D. S. Ricketts, "Advances in 3D additive manufacturing for complex mm-wave components and sub-systems." *IEEE Radio Wireless Week*, Jan 2020. **Invited**.
6. **M. Aiken** and D. S. Ricketts, "Simple Laminated PCB Artificial Dielectrics for mm-Wave Quasioptical Lenses," 2019 49th European Microwave Conference (EuMC), Paris, 2019.
7. J. Besnoff, Y. Buchbut, K. Scheim and D. S. Ricketts, "A 50% Fractional Bandwidth, Wireless Power Communication System Achieving 6.78 Mbps at 13.56 MHz Carrier," 2018 48th European Microwave Conference (EuMC), Madrid, 2018, pp. 178-181.
8. J. Besnoff, Y. Buchbut, K. Scheim and D. S. Ricketts, "Dynamic Impedance Matching of Multiple Loads in Wireless Power Transfer using a Genetic Optimization Approach," 2018 IEEE/MTT-S International Microwave Symposium - IMS, Philadelphia, PA, 2018, pp. 1272-1274.
9. **J. Shen, D. P. Parekh**, M. D. Dickey and D. S. Ricketts, "3D Printed Coaxial Transmission Line Using Low Loss Dielectric and Liquid Metal Conductor," 2018 IEEE/MTT-S International Microwave Symposium - IMS, Philadelphia, PA, 2018, pp. 59-62.
10. **J. Shen**, M. Abbasi, and David S. Ricketts, "3D Printed Antennas: Enabling Complex Antenna Structures," *USNC-URSI*, Jan 2018.
11. J. Besnoff, D. S. Ricketts, Y. Buchbut, G. Castillo, M. Laifendfeld and K. Scheim, "Smart wireless power: A wireless power and bi-directional LIN communication system," 2017 IEEE International Conference on Microwaves, Antennas, Communications and Electronic Systems (COMCAS), Tel-Aviv, 2017, pp. 1-3.
12. **J. Shen, M. Aiken**, M. Abbasi, **D. P. Parekh, X. Zhao**, M. D. Dickey, David S. Ricketts, "Rapid prototyping of low loss 3D printed waveguides for millimeter-wave applications," 2017 IEEE MTT-S International Microwave Symposium (IMS), Honolulu, HI, 2017, pp. 41-44.
13. D. S. Ricketts, "Analog limitations for high-speed digital radios: Where the bits stop working," 2017 IEEE 60th International Midwest Symposium on Circuits and Systems (MWSCAS), Boston, MA, 2017, pp. 37-40. **(Invited)**
14. M. Abbasi, B. Wang, S. Tamaru, H. Kubota, A. Fukushima and D. Ricketts, "Precision power measurement of spin-torque nano-oscillators using an accurate de-embedding structure and analysis," 2017 IEEE International Magnetism Conference (INTERMAG), Dublin, 2017, pp. 1-1.
15. D. Ricketts and M. Abbasi, "Analytical limits to maximum RF performance of spin torque nano-oscillators," 2017 IEEE International Magnetism Conference (INTERMAG), Dublin, 2017, pp. 1-1.
16. **J. Shen, M. Aiken**, C. Ladd, M. Dickey and D. S. Ricketts, "A Simple Electroless Plating Solution for 3D Printed Microwave Components," *IEEE Asia Pacific Microw.Conf.*, Dec 2016. **(Best paper award)**
17. **W. Harris**, T. Nichols, M. Abbasi and D. S. Ricketts, "A Simple Electroless Plating Solution for 3D Printed Microwave Components A Versatile mm-Wave Micromachined Anti-Reflective Layer," *IEEE Asia Pacific Microw.Conf.*, Dec 2016.
18. M. Abbasi and D. S. Ricketts, "W-Band Conical and Corrugated Horn Antennas Using Stereolithography 3D-Printing Technology," *IEEE Asia Pacific Microw.Conf.*, Dec 2016.

19. M. Abbasi and D. S. Ricketts, "mm-Wave and THz Multipliers: Advances and Opportunities," *IEEE Asia Pacific Microw. Conf.*, Dec 2016. **(Invited)**
20. **D. Lal**, M. Abbasi and D. S. Ricketts, "A broadband, compact 140–170GHz double side-band receiver in 90nm SiGe technology," 2016 46th European Microwave Conference (EuMC), London, 2016, pp. 687-690.
21. **Lal, D.**; Abbasi, M. and D. S. Ricketts, "A Compact, High Linearity 40GS/s Track-and-Hold Amplifier in 90nm SiGe Technology," *IEEE Custom Integrated Circuits Conf.*, Sept. 2015.
22. Besnoff, J. and D. S. Ricketts, "Wide bandwidth for high-speed communication in mid-range, resonant WPT and RFID systems," *Microwave Conference (EuMC)*, 2015 European.
23. Besnoff, J.; Ricketts, D.S., "Near field wireless power transfer and quadrature amplitude modulated (QAM) communication link," in *Wireless Power Transfer Conference (WPTC)*, 2015 IEEE , vol., no., pp.1-4, 13-15 May 2015.
24. Besnoff, J.; Ricketts, D., "Quadrature amplitude modulated (QAM) communication link for near and mid-range RFID systems," in *RFID (RFID)*, 2015 IEEE International Conference on , vol., no., pp.151-157, 15-17 April 2015.
25. **Wei Tai**; Ricketts, D.S., " A Compact, High-gain Q-Band Stacked Power Amplifier in 45nm SOI CMOS With 19.2dBm Psat and 19% PAE, IEEE PAWR Conference, Jan 2015," *IEEE PAWR Conference*, Jan 2015.
26. M. J. Chabalko, **W. C. Harris**, D. D. Stancil and D. S. Ricketts, "Experimental Characterization of Volume-mode Waves in Near-field Anisotropic Metamaterials with Application to Wireless Power Transfer," *Asia-Pacific Microwave Conference*, Nov 2014.
27. Junfeng Xu; Ricketts, D.S., "Broadband W-band On-Chip Yagi Antenna Using Superstrate for High Efficiency and Endfire Radiation" *Asia Pacific Microwave Conference*, Nov. 2014
28. Chabalko, M.J.; Laifenfeld, M.; Buchbut, Y.; Ricketts, D.S., "Resonantly-coupled wireless powered seat locomotion in automotive applications," *European Microwave Conference (EuMC)*, 2014 44th , vol., no., pp.421,424, 6-9 Oct. 2014.
29. Chabalko, M.J.; Ricketts, D.S., "The effects of magneto-static resonances in metamaterials on the quality factor of coils in near field applications," *Antennas and Propagation Society International Symposium (APSURSI)*, 2014 IEEE , vol., no., pp.426,427, 6-11 July 2014.
30. Chabalko, M.; Alarcon, E.; **Bou, E.**; Ricketts, D.S., "Optimization of WPT efficiency using a conjugate load in non-impedance matched systems.," *Antennas and Propagation Society International Symposium (APSURSI)*, 2014 IEEE , vol., no., pp.645,646, 6-11 July 2014
31. Chabalko, M.J.; Ricketts, D.S., "Low-frequency metamaterial permeability retrieval for near-field applications," *Antennas and Propagation Society International Symposium (APSURSI)*, 2014 IEEE , vol., no., pp.233,234, 6-11 July 2014
32. **Wei Tai**; Ricketts, D.S., "A W-band 21.1 dBm power amplifier with an 8-way zero-degree combiner in 45 nm SOI CMOS," *Microwave Symposium (IMS)*, 2014 IEEE MTT-S International , vol., no., pp.1,3, 1-6 June 2014
33. **Wei Tai**; Ricketts, D.S., "Watt-Level, All-Silicon mm-Wave Power Amplifiers Using Zero-Degree Combiners" *GOMACTech (Government Microcircuit Applications and Critical Technology) Conference*, April 2014
34. **Wei Tai**; Ricketts, D.S., "A Q-band power amplifier with high-gain pre-driver and 18.7 dBm output power for fully integrated CMOS transmitters," *Power Amplifiers for Wireless and Radio Applications (PAWR)*, 2014 IEEE Topical Conference on , vol., no., pp.34,36, 19-23 Jan. 2014
35. **Chen, M.W.**; Carley, L.R.; Ricketts, D.S., "A process-technology-scaling-tolerant pipelined ADC architecture achieving 6-bit and 4 GS/s ADC in 45nm CMOS," *Silicon Monolithic Integrated Circuits in Rf Systems (SiRF)*, 2014 IEEE 14th Topical Meeting on , vol., no., pp.16,18, 19-23 Jan. 2014
36. M. Trotter, J. D. Griffin, D. S. Ricketts, "Enhanced Accuracy for a Complex Image Theory Position Estimator using Frequency Diversity," *Wireless Sensors and Sensor Networks*, IEEE Topical meeting on, Feb. 2014.
37. Junfeng Xu; **Wei Tai**; Ricketts, D.S., "Microwave watt-level rectifiers for power recycling applications," *Microwave Integrated Circuits Conference (EuMIC)*, 2013 European, pp.516,519, 6-8 Oct. 2013.
38. Ricketts, D.S.; Chabalko, M.J.; **Hillenius, A.**, "Optimization of wireless power transfer for mobile receivers using automatic digital capacitance tuning," *Microwave Conference (EuMC)*, 2013 European , vol., no., pp.515,518, 6-10 Oct. 2013.
39. M. Chabalko and D. S. Ricketts, "The Effects of Magneto-static Surface Resonances in Metamaterials on the Quality Factor of Coils in Near Field Applications," *Antennas and Propagation Society International Symposium (APSURSI)*, July, 2014.
40. Trotter, M.S.; Ricketts, D.S.; Griffin, J.D., "Experimental demonstration of complex image theory for vertical magnetic dipoles with applications to remote sensing and position tracking," *Electromagnetics in Advanced Applications (ICEAA)*, 2013 International Conference on , vol., no., pp.1248,1251, 9-13 Sept. 2013.

41. **O. Ozcan, W. Hu**, M. Sitti, J. A. Bain and D.S. Ricketts, "Experimental Investigation of Force, Conduction and Growth in Nano-oxidation using scanning probe microscopy," Enabling Nanomanufacturing for Rapid Innovation, Aug. 2013. [Best Poster]
42. D. S. Ricketts and M. Chabalko, "Distributed Resonant Coil Systems for Efficient Wireless Power Transfer," Progress in Electromagnetics Research Symposium (PIERS), Aug. 2013.
43. J. Xu and D. S. Ricketts, "A Transmission line based resistance compression network (TRCN) for microwave applications," Microwave Symposium Digest (IMS), 2013 IEEE MTT-S International , vol., no., pp.1,3, 2-7 June 2013
44. D. S. Ricketts and M. Chabalko, "On the efficient wireless power transfer in resonant multi-receiver systems," Circuits and Systems (ISCAS), 2013 IEEE International Symposium on , vol., no., pp.2779,2782, 19-23 May 2013
45. **Arumugam, D.D.; Sibley, M.**; Griffin, J.D.; Stancil, D.D.; Ricketts, D.S., "An active position sensing tag for sports visualization in American football," RFID (RFID), 2013 IEEE International Conference on , vol., no., pp.96,103, April 30 2013.
46. **W. Tai**, L. R. Carley and D. S. Ricketts, "A 0.7W Fully Integrated 42GHz Power Amplifier with 10% PAE in 130nm SiGe BiCMOS," Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2013 IEEE International , vol., no., pp.142,143, 17-21 Feb. 2013
47. **M. W. Chen, D. Tian, S. Phatak**, L. R. Carley, D. S. Ricketts, "A 4GHz-Bandwidth Op-Amp Free Track-and-Hold and 6-bit Flash ADC in 45nm SOI CMOS" Silicon Monolithic Integrated Circuits in RF Systems (SiRF), 2013 IEEE 13th Topical Meeting on , vol., no., pp.126,128, 21-23 Jan. 2013
48. **D. Birt, K. An, M. Tsoi**, S. Tamaru, D. Ricketts, K.L. Wong, P.K. Amiri, K.L. Wang and X. Li," Oscillatory Spatial Intensity Pattern for Spin Waves Excited with a Coplanar Waveguide Antenna," Conference on Magnetism and Magnetic Materials, Chicago, IL, paper EC-02, Jan. 2013.
49. **C. Li** and D. S. Ricketts, "A low-loss, compact,  $\lambda/4$  power combiner architecture," Microwave Integrated Circuits Conference (EuMIC), 2012 7th European , vol., no., pp.147,150, 29-30 Oct. 2012
50. D. S. Ricketts and **A. Hillenius**, "Equivalence of inductive coupling and strongly coupled Magnetic resonance in wireless power transfer," Progress in Electromagnetics Research Symposium (PIERS), Aug. 2012.
51. **D. Arumugam**, J. Griffin, D. Stancil and D. S. Ricketts, "Experimental study on the effects of groups of people on magnetoquasistatic positioning accuracy," Antennas and Propagation Society International Symposium (APSURSI), 2012 IEEE , vol., no., pp.1,2, 8-14 July 2012
52. D. S. Ricketts, "A dispersion-tapered reflection soliton oscillator," Microwave Symposium Digest (MTT), 2012 IEEE MTT-S International , vol., no., pp.1,3, 17-22 June 2012
53. **D. Tian**, L. R. Carley and D. S. Ricketts, "Frequency Scaling of Power Reclamation Networks in Outphasing PA Architectures," Circuits and Systems (ISCAS), 2012 IEEE International Symposium on , vol., no., pp.1058,1061, 20-23 May 2012
54. S. Tamaru and D. S. Ricketts, "Origin of variation in the oscillation characteristics of point contact based spin torque oscillators," Magnetics Letters, IEEE , vol.3, no., pp.3000504,3000504, 2012
55. **W. Hu** J. A. Bain and D. S. Ricketts, "In-situ characterization using AFM probes in multiple modes," Int. Conf. Electron, Ion, Photon Beam Technology and Nanofabrication, May, 2012.
56. **Lee, B.J.; Hillenius, A.**; Ricketts, D.S., "Magnetic resonant wireless power delivery for distributed sensor and wireless systems," Wireless Sensors and Sensor Networks (WiSNet), 2012 IEEE Topical Conference on , vol., no., pp.13,16, 15-18 Jan. 2012.
57. **D. Arumugam**, J. Griffin, D. Stancil and D. S. Ricketts, "A wireless orientation sensor using magnetoquasistatic fields and complex image theory," Radio and Wireless Symposium (RWS), 2012 IEEE , vol., no., pp.251,254, 15-18 Jan. 2012
58. **W. Tai**, L. R. Carley and D. S. Ricketts, "A Q-band SiGe Power Amplifier with 15.5 dBm Saturated Output Power and 26% Peak PAE," Bipolar/BiCMOS Circuits and Technology Meeting (BCTM), 2011 IEEE , vol., no., pp.146,149, 9-11 Oct. 2011
59. **D. Arumugam**, D. Stancil and D. S. Ricketts, "Proximity and Orientation Sensing Using Magnetoquasistatic Fields and Complex Image Theory" Vehicular Technology Conference (VTC Fall), 2011 IEEE , vol., no., pp.1,5, 5-8 Sept. 2011
60. **W. Hu**, J. Gu, **Z. George** and D. S. Ricketts, "Directed scanning probe nanomanufacturing of lateral Ti-TiO<sub>2</sub>-Ti junctions for low capacitance MIM rectenna diodes," Micro and Nano Engineering Conf., Berlin, Sept. 2011.
61. **D. Arumugam**, J. Griffin, D. Stancil and D. S. Ricketts, "2-Dimensional Position Measurement using Magnetoquasistatic Fields," Antennas and Propagation in Wireless Communications (APWC), 2011 IEEE-APS Topical Conference on , vol., no., pp.1193,1196, 12-16 Sept. 2011

62. **W. Hu, Y. Tang, Y. Zhang**, J. Gu, S. Tamaru, J. A. Bain, L. R. Carley, R. F. Davis, G. K. Fedder and D. S. Ricketts, "TI/TIO<sub>2</sub> nanodevice fabrication using compliant probes and CMOS probe-arrays," Technologies for Future Micro-Nano Manufacturing, Napa Valley, CA, Aug. 2011.
63. **D. Arumugam**, J. Griffin, D. Stancil and D. S. Ricketts, "Higher Order Loop Corrections for Short Range Magnetoquasistatic Position Tracking," Antennas and Propagation (APSURSI), 2011 IEEE International Symposium on , vol., no., pp.1755,1757, 3-8 July 2011
64. **M. E. Karagozler, A. M. Thaker**, S. Goldstein and D. S. Ricketts, "Electrostatic-actuation generation and control of micro robots in a post-processed HV SOI CMOS," Circuits and Systems (ISCAS), 2011 IEEE International Symposium on , vol., no., pp.2509,2512, 15-18 May 2011
65. **W. Hu**, S. Tamaru, J. A. Bain and D. S. Ricketts, "High Current Pulse Generation for Thermal Surface Modification using Standard STM," Int. Conf. Electron, Ion, Photon Beam Technology and Nanofabrication, May. 2011.
66. J. R. Smith, D. S. Ricketts and J. A. Bain, "Localized thermal modification of surfaces via pulsed electron bombardment from an STM tip," Int. Conf. Electron, Ion, Photon Beam Technology and Nanofabrication, May. 2011.
67. **D. Arumugam**, J. Griffin, D. Stancil and D. S. Ricketts, "Long Range Magnetoquasistatic Position Tracking using a Simple Active RFID Tag," IEEE Int. Conf. RFID, Apr. 2011.
68. S. Tamaru and D. S. Ricketts, "Influence of the bias field orientation on the interaction strength between two closely formed spin torque oscillators," Int. Magnetism Conf., paper CO-05, Taiwan, Apr 2011.
69. **E.R. Evarts, R.A. Booth, L.R. Shah, Y. Tang**, S. Tamaru, D.S. Ricketts, J.A. Bain, S.A. Majetich,"Sub-30 nm Magnetic Tunnel Junction and Spin Valve Nanopillar Analysis Using Conductive Atomic Force Microscopy," Int. Magnetism Conf., paper BB-03, Taiwan, Apr 2011.
70. J. R. Smith, **W. Hu, Y-Y Dang, O. Ozcan**, M. Sitti, J. A. Bain, D. S. Ricketts, R. Davis, "Scanning Probe Nanomanufacturing on Si: Surface Characterization of the Process Technique," Materials Research Symposium, paper G1.5, Nov. 2010
71. **E. R. Evarts**, M. Moneck, R. A. Booth, C. Hogg, D. S. Ricketts, J-G Zhu, J.A. Bain, and S. A. Majetich, "Spin Torque Switching of 26 nm Diameter Magnetic Tunnel Junction Using a Conductive Atomic Force Microscope," Conference on Magnetism and Magnetic Materials, Atlanta, GA, paper FC-13, Nov. 2010.
72. **E. R. Evarts, T.T. Farkas, B. Tsukerman**, L. Cao, D. S. Ricketts, G. Markovich, J.A. Bain, and S.A. Majetich, "Noise Measurements on Magnetic Tunnel Junction Nanopillars using Conductive Atomic Force Microscopy," Conference on Magnetism and Magnetic Materials, Atlanta, GA, paper CB-10, Nov. 2010.
73. **M. W. Chen** and D. S. Ricketts, "An 8.6GHz 42ps Pulse-Width Electrical Mode-Locked Oscillator," International Solid-State Circuits Conference (ISSCC), pp. 500-501, Feb. 2010.
74. D. S. Ricketts, L. Cao and S. Tamaru, "Spin-torque oscillator arrays as a solution for line width reduction in RF applications", Conference on Magnetism and Magnetic Materials, paper EY-01, Washington D.C., Dec. 2009.
75. D. S. Ricketts, T. Schlesinger, Y. Luo and J. Bain, "Materials and Devices for Hybrid CMOS Circuits: Expanding the Functionality of Nanoscale CMOS," Nano-DDS Conference, Ft. Lauderdale, FL, Oct. 2009 (Invited).
76. D. S. Ricketts and S. Bruck, "Stochastic Logic", NRI-MIND, Architectures for post- CMOS switches (Invited), Notre Dame, IN, Oct. 2009.
77. D. S. Ricketts, X. Li and D. Ham, "Soliton Electronics," CMOS Emerging Technology Workshop, Whistler, Canada, 2007. (invited)
78. W. F. Andress, D. S. Ricketts, X. Li, and D. Ham, "Passive & active control of regenerative standing & soliton waves," (Invited) Proc. of the IEEE Custom Integrated Circuits Conference, pp. 29-36, Sept. 2006.
79. D. S. Ricketts, X. Li and D. Ham, "Taming the electrical soliton: A new direction in picosecond electronics," Radio Frequency Integrated Circuits (RFIC) Symposium, 2006 IEEE , vol., no., pp.4 pp.,24, 11-13 June 2006
80. D. S. Ricketts and D. Ham, "A chip-scale electrical soliton modelocked oscillator," IEEE International Solid-State Circuits Conference (ISSCC), pp. 432-433, Feb 2006.
81. D. S. Ricketts, X. Li, M. DePetro, and D. Ham, "A self-sustained electrical soliton oscillator," Microwave Symposium Digest, 2005 IEEE MTT-S International , vol., no., pp.4 pp.,, 12-17 June 2005
82. D. Ham, W. Andress, and D. S. Ricketts, "Phase noise in oscillators," (Invited) Int. Workshop on Sip/SoC Integration of MEMS and Passive Components with RF-ICs, March 2004.

INVITED CONFERENCE PRESENTATIONS (WITHOUT PAPERS)

**Graduate student author; undergraduate author**

1. D. S. Ricketts, W. Harris, J. Zhu, D. Baron, "Dynamic artificial surfaces for mm-wave imaging using photon induced plasmas in silicon lenses." DMI Online Workshop on Energy/Quantum/Metamaterials, Dec, 2020.
2. D. S. Ricketts, "Lessons from Build-a-Radio/Radar in a Day: The Ins and Outs of Experiential Design for Students," European Microwave Week, Teaching Microwave Engineering Special Session, Sept 2020.
3. M. Abbasi and D. S. Ricketts, "100 Gb/s All-electronic Radios: Opportunities and Challenges", GomacTech, Mar. 2014
4. **W. Tai, C. Li, Z. Li, G. Yahalom**, D.S. Ricketts, V. Stojanovic and J. Dawson, "A 45 GHz Asymmetric Multilevel Outphasing Transmitter in 45nm SOI CMOS," Student Research Int. Solid-State Circuits Conf, IEEE, Feb. 2012.
5. J.R. Smith, **W. Hu, Y.Y. Dang, O. Ozcan**, M. Sitti, J. Bain, R. Davis and D. S. Ricketts, "Writing Si nanowires on Si (100) with an STM tip: surface preparation and initial results," Materials Research Symposium, M11.50, Boston, MA, Nov. 2009
6. R. S. Friedman, M. C. McAlpine, D. S. Ricketts, D. Ham, C. M. Lieber, "Fully integrated high frequency nanowire ring oscillators," Materials Research Symposium, Mar. 2005.
7. D. S. Ricketts, "Current sensing and accuracy for CPU multi-phase DC-DC converters: the sub 20 mV challenge," IBM Power Delivery Symposium, 2002.

#### ACADEMIC WORKSHOPS and SHORT COURSES (Chair or Co-Chair)

1. RF and Electronic Warfare Workshop with NSA. Dec. 2023.
2. "Build a Foxhole Radio" International Microwave Symposium, San Diego, CA June, 2023
3. RF Engineering workshop, US Navay Academy, May 2023
4. RF Bootcamp in residence course, delivered at UT Dallas in collaboration with Texas Analog Center of Excellence. May 2023.
5. 12<sup>th</sup> Tom Brazil Doctoral School of microwaves "Build a Frequency Modulated Continuous Wave Radar in 1-day" IEEE European Microwave Week, Milan, Italy, Sept 2022.
6. 11<sup>th</sup> Tom Brazil Doctoral School of microwaves "Build a modern digital radio" IEEE European Microwave Week, London, UK, June 2021.
7. "Build a NIST Atomic Clock Radio" International Microwave Symposium, Denver, Co June, 2022.
8. 5th European Microwave Student and Doctoral School: "Build a Frequency Modulated Continuous Wave Radar in 1-day" IEEE European Microwave Week, Utrecht, NL 2020 (virtual).
9. Frequency-Modulated Continuous Wave Radar in 1-day", European Microwave, Utrecht, NL, 2020.
10. "4<sup>th</sup> European Microwave Student and Doctoral Schools: Build a modern digital radio," IEEE , IEEE European Microwave Week, Paris, France, Oct 2019.
11. "Build a 950 MHz radar in a day," IEEE Int. Microwave Symposium, Boston, MA, June 2019.
12. "Design, Fab and Test Your Own Microwave Component," Industry Workshop, IEEE Int. Microwave Symposium, Boston, MA, June 2019..
13. "From Bits to Waves: Building a Modern Digital Radio in 1 Day – Hand-on Workshop," IEEE Asia Pacific Microwave Conference, Kyoto, Japan, 2018.
14. "4<sup>th</sup> European Microwave Student and Doctoral Schools: Build a modern digital radio," IEEE , IEEE European Microwave Week, Madrid, Spain, Sep 2017.
15. "Build a 16 QAM Radio – Student Design Competition," IEEE Int. Microwave Symposium, Philadelphia, PA, June 2018.
16. "Design, Fab and Test Your Own Microwave Component," Industry Workshop, IEEE Int. Microwave Symposium, Philadelphia, PA, June 2018.
17. "3<sup>rd</sup> European Microwave Student and Doctoral Schools: Build a modern digital radio," IEEE , IEEE European Microwave Week, Nuremberg, Germany, Oct 2017.
18. "Build a Modern Digital Radio in a day," Int. Microwave Symposium, Honolulu, HI, June 2017.
19. "From Bits to Waves: Building a Modern Digital Radio in 1 Day – Hand-on Workshop," IEEE Asia Pacific Microwave Conference, New Delhi, India, Nov 2016.
20. "From Bits to Waves: Building a Modern Digital Radio in 1 Day – Hand-on Workshop," IEEE European Microwave Week, London, UK, Oct 2016.
21. "From Bits to Waves: Building a Modern Digital Radio in 1 Day – Hand-on Workshop," EDICON, Boston, MA, Sep. 2016.
22. "Emerging devices for Microwave Circuits and Systems," IEEE Int. Microwave Symposium, San Francisco CA,, May 2016.

23. "Build a Modern Digital Radio in a day," IEEE Int. Microwave Symposium, San Francisco, CA, May 2016.
24. "Build a Modern Digital Radio in a day," IEEE Radio Wireless Week, Austin, Texas, Jan, 2016.

#### INVITED RESEARCH PRESENTATIONS, Universities and Industry

1. "From one to one million Volts," ECE Colloquim, NCSU Apr. 2024
2. "Live from Faraday's Lab": An Intuitive and Historical Perspective on Electromagnetism" IEEE MTT Webinar, May 2022.
3. "NCSU Rabbit Radar: Design, Simulation & Building your own Frequency Modulated Continuous Wave Radar at Home," IEEE MTT-S Virtual Lecture, Sept, 2020
4. "From Bits to Waves - Building a Modern Digital Radio," Cadence Live, August 2020.
5. "Data, Sensors and New Technologies for Smart Cities," RMIT, Melbourne Australia, Mar 2019.
6. "New Approaches to IoT in Smart Cities," Western Sydney University, Sydney, Australia, Mar 2019.
7. "Enhancing, Shaping and Steering WPT Fields," WPT NSF ERC Industry Workshop, Alexandria, VA, Dec 2018.
8. "High-speed GaN RF DC-DC Converter design," Power America Webinar, NCSU, Oct. 2018.
9. "High-speed Communication & Field Enhancement Using Artificial Materials," Pennsylvania State University, Oct 2018.
10. "Modern Digital Radios," EuMW Microapp Lecture, Madrid Sept. 2018.
11. "Sensors and Networks for Smart Cities," City of San Diego, CA, Apr 2018.
12. "Emerging Technologies in Sensors for Smart Cities," Facebook, Dublin, Feb 2018.
13. "Science in Microwaves," NSF Workshop at IMS2017, June 2017.
14. "Magic with Magnetic Fields: NFL Football Tracking", Raleigh Engineers Club, Raleigh, NC, June 2017.
15. "Maximum power and phase noise in spin-torque oscillators," AIST Dec 2016.
16. "High-power, broadband multipliers for high-speed microscale radios," IEEE IMS invited workshop presentation, May 2016.
17. "Advances in wireless power transfer research: challenges and opportunities," General Motors, Feb. 2016.
18. "Magic with magnetic fields: NFL football tracking and advances in wireless power transfer & communication," Univ. of Washington, Feb, 2015.
19. "State of the art and future of high-speed wireless transceivers: Opportunities and challenges for near-THz communication," CMOS Emerging Technologies Conference, **Plenary, Invited**, May 2015.
20. "Advances in wireless power transfer research from academia: Challenges and opportunities," Wireless Power Summit, **Invited**, Berkeley, CA, Nov 2014.
21. "Advances in high-speed integrated and nanoelectronics," AIST Nov 2014.
22. "Watt-level, Highly Efficient, Fully Integrated all-Silicon Linear Power Amplification for mm-Wave Radar and Communications," Berkeley Nov. 2014.
23. "High-speed integrated circuits: From water waves to optical sampling," Analog Devices, Oct 2014.
24. "Advanced RF substrates: Applications in mm-wave electronics," DuPont 2014.
25. "Advanced mm-wave Circuits and Systems," Nuvotronics, 2014.
26. "Watt-level, Highly Efficient, Fully Integrated all-Silicon Linear Power Amplification for mm-Wave Radar and Communications," University of Delft, Netherlands, 2014
27. "Watt-level, Highly Efficient, Fully Integrated all-Silicon Linear Power Amplification for mm-Wave Radar and Communications," University of Pavia, Italy, 2014
28. "Magnetoquasistatics: Emerging Applications in Sports Visualization and Enhanced Wireless Power Transfer," University of Perugia, Italy, 2014
29. "Power, Sensing and Communication: Opportunities for a wireless world," General Motors Research, Herzlia Israel, Oct. 2013.
30. "Enabling Rapid Innovation in Nanomanufacturing," ENRI NSF workshop keynote, Napa, CA. Aug. 2013.
31. "Watt-level, Highly Efficient, Fully Integrated Linear Power Amplification for mm-Wave Radar and Communications," MIT, Boston Ma, May 2013.
32. "Watt-level, Highly Efficient, Fully Integrated Linear Power Amplification for mm-Wave Radar and Communications," Qualcomm, San Diego, CA, Jan 2013.
33. "Impedance Matched Magnetoquasistatic Wireless Power: On the equivalence of inductive and strongly coupled magnetic resonance and the challenges of multiple and mobile receivers" Qualcomm, San Diego, CA, Jan 2013.

34. RF from Kilometer to Millimeter Waves: NFL Football Tracking and High-power mm-Wave Circuits and Systems,” POSTECH, Korea Aug 2012 (Distinguished Lecturer)
35. “Watt-level, Highly Efficient, Fully Integrated Linear Power Amplification for mm-Wave Radar and Communications,” Jet Propulsion Laboratory, Pasadena, CA, Jul 2012.
36. “NFL Football Tracking, Microrobots and Nanoelectronics: Novel applications of Analog Circuits, E&M and MEMS,” University of FL, Apr 2012.
37. “RF devices, circuits & systems: from nanometers to kilometers,” University of Illinois, Urbana Champagne, Apr 2012.
38. “Applications of Analog Circuits and Electromagnetics in mm-wave RF and  $\mu$ Robots,” NCSU Mar 2012.
39. “RF from Kilometer- to Millimeter-waves: NFL Football Tracking and Power Amplifier Circuits & Systems,” UMich. Mar 2012.
40. “RF devices, circuits and systems: from nanometer to kilometer” University of Utah, Feb 2012
41. “NFL Football Tracking and Microrobots: Novel Applications of Analog Circuits, MEMS and E&M,” Harvard University, Feb 2012
42. “RF devices, circuits and systems: from nanometer to kilometer,” Duke Univ, Jan 2012
43. “At the boundaries of high-frequency analog & RF ICs: Speed, energy and uncertainty”, Univ. NC State, NC, Dec 2011, (**Invited, Distinguished Lecturer**)
44. “Quasistatics in E&M: Sports Visualization, Wireless Power and Microrobots,” Ga Tech, GA Nov. 2011.
45. “RF devices, circuits and systems: from nanometer to kilometer,” Univ. of Texas, Austin, Oct 2011
46. “RF devices, circuits and systems: from nanometer to kilometer,” Princeton Univ., Oct 2011
47. “High-speed PA and ADCs,” Univ. Wisconsin, Oct. 2011
48. “At the boundaries of high-frequency analog & RF ICs: Speed, energy and uncertainty”, GA Tech, GA, May 2011
49. “RF PA’s and spin-torque oscillators for RF,” University of FL, Mar, 2011
50. “Tip-directed, Field-assisted Nanofabrication,” NIST, Mar 2011.
51. “Extending the boundaries of analog and RF electronics,” Brown Univ., Mar, 2011.
52. “Nanoscale magnetism for integrated power conversion and RF,” ARL, Jan, 2011.
53. “Ultimate limitation of conversion in conventional ADCs,” ONR Superconducting Electronics Program, San Diego, Jan. 2011.
54. “Tip-assisted, field emission nanofabrication,” Zyvex Corp., Apr., 2010.
55. “Tip-assisted Nanofabrication,” Worcester Polytechnic Institute, MA, Mar. 2010.
56. “Spin Torque Oscillators for Agile RF,” DARPA YFA Program, Oct. 2009.
57. “Perspectives on electrical oscillators,” IBM Research, NY, Apr., 2009
58. “Electrical oscillators and phase noise,” NIST, Boulder, CO, Oct. 2008
59. “Creativity in science and engineering,” Innovation in Science and Engineering, Harvard University, Oct. 2008
60. “The Double Helix, a case study in scientific discovery,” Innovation in Science & Technology, Paris University Consortium, Paris France, 2008.
61. “Creativity in science and engineering,” Innovation in Science & Technology, Paris University Consortium, Paris France, 2008.
62. “New directions : soliton mode-locking and nanowire circuits,” CMU, Sept. 2006
63. “Electrical soliton oscillators” University of Michigan, Mar, 2006
64. “Electrical soliton oscillator and nanowire Circuits,” University of California, Berkeley, Apr. 2006
65. “Electrical soliton oscillators,” Cornell University, Mar 2006.
66. “Electrical solitons,” The Cooper Union, Feb. 2006.

#### STEM Workshops, K-12

1. STEM workshop for middle-school students in collaboration with Naval Information Warfare Center Atlantic STEM. July 2023.
2. IEEE Project CONNECT workshop teaching High School how to build AM radio. June 2023.

### **III.C. ORGANIZATION PARTICIPATION**

Participation in centers, consortia, institutes, interdisciplinary/multidisciplinary activities and other organized scholarly efforts between departments within and across colleges or institutions

N/A

### **IV. EXTENSION AND ENGAGEMENT WITH CONSTITUENCIES OUTSIDE THE UNIVERSITY**

Faculty Affiliate (2023-) Bloomberg Cities Center, Kennedy School of Government  
Faculty Associate (2014-), Innovation Fellow (2011-2014) Technology and Entrepreneurship Center, School of Engineering and Applied Science (SEAS), Harvard University. Courtesy appointment in SEAS for collaboration on innovation with students and faculty. Guest lecture in ES139/239 courses and assist with program development for symposia.

### **IV.A ACCOMPLISHMENTS**

List accomplishments as applicable, e.g., bulletins, brochures, reports, pamphlets, non-refereed publications, computer software, educational videotapes, slide sets, popular press articles, and other pertinent evidence.

Experiential ECE Lectures – 800,000 You Tube views (two lectures)

Online dissemination of RF system design - ~**200,000 You Tube** views. Non-NCSU watch **800+ hours viewed per month** of PIs RF system design YouTube videos.

Developed two online courses including 70 video lectures and 20 laboratory assignments.

[www.rickettslab.org/radiosystemdesign](http://www.rickettslab.org/radiosystemdesign)

[www.rickettslab.org/adc](http://www.rickettslab.org/adc)

### **IV.B. PROGRAM IMPACTS**

Describe results/impact of accomplishment.

N/A

## **VI. SERVICE TO THE UNIVERSITY AND PROFESSIONAL SOCIETIES**

University service (department, college, and university committees and governance organizations); state, regional, national and international professional activities and committee work, including professional associations.

### DEPARTMENT SERVICE

Teaching Review Committee F22-  
Promotion, Tenure Committee Co-Chair 2023  
Marketing and Communication (ECE Department) – 2020-22  
ECE Open House (ECE Department) – 2020-  
Faculty Search Committee (ECE Department) – 2017, 2019, 2022  
Course Curricula Committee (ECE Department) - 2015-present  
Senior Design Director Search Committee (ECE Department) - 2014  
Participated in Engineering Open House (ECE Department), 2014

### UNIVERSITY SERVICE

N/A

### PROFESSIONAL SOCIETIES

**Chair**, IEEE Chapter ACME (Joint chapter of Antennas and Propagation (AP), Electronic Packaging Society (EP), Microwave Theory and Techniques (MTT), and Electron Devices (ED) 2019-2023

Technical Committee **Chair** for IEEE T-MTT 9 Society 2020-2022

Technical Committee **Vice-chair** for IEEE T-MTT 7 Society 2015-2019

Technical Program **Chair**: Enabling Nanomanufacturing for Rapid Innovation, TRC/NSF Workshop, Aug. 2013

Technical Program Committee (member) – IEEE International Microwave Symposium 2014-;

Technical Program Committee IEEE BioWireless 2012-2015.

Session Chair - Nanotechnology, CMOS Emerging Technologies Conf., Banff, Canada 2009; NANO-DDS, Chemically-Synthesized, Biomimetic Systems and Biologically-Inspired Architectures Session, August 2011.

NSF Panelist (6 panels)

Reviewer for journals: ACS Nano Letters, Journal of Solid State Circuits (IEEE) Electron Device Letters (IEEE) Transactions on Circuits and Systems (IEEE) Proceedings of the National Academy of Sciences, MacArthur Foundation (Fellows program) Nano Letters, Sensors Journal of Applied Physics, Journal of Emerging and Selected Topics in Power Electronics, IET Circuits, Devices & Systems, IEEE Transactions on Power Electronics, IEEE Antennas and Wireless Propagation Letters, IEEE Transaction on Antennas and Propagation, IEEE Microwave and Wireless Components Letters, IEEE Transactions on Biomedical Circuits and Systems, Micromachines, IET Microwaves, Antennas & Propagation, International Journal of Circuit Theory and Applications, Scientific Reports.