

## AMENDED APPENDIX A-03

### Invalidity Chart for U.S. Patent No. 8,717,101 (“’101 Patent”)<sup>1</sup> U.S. Patent Publication No. 2009/0212863 (“*Ishimaru*”)

#### I. Overview

Claims 1-2, 10-11, 17-18 and 21-22 of the ’101 Patent are anticipated and/or rendered obvious by:

- U.S. Patent Publication No. 2009/0212863 (“*Ishimaru*”),<sup>2</sup> alone or in combination with the knowledge of a person of ordinary skill in the art (“POSITA”).

Claims 1-2, 10-11, 17-18 and 21-22 of the ’101 Patent are obvious in view of:

- *Ishimaru* in view of Linden T. Harrison, Current Sources & Voltage References (2005) (“*Harrison*”).<sup>3</sup>

Claim 20 of the ’101 Patent is obvious in view of:

- *Ishimaru* in view of Johnson, Silicon-Germanium BiCMOS HBT Technology for Wireless Power Amplifier Applications, IEEE Journal of Solid-State Circuits, Vol. 39, No. 10, (Oct. 2004) (“*Johnson*”)<sup>4</sup>; or
- *Ishimaru* in view of *Harrison* and *Johnson*.

The following additional references are illustrative of the state of the art and knowledge of a POSITA:

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<sup>1</sup> In addition to the ’101 Patent, Complainants assert a continuation patent in the same patent family, US 9,917,563 (“the ’563 Patent”). These contentions refer to the two patents, collectively, as the “Group 1 Patents.”

<sup>2</sup> *Ishimaru* published on August 27, 2009 and is prior art to the ’101 Patent at least under Pre-AIA 35 U.S.C. § 102(b).

<sup>3</sup> *Harrison* was published in 2005 and is prior art to the Group 1 Patents under Pre-AIA 35 U.S.C. § 102(b).

<sup>4</sup> *Johnson* published in October 2004 and is prior art to the Group 1 Patents at least under Pre-AIA 35 U.S.C. § 102(b).

- *Grebene*, Bipolar and MOS Analog Integrated Circuit Design (2003) (“*Grebene*”) was published in 2003 and is prior art to the Group 1 Patents under Pre-AIA 35 U.S.C. § 102(b).
- *Gray*, Analysis and Design of Analog Integrated Circuits (5<sup>th</sup> Ed 2009) (“*Gray*”) was published in 2009 and is prior art to the Group 1 Patents under Pre-AIA 35 U.S.C. § 102(b).
- Barrie Gilbert, “Bipolar Current Mirrors,” Chapter 6 in Tomazou *et al.*, Analogue IC Design: The Current-Mode Approach (Reprinted 2008) (“*Gilbert*”) was published in 2008 and is prior art to the Group 1 Patents under Pre-AIA 35 U.S.C. § 102(b).
- *Illingworth*, Dictionary of Electronics (3<sup>rd</sup> Ed. 1998). *Illingworth* published in 1998 and is prior art to the Group 1 Patents at least under Pre-AIA 35 U.S.C. § 102(b).
- *Laplante*, Comprehensive Dictionary of Electrical Engineering (2nd Ed. 2005). *LaPlante* published in 2005 and is prior art to the Group 1 Patents at least under Pre-AIA 35 U.S.C. § 102(b).
- U.S. Patent Pub. 2011/0128078 to Doherty *et al.*, “System and Method of Prebias for Rapid Power Amplifier Response Correction” (“*Doherty*”) was published on June 2, 2011 and is prior art to the Group 1 Patents under at least Pre-AIA 35 U.S.C. § 102(e).
- Japanese Patent Publication No. 2009-283991 to Akagi (Certified Translation) (“*Akagi*”). *Akagi* published on December 3, 2009 and is prior art to the Group 1 Patents at least under Pre-AIA 35 U.S.C. § 102(b).
- U.S. Patent Publication No. 2004/0232982 to Ichitsubo *et al.*, “RF Front-End Module for Wireless Communication Devices” (“*Ichitsubo*”), published November 25, 2004 and is prior art to the Group 1 patents under Pre-AIA 35 U.S.C. § 102(b).
- TriQuint Semiconductor, Application Note TVS Protection and Bias Sequencing for HBT Amplifiers (June 2009) (“*Triquint*”) published in 2009 and is prior art to the Group 1 Patents under Pre-AIA 35 U.S.C. § 102(b).

Respondent’s contentions and claim charts take into account Complainants’ apparent constructions. Respondent’s assertion that a particular limitation is disclosed by a prior-art reference, or Respondent’s assertion that a particular claim limitation is disclosed by a prior-art reference in a particular manner, may be based in whole or in part on Complainants’ apparent claim interpretations, infringement theories, and/or mappings. In relying on Complainants’ apparent claim interpretations, infringement theories, and/or mappings are mappings, Respondent does not admit that Complainants’ apparent claim interpretations, infringement theories, and/or mappings are supportable or proper or that the claim limitations in question are definite or otherwise amenable to construction. Respondent will argue for appropriate constructions of any term or claim of any patent at issue in this action pursuant to the procedural schedule.

Respondent reserves the right to modify and/or amend the analysis in this chart based on claim constructions and/or any changes or explanations of apparent claim constructions, infringement theories and/or mappings.

The citations to portions of any prior-art reference in this chart are exemplary only. Respondent will rely on the entirety of the references cited in this chart to show that the asserted claims are invalid. Discovery is ongoing and Respondent will update this chart as appropriate based on the results of its investigation, including third-party discovery.

## **II. State of the Art**

This section provides evidence of the state of the art, using references that reflect the general knowledge, skill, common sense, and creativity possessed by a POSITA as of the claimed priority date of May 13, 2011 for the Group 1 Patents. The references below provide evidence of the conventional purposes and structures of well-known components and functionality in the art, further informing the motivations to modify and/or combine the references as explained in these invalidity contentions. The references provide evidence of the predictability of the subject matter of the Group 1 Patents, and the associated knowledge and skill of the POSITA to be taken into account when considering the reasonable expectations of success for the implementations, modifications, and combinations of the references referenced in these invalidity contentions.

- A. The Group 1 Patents' Purported Problem of Gain Being Too Low at Startup of an RF Power Amplifier, and the Purported Solution of Increasing Bias Current at Startup Using RC Networks Was Well Known to a POSITA in the Prior Art.

As shown by the following references, the startup gain characteristics of RF power amplifiers due to thermal effects, and the solution of boosting bias current at startup to increase gain using RC "speed up" circuits, was well known to a POSITA before the purported invention of the Group 1 Patents.

- 1. *Doherty* - U.S. Patent Pub. No. 2011/0128078 ("Doherty")

The gain and phase response of a PA varies with temperature such that at temperatures below the steady-state operating temperature, the actual gain exhibited by the PA having a specific bias signal applied thereto will be less than the expected gain of the PA at steady-state operating temperatures in response to that same specific bias signal, and correspondingly, the actual phase response at a specific bias may be different from the expected phase response of the PA at steady-state operating temperatures. As the PA warms up, the actual gain of the PA increases to its expected value while the phase response of the PA approaches an expected steady-state phase response. In order to achieve a desired target operating gain and phase response, a standard or steady-state bias level can be applied to the PA while the PA is operating at its

steady-state operating temperature, but at temperatures below the steady-state operating temperature, the standard bias level is insufficient to achieve the target operating response.

*Doherty*, ¶ 6.

Due to its profound affect on the gain and phase response of the PA, one main contributor to unwanted changes in a PA's response and dynamic EVM is thermal changes of the PA caused by dynamic heating effects. Under pulsed conditions, the PA's temperature fluctuates between idle temperatures and its steady-state operating temperature, which in turn causes variations in the gain and phase of the PA away from the target operating response. One particular situation for which this can occur, is when the PA receives an RF signal data burst, after it has remained idle long enough that its temperature has fallen below its steady-state operating temperature. In one standard RF transmitter application, a Tx enable is received 500 ns to 1  $\mu$ s before the RF signal data to be transmitted is received. If the PA is sufficiently small, this time period is long enough to allow the PA to turn on and warm-up to its steady-state operating temperature. If the PA is large, the time period between receipt of the Tx enable and the receipt of RF signal data may be shorter than the time the PA needs to reach its steady-state operating temperature. In this case, some of the RF signal data may be received and amplified while the PA is in a thermally changing state during which the gain and phase response of the amplifier is also changing. This occurs primarily at the beginning of the pulse sequence, when the PA is coolest and hence at a temperature farthest from its steady-state operating temperature.

*Doherty*, ¶ 8.

In order to ensure low dynamic EVM and an output signal that is not distorted by unwanted gain and phase variations, a PA is generally not used unless it is thermally stable. A common approach to avoid the problem of dynamic EVM is simply to wait until a PA is thermally stable before using it to amplify the signal. A second common approach is to speed up the gain and phase response of the PA by applying an external resistor and speed-up capacitor to provide more forward current earlier to the PA. Although the speed-up capacitor can improve the time response of the PA, as a passive mechanism it cannot provide the additional forward current until the RF input signal itself arrives. Consequently, the beginning of the RF signal data will suffer from some amount of dynamic EVM and the additional current may not be sufficient to bring the PA into a thermally stable state at a desired rate.

*Doherty*, ¶ 9.

2. *Ishimaru* - US Patent Publication No. 2009/0212863 (“*Ishimaru*”)

In the power amplifier of the invention, at a start of power amplification by an amplifier transistor **103** serving as an amplification section, a speedup circuit **122** transiently increases a bias which is fed to the amplifier transistor **103** via a bias power source section composed of a bias circuit **111** and a power source circuit **112**. As a result, the power amplification factor of the amplifier transistor **103** is transiently increased at the start of power amplification by the amplifier transistor **103**. Thus, the time elapsing until temperature variations due to heat generation of the amplifier transistor **103** come to an equilibrium on the whole circuit is shortened, with a result of reduced distortion of the amplification signal such as a modulated-wave signal. Accordingly, in the invention, it becomes possible to suppress distortion increases of an amplification signal due to heat generation at the start time without using any temperature sensing element.

*Ishimaru*, Abstract; see also ¶ 7, ¶ 13, Fig. 1.

Next, FIG. 3 shows an example (simulation result) of transient response of the operating current (collector current Ic3) of the amplifier transistor 103 in the power amplifier of this embodiment. In this embodiment, the current to be fed from the bias transistor 107 to the amplifier transistor 103 is forcedly increased at turn-on of the amplifier, with the result that the value of the operating current Ic3 comes to a steady state in about 4 the time of transient response of the comparative example of FIG. 2. Thus, occurrence of distortions of the amplification signal due to temperature variations in the amplifier circuit is suppressed, so that the linearity of the circuit in burst operation is improved. That is, gain variations due to collector current variations of the power amplifier using a bipolar transistor can be compensated.

*Ishimaru*, ¶ 54, Fig. 1, Fig. 2, Fig. 3.

In the power amplifier of this embodiment also, the capacitance value of the capacitance element **121** of the speedup circuit **122** is adjusted so as to cancel transient variations in gain due to the temperature variations at a start of power amplification. As a result of this, deterioration of the linearity due to variations of amplification gain can be canceled so that the value of dynamic EVM (error vector magnitude) can be improved.

*Ishimaru*, ¶ 55, Fig. 1.

Fig.2 PRIOR ART

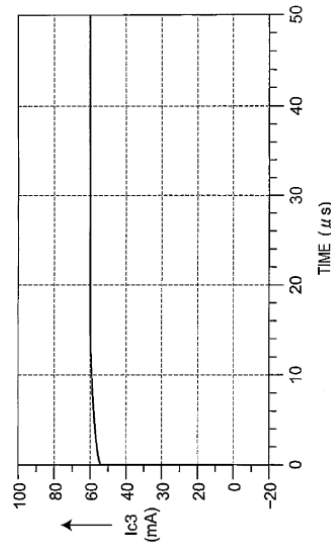
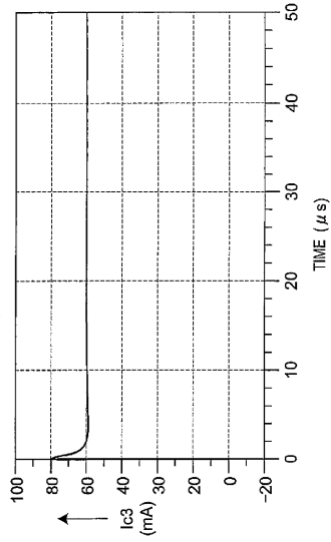
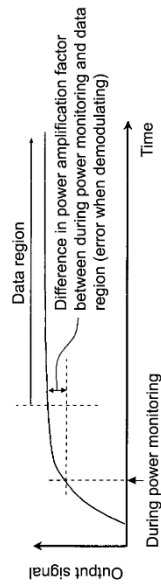


Fig.3



3. Akagi – Japanese Patent Application Publication No. JP 2009-283991 A – (Published Dec. 3, 2009) (“Akagi”)

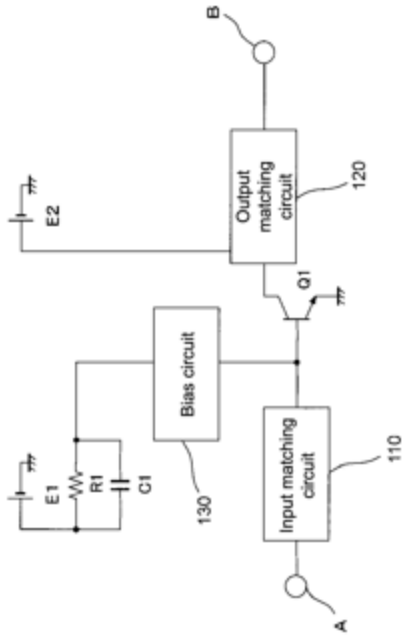
[FIG. 5A]



Akagi, Fig. 5A.

In the high-frequency power amplifier, the bipolar transistor Q1, due to the thermal response of itself, when the DC power source E1 is turned on by pulse operation, the power amplification factor changes immediately after the power source is on compared to after time elapses while the on-state is maintained; the power amplification factor increases after a fixed time has elapsed than immediately after the power source is turned on, and falls into a fixed value (for example, see non-patent document 1).

Akagi, ¶ 5, Fig. 1.



Akagi, Fig. 4.

Thus, in the conventional high-frequency power amplifier, as illustrated in FIG. 4, a method wherein a circuit in which the resistor R1 and the capacitor C1 as an example of a capacitance element are connected in parallel is inserted in series between the DC power source E1 and the bias circuit 130 is generally used. In this case, immediately after the DC power source E1 is turned on, an instantaneous current flows into the bias circuit 130 via the capacitance C1, and the same voltage as the DC voltage of the DC power source E1 is applied to the bias circuit 130. The voltage value applied to the bias circuit 130 gradually decreases according to a time constant determined by the resistor R1 and the capacitor C1, and finally reaches a value corresponding to a voltage drop caused by the current flowing through the resistor R1. Thus, for the amplifier, the DC voltage of the DC power source E1 is applied immediately after the power source is turned on, the bias point is set to be high, and the power amplification factor becomes high, but, as time advances, current flows through the resistor R1, causing a voltage drop, and the amplifier operates at a low bias point and the power amplification factor becomes small by the amount of voltage drop. Thus, the power amplification factor correction is performed based on the thermal response.

Akagi, ¶ 7, Fig. 4.

## B. The Group 1 Patents Use a Current Mirror, But Current Mirrors Were Well Known in the Prior Art

As evidenced by the following references, current mirrors were pervasively used building blocks of circuits in the prior art pertinent to the Group 1 Patents.

### 1. Pervasively Used

In the prior art, current mirrors were well established in the general knowledge in the art, widely used and understood, as evidenced by their extensive description in the literature, including textbooks. *See, e.g., Gilbert* in Toumazou, *Analog IC Design - The Current-Mode Approach - Ch 6* (2008) pp. 239-296 (chapter 6 dedicated to bipolar current mirrors, and beginning “**Few readers of this book will need to be introduced to the concept of the current mirror; it has become a familiar icon of modern analog design.**”); *Gray*, *Analysis and Design of Analog Integrated Circuits* (5<sup>th</sup> Ed 2009) (“*Gray*”) Ch. 4 (current mirrors), *id.* p. 251 (“**Current mirrors** made by using active devices **have come to be widely used in analog integrated circuits** both as biasing elements and as load devices for amplifier stages.”). *Harrison*, *Current Sources & Voltage References* (2005), p. 70 (“**[V]irtually all BJT current sources are configured as current mirrors** (aka current reflectors), where an input current is mirrored at the output, in either a matched 1:1 or other **ratio.**” *Harrison*, p. 70.

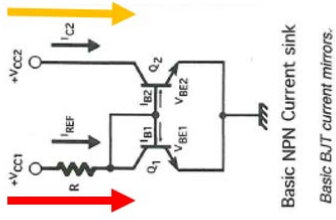
### 2. Well Known, Predictable Building Blocks of Analog IC Circuit Design

As was well-known in the art, a current mirror was a useful building block used to accurately copy or reflect, *i.e.*, to mirror, a current from one branch of a circuit to another. For example:

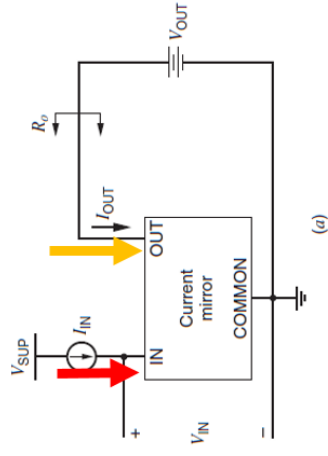
[T]he reference current in one branch of the circuit is **accurately reproduced or reflected** in a second branch, **relatively independent of the absolute values of the device parameters**. Because of this property, these subcircuits are also known as *current mirror* circuits. Such circuit configurations are **particularly useful building blocks** for analog circuit design, since they provide a means of establishing the dc bias levels within the circuit, within the accuracy of the matching or tracking properties of the monolithic components.

*Grebene*, *Bipolar and MOS Analog Integrated Circuit Design* (2003) p. 170.

Current mirrors were generally known to be useful in coupling circuits together by starting with an **input current acting as a source or control current** from a first branch of a circuit, the first branch pushing current into the mirror, and mirroring that over to a corresponding **output current acting as a current sink**, the mirror pulling that current from the second branch of the circuit. For example:

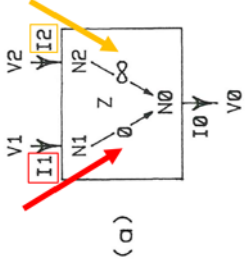


Harrison, p. 71, Fig. 4.18



Gray, Analysis and Design of Analog Integrated Circuits (5<sup>th</sup> Ed 2009) p. 252, Fig. 4.1(a) (annotated)

Likewise, *Gilbert* described the current mirror having similar input and output currents:

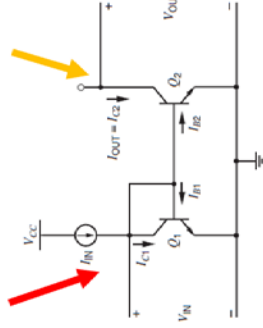


Gilbert in Toumazou, Analogue IC Design - The Current-Mode Approach (2008), p. 240, Fig. 6.1a (annotated).

The simplest current mirror is a three-terminal device, Figure 6.1 a, having an input node, N1, capable of accepting a current,  $I_1$ , of only one polarity, an output node, N2, into which a replication,  $I_2$ , of the input current flows in the same direction, and a common node, N0, in which the sum of the input and output currents flow.

Gilbert in Toumazou, Analogue IC Design - The Current-Mode Approach (2008), p. 239, Fig. 6.1a.

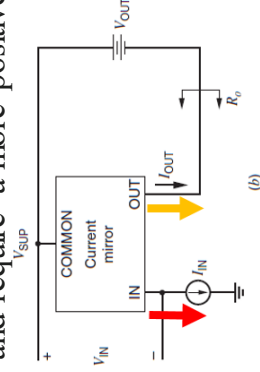
A “simple bipolar current mirror” is shown by Gray, with the controlling input current and mirrored output current:



Gray, p. 253, Fig. 4.2 (annotated).

Such current mirrors were well known, and categorized as “positive” current mirrors, each pulling current into the mirror, called a current sink. Gilbert in Toumazou, Analogue IC Design - The Current-Mode Approach (2008), p. 330 (“Current mirrors are firstly categorised as positive or negative. Positive current mirrors have an output in the form of a current sink.... Thus they require a power supply which is at a relatively negative potential”).

“Negative” current mirrors were also well known. The outputs of these currents were configured as a **current source**. Gilbert in Toumazou, Analogue IC Design - The Current-Mode Approach (2008), p. 330 (“Negative current mirrors have a current source output ... and require a more positive power supply.”). Gray illustrates such current mirrors as follows:



Gray, p. 252, Fig. 4.1(b) (annotated); see also Bellantoni, Morisawa.

Thus, it was also generally known in the art that one could beneficially use current mirrors having a reference current flowing out of the current mirror at its input (e.g. pulled out of the mirror by a first part of the circuit), with the current mirror then providing the mirrored current at its output as a current source, with current flowing to the next part of the circuit.

### 3. Current Mirror Gain

Furthermore, it was well known to use current mirrors to provide a desired *current amplification* when mirroring the current:

A current mirror is an element with at least three terminals, as shown in Fig. 4.1. The common terminal is connected to a power supply, and the input current source is connected to the input terminal. **Ideally, the output current is equal to the input current multiplied by a desired current gain.** If the gain is unity, the input current is reflected to the output, leading to the name *current mirror*.

Gray, p. 251. Likewise, Harrison, Current Sources & Voltage References (2005) described the wide application of current sources formed using current mirrors: “As a result, **virtually all BJT current sources are configured as current mirrors** (aka current reflectors), where an input current is mirrored at the output, **in either a matched 1:1 or other ratio. This may be either a fraction or a multiple of the input, or scaled in some other manner.**” Harrison, p. 70.

Thus, a current mirror could increase the gain of current (*amplify current*) in at least two ways:

First, it was general knowledge in the prior art that current mirrors were useful to achieve a desired current amplification by simply setting the emitter areas (sizes) of the mirror's transistors to the desired gain. For example, *Gray* described “Since the saturation current of a bipolar transistor is proportional to its emitter area, the first term in (4.6) shows that **the gain of the current mirror can be larger or smaller than unity because the emitter areas can be ratioed.**”

$$I_{OUT} = \frac{I_{S2}}{I_{S1}} I_{C1} = \left( \frac{I_{S2}}{I_{S1}} I_{IN} \right) \left( \frac{1}{1 + \frac{(I_{S2}/I_{S1})}{\beta_F}} \right) \quad (4.6)$$

*Gray*, p. 25 (eq. 4.6) (referencing collector currents  $I_C$  shown in the mirror of Fig. 4.2, and saturation currents  $I_S$ , that are proportional to emitter area).

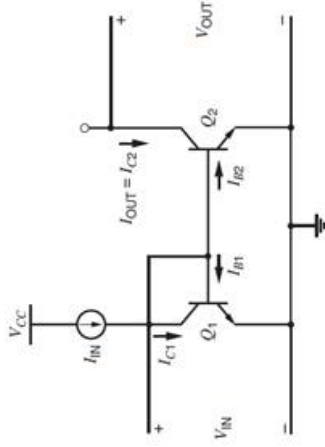


Figure 4.2 A simple bipolar current mirror.

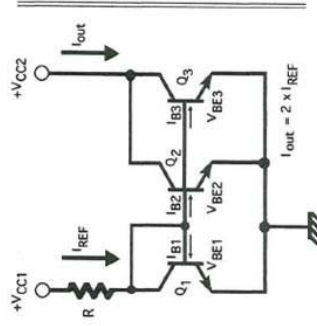
*Gray*, Fig. 4.2 (showing basic current mirror with collector currents  $I_C$  referenced in Equation 4.6)

Similarly, *Gray* describes setting the area ratio for MOS current mirrors to establish gain. *Gray*, p. 254 (discussing, for MOS transistors, “[t]o ratio the transistor sizes, either the widths or the lengths can be made unequal in principle. ... [T]he widths are ratioed rather than the lengths in most practical cases.” *Gray*, p. 257. Likewise, *Grebene* described: “[T]he basic current mirror ... provides a means of obtaining a current reference level, independent of implicit device parameters, which can be ‘scaled’ by proper choice of the emitter areas of the two transistors.” *Grebene*, Bipolar and MOS Analog Integrated Circuit Design (2003) p. 172; see also *Gilbert* in Toumazou, Analogue IC Design - The Current-Mode Approach (2008), p. 252 (“the ratio of the collector currents must be identical to the emitter area ratio, A.”). *Gilbert* explains that “[t]here is no particular difficulty in achieving high mirror ratios. In many cases, simple emitter area ratios will suffice, supported by current gain if necessary (as in the EFA mirror, which is not

limited to the use of a single transistor for current boosting). **In practical monolithic designs, emitter area ratios of up to 100:1 are not hard to achieve [.]” Gilbert** at 280.

Second, it was general knowledge in the prior art that current mirrors were also useful to achieve integer levels of amplification by simply ratioing the number of transistor units on one side of the mirror to those on the other in the desired amplification ratio. For example, Gray taught that **“If the desired current-mirror gain is a rational number, M/N, the area ratio is usually set by connecting M identical devices called units in parallel to form Q2 and N units in parallel to form Q1 ...” Gray**, p. 254. One motivation to use this method was to “minimize mismatch arising from lithographic effects in forming the emitter regions.” *Id.* The same is true for MOS-based current mirrors. *Gray*, p. 257 (“If the desired current-mirror gain is a rational number, M/N, the ratio is usually set by connecting M identical devices called *units* in parallel to form M<sub>2</sub> and N units in parallel to form M<sub>1</sub> to minimize mismatch arising from lithographic effects in forming the gate regions.”).

*Harrison* likewise observes “...it is often necessary to generate integer multiples or fractions on an initial current. For the IC designer this is **accomplished in the design by creating transistors with multiple emitters, or with bulk emitter area ratioed in either greater or lesser amounts.** In this way a current can be made, say, 10 times or one-tenth of the initial input current[.]” *Harrison*, p. 95 (emphasis added). *Harrison*, p. 95, states “For the board-level designer, generating multiples or fractions of an initial current can be accomplished in different ways. One way to do this is by paralleling individual transistors as shown in the following circuits, in what is known as current scaling.” *Harrison* shows the following current scaling mirror with  $I_{OUT} = 2 I_{CI}$ .



Simple NPN Current sink  
(x2) Multiplier

Figure 4.34. Examples of current multipliers.

$$I_{OUT} = 2 \left( \frac{\beta}{\beta + 2} \right) \left( \frac{V_{CC1} - V_{BE1}}{R} \right) \quad (\text{Eq. 4.84})$$

$$\therefore I_{C3} \approx 2 I_{C1} \quad (\text{Eq. 4.85})$$

*Harrison*, p. 97, Fig. 4.34, Equations 4.84 and 4.85.

In fact, using current mirrors to provide amplification is a common feature of RF power amplifiers. *See, e.g.*, U.S. Patent Publication No. 2005/0140457 to *Bellantoni* at ¶ 69. (“A modulation bias current through each of the power transistor cells  $Q_{n1}$  . . .  $Q_{ni}$  thus results and is equal to the reference current multiplied by the ratio of the width of the power transistor cell to that of the reference transistor  $Q_{ref}$ , independent of variations in transistor characteristics or operating temperature or other environmental conditions.”)

#### 4. Additional Benefits and Properties Were Well-Known

Additional benefits and properties of current mirrors were well known and formed part of the general knowledge in the art. For example:

**Current mirrors find endless uses not only in biasing applications of low to moderate accuracy, where their high output impedance makes them valuable as good approximations to ideal current sources. More complex mirrors provide special capabilities, such as high accuracy over many decades of current, exceptionally high output resistance, very low or high transfer ratios, and so on.**

*Gilbert* in Toumazou, Analogue IC Design - The Current-Mode Approach (2008), p. 239.

“The use of **current mirrors** in biasing **can result in superior insensitivity of circuit performance to variations in power supply and temperature.**” Gray, p. 251. “Current mirrors are **frequently more economical than resistors** in terms of the die area required to provide bias current of a certain value, particularly when the required value of bias current is small.” *Gray*, p. 251. “When used as a load element in transistor amplifiers, the high incremental resistance of the current mirror results in high voltage gain at low power supply voltages.” *Gray*, p. 251.

C. The Group 1 Patent’s Disclosure of a Single Integrated Circuit, Mounted on a Single Package Substrate to form a Single Package Module Was Well-Known to a POSITA in the Prior Art, Including the ’563 Patent’s Claimed Integration of a Power Amplifier and Biasing Circuitry in a Single Integrated Circuit<sup>5</sup>

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<sup>5</sup> This section is not directly relevant to prior art invalidity of the ’101 Patent. Respondents are including it here for ease of reference to consolidate the State of the Art discussion for the Group 1 Patents in a main location in these contentions.

As shown by the following references, integrating a power amplifier and biasing circuitry onto a single integrated circuit, single package substrate, and/or single package module was well known to a POSITA before the purported invention of the Group 1 Patents.

#### 1. Single Integrated Circuit

In the prior art, a POSITA understood that power amplifiers and bias circuits could be advantageously implemented on the same integrated circuit.

U.S. Patent Publication No. 2011/0025422 to *Marra et al.* at ¶¶ 65-68 (describing “an integrated circuit” including “an amplifier and a bias circuit”).

U.S. Patent No. 6,831,517 to *Hedberg et al.* at 2:37-43 (“another advantage of the present invention that a bias-management system is provided in which a reference transistor of a bias regulator and an output transistor of a power amplifier are fabricated upon a common integrated-circuit substrate to provide close thermal coupling between the bias regulator and the power amplifier”). *Hedberg* teaches that the advantages of being on a common die include “correlated process-dependent characteristics such as  $V_{be}$  match, which ensures the current ratio in these transistors are determined by size ratio and not process characteristic differences.” *Hedberg* at 5:5-15.

*Johnson*, Silicon-Germanium BiCMOS HBT Technology for Wireless Power Amplifier Applications, IEEE Journal of Solid-State Circuits, vol. 39, No. 10, (Oct. 2004). *Johnson* described numerous advantages of placing a PA and bias circuit on an integrated circuit attached to a package substrate in a packaged module. *Johnson*, Fig. 12 (showing PA and bias circuit on BiCMOS die); Fig. 17 (showing photo of die containing modulator, power amplifiers, biasing circuits, switch, and associated circuitry); p. 1612 (teaching BiCMOS flip-chip IC on LTCC having “low thermal resistance”, “low parasitic inductance”, “good thermal conductivity”, and a “small footprint”, a “very strong path for PA modules”, with “superior performance and stability” with “low component count”). *See, e.g., Illingworth* defines BiCMOS as “[i]ntegrated circuits that contain both bipolar junction transistors and complementary MOS transistors (CMOS). The combination of both types of device on the same chip has a wide variety of functions and allows the advantages of both processes to be exploited.” *Illingworth*, p. 38-39. “BiCMOS circuits provide improved system performance and a reduction in the number of components, hence reduced chip sizes and lower costs.” *Illingworth*, p. 39.

U.S. Patent No. 7,304,539 to *Tsurumaki et al.* at 1:25-44 (“A high frequency power amplifier circuit (having multi-stage composition usually) that uses a semiconductor amplifying device, such as a MOSFET (insulated gate field-effect transistor) or a GaAs-MESFET is incorporated in the transmitting-side output unit of a radio communication system (mobile communication system), such as a cellular phone. This high frequency power amplifier circuit is, usually, constructed in most cases as a single electronic component. In the electronic component, a semiconductor chip including an amplifying transistor and its bias circuit is mounted on an insulating substrate, such as a ceramic substrate in which printed wiring applies on the surface or in the inside, together with a discrete

component such as another semiconductor chip or a capacitor, and each component is coupled by the printed wiring or a bonding wire. This electronic component is called an RF power module. Incidentally, in the case of a semiconductor chip used in an RF power module for a cellular phone, high integration is advancing to enable the high performance and miniaturization of the module.”)

U.S. Patent Publication No. 2011/0128078 to *Doherty* et al. at ¶¶ 58-60 (describing an invention “in the context of an integrated chip (IC) power amplifier” that included a power amplifier and “biasing circuitry”), ¶ 89 (illustrating that implementing power amplifiers on a single package was well known and stating “variations in timing and amplitudes are also capable of compensating for gain and phase of the IC when placed into semiconductor packages with differing thermal time constants, e.g. different settings may be needed on the same IC when used in different packages”).

U.S. Patent Publication No. 2004/0232982 to *Ichitsubo* et al. at ¶25 (describing a radio frequency power amplifier (PA) module in which the “Power Amplifiers 24, the Power Sensor 26, the Bias Circuit 22, can be fabricated in an integrated circuit on a semiconductor chip.”).

Dictionary definitions likewise demonstrate generally held, common knowledge regarding “integrated circuits” in the prior art. *See also Laplante*, *Comprehensive Dictionary of Electrical Engineering* (2<sup>nd</sup> Ed. 2005) p. 443 (defining “MMIC” or “Monolithic Microwave Integrated Circuit” as “integrated circuits made of gallium arsenide (GaAs), silicon, or other semiconducting materials where all of the components needed to make a circuit (resistors, inductors, capacitors, transistors, diodes, transmission lines) are formed onto a single wafer of material using a series of process steps”), p. 351 (defining “integrated circuit” as “many transistors, resistors, capacitors, etc., fabricated and connected together to make a circuit on one monolithic slab of semiconductor material”); *Reddy*, *Encyclopedia of Electronics and Telecommunication Engineer* (2007), p. 169 (“Integrated Circuit (IC) A device in which components such as resistors, capacitors, and transistors are formed on the surface of a single piece of semiconductor.”)

*See* ECP052 data sheet, providing parameters and specifications that one would expect of a “package module”, including beneficial protective and functional aspects of a integrated circuit housing, including electrical and mechanical connections between the integrated circuit and the remaining electrical components, thermal properties, electrostatic discharge (ESD) protections, physical protections of a housing, and a surface to provide identification markings. *See* WJ Communications Data Sheet ECP052 (August 2004), p. 5, available at: <https://web.archive.org/web/20041105150302/http://www.wj.com/pdf/ECP052.pdf>

## 2. Package Substrate and Packaged Module

In the prior art, a POSITA understood that an integrated circuit containing a power amplifier was commonly and advantageously mounted on a package substrate.

*Johnson*, Silicon-Germanium BiCMOS HBT Technology for Wireless Power Amplifier Applications, IEEE Journal of Solid-State Circuits, vol. 39, No. 10, (Oct. 2004). *Johnson* described numerous advantages of placing a PA and bias circuit on an integrated circuit attached to a package substrate in a packaged module. *Johnson*, Fig. 12 (showing PA and bias circuit on BiCMOS die); Fig. 17 (showing photo of die containing modulator, power amplifiers, biasing circuits, switch, and associated circuitry); p. 1612 (teaching BiCMOS flip-chip IC on LTCC having “low thermal resistance”, “low parasitic inductance”, “good thermal conductivity”, and a “small footprint”, a “very strong path for PA modules”, with “superior performance and stability” with “low component count”).

U.S. Patent Publication No. 2004/0232982 to *Ichitsubo* et al. at ¶25 (describing a radio frequency power amplifier (PA) module “built on a module substrate [that] ... includes metal pins adapted to receiving connecting terminals of integrated circuits including the Power Amplifiers 24, the Bias Circuit 22, the Power Sensor 26, and optionally Control Logic 28.”).

In the prior art, a POSITA knew that integrated circuits were implemented in packaged modules, as part of the general knowledge in the art. See, e.g., *Laplante*, Comprehensive Dictionary of Electrical Engineering (2<sup>nd</sup> Ed. 2005) p. 495 (defining “package” as “in MMIC technology, die or chips have to ultimately be packaged to be useful. An example of a package is the T07 ‘can.’ The MMIC chip is connected within the can with bond wires connecting from pads on the chip to lead pins on the package. The package protects the chip from the environment and allows easy connection of the chip with other components needed to assemble an entire system, such as a DBS TV receiver.”), p. 443 (defining “MMIC” or “Monolithic Microwave Integrated Circuit” as “integrated circuits made of gallium arsenide (GaAs), silicon, or other semiconducting materials where all of the components needed to make a circuit (resistors, inductors, capacitors, transistors, diodes, transmission lines) are formed onto a single wafer of material using a series of process steps”); U.S. Patent Publication No. 2004/0232982 to *Ichitsubo* et al. at ¶25.

*Reddy*, Encyclopedia of Electronics and Telecommunication Engineer (2007), p. 215. (“Multichip Module **A module** capable of supporting several ICs in a **single package**. **Typically, multichip modules are based on ceramic**, contain high performance ICs with high pin count, and use some form of advanced interconnect technology such as TAB, COB, or CR.”). The ceramic or other material is a *package substrate*.

*Murase*, Multi-chip Transmitter/Receiver Module Using High Dielectric Substrates for 5.8 Ghz ITS Applications, 1999 MTT-S Digest. *Murase* proposes “small and integrated microwave multi-chip modules (MCMs)” (packaged module) using “high dielectric substrates” (*package substrates*). *Murase*, p. 211. *Murase* describes a “microstrip filter chip” and two “GaAs IC chips”, all on a “low-cost alumina substrate” (*package substrate*). *Id.*, see also p. 212 (Table 1 and “Three chips were die-bonded on a package substrate and wire-bonded each other or to the package. The **package substrate** has simple and low-cost structure, which consists of two alumina layers and three metal layers.”) *Murase* describes multiple benefits to MCMs, including: “using high dielectric constant substrates” (*package substrate*) provide “great advantage to miniaturization of modules” and “integration of functional passive devices for the new microwave wireless systems.” *Id.* 214. “low cost alumina substrate” *Id.* 211. Small “package external size” while including a “band pass filter and a switch.” *Id.*

See ECP052 data sheet, providing parameters and specifications that one would expect of a “package module”, including beneficial protective and functional aspects of an integrated circuit housing, including electrical and mechanical connections between the integrated circuit and the remaining electrical components, thermal properties, electrostatic discharge (ESD) protections, physical protections of a housing, and a surface to provide identification markings. See WJ Communications Data Sheet ECP052 (August 2004), p. 5, available at: <https://web.archive.org/web/20041105150302/http://www.wj.com/pdf/ECP052.pdf>.

*DieIs* describes advantages of a “system-in-a-package (SiP)”, even for demanding environment of 5 GHz WLAN, reporting “a fully integrated single-package RF prototype module for a 5 GHz WLAN receiver front-end”, “implemented with a thin film multichip module (MCM-D) interconnect technology”, that “would make use of a silicon IC technology (CMOS or BiCMOS).” *DieIs* p. 384 (Abstract).

*DieIs* discloses package substrates in a package module, with various dies mounted thereto:

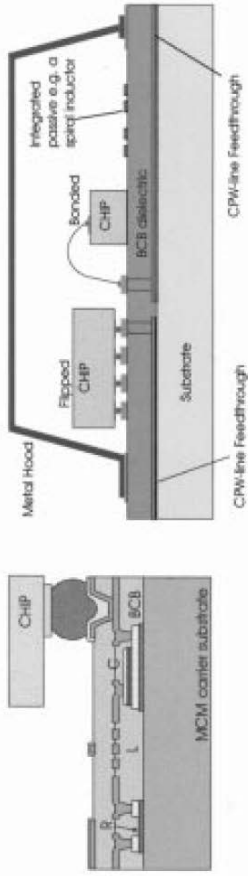


Fig. 2. Cross section of an MCM substrate with integrated passives and an indicative drawing of some supported mounting possibilities.

*DieIs*, Fig. 2, p. 386.

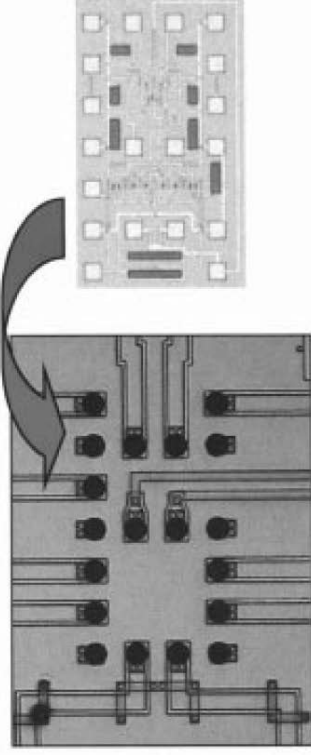


Fig. 3. Principle of flip-chip mounting. Left: detail of the MCM-D module with bumped pads, Right: clip, which is to be mounted upside-down on this module.

*DieIs*, Fig. 3, p. 38.

*DieIs* teaches the following advantages for MCMs:

- “High quality components can be integrated in the package” p. 384.
  - “The active components are commercially available, “bare die” components, which are flip-chip mounted onto the MCM substrate.” *Id.*
  - A “glass substrate” (*package substrate*) can be used that has the benefit of “circumvent[ing] substrate coupling” because it “is almost a perfect insulator.” p. 385.
  - “In addition, one does not have to stick to one IC-technology. Every component can be integrated in the best-fitted technology: e.g, CMOS for digital and BiCMOS for the low-frequency analog and the RF, except for the power amplifier. For the latter block, GaAs is probably required. This also leads to much more design freedom.” p. 386.
- D. The Group 1 Patents Reference the Use of a Heterojunction Bipolar Transistor (HBT) for its Power Amplifier, But the Use of HBTs for PAs Was Well-Known in the Art

By May 2011, it was well known to implement PAs using bipolar junction transistors (BJT). See *Johnson* 1605 (explaining that “bipolar transistors have evolved as the preferred choice” for wireless PAs due to “higher gain and current density at the frequencies employed”). Furthermore, it was well-known, general knowledge in the art that a high performing type of BJT for RF PAs

was a BJT with a wide band gap emitter, known as a Heterojunction Bipolar Transistor (HBT). *See, e.g., Illingworth*, at 259 (defining HBT, including, e.g., “A bipolar junction transistor that incorporates a wide band gap emitter” with the result of reduced base resistance, “maximizing the desired injection of carriers from emitter to base.... HBTs are used at radio- and microwave frequencies, in integrated circuit and power applications”). HBTs were known to be specifically adapted for high performance to meet the demands of RF power amplification applications. *See, e.g., id.* (describing that the HBT properties “leads to an improvement in the high-frequency performance of the transistor. HBTs are used at radio- and microwave frequencies, in integrated circuit and power applications, and in optoelectronic ICs.”). In fact, HBTs were the dominant, market leading form for RF PAs implemented with BJTs, with well-documented advantages known to a POSITA. *TriQuint*, at 1 (“RF medium and high power amplifiers realized with HBT technology are increasingly popular in telecommunications systems due to the inherently superior linearity and efficiency performance compared to competing technologies. The reliability of HBT RF devices is well known to be excellent from Highly Accelerated Stress Testing (HAST) and High Temperature Operating Lifetime (HTOL) testing.”); *Johnson* at 1605 (explaining advantages including “provid[ing] high integration and [] reduce[d] cost,” reduced chip area and increased chip robustness, temperature insensitive current gain, and well characterized reliability at high current densities enabling further reduction in device size).

It was known that HBTs came in a variety of advantageous forms, including Gallium Arsenide (GaAs) and Silicon Germanium (SiGe). *Illingworth*, at 259. For example, SiGe HBTs found “increasing use in wireless PA applications” due to “favorable thermal properties,” “volume manufacturing capability,” and “design automation support,” which had all “long been recognized.” *Johnson*, at 1612. Such HBTs had “favorable device ruggedness for PA applications.” *Id.* HBT PA designs had been demonstrated to meet the needs of a range of wireless standards, including the robustness required at the high speed, output power and linearity called for by the GSM, GPRS, and EDGE wireless standards. *Id.* It was known that the “favorable thermal properties, lower cost of wafer processing and the higher integration capabilities” of such HBTs “make them a compelling choice for wireless applications” and provide a “very strong path for PA modules.” *Id.*

Thus, the use of BJT transistors to form a PA, including the HBT form of BJTs and their advantages, formed part of the general knowledge in the art before the invention.

### III. Claim Chart

Claim chart begins on the following page.

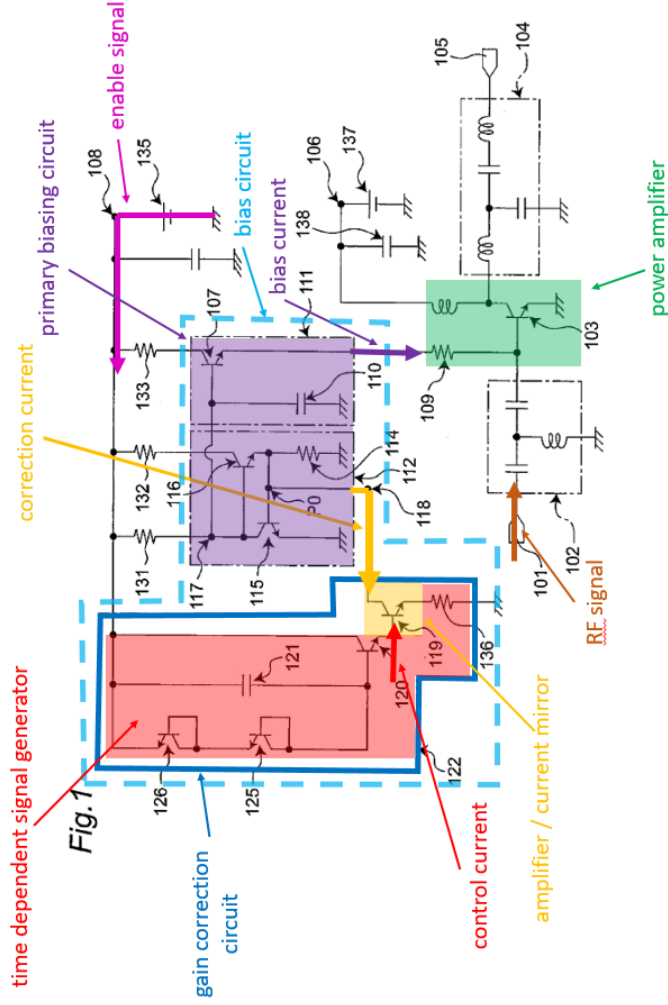
**Claim Language**

[1pre] 1. A power amplifier system comprising:

**Ishimaru Alone and/or in Combination with Other References**

To the extent the preamble is limiting, *Ishimaru* discloses a *power amplifier system* for “a high frequency power amplifier to be used in radio communication devices.” See, e.g.:

*Ishimaru* discloses the circuitry for the *power amplifier system* includes “an amplification section having a first transistor for performing power amplification,” as well as “a bias power source section,” “bias circuit,” and “a speedup circuit.” *Ishimaru* at Abstract, ¶¶10-12, Fig. 1 (annotated below):



*Ishimaru*, Fig. 1 (annotated).

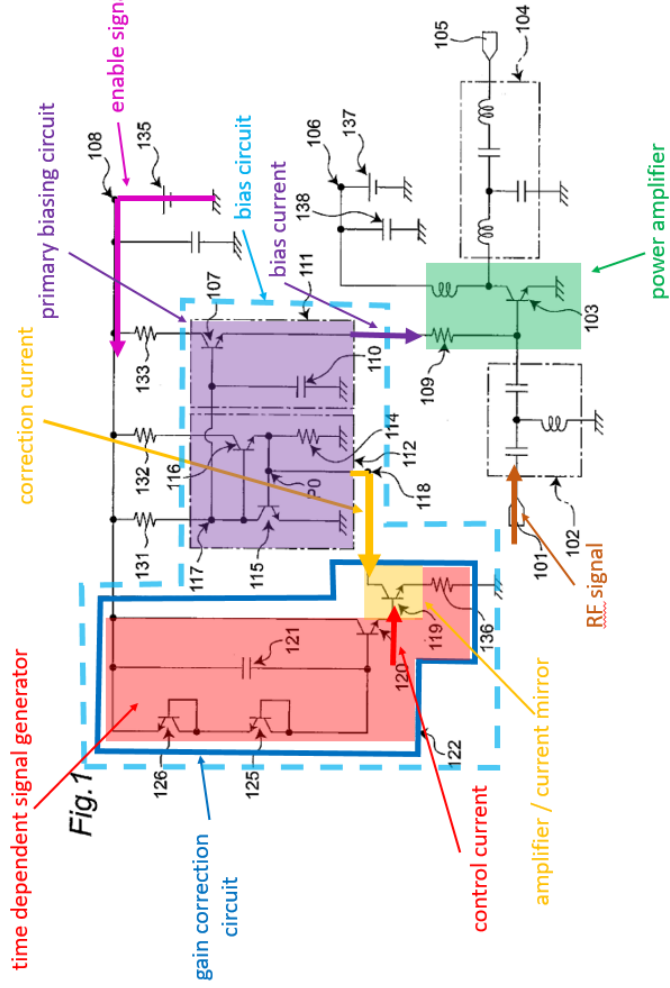
**Claim Language**

[1a] a power amplifier configured to amplify a radio frequency (RF) signal; and

**Ishimaru Alone and/or in Combination with Other References**

*Ishimaru* discloses a power amplifier configured to amplify a radio frequency (RF) signal in radio communications devices. See, e.g.:

*Ishimaru* discloses “a high-frequency power amplifier to be used in radio communication devices.” *Ishimaru* ¶1. The circuitry for the PA includes “an amplification section having a first transistor for performing power amplification” (green) (a power amplifier). *Ishimaru* ¶¶10-12. As illustrated in Figure 1 (annotated below), *Ishimaru* further discloses that “a high-frequency signal as an input signal [is] inputted from an input signal terminal 101, ... is amplified by an amplifier transistor 103 serving as a first transistor, and then, ... outputted from an output signal terminal 105” (power amplifier configured to amplify). *Ishimaru* ¶42.



**Claim Language**

**Ishimaru Alone and/or in Combination with Other References**

*Ishimaru*, Fig. 1 (annotated).

Because *Ishimaru* is directed to a PA for a **radio** communications device, a POSITA reading *Ishimaru* understood that the high-frequency input signal at input terminal 101 is a *radio frequency (RF) signal* (brown arrow) for amplification by amplifier transistor 103 (*a power amplifier configured to provide amplification*) to generate an amplified radio frequency signal at output terminal 105

*Ishimaru* discloses:

“The present invention relates to **power amplifiers** and, for example, to a **high-frequency power amplifier** to be **used in radio communication** devices or the like.” *Ishimaru* at ¶ 1.

“FIG. 1 is a circuit diagram showing a circuit construction in an embodiment of the power amplifier of the invention.

In this power amplifier, a **high-frequency signal** as an input signal inputted from an input signal terminal 101, passing through an input matching circuit 102, is **amplified by an amplifier transistor 103** serving as a first transistor, and then, after passing through an output matching circuit 104, outputted from an output signal terminal 105. In FIG. 1, reference sign 106 denotes a collector bias terminal of the amplifier transistor 103. Between the collector bias terminal 106 and the ground are connected a DC power source 137 and a capacitance element 138. The amplifier transistor 103 forms an amplification section.” *Ishimaru* at ¶¶ 41-42.

“Technical Problem

Accordingly, an object of the present invention is to provide a power amplifier which is capable of suppressing distortion increases of an amplification signal due to heat generation upon start-up without using any temperature sensing element.”

**Claim Language**

***Ishimaru* Alone and/or in Combination with Other References**

*Ishimaru* at ¶¶ 6-7.

“Solution to Problem

In order to achieve the above object, there is provided a power amplifier comprising: an amplification section having a first transistor for performing power amplification; a bias power source section having a second transistor for feeding a bias to the first transistor; and a speedup circuit for transiently increasing the bias fed to the first transistor by bias power source section at a start of the power amplification.”

*Ishimaru* at ¶¶ 8-12.

“In the power amplifier of the invention, at a start of power amplification by an amplifier transistor **103** serving as an amplification section, a speedup circuit **122** transiently increases a bias which is fed to the amplifier transistor **103** via a bias power source section composed of a bias circuit **111** and a power source circuit **112**. As a result, the power amplification factor of the amplifier transistor **103** is transiently increased at the start of power amplification by the amplifier transistor **103**. Thus, the time elapsing until temperature variations due to heat generation of the amplifier transistor **103** come to an equilibrium on the whole circuit is shortened, with a result of reduced distortion of the amplification signal such as a modulated-wave signal. Accordingly, in the invention, it becomes possible to suppress distortion increases of an amplification signal due to heat generation at the start time without using any temperature sensing element.” *Ishimaru*, Abstract; *see also* ¶¶ 7, 13, Fig. 1.

“Next, FIG. 3 shows an example (simulation result) of transient response of the operating current (collector current Ic3) of the amplifier transistor 103 in the power amplifier of this embodiment. In this embodiment, the current to be fed from the bias transistor 107 to the amplifier transistor 103 is forcedly increased at turn-on of the amplifier, with the result that the value of the operating current Ic3 comes to a steady state in about 4 the time of transient response of the comparative example of FIG. 2. Thus, occurrence of distortions of the amplification signal due to temperature variations in the amplifier circuit is

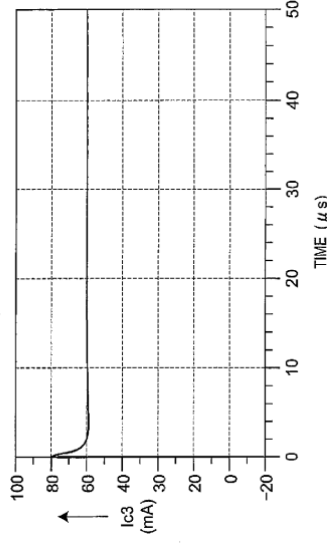
**Claim Language**

**Ishimaru Alone and/or in Combination with Other References**

suppressed, so that the linearity of the circuit in burst operation is improved. That is, gain variations due to collector current variations of the power amplifier using a bipolar transistor can be compensated.” *Ishimaru* at ¶ 54, Fig. 1, Fig. 2, Fig. 3.

“In the power amplifier of this embodiment also, the capacitance value of the capacitance element 121 of the speedup circuit 122 is adjusted so as to cancel transient variations in gain due to the temperature variations at a start of power amplification. As a result of this, deterioration of the linearity due to variations of amplification gain can be canceled so that the value of dynamic EVM (error vector magnitude) can be improved.” *Ishimaru* at ¶ 55, Fig. 1.

Fig.3

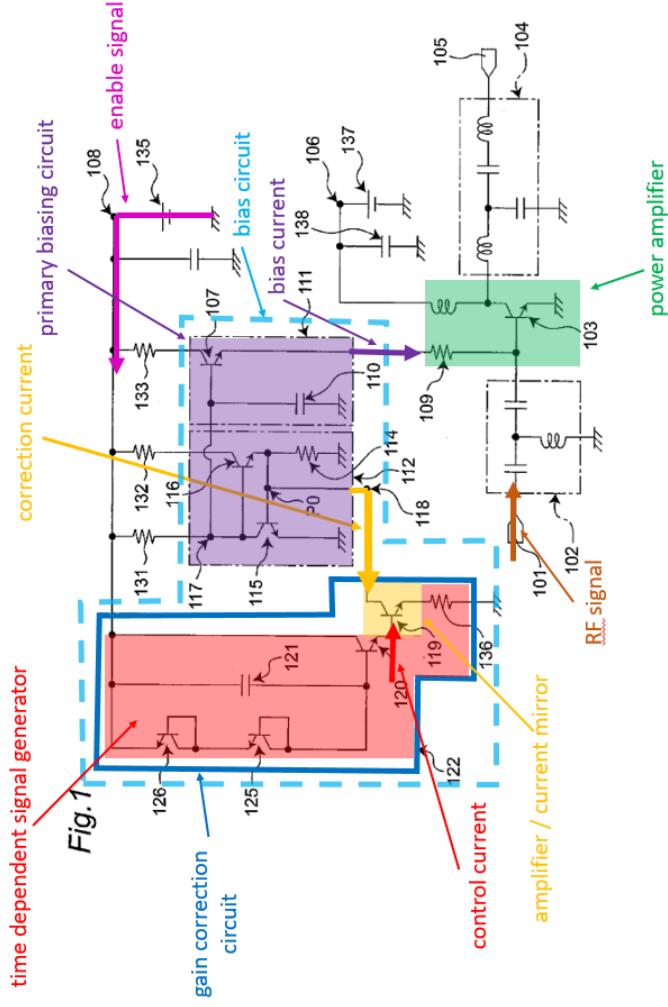


*Ishimaru*, Fig. 3.

[1b] a bias block for biasing the power amplifier, the bias block including

*Ishimaru* discloses a bias block for biasing the power amplifier. See, e.g.:

*Ishimaru* discloses “speedup circuit 122”, “power source circuit 112”, and “bias circuit 111” (collectively a bias block) (light blue) that receives a control voltage from voltage source 135 (enable signal) (pink arrow) and “supplies a base bias current” (purple arrow) to a “base terminal” of “amplifier transistor 103” (biasing the power amplifier) (green). *Ishimaru* Abstract, ¶¶ 24, 31, 43, 45, 49-52.



Ishimaru, Fig. 1 (annotated).

Ishimaru discloses:

“Also, a bias transistor 107 as a second transistor is a transistor that supplies a base bias current to a base terminal of the amplifier transistor 103. An emitter of the bias transistor 107 is connected to a base terminal of the amplifier transistor 103 via a resistance element 109. The resistance element 109 is a ballast (stabilization) resistor which is inserted in a base bias channel to prevent thermal runaway of the amplifier transistor 103.”

Ishimaru at ¶ 43.

**Claim Language**

***Ishimaru* Alone and/or in Combination with Other References**

“The bias transistor 107 has its collector connected to a bias terminal 108 via a resistance element 133. The bias terminal 108 is connected to a control voltage source 135.

A bias circuit 111 composed of the bias transistor 107 and a capacitance element 110 connected to a base terminal of the bias transistor 107 has a function of increasing the base bias current in response to an increase in signal strength of the input signal, and functions to keep the amplification ratio of an output signal as well as its phase rotation after amplification constant even when the signal strength of the input signal has changed.”

*Ishimaru* at ¶¶ 44-45.

“A power source circuit 112 is connected to the base terminal of the bias transistor 107 of the bias circuit 111. The bias circuit 111 and the power source circuit 112 constitute a bias power source section.

The power source circuit 112 feeds generally a sum of a “base-emitter voltage” of the amplifier transistor 103 and a “base-emitter voltage” of the bias transistor 107 to the base terminal of the bias transistor 107. That is, the power source circuit 112 feeds a voltage double the base-emitter voltage (hereinafter, referred to as VBE) of a transistor used in the power source circuit 112 to the base terminal of the bias transistor 107. It is noted that voltage drops of the ballast resistor 109 are neglected in this case.”

*Ishimaru* at ¶¶ 46-47.

“In this embodiment, as shown in FIG. 1, the power source circuit 112 has a third transistor 115, a fourth transistor 116, and a resistance element 114. The third transistor 115 has its collector connected to the base of the bias transistor 107 and its emitter connected to the ground. Also, a base of the third transistor 115 is connected to an emitter of the fourth transistor 116. The collector of the third transistor 115 is connected to the bias terminal 108 via a resistance element 131. Meanwhile, the fourth transistor 116 has its

**Claim Language**

***Ishimaru* Alone and/or in Combination with Other References**

emitter connected to the ground via the resistance element 114 and its collector connected to the bias terminal 108 via a resistance element 132.”

*Ishimaru* at ¶ 48.

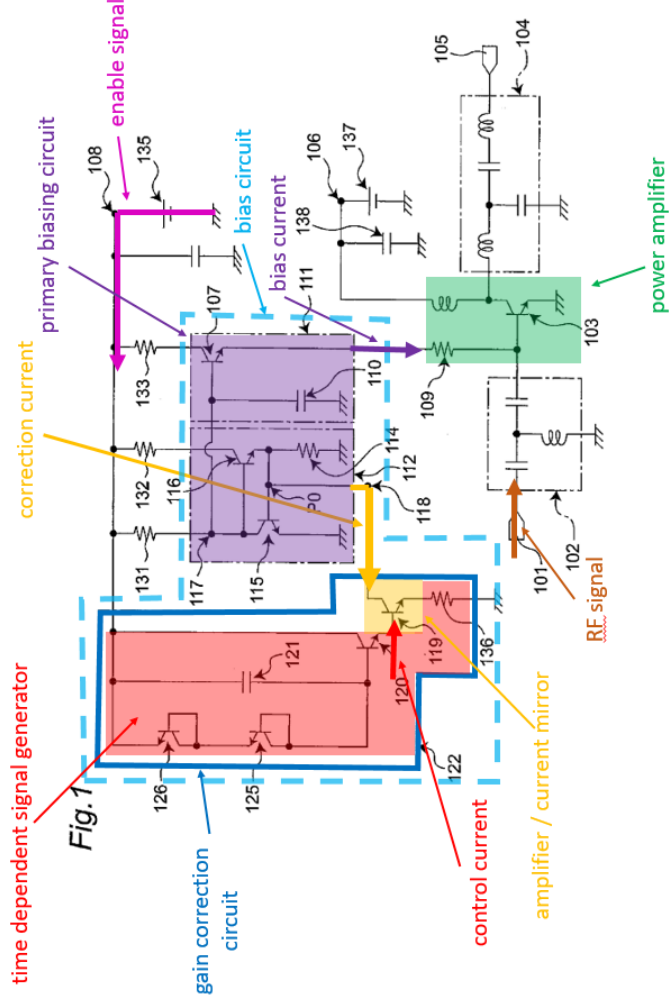
“A connecting point P0 between the base of the third transistor 115 and the emitter of the fourth transistor 116 in the power source circuit 112 is connected to an output terminal 118 of a speedup circuit 122.”

The speedup circuit 122 has a fifth transistor 119 whose collector is connected to the output terminal 118, and a sixth transistor 120 whose emitter is connected to a base of the fifth transistor 119. The emitter of the fifth transistor 119 is connected to the ground via a resistance element 136.

The speedup circuit 122 also has a capacitance element 121 which is connected between a base of the sixth transistor 120 and the bias terminal 108, and two diodes 125, 126 which are connected in series between the base of the sixth transistor 120 and the bias terminal 108.

In the speedup circuit 122, with electric charge flowing into the capacitance element 121 at a rise time of the control voltage of the control voltage source 135 (at turn-on of the amplifier), a current transiently (temporarily) flows from the output terminal 118 into the fifth transistor 119, causing the voltage value of the output terminal 118 to lower. As a result, due to a change of the bias point of the third transistor 115, the voltage of a connecting terminal 117, which connects the collector of the third transistor 115 to the base of the bias transistor 107, transiently increases. Thus, at the rise time, the current fed to the amplifier transistor 103 by the bias transistor 107 transiently increases. Therefore, at the rise time, the power amplification factor of the amplifier transistor 103 transiently increases, so that the time elapsing until temperature variations due to heat generation of the amplifier transistor 103 come to an equilibrium on the whole circuit is shortened, with

Claim Language	Ishimaru Alone and/or in Combination with Other References
<p>[1b.1] a time-dependent signal generator configured to shape an enable signal of the power amplifier to generate a control current,</p>	<p>a result of reduced distortion of the amplification signal (e.g., modulated wave signal).” Ishimaru at ¶¶ 49 - 52.</p> <p>Ishimaru discloses a <i>time-dependent signal generator configured to shape an enable signal of the power amplifier to generate a control current</i>. See, e.g.:</p> <p>Ishimaru discloses that the control voltage from control voltage source 135 at bias terminal 108 “controls turn-on and -off of power amplification.” <i>Ishimaru</i> at ¶24. Thus, as shown in annotated Fig. 1 below, <i>Ishimaru’s</i> control voltage is an <i>enable signal of the power amplifier</i> (pink) as the power amplifier is only operable when the bias is active and the bias is only active when the terminal 108 is high.</p> <p>With reference to annotated Fig. 1 below, <i>Ishimaru</i> discloses a “speedup circuit 122” (dark blue) that includes a capacitance element 121, diodes 125 and 126, transistors 119 and 120, and resistance element 136 (<i>a time-dependent signal generator</i>) (red). <i>Ishimaru</i> ¶¶50-51. In response to “a rise time of the control voltage source 135 (at turn-on of the amplifier)” (<i>an enable signal</i>) (pink arrow), the speedup circuit applies a transient or time-varying current signal to the base of transistor 119, <i>control current, I<sub>CONTROL</sub></i> (red arrow). <i>Ishimaru</i> ¶52. This is a control current at least because it is used to control the correction to the biasing of <i>Ishimaru’s</i> power amplifier to compensate for gain variation.</p>



Ishimaru, Fig. 1 (annotated).

Ishimaru's speedup circuit 122 (dark blue) includes a time dependent signal generator (red) in that it is a circuit configured to change an enable signal (pink arrow) of the PA to achieve a desired shape of  $I_{CONTROL}$  (red arrow), where the control current changes based on time. The shaping eventually results in the corresponding time-dependent current shown in Figure 3. Ishimaru at ¶8-12, 52-56, Fig. 3. The speedup circuit 112 (dark blue) shapes  $I_{CONTROL}$  (red arrow) and amplifies it to form a correction current ( $I_{CORRECTION}$ ) (gold arrow) as a "current that transiently (temporarily) flows" out of the PA's primary biasing circuit (purple). Ishimaru at ¶52. The time-dependent shape of the  $I_{CONTROL}$  (red arrow) is thereby used to shape the  $I_{CORRECTION}$  (gold arrow) in an amount and duration necessary to cause the primary biasing circuit to send a corresponding temporary boost in

**Claim Language**

***Ishimaru* Alone and/or in Combination with Other References**

*I<sub>BIAS</sub>* to the power amplifier (**green**) to boost its gain during the startup period when its gain would otherwise be too low, *i.e.* to correct for the gain variation of the power amplifier. *Ishimaru* at ¶¶8-12, 52-55, Figs. 2 and 3. The speed up circuit, and its capacitor 121, changes the flat nature of the enable/on signal into a signal that is not just “on”, but instead is made to have a desired time-varying shape for compensating power amplifier gain variation. *Ishimaru* at ¶¶49-52, 55-56.

*Ishimaru* discloses:

“The bias transistor **107** has its collector connected to a bias terminal **108** via a resistance element **133**. The bias terminal **108** is connected to a control voltage source **135**.” *Ishimaru* at ¶ 44.

“In this embodiment, as shown in FIG. 1, the power source circuit 112 has a third transistor 115, a fourth transistor 116, and a resistance element 114. The third transistor 115 has its collector connected to the base of the bias transistor 107 and its emitter connected to the ground. Also, a base of the third transistor 115 is connected to an emitter of the fourth transistor 116. The collector of the third transistor 115 is connected to the bias terminal 108 via a resistance element 131. Meanwhile, the fourth transistor 116 has its emitter connected to the ground via the resistance element 114 and its collector connected to the bias terminal 108 via a resistance element 132.

A connecting point P0 between the base of the third transistor 115 and the emitter of the fourth transistor 116 in the power source circuit 112 is connected to an output terminal 118 of a speedup circuit 122.

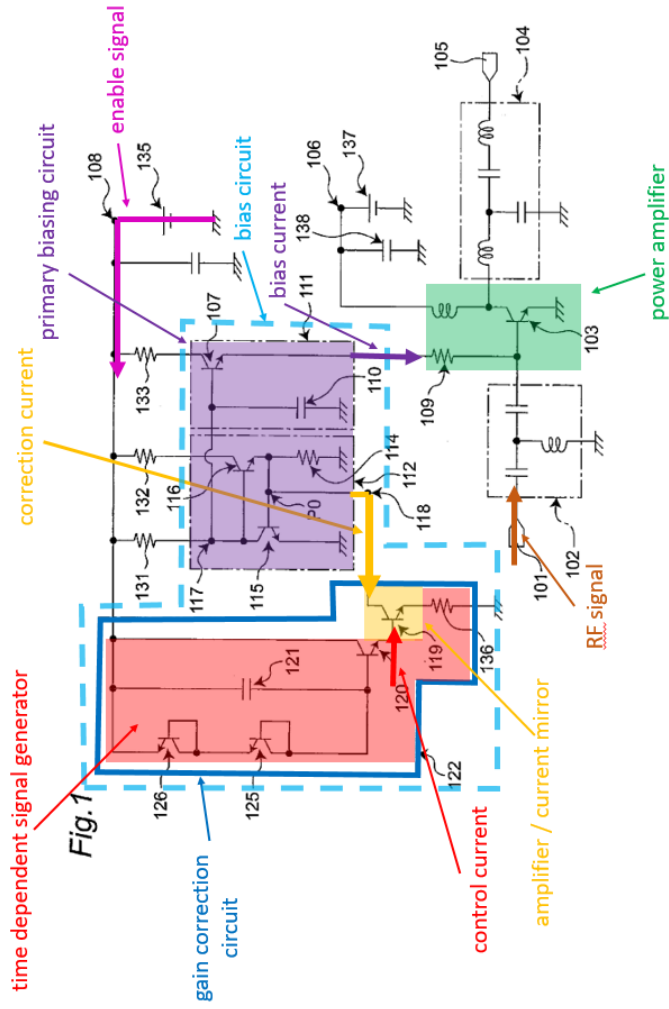
The speedup circuit 122 has a fifth transistor 119 whose collector is connected to the output terminal 118, and a sixth transistor 120 whose emitter is connected to a base of the fifth transistor 119. The emitter of the fifth transistor 119 is connected to the ground via a resistance element 136.

Claim Language	<i>Ishimaru</i> Alone and/or in Combination with Other References
[1b.2] a current amplifier configured to amplify the control current to generate a	<p>The speedup circuit 122 also has a capacitance element 121 which is connected between a base of the sixth transistor 120 and the bias terminal 108, and two diodes 125, 126 which are connected in series between the base of the sixth transistor 120 and the bias terminal 108.</p> <p>In the speedup circuit 122, with electric charge flowing into the capacitance element 121 at a rise time of the control voltage of the control voltage source 135 (at turn-on of the amplifier), a current transiently (temporarily) flows from the output terminal 118 into the fifth transistor 119, causing the voltage value of the output terminal 118 to lower. As a result, due to a change of the bias point of the third transistor 115, the voltage of a connecting terminal 117, which connects the collector of the third transistor 115 to the base of the bias transistor 107, transiently increases. Thus, at the rise time, the current fed to the amplifier transistor 103 by the bias transistor 107 transiently increases. Therefore, at the rise time, the power amplification factor of the amplifier transistor 103 transiently increases, so that the time elapsing until temperature variations due to heat generation of the amplifier transistor 103 come to an equilibrium on the whole circuit is shortened, with a result of reduced distortion of the amplification signal (e.g., modulated wave signal).” <i>Ishimaru</i> at ¶¶ 48 - 52.</p> <p>“In the power amplifier of this embodiment also, the capacitance value of the capacitance element 121 of the speedup circuit 122 is adjusted so as to cancel transient variations in gain due to the temperature variations at a start of power amplification. As a result of this, deterioration of the linearity due to variations of amplification gain can be canceled so that the value of dynamic EVM (error vector magnitude) can be improved.” <i>Ishimaru</i> at ¶ 55.</p>
[1b.2] a current amplifier configured to amplify the control current to generate a	<p><b><u><i>Ishimaru</i> discloses and renders obvious this limitation.</u></b></p> <p><i>Ishimaru</i> discloses and renders obvious a current amplifier configured to amplify the control current to generate a correction current, the current amplifier including a current mirror. See, e.g.:</p>

Claim Language	Ishimaru Alone and/or in Combination with Other References
<p>correction current . . . the current amplifier including a current mirror<sup>6</sup></p>	<p>Ishimaru discloses that <math>I_{CONTROL}</math> (control current) (red arrow) is amplified by transistor 119, (current amplifier) (gold) resulting in the transient <math>I_{CORRECTION}</math> (correction current) (gold arrow) being pulled into the collector of transistor 119 from node 118. Ishimaru at ¶52. A POSITA understood that transistor 119 amplifies its base current, <math>I_{CONTROL}</math>, by the beta factor, <math>\beta</math>,<sup>7</sup> of transistor 119 to provide amplification, e.g., 60 to 150 or higher. Harrison 53-55; Illingworth 38 (practical <math>\beta</math> values can be “up to 500”). Thus, transistor 119 is a current amplifier configured to amplify the current at its base (red arrow) (the control current) to generate the amplified <math>I_{CORRECTION}</math> at its collector (gold arrow) (to generate a correction current). <math>I_{CORRECTION}</math> (gold arrow) is a “current that transiently (temporarily) flows” out of the power amplifier’s primary biasing circuit (purple). Ishimaru ¶52. <math>I_{CORRECTION}</math> (gold arrow) is a correction current in that it is shaped in an amount and duration necessary to cause the primary biasing circuit (discussed below) to send a corresponding temporary boost in <math>I_{BIAS}</math> (purple arrow) to the power amplifier (green) to boost its gain during the startup period when its gain would otherwise be too low, i.e. to correct for the gain variation of the power amplifier. Ishimaru ¶¶8-12, 52, 55, Figs. 2 and 3.</p>

<sup>6</sup> The current mirror limitation (the current amplifier including a current mirror) appears at the end of claim 1 of the '101 Patent. This chart includes the limitation here so as to discuss it topically with the “current amplifier” claim limitations, consistent with the other asserted independent claims of the Group 1 Patents.

<sup>7</sup> A POSITA understood that the collector current  $I_C$  of a BJT transistor such as 119 is related to the base current  $I_B$  by  $\beta_F$ , (the “forward gain current”):  $I_C = \beta_F * I_B$ . Grebene, p. 59. (Eq. 2.1). Thus, the BJT functions as a “current-controlled current amplifier.” Grebene, p. 58, Fig. 2.6. “A given amount of base current  $I_B$  injected into the base terminal causes a much larger collector current  $I_C$  to flow.” *Id.*



Ishimaru, Fig. 1 (annotated).

Ishimaru discloses:

“In this embodiment, as shown in FIG. 1, the power source circuit 112 has a third transistor 115, a fourth transistor 116, and a resistance element 114. The third transistor 115 has its collector connected to the base of the bias transistor 107 and its emitter connected to the ground. Also, a base of the third transistor 115 is connected to an emitter of the fourth transistor 116. The collector of the third transistor 115 is connected to the bias terminal 108 via a resistance element 131. Meanwhile, the fourth transistor 116 has its

**Claim Language**

***Ishimaru* Alone and/or in Combination with Other References**

emitter connected to the ground via the resistance element 114 and its collector connected to the bias terminal 108 via a resistance element 132.

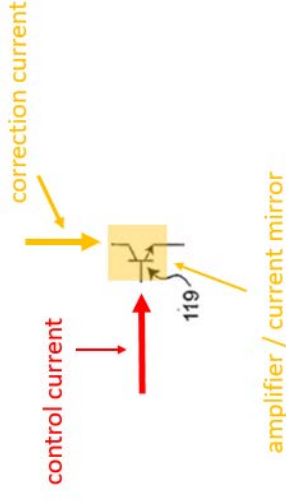
A connecting point P0 between the base of the third transistor 115 and the emitter of the fourth transistor 116 in the power source circuit 112 is connected to an output terminal 118 of a speedup circuit 122.” *Ishimaru* at ¶¶ 48-49.

“In the speedup circuit 122, with electric charge flowing into the capacitance element 121 at a rise time of the control voltage of the control voltage source 135 (at turn-on of the amplifier), a current transiently (temporarily) flows from the output terminal 118 into the fifth transistor 119, causing the voltage value of the output terminal 118 to lower. As a result, due to a change of the bias point of the third transistor 115, the voltage of a connecting terminal 117, which connects the collector of the third transistor 115 to the base of the bias transistor 107, transiently increases. Thus, at the rise time, the current fed to the amplifier transistor 103 by the bias transistor 107 transiently increases. Therefore, at the rise time, the power amplification factor of the amplifier transistor 103 transiently increases, so that the time elapsing until temperature variations due to heat generation of the amplifier transistor 103 come to an equilibrium on the whole circuit is shortened, with a result of reduced distortion of the amplification signal (e.g., modulated wave signal).” *Ishimaru* at ¶ 52.

“In the power amplifier of this embodiment also, the capacitance value of the capacitance element 121 of the speedup circuit 122 is adjusted so as to cancel transient variations in gain due to the temperature variations at a start of power amplification. As a result of this, deterioration of the linearity due to variations of amplification gain can be canceled so that the value of dynamic EVM (error vector magnitude) can be improved.” *Ishimaru* at ¶ 55.

### Current Mirror

*Ishimaru*'s transistor 119 (the *current amplifier*) is a *current mirror* in that transistor 119 is configured to replicate (i.e. *mirror*) and scale (amplify) the  $I_{CONTROL}$  (red arrow) to generate the  $I_{CORRECTION}$  (gold arrow), as shown in Fig. 1, partially reproduced below:



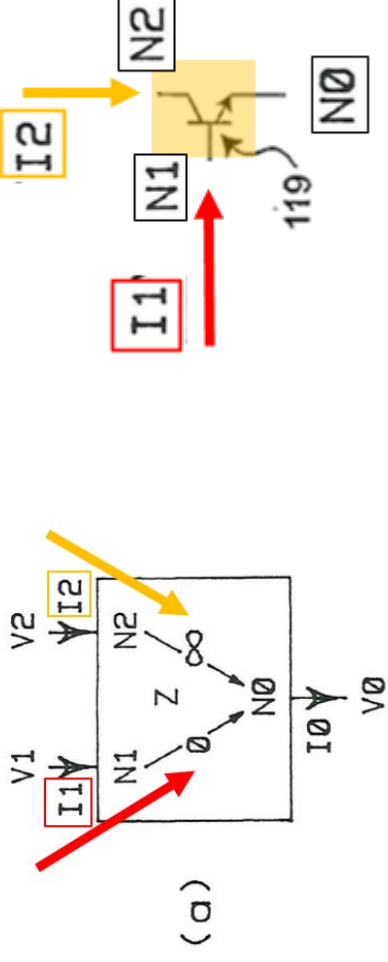
*Ishimaru* Fig. 1 (annotated) (partial).

Consistent with the discussion of current mirrors in the State of the Art section, transistor 119 as connected in *Ishimaru* is configured to mirror in that it is configured to replicate (reproduce, duplicate, reflect, etc.), i.e., *mirror* the current at its input (the base of transistor 119) to generate the current at its output (the collector of transistor 119). State of the Art (Appendix A-03, § II); *Ishimaru* Fig. 1.

When connected as shown in *Ishimaru*, transistor 119 takes the general, three-node form set out by *Barrie Gilbert* and *Gray* for a *current mirror*. *Gilbert* Fig. 6.1a; *Gray* Fig. 4.1. Accordingly, in the side-by-side images below, *Ishimaru*'s transistor 119 is used as a current mirror in that node N1 (of *Gilbert* Figure 6.1a showing a current mirror) is the base of transistor 119, N2 the collector of transistor 119, and N0 the emitter of transistor 119, with the circuit replicating (and scaling) current I1 to generate output current I2. *Gilbert* 242, Fig. 6.1a; *Gray* Fig. 4.1.

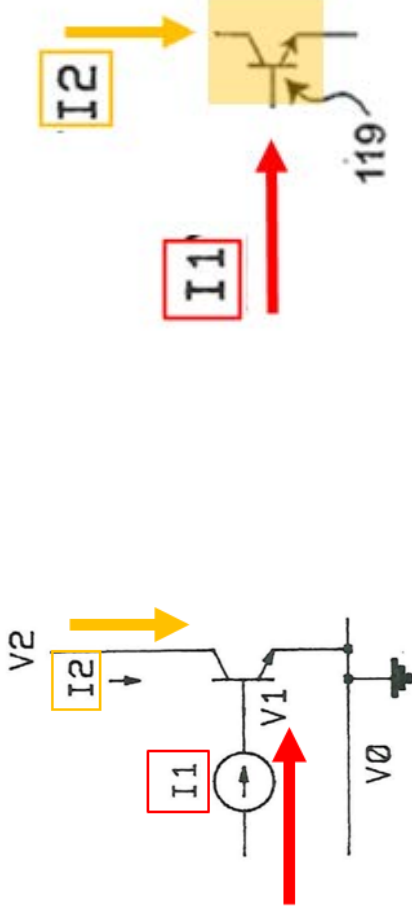
Claim Language

Ishimaru Alone and/or in Combination with Other References



Gilbert 240, Fig. 6.1a (annotated) Ishimaru Fig. 1 (annotated) (partial)

Likewise, Ishimaru's transistor 119 is connected and used in the same way as Gilbert's single transistor current mirror shown in his Figure 6.2a.



Gilbert 243, Fig. 6.2a (annotated) Ishimaru Fig. 1 (annotated) (partial)

In addition to the replication discussed above, *Ishimaru*'s current mirror is further configured to **amplify** the  $I_{CONTROL}$ , scaling it up by the amplification factor to form  $I_{CORRECTION}$ , namely scaling by the common-emitter current-gain,  $\beta$ , of the transistor 119, which quantifies the "mirror ratio" (discussed below) of *Ishimaru*'s current mirror. State of the Art (Appendix A-03, § II.B). *Illingworth* 38; *Gilbert* 242-243. The current at the collector ( $I_{C119}$ ) of transistor 119 (a transistor having  $\beta_{119}$ ) is generally related to the current at the transistor's base ( $I_{B119}$ ) by the equation:  $I_{C119} = \beta_{119} * I_{B119}$ . Thus, the ratio of the input current  $I_{B119}$  to the output current  $I_{C119}$  is generally  $\beta_{119}$ . The gain through the transistor is the "mirror ratio", "M", by which *Ishimaru*'s *current mirror* scales the  $I_{CONTROL}$  to generate the  $I_{CORRECTION}$ . *Gilbert* 242-243; *Ishimaru* Fig. 1. The gain of transistor 119 can be configured to a target value by designing the voltage and current biasing of the transistor 119 (within the constraints of the circuit), such that a  $\beta$  in a range, e.g., of about 60 to 150 or more, can be achieved. The time constant of the transient can

**Claim Language**

***Ishimaru* Alone and/or in Combination with Other References**

then be tuned through the choice of components, namely C121 and R136. *Ishimaru* ¶¶55-56; *see also, infra*, Claim 2.

Thus, transistor 119 as connected in *Ishimaru* is a *current mirror* in that it constitutes a circuit configured to mirror a current, which can be configured to achieve a target gain. Transistor 119 is a circuit that has electrical interconnections, including input/output, and other connections that permit current to flow through the circuit.

***Ishimaru* in view of *Harrison* discloses this limitation.**

To the extent Complainant asserts that *Ishimaru* does not disclose or render obvious a current mirror, *Ishimaru* in view of *Harrison* discloses this limitation.

As discussed above for this limitation, *Ishimaru* discloses a speedup circuit 122 that responds at “a rise time of the control voltage of the control voltage source 135 (at turn-on of the amplifier)” to generate a time-varying current via capacitor 121 that is amplified by 120 and 119 (*current amplifier*). Furthermore, as illustrated in the annotated Figure 1, below, a POSITA recognizes that *Ishimaru* uses the amplified version of the current (**red arrow**) as a current sink to pull a specifically shaped correction current (**gold arrow**) out of the primary biasing circuit.

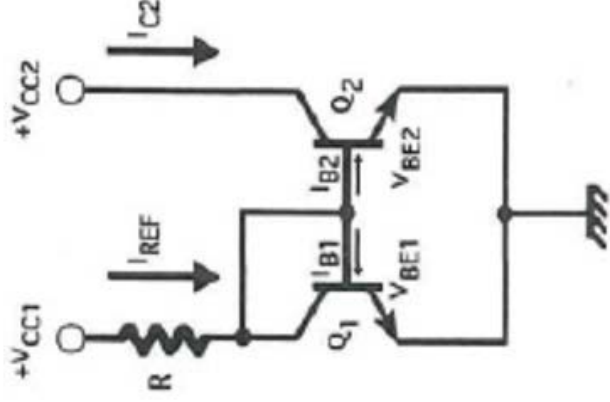


**Claim Language**

***Ishimaru* Alone and/or in Combination with Other References**

mirror structures to couple the two sides of *Ishimaru*'s circuit to achieve the well-known benefits of such current mirrors.

In that regard, *Harrison* teaches a well-known "basic" current mirror using NPN transistors that operates as a "mirror-sink," as shown in the excerpt of Figure 4.18 below:



*Harrison* 71, Fig. 4.18.

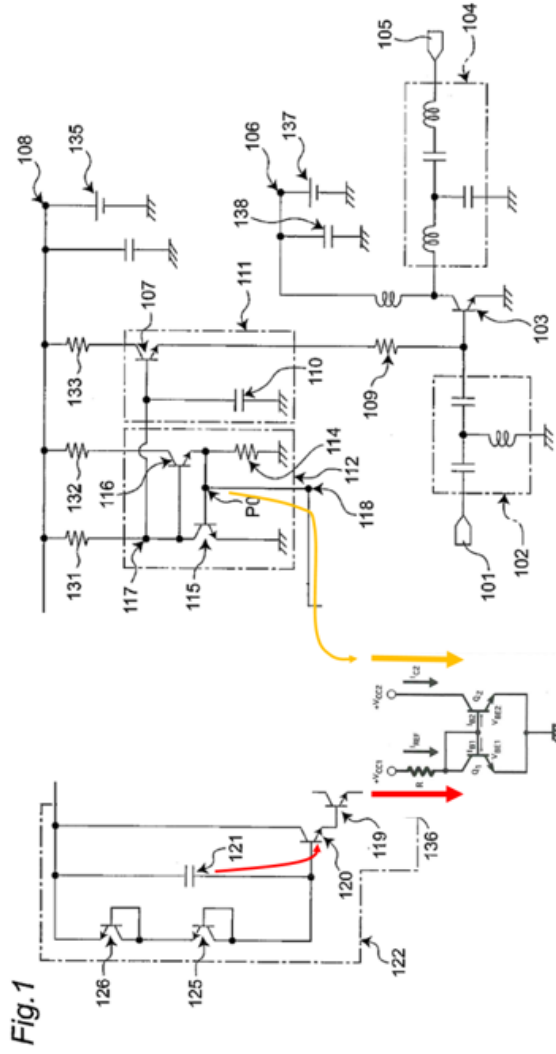
As shown in Fig. 4.18, *Harrison*'s current mirror has at least two transistors (Q1 and Q2) with their base terminals tied together. *Harrison* 71, Fig. 4.18. Further, *Harrison*'s current mirror is a circuit configured to mirror  $I_{REF}$  to  $I_{C2}$ , and is configurable to achieve a target gain that can be finely tuned by adjusting the ratio of the transistor sizes. *Harrison*

Claim Language

Ishimaru Alone and/or in Combination with Other References

95 (describing “current scaling” by setting the ratio of the emitter area). See also Gilbert 280; Gray 254, 257; Grebene 172.

A POSITA would recognize modifying the speedup circuit as taught by Ishimaru to add a basic current mirror as taught by Harrison would be beneficial because it provides flexibility in allowing a broader range of voltages and a broader range of amplification due to the ability to achieve the desired current amplification by changing the ratios of transistor sizes in the basic current mirror. See State of the Art, § II.B. Obviousness does not require bodily incorporation of references or building an actual circuit, but the ease with which a POSITA would advantageously apply Harrison’s teaching to Ishimaru as illustrated below in the following annotated figures, derived from Ishimaru’s Figure 1 and Harrison’s Figure 4.18.



As illustrated above, a basic current mirror such as taught by Harrison can be advantageously added to Ishimaru’s speedup circuit by interposing the basic current mirror



**Claim Language**

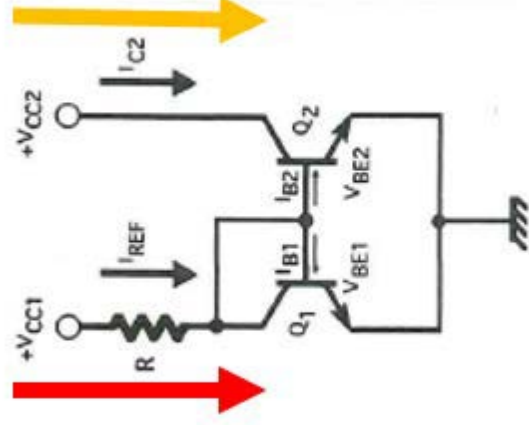
***Ishimaru* Alone and/or in Combination with Other References**

*mirror* to generate a time-varying correction current (gold arrow) that is pulled from node 118.

A POSITA would have been highly motivated to combine *Ishimaru*'s teaching of a bias circuit for a PA with *Harrison*'s disclosure of a basic current mirror and have a reasonable expectation of success for at least the following reasons:

*Harrison* discloses a "basic" current mirror. *Harrison* 71. Current mirrors were well-known in the art and were considered "a familiar icon of modern analog design." *Gilbert* 239. Indeed, current mirrors were "widely used in analog integrated circuits" "as biasing elements" and were "particularly useful building blocks for analog circuit design." *Gray* 251; *Grebene* 170.

One of these advantages was that current mirrors take a reference current in one branch of a circuit and accurately reproduce or reflect that current in a second branch of that circuit, and can do so "relatively independent of the absolute values of the device parameters." *Grebene* 170-171. Thus, current mirrors were useful in coupling circuits together such that an input current could be provided into one branch of a circuit and the current mirror would then replicate (or *mirror*) that current such that the current mirror would pull a mirrored version of that current out of the second branch of the circuit. *Harrison* illustrates this configuration (called a current sink), where the input branch is annotated in red and the output branch is annotated in yellow. *Harrison* 71.



Basic NPN Current sink

Basic BJT current mirrors.

Harrison Fig. 4.18 (annotated).

Further, current mirrors were known to be useful in providing desired current scaling when mirroring a current (called **current mirror gain**) by changing the ratios of transistor sizes. Harrison 95 (describing “current scaling” by setting the ratio of the emitter area). In the case of bipolar junction transistors, this would be done by changing the relative sizes of the emitters of the current mirror transistors. Gray 25. Scaling transistor sizes in current mirrors to achieve granular, targeted levels of scaling that could advantageously be fine-

**Claim Language**

***Ishimaru* Alone and/or in Combination with Other References**

tuned was well understood as of the priority date of the '101 Patent, and described in multiple textbooks. See *Gray* 251-257; *Grebene* 172; *Gilbert* 252, 280.

In addition, a POSITA understood that *Harrison*'s two-transistor current mirror would advantageously provide better isolation between the left side and the right side of *Ishimaru*'s circuit. First, because there are separate emitter currents and paths in the two-transistor mirror, there is a degree of separation between the left and right sides of the circuit. Second, it avoids the issue that using a single transistor like *Ishimaru*'s 119 as the current mirror has coupling (parasitic) between its base and collector due to standard parasitic capacitance. This coupling across 119 can create unwanted coupling across the transistor, such that noise on one side of the circuit can pass to the other side. Adding *Harrison*'s two-transistor current mirror does not have this limitation, providing better isolation between the input and output current signals than *Ishimaru* provides.

A POSITA would thus have been motivated to modify the teachings of *Ishimaru* to add a basic current mirror as taught by *Harrison* because a POSITA understood that *Ishimaru*'s circuit is designed to amplify the current that flows through capacitor 121 (annotated in red below) to generate the current sink pulled from node 118 (annotated in yellow). *Ishimaru* ¶¶50-52, Fig. 1.

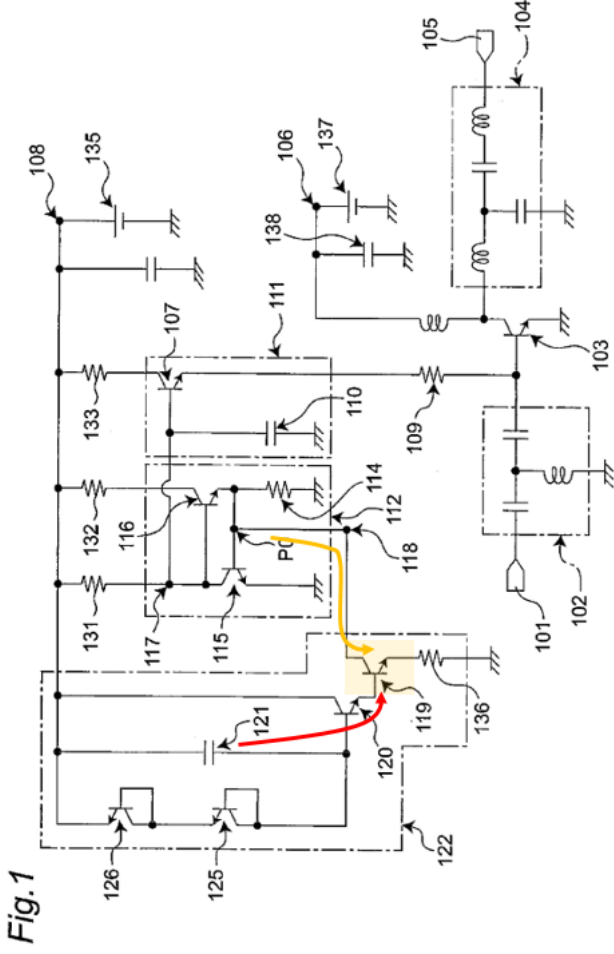


Fig. 1

Ishimaru Fig. 1 (annotated).

A POSITA recognized that *Ishimaru* used a current source (red) from circuit 122 to generate a current sink (yellow) from 112, coupling the two circuits using the current mirroring provided by transistor 119. A POSITA readily understood that this coupling could be improved by use of the basic current mirror of *Harrison* because of multiple advantages of providing an additional stage of fine tuning the current amplification. The additional stage of fine tuning would give the designer an additional degree of freedom in designing the circuit, would provide better isolation between the two sides of the circuit, and allow fine tuning in a final amplification stage that had better linearity, better control,

**Claim Language**

***Ishimaru* Alone and/or in Combination with Other References**

and higher configurability of its mirror ratio, M, in scaling the mirrored current.). See also State of the Art § II.B (discussing two-transistor mirrors).

A POSITA would understand that, without the additional teachings of *Harrison*, *Ishimaru*'s circuit is constrained by the limited configurability of the  $\beta$  (amplification factor) of transistors 119 and 120. *Harrison* 53-55. A POSITA was aware that the  $\beta$  of transistors 119 and 120 would be, e.g., 60 to 150 or more, meaning that the gain of *Ishimaru*'s transistors 119 and 120 would be a relatively large and cumbersome gain (for example, x100 for transistor 120 and x100 for transistor 119 would result in a total gain of 10,000). *Harrison* 53-55; *Illingworth* 38 (practical  $\beta$  values can be "up to 500"). While the  $\beta$  values provide amplification, and, for transistor 119 provide a mirror ratio, that mirror ratio is "not very linear" and "poorly-controlled" compared to other current mirrors, such as the basic current mirror of *Harrison*. *Gilbert* 242; *Harrison* 53-55. Thus, a POSITA readily understood that having to rely upon just the  $\beta$  gains of transistors 119 and 120 is another factor making *Ishimaru*'s circuit overly complicated and constrained.

Adding a basic current mirror similar to that taught by *Harrison*, however, allows for an additional stage of amplification that can be finely tuned, linear, tightly controlled and granular scaling of the current by adjusting the emitter area of the current mirror transistors, as discussed above. Being able to scale currents in this manner would be useful for a circuit designer wanting to establish a speedup control circuit that could advantageously be reused and adapted for different power amplifier applications and product lines. That is because a POSITA understood that different power amplifiers have different startup and steady state operating qualities, and that the gain variation in *Ishimaru*'s Figure 2 is specific to a given power amplifier in a given layout, in a specific operating point and use case. The corresponding corrective transient current thus has a specific amplitude and duration that is suitable for the application at issue.

For example, using different power amplifier circuit layouts (*i.e.* where components are dimensionally closer or farther away from each other), different power amplifier packaging, or different power amplifier integrated circuits using a different semiconductor manufacturing process (e.g., Gallium Arsenide ("GaAs") Heterojunction Bipolar

**Claim Language**

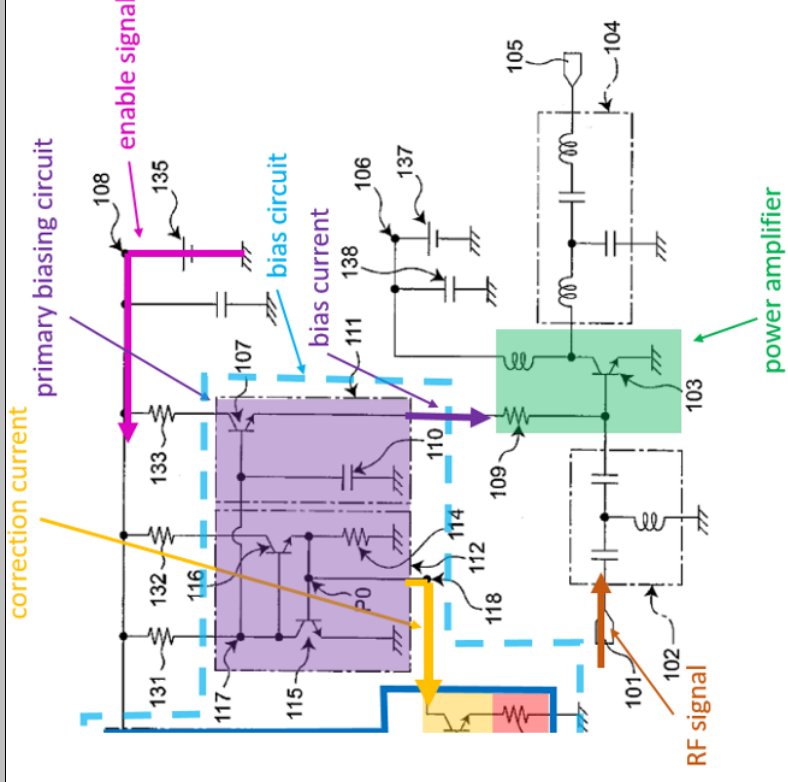
***Ishimaru* Alone and/or in Combination with Other References**

Transistors (“HBTs”) (together “GaAs HBTs”), or Silicon Germanium Bipolar CMOS HBTs (“SiGe BiCMOS HBTs”), will result in different thermal behaviors and startup effects, and so the amount of correction required will vary. *Ishimaru* itself recognizes that temperature effects depend on the layout of the power amplifier and the amount of correction required varies across applications. *Ishimaru* ¶23 (“[T]urn-on behavior of the control voltage source in the amplifier depends on the layout of the amplifier, particularly on the placement of transistors[.]”), ¶3 (“In some communication systems, slight changes of amplification gain as small as 0.2 to 0.3 dB may matter.”), ¶4 (“there are some cases in which variations in amplification ratio or phase on the order of several tens to several hundreds of  $\mu$ s caused by relatively slow temperature increases due to heat generation as an example do matter.”).

Thus, *Ishimaru* provides express motivation for a POSITA to add a current mirror of similar design to *Harrison*’s for its intended purpose in order to provide flexibility in scaling *Ishimaru*’s current, including allowing a designer to tune the operation of *Ishimaru*’s corrective current transient in Figure 3 to a higher peak (such as for a power amplifier having a larger gain variation). A POSITA understands that *Ishimaru*’s circuit otherwise constrains the ability to tune the  $I_{CORRECTION}$  at node 118 as a function of the current through capacitor 121 because of the common, fixed relationships caused by transistor 119 and resistor 136 and the design constraints that limit the configurability of the amplification factors  $\beta$  of transistors 119 and 120. A POSITA would have recognized that *Harrison*’s two-transistor current mirror would advantageously provide an extra degree of freedom in tuning *Ishimaru*’s circuit to compensate for the gain problems of a given PA.

Modifying the teachings of *Ishimaru* with the basic current mirror taught by *Harrison* would involve no more than combining prior art elements (*Ishimaru* and a conventional current mirror) according to known methods (coupling a current source through a positive current mirror to a current sink, while scaling the mirror’s gain to provide tunable amplification) to yield predictable results. Adding a current mirror simply uses a known

Claim Language	Ishimaru Alone and/or in Combination with Other References
	<p>technique (scaling currents between two branches of a current mirror) to improve <i>Ishimaru</i> by scaling its currents between the two branches of its circuits in the same way.</p> <p>The combined teachings of <i>Ishimaru</i> and <i>Harrison</i> is consistent with the disclosure of the '101 Patent that the term <i>current mirror</i> can refer to current amplification circuits including a plurality of current mirrors combined (e.g., cascaded) to achieve a target gain. '101 Patent 11:42-45.</p>
<p>[1b.3] and a primary biasing circuit configured to generate a bias current for the power amplifier based at least partly on the correction current, the bias current configured to correct for a variation in gain of the power amplifier when the power amplifier is enabled,</p>	<p><i>Ishimaru</i> discloses a primary biasing circuit configured to generate a bias current for the power amplifier based at least partly on the correction current, the bias current configured to correct for a variation in gain of the power amplifier when the power amplifier is enabled. See, e.g.:</p> <p><i>Ishimaru</i> discloses “power source circuit 112”, and “bias circuit 111” (collectively, a primary biasing circuit) (purple), which together supply a “base bias current” (<math>I_{BIAS}</math>, a bias current for the power amplifier) (purple arrow) to the amplifier transistor 103 (green). This boost in <math>I_{BIAS}</math> is based on the current drawn out of node 118 (<math>I_{CORRECTION}</math>, the correction current) (gold arrow) when the control voltage is applied (the power amplifier is enabled) (pink arrow) to correct for a variation in gain of the power amplifier at startup.</p> <p>See annotated excerpt of Figure 1, below:</p>



Ishimaru, Fig. 1 (annotated) (partial).

Ishimaru discloses:

“Also, a bias transistor 107 as a second transistor is a transistor that supplies a base bias current to a base terminal of the amplifier transistor 103. An emitter of the bias transistor 107 is connected to a base terminal of the amplifier transistor 103 via a resistance element 109. The resistance element 109 is a ballast (stabilization) resistor which is inserted in a base bias channel to prevent thermal runaway of the amplifier transistor 103.

**Claim Language**

***Ishimaru* Alone and/or in Combination with Other References**

The bias transistor 107 has its collector connected to a bias terminal 108 via a resistance element 133. The bias terminal 108 is connected to a control voltage source 135.

A bias circuit 111 composed of the bias transistor 107 and a capacitance element 110 connected to a base terminal of the bias transistor 107 has a function of increasing the base bias current in response to an increase in signal strength of the input signal, and functions to keep the amplification ratio of an output signal as well as its phase rotation after amplification constant even when the signal strength of the input signal has changed.

A power source circuit 112 is connected to the base terminal of the bias transistor 107 of the bias circuit 111. The bias circuit 111 and the power source circuit 112 constitute a bias power source section.

The power source circuit 112 feeds generally a sum of a “base-emitter voltage” of the amplifier transistor 103 and a “base-emitter voltage” of the bias transistor 107 to the base terminal of the bias transistor 107. That is, the power source circuit 112 feeds a voltage double the base-emitter voltage (hereinafter, referred to as VBE) of a transistor used in the power source circuit 112 to the base terminal of the bias transistor 107. It is noted that voltage drops of the ballast resistor 109 are neglected in this case.” *Ishimaru* at ¶¶ 43 - 47.

“In the speedup circuit 122, with electric charge flowing into the capacitance element 121 at a rise time of the control voltage of the control voltage source 135 (at turn-on of the amplifier), a current transiently (temporarily) flows from the output terminal 118 into the fifth transistor 119, causing the voltage value of the output terminal 118 to lower. As a result, due to a change of the bias point of the third transistor 115, the voltage of a connecting terminal 117, which connects the collector of the third transistor 115 to the base of the bias transistor 107, transiently increases. Thus, at the rise time, the current fed to the amplifier transistor 103 by the bias transistor 107 transiently increases. Therefore, at the rise time, the power amplification factor of the amplifier transistor 103 transiently increases, so that the time elapsing until temperature variations due to heat generation of the amplifier transistor 103 come to an equilibrium on the whole circuit is shortened, with

**Claim Language**

***Ishimaru* Alone and/or in Combination with Other References**

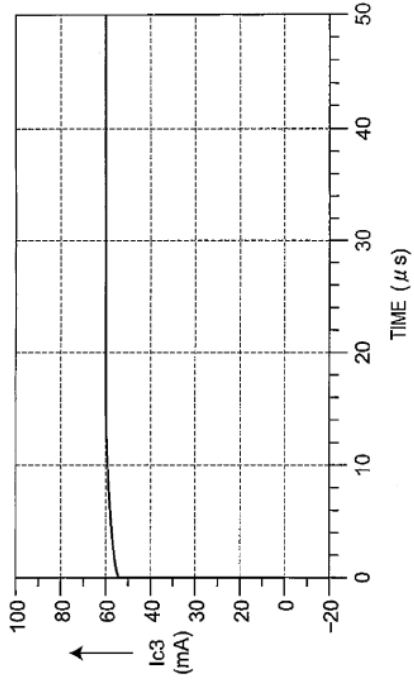
a result of reduced distortion of the amplification signal (e.g., modulated wave signal).” *Ishimaru* at ¶ 52.

“In the power amplifier of this embodiment also, the capacitance value of the capacitance element **121** of the speedup circuit **122** is adjusted so as to cancel transient variations in gain due to the temperature variations at a start of power amplification. As a result of this, deterioration of the linearity due to variations of amplification gain can be canceled so that the value of dynamic EVM (error vector magnitude) can be improved.” *Ishimaru* at ¶ 55.

“Next, FIG. 3 shows an example (simulation result) of transient response of the operating current (collector current Ic3) of the amplifier transistor 103 in the power amplifier of this embodiment. In this embodiment, the current to be fed from the bias transistor 107 to the amplifier transistor 103 is forcedly increased at turn-on of the amplifier, with the result that the value of the operating current Ic3 comes to a steady state in about 4 the time of transient response of the comparative example of FIG. 2. Thus, occurrence of distortions of the amplification signal due to temperature variations in the amplifier circuit is suppressed, so that the linearity of the circuit in burst operation is improved. That is, gain variations due to collector current variations of the power amplifier using a bipolar transistor can be compensated.” *Ishimaru* at ¶ 54, Fig. 1, Fig. 2, Fig. 3.

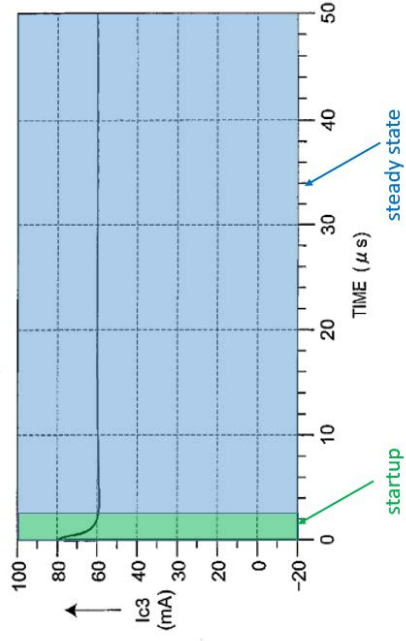
“In the power amplifier of this embodiment also, the capacitance value of the capacitance element **121** of the speedup circuit **122** is adjusted so as to cancel transient variations in gain due to the temperature variations at a start of power amplification. As a result of this, deterioration of the linearity due to variations of amplification gain can be canceled so that the value of dynamic EVM (error vector magnitude) can be improved.” *Ishimaru* at ¶ 55, Fig. 1.

Fig.2 PRIOR ART

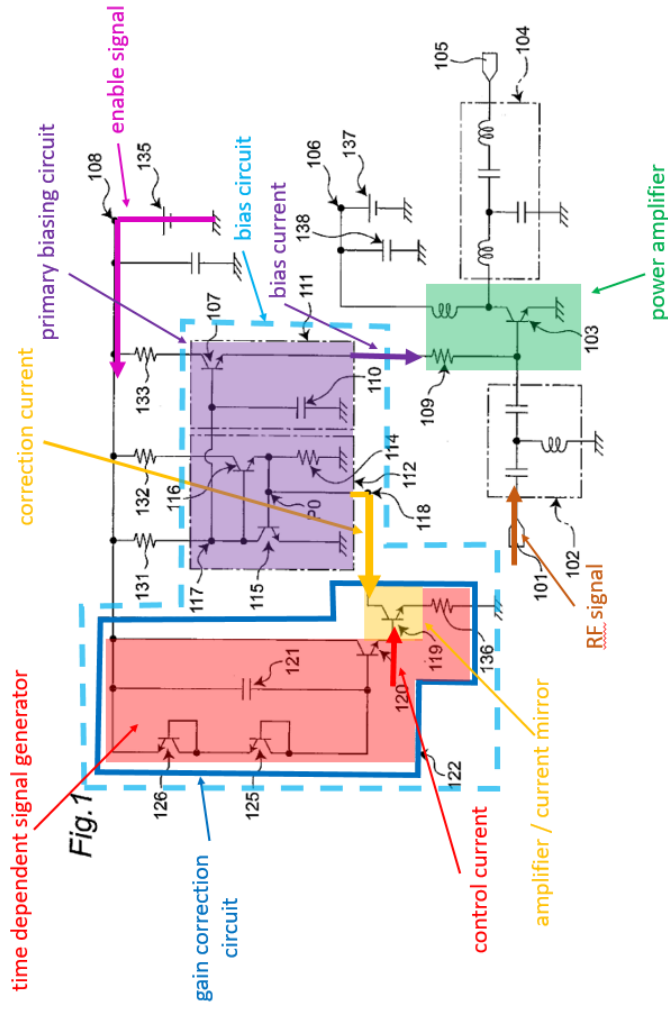


Ishimaru, Fig. 2 (annotated).

Fig.3



Claim Language	Ishimaru Alone and/or in Combination with Other References
<p>[2] 2. The power amplifier system of claim 1 wherein the time-dependent signal generator includes a resistor-capacitor (RC) network.</p>	<p>Ishimaru, Figs. 2 and 3 (annotated).</p> <p style="text-align: center;"><b>Claim 2</b></p> <p>Ishimaru discloses the time-dependent signal generator includes a resistor-capacitor (RC) network. See, e.g.:</p> <p>Ishimaru discloses a “speedup circuit 122” (dark blue) that includes a time-dependent signal generator (red) that “transiently (temporarily) increases” the <math>I_{BIAS}</math> (purple) fed to the amplifier transistor (green) by the bias circuit during the period after startup. Ishimaru at ¶13. Speedup circuit 122 includes transistors 119, 120, resistor 136, as well as a capacitor 121 connected between the base of transistor 120 and bias terminal 108 (a resistor-capacitor (RC) network). Ishimaru at ¶¶50-51, 55-56.</p> <p>See annotated Figure 1 below:</p>



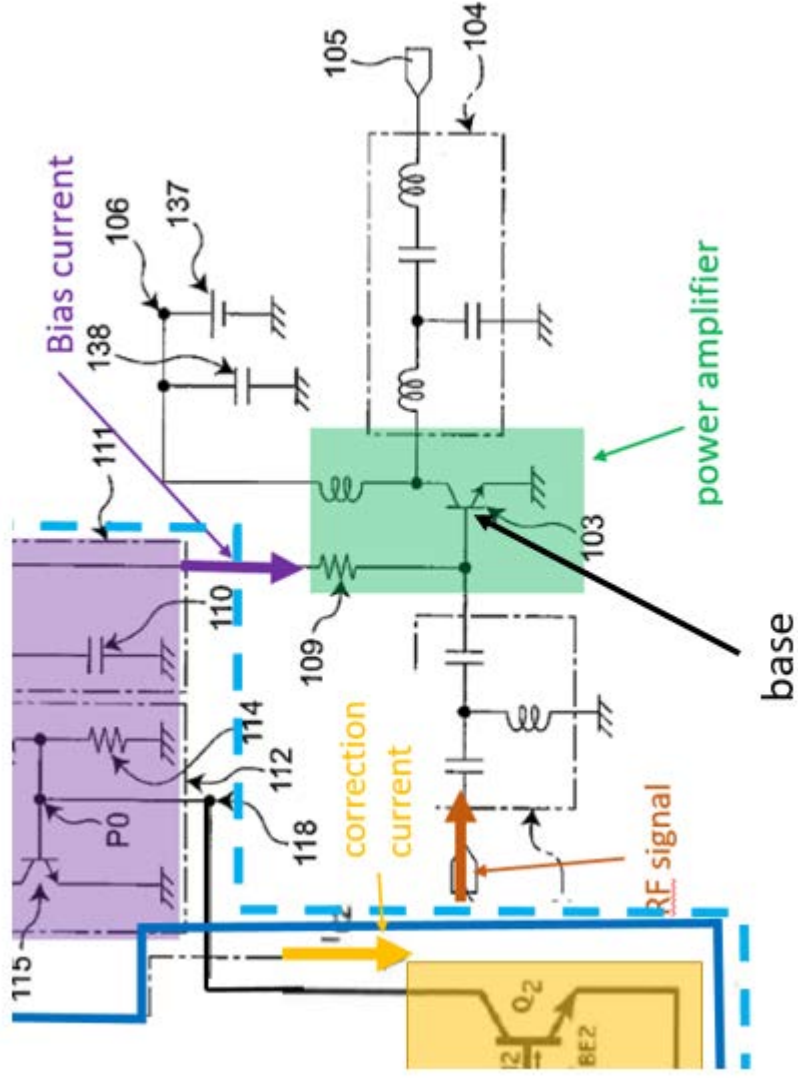
Ishimaru, Fig. 1 (annotated).

Ishimaru discloses:

“The speedup circuit 122 has a fifth transistor 119 whose collector is connected to the output terminal 118, and a sixth transistor 120 whose emitter is connected to a base of the fifth transistor 119. The emitter of the fifth transistor 119 is connected to the ground via a resistance element 136.

The speedup circuit 122 also has a capacitance element 121 which is connected between a base of the sixth transistor 120 and the bias terminal 108, and two diodes 125, 126 which

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	<p>are connected in series between the base of the sixth transistor 120 and the bias terminal 108.” <i>Ishimaru</i> at ¶¶ 50 - 51.</p> <p>A POSITA understands that the time constant of this RC network is established in part by resistor 136 and capacitor 121. This is also true in the combination of <i>Ishimaru</i> with <i>Harrison</i>. See [1b.2].</p>
<b>Claim 10</b>	
<p>[10] 10. The power amplifier system of claim 1 wherein the power amplifier includes a bipolar transistor having an emitter, a base and a collector, the base configured to receive the RF signal and the bias current.</p>	<p><i>Ishimaru</i> discloses a power amplifier including a bipolar transistor having an emitter, base, and collector, where the base is configured to receive the RF signal and the bias current. See, e.g.:</p> <p><i>Ishimaru</i> discloses a “power amplifier” (a power amplifier) that has “amplifier transistor 103” shown and described as “the power amplifier using a bipolar transistor” (including a bipolar transistor having an emitter, base, and collector), with the base receiving the “high-frequency signal” for “radio communication devices” from terminal 101 (where the base is configured to receive the RF signal) and bias transistor 107 “supplies a base bias current to a base terminal of the amplifier transistor 103” (the base receives the bias current). As illustrated in the annotated portion of Figure below, the base of transistor 103 receives the RF signal (brown arrow) and the bias current (purple arrow):</p>



Ishimaru, Fig. 1 (annotated) (partial).

Ishimaru discloses:

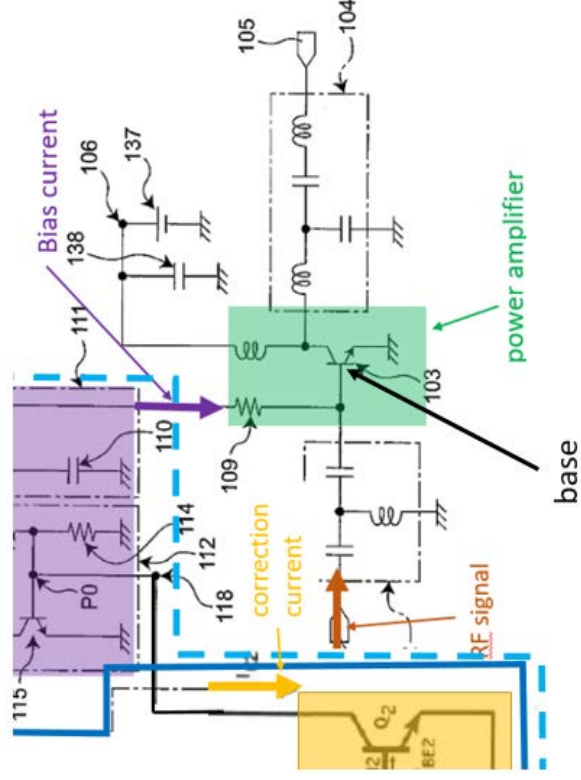
‘FIG. 1 is a circuit diagram showing a circuit construction in an embodiment of the power amplifier of the invention.

Claim Language	<i>Ishimaru</i> Alone and/or in Combination with Other References
	<p>In this power amplifier, a high-frequency signal as an input signal inputted from an input signal terminal 101, passing through an input matching circuit 102, is amplified by an amplifier transistor 103 serving as a first transistor, and then, after passing through an output matching circuit 104, outputted from an output signal terminal 105. In FIG. 1, reference sign 106 denotes a collector bias terminal of the amplifier transistor 103. Between the collector bias terminal 106 and the ground are connected a DC power source 137 and a capacitance element 138. The amplifier transistor 103 forms an amplification section.” <i>Ishimaru</i> at ¶¶ 41 - 42.</p> <p>“Also, a bias transistor 107 as a second transistor is a transistor that supplies a base bias current to a base terminal of the amplifier transistor 103. An emitter of the bias transistor 107 is connected to a base terminal of the amplifier transistor 103 via a resistance element 109. The resistance element 109 is a ballast (stabilization) resistor which is inserted in a base bias channel to prevent thermal runaway of the amplifier transistor 103 is a ballast (stabilization) resistor which is inserted in a base bias channel to prevent thermal runaway of the amplifier transistor 103.”</p> <p><i>Ishimaru</i> at ¶43.</p>
<p>[11] 11. The power amplifier system of claim 10 wherein the emitter is electrically connected to a power low voltage and the collector is configured to generate an amplified version of the RF signal.</p>	<p style="text-align: center;"><b>Claim 11</b></p> <p><i>Ishimaru</i> discloses that <i>the emitter of the bipolar transistor in the power amplifier is electrically connected to a power low voltage and the collector is configured to generate an amplified version of the RF signal. See, e.g.:</i></p> <p><i>Ishimaru</i> discloses that the emitter of transistor 103 is electrically connected to ground (<i>the emitter of the bipolar transistor in the power amplifier is electrically connected to a power low voltage</i>). As shown in annotated Figure 1 below, an input signal terminal 101 receives a high-frequency signal (<b>brown arrow</b>) as an input signal, and this input signal passes through an input matching circuit 102, and is then amplified by amplifier transistor 103 (<b>green</b>). The amplifier transistor 103 outputs a signal through output matching circuit 104 to output signal terminal 105 as an amplified version of the RF input signal (<i>the collector</i></p>

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is configured to generate an amplified version of the RF signal). Ishimaru ¶¶41-43, 46, 49.



Ishimaru, Fig. 1 (annotated) (partial).

Ishimaru discloses:

“FIG. 1 is a circuit diagram showing a circuit construction in an embodiment of the power amplifier of the invention.

In this power amplifier, a high-frequency signal as an input signal inputted from an input signal terminal 101, passing through an input matching circuit 102, is amplified by an amplifier transistor 103 serving as a first transistor, and then, after passing through an output matching circuit 104, outputted from an output signal terminal 105. In FIG. 1,

Claim Language	Ishimaru Alone and/or in Combination with Other References
	<p>reference sign 106 denotes a collector bias terminal of the amplifier transistor 103. Between the collector bias terminal 106 and the ground are connected a DC power source 137 and a capacitance element 138. The amplifier transistor 103 forms an amplification section.” <i>Ishimaru</i> at ¶¶ 41 - 42.</p> <p>“Also, a bias transistor 107 as a second transistor is a transistor that supplies a base bias current to a base terminal of the amplifier transistor 103. An emitter of the bias transistor 107 is connected to a base terminal of the amplifier transistor 103 via a resistance element 109. The resistance element 109 is a ballast (stabilization) resistor which is inserted in a base bias channel to prevent thermal runaway of the amplifier transistor 103 is a ballast (stabilization) resistor which is inserted in a base bias channel to prevent thermal runaway of the amplifier transistor 103.”</p> <p><i>Ishimaru</i> at ¶43.</p>
<b>Claim 17</b>	
[17pre] 17. A method of biasing a power amplifier, the method comprising:	See claims [1b], [1b.1], [1b.2], [1b.3].
[17a] shaping an enable signal using a time-dependent signal generator to generate a control current;	See claim [1b.1].
[17b] amplifying the control current using a current mirror of a current amplifier to generate a correction current; and	See claim [1b.2].
[17c] generating a bias current for a power amplifier using a primary biasing circuit, the primary biasing circuit	See claim [1b.3].

Claim Language	<i>Ishimaru</i> Alone and/or in Combination with Other References
<p>configured to use the correction current to correct for a variation in gain of the power amplifier when the power amplifier is enabled.</p>	
<b>Claim 18</b>	
<p>[18] 18. The method of claim 17 wherein shaping the enable signal includes using a resistor-capacitor (RC) network of the time-dependent signal generator.</p>	<p>See claim [2].</p>
<b>Claim 20</b>	
<p>[20] 20. The method of claim 17 wherein generating the bias current includes shaping the bias current so as to compensate for a gain variation of a heterojunction bipolar transistor (HBT).</p>	<p><i>Ishimaru</i> in view of <i>Johnson</i>, and <i>Ishimaru</i> in view of <i>Harrison</i> and further in view of <i>Johnson</i> render claim 20 obvious.</p> <p><i>Ishimaru</i> in view of <i>Johnson</i> discloses limitation [20] (i.e., generating the bias current includes shaping the bias current so as to compensate for a gain variation of a heterojunction bipolar transistor (HBT)).</p> <p>As discussed above with respect to [1b.3], [17c] and claim 10, <i>Ishimaru</i> discloses shaping the bias current to compensate for a gain variation of the BJT used for its PA transistor 103 for radio communication devices. See [1b.3], [17c], and Claim 10; <i>Ishimaru</i> ¶¶1, 54, 55.</p> <p>A POSITA would understand <i>Ishimaru</i>'s solution to apply to all types of BJT processes for PAs for such radio communications devices, of which heterojunction bipolar transistors (HBT) were a popular, market-leading form for RF PAs. See State of the Art § II.D. As explained in the State of the Art, it was part of the general knowledge in the art to use the HBT form of BJT, as was widely done and well documented, for bipolar junction transistor implementations of RF PAs. <i>Id.</i> This is because HBTs were an improved form of</p>

**Claim Language**

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BJTs, with well-documented advantages for RF power amplification, including, e.g., having the robustness, speed, density, and linearity necessary for such circuits.

While *Ishimaru* does not expressly refer to the use of HBTs, a POSITA would have been motivated to implement *Ishimaru*'s BJT as an HBT (as taught by *Johnson*) for several reasons. First, *Ishimaru* expressly discloses a solution for RF PAs implemented as BJTs, and a POSITA would reasonably draw the inference that *Ishimaru* disclosed the use of its solution for the market leading forms of such BJTs, namely HBTs. State of the Art §II.D. Indeed, it was conventional to use HBTs in the context of radio communication devices having RF PAs using BJT transistors like *Ishimaru*'s. Second, *Ishimaru* is directed to an incremental improvement in the startup behavior of BJT-based RF PAs that is directed at the margin of high performing devices, i.e., the type of BJT-based RF PAs commonly implemented as HBTs. A POSITA understood that HBTs, as BJTs, suffer the same thermal effects described by *Ishimaru*, and would likewise benefit in the same way as other BJTs. For these reasons, a POSITA reading *Ishimaru* in 2011 understood that *Ishimaru*'s "radio communication device" with its PA (green) and bias circuits (blue) would be implemented in an integrated circuit attached to a package substrate in a packaged module as claimed. Thus, while not explicitly stated, the HBT form claimed is nonetheless disclosed to a POSITA in view of the reasonable inferences that a skilled artisan would draw when reading *Ishimaru*.

To the extent *Ishimaru* does not reasonably infer that its PA would employ BJTs using the market-leading HBT form, that would have at minimum been obvious to a POSITA in view of *Johnson*, for the same reasons discussed above and as evidenced by the well-known advantages of HBTs for RF PAs. See State of the Art § II.D. A POSITA would have been motivated to use an HBT for *Ishimaru*'s BJT PA 103 to achieve any one of a host of known benefits such as their "improvement in the high frequency performance of the transistor" (*Illingworth*), their "inherently superior linearity and efficiency performance" (*TriQuint*), their "reliability [being] well known to be excellent" (*TriQuint*), and other advantages in cost, size, robustness, etc. (*Johnson*). See State of the Art § II.D. A POSITA would have been motivated to implement at least the PA of *Ishimaru* as an HBT following these well-documented advantages. *Id.* Doing so would involve nothing more

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than using a market-leading prior art technique (using HBT type of BJT-based RF PAs) according to conventional wisdom for the benefits and successes confirmed by the market and reported by others. Finally, there would have been nothing technologically counterintuitive about implementing *Ishimaru*'s PA system with an HBT as compared to other forms of a BJT. Indeed, the '101 Patent references HBTs in passing, without any special significance, criticality, challenges, or counterintuitive concepts or properties. '101 Patent, 7:53-55. This lack of detail is consistent with the well-developed state of the art for HBT RF PAs. *See* State of the Art § II.D. Furthermore, given *Ishimaru*'s teachings, the selection of a market-leading BJT type (HBT) would have been viewed with a reasonable expectation of success with predictable benefits, all well within the skill of a POSITA as demonstrated by the popularity of HBTs in the marketplace. *Id.*

With respect to *Johnson* specifically, *Johnson* taught multiple advantages, that would motivate adoption of its teachings, in whole or in part:

“SiGe BiCMOS technology is finding increasing use in wireless PA applications. The favorable thermal properties, volume manufacturing capability, and design automation support of SiGe BiCMOS technology have long been recognized. Detailed investigation of the SOA analysis of SiGe HBTs reveals favorable device ruggedness for PA applications.” *Johnson* p. 1612.

“PA designs have been demonstrated for GSM, GPRS, and EDGE wireless standards using a SiGe HBT technology specifically tailored to meet the divergent requirements of high VSWR robustness at high output power and high linearity. The GPRS/EDGE FEM shown here exceeds the 15:1 VSWR requirement at 33 dBm with an overall efficiency of 37%. The SiGe HBT was optimized to simultaneously provide ruggedness and speed and is compatible with the base 0.5 μm CMOS. The favorable thermal properties, lower cost of wafer processing, and the higher integration capabilities demonstrated by these SiGe PAs make them a compelling choice for wireless applications. A SiGe BiCMOS flip-chip together with LTCC is a very strong path for PA modules. The combined module exhibits

Claim Language	<i>Ishimaru</i> Alone and/or in Combination with Other References
	<p>superior performance and stability together with a low component count for the entire front-end solution.” <i>Johnson</i> p. 1612.</p> <p>“Excellent power control is achieved with on-chip PMOS, which regulates the PA collector voltage in the FEM.” <i>Johnson</i> p. 1610.</p> <p>A POSITA would have been motivated to implement at least the power amplifier of <i>Ishimaru</i> as an HBT following the express teachings and benefits stated by <i>Johnson</i>, as discussed above. A POSITA would have been further motivated to use an HBT like <i>Johnson</i>'s following the well-known advantages and industry success of HBTs that were part of the general knowledge in the art, as discussed in the State of the Art, § II.D. Doing so would involve nothing more than using a market-leading prior art technique (using HBT for PAs) according to conventional wisdom for nothing more than the benefits reported and successful adoption of the technique by others. Moreover, there were only a finite number of suitable BJTs to use for PAs, and a POSITA would have been motivated to try at least the ones that had been reported positively, including SiGe HBTs such as <i>Johnson</i>'s.</p>
<b>Claim 21</b>	
[2]pre] 21. A bias circuit for biasing a power amplifier, the bias circuit comprising:	See claim [1b].
[21a] a time-dependent signal generator configured to shape an enable signal of the power amplifier to generate a control current;	See claim [1b.1].
[21b] a current amplifier configured to amplify the control current to generate a	See claim [1b.2].

<b>Claim Language Alone and/or in Combination with Other References</b>	
<b>Claim Language</b>	
correction current, the current amplifier including a current mirror; and	
[21c] primary biasing block configured to generate a bias current for the power amplifier based at least partly on the correction current, the bias current configured to correct for a variation in gain of the power amplifier when the power amplifier is enabled.	See claim [1b.3].
<b>Claim 22</b>	
[22] 22. The bias circuit of claim 21 wherein the time-dependent signal generator includes a resistor-capacitor (RC) network.	See claim [2].