

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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KANGXI COMMUNICATION TECHNOLOGIES (SHANGHAI) CO., LTD.  
Petitioner,

v.

SKYWORKS SOLUTIONS, INC.,  
Patent Owner.

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U.S. Patent 8,717,101

Title: APPARATUS AND METHODS FOR BIASING POWER AMPLIFIERS

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*Inter Partes* Review No.: 2025-00373

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**PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT 8,717,101  
UNDER 35 U.S.C. §§311-319 AND 37 C.F.R. §§42.1-.80, 42.100-.107**

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**PETITIONER’S EXHIBIT LIST**

<b>Exhibit</b>	<b>Brief Description</b>
1001	U.S. Patent 8,717,101 (“the ’101 Patent”)
1002	Prosecution History for U.S. Patent 9,917,101
1003	Declaration of Dr. David Ricketts
1004	U.S. Patent Publication 2009/0212863 (“ <i>Ishimaru</i> ”)
1005	U.S. Patent Publication 2004/0232982 (“ <i>Ichitsubo</i> ”)
1006	Excerpts of Linden T. Harrison, Current Sources and Voltage References, A Design Reference for Electronics Engineers (Elsevier 2005) (“ <i>Harrison</i> ”)
1007	U.S. Patent Publication 2011/0025422 (“ <i>Marra</i> ”)
1008	Johnson, “Silicon-Germanium BiCMOS HBT Technology for Wireless Power Amplifier Applications,” IEEE J. Solid State Circuits, Vol. 39, No. 10 (Oct. 2004) (“ <i>Johnson</i> ”)
1009	Excerpts of Laplante, Comprehensive Dictionary of Electrical Engineering (2d Ed. 2005) (“ <i>Laplante</i> ”)
1010	U.S. Patent Publication No. 2011/0128078 (“ <i>Doherty</i> ”)
1011	Christopher Bowick, “What’s in an RF Front End,” EE Times (Feb. 4, 2008) available at: <a href="https://www.eetimes.com/whats-in-an-rf-front-end/">https://www.eetimes.com/whats-in-an-rf-front-end/</a> (last accessed December 12, 2024) (“ <i>Bowick</i> ”)
1012	Barrie Gilbert, “Bipolar Current Mirrors”, Chapter 6 in Tomazou <i>et al.</i> , Analog IC Design: The Current Mode Approach (Reprinted 2008) (“ <i>Gilbert</i> ”)
1013	Excerpts of Gray <i>et al.</i> , Analysis and Design of Analog Integrated Circuits (5 <sup>th</sup> Ed. 2009) (“ <i>Gray</i> ”)
1014	Excerpts of Grebene, Bipolar and MOS Analog Integrated Circuit Design (2003) (“ <i>Grebene</i> ”)
1015	Excerpts of Illingworth, Dictionary of Electronics (3d Ed. 1998)
1016	Declaration of June Ann Munford
1017	TriQuint Semiconductor, Application Note TVS Protection and Bias Sequencing for HBT Amplifiers, p. 1 (June 2009) (“ <i>TriQuint</i> ”)

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1018	Certified Translation of Japanese Patent Application Publication No. JP 2009-283991 (“ <i>Akagi</i> ”)
1019	U.S. Patent No. 6,831,517 (“ <i>Hedberg</i> ”)
1020	Joint Claim Construction Chart in ITC Inv. No. 337-TA-1413
1021	VintageTek biography, Barrie Gilbert, available at <a href="https://vintagetek.org/barrie-gilbert/">https://vintagetek.org/barrie-gilbert/</a> (“ <i>Gilbert Biography</i> ”)
1022	<i>Diels</i> , Single-Package Integration of RF Blocks for a 5 GHz WLAN Application, IEEE Transactions On Advanced Packaging, Vol. 24, No. 3, (August 2001) (“ <i>Diels</i> ”)
1023	<i>Scherz</i> , Practical Electronics for Inventors (2000) ( <i>Sherz</i> )
1024	<i>Horowitz</i> , Elementary Electricity and Electronics, Component by Component, (1986) (“ <i>Horowitz</i> ”)
1025	<i>Yanjun</i> , “A 2.4-GHz SiGe HBT power amplifier with bias current controlling circuit”, Chinese Institute of Electronics, Journal of Semiconductors, Vol. 30, No. 5, (May 2009), (“ <i>Yanjun</i> ”)
1026	Patent Owner’s Markman Briefs in ITC Inv. No. 337-TA-1413
1027	Petitioner’s Markman Briefs in ITC Inv. No. 337-TA-1413
1028	Commission Investigative Staff’s Markman Briefs in ITC Inv. No. 337-TA-1413

## I. INTRODUCTION

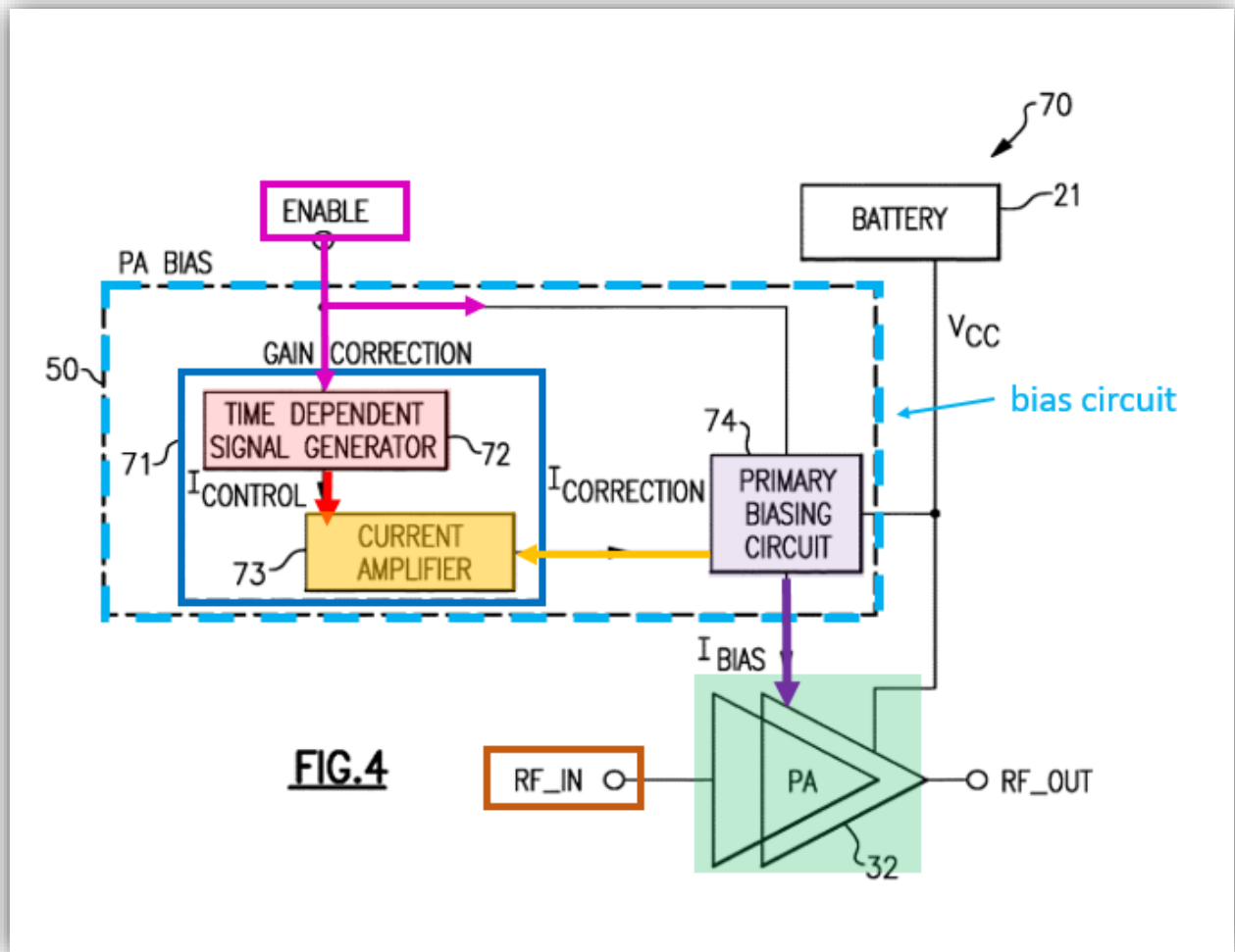
Pursuant to 35 U.S.C. §§311 *et seq.* and 37 C.F.R. §§42.1 *et seq.*, Kangxi Communication Technologies (Shanghai) Co., Ltd. (“Petitioner”) hereby petitions for an *inter partes* review of U.S. Patent 8,717,101 (“the ’101 Patent”). Petitioner respectfully submits that Claims 1-2, 10-11, 17-18, and 20-22 (the “Challenged Claims”) of the ’101 Patent are unpatentable under 35 U.S.C. §103 in view of the prior art references discussed herein. This Petition demonstrates by a preponderance of the evidence that there is a reasonable likelihood that Petitioner will prevail with respect to at least one of these claims. Accordingly, it is respectfully requested that the Board institute an *inter partes* review of the ’101 Patent pursuant to 37 C.F.R. §42.108.

## II. OVERVIEW

The ’101 Patent is directed to a power amplifier (“PA”) and biasing circuit that addresses the problem of PA gain variation at startup, *i.e.*, gain variation during the time period between when the PA is enabled (turned on) and when it reaches steady state operation. Thermal effects at startup can cause the amplifier’s gain to be lower than steady-state gain until the circuitry heats up. This startup/warm-up phenomenon was known in the art at the time of the invention. EX-1003 ¶¶34-37.

The proposed solution was to provide a current boost to the PA bias current to correct for variation of gain when the PA is activated/enabled, *i.e.*, during startup.

EX-1001 4:41-55, 10:9-13; EX-1003 ¶34. Figure 4 of the '101 Patent illustrates a PA bias block that produces a bias current ( $I_{BIAS}$ ) (purple arrow) to the PA (green) including a current boost at startup:



EX-1001 Fig. 4 (Annotated).

The '101 Patent's enable signal (pink arrow) is activated at startup, causing a time-dependent signal generator (red) to generate a shaped control current ( $I_{CONTROL}$ ) (red arrow) that is received by a current amplifier (gold) implemented as a current

mirror. The current mirror replicates (*i.e.* mirrors) and amplifies the  $I_{CONTROL}$  (red arrow) to form the correction current ( $I_{CORRECTION}$ ) (gold arrow), which is pulled<sup>1</sup> from a primary biasing circuit (purple). EX-1003 ¶35.

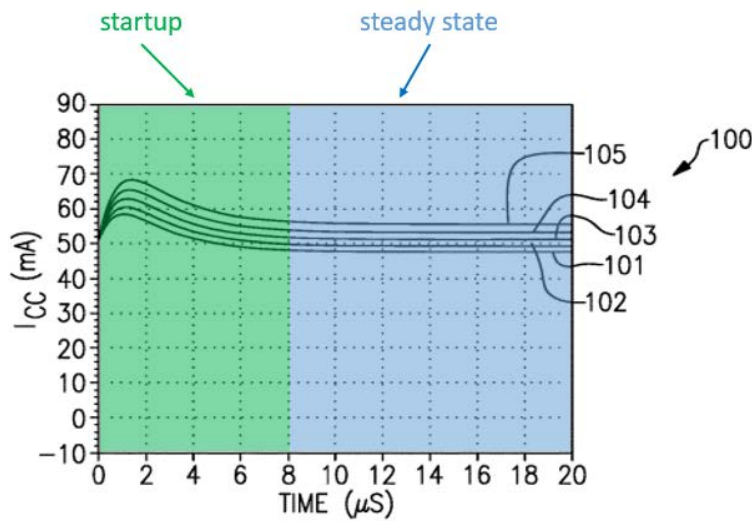
The '101 Patent's time-dependent signal generator and amplifier / current mirror together form a gain correction circuit (dark blue). The  $I_{CONTROL}$  (red arrow) and  $I_{CORRECTION}$  (gold arrow) are shaped to temporarily adjust current in the PA's primary biasing circuit (purple) in an amount and duration necessary to cause the primary biasing circuit to provide a corresponding temporary boost in  $I_{BIAS}$  to boost the PA's gain at startup, compensating for gain variations when the PA is enabled.

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<sup>1</sup> Although Figure 4 has an arrowhead suggesting that  $I_{CORRECTION}$  flows into the primary biasing circuit in some embodiments, that figure is directed to a generic current amplifier, whereas all of the Challenged Claims are directed to the embodiment where the amplifier includes, or is implemented as, a "current mirror." EX-1001 Fig. 5 (mirror 83), 10:23, 11:36-38; *see* §IV.F.2 (discussing current mirrors). In the current mirror disclosure,  $I_{CORRECTION}$  is pulled from the primary biasing circuit as shown in Figure 5. This ability to pull current in a desired amount is a conventional use of a current mirror. *See* §IV.F.2. Given that all of the Challenged Claims are directed to current mirror embodiments, we annotate the direction of  $I_{CORRECTION}$  in Figure 4 using the direction shown in Figure 5.

The amount and duration of the  $I_{CORRECTION}$  is thus configured to counteract and compensate for the thermal startup characteristics of a given PA, *i.e.*, the PA's gain over time absent compensation. EX-1003 ¶36.

The resulting short “boost” in  $I_{BIAS}$  to the PA overcomes its low gain at startup, thereby reaching steady state sooner and providing a flatter gain response versus time, as illustrated by Fig. 6 of the '101 Patent:

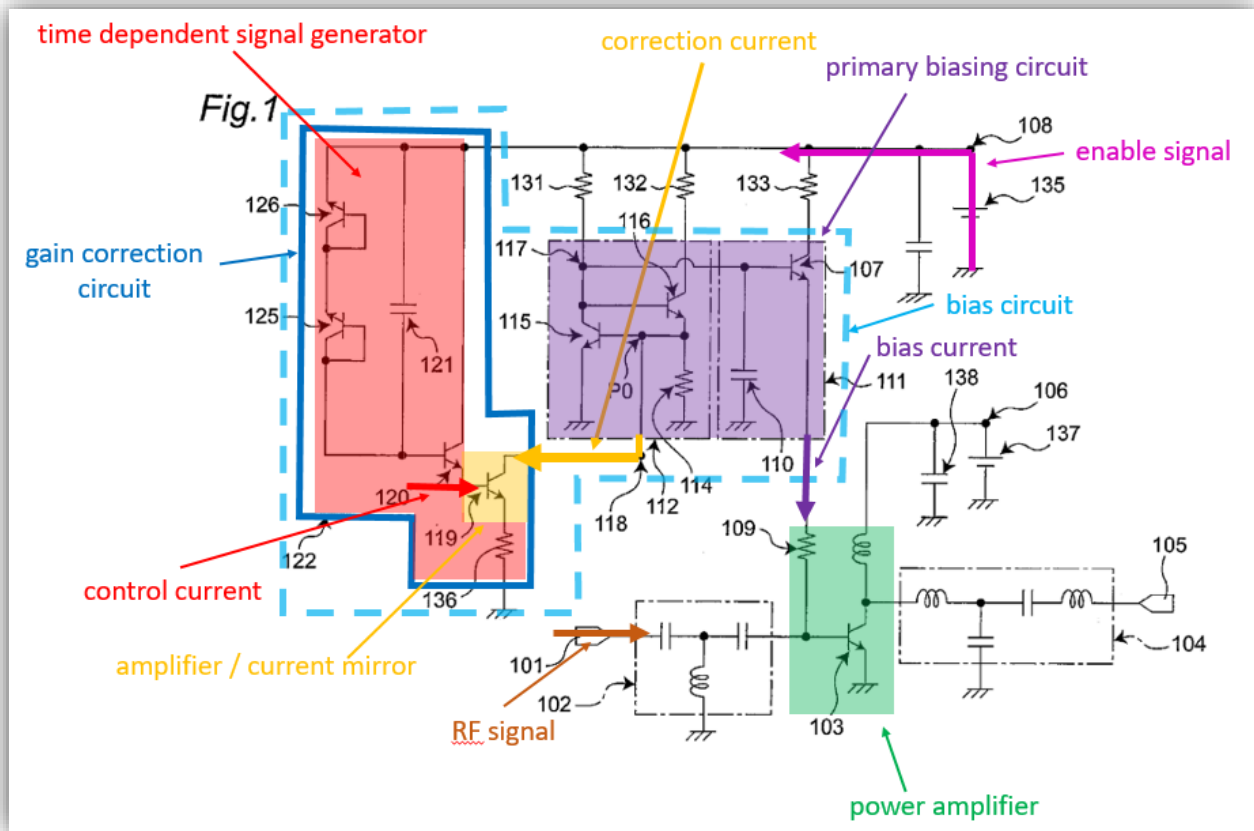


**FIG.6**

EX-1001 Fig. 6 (annotated); EX-1003 ¶37.

However, the use of biasing circuitry to generate a boost current to correct for low gain when a PA is enabled (*i.e.* at startup) was known in the prior art. For example, *Ishimaru* discloses a nearly identical architecture for a PA bias circuit that addresses the same gain variation at PA enablement due to thermal effects at

startup. EX-1004 ¶¶52-54; EX-1003 ¶38. *Ishimaru's* architecture is illustrated below (elements in common with the '101 Patent annotated in a common color):



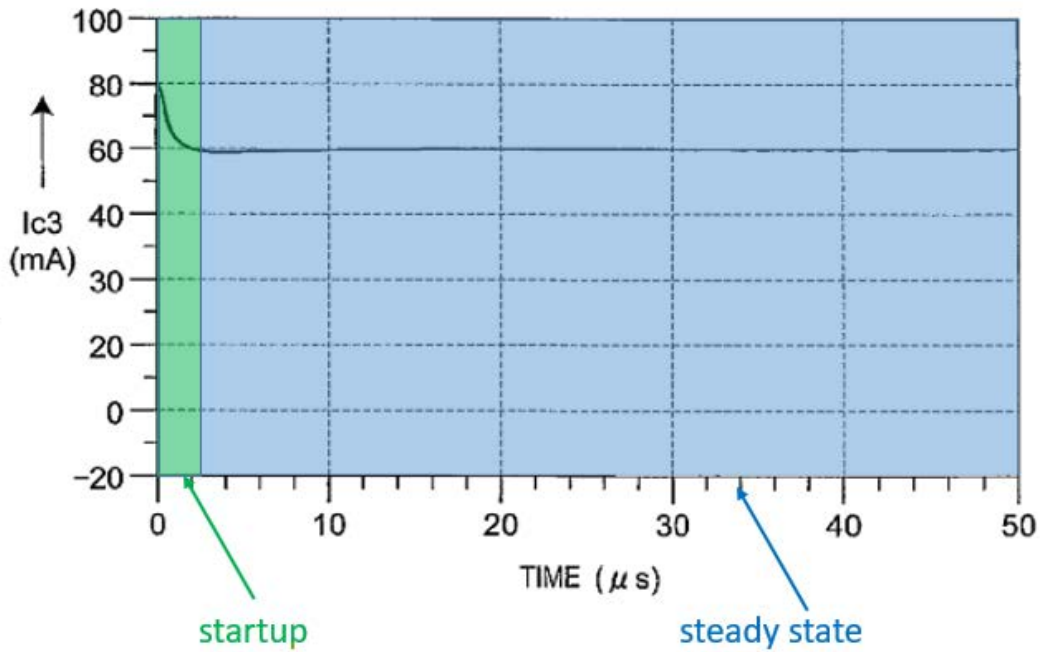
EX-1004 Fig. 1 (annotated).

*Ishimaru's* enable signal (pink arrow) is activated at startup, causing a time-dependent signal generator (red) to generate a shaped control current ( $I_{CONTROL}$ ) (red arrow) that is received by a current amplifier (gold) implemented as a current mirror. The current mirror replicates (*i.e.* mirrors) and amplifies  $I_{CONTROL}$  (red arrow) to form a correction current ( $I_{CORRECTION}$ ) (gold arrow), which is pulled from a primary biasing circuit (purple). EX-1003 ¶39.

*Ishimaru*'s time-dependent signal generator and amplifier/current mirror together form a gain correction circuit (dark blue), which *Ishimaru* calls a "speedup circuit." The speedup circuit (dark blue) is a gain correction circuit in that it is a circuit that generates  $I_{CONTROL}$  and  $I_{CORRECTION}$  (gold arrow) shaped for the purpose of correcting for the low gain of the PA (green) at startup. The  $I_{CONTROL}$  and  $I_{CORRECTION}$  (gold arrow) are shaped to temporarily pull current out of the PA's primary biasing circuit (purple) in an amount and duration necessary to cause the primary biasing circuit to provide a corresponding temporary boost in bias current ( $I_{BIAS}$ ) to the PA (green) to boost its gain during the startup period when its gain would otherwise be too low. The  $I_{CORRECTION}$  is thus configured to compensate for the thermal startup characteristics of a given PA, *i.e.*, the PA's gain over time absent compensation. EX-1003 ¶40.

The resulting short "boost" in  $I_{BIAS}$  is provided to the PA to overcome its low gain at startup, thereby reaching steady state sooner and providing a flatter gain response versus time, as illustrated in Figure 3 of *Ishimaru*:

*Fig.3*



EX-1004 Fig. 3 (annotated); EX-1003 ¶41.

Thus, *Ishimaru* is a parallel disclosure to the '101 Patent in that *Ishimaru* is directed to the same problem and proposes the same solution, but uses slightly different words to describe the same concepts. EX-1003 ¶42.

Thus, as described in Ground 1, the Challenged Claims are obvious over *Ishimaru*. EX-1003 ¶43.

Ground 2 is provided to the extent that the Patent Owner asserts that the *current mirror* term of the Challenged Claims requires importing additional limitations from the specification, in which case the *Harrison* reference discloses these additional limitations. EX-1003 ¶44.

### **III. GROUNDS FOR STANDING UNDER 37 C.F.R. §42.104(a)**

Petitioner certifies that the '101 Patent is available for IPR.

### **IV. REASONS FOR THE REQUESTED RELIEF**

As explained in §§II and VI–VIII of this Petition and in the attached Declaration of Petitioner's Expert, Dr. David Ricketts (EX-1003), the PA and biasing circuit, as described and claimed in the '101 Patent, were obvious over the prior art to a person of ordinary skill in the art ("POSITA") at the time of the invention.

#### **A. Overview of the '101 Patent**

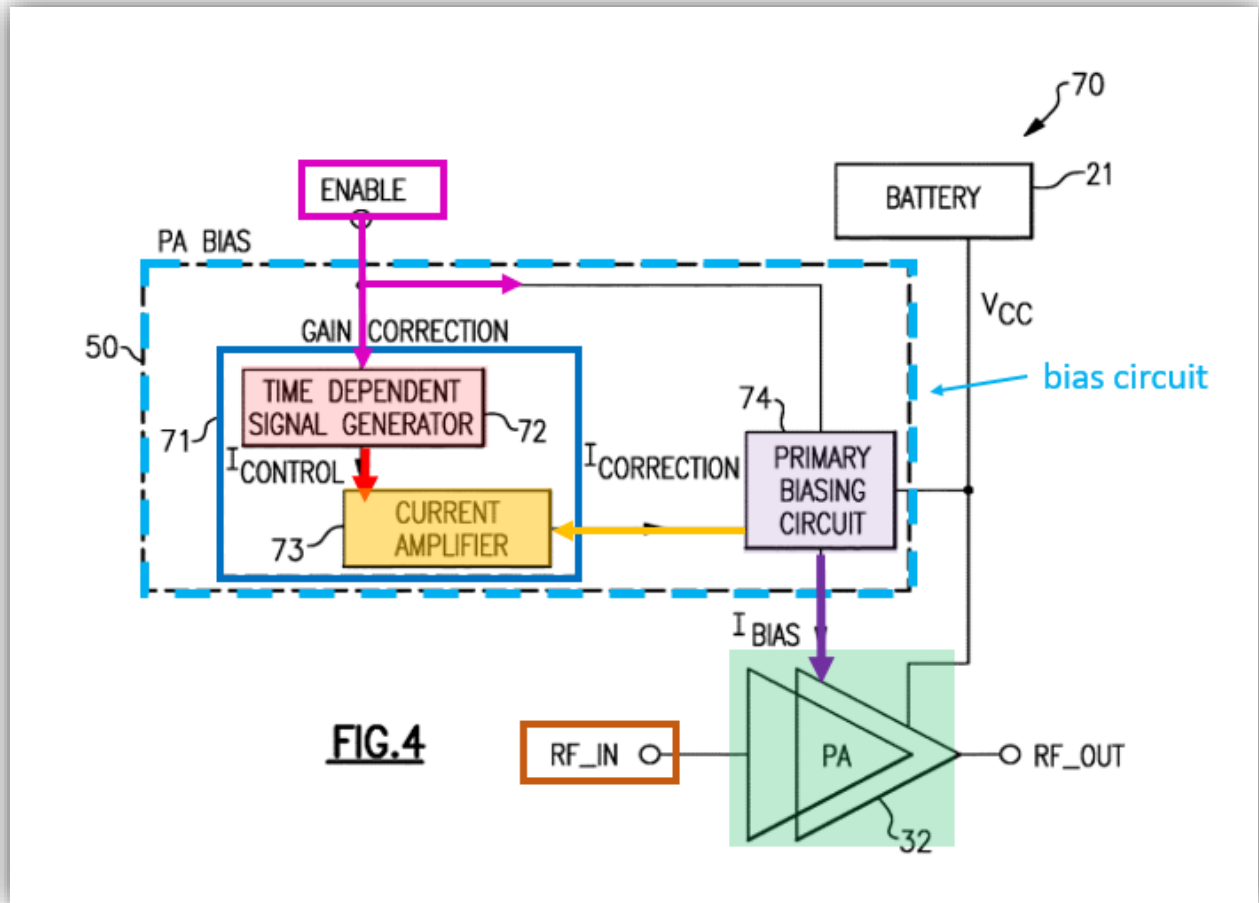
The '101 Patent explains that "RF power amplifiers can be used to boost the power of a RF signal having a relatively low power," and such "[p]ower amplifiers can be included in mobile phones to amplify a RF signal for transmission." EX-1001 1:19-24. The '101 Patent explains that "[t]here is a need for improving power amplifier biasing." EX-1001 1:31-33. Biasing is the application of a suitable DC voltage or current (typically a DC offset applied to the base terminal of a transistor) to set or place the constituent PA transistor in an "on" state at a particular operating point so that it is ready to undertake AC signal amplification. EX-1023 141. Bias conditions of a PA can be thought of as "idling conditions" in that they are established when there is no AC signal at the input of the transistor, *i.e.* the conditions present when idling. EX-1024 220-228; EX-1003 ¶¶45-50.

The '101 Patent is directed to the problem that “shortly after a power amplifier is enabled, absent compensation, the current of a primary biasing circuit can come up slow due to thermal effects, and the power amplifier’s gain can be low.” EX-1001 4:32-35; EX-1003 ¶45.

The specification purports to solve that problem by providing “a current boost ... to the power amplifier [bias signal] so as to provide the power amplifier with a substantially flat gain response versus time.” EX-1001 4:28-40. Specifically, the specification describes “a power amplifier and a power amplifier bias block” where the bias block receives “an enable signal” to turn the PA on. *Id.* The bias block includes a “primary biasing circuit” and a “gain correction block”, which includes a “time-dependent signal generator” and “current amplifier.” The “time-dependent signal generator” shapes the enable signal to generate  $I_{CONTROL}$ , which is amplified to generate  $I_{CORRECTION}$ . The primary biasing circuit generates  $I_{BIAS}$  for the PA using  $I_{CORRECTION}$ .  $I_{CORRECTION}$  is used to adjust  $I_{BIAS}$  to compensate for a variation in gain of the PA over time when the PA is “transitioned from a disabled state to an enabled state.” Specifically,  $I_{BIAS}$  is temporarily “boosted” to overcome the PA’s “low” gain at startup, providing the PA “with a substantially flat gain response versus time.” *Id.* 4:10-39; EX-1003 ¶46.

Figure 4 (below) illustrates the PA system with a PA bias block 50, battery 21, and PA 32 (green). EX-1001 8:64-9:1. The PA bias block includes both a gain

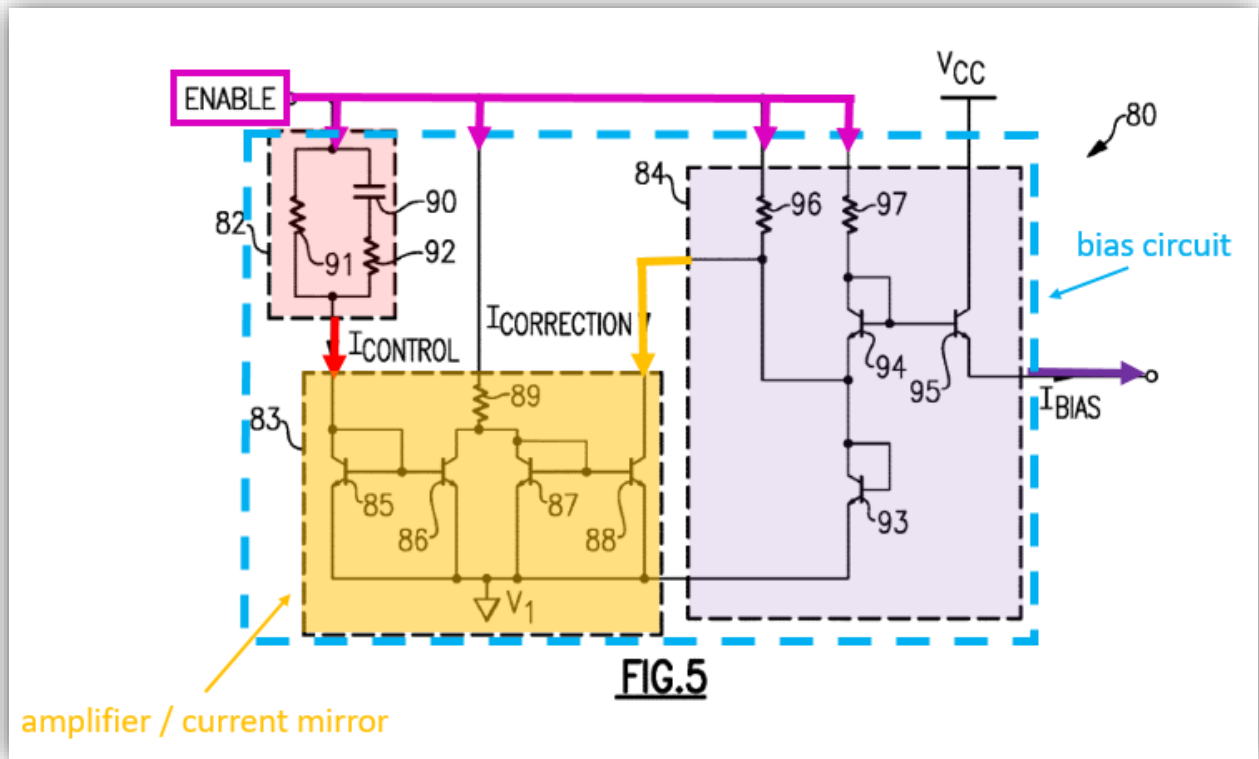
correction block 71 (dark blue) and a primary biasing circuit 74 (purple). When the ENABLE signal is on, the bias block provides  $I_{BIAS}$  to the base of a bipolar transistor of PA 32. *Id.* 9:13-22; EX-1003 ¶47.



*Id.* Fig. 4 (annotated).

The “bias circuit” (light blue) consists of a conventional “primary bias circuit” 74 (purple) driven by a conventional, unmodified “enable signal” (purple), plus a supplemental “gain correction circuit” (dark blue) that generates the supplemental  $I_{CORRECTION}$  to shape the  $I_{BIAS}$  that emerges from the primary bias circuit. The “time-

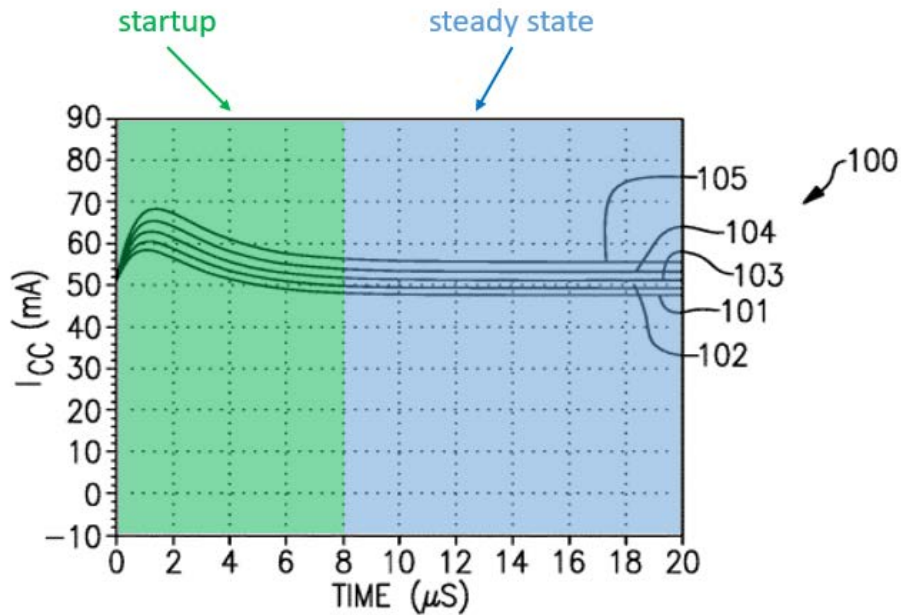
dependent signal generator” (red) produces a small current signal  $I_{CONTROL}$  that varies in time with a desired shape and then the current amplifier (gold) scales up (*i.e.* amplifies) that shaped signal to an appropriate amplitude, creating  $I_{CORRECTION}$ . The current amplifier replicates (*i.e.* mirrors) and amplifies  $I_{CONTROL}$  (red arrow) to form  $I_{CORRECTION}$  (gold arrow), which is pulled from the primary biasing circuit (purple). This replication of current is referred to as a “current mirror” as discussed in the State of the Art section. EX-1001 10:62-11:45, Figs 4-5; EX-1003 ¶48; *see also* §IV.F.2.



EX-1001 Fig. 5 (annotated).

In sum, in operation, the enable signal (pink arrow) is activated when the PA is enabled, switching from off to on. The time-dependent signal generator, in response, takes that flat “enable” signal and generates a shaped  $I_{CONTROL}$  (red arrow) that is received by the current amplifier (gold). The current amplifier (gold) scales up (amplifies)  $I_{CONTROL}$  (red arrow) to form  $I_{CORRECTION}$  (gold arrow). The primary biasing circuit (purple) receives the shaped  $I_{CORRECTION}$  and correspondingly adjusts the magnitude of the  $I_{BIAS}$  (purple arrow) to compensate for a variation in gain of the PA during startup. The short-term “boost” in  $I_{BIAS}$  helps overcome the PA’s low gain during startup, correcting for that gain variation of the PA. EX-1001 9:13-36; 9:47-56; EX-1003 ¶49.

Figure 6 (below) is a graph of the collector current (of the PA transistor) versus time, where time zero is when the PA is enabled and where plots 101 through 105 correspond to different battery voltage values. The time-dependent signal generator generates  $I_{CONTROL}$  to adjust the PA’s  $I_{BIAS}$  so that the PA’s gain reaches steady state after about  $8\mu\text{s}$ . EX-1001 12:29-47; EX-1003 ¶50.



**FIG.6**

EX-1001 Fig. 6 (annotated).

### **B. Prosecution History of the '101 Patent**

The '101 Patent arose out of application 13/468,749, filed May 10, 2012, 2016. EX-1001 (21-22). During examination, the Patent Office rejected the independent claims over prior art, but indicated that the dependent claims that recited a “current mirror” were allowable. EX-1002 88-90. To overcome the rejection, the Applicant amended the independent claims to recite that the current amplifier included a “current mirror.” The amendment to Claim 1 is representative:

1. (Currently Amended) A power amplifier system comprising:  
a power amplifier configured to amplify a radio frequency (RF) signal; and  
a bias block for biasing the power amplifier, the bias block including a time-dependent signal generator configured to shape an enable signal of the power amplifier to generate a control current, a current amplifier configured to amplify the control current to generate a correction current, and a primary biasing circuit configured to generate a bias current for the power amplifier based at least partly on the correction current, the bias current configured to correct for a variation in gain of the power amplifier when the power amplifier is enabled, the current amplifier including a current mirror.

EX-1002 0099. In response, the Examiner allowed the independent claims, asserting:

Claims 1-3, 6-7, 9-14 are allowed over the prior art of record. The prior art of record considered individually or in combination, fails to fairly teach or suggest the claimed circuit comprising, among other limitations and unobvious limitations of “...the current amplifier including a current mirror” structurally and functionally interconnected with other limitations in the manner as cited in the claim.

EX-1002 0124. However, as shown by this Petition, creating a boost in bias current to compensate for the gain variation of a PA at startup, including using a current amplifier including a current mirror, was already known.

**C. Priority Date of the Challenged Claims**

The '101 Patent claims priority to May 13, 2011. EX-1001 (60) (provisional application 61/486,186, filed on May 13, 2011). This Petition assumes that date as the “Priority Date.”

**D. Claim Construction**

Petitioner proposes that each claim term in the Challenged Claims be given its plain and ordinary meaning in this proceeding, and that no specific construction of any claim term is required because the prior art relied on in this Petition meets each of the claim terms under any reasonable construction. The parties have identified and briefed different constructions of the “plain and ordinary meaning” for various claim terms pending in the Related ITC litigation. *See* EX-1020 2-4; EX-1026; EX-1027; EX-1028. However, neither party contends that the meaning of any claim term deviates from its plain and ordinary meaning due to any lexicography, disclaimer or disavowal in the intrinsic evidence. *Id.* Furthermore, the Grounds in this Petition render the claims unpatentable under either parties’ construction, and thus the Board need not construe any term.

**E. Level of Ordinary Skill in the Art**

A Person of Ordinary Skill in the Art (“POSITA”) in May 2011 would have been someone knowledgeable and familiar with analog and RF circuit design. A POSITA would have gained knowledge of these concepts through a mixture of training and work experience, such as by having at least a Bachelor’s degree in

electrical engineering, or related field, and at least two to three years of training or additional work experience in the area of RF electronics, or a related field. Additional hands-on and design experience could compensate for less formal education, and vice versa, at the time of the priority date of each patent. The knowledge and skill of a POSITA is further reflected in the prior art references themselves, as well as the State of the Art, discussed below. EX-1003 ¶53.

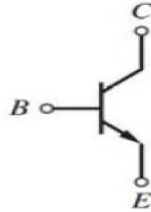
#### **F. State of the Art**

This section describes the state of the art as of the Priority Date. This section, and the expert testimony and documentary evidence cited, provide additional factual support for the general knowledge, common understanding and skill of a POSITA at the Priority Date. This section provides additional factual support and motivation to modify and combine the teachings in the references, and further demonstrates why doing so would involve a reasonable expectation of success. EX-1003 ¶54.

##### **1. The Gain Variation of Power Amplifier at Startup Was Known**

A POSITA in May 2011 understood that a PA was commonly implemented using one or more transistors (such as a bipolar junction transistor (BJT)) to amplify an RF signal. EX-1008(*Johnson*)1605 (“bipolar transistors have evolved as the preferred choice” for wireless PAs due to “higher gain and current density at the frequencies employed”). EX-1003 ¶¶55-58. A BJT transistor has three terminals,

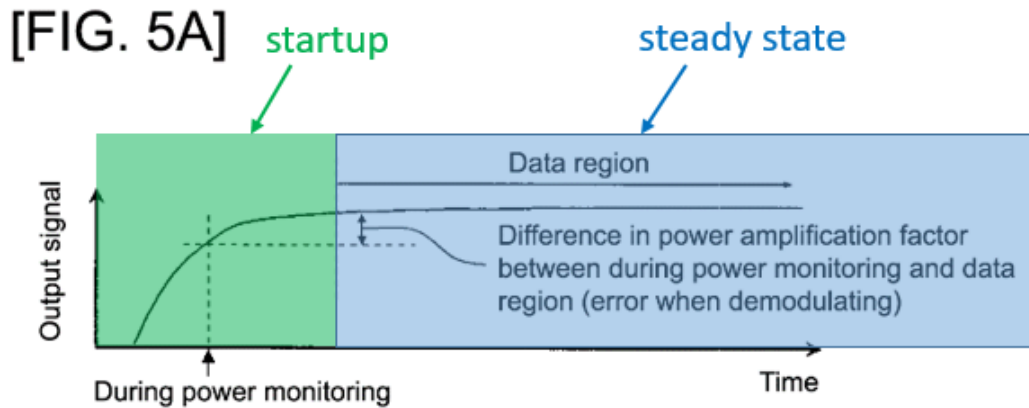
“collector”, “base” and “emitter” as labelled, “C”, “B”, and “E”, respectively, in the figure below.



EX-1013(*Gray*) 92. The biasing and operation of such transistors to amplify a signal applied to the base of the transistor was well known. EX-1024(*Horowitz*) 222-228; EX-1006 47-50, 52-55; EX-1015 38; EX-1003 ¶55.

A POSITA in May 2011 was well aware that the gain response of a PA “varies with temperature” and that “at temperatures below the [PA’s] steady-state operating temperature,” the gain of a PA will be lower than it would be at the steady-state operating temperature (assuming the same bias signal). EX-1010 ¶¶5-6. It was known that, as the PA warms up, the gain of the PA approaches its steady-state expected value. A POSITA was thus aware that “at temperatures below the steady-state operating temperature, the standard bias level is insufficient to achieve the target operating response.” EX-1010 ¶6. This problem existed in conditions where “the PA’s temperature fluctuates between idle temperatures and its steady-state operating temperature” and this fluctuation “causes variations in the gain and phase of the PA away from the target operating response.” EX-1010 ¶8; EX-1003 ¶56.

Further, it was known that a PA was conventionally operated in bursts, turning it on just before, and off just after, transmission of a signal, “in order to suppress power consumption” when not in use. EX-1018 ¶4; EX-1003 ¶57. Consistent with EX-1010 discussed above, it was well known that the gain (or “power amplification factor”) of the PA is lower at startup (green) than at steady state (blue), as shown below:



EX-1018 Fig. 5A (annotated), ¶6.

A POSITA also knew that this issue of the PA gain being too low on startup could be addressed using resistor-capacitor based “speedup” circuits to provide a temporary boost to the  $I_{BIAS}$  supplied to a PA. For example, *Doherty* described that a “common approach” to avoid “unwanted ... gain variations” in the PA was to “speed up the gain ... response of the PA by applying an external resistor and speed-up capacitor to provide more forward [bias] current earlier to the PA.” EX-1010 ¶9. Likewise, *Akagi* described that in “the conventional high-frequency power

amplifier”, a resistor and capacitor circuit (EX-1018 Fig. 4, R1, C1) is generally used so that “immediately after the DC power source E1 is turned on, an instantaneous current flows into the bias circuit” to cause the PA’s “bias point” to be “set to be high, and the power amplification factor becomes high” to provide “power amplification factor correction” to compensate for the thermal properties of the PA. EX-1018 ¶7, Fig. 4. Thus, a POSITA had a well-developed understanding of using time-dependent current generation, including RC speedup circuits, to adapt a PA biasing circuit to boost a PA’s  $I_{BIAS}$  in the period just after enablement of the PA. EX-1003 ¶58.

## 2. Current Mirrors Were Widely Known

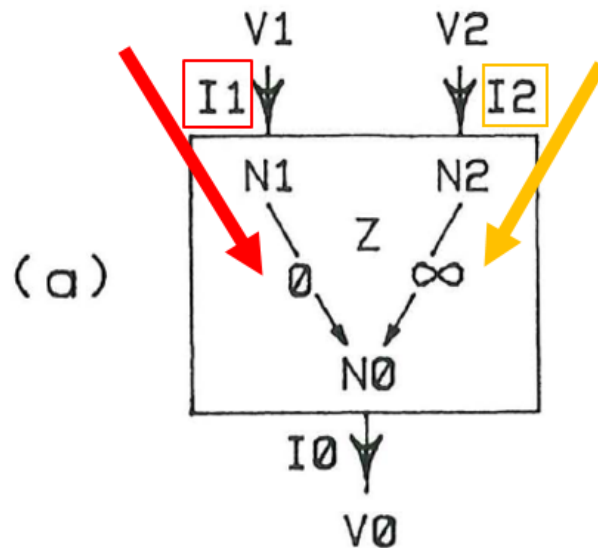
Current mirrors were likewise commonplace and formed part of the general knowledge in the art long before May 2011. EX-1003 ¶¶59-77. As discussed further below, a POSITA was well versed in their multiple and various structures, from single-transistor mirrors, to complicated, multi-transistor designs. A POSITA understood how to use and include current mirrors in analog circuit designs, including RF PAs and their biasing circuits. Their behavior and benefits were predictable and well documented. They were pervasive in the literature. EX-1003 ¶59.

Barrie Gilbert started his textbook chapter on “Bipolar Current Mirrors” by observing that “[f]ew readers of this book will need to be introduced to the concept

of the current mirror; it has become a familiar icon of modern analog design.” EX-1012 239. They were “widely used in analog integrated circuits [] as biasing elements.” EX-1013(*Gray*) 251. Indeed, current mirrors were considered “particularly useful building blocks for analog circuit design” because “they provide a means of establishing the DC bias levels within the circuit.” EX-1014(*Grebene*) 170. Using current mirrors in biasing had advantages including “superior insensitivity of circuit performance to variations in power supply and temperature.” EX-1013 251; EX-1003 ¶¶60-62.

As its name suggests, a current mirror is a circuit that “replicates” (in the sense of “reproduces”, “reflects”, “replicates”, “duplicates” *etc.*)—*i.e.* “mirrors”—an input current as its output current. EX-1014 170 (“the reference current” is “**reproduced or reflected**” and “because of this property” are “known as *current mirror* circuits.”); EX-1012 240 (“an output node ... into which a **replication**” of “the input current flows in the same direction”); EX-1013 251 (“[T]he input current is **reflected** to the output, **leading to the name *current mirror*.**”); EX-1006 70-71 (“*current mirrors* (aka current reflectors), where an input current is mirrored at the output, in either a matched 1:1 or other ratio.”). EX-1003 ¶61.

*Gilbert* begins by describing the “generalized form” of a current mirror.<sup>2</sup> He described the “simplest current mirror” was a three node device, with “an input node, N1, capable of accepting a current  $I_1$ ” (red arrow) of “only one polarity, an output node, N2, into which a **replication**  $I_2$ ” (gold arrow) of “the input current flows in the same direction, and a common node, N0, in which the sum of the input and output currents flow.” EX-1012 240; EX-1003 ¶63.



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<sup>2</sup> Barrie Gilbert was one of the pre-eminent industry leaders in analog circuit design. EX-1021 (“Barrie was likely the most famous analog circuit designer in the world.”). He was featured, for example, on “the cover of the Fall 2007 IEEE Solid-State Circuits Society News issue and virtually the entire issue devoted to him.” EX-1021 (IEEE cover page titled “The Gears of Genius: Barrie Gilbert and Analog Circuits”). EX-1003 ¶62.

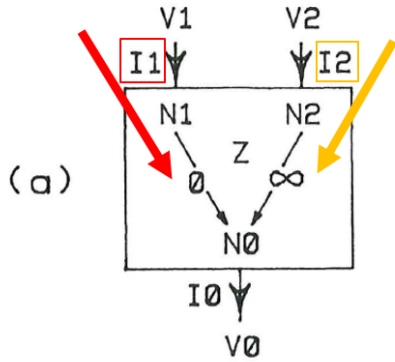
EX-1012 240, Fig. 6.1a (annotated); *accord* EX-1013 Fig. 4.1a.

In such current mirrors, the replicated current ( $I_2$ , gold arrow above) is pulled into the mirror, and is thus called a “current sink.” This arrangement is referred to as a “positive” current mirror. EX-1012 330; EX-1013 Fig. 4.1; EX-1003 ¶¶64-65.

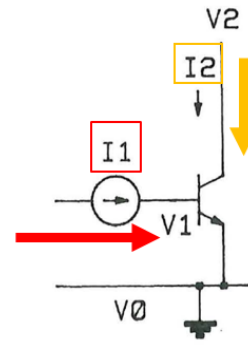
This ability of a current mirror to take an input current that is acting as a current source (*red*), and then replicate that same current *i.e. mirror* it, to create a current *sink* at the output node of the mirror, was well known to a POSITA. This was a common reason to include a current mirror in a circuit, *i.e.*, when one needed to couple a current source from one circuit as a current sink pulling a replicated amount of current from another circuit. EX-1003 ¶66.

#### Single Transistor Current Mirrors

Current mirrors were known to come in many forms. For example, it was well known to use a single transistor to take, *e.g.*, a current source as an input current, and then replicate (*mirror*) it to an output terminal of the transistor as, *e.g.*, a current sink. For example, *Gilbert* provides a section on “One-transistor Mirrors”, describing how to arrange a single BJT transistor as a current mirror. EX-1003 ¶67.



*Gilbert, 240, Fig. 6.1a (annotated)*

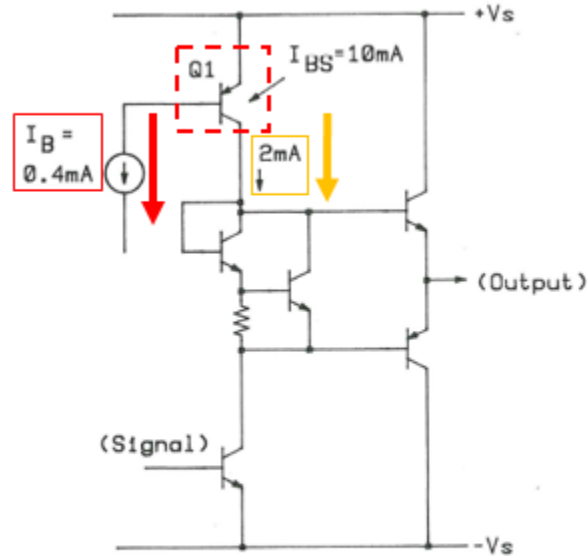


*Gilbert, 243, Fig. 6.2a (annotated)*

*Gilbert* explained that “[i]n the simplest possible scenario, a single BJT can be used as a mirror.” EX-1012 242 (section titled “One-transistor Mirrors”). With reference to the transistor in Fig. 6.2 (above), *Gilbert* explained that node N1 (of the general current mirror form shown in Figure 6.1a) is the base of the transistor in Fig. 6.2a (*i.e.* the input of the current mirror), and likewise, N2 is the collector (*i.e.* the output of the current mirror), and N0 the emitter (*i.e.* the common node of the current mirror). EX-1012 242; EX-1003 ¶68.

While “not very linear” and “poorly-controlled” compared to other current mirrors, the “mirror ratio,  $M$ ” of the single BJT mirror is the “common-emitter current-gain,  $\beta$ ”. EX-1012 242. The output is scaled by the amplification factor of the BJT, namely the common-emitter current-gain,  $\beta$ . That is because in a BJT biased into its active region, the collector current ( $I_C$ ) and base current ( $I_B$ ) are generally related by the equation:  $I_C = I_B * \beta$ . EX-1015 38; EX-1012 242-243; EX-1003 ¶69.

Similarly, in the following example, *Gilbert* shows and describes a single transistor current mirror, “Q1”, to bias “an operational amplifier”. EX-1003 ¶70.



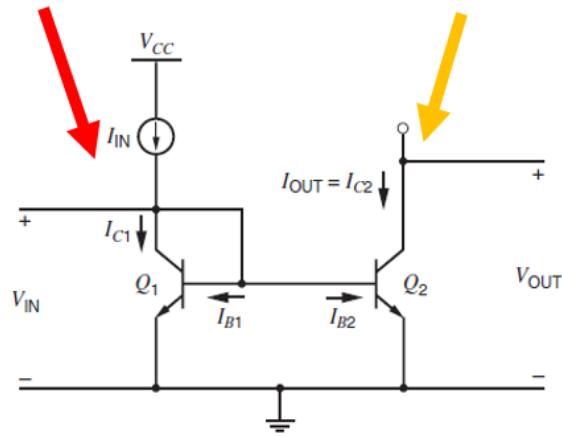
*Gilbert*, Fig. 6.4 (annotated)

EX-1012 Fig. 6.4 (annotated).

*Gilbert* described the transistor Q1 in the above figure as a “simple open-base PNP **current mirror**”, “used to bias an [operational amplifier] ... with improved efficiency.” EX-1012 248; EX-1003 ¶71.

### Two-Transistor Current Mirrors

Long before May 2011, undergraduate electrical engineering students were likewise conversant with the basic two-transistor current mirror form. EX-1013 253, Fig. 4.2; EX-1012 251, Fig. 6.7a. For example, a “simple bipolar current mirror” is shown in the annotated Figure 4.2 below, with the input current annotated in red and the mirrored output current in yellow. EX-1003 ¶72.



EX-1013 253, Fig. 4.2.

This two-transistor current mirror format was a heavily documented, staple of analog circuit design having highly predictable behaviors and advantages, readily known to undergraduate level students. EX-1003 ¶73.

Although a POSITA knew of simple single and two transistor current mirror designs, a POSITA also knew that “current mirrors” were not limited to any one configuration or arrangement. More advanced, multi-transistor structures were likewise known for mirroring an input current to an output current, with various connections between the gates of the mirrors. EX-1012 261, Fig. 6.12b, 276-77, Fig. 6.25b; EX-1012 292, Fig. 6.42c; EX-1003 ¶¶74-75.

One well-known benefit of current mirrors was that they could be configured to provide a desired current amplification when mirroring the current, such that the “output current is equal to the input current multiplied by a desired current gain.” EX-1013 251. It was well known that one could advantageously set the gain by

controlling the size of the transistors involved. EX-1013 254, 257. In the case of bipolar transistors, this was done by scaling emitter area. EX-1012 280; EX-1014 172; EX-1003 ¶76.

Thus, there was a robust state of the art in current mirrors at the time of the purported invention. A POSITA knew how to design and implement a wide variety of mirror circuits, from single transistor to complicated multi-transistor circuits, all achieving well understood, predictable behavior in replicating, *i.e.*, mirroring an input current to an output current. EX-1003 ¶77.

### **3. BJT Power Amplifiers Were Commonly Implemented Using Heterojunction Bipolar Transistors (HBTs)**

By May 2011, it was well known to implement PAs using bipolar junction transistors (BJT). *Supra* §IV.F.1; EX-1008(*Johnson*) 1605 (explaining that “bipolar transistors have evolved as the preferred choice” for wireless PAs due to “higher gain and current density at the frequencies employed”). EX-1003 ¶¶78-80. Furthermore, it was well-known, general knowledge in the art that a high performing type of BJT for RF PAs was a BJT with a wide band gap emitter, known as a Heterojunction Bipolar Transistor (HBT). *See, e.g.*, EX-1015 259 (defining HBT, including, *e.g.*, “A bipolar junction transistor that incorporates a wide band gap emitter” with the result of reduced base resistance, “maximizing the desired injection of carriers from emitter to base.... HBTs are used at radio- and microwave frequencies, in integrated circuit and power applications”). HBTs were known to be

specifically adapted for high performance to meet the demands of RF power amplification applications. *See, e.g.*, EX-1015 259 (describing that the HBT properties “leads to **an improvement in the high-frequency performance** of the transistor. **HBTs are used at radio- and microwave frequencies**, in integrated circuit and power applications, and in optoelectronic ICs.”). In fact, HBTs were the dominant, market leading form for RF PAs implemented with BJTs, with well-documented advantages known to a POSITA. EX-1017(*TriQuint*) 1 (“RF medium and high **power amplifiers realized with HBT technology are increasingly popular in telecommunications systems** due to the **inherently superior linearity and efficiency performance** compared to competing technologies. The **reliability of HBT RF devices is well known to be excellent** from Highly Accelerated Stress Testing (HAST) and High Temperature Operating Lifetime (HTOL) testing.”); EX-1025(*YanJun*) 1 (“In past years, **HBT PAs have dominated the medium power transmitter market due to their excellent linearity and PAE.**”); EX-1008 1605 (explaining advantages including “provid[ing] high integration and [] reduce[d] cost,” reduced chip area and increased chip robustness, temperature insensitive current gain, and well characterized reliability at high current densities enabling further reduction in device size). EX-1003 ¶78.

It was known that HBTs came in a variety of advantageous forms, including Gallium Arsenide (GaAs) and Silicon Germanium (SiGe). EX-1015 259. For

example, SiGe HBTs found “increasing use in wireless PA applications” due to “favorable thermal properties,” “volume manufacturing capability,” and “design automation support,” which had all “long been recognized.” EX-1008 1612. Such HBTs had “favorable device ruggedness for PA applications.” *Id.* HBT PA designs had been demonstrated to meet the needs of a range of wireless standards, including the robustness required at the high speed, output power and linearity called for by the GSM, GPRS, and EDGE wireless standards. *Id.* It was known that the “favorable thermal properties, lower cost of wafer processing, and the higher integration capabilities” of such HBTs “make them a compelling choice for wireless applications” and provide a “very strong path for PA modules.” *Id.*; EX-1003 ¶79.

Thus, the use of BJT transistors to form a PA, including the HBT form of BJTs and their advantages, formed part of the general knowledge in the art before the invention. EX-1003 ¶80.

## V. IDENTIFICATION OF HOW THE CLAIMS ARE UNPATENTABLE

### A. Challenged Claims

This Petition challenges claims 1, 2, 10-11, 17, 18, 20, 21, and 22 of the '101 Patent.

### B. Statutory Grounds for Challenges

Grounds	Claims	Basis	References
Ground 1	1, 2, 10-11, 17, 18, 20, 21, and 22	§103	<i>Ishimaru</i>

Grounds	Claims	Basis	References
Ground 2	1, 2, 10-11, 17, 18, 20, 21, and 22	§103	<i>Ishimaru</i> in view of <i>Harrison</i>

U.S. Patent Publication 2009/0212863 to *Ishimaru* (EX-1004, “*Ishimaru*”) was filed on February 13, 2009, published on August 27, 2009, and is prior art to the ’101 Patent under at least pre-AIA 35 U.S.C. §102(b).

“Current Sources & Voltage References” was authored by Linden T. Harrison (“*Harrison*”) and published by Elsevier Inc. in 2005. EX-1006 2; EX-1016 (Munford Declaration) ¶19. *Harrison* is prior art to the ’101 Patent under at least pre-AIA 35 U.S.C. §102(b), and was publicly available before the earliest priority date for the ’101 Patent. EX-1016 ¶¶8-19.

**C. Ground 1: Claims 1-2, 10-11, 17-18, and 20-22 Are Obvious over *Ishimaru***

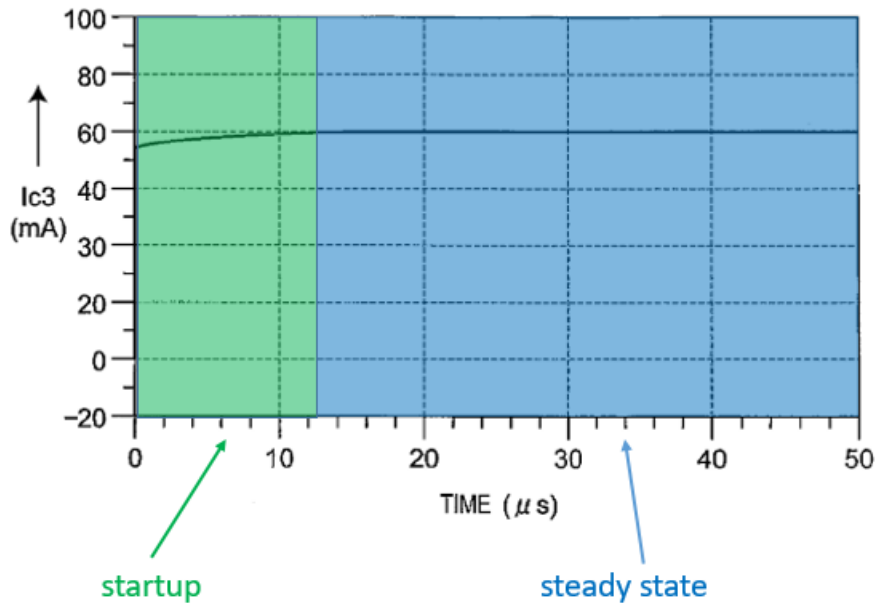
**1. *Ishimaru***

*Ishimaru* is titled “Power Amplifier” and relates to “a high frequency power amplifier to be used in radio communication devices or the like.” EX-1004 Abstract, ¶1. *Ishimaru* explains that PAs in communication systems such as those using “Orthogonal Frequency Division Multiplex[ing]” have “such a circuit design for linearization that the system runs on a linear amplification range of enough smaller outputs than a maximum output of the power amplifier” so that the output RF signal “is not distorted in the power amplifier.” *Id.* ¶2. *Ishimaru* further explains that

“linear amplification” “means that even with input signal power changed, the output signal power is amplified at a constant ratio for output while the phase keeps unchanged.” Further, *Ishimaru* explains that in some communication systems, “slight changes of amplification gain as small as 0.2 to 0.3 dB may matter,” *i.e.*, affect a communication link. *Id.* ¶3. A POSITA would thus understand that *Ishimaru* is from the same field of art as the ’101 Patent because it relates to the field of RF electronics generally, PAs specifically, and controlling/compensating gain in particular. EX-1003 ¶83.

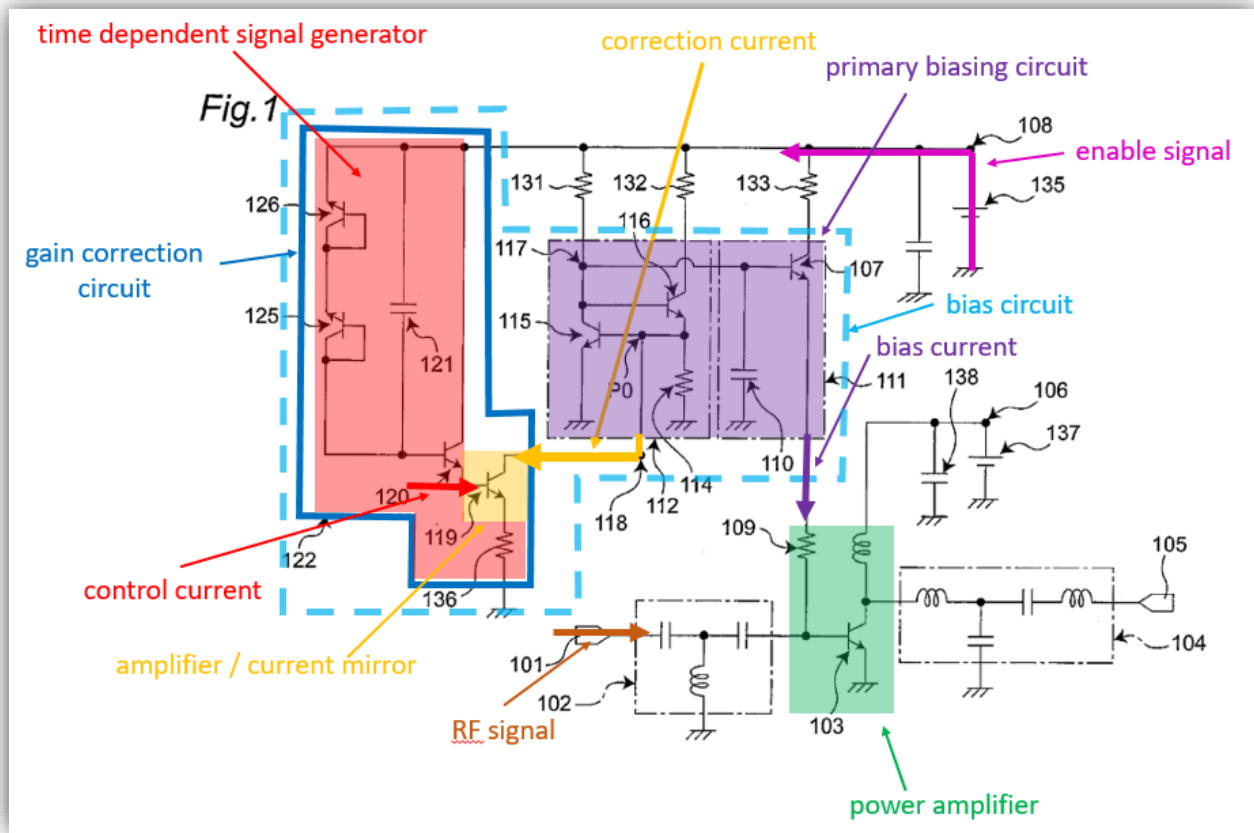
*Ishimaru* explains that thermal changes that occur slowly during startup can last for “tens to several hundreds of microseconds” and affect the “amplification ratio” of the PA during that time. EX-1004 ¶4; EX-1003 ¶84. In an example of such gain variation of the PA at startup, *Ishimaru* showed how collector current of the PA comes up slowly (~10 us in this example):

Fig.2 PRIOR ART



EX-1004 Fig. 2 (annotated).

*Ishimaru's* solution, shown in Figure 1 below, was a PA and bias circuit that included a “speedup circuit” that “transiently (temporarily) increases” the  $I_{BIAS}$  fed to the amplifier transistor by the bias circuit during the period after startup. EX-1004 ¶13. Speedup circuit 122 includes transistors 119, 120, resistance element 136, as well as a capacitance element 121 connected between the base of transistor 120 and bias terminal 108. *Id.* ¶50-51; EX-1003 ¶85.



EX-1004 Fig. 1 (annotated).

Figure 1 shows an input signal terminal 101 that receives a high-frequency signal (brown arrow) as an input signal, and this input signal passes through an input matching circuit 102, and is then amplified by amplifier transistor 103 (green). The amplifier transistor 103 outputs a signal through output matching circuit 104 to output signal terminal 105. Figure 1 also depicts a bias circuit 111 and a bias power source section 112, which together constitute a bias power source section (purple), and a speedup circuit 122 (dark blue). EX-1004 ¶¶43, 46, 49; EX-1003 ¶86.

Bias circuit 111 includes a bias transistor 107 and capacitance element 110, where a collector of the bias transistor is connected to a bias terminal 108, which is

in turn connected to a control voltage source 135. EX-1004 ¶44. The emitter of the bias transistor 107 is connected to the base of the amplifier transistor 103, and “supplies a base bias current” (purple arrow) to the base of the amplifier transistor (green). *Id.* ¶43. Power source circuit 112 is connected to the base of the bias transistor 107. *Id.* ¶46. Power source circuit 112 has a connecting point P0, which is connected to an output terminal 118 of a speedup circuit 122. *Id.* ¶49; EX-1003 ¶87.

The circuit used “capacitance element 121” “at turn-on of the amplifier” to generate an  $I_{CORRECTION}$  (gold arrow) that “transiently (temporarily) flows” out of the biasing circuit from “output terminal 118.” That causes the voltage on the base of bias transistor 107 to “transiently increase[]”, causing the bias “current fed to the amplifier transistor 103” to likewise “transiently increase[.]” EX-1004 ¶52; EX-1003 ¶88.

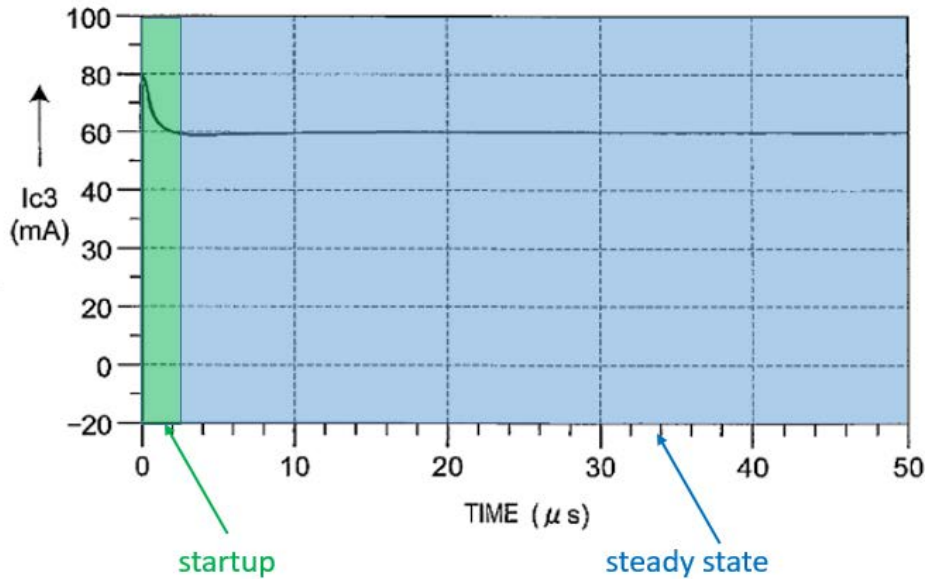
As illustrated in annotated Figure 1, a POSITA understood that the bias circuit (light blue) consists of a conventional “primary bias circuit” 111, 112 (purple) driven by a conventional, unmodified “enable signal” (pink), plus a gain correction circuit (speedup circuit) (dark blue) that generates the  $I_{CORRECTION}$  (gold arrow) to shape the bias current (purple arrow) that emerges from the primary bias circuit. That  $I_{CORRECTION}$  is generated by the gain correction circuit using a time-dependent signal generator (red) to generate a small  $I_{CONTROL}$  (red arrow) with the desired shape, and

then scaling up that shaped signal to an appropriate amplitude using a “current amplifier” (gold). The current amplifier replicates (*i.e.* mirrors) and amplifies  $I_{CONTROL}$  (red arrow) to form  $I_{CORRECTION}$  (gold arrow), which is pulled from the primary biasing circuit (purple). EX-1003 ¶89.

*Ishimaru* explains that, at a rise time of control voltage source 135 (which is input to bias terminal 108 and is the enable signal), “with electric charge flowing into the capacitance element 121” “a current transiently (temporarily) flows from the output terminal 118 into the fifth transistor 119, causing the voltage value of the output terminal 118 to lower.” EX-1004 ¶52. The  $I_{BIAS}$  (purple arrow) fed “to the amplifier transistor 103 is forcedly increased at turn-on of the amplifier.” *Id.* ¶54. This means that “at the rise time, the current fed to the amplifier transistor 103 by the bias transistor 107 transiently increases.” *Id.* ¶52; EX-1003 ¶90.

Accordingly, to compensate for the startup phenomenon shown in Figure 2 (above), *Ishimaru* disclosed simulation results of the transient boost in PA collector current at PA startup. EX-1004 ¶54, Fig. 3; EX-1003 ¶91.

Fig.3



EX-1004 Fig. 3 (annotated).

*Ishimaru* taught that the forced transient boost in current corrected for the startup gain variation of the PA:

Therefore, at the rise time, **the power amplification factor of the amplifier transistor 103 transiently increases**, so that the **time elapsing until temperature variations** due to heat generation of the amplifier transistor 103 **come to an equilibrium** on the whole circuit **is shortened**, with a result of **reduced distortion of the amplification signal** (e.g., modulated wave signal).

EX-1004 ¶52.

Thus, occurrence of **distortions of the amplification signal due to temperature variations in the amplifier circuit is suppressed**, so that the **linearity** of the circuit in burst operation **is improved**. That is, **gain variations** due to collector current variations **of the power amplifier**

using a bipolar transistor **can be compensated**.

EX-1004 ¶54. EX-1003 ¶92.

## 2. Detailed Application of *Ishimaru* to the Challenged Claims

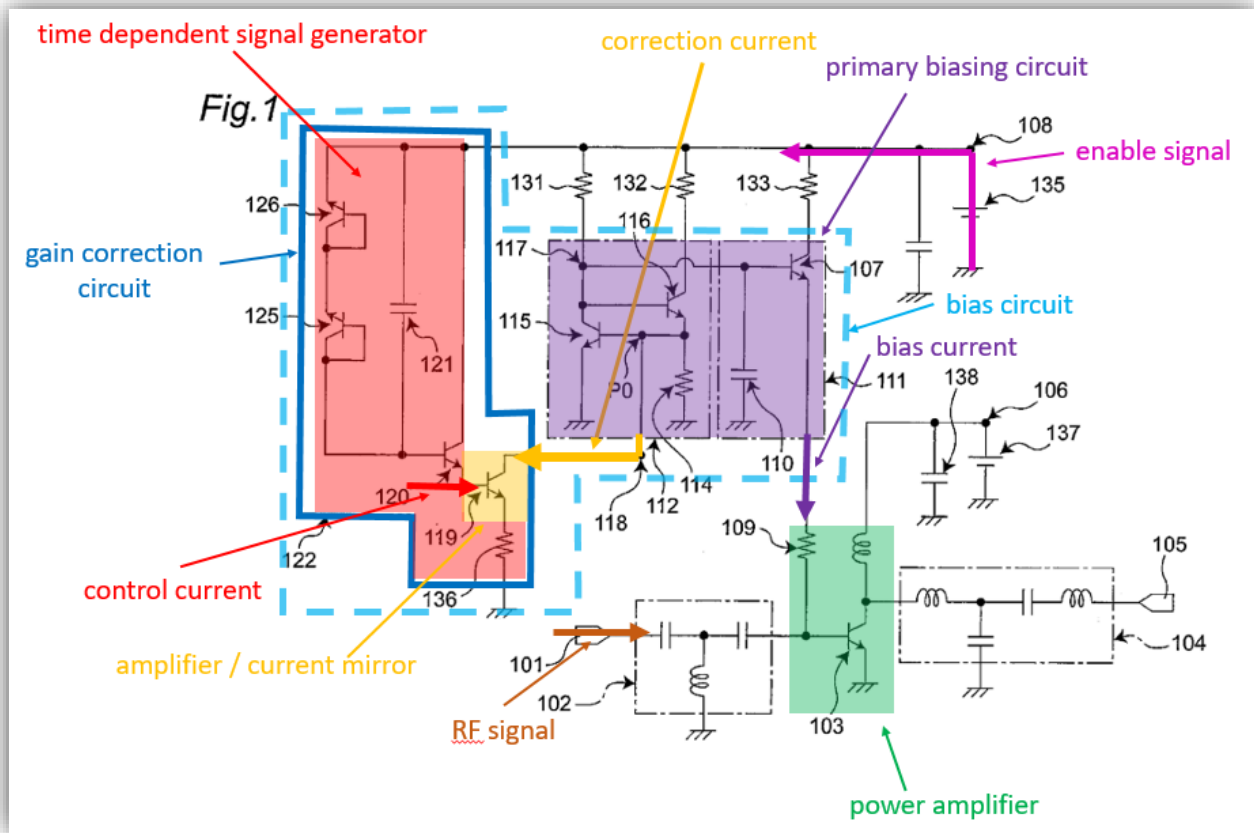
### Claim 1

#### ***[1.0] A power amplifier system comprising:***

To the extent that the preamble is limiting, the bias and PA circuitry in *Ishimaru*'s Figure 1 is a power amplifier system for “a high-frequency power amplifier to be used in radio communication devices.” EX-1004 ¶¶1, 41, Fig. 1. The circuitry for the PA system includes “an amplification section having a first transistor for performing power amplification”, as well as “a bias power source section”, “bias circuit,” and “a speedup circuit.” EX-1004 Abstract, ¶¶10-12, Fig. 1 (annotated below); EX-1003 ¶¶93-137.

#### ***[1.1] a power amplifier configured to amplify a radio frequency (RF) signal; and***

*Ishimaru* discloses this limitation. EX-1003 ¶¶94-96. *Ishimaru* discloses a power amplifier configured to amplify a radio frequency RF signal (green) in radio communications devices. EX-1004 ¶¶1, 41, Fig. 1; EX-1003 ¶94.



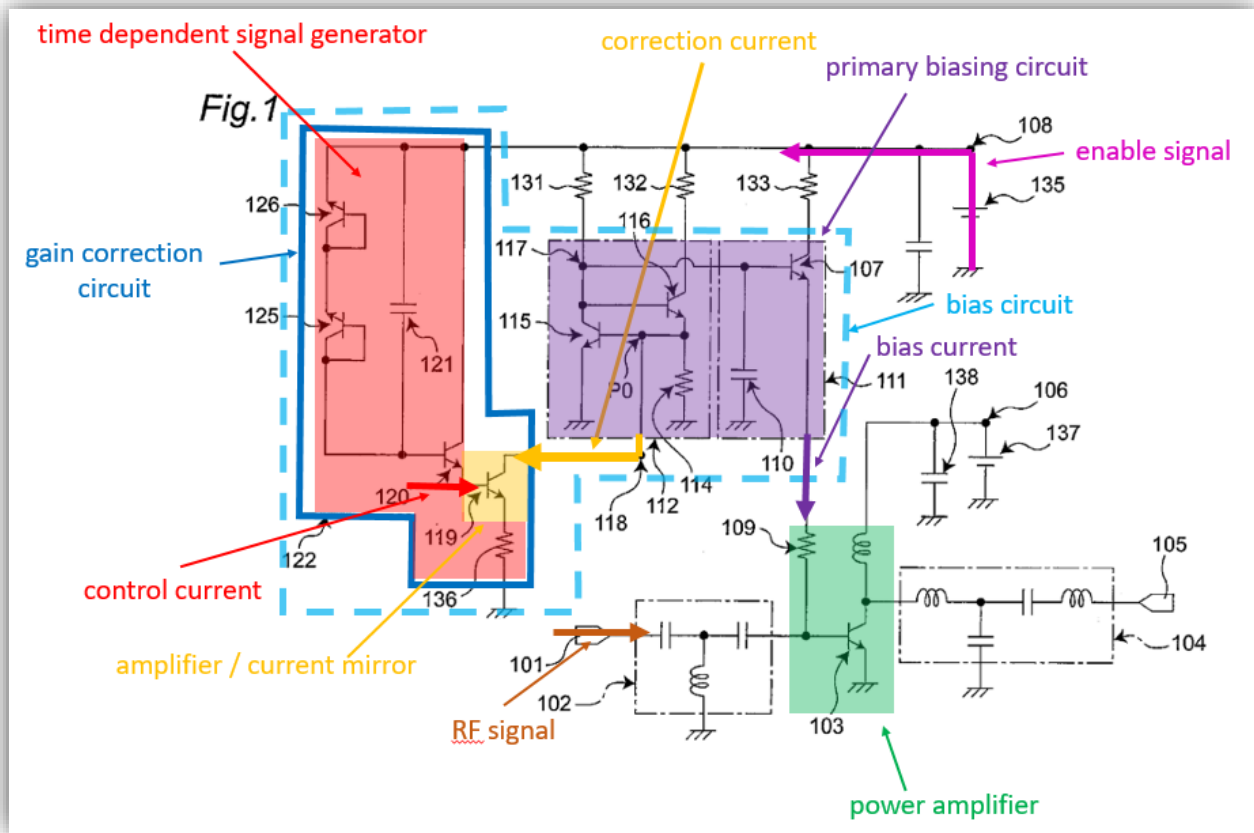
EX-1004 Fig. 1 (annotated).

*Ishimaru* discloses “a high-frequency power amplifier to be used in radio communication devices.” EX-1004 ¶1. The circuitry for the PA includes “an amplification section having a first transistor for performing power amplification” (green) (*a power amplifier*). EX-1004 ¶¶10-12. As illustrated in Figure 1 (annotated below), *Ishimaru* further discloses that “a high-frequency signal as an input signal [is] inputted from an input signal terminal 101, ... is amplified by an amplifier transistor 103 serving as a first transistor, and then, ... outputted from an output signal terminal 105” (*power amplifier configured to amplify*). EX-1004 ¶42; EX-1003 ¶95.

Specifically, because *Ishimaru* is directed to a PA for a **radio** communications device, a POSITA reading *Ishimaru* understood that the high-frequency input signal at input terminal 101 is a *radio frequency (RF) signal* (brown arrow) for amplification by amplifier transistor 103 (*a power amplifier configured to provide amplification*) to generate an amplified radio frequency signal at output terminal 105; EX-1003 ¶96.

***[1.2] a bias block for biasing the power amplifier, the bias block including***

*Ishimaru* discloses this limitation. EX-1003 ¶97. As shown in Figure 1, *Ishimaru* discloses a “speedup circuit 122,” “power source circuit 112,” and “bias circuit 111” (collectively, *a bias block*) (light blue) that receives a control voltage from voltage source 135 (enable signal) (pink arrow) and supplies a “base bias current” ( $I_{BIAS}$ ) (purple arrow) to the base terminal of amplifier transistor 103 (*biasing the power amplifier*) (green). EX-1004 Abstract, ¶¶24, 31, 43, 45, 49-52; EX-1003 ¶97.



EX-1004 Fig. 1 (annotated).

**[1.2.1] a time-dependent signal generator configured to shape an enable signal of the power amplifier to generate a control current,**

*Ishimaru* discloses this limitation. EX-1003 ¶¶98-100. *Ishimaru* discloses that the control voltage from control voltage source 135 at bias terminal 108 “controls turn-on and -off of power amplification.” EX-1004 ¶24. Thus, *Ishimaru*’s control voltage is *an enable signal of the power amplifier* (pink) as the PA is only operable when the bias is active and the bias is only active when the terminal 108 is high. EX-1003 ¶98.

With reference to Figure 1, *Ishimaru* discloses a speedup circuit 122 (dark blue) that includes a capacitance element 121, diodes 125 and 126, transistors 119 and 120, and resistance element 136 (*a time-dependent signal generator*) (red). EX-1004 ¶¶50-51. In response to the “rise time of the control voltage of the control voltage source 135 (at turn-on of the amplifier),” (*enable signal*) (pink arrow), the speedup circuit applies a transient or time-varying current to the base of transistor 119, a *control current*,  $I_{CONTROL}$  (red arrow). EX-1004 ¶52. This is a control current at least because it is used to control the correction to the biasing of *Ishimaru*’s PA to compensate for gain variation, as discussed next. EX-1003 ¶99.

*Ishimaru*’s speedup circuit 122 (dark blue) includes a *time dependent signal generator* (red) in that it is a circuit configured to change an enable signal (pink arrow) of the PA to achieve a desired shape of  $I_{CONTROL}$  (red arrow), where the control current changes based on time. The shaping eventually results in the corresponding time-dependent current shown in Figure 3. EX-1004 ¶¶8-12, 52-56, Fig. 3. As explained in more detail below with respect to limitation [1.2.2], the speedup circuit 112 (dark blue) shapes  $I_{CONTROL}$  (red arrow) and amplifies it to form a correction current ( $I_{CORRECTION}$ ) (gold arrow) as a “current that transiently (temporarily) flows” out of the PA’s primary biasing circuit (purple). EX-1004 ¶52; *see* [1.2.2]. The time-dependent shape of the  $I_{CONTROL}$  (red arrow) is thereby used to shape the  $I_{CORRECTION}$  (gold arrow) in an amount and duration necessary to cause the primary

biasing circuit to send a corresponding temporary boost in  $I_{BIAS}$  to the PA (green) to boost its gain during the startup period when its gain would otherwise be too low, *i.e.* to correct for the gain variation of the PA. EX-1004 ¶¶8-12, 52-55, Figs. 2 and 3. The speed up circuit, and its capacitor 121, changes the flat nature of the enable/on signal into a signal that is not just “on”, but instead is made to have a desired time-varying shape for compensating PA gain variation. EX-1004 ¶¶49-52, 55-56; EX-1003 ¶100.

***[1.2.2] a current amplifier configured to amplify the control current to generate a correction current, and***

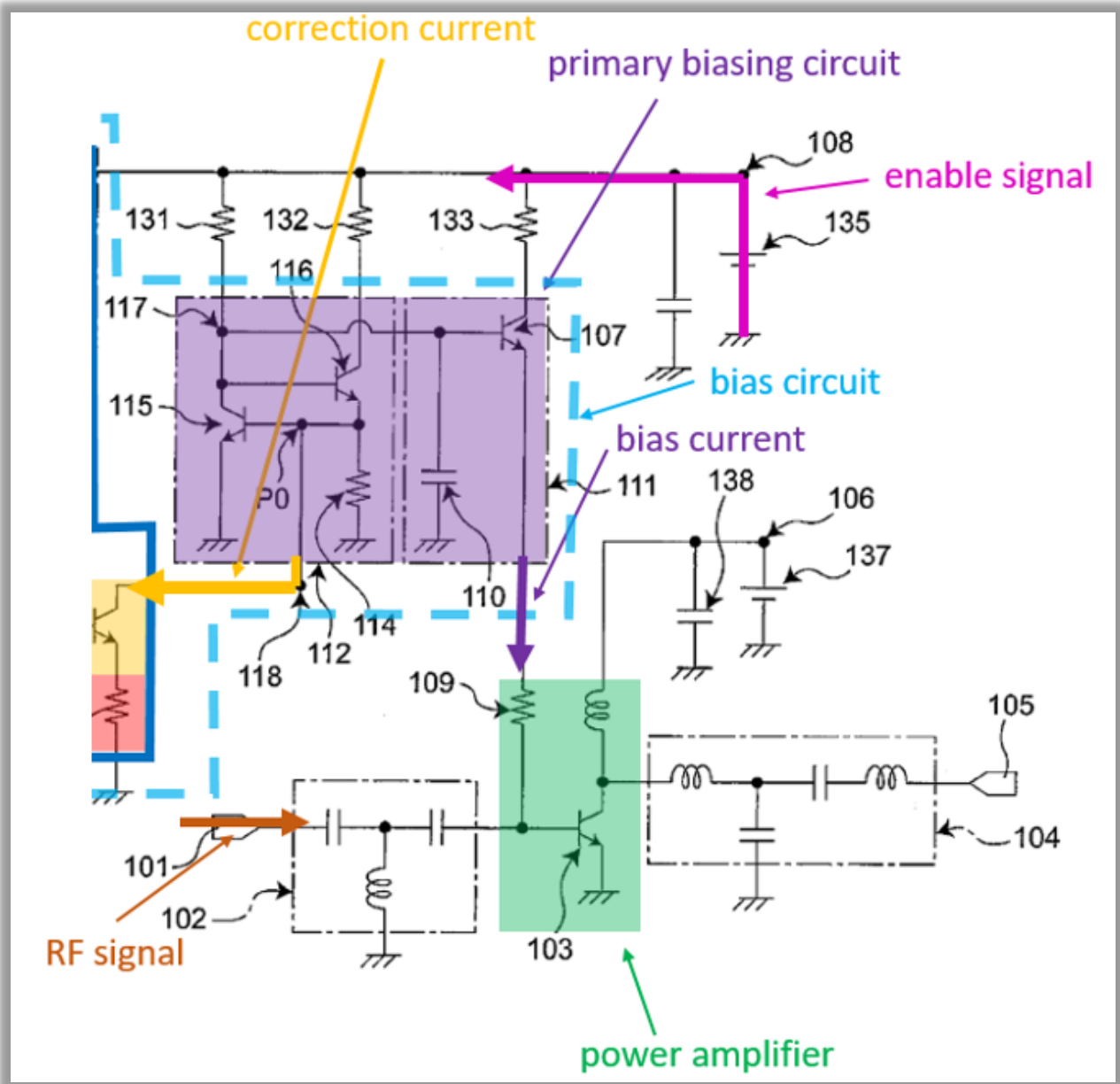
*Ishimaru* discloses this limitation. EX-1003 ¶¶101-102. The  $I_{CONTROL}$  (red arrow) is amplified by transistor 119, (*current amplifier*) (gold) resulting in the transient  $I_{CORRECTION}$  (gold arrow) being pulled into the collector of transistor 119 from node 118. EX-1004 ¶52; *see also* [1.2.1]. EX-1003 ¶101.

A POSITA recognized that transistor 119 amplifies its base current by the beta factor,  $\beta$ , of transistor 119 to provide amplification, *e.g.*, 60 to 150 or higher. EX-1006 53-55; EX-1015 38 (practical  $\beta$  values can be “up to 500”). Thus, transistor 119 is a *current amplifier configured to amplify* the current at its base (red arrow) (*the control current*) to generate the amplified  $I_{CORRECTION}$  at its collector (gold arrow) (*to generate a correction current*).  $I_{CORRECTION}$  (gold arrow) is a “current that transiently (temporarily) flows” out of the PA’s primary biasing circuit (purple). EX-1004 ¶52.  $I_{CORRECTION}$  (gold arrow) is a correction current in that it is shaped in

an amount and duration necessary to cause the primary biasing circuit (discussed below) to send a corresponding temporary boost in  $I_{BIAS}$  (purple arrow) to the PA (green) to boost its gain during the startup period when its gain would otherwise be too low, *i.e.* to correct for the gain variation of the PA. EX-1004 ¶¶8-12, 52, 55, Figs. 2 and 3. *See also, infra*, [1.2.4] (discussing amplifier implemented as a current mirror). EX-1003 ¶102.

***[1.2.3] a primary biasing circuit configured to generate a bias current for the power amplifier based at least partly on the correction current, the bias current configured to correct for a variation in gain of the power amplifier when the power amplifier is enabled,***

*Ishimaru* discloses this limitation. EX-1003 ¶¶103-111. As shown in the portion of Figure 1 reproduced below, *Ishimaru* discloses a power source circuit 112 and bias circuit 111, which constitute *the primary biasing circuit* (purple) which together supply a “base bias current” ( $I_{BIAS}$ , *a bias current for the power amplifier*) (purple arrow) to the amplifier transistor 103. As explained below, this boost in  $I_{BIAS}$  is based on the current drawn out of node 118 ( $I_{CORRECTION}$ , *the correction current*) (gold arrow) when the control voltage is applied (*the power amplifier is enabled*) (pink arrow) to correct for a variation in gain of the PA at startup. EX-1003 ¶103.



EX-1004 Fig. 1 (partial) (annotated).

*Ishimaru* explains that “bias circuit 111 and the power source circuit 112 constitute a bias power source section.” EX-1004 ¶46. The combination of this circuitry is a *primary biasing circuit* in that it is the main circuitry used to generate the  $I_{BIAS}$  that biases the operating point of the transistor of the PA (green) to its

intended state (e.g. *enabled*, and biased to operate at its intended operating point, suitable for amplification). *See, e.g.*, EX-1024 220, 222-228; EX-1006 Fig. 2.1. More specifically, bias circuit 111 is “composed of the bias transistor 107 and a capacitance element 110” connected to the base of bias transistor 107. EX-1004 ¶45. Bias transistor 107’s collector is connected to bias terminal 108 through a resistor 133, and the bias terminal 108 is connected to control voltage source 135 (*enable signal*) (pink arrow). EX-1004 ¶44. The emitter of bias transistor 107 is connected to a base terminal of the amplifier transistor 103 via resistance element 109 and “supplies a base bias current to the base of amplification transistor 103.” EX-1004 ¶43. This “base bias current” ( $I_{BIAS}$ ) is a *bias current*. EX-1003 ¶104.

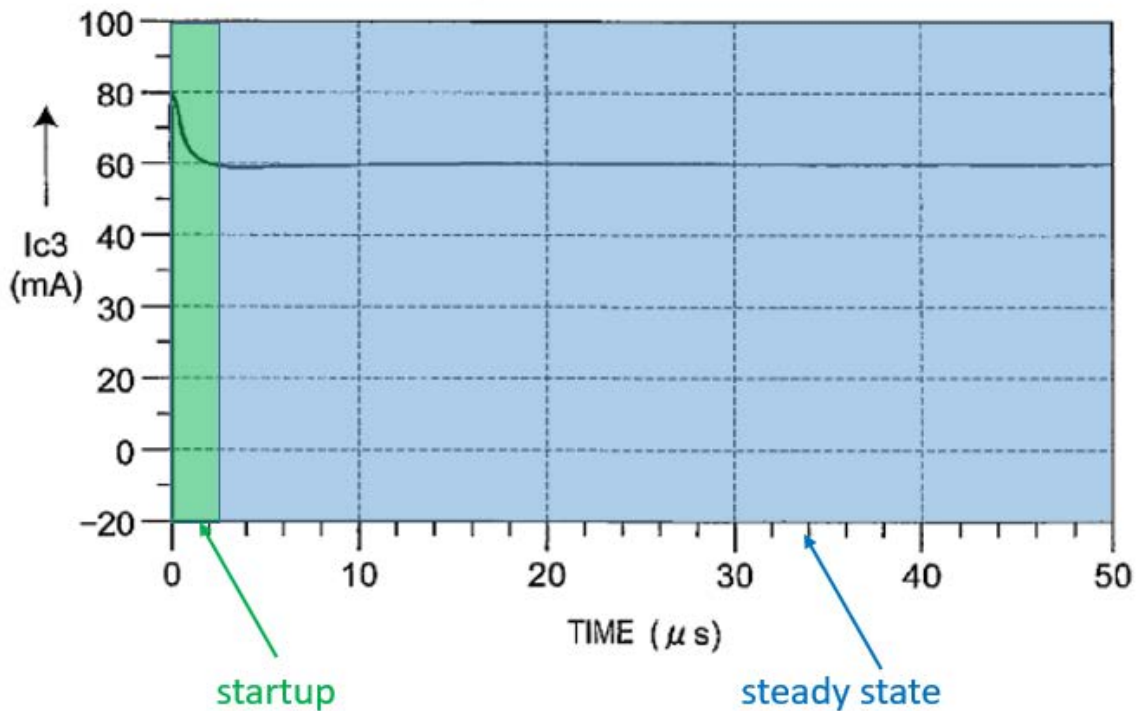
Bias transistor 107 in circuit 111 operates in conjunction with power source circuit 112 to generate  $I_{BIAS}$  that is applied to the amplifier transistor 103 and thus, circuit 111 and 112 collectively are a *primary biasing circuit* (purple). EX-1003 ¶105.

More specifically, as shown in the portion of the annotated Figure 1 above, node 117 of circuit 112 is connected to the base terminal of the bias transistor 107 and, thus, controls the bias point of transistor 107 and, consequently, the transistor 107’s collector current. EX-1004 ¶¶46, 48. Node P0 of power source circuit 112 (*i.e.*, the base of transistor 115 and emitter of transistor 116) is connected to output terminal 118 of speedup circuit 122. *Id.* ¶¶48-49. EX-1003 ¶106.

*Ishimaru* explains that, at a rise time of the control voltage from the control voltage source 135, “a current transiently (temporarily) from the output terminal 118” flows into the speedup circuit 122. EX-1004 ¶52. As explained in [1.2.2] above, this current is  $I_{CORRECTION}$ . EX-1004 ¶52. The transient rise in  $I_{CORRECTION}$  causes the voltage at output terminal 118 to lower, which raises the voltage at the collector of transistor 115 (node 117), which controls the bias transistor 107, and this causes “the current fed to the amplifier transistor by the bias transistor 107” (*the bias signal*) to transiently increase to correct for a variation in gain of the PA when the PA is enabled. EX-1004 ¶52, *see also* ¶¶8-12, 31, 53-55, Figs. 2 and 3; EX-1003 ¶107.

Figure 3, which shows the transient response of the collector current of the amplifier transistor 103, illustrates how the transient rise in  $I_{CORRECTION}$  causes the collector current of the amplifier transistor 103 to temporarily increase during startup to compensate for gain variations due to collector current variations of the PA using a bipolar transistor (*to correct for a variation in gain of the power amplifier when the power amplifier is enabled*). EX-1004 ¶54, Fig. 3; EX-1003 ¶108.

*Fig.3*



EX-1004 Fig. 3 (annotated), contrast Fig. 2, ¶53.

More specifically, the transient rise in  $I_{CORRECTION}$  causes the collector current of the amplifier transistor 103 to temporarily increase during startup *to correct for a variation in gain of the power amplifier when the power amplifier is enabled*:

Thus, occurrence of **distortions of the amplification signal due to temperature variations in the amplifier circuit is suppressed**, so that the **linearity** of the circuit in burst operation **is improved**. That is, **gain variations** due to collector current variations **of the power amplifier** using a bipolar transistor **can be compensated**.

*Id.* ¶54; EX-1003 ¶109.

This transient increase in the collector current of amplifier transistor 103 is due to a transient increase in  $I_{BIAS}$  (*a bias signal*) into amplifier transistor 103 because the collector current amplifies the base bias current via the amplifier transistor 103's amplification factor  $\beta$ . Further, *Ishimaru* explicitly explains that the collector current 103 (also called "operating current  $I_{c3}$ ") "comes to a steady state in about  $\frac{1}{4}$  of the time of transient response of the comparative example of Fig. 2," which is the transient response without speedup circuit 122. EX-1004 ¶¶53-54, Figs. 2 and 3; EX-1003 ¶110.

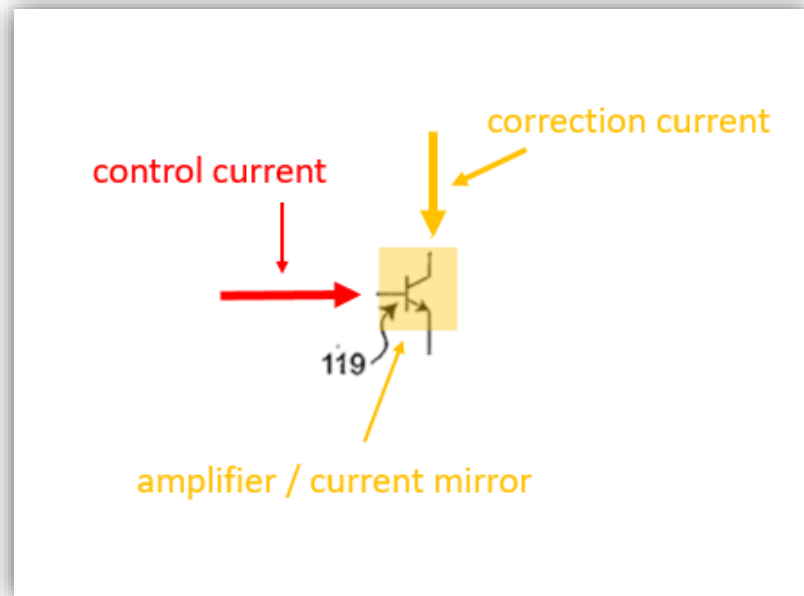
Accordingly, *Ishimaru* discloses a *primary biasing circuit* (purple) configured to generate a *bias current* (purple arrow) for the *power amplifier* (green) based at least partly on the *correction current* (gold arrow), the *bias current configured to correct for a variation in gain of the power amplifier* (purple arrow) at startup (*when the power amplifier is enabled*). EX-1003 ¶111.

**[1.2.4] the current amplifier including a current mirror.**

*Ishimaru*'s transistor 119 is a current amplifier. EX-1003 ¶¶112-117; See [1.2.2]. Like the preferred embodiment of the '101 Patent, a current mirror can constitute the current amplifier. See EX-1001 10:23. As shown in Fig. 1, partially reproduced below, *Ishimaru*'s transistor 119 is a *current amplifier including a current mirror* (gold) in that transistor 119 is configured to replicate (*i.e. mirror*) and

scale (amplify) the  $I_{CONTROL}$  (red arrow) to generate the  $I_{CORRECTION}$  (gold arrow).

EX-1003 ¶112.

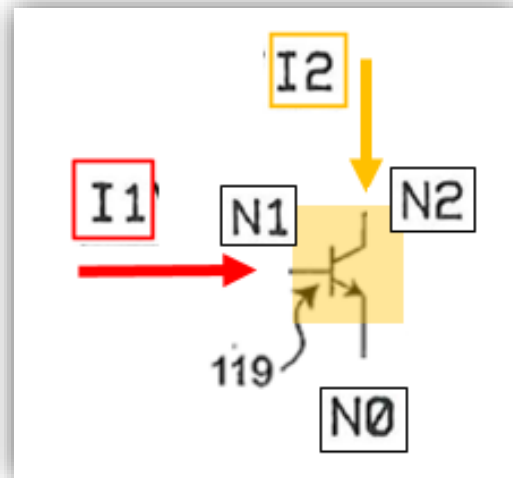
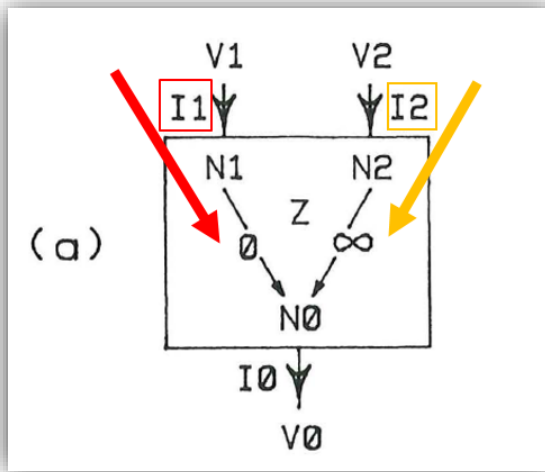


EX-1004 Fig. 1 (annotated) (partial).

Consistent with the discussion of current mirrors in the State of the Art section, transistor 119 as connected in *Ishimaru* is configured to mirror in that it is configured to replicate (reproduce, duplicate, reflect, etc.), *i.e.*, *mirror* the current at its input (the base of transistor 119) to generate the current at its output (the collector of transistor 119). §IV.F.2; EX-1004 Fig. 1; EX-1003 ¶113.

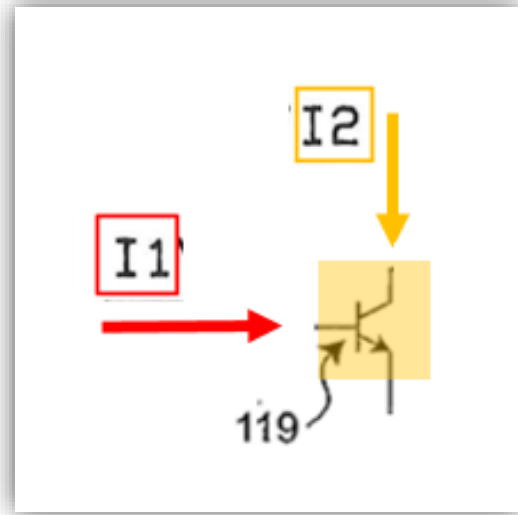
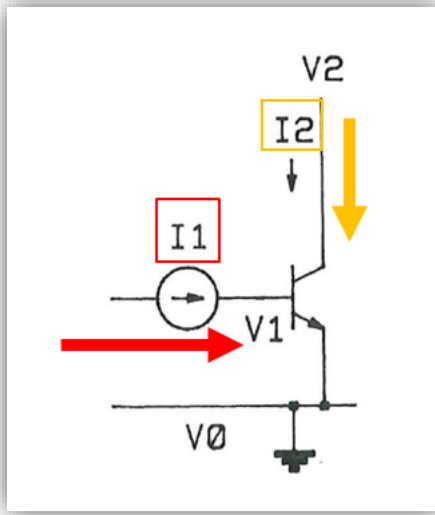
When connected as shown in *Ishimaru*, transistor 119 takes the general, three-node form set out by Barrie Gilbert and Gray for a *current mirror*. EX-1012 Fig. 6.1a; EX-1013 Fig. 4.1). Accordingly, in the side-by-side images below, *Ishimaru*'s transistor 119 is used as a current mirror in that node N1 (of *Gilbert* Figure 6.1a

showing a current mirror) is the base of transistor 119, N2 the collector of transistor 119, and N0 the emitter of transistor 119, with the circuit replicating (and scaling) current I1 to generate output current I2. EX-1012 242, Fig. 6.1a; EX-1013 Fig. 4.1; EX-1003 ¶114.



EX-1012 240, Fig. 6.1a (annotated) EX-1004 Fig. 1 (annotated)(partial)

Likewise, *Ishimaru's* transistor 119 is connected and used in the same way as *Gilbert's* single transistor current mirror shown of his Figure 6.2a. EX-1003 ¶115.



EX-1012 243, Fig. 6.2a (annotated)      EX-1004 Fig. 1 (annotated)(partial)

In addition to the replication discussed above, *Ishimaru's* current mirror is further configured to **amplify** the  $I_{CONTROL}$ , scaling it up by the amplification factor to form  $I_{CORRECTION}$ , namely scaling by the common-emitter current-gain,  $\beta$ , of the transistor 119, which quantifies the “mirror ratio” (discussed below) of *Ishimaru's* current mirror. §IV.F.2, EX-1015 38; EX-1012 242-243. The current at the collector ( $I_{C119}$ ) of transistor 119 (a transistor having  $\beta_{119}$ ) is generally related to the current at the transistor's base ( $I_{B119}$ ) by the equation:  $I_{C119} = \beta_{119} * I_{B119}$ . *Id.*; EX-1004 Fig. 1. Thus, the ratio of the input current  $I_{B119}$  to the output current  $I_{C119}$  is generally  $\beta_{119}$ . EX-1004 Fig. 1. The gain through the transistor is the “mirror ratio”, “M”, by which *Ishimaru's current mirror* scales the  $I_{CONTROL}$  to generate the  $I_{CORRECTION}$ . EX-1012 242-243; EX-1004 Fig. 1. The gain of transistor 119 can be configured to a target value by designing the voltage and current biasing of the

transistor 119 (within the constraints of the circuit), such that a  $\beta$  in a range, *e.g.*, of about 60 to 150 or more, can be achieved. The time constant of the transient can then be tuned through the choice of components, namely C121 and R136. EX-1004 ¶¶55-56. EX-1004 ¶¶55-56; *see also, infra*, Claim 2; EX-1003 ¶116.

Thus, transistor 119 as connected in *Ishimaru* is a *current mirror* in that it constitutes a circuit configured to mirror a current, which can be configured to achieve a target gain. Transistor 119 is a circuit that has electrical interconnections, including input/output, and other connections that permit current to flow through the circuit. EX-1020 2; EX-1003 ¶117.

## **Claim 2**

***[2] The power amplifier system of claim 1 wherein the time-dependent signal generator includes a resistor-capacitor (RC) network.***

*Ishimaru* discloses this limitation. EX-1003 ¶¶118-119. As illustrated in Figure 1, *Ishimaru*'s PA system includes a speedup circuit (dark blue) that includes a *time-dependent signal generator* (red) that “transiently (temporarily) increases” the  $I_{BIAS}$  fed to the amplifier transistor by the bias circuit during the period after startup. EX-1004 ¶13. Speedup circuit 122 includes transistors 119, 120, *resistor* 136, as well as a *capacitor* 121 connected between the base of transistor 120 and bias terminal 108. *Id.* ¶¶50-51, 55-56. The charging time of capacitor 121 depends on the size of the capacitor and the resistance through R136 to ground, which sets

the shape of the control current from the speedup circuit 122. *Id.* ¶¶55-56. A POSITA understands that this speedup circuit forms an *RC network*. EX-1003 ¶118.

More specifically, a POSITA understands that *Ishimaru* applies a large current amplification (by virtue of transistors 119, and 120)<sup>3</sup> to the transient current controlled by “capacitance element 121.” EX-1004 ¶¶52, 55-56, Fig. 1 (capacitor 121, transistors 119 and 120, and resistor 136). When the enable signal turns on, capacitor 121 charges by virtue of current flowing through transistor 119, transistor 120 and resistor 136 to ground. Owing to the very high gain of transistors 119 and 120, the current in the capacitor can be made very small, and therefore the capacitor 121 can be made small for a given time constant. Likewise, the size of resistor 136 can be small as the capacitor current ( $I_{C121}$ ) is generally the resistor current ( $I_{R136}$ ) divided by the gain of transistors 119 and 120. In *Ishimaru*, a physically small resistor can be used for R136 as its current when traced back to C121, will be greatly reduced by the gain of 119 and 120. Increasing the size of R136, or the size of C121, will slow the rate at which C121 charges, providing the circuit with a time-dependent signal that has a longer time constant. Conversely, a smaller C121 and/or R136 will allow the capacitor to charge more rapidly, providing a time-dependent signal that

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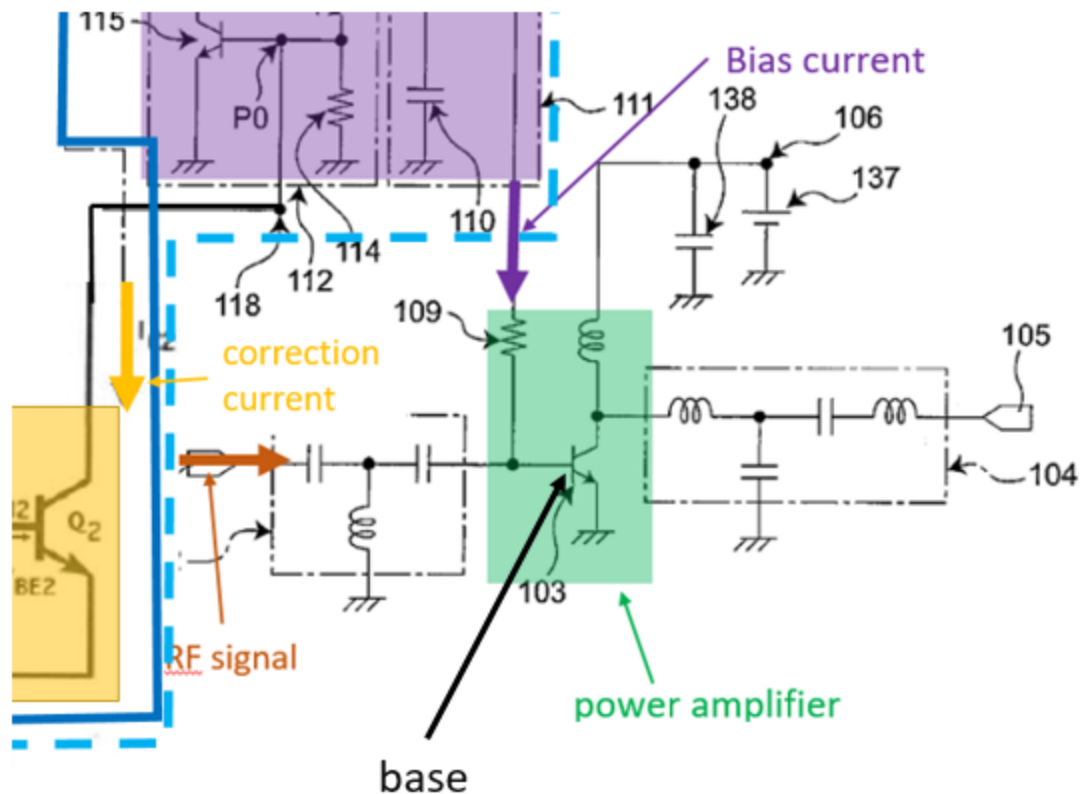
<sup>3</sup> Each transistor has an amplification factor, “ $\beta$ ” that relates the transistor’s base current to its collector current. EX-1003 119 (*e.g.* EX-1015 38).

reaches steady state more quickly. Thus, *Ishimaru's time-dependent signal generator* includes a resistor-capacitor (RC) network that includes capacitor 121 and resistor 136. EX-1003 ¶119.

### **Claim 10**

***[10] The power amplifier system of claim 1 wherein the power amplifier includes a bipolar transistor having an emitter, a base and a collector, the base configured to receive the RF signal and the bias current.***

*Ishimaru* discloses this limitation. EX-1003 ¶120. *Ishimaru* discloses that transistor 103 is a bipolar transistor. EX-1004 ¶¶54, 55. In *Ishimaru*, the base of transistor 103 receives the “high-frequency signal” for “radio communication devices” from terminal 101 (*where the base is configured to receive the RF signal*) and bias transistor 107 “supplies a base bias current to a base terminal of the amplifier transistor 103” (*the base receives the bias current*). EX-1004 ¶¶41-42. As illustrated in the annotated portion of Figure 1 below, the base of transistor 103 receives *the RF signal* (brown arrow) and the *bias current* (purple arrow). EX-1003 ¶120



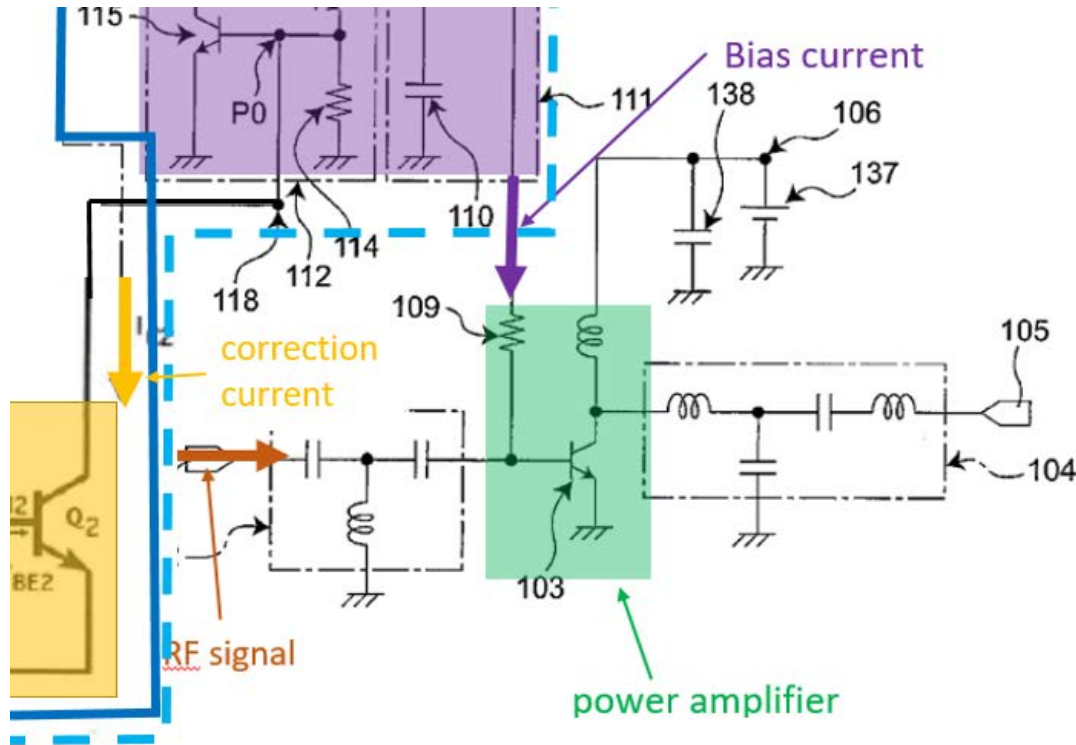
EX-1004, FIG 1 (annotated); see §IV.F.1 (showing BJT terminals).

**Claim 11**

*[11] The power amplifier system of claim 10 wherein the emitter is electrically connected to a power low voltage and the collector is configured to generate an amplified version of the RF signal.*

*Ishimaru* discloses this limitation. EX-1003 ¶¶121-122. Figure 1 shows an input signal terminal 101 that receives a high-frequency signal (brown arrow) as an input signal, and this input signal passes through an input matching circuit 102, and is then amplified by amplifier transistor 103 (green). The amplifier transistor 103 outputs a signal through output matching circuit 104 to output signal terminal 105

as an amplified version of the RF input signal (*the collector is configured to generate an amplified version of the RF signal*). EX-1004 ¶¶41-43, 46, 49; EX-1003 ¶121.



EX-1004, FIG 1 (partial) (annotated).

Figure 1 further illustrates that the emitter of transistor 103 is electrically connected to Ground, which a POSITA understood was a *power low voltage*. *Ishimaru's* disclosure is consistent with the disclosure of the '101 Patent, in which the emitter of PA transistor 61 is likewise connected to ground. EX-1001 7:45-51, Fig. 3B; EX-1003 ¶122.

**Claim 17**

***[17.0] A method of biasing a power amplifier, the method comprising:***

To the extent the preamble is limiting, *Ishimaru* discloses this limitation for the same reasons as discussed with respect to limitation [1.2]. EX-1003 ¶123.

***[17.1] shaping an enable signal using a time-dependent signal generator to generate a control current;***

*Ishimaru* discloses this limitation for the same reasons as discussed with respect to limitation [1.2.1]. EX-1003 ¶124.

***[17.2] amplifying the control current using a current mirror of a current amplifier to generate a correction current; and***

*Ishimaru* discloses this limitation for the same reasons as discussed with respect to limitations [1.2.2] and [1.2.4]. EX-1003 ¶125.

***[17.3] generating a bias current for a power amplifier using a primary biasing circuit, the primary biasing circuit configured to use the correction current to correct for a variation in gain of the power amplifier when the power amplifier is enabled.***

*Ishimaru* discloses this limitation for the same reasons as discussed with respect to limitation [1.2.3]. EX-1003 ¶126.

## **Claim 18**

***[18] The method of claim 17 wherein shaping the enable signal includes using a resistor-capacitor (RC) network of the time-dependent signal generator.***

*Ishimaru* discloses this limitation for the same reasons as discussed with respect to Claim 2. EX-1003 ¶127.

**Claim 20**

***[20]. The method of claim 17 wherein generating the bias current includes shaping the bias current so as to compensate for a gain variation of a heterojunction bipolar transistor (HBT).***

*Ishimaru* discloses this limitation for the reasons as discussed with respect to Claim 10 and [1.2.3], and further in view of the general knowledge in the art concerning HBT transistors. EX-1003 ¶¶128-132; *See* §IV.F.3.

As discussed for claim 10 and [1.2.3], *Ishimaru* discloses shaping the bias current to compensate for a gain variation of the BJT used for its PA transistor 103 for radio communication devices. *See* Claim 10 and [1.2.3]; EX-1004 ¶¶1, 54, 55; EX-1003 ¶129.

A POSITA would understand *Ishimaru*'s solution to apply to all types of BJT processes for PAs for such radio communications devices, of which heterojunction bipolar transistors (HBT) were a popular, market-leading form for RF PAs. *See* §IV.F.3. As explained in the State of the Art, it was part of the general knowledge in the art to use the HBT form of BJT, as was widely done and well documented, for bipolar junction transistor implementations of RF PAs. *Id.* This is because HBTs were an improved form of BJTs, with well-documented advantages for RF power amplification, including, *e.g.*, having the robustness, speed, density, and linearity necessary for such circuits. EX-1003 ¶130; §IV.F.3.

While *Ishimaru* does not expressly refer to the use of HBTs, that is nonetheless understood by a POSITA for several reasons. First, *Ishimaru* expressly discloses a solution for RF PAs implemented as BJTs, and a POSITA would reasonably draw the inference that *Ishimaru* disclosed the use of its solution for the market leading forms of such BJTs, namely HBTs. §IV.F.3. Indeed, it was conventional to use HBTs in the context of radio communication devices having RF PAs using BJT transistors like *Ishimaru*'s. Second, *Ishimaru* is directed to an incremental improvement in the startup behavior of BJT-based RF PAs that is directed at the margin of high performing devices, *i.e.*, the type of BJT-based RF PAs commonly implemented as HBTs. A POSITA understood that HBTs, as BJTs, suffer the same thermal effects described by *Ishimaru*, and would likewise benefit in the same way as other BJTs. For these reasons, a POSITA reading *Ishimaru* in 2011 understood that *Ishimaru*'s "radio communication device" with its PA (green) and bias circuits (blue) would be implemented in *an integrated circuit attached to a package substrate in a packaged module* as claimed. Thus, while not explicitly stated, the HBT form claimed is nonetheless disclosed to a POSITA in view of the reasonable inferences that a skilled artisan would draw when reading *Ishimaru*. *Eli Lilly v. L.A. Biomedical Rsch. Inst.*, 849 F.3d 1073, 1074–75 (Fed. Cir. 2017) (A reference's disclosure includes both its express teachings as well as that which a

POSITA would reasonably understand or infer therefrom); *In re Preda*, 401 F.2d 825, 826 (CCPA 1968); EX-1003 ¶131.

To the extent that Patent Owner argues that a POSITA would not have drawn the reasonable inference that *Ishimaru*'s PA would employ BJTs using the market-leading HBT form, that would have at minimum been obvious to a POSITA in view of the general knowledge in the art, for the same reasons discussed above and evidenced by the well-known advantages of HBTs for RF PAs. §IV.F.3. A POSITA would have been motivated to use an HBT for *Ishimaru*'s BJT PA 103 to achieve any one of a host of known benefits such as their "improvement in the high frequency performance of the transistor" (EX-1015), their "inherently superior linearity and efficiency performance" (EX-1017), their "reliability [being] well known to be excellent" (EX-1017), and other advantages in cost, size, robustness, *etc.* (EX-1008, EX-1025). §IV.F.3. A POSITA would have been motivated to implement at least the PA of *Ishimaru* as an HBT following these well-documented advantages. *Id.* Doing so would involve nothing more than using a market-leading prior art technique (using HBT type of BJT-based RF PAs) according to conventional wisdom for the benefits and successes confirmed by the market and reported by others. Finally, there would have been nothing technologically counterintuitive about implementing *Ishimaru*'s PA system with an HBT as compared to other forms of a BJT. Indeed, the '101 Patent references HBTs in passing, without any special

significance, criticality, challenges, or counterintuitive concepts or properties. EX-1001 7:53-55. This lack of detail is consistent with the well-developed state of the art for HBT RF PAs. §IV.F.3. Furthermore, given *Ishimaru*'s teachings, the selection of a market-leading BJT type (HBT) would have been viewed with a reasonable expectation of success with predictable benefits, all well within the skill of a POSITA as demonstrated by the popularity of HBTs in the marketplace. §IV.F.3. EX-1003 ¶132.

### **Claim 21**

***[21.0] A bias circuit for biasing a power amplifier, the bias circuit comprising:***

To the extent that the preamble is limiting, *Ishimaru* discloses a bias circuit (light blue) as illustrated in Figure 1, as discussed in limitation [1.2]. EX-1003 ¶133.

***[21.1] a time-dependent signal generator configured to shape an enable signal of the power amplifier to generate a control current;***

*Ishimaru* discloses this limitation for the same reasons as discussed with respect to limitation [1.2.1]. EX-1003 ¶134.

***[21.2] a current amplifier configured to amplify the control current to generate a correction current, the current amplifier including a current mirror; and***

*Ishimaru* discloses this limitation for the same reasons as discussed with respect to limitations [1.2.2] and [1.2.4]. EX-1003 ¶135.

***[21.3] a primary biasing block configured to generate a bias current for the power amplifier based at least partly on the correction***

***current, the bias current configured to correct for a variation in gain of the power amplifier when the power amplifier is enabled.***

*Ishimaru* discloses this limitation for the same reasons as discussed with respect to limitation [1.2.3]. EX-1003 ¶136.

**Claim 22**

***[22] The bias circuit of claim 21 wherein the time-dependent signal generator includes a resistor-capacitor (RC) network.***

*Ishimaru* discloses this limitation for the same reasons as discussed with respect to Claim 2. EX-1003 ¶137.

**D. Ground 2: Claims 1-2, 10-11, 17-18, and 20-22 Are Obvious over *Ishimaru* in View of *Harrison***

Ground 2 is submitted to address Patent Owner’s claim construction of *current mirror* that differs from Petitioner’s plain meaning in that Patent Owner’s construction adds the limitations that the *current mirror* must have “at least two transistors with their base or gate terminals tied together.” While Petitioner asserts that the State of the Art (§IV.F.2) demonstrates that a POSITA understood that a *current mirror* is not limited to any specific number or configuration of transistors, the Board need not construe the term as Ground 2 discloses a current mirror even under Patent Owner’s claim construction. EX-1003 ¶138.

Ground 2 is identical to Ground 1 except for limitations [1.2.4] and [21.2] which recite that *the current amplifier including a current mirror*, and limitation [17.2] that recites *amplifying the control current using a current mirror*. All other limitations are disclosed by *Ishimaru* as discussed with respect to Ground 1 set forth above. EX-1003 ¶139.

**1. The *Harrison* Reference**

*Harrison* is a book titled “Current Sources & Voltage References” and its Chapter 4 is titled “Using BJTs to Create Current Sources.” EX-1006 47. *Harrison* explains that a bipolar junction transistor (or “BJT”) is a “current-operated semiconductor device” with “three terminals that are designated the base, the collector, and the emitter.” *Id.* 49; EX-1003 ¶140.

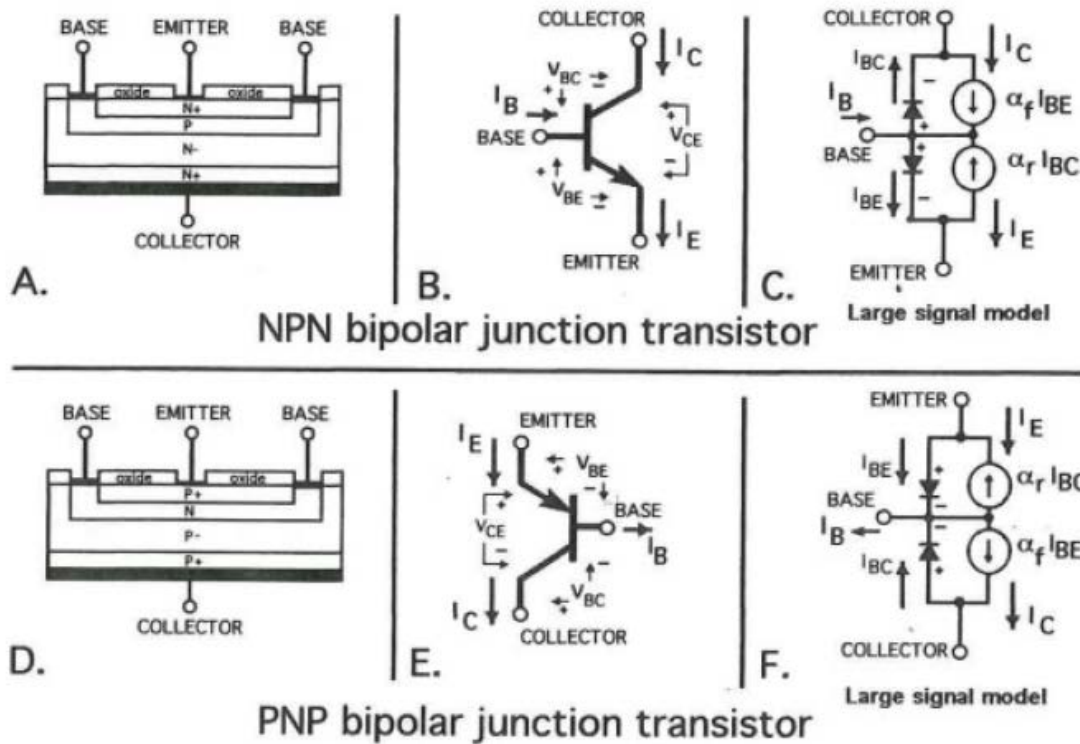


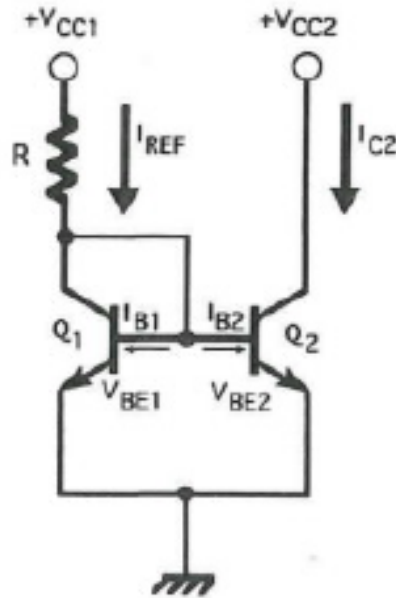
Figure 4.2. Showing the structure of the BJT, as well as its various voltages, currents, and polarities. Notice the two inherent diodes that provide forward and reverse bias.

EX-1006 50, Fig. 4.2.

*Harrison* explains that “simple current sources” using bipolar analog transistors were used starting in the late 1960s “for purposes of biasing and stability” and analog circuit designers “found a reliable method of biasing their circuits and thereby improving the overall quality and accuracy of their products.” *Id.* 68. *Harrison* further explains that “virtually all BJT current sources are configured as *current mirrors* (aka current reflectors), where an input current is mirrored at the output, in either a matched 1:1 or other ratio.” *Id.* 70. *Harrison* is from the same field of art as the '101 Patent because it describes the operation of analog circuit

components, such as bipolar junction transistors, that are used in RF electronics and PAs. EX-1003 ¶141.

*Harrison* illustrates simple two-transistor current source designs using BJT NPN transistors:



Basic NPN Current sink

Figure 4.18. Basic BJT current mirrors.

EX-1006 Fig. 4.18 (reproduced in part), 71 (“reference current,  $I_{REF}$ , will be mirrored (duplicated)”); EX-1003 ¶142.

*Harrison*’s two-transistor current mirror shown and described in Fig. 4.18 was a widely understood circuit, well established in the general knowledge of a POSITA. §IV.F.2; EX-1013 251-54, 257, Fig. 4.2; EX-1012 251, 280, Fig. 6.7(a); EX-1014 172. *Harrison* is exemplary of that general knowledge. EX-1003 ¶143.

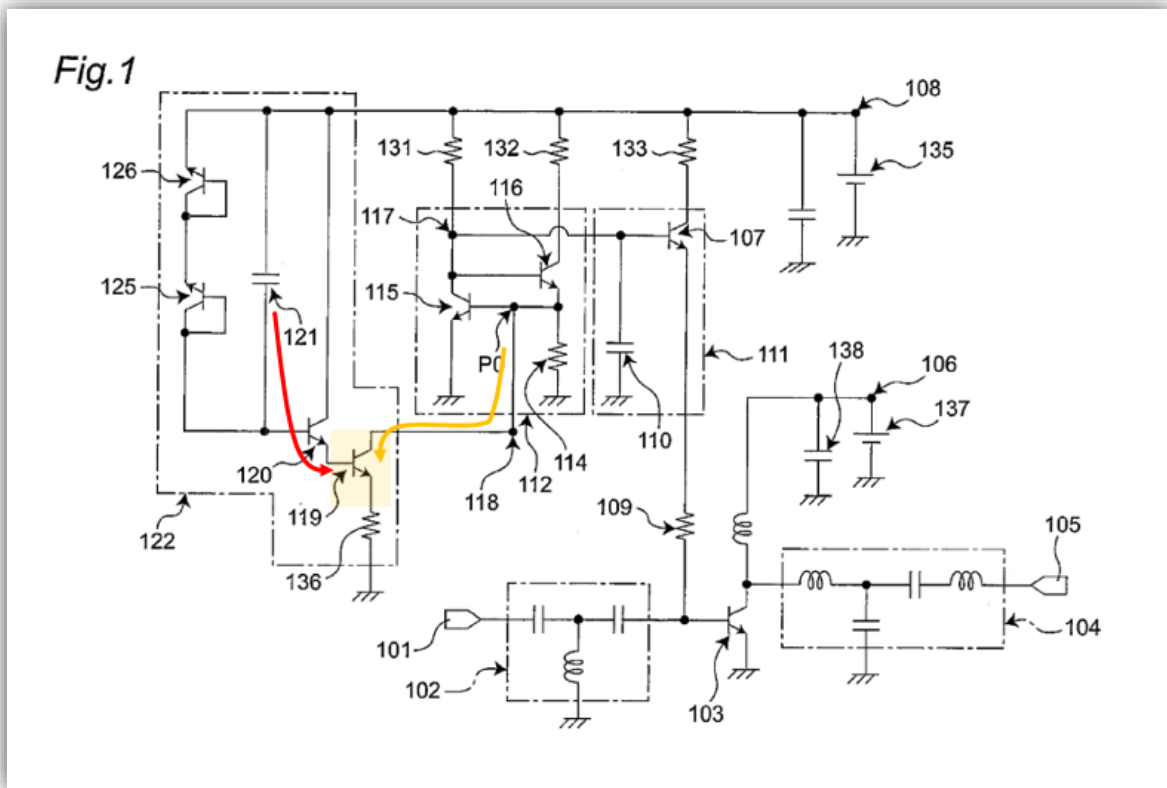
**2. Detailed Application of *Ishimaru* in View of *Harrison***

**Claim 1**

***[1.2.4] the current amplifier including a current mirror.***

To the extent Patent Owner argues that *Ishimaru* does not disclose a *current mirror*, *Ishimaru* in view *Harrison* discloses this limitation. EX-1003 ¶¶144-165.

As discussed in Ground 1, *Ishimaru* discloses a speedup circuit 122 that responds at “a rise time of the control voltage of the control voltage source 135 (at turn-on of the amplifier)” to generate a time-varying current via capacitor 121 that is amplified by and 119 (*current amplifier*). §V.C. Furthermore, as illustrated in the annotated Figure 1, below, a POSITA recognizes that *Ishimaru* uses the amplified version of the current (red arrow) as a current sink to pull a specifically shaped correction current (gold arrow) out of the primary biasing circuit. EX-1003 ¶145.

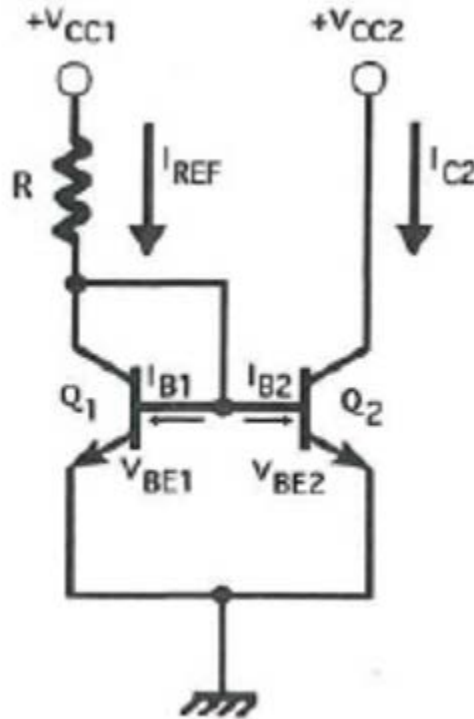


EX-1004 Fig. 1 (annotated).

A POSITA readily recognizes the coupling of the left and right sides of *Ishimaru*'s circuit as involving a current source generated on the left side that is replicated as a current sink on the right side, which is a coupling that takes the general form of a *current mirror* (*i.e.* transistor 119 as discussed in Ground 1). EX-1003 ¶146.

A POSITA further recognizes that the current source / current sink coupling of *Ishimaru* would be well suited for, and ready for improvement by, the use of additional current mirror structures to couple the two sides of *Ishimaru*'s circuit to achieve the well-known benefits of such current mirrors. EX-1003 ¶147.

In that regard, *Harrison* teaches a well-known “basic” current mirror using NPN transistors that operates as a “mirror-sink,” as shown in the excerpt of Figure 4.18 below:

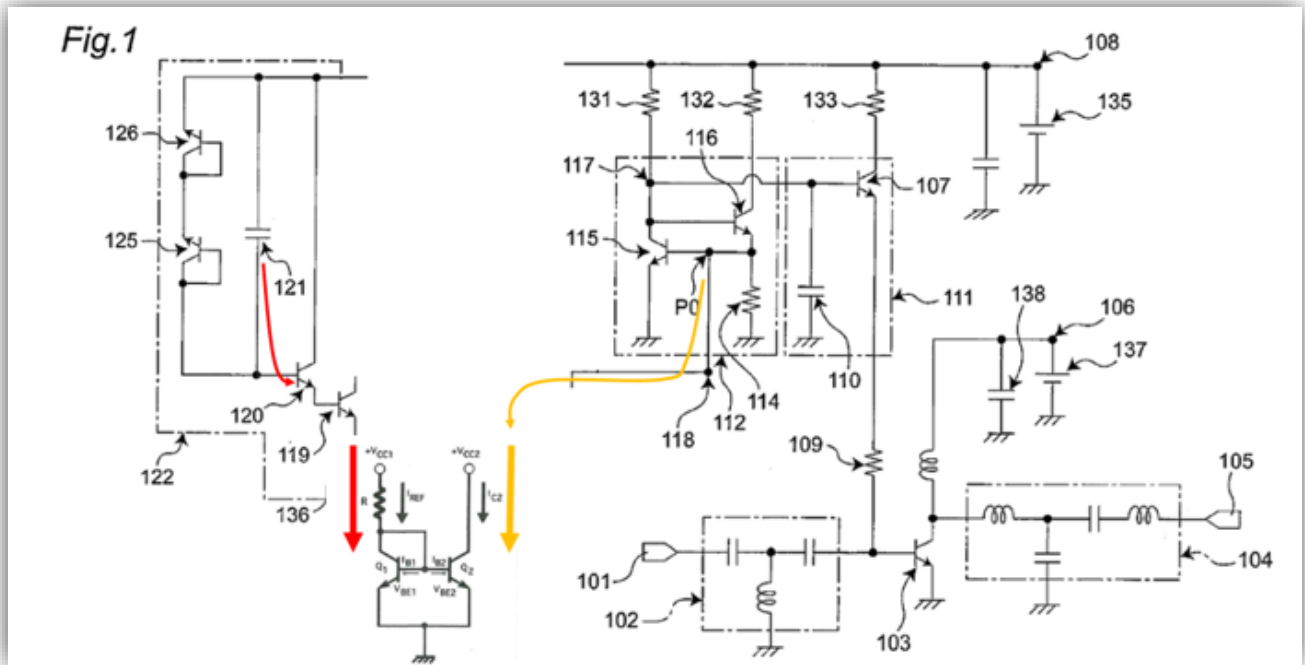


EX-1006 71; Fig. 4.18; EX-1003 ¶148.

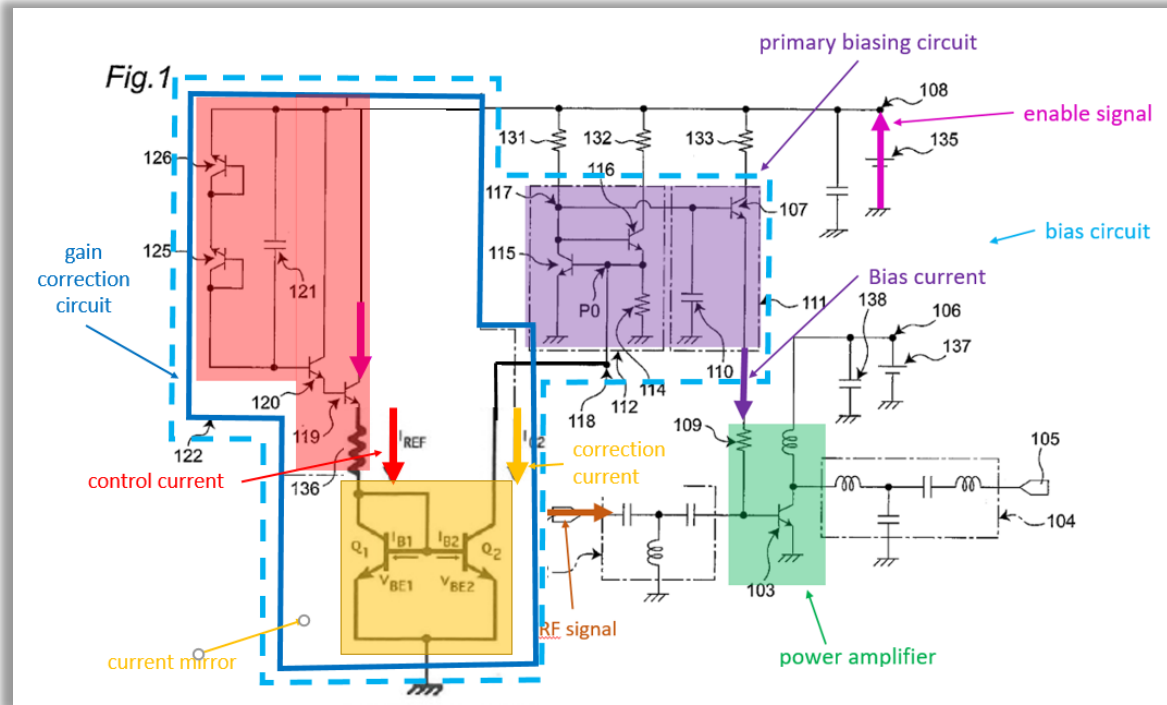
As can be seen in Figure 4.18 above, this current mirror also satisfies Patent Owner’s proposed construction of current mirror in that it has at least two transistors (Q1 and Q2) with their base terminals tied together. EX-1020 2; EX-1006 71, Fig. 4.18. Furthermore, the basic current mirror above is a circuit configured to mirror  $I_{REF}$  to  $I_{C2}$ , and is configurable to achieve a target gain that can be finely tuned by adjusting the ratio of the transistor sizes. EX-1006 95 (describing “current scaling”

by setting the ratio of the emitter area); EX-1003 ¶149; *see also* EX-1012 280; EX-1013 254, 257; EX-1014 172.

A POSITA would recognize modifying the speedup circuit as taught by *Ishimaru* to add a basic current mirror as taught by *Harrison* would be beneficial because it provides flexibility in allowing a broader range of voltages and a broader range of amplification due to the ability to achieve the desired current amplification by changing the ratios of transistor sizes in the basic current mirror. §IV.F.2. Obviousness does not require bodily incorporation of references or building an actual circuit, but the ease with which a POSITA would advantageously apply *Harrison's* teaching to *Ishimaru* as illustrated below in the following annotated figures, derived from *Ishimaru's* Figure 1 and *Harrison's* Figure 4.18. EX-1003 ¶150.



As illustrated above, a basic current mirror such as taught by *Harrison* can be advantageously added to *Ishimaru*'s speedup circuit by interposing the basic current mirror at the emitter of transistor 119, and then connecting node P0/118 to the collector of current mirror transistor Q2. The collector of transistor 119 is then connected to the control voltage source (*the enable signal*). EX-1003 ¶151.

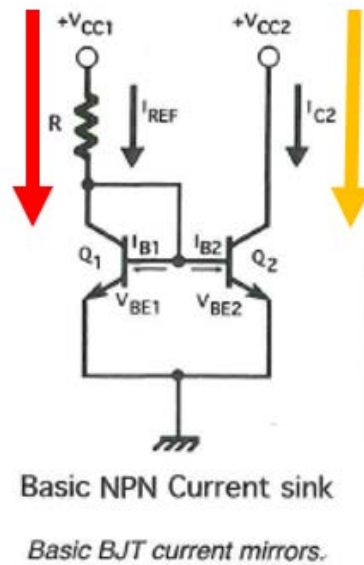


As shown in the above annotations and simulation, *Ishimaru*' speedup circuit modified with *Harrison*'s basic current mirror is a gain correction circuit (dark blue) that responds at "a rise time of the control voltage of the control voltage source 135 (at turn-on of the amplifier)" in response to activation of the PA enable signal (pink) to generate a transient current signal via capacitor 121 that is amplified by transistors 120 and 119 and passed through resistor 136 to generate a control current (red arrow). *Ishimaru* modified with *Harrison* then takes this amplified time varying current signal (red arrow) and mirrors it using the basic *current mirror* to generate a time-varying correction current (gold arrow) that is pulled from node 118. EX-1003 ¶152.

A POSITA would have been highly motivated to combine *Ishimaru*'s teaching of a bias circuit for a PA with *Harrison*'s disclosure of a basic current mirror and have a reasonable expectation of success for at least the following reasons. EX-1003 ¶153.

*Harrison* discloses a “basic” current mirror. EX-1006 71. Current mirrors were well-known in the art and were considered “a familiar icon of modern analog design.” EX-1012 239. Indeed, current mirrors were “widely used in analog integrated circuits” “as biasing elements” and were “particularly useful building blocks for analog circuit design.” EX-1013 251; EX-1014 170; EX-1003 ¶154.

One of these advantages was that current mirrors take a reference current in one branch of a circuit and accurately reproduce or reflect that current in a second branch of that circuit, and can do so “relatively independent of the absolute values of the device parameters.” *Id.*; EX-1014 171. Thus, current mirrors were useful in coupling circuits together such that an input current could be provided into one branch of a circuit and the current mirror would then replicate (or *mirror*) that current such that the current mirror would pull a mirrored version of that current out of the second branch of the circuit. *Harrison* illustrates this configuration (called a current sink), where the input branch is annotated in red and the output branch is annotated in yellow. EX-1006 71; EX-1003 ¶155.



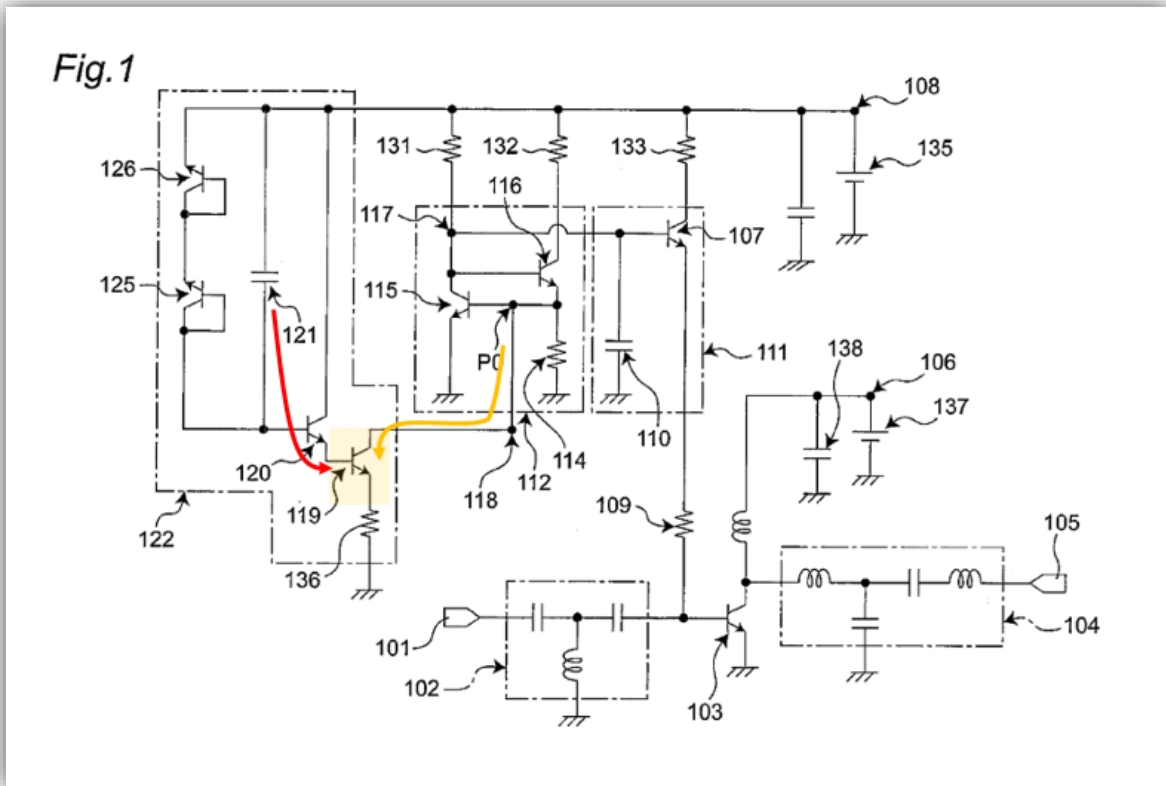
EX-1006 (Fig. 4.18) (annotated).

Further, current mirrors were known to be useful in providing desired current scaling when mirroring a current (called **current mirror gain**) by changing the ratios of transistor sizes. EX-1006 95 (describing “current scaling” by setting the ratio of the emitter area). In the case of bipolar junction transistors, this would be done by changing the relative sizes of the emitters of the current mirror transistors. EX-1013 25. Scaling transistor sizes in current mirrors to achieve granular, targeted levels of scaling that could advantageously be fine-tuned was well understood as of the priority date of the '101 Patent, and described in multiple textbooks. EX-1013 251-257; EX-1014 172; EX-1012 252, 280; EX-1003 ¶156.

In addition, a POSITA understood that *Harrison's* two-transistor current mirror would advantageously provide better isolation between the left side and the

right side of *Ishimaru*'s circuit. First, because there are separate emitter currents and paths in the two-transistor mirror, there is a degree of separation between the left and right sides of the circuit. Second, it avoids the issue that using a single transistor like *Ishimaru*'s 119 as the current mirror has coupling (parasitic) between its base and collector due to standard parasitic capacitance. This coupling across 119 can create unwanted coupling across the transistor, such that noise on one side of the circuit can pass to the other side. Adding *Harrison*'s two-transistor current mirror does not have this limitation, providing better isolation between the input and output current signals than *Ishimaru* provides. EX-1003 ¶157.

A POSITA would thus have been motivated to modify the teachings of *Ishimaru* to add a basic current mirror as taught by *Harrison* because a POSITA understood that *Ishimaru*'s circuit is designed to amplify the current that flows through capacitor 121 (annotated in red below) to generate the current sink pulled from node 118 (annotated in yellow). EX-1004 ¶¶50-52, Fig. 1; EX-1003 ¶158.



EX-1004 Fig. 1 (annotated).

A POSITA recognized that *Ishimaru* used a current source (red) from circuit 122 to generate a current sink (yellow) from 112, coupling the two circuits using the current mirroring provided by transistor 119. A POSITA readily understood that this coupling could be improved by use of the basic current mirror of *Harrison* because of multiple advantages of providing an additional stage of fine tuning the current amplification. The additional stage of fine tuning would give the designer an additional degree of freedom in designing the circuit, would provide better isolation between the two sides of the circuit, and allow fine tuning in a final amplification stage that had better linearity, better control, and higher configurability

of its mirror ratio,  $M$ , in scaling the mirrored current.). EX-1003 ¶159; *See also* §IV.F.2 (discussing two-transistor mirrors).

A POSITA would understand that, without the additional teachings of *Harrison*, *Ishimaru*'s circuit is constrained by the limited configurability of the  $\beta$  (amplification factor) of transistors 119 and 120. EX-1006 53-55. A POSITA was aware that the  $\beta$  of transistors 119 and 120 would be, *e.g.*, 60 to 150 or more, meaning that the gain of *Ishimaru*'s transistors 119 and 120 would be a relatively large and cumbersome gain (for example, x100 for transistor 120 and x100 for transistor 119 would result in a total gain of 10,000). EX-1006 53-55; EX-1015 38 (practical  $\beta$  values can be "up to 500"). While the  $\beta$  values provide amplification, and, for transistor 119 provide a mirror ratio, that mirror ratio is "not very linear" and "poorly-controlled" compared to other current mirrors, such as the basic current mirror of *Harrison*. EX-1012 242; EX-1006 53-55. Thus, a POSITA readily understood that having to rely upon just the  $\beta$  gains of transistors 119 and 120 is another factor making tuning *Ishimaru*'s circuit overly complicated and constrained. *Id.*; EX-1003 ¶160.

Adding a basic current mirror similar to that taught by *Harrison*, however, allows for an additional stage of amplification that can be finely tuned, linear, tightly controlled and granular scaling of the current by adjusting the emitter area of the current mirror transistors, as discussed above. Being able to scale currents in this

manner would be useful for a circuit designer wanting to establish a speedup control circuit that could advantageously be reused and adapted for different PA applications and product lines. That is because a POSITA understood that different PAs have different startup and steady state operating qualities, and that the gain variation in *Ishimaru*'s Figure 2 is specific to a given PA in a given layout, in a specific operating point and use case. The corresponding corrective transient current thus has a specific amplitude and duration that is suitable for the application at issue. EX-1003 ¶161.

For example, using different PA circuit layouts (*i.e.* where components are dimensionally closer or farther away from each other), different PA packaging, or different PA integrated circuits using a different semiconductor manufacturing process (*e.g.*, Gallium Arsenide (“GaAs”) Heterojunction Bipolar Transistors (“HBTs”) (together “GaAs HBTs”), or Silicon Germanium Bipolar CMOS HBTs (“SiGe BiCMOS HBTs”)), will result in different thermal behaviors and startup effects, and so the amount of correction required will vary. *Ishimaru* itself recognizes that temperature effects depend on the layout of the PA and the amount of correction required varies across applications. EX-1004 ¶23 (“[T]urn-on behavior of the control voltage source in the amplifier depends on the layout of the amplifier, particularly on the placement of transistors[.]”), ¶3 (“In some communication systems, slight changes of amplification gain as small as 0.2 to 0.3 dB may matter.”), ¶4 (“there are some cases in which variations in amplification

ratio or phase on the order of several tens to several hundreds of  $\mu\text{s}$  caused by relatively slow temperature increases due to heat generation as an example do matter.”). EX-1003 ¶162.

Thus, *Ishimaru* provides express motivation for a POSITA to add a current mirror of similar design to *Harrison*'s for its intended purpose in order to provide flexibility in scaling *Ishimaru*'s current, including allowing a designer to tune the operation of *Ishimaru*'s corrective current transient in Figure 3 to a higher peak (such as for a PA having a larger gain variation). A POSITA understands that *Ishimaru*'s circuit otherwise constrains the ability to tune the  $I_{CORRECTION}$  at node 118 as a function of the current through capacitor 121 because of the common, fixed relationships caused by transistor 119 and resistor 136 and the design constraints that limit the configurability of the amplification factors  $\beta$  of transistors 119 and 120. A POSITA would have recognized that *Harrison*'s two-transistor current mirror would advantageously provide an extra degree of freedom in tuning *Ishimaru*'s circuit to compensate for the gain problems of a given PA. EX-1003 ¶163.

Modifying the teachings of *Ishimaru* with the basic current mirror taught by *Harrison* would involve no more than combining prior art elements (*Ishimaru* and a conventional current mirror) according to known methods (coupling a current source through a positive current mirror to a current sink, while scaling the mirror's gain to provide tunable amplification) to yield predictable results. Adding a current mirror

simply uses a known technique (scaling currents between two branches of a current mirror) to improve *Ishimaru* by scaling its currents between the two branches of its circuits in the same way. EX-1003 ¶164.

The combined teachings of *Ishimaru* and *Harrison* is consistent with the disclosure of the '101 Patent that the term *current mirror* can refer to current amplification circuits including a plurality of current mirrors combined (*e.g.*, cascaded) to achieve a target gain. EX-1001 11:42-45. EX-1003 ¶165.

### **Claim 17**

***[17.2] amplifying the control current using a current mirror of a current amplifier to generate a correction current; and***

*Ishimaru* in view of *Harrison* discloses this limitation for the same reasons as discussed with respect to limitation [1.2.4]. EX-1003 ¶166.

### **Claim 21**

***[21.2] a current amplifier configured to amplify the control current to generate a correction current, the current amplifier including a current mirror; and***

*Ishimaru* in view of *Harrison* discloses this limitation for the same reasons as discussed with respect to limitation [1.2.4]. EX-1003 ¶167.

Thus, for Ground 2 *Ishimaru* in view of *Harrison* discloses each of the Challenged Claims. EX-1003 ¶168.

## VI. DISCRETIONARY DENIAL WOULD BE INAPPROPRIATE

### A. Discretionary denial under the *Fintiv* factors is not appropriate.

There is no active district court case, and the ITC case is not a basis to deny this petition under *Fintiv*. K. Vidal, *Interim Procedure For Discretionary Denials in AIA Post-Grant Proceedings With Parallel District Court Litigation*, June 21, 2022 (guidance for *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11, at 6)). Pursuant to the Director's June 2022 Guidance Memo:

The plain language of the *Fintiv* factors... does **not** apply to parallel U.S. International Trade Commission (ITC) proceedings, as the ITC lacks authority to invalidate a patent and the ITC's invalidity rulings are not binding on the Office or on district courts ... For the foregoing reasons, the PTAB **no longer** discretionarily denies petitions based on applying *Fintiv* to a parallel ITC proceeding. This memorandum memorializes that practice. The PTAB will **not** discretionarily deny petitions based on applying *Fintiv* to a parallel ITC proceeding.

*Id.* Here, the district court case was filed in C.D. California on May 6, 2024, a co-pending ITC proceeding was filed on July 16, 2024 and investigation instituted on August 16, 2024, and, on September 13, 2024, pursuant to 28 U.S.C. §1659, the district court **granted Petitioner's motion to stay** the district court proceeding until the ITC determination becomes final.

**B. The Board Should Not Deny Institution Under 35 U.S.C. §325(d)**

None of the references cited in Grounds 1 and 2, nor the same or similar arguments pertaining thereto, were before the examiner during prosecution of the '101 Patent. Thus, the Board should not deny institution under 35 U.S.C. §325(d). *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 8 (PTAB Feb. 13, 2020) (precedential).

**VII. MANDATORY NOTICES – 37 C.F.R. §42.8**

**A. Real Parties-In-Interest Under 37 C.F.R. §42.8(b)(1)**

Petitioner certifies that the real party-in-interest in this Petition is Kangxi Communications Technologies (Shanghai) Co., Ltd.

**B. Related Matters Under 37 C.F.R. §42.8(b)(2)**

**1. Judicial Matters**

To Petitioners' knowledge, the '101 Patent is involved in the following litigation and investigation:

<b>Case Heading</b>	<b>Number</b>	<b>Tribunal</b>	<b>Date</b>
<i>Skyworks Solutions, Inc. v. Kangxi Communication Technologies Shanghai Co., Ltd et al.</i>	CDCA-8-24-cv-00974	CDCA	May 6, 2024
<i>Wireless Front-End Modules, Devices Containing the Same, and Components Thereof</i>	Inv. No. 337-TA-3762	ITC	July 17, 2024

**2. Administrative Matters**

As of this Petition’s filing date and to the best knowledge of Petitioner, the ’101 Patent has not been subject to any *inter partes* reviews, reissues, or reexaminations.

Petitioner is filing a petition for *inter partes* review of a related patent, U.S. Patent 9,917,563, simultaneously herewith as IPR2025-00372.

**3. Related Patents**

To the best knowledge of Petitioner, the following U.S. patents and patent applications related to the ’101 Patent include U.S. Patent 9,136,803, 9,667,203, 9,917,563, and 10,566,943.

**C. Lead and Back-Up Counsel Under 37 C.F.R. §42.8(b)(3)**

Lead Counsel	Back-Up Counsel
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In a concurrently filed Power of Attorney, Petitioner has granted Power of Attorney to these practitioners at Duane Morris LLP.

**D. Service Information Under 37 C.F.R. §42.8(b)(4)**

Service via hand-delivery may be made at the postal mailing address of either lead or back-up counsel. Petitioner consents to service by e-mail.

**E. Payment of Fees – 37 C.F.R. §42.103**

The required fee is being paid using the Patent Review Processing System.

**VIII. CONCLUSION**

Petitioner requests the Board institute an IPR and cancel the Challenged Claims.

Respectfully submitted,

DUANE MORRIS LLP

Dated: January 14, 2025

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## **CERTIFICATE OF COMPLIANCE WITH WORD COUNT**

Pursuant to 37 C.F.R. §42.24 *et seq.*, the undersigned certifies that this document complies with the type-volume limitations. This document contains 13,311 words as calculated by the “Word Count” feature of Microsoft Word 2016, the word processing program used to create it.

Pursuant to 37 C.F.R. §42.24(d), this word count excludes the table of contents, table of authorities, mandatory notices under §42.8, certificate of service, certificate of word count, appendix of exhibits, and any claim listing.

Dated: January 14, 2025

/John M. Baird/

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Reg. No. 57,585

*Lead Counsel for Petitioner*

## CERTIFICATION OF SERVICE ON PATENT OWNER

Pursuant to 37 C.F.R. §§42.6(e), 42.8(b)(4) and 42.105, the undersigned certifies that on January 14, 2025, a complete and entire copy of this Petition for *Inter Partes* Review of U.S. Patent 8,717,101 and all supporting exhibits were served via Federal Express, postage prepaid, to the correspondence address of record for the '101 Patent:

*Date of service* January 14, 2025

*Manner of service* FEDERAL EXPRESS

*Documents served* Petition for *Inter Partes* Review Under 35 U.S.C. § 312 and 37 C.F.R. § 42.104 of U.S. 8,717,101; Petitioner's Exhibit List; All Exhibits; Petitioner's Power of Attorney.

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