

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

KANGXI COMMUNICATION TECHNOLOGIES (SHANGHAI) CO., LTD.
Petitioner,

v.

SKYWORKS SOLUTIONS, INC.
Patent Owner.

Case IPR2025-00373
Patent 8,717,101

PATENT OWNER'S PRELIMINARY RESPONSE

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I. Introduction

Denial is warranted because the Petition fails to establish a reasonable likelihood of unpatentability. U.S. Patent No. 8,717,101 (the “’101 patent”) claims a system and method for biasing a power amplifier. This novel power amplifier system compensates for a variation in gain of the power amplifier by using a current mirror to generate a correction current that is used to generate the bias signal. As of the ’101 patent’s priority date, it was not publicly known to bias a power amplifier in this manner.

Petitioner’s grounds rely on substantially the same art and arguments the Examiner considered during prosecution of the U.S. Patent No. 9,917,563 (the “’563 patent”), which shares the same specification as and claims priority, through a series of continuations, to the ’101 patent. In Ground 1, Petitioner asserts that challenged claims are obvious over a single reference, Ishimaru. Petitioner bases its Petition on an argument that was already considered and rejected by the Patent Office. In particular, the Examiner already correctly found that a single transistor in a prior art reference to Alon does not disclose the claimed “current mirror” in the ’101 patent. Petitioner alleges no material error by the Examiner and relies on Ishimaru to make the *exact same* argument. This argument already failed once at the Patent Office and should fail again now.

In Ground 2, Petitioner asserts two references, Ishimaru and Harrison. Like Ground 1, the Patent Office already considered substantially the same art and arguments that Petitioner raises in Ground 2. In allowing the claims, the Examiner explained that none of the prior art of record, including prior art that disclosed current mirrors, discloses mirroring the control current to generate a correction current. In addition, Petitioner fails to show a motivation to combine Ishimaru and Harrison. To start, Petitioner proposes modifying Ishimaru's speedup circuit to include Harrison's current mirror. But neither Ishimaru nor Harrison discloses any motivation for including a current mirror in this speedup circuit. Petitioner's motivation for combining Ishimaru and Harrison is to supposedly provide a broader range of amplification, fine tuning of the amplification, and better isolation in the speedup circuit. As to providing a broader range of amplification and/or fine tuning the amplification, Ishimaru *teaches away* from this approach. Instead of trying to achieve a specific level of amplification, Ishimaru's proposed solution uses the uncontrolled level of amplification provided by the transistors in its speedup circuit. Ishimaru explains that using an uncontrolled gain is one of the *advantages* of its approach. A POSITA would therefore not be motivated to modify Ishimaru to add a current mirror to control the gain of the speedup circuit. In addition, Petitioner's proposed modifications could cause insufficient voltage

headroom for the proposed circuit to properly operate. Further, there is no reason why the functional circuit in Ishimaru, which works for its intended purpose, would need or benefit from allegedly improved isolation of a current mirror, if any.

Ultimately, Petitioner fails to articulate why the challenged claims are unpatentable under either ground. Institution should be denied.

II. Overview of the '101 Patent

A. Specification

The '101 patent discloses and claims an invention for “improved power amplifier systems” and for “improving power amplifier biasing.” EX1001-101P, 1:31-33. In particular, the '101 patent discloses improved power amplifier biasing that “can be used to compensate for a gain variation of the power amplifier.” *Id.*, 9:43-46. An exemplary embodiment of the '101 patent describes a bias circuit that receives an enable signal and generates a bias signal for the power amplifier. The bias circuit generates a control current using the enable signal, mirrors the control current to generate a correction current, and generates the bias signal based at least in part on the correction current.

Figure 4, shown below, depicts details of an exemplary power amplifier disclosed by the '101 patent.

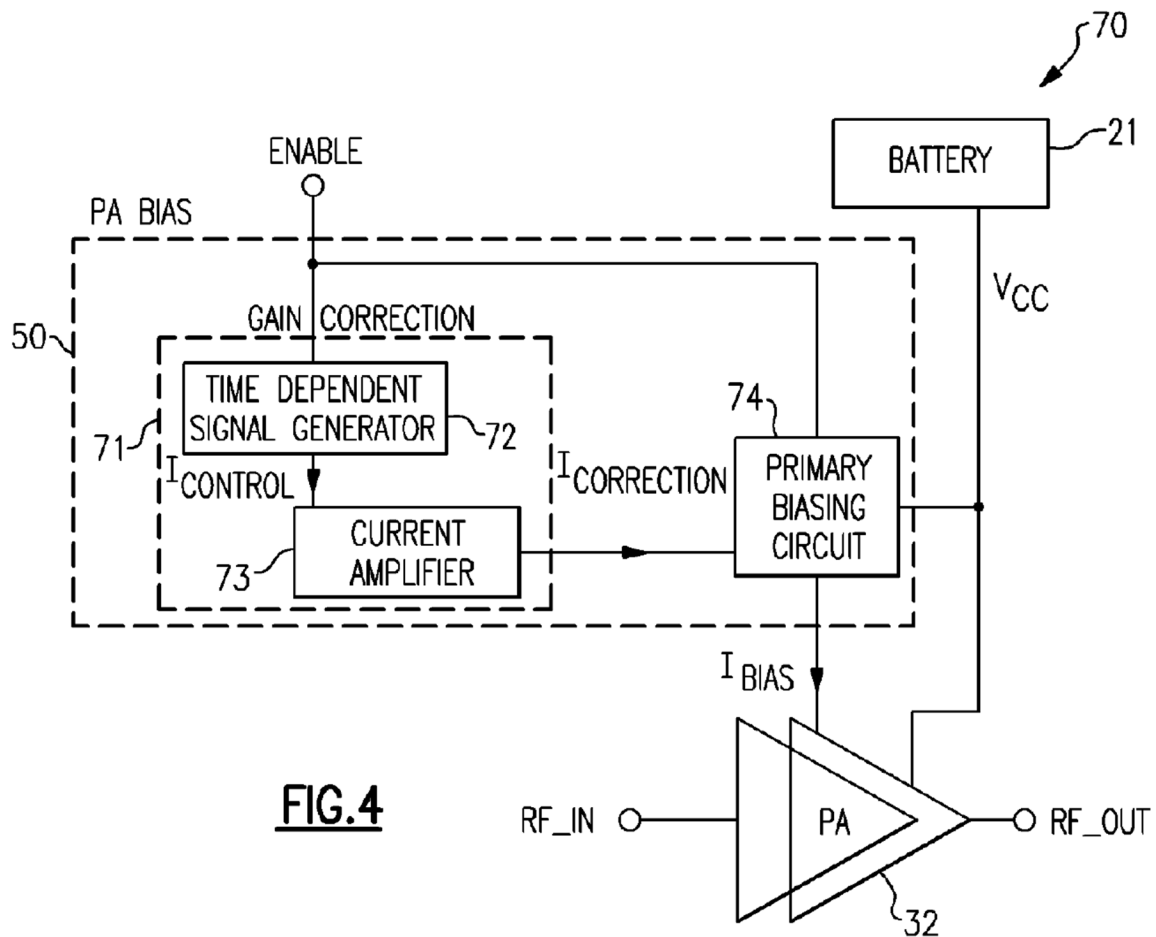


FIG. 4

EX1001-101P, Fig. 4.

As shown above, the power amplifier bias block 50 includes primary biasing circuit 74 and gain correction block 71. EX1001-101P, 9:13-15. Control block 72 generates a control current I_{CONTROL} based on an enable signal. *Id.*, 9:47-9:50. Control current I_{CONTROL} is provided to current amplifier 73 to generate a correction current $I_{\text{CORRECTION}}$. *Id.*, 9:50-53. The primary biasing circuit 74 generates a bias current I_{BIAS} based on the correction current $I_{\text{CORRECTION}}$. *Id.*, 10:8-13, Fig. 4.

Figure 5, shown below, depicts an exemplary circuit diagram of the power amplifier bias block 50 in Figure 4 of the '101 patent:

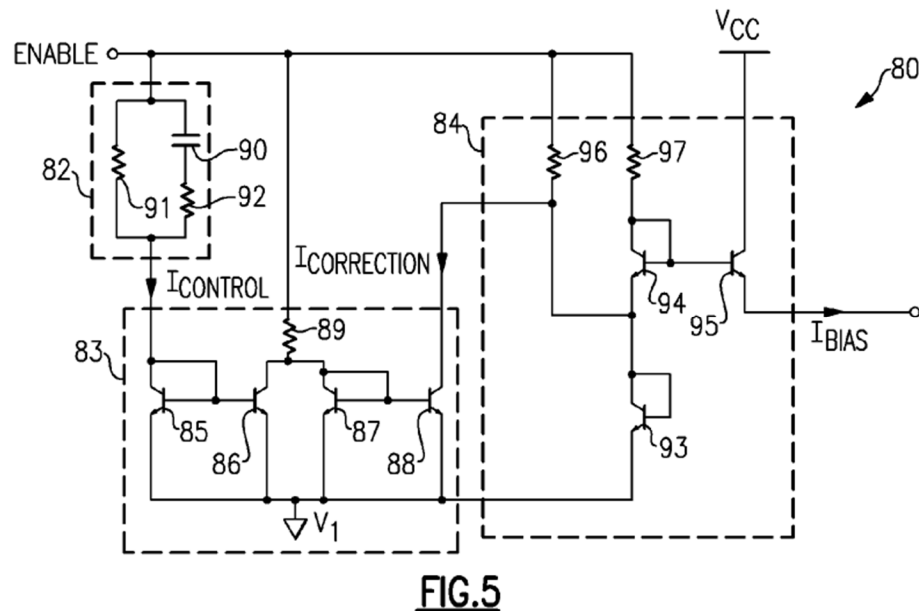


FIG.5

EX1001-101P, Fig. 5.

As shown above, the power amplifier bias block 80 includes “a resistor-capacitor (RC) network 82, a current mirror 83, and a primary bias circuit 84.”

EX1001-101P, 10:18-21. To generate the bias current I_{BIAS} , the RC network 82

first uses the enable signal to generate the control current $I_{CONTROL}$. *Id.*, 10:37-41.

Then, the current mirror 83 mirrors the control current $I_{CONTROL}$ to generate the

correction current $I_{CORRECTION}$. *Id.*, 10:62-11: 1. The correction current $I_{CORRECTION}$

is provided to the primary bias circuit 84. *Id.*, 11:46-59. Primary biasing circuit 84

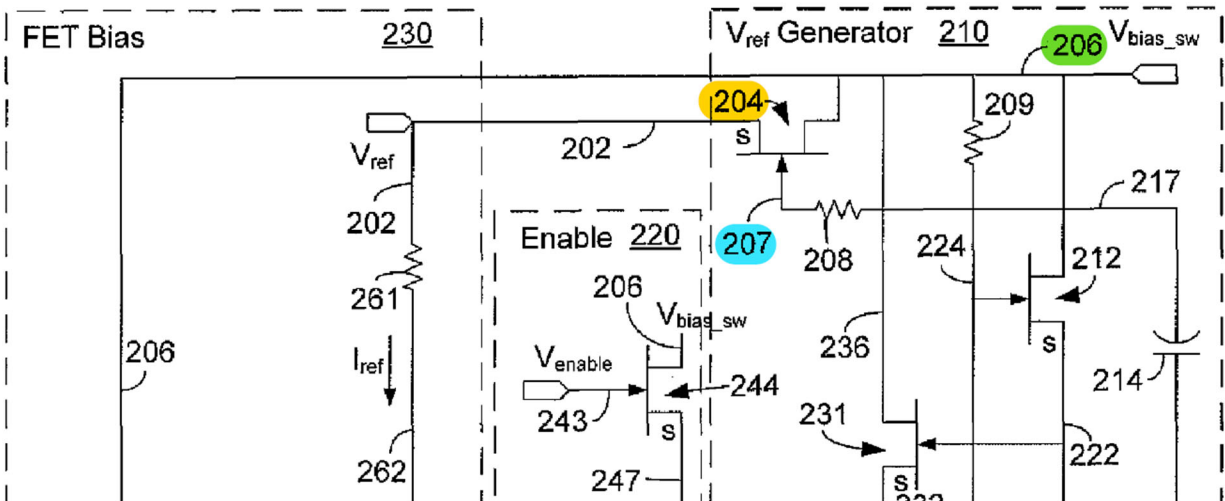
uses the correction current to generate a bias current I_{BIAS} for the power amplifier.

Id., 11:46-12:13.

B. File History

The application leading to the '101 patent was filed on May 10, 2012 and claims priority to a provisional application filed on May 13, 2011.

The originally filed claims, including application claim, were rejected by the Examiner in a Non-Final Office Action “as being anticipated by Alon” (USP7869775 (“Alon”) (EX2009)). EX1002-101FH, 88 (Office Action dated 8-2-2013, 2). Application claim 18 recited: “[a] method of biasing a power amplifier, the method comprising ... amplifying the control current using a current amplifier to generate a correction current[.]” EX1002-101FH, 34 (Application as Filed, 27). The Examiner stated that Alon discloses “a power amplifier/transceiver system as well as a method of biasing a power amplifier,” “meeting claims 1, 12-14, 18, and 22.” EX1002-101FH, 88-89 (Office Action dated 8-2-2013, 2-3). In particular, as shown in the annotated figure below, the Examiner contended that Alon’s “device 204 [in yellow below] can be read as the claimed current amplifier” configured “to amplify the control current [207, blue] to generate a correction current (206 [green]).” *Id.*, 89 (Office Action dated 8-2-2013, 3); EX2009-Alon, Fig. 2 (partial).



However, as shown in the excerpt from Alon's Figure 2 reproduced above, Alon's device 204 is a single transistor that is driven by signal 207 (blue). EX2009-Alon, Fig. 2, 5:48-53. The Examiner read signal 207 (blue) "as the claimed control current" applied to transistor 204, and transistor 204 "as the claimed current amplifier." EX1002-101FH, 89 (Office Action dated 8-2-2013, 3). The Examiner explained that transistor 204 was "configured to amplify the control current to generate a correction current (206)" highlighted green above. *Id.*, 88-89 (Office Action dated 8-2-2013, 2-3). Based on this reading of Alon's single transistor 204, the Examiner rejected then-pending application claims 1-3, 12-14, 18-20, 22, and 23-25.

Notably, however, the Examiner stated that dependent application claim 21—which depended from application claim 18—"would be allowable if rewritten in independent form[.]" *Id.*, 90 (Office Action dated 8-2-2013, 4). This claim

required, “wherein amplifying the control current further includes amplifying the control current *using a current mirror* of the current amplifier.” EX1002-101FH, 35 (Application as Filed, 28) (emphasis added). The Examiner thus indicated that Alon’s single transistor 204 was not a current mirror as claimed in then-pending application claim 21, and that this difference—the difference between Alon’s use of a single transistor and the ’101 patent’s use of a current mirror to amplify the control current—made application claim 21 an invention that was patentable over the cited prior art. *Id.*

Patent Owner responded by amending what became issued claims 1, 17, and 21 of the ’101 patent to require a current mirror type of current amplifier, for example by amending application claim 18 to require “amplifying the control current using a current mirror of a current amplifier to generate a correction current[.]” EX1002-101FH, 102 (Amendment and Response to Office Action dated 10-31-2013, 5 (underlining in original)).

The Examiner allowed the ’101 claims as amended in a Notice of Allowability dated December 24, 2013. EX1002-101FH, 124 (Notice of Allowability dated 12-24-2013), 2. Explaining reasons for allowance, the Examiner stated that the “prior art of record [e.g., Alon] considered individually or in combination, fails to fairly teach or suggest the claimed circuit comprising ...

‘...the current amplifier including a current mirror’ structurally and functionally interconnected with other limitations in the manner as cited in the claim.” *Id.*
(underlining in original).

III. Person Of Ordinary Skill In The Art

A person of ordinary skill in the art (POSITA) at the time of the invention of the '101 patent would have had at least a Bachelor's Degree in Electrical Engineering or a related field and at least two years of training or additional work experience in the area of RF electronics, or a related field.

IV. Claim Construction

The words of a claim “are generally given their ordinary and customary meaning” to a person of ordinary skill in the art at the time of the invention. *See Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) at 1312-1313. Petitioner “proposes that each claim term ... be given its plain and ordinary meaning in this proceeding, and that no specific construction of any claim term is required.”

Petition, 15. In the parallel ITC litigation¹, Petitioner and Patent Owner proposed claim constructions for the following terms in the parallel ITC litigation: “current mirror” (claims 1, 2, 10, 11, 17, 18, 20, 21, 22), “current amplifier configured to amplify the control current to generate a correction current,” (claims 1, 2, 10, 11,

¹ Certain Wireless Front-End Modules, Devices Containing the same, and Components Thereof, Inv. No. 337-TA-1413 (ITC) (July 16, 2024)

21, 22), “amplifying the control current using a current mirror of a current amplifier to generate a correction current,” (claims 17, 18, 20), and “time dependent signal generator configured to shape an enable signal of the power amplifier to generate a control current” / “shaping an enable signal using a time-dependent signal generator to generate the control current” (claims 1, 2, 10, 11, 17, 18, 20, 21, 22). Only the construction of “current mirror” is relevant to the patentability of the claims in view of Petitioner’s grounds.² For the reasons explained in further detail below, the Board should adopt Patent Owner’s proposed construction for “current mirror.”

A. **“current mirror” (’101 patent claims 1, 2, 10, 11, 17, 18, 20, 21, 22)**

Patent Owner’s Proposed Construction	Petitioner’s Proposed Construction
Plain meaning, which is “one or more circuits configured to mirror a current, which can be configured to achieve a target gain, having at least two transistors with their base or gate terminals tied together”	Plain meaning, which is “one or more circuits configured to mirror a current, which can be configured to achieve a target gain”

² The parties’ proposed constructions for the other claim terms are set forth in the Joint Claim Construction Chart in the parallel ITC litigation. EX1020-Joint_CC_Chart.

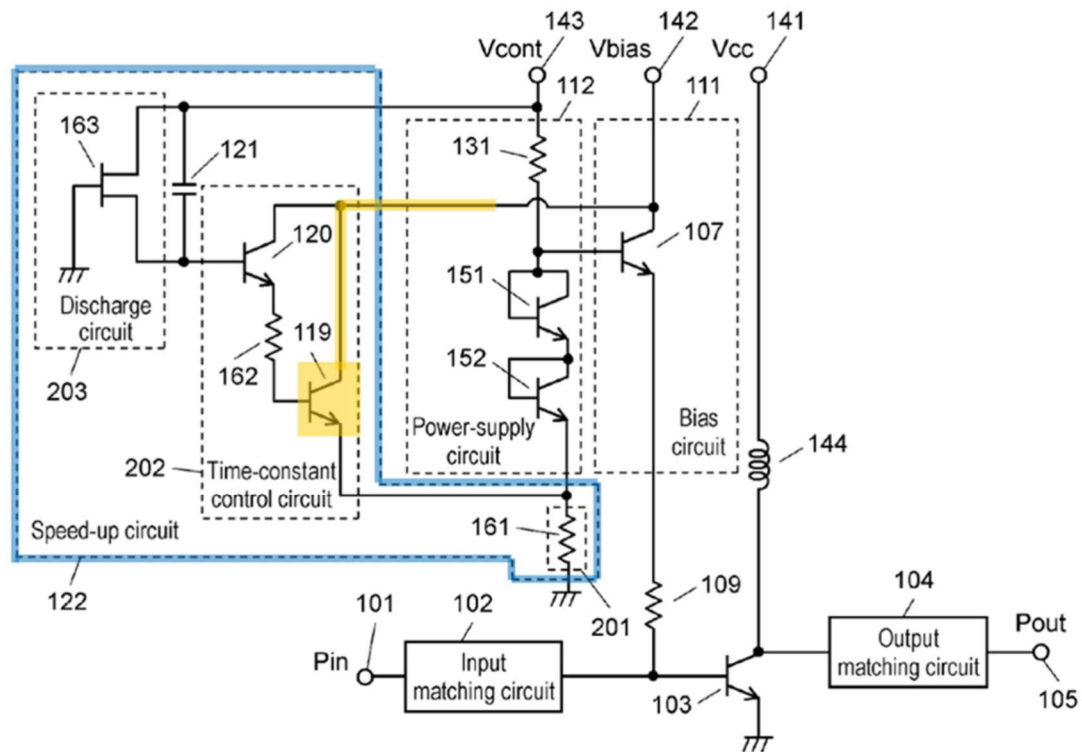
Petitioner and Patent Owner agree that the claimed “current mirror” comprises “one or more circuits configured to mirror a current, which can be configured to achieve a target gain.” EX1020-Joint_CC_Chart. Patent Owner's proposed claim construction makes clear that the claimed “current mirror” “[has] at least two transistors with their base or gate terminals tied together.” *Id.* Patent Owner's proposed construction is supported by the specification and file history of the '101 patent, the file history of the '563 patent (child patent to the '101 patent) as well as extrinsic evidence. Accordingly, the Board should adopt Patent Owner's proposed construction.

First, it is undisputed that that the claimed “current mirror” comprises “one or more circuits configured to mirror a current, which can be configured to achieve a target gain” EX1020-Joint_CC_Chart. The specification of the '101 patent, as well as extrinsic evidence, confirm that the claimed “current mirror” is configured “to achieve a target gain.” For example, the specification of the '101 patent unequivocally states: “[a]s used herein, the term current mirror can refer to current amplification circuits including a plurality of current mirrors combined (e.g., cascaded) **to achieve a target gain**” EX1001-101P, 11:42-45 (emphasis added); *see also id.*, 10:62-11:1, 11:39-45 (explaining that the “target gain” can be “any suitable gain” and can have any “suitable magnitude”). A POSITA would

have understood that a “target gain” is “achieved” by multiplying an input current by a suitable gain factor to produce an output current. *See* EX1026 (pp. 69-125)-Wentzloff_CC_Decl, ¶¶ 58-60. Extrinsic evidence further confirms a POSITA’s understanding that a “current mirror” is configured “to achieve a target gain.” For example, a textbook titled “Analysis and Design of Analog Integrated Circuits” (5th Ed. 2009) (hereinafter, “Gray”) explains that, in a “current mirror,” “the output current is equal to the input current multiplied by a desired current gain. If the gain is unity, the input current is reflected to the output, leading to the name *current mirror*.” EX2016-Gray, 251 (italics in original). Thus, a “current mirror” comprises “one or more circuits to mirror a current, which can be configured to achieve a target gain” Petitioner agrees.

Second, the file history of a child of the ’101 patent (the ’563 patent) confirms that the claimed “current mirror” requires “at least two transistors with their base or gate terminals tied together.” In particular, Patent Owner’s amendments during prosecution of the ’563 patent make this requirement clear. Specifically, the Examiner rejected application claim 14 (corresponding to issued claim 14) over USP8692619 to Wakita (EX2011). EX2008-563FH, 2-6 (Office Action dated 2-27-2017, 2-6). As shown below, Wakita discloses a speedup circuit 122 (blue), that includes a transistor 119 (gold):

FIG. 1



EX2011-Wakita (annotated). The Examiner contended that the collector current of transistor 119 (gold) corresponded to the claimed “correction current.” EX2008-563FH, 3 (Office Action dated 2-27-2017, 3). In response to the rejection, Patent Owner amended application claim 14 to recite: “*to mirror* the control current to generate a correction current” and argued that Wakita failed to disclose or suggest the claims as amended. EX2008-563FH, 16, 19-20 (Response to Office Action dated 5-16-2017, 4, 7-8) (emphasis added). Patent Owner, therefore, took the position that a single transistor (transistor 119) fails to disclose or suggest “mirroring” a control current. *Id.*, 19-20 (Response to Office Action dated 5-16-

2017, 7-8). In other words, Patent Owner argued that a current mirror *cannot* comprise a single transistor.

The Examiner agreed with Patent Owner that Wakita, and in particular a single transistor like Wakita's transistor 119, fails to disclose or suggest a current mirror. EX2008-563FH, 33-34 (Notice of Allowance, 2-3). In allowing the claims, the Examiner stated in the "reasons for allowance" that the prior art of record (including Wakita) "fails to fairly teach or suggest the claimed circuit comprising, among other limitations and unobvious limitations of '... and to mirror the control current to generate a correction current...' structurally and functionally interconnected with other limitations in the manner as cited in the claim." *Id.* (underlining in original). By emphasizing that the '563 patent claims, as granted, require "mirroring" a current, the Examiner thus confirmed that the claimed "current mirror" requires at least two transistors as distinct from the single transistor structure in Wakita. *Id.* Patent Owner's proposed construction—and its requirement of at least two transistors—is consistent with and required by this prosecution history. *See Phillips*, 415 F.3d at 1317 ("the prosecution history can often inform the meaning of the claim language by demonstrating how the inventor understood the invention and whether the inventor limited the invention in the course of prosecution").

terminal 206 connected to the alleged “correction current,” which Alon identified as “Vbias_sw.” EX2009-Alon, Fig. 2 (partial); 5:48-53.

Despite rejecting the independent claim, the Examiner stated that dependent application claim 21—which was dependent from application claim 18 and included the additional requirement of a “current mirror”—“would be allowable if rewritten in independent form[.]” EX1002-101FH, 90 (Office Action dated 8-2-2013, 4). The Examiner thus recognized a patentable distinction between a single field effect transistor, which the Examiner deemed unpatentable, and a current mirror for a current amplifier, which the Examiner found to be patentably distinct. *Id.*, 88-90 (Office Action dated 8-2-2013, 2-4).

Patent Owner amended what became issued claims 1, 17, and 21 to clarify that the current amplifier claimed in the '101 patent included a current mirror. Patent Owner explained in remarks accompanying this amendment that application claim 18 had “been amended to incorporate the limitations of original claim 21,” and that this amendment distinguished the invention claimed in the '101 patent from Alon and its single transistor type of current amplifier. EX1002-101FH, 99-103 (Amendment and Response to Office Action dated 10-31-2013, 2-6. The Patent Examiner agreed, allowing the '101 patent claims (as amended) in a Notice of Allowability. EX1002-101FH, 124-126 (Notice of Allowability dated 12-24-

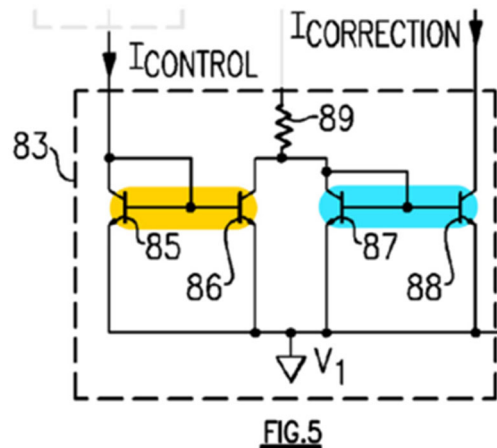
2013, 2-4). The Examiner explained in his “reasons for allowance” that the “prior art of record [e.g., Alon] considered individually or in combination, fails to fairly teach or suggest the claimed circuit comprising ... ‘...the current amplifier including a current mirror’ structurally and functionally interconnected with other limitations in the manner as cited in the claim.” *Id.*

By emphasizing that the ’101 patent claims, as granted, require a current mirror that is “structurally and functionally interconnected” in the manner the claims recite, the Examiner confirmed that the claimed “current mirror” requires at least two transistors as distinct from Alon’s single transistor structure. *Id.* Patent Owners’ proposed construction—and its requirement of at least two transistors—is consistent with and required by this prosecution history. *See Phillips*, 415 F.3d at 1317 (“the prosecution history can often inform the meaning of the claim language by demonstrating how the inventor understood the invention and whether the inventor limited the invention in the course of prosecution”).

Third, the specification of the ’101 patent supports that the claimed “current mirror” “[has] at least two transistors with their base or gate terminals tied together.” The specification uniformly describes and depicts the claimed “current mirror” as comprising at least two transistors with their base or gate terminals tied together. The specification describes the current amplification circuit as including

“a plurality of current mirrors combined (*e.g.*, cascaded) to achieve a target gain.”

EX1001-101P, 11:42-45. This is shown in Figure 5 (reproduced in relevant part below), which depicts a “current amplifier 83” as formed by two “current mirrors” (highlighted yellow and blue, respectively), each formed by a pair of transistors with their base terminals tied together:



Id., 11:7-45, Fig. 5 (partial). As shown in the excerpt of Figure 5 above, the bases of bipolar transistors 85 and 86 are connected by the trace highlighted in yellow, and the bases of bipolar transistors 87 and 88 are connected by the trace highlighted in blue. *Id.*

The Summary of the Invention in the '101 patent specification also explains that a first “current mirror” (*e.g.*, highlighted yellow in Figure 5 above) is formed from “a first bipolar transistor and a second bipolar transistor” having a signal line “electrically connected to a base of the first bipolar transistor and to a base of the

second bipolar transistor[.]” EX1001-101P, 1:65-2:19; *see also id.*, 11:10-15 (“The first NPN bipolar transistor 85 includes ... a base and a collector electrically connected to a base of the second NPN bipolar transistor 86”). Similarly, the second “current mirror” (*e.g.*, highlighted blue) is formed from “a third bipolar transistor” and “a fourth bipolar transistor” where “a base of the third bipolar transistor” is electrically connected “to a base of the fourth bipolar transistor[.]” *Id.*, 2:7-19; *see also id.*, 11:18-21 (describing “a base and a collector of the third NPN bipolar transistor 87” as “electrically connected ... to a base of the fourth NPN bipolar transistor 88”). A POSITA reading the specification of the ’101 patent would therefore conclude that the claimed “current mirror” has “at least two transistors with their base or gate terminals tied together.” EX1026 (pp. 69-125)-Wentzloff_CC_Decl, ¶¶ 63-64.

Fourth, extrinsic evidence supports Patent Owner’s proposed construction. For example, Steven M. Kaplan, “Electrical and Electronics Engineering Dictionary” (2004) (EX2022) defines a “current mirror” as “[a] circuit in which the current on one side is forced to be a replica of that of the other side” which is “[a]ccomplished, for instance, by the bases and emitters of two bipolar junction transistors being connected together.” EX2022-Kaplan, 159. Gray similarly describes a “current mirror” as at least “two transistors” having their

bases (bipolar) or gates (MOS) tied together. See EX2016-Gray, 253. Gray explains, for example, that “a bipolar version of this mirror” is shown in its “simplest form” in “Fig. 4.2” as “two transistors” “Q1” and “Q2” having their base terminals tied together (shown with yellow highlighting below):

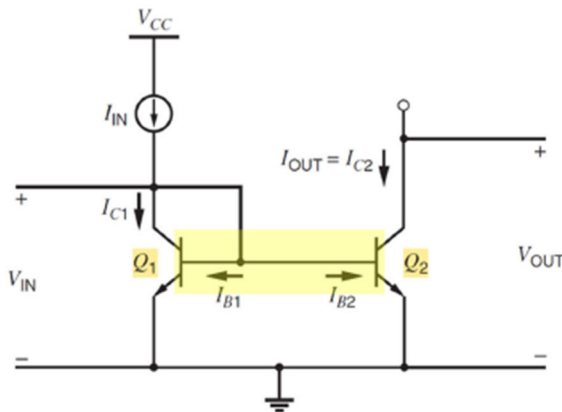


Figure 4.2 A simple bipolar current mirror.

EX2016-Gray, 253. Finally, Gray also defines “an MOS version of the simple current mirror” in “Figure 4.4” as transistors “M1” and “M2” having their gates tied together (shown with yellow highlighting below):

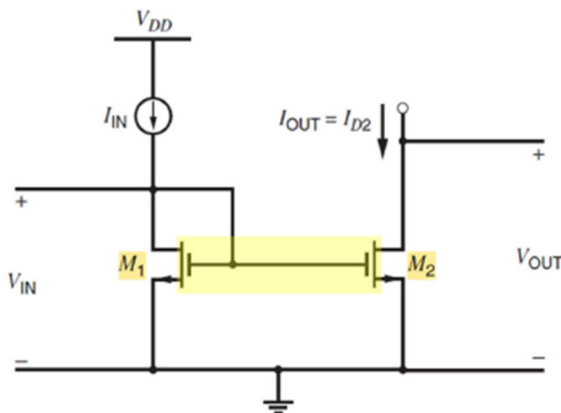


Figure 4.4 A simple MOS current mirror.

Id., 255-56. In each case, whether bipolar or MOS, the key attribute of a “current mirror” is that it has at least two transistors with their base (bipolar) or gate (MOS) terminals tied together. Thus, the extrinsic evidence further supports Patent Owner's proposed construction.

V. Petitioner Is Not Reasonably Likely to Prevail on Either Ground

Institution should be denied because Petitioner has not established a reasonable likelihood of prevailing on any ground. 35 U.S.C. § 314(a).

A. Ground 1: Petitioner Has Not Shown Obviousness Over Ishimaru

Petitioner failed to demonstrate a reasonable likelihood of prevailing on Ground 1.

1. Claim 1 is Nonobvious over Ishimaru

Claim 1 is nonobvious over Ground 1 because Ishimaru does not disclose a “current mirror,” a “control current,” or an “enable signal.”

a. Ishimaru does not disclose “a current mirror”

Petitioner alleges that Ishimaru's transistor 119 is a “current mirror” as recited in claim 1. Petition, 47-51. However, transistor 119 is not a current mirror under any party's proposed construction for the term.

Transistor 119 is not a current mirror under Patent Owner's proposed construction—“one or more circuits configured to mirror a current, which can be configured to achieve a target gain, having *at least two transistors with their base*

or gate terminals tied together.” See Section IV.A. Transistor 119 is a single transistor, and thus not “at least two transistors,” let alone two or more transistors “with their base or gate terminals tied together,” as construed by Patent Owner. EX2006-WentzloffRpt, ¶¶109, 168.

Transistor 119 is also not a current mirror under any party's proposed construction, which all require “one or more circuits configured to *mirror a current*, which can be *configured to achieve a target gain*.” Transistor 119 is incapable of mirroring a current and cannot be configured to achieve a target gain.

Transistor 119 is incapable of mirroring a current, and thus is not the claimed “current mirror” under any party's proposed construction, for the following reasons.

First, transistor 119 is a bipolar junction transistor (BJT), which is incapable of generating an output (collector current) that mirrors its input (base current). As Petitioner acknowledges, transistor 119 has a beta (β) that is the ratio between its output (collector current) and input (base current). Petition, 50. For a circuit component to mirror, the ratio between its output and input should remain constant. For example, if its input rises in value over time, while the output/input ratio decreases in value over that same period of time, then the output may actually decrease over that time period, instead of mirroring the input's rise. Turning to

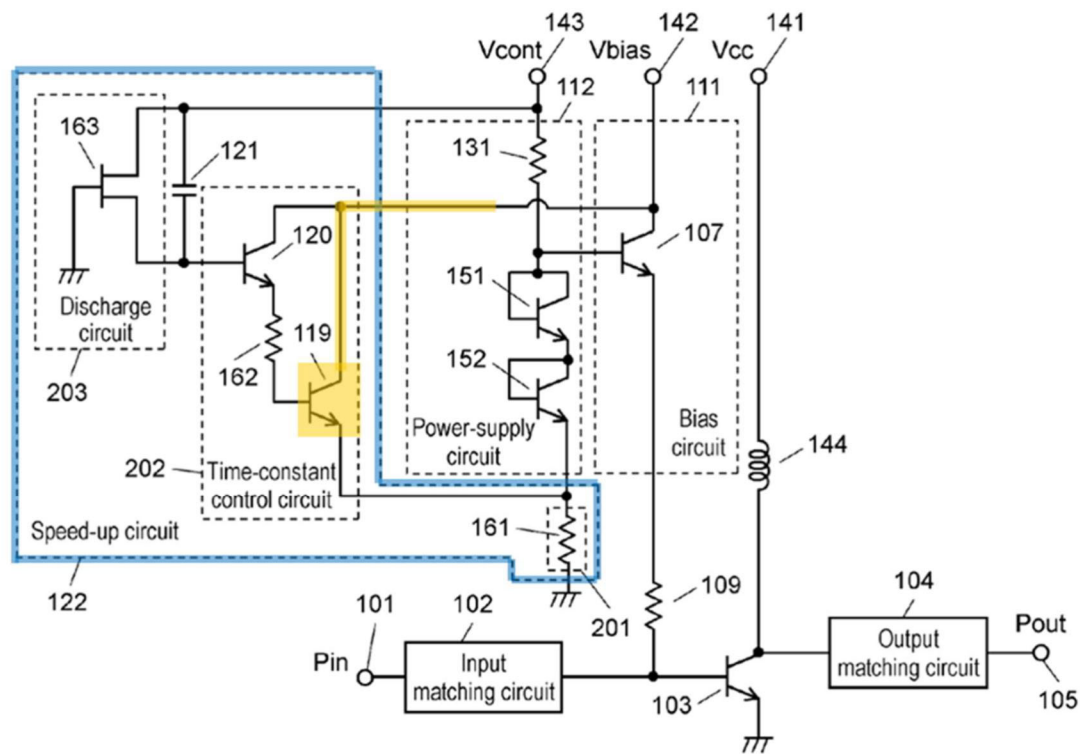
transistor 119, rather than remain fixed in value, β of a BJT like transistor 119 varies widely, meaning the size of its output relative to its input varies widely. Transistor 119's β varies due to manufacturing variability, meaning it varies between different circuits and even between different transistors within the same circuit. EX1006-Harrison, 53-56 (“Gain [of a BJT] is a variable parameter that is difficult to control in processing and manufacturing. As a result, manufacturers normally provide only a minimum gain specification. The particular process will yield a range of gains, where any one device's value may typically range from, say, 100 to 350....Devices with higher gains, or with gains close together, may cost more. Small-signal transistors tend to have gains ranging from around 60 to several hundred, whereas power transistors tend to have much lower gains, typically less than 50.”). Transistor 119's β also varies due to operating conditions such as the value of the collector current, the value of the base current, and the operating temperature. *Id.*, (“To be meaningful, the gain should be specified at a particular collector-emitter voltage (V_{CE}), collector current (I_C), base current (I_B), and temperature.”), 56 (Fig. 4.6 “Showing how temperature affects h_{FE} [β]); EX2016-Gray, 24 (Fig. 1.15); EX1012-Gilbert, 242 (describing β as “poorly-controlled” and “not very linear”); EX2006-WentzloffRpt, ¶¶79-80, 169; *see also id.*, 81-90.

Second, the file history of US9717563 (“the ’563 patent”), which shares the same specification as and claims priority to the ’101 patent through a series of continuation applications, shows that a single BJT like transistor 119 is not configured to mirror a control current to generate a correction current.

During prosecution of the ’563 patent, both the Patent Owner and the Examiner agreed that a single BJT like transistor 119 is not configured to mirror. In particular, the Examiner rejected application claim 14 (corresponding to issued claim 14) over USP8692619 to Wakita (EX2011), while not rejecting application claim 18, reciting a “current amplifier [that] includes a current mirror configured to generate the correction current by mirroring the control current,” over Wakita or any other references. EX2008-563FH, 3-6 (Office Action dated 2-27-2017, 2-5). The Examiner contended that speedup circuit 122 (blue) constitutes the claimed “gain correction circuit,” that the output of block 202, which is the collector current of a transistor 119 (gold) in speedup circuit 122, constitutes the claimed “correction current” generated by the “gain correction circuit,” and that transistor 119 (gold) constitutes a “current amplifier . . . configured to generate the correction current by amplifying the control current.” *Id.*, 4 (“a gain correction circuit (122 of Fig. 1 can be read as the claimed circuit OR at least it is functionally equivalent to it) configured to generate (via output of 202 of Fig. 1) a correction current...”), 5

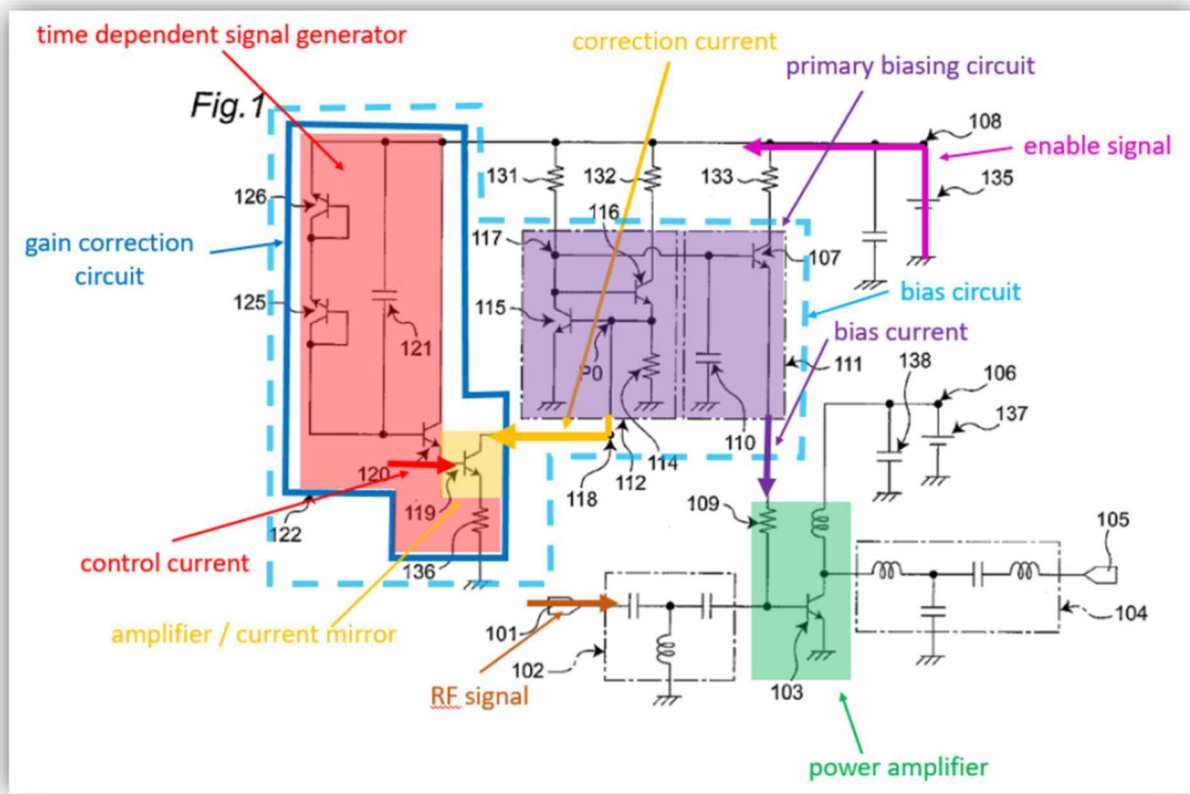
(“current amplifier (120 and/or 119 of Fig. 1 can be read as the claimed amplifier”), 6.

FIG. 1



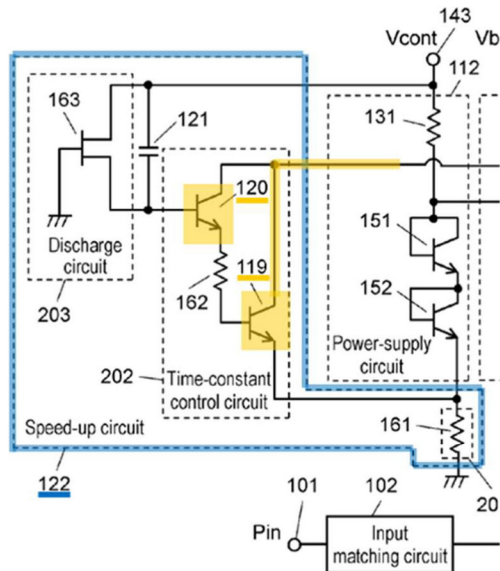
EX2011-Wakita, Fig. 1 (annotated). Notably, by not rejecting application claim 18 over Wakita, the Examiner found that transistor 119, despite allegedly generating the correction current by amplifying the control current, did *not* constitute “a *current mirror* configured to generate the correction current by mirroring the control current,” as recited in application claim 18. Likewise, Petitioner contends that the speedup circuit 122 of Ishimaru Figure 1 constitutes a “gain correction circuit,” that the collector current of transistor 119 in speedup circuit 122

constitutes the claimed “correction current” generated by the “gain correction circuit” and that transistor 119 is an amplifier.



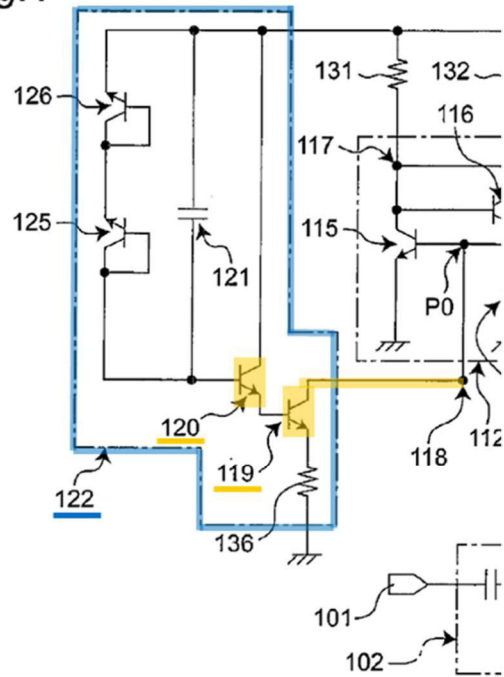
Petition, 32 (EX1004-Ishimaru, Fig. 1 as annotated by Petitioner). That Wakita’s Figure 1 (on the left) and Ishimaru’s Figure 1 (on the right) include the same circuit with the same circuit elements—a speedup circuit 122 (blue) including cascaded BJTs 119 and 120 (gold), where the emitter of transistor 120 is connected to the gate of transistor 120 and the collector of transistor 119 is the output of speedup circuit 122—is no coincidence.

FIG. 1



Wakita

Fig.1



Ishimaru

EX2011-Wakita, Fig. 1 (cropped, annotated); EX1004-Ishimaru, Fig. 1 (cropped, annotated). Wakita describes Ishimaru as prior art, and Wakita's invention was directed to improving upon Ishimaru. *See, e.g.,* EX2011-Wakita, 1:66-2:59.

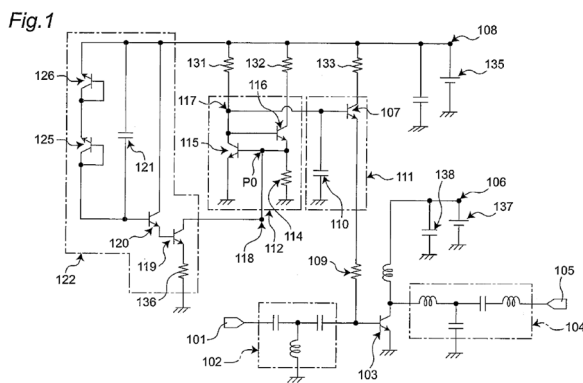
Responding to the rejection over Wakita, Patent Owner amended application claim 14 to recite that the gain correction circuit is configured "to mirror the control current to generate a correction current" and argued that Wakita failed to disclose or suggest the claims as amended. EX2008-563FH, 16, 19-20 (Response to Office Action dated 5-16-2017, 4, 7-8). Patent Owner thus argued that Wakita's speedup circuit 122, including its transistor 119, fails to teach or suggest

“mirror[ing] the control current to generate a correction current,” as recited in the claims as amended. Patent Owner's statements during prosecution of the '563 patent directly contradict Petitioner's contention that Ishimaru's transistor 119, of speedup circuit 122, mirrors a control current to generate a correction current. Further, the Examiner agreed with Patent Owner, stating in the “reasons for allowance” that the prior art of record “fails to fairly teach or suggest the claimed circuit comprising, among other limitations and unobvious limitations of ‘... and to mirror the control current to generate a correction current...’ structurally and functionally interconnected with other limitations in the manner as cited in the claim.” *Id.*, 33-34 (Notice of Allowance, 2-3) (underlining in original).

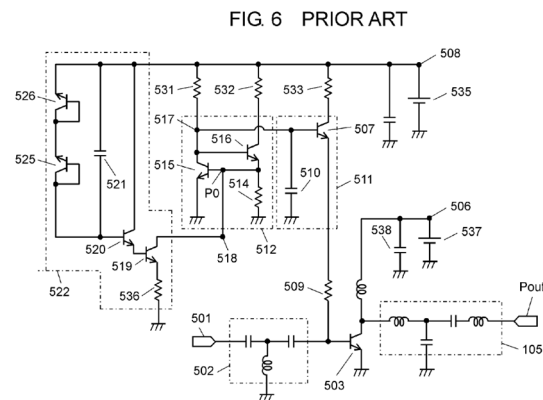
Because claim 14 was allowed over the same circuit feature—transistor 119 of speedup circuit 122—that Petitioner now contends is the claimed “current mirror,” the file history of the '563 patent makes clear that Petitioner's argument is mistaken. EX2006-WentzloffRpt, ¶¶99-101, 169.

In addition, during prosecution of the '563 patent, the Examiner considered the same circuit of Ishimaru Figure 1 that Petitioner relies on for its grounds, and allowed the claims over that circuit. As an initial matter, Ishimaru itself was disclosed and considered by the Examiner during prosecution of the '563 patent. EX2008-563FH, 36 (List of References Considered by Examiner signed 7-12-

2017). Moreover, as discussed above, the Examiner rejected the pending claims over Wakita. EX2008-563FH, 3-6 (Office Action dated 2-27-2017, 2-5). Wakita cites and describes Unexamined Japanese Patent Publication No. 2009-200770, which was filed as Japanese Patent Application No. 2008-39735 to which Ishimaru claims priority. EX2011-Wakita, 1:37-38 (“Unexamined Japanese Patent Publication No. 2009-200770 [to Ishimaru] (hereinafter PTL 1)”), 1:47 (“FIG. 6 illustrates a circuit diagram disclosed in PTL 1.”), Fig. 6. Wakita’s Figure 6 depicts the *exact same circuit*—with the same components connected in the same configuration to form the same subcircuits—as Ishimaru Figure 1, as can be seen in a side-by-side comparison of the figures:



EX1004-Ishimaru, Fig. 1



EX2011-Wakita, Fig. 6

Thus, Wakita, which was reviewed by the Examiner to form the basis of prior art rejections, discloses the exact same circuit, that forms the primary basis for this Petition. As noted above, the Examiner in the “reasons for allowance” found that

the prior art of record, including Wakita and Ishimaru, “fails to fairly teach or suggest the claimed circuit comprising, among other limitations and unobvious limitations of ‘... and to mirror the control current to generate a correction current...’ structurally and functionally interconnected with other limitations in the manner as cited in the claim.” *Id.*, 33-34 (Notice of Allowance, 2-3) (underlining in original). Thus, the Examiner found that the same circuit Petitioner relies upon, in Ishimaru’s Figure 1, did not teach or suggest a current mirror, contrary to Petitioner’s argument. EX2006-WentzloffRpt, ¶¶95-98, 169.

In addition to being incapable of mirroring a current, transistor 119 cannot be configured to achieve a target gain, and thus is not the claimed “current mirror” under any party’s proposed construction. Petitioner contends that “[t]he gain of transistor 119 can be configured to a target value by designing the voltage and current biasing of the transistor 119 (within the constraints of the circuit), such that a β in a range, *e.g.*, of about 60 to 150 or more, can be achieved.” Petition, 50-51. However, transistor 119 cannot actually be configured to achieve a target β within its range, which Petitioner concedes is quite large, varying from, according to Petitioner, as low as “about 60” to “150 or more.” *Id.* A BJT, like transistor 119, has a large range of potential values that are defined by the BJT manufacturing process. *See, e.g.*, EX1015-Illingworth, 38 (“ β is always greater than unity and

practical values up to 500 are used.”); EX1014-Grebene, 172 (“ β in the range of 100-200”). A transistor’s β is a function of processor parameters like the doping densities of the materials it is made from, where “[t]ypical values of β_F for npn transistors in integrated circuits are 50 to 500, whereas lateral pnp transistors [] have values 10 to 100.” EX2016-Gray, 12 (equation 1.48). Furthermore, normal manufacturing variations can significantly impact the actual beta value of any particular BJT. *See* EX1006-Harrison, 53-56 (“Gain is a variable parameter that is difficult to control in processing and manufacturing. As a result, manufacturers normally provide only a minimum gain specification. The particular process will yield a range of gains, where any one device’s value may typically range from, say, 100 to 350. ... Devices with higher gains, or with gains close together, may cost more. Small-signal transistors tend to have gains ranging from around 60 to several hundred, whereas power transistors tend to have much lower gains, typically less than 50.”); EX1012-Gilbert, 243 (“ β increases with V_2 due to base-width modulation, and in the customary BJT model would be exactly doubled when the collector bias voltage, VCB (roughly, V_2), is equal to the forward Early voltage, VAF.”); *see also* EX2016-Gray, 24 (Figure 1.15); EX1006-Harrison, 56 (Figure 4.6). Notably, Petitioner has admitted in the parallel ITC litigation that the ability to control Ishimaru’s transistor 119’s β value is “poor[]” and that the

“configurability” of Ishimaru’s transistor 119’s β is “limited,” which is the opposite of being configurable to target a specific β value. EX2010-InvalidityContentions, 48 (“Ishimaru’s circuit is constrained by the limited configurability of the β (amplification factor) of transistors 119 and 120....While the β values provide amplification, and, for transistor 119 provide a mirror ratio, that mirror ratio is ‘not very linear’ and ‘poorly-controlled’”). Because transistor 119 cannot be manufactured, designed, and/or operated to have a targeted and desired β value from within its range, transistor 119 cannot be configured to achieve a target gain, and is thus not a “current mirror” under any party’s proposed construction of the term. EX2006-WentzloffRpt, ¶¶110-112, 170; *see also id.*, ¶¶113-114.

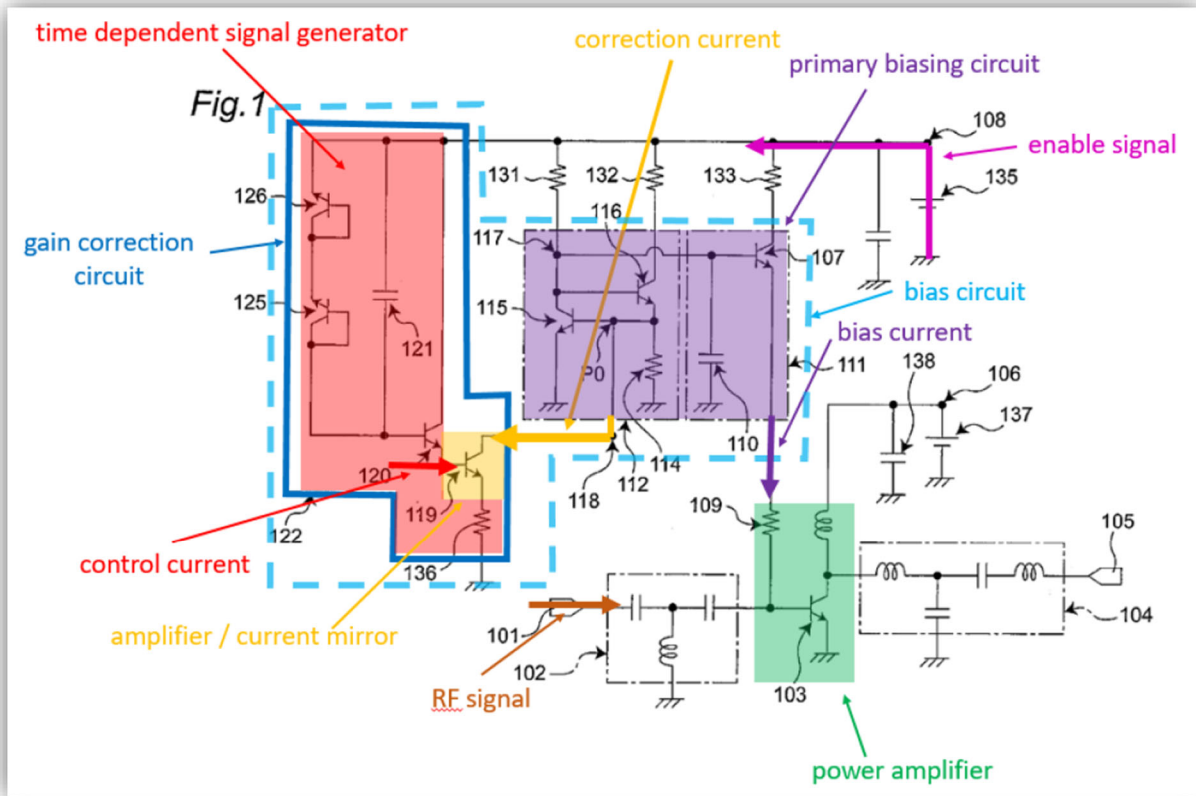
b. Ishimaru does not disclose “a control current”

Petitioner alleges that the current applied to the base of Ishimaru’s transistor 119 is the claimed control current. Petition, 40. As the ’101 patent explains, a control current input to a current mirror will control the output such that the output mirrors the input with a *target* amount of gain, rather than just a variable, unknown, uncontrolled amount of gain. *See* EX1001-101P, 11:40-45 (“the current mirror 83 is configured to amplify the control current I_{CONTROL} by a factor ranging between about 5 to about 50, for example, about 10. As used herein, the term

current mirror can refer to current amplification circuits including a plurality of current mirrors combined (e.g., cascaded) to achieve a target gain”). Contrary to Petitioner’s assertion, however, transistor 119’s base current cannot control transistor 119’s collector current. As explained above in Section V.A.1.a, the ratio between transistor 119’s collector current and base current, denoted β , varies widely both due to manufacturing variability and based on operating conditions. As such, the alleged correction current, rather than being controlled by the alleged control current as Petitioner alleges, is actually unknown and unpredictable, and thus “uncontrolled.” *See* EX1012-Gilbert, 244. As such, Ishimaru does not disclose a “control current” as recited in claim 14. EX2006-WentzloffRpt, ¶¶91-93, 161. Furthermore, Petitioner does not allege that a control current would have obvious over Ishimaru alone or in view of any other prior art references.

c. Ishimaru does not disclose “an enable signal”

Petitioner alleges that “the control voltage from control voltage source 135 at bias terminal 108” is the claimed enable signal. Petition, 39.



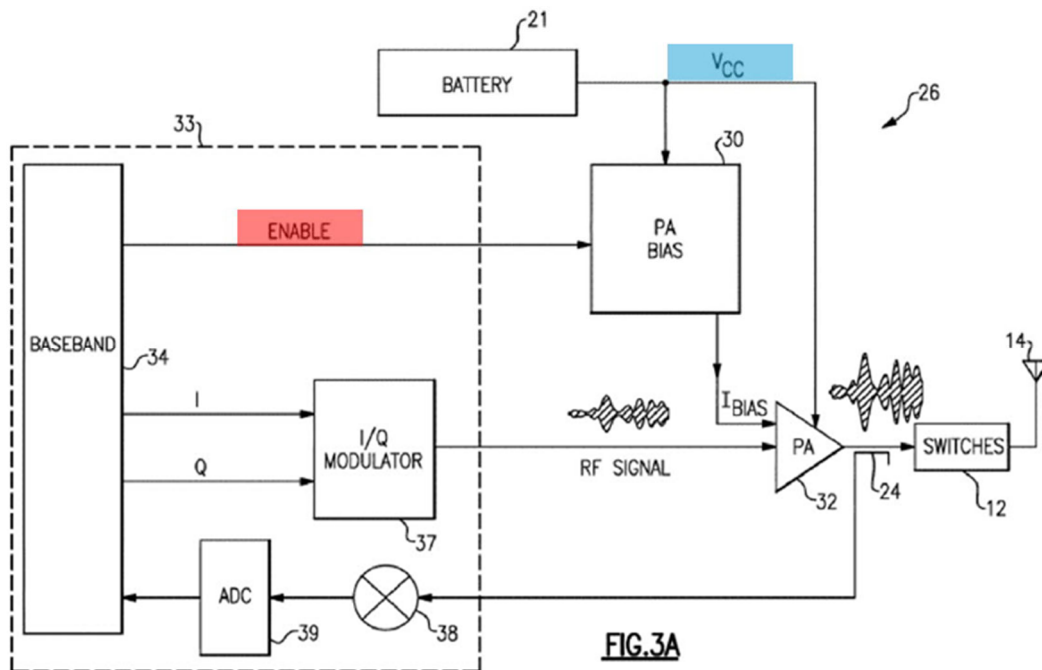
Id. (EX1004-Ishimaru, Fig. 1 as annotated by Petitioner). However, Ishimaru's control voltage source 135 is a power source, which is distinct from, and thus does not constitute, an enable signal.

A POSITA would understand that control voltage source 135 is a power source. Control voltage source 135 is depicted in Figure 1 using a circuit symbol ($\frac{\perp}{\text{T}}$) that, as would have been understood by a POSITA, represents a power source. EX2017-Thomas, 19 (Figure 2-6); EX2006-WentzloffRpt, ¶¶63, 160. Ishimaru's use of this symbol to denote a power source is confirmed by its use of the same circuit symbol to represent "DC power source 137." EX1004-Ishimaru,

¶42, Fig. 1. A power source, like power source V_{CC} described in the '101 patent, can be a battery or can be provided by a voltage regulator powered by a battery. EX1001-101P, 7:12-16 (“Although FIG. 3A illustrates the battery 21 directly generating the power high voltage V_{CC} , in certain implementations the power high voltage V_{CC} can be a regulated voltage generated by a regulator that is electrically powered using the battery 21.”). EX2006-WentzloffRpt, ¶¶69, 160. Petitioner states that Ishimaru's control voltage source 135 “controls turn-on and turn-off of power amplification.” Petition, 39 (citing EX1004-Ishimaru, ¶24). But this description tacitly concedes that control voltage source 135 is a power source and thus can turn on and off the power supplied to the associated circuitry. As explained below, a power source is not an enable signal.

An enable signal is a specific circuit feature distinct from a power source. An enable signal is an electrical signal for activating an associated system or circuit, that separately has a power source for supplying power to the system or circuit. See EX2018-HMC7748, 1 (Analog Devices datasheet “Functional Block Diagram” showing a pin for an enable signal (“EN”) separate from power source pins (“12V,” “28V”)); EX2006-WentzloffRpt, ¶¶71, 160. An enable signal can be in a high state or a low state, for the purpose of signaling that the system or circuit should be enabled or disabled (activated or deactivated). Typically, an enable

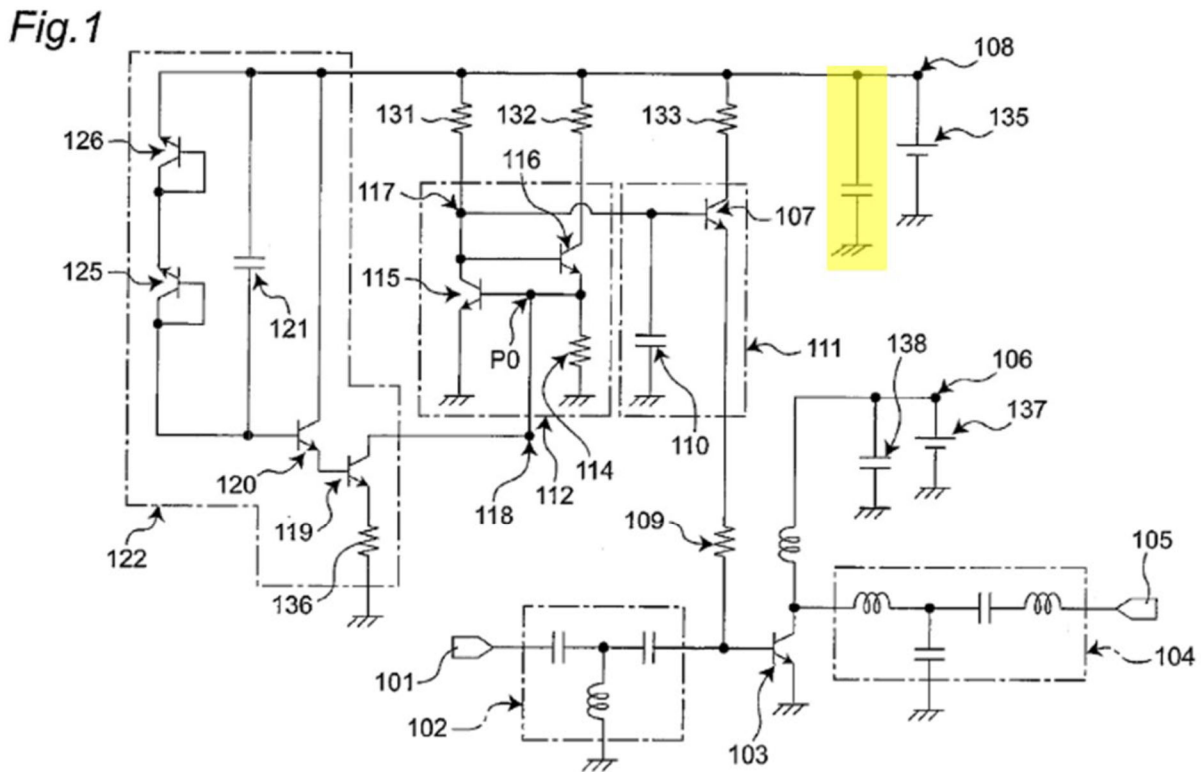
signal is sent by a processor that controls or coordinates the system or circuit. This distinction between an enable signal and power source is consistent with and supported by the '101 patent, which describes a power amplifier bias block that “can receive an enable signal ENABLE [red] from the baseband processor 34 *and* a battery or power high voltage V_{CC} [blue] from the battery 21.” EX1001-101P, 7:8-10; *see also id.*, 7:10-19, 8:9-28, 9:13-28, 10:18-26, 11:46-67, Figs. 3A, 3B, 4, 5.



EX1001-101P, Fig. 3A (annotated). EX2006-WentzloffRpt, ¶¶65, 69-70, 160.

Not only do an enable signal and power source serve different functions in a circuit, but they also operate differently, such that a power source cannot function as an enable signal. A power source switches states relatively slowly as compared

to, for example, an electrical signal sent by a baseband process. When switching between powered-on and powered-off states, the capacitance at the power source itself and from components connected to it slows down how quickly it can power on and power off. Notably, Ishimaru depicts control voltage source 135 as connected to a capacitor (highlighted), which will further slow down how quickly control voltage source 135 can rise to power on and fall to power off.

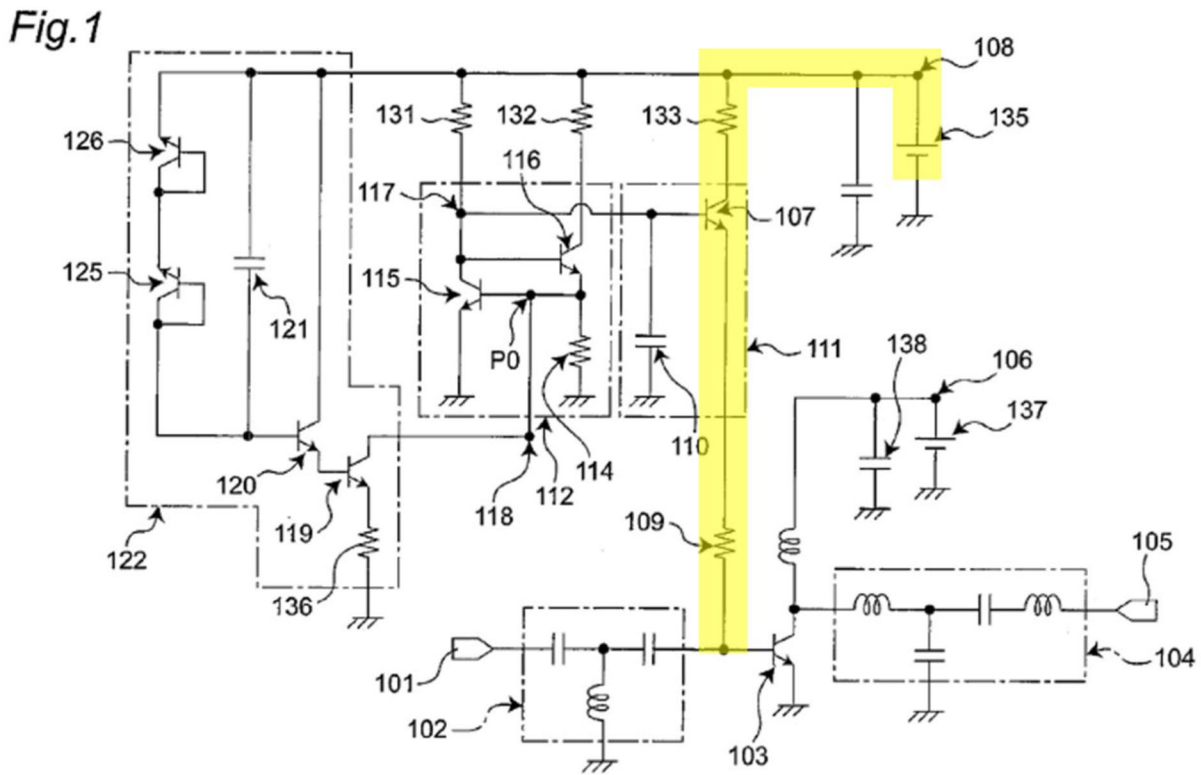


EX1004-Ishimaru, Fig. 1 (highlighted). A POSITA would have understood that a power source, like Ishimaru's control voltage source, turns on and off too slowly to be used as an enable signal. For example, if a power source is turned off (for

example, to place a subsequent circuit in a “0” state) and then, before the voltage output from the power source falls below a certain level, turned back to on (to place the subsequent circuit in a “1” state), components powered by that power source would not be completely powered off during the transition, which can result in the circuit powering up from an unknown state and incorrectly conveying a “1” state instead of a “0” state in the subsequent circuit. EX2006-WentzloffRpt, ¶¶65-66, 160. In addition, a control voltage source powers on and off too slowly to pulse a power amplifier in a wireless transmitter, as described in the '101 patent. EX1001-101P, 4:15-17 (“the power amplifier bias block can receive an enable signal that can be used to enable or disable the power amplifier so as to *pulse* the power amplifier’s output”). By contrast, an enable signal allows a baseband processor to efficiently control a power amplifier in a wireless transmitter, which is especially beneficial for complex systems with multiple power amplifiers for different wireless communications, such as Wi-Fi, WLAN, GSM, CDMA, W-CDMA, LTE, or EDGE. EX1001-101P, 5:29-40, 9:23-28 (“the enable signal ENABLE can be *selectively controlled* so as to *pulse* the output of the power amplifier”), 7:8-19 (“[t]he power amplifier bias block 30 can receive an enable signal ENABLE from the baseband processor 34 and a battery or power high voltage V_{CC} from the battery 21 ...”), Fig. 3A (depicting power amplifier bias

block 30 receiving an enable signal ENABLE from baseband processor 34). By using an enable signal to switch each power amplifier between a transmitting and non-transmitting state quickly, the other power amplifiers in the same system would not unintentionally be enabled at the same time and inadvertently transmit unwanted signals, thereby degrading performance. Unlike an enable signal that enables and disables a power amplifier, a voltage source that turns the entire power amplifier on and off would be too slow to accurately pulse the power amplifier's output. EX2006-WentzloffRpt, ¶¶67, 160.

An enable signal also differs from a power source in that they have markedly different current needs. By performing a signaling function, specifically to signal whether a system or circuit should be enabled or disabled, an enable signal only needs a relatively small amount of current. By contrast, for Ishimaru's circuit to work, the current from control voltage source 135 should be relatively high, as it powers the bias current to the power amplifier transistor 103. The bias current to the power amplifier transistor 103 has to come from voltage source 135 through transistor 107, as highlighted in Figure 1 below.



EX1004-Ishimaru, Fig. 1 (highlighted). That is, the control voltage source 135 has to supply the full bias current to the power amplifier transistor 103, which is why Ishimaru uses a power source to provide sufficient current. In contrast, in the '101 patent, the bias current is sourced from a separate power supply (V_{CC}) that can remain always on and supply sufficient current to the power amplifier, allowing for a separate, low-current enable signal ENABLE to control transistor 95.

As such, Ishimaru does not disclose an “enable signal” as recited in claim 14. Furthermore, Petitioner does not allege that an enable signal would have been obvious over Ishimaru alone or in view of any other prior art references.

2. Claims 17 and 21 are Nonobvious over Ishimaru

Claims 17 and 21 are nonobvious over Ground 1 for the same reasons discussed above with respect to claim 1 in Section V.A.1.

3. Claims 2, 10, 11, 18, 20, and 22 are Nonobvious over Ishimaru

Because Ishimaru does not render obvious claims 1, 17, and 21 as explained above, it also does not render obvious claims 2, 10, 11, 18, 20, and 22, at least based on their dependency on claim 1, 17, or 21.

B. Ground 2: Petitioner Has Not Shown Obviousness Over Ishimaru and Harrison

Petitioner failed to demonstrate a reasonable likelihood of prevailing on Ground 2. Petitioner asserts Ground 2 only to address the term “current mirror” in claims 1, 17, and 21. Petitioner, 62. To address these limitations, Petitioner contends it would have been obvious to modify Ishimaru’s speedup circuit 122 with Harrison’s current mirror, as shown below. *Id.*, 69-70.

voltages or amplification. Instead, Ishimaru's circuit is already able to "suppress distortion" of an amplification signal without the drawbacks and problems of using a temperature sensor. *Id.* In fact, one of the benefits of Ishimaru's circuit is that it is able to achieve its benefits without needing a specific level of amplification, hence Ishimaru's use of an uncontrolled, unpredictable, and unknown level of amplification as provided by transistors 119 and 120. As such, a POSITA would not have been motivated to adjust or tune that level of amplification, and thus would not be interested in this purported benefit of a broader range of amplification, and thus would not modify Ishimaru's circuit as Petitioner proposes.

In particular, a current mirror is contrary to the purported technical solution and benefit as disclosed by Ishimaru. A current mirror provides a level of amplification that is controlled in order to achieve a target gain. By contrast, as discussed in Section V.A.1, Ishimaru uses BJT transistors (like transistors 119 and 120) that provide an uncontrolled, unpredictable, and variable level of current amplification—the opposite of a controlled level of amplification, as provided by a current mirror. Ishimaru's use of an uncontrolled level of amplification is actually one of the advantages of Ishimaru's proposed solution, which improves upon power amplifier biasing techniques that instead used controlled amplification. Ishimaru describes the prior art as controlling the biasing of a power amplifier

based on a sensed temperature. EX1004-Ishimaru, ¶4 (describing USP4924194 as disclosing “a circuit in which heat generation of an amplifier transistor is detected by a temperature sensing element (PIN diode) thermally coupled to the amplifier transistor and the detection result is reflected on a bias voltage of the amplifier transistor”). Ishimaru explains the drawbacks of using a temperature sensor to control the biasing of a power amplifier. *Id.*, ¶5 (“close placement of the temperature sensing element and the amplifier transistor may cause an amplification signal to leak to the temperature sensing element, with a possibility of causing unexpected malfunction.”). Instead of trying to control the bias current to achieve a specific level of amplification based on a sensed temperature, Ishimaru’s proposed solution removes the temperature sensor, thus avoiding the drawbacks of having such a sensor, and no longer requires a specific level of amplification, instead using the uncontrolled level of amplification provided by transistors 119 and 120. EX1004-Ishimaru, Abstract (“Accordingly, in the invention, it becomes possible to suppress distortion increases of an amplification signal due to heat generation at the start time without using any temperature sensing element.”), ¶¶7, 12, 24.

As such, Ishimaru teaches away from using a controlled, target level of amplification, such as that provided by a current mirror. A POSITA would not

have been motivated to add a current mirror to Ishimaru because a POSITA would not have been motivated to modify or adjust the amplification provided by Ishimaru's transistors 119 and 120—an uncontrolled, variable level of amplification—by adding a current mirror—providing a controlled, target level of amplification. EX2006-WentzloffRpt, ¶¶139-141, 180-181.

Second, Petitioner contends that Harrison's current mirror “would advantageously provide better isolation between the left side and the right side of Ishimaru's circuit.” Petition, 72-73. However, Petitioner provides no evidence, support, or reasoning for why any alleged coupling between Ishimaru's left and right sides is sufficiently problematic that better isolation is needed or that the level of coupling provided by Harrison's current mirror is a sufficient improvement. Ishimaru describes a function circuit that works for its intended purpose and there is no indication that it would need or benefit from any alleged improved isolation. EX2006-WentzloffRpt, ¶¶145, 180-181.

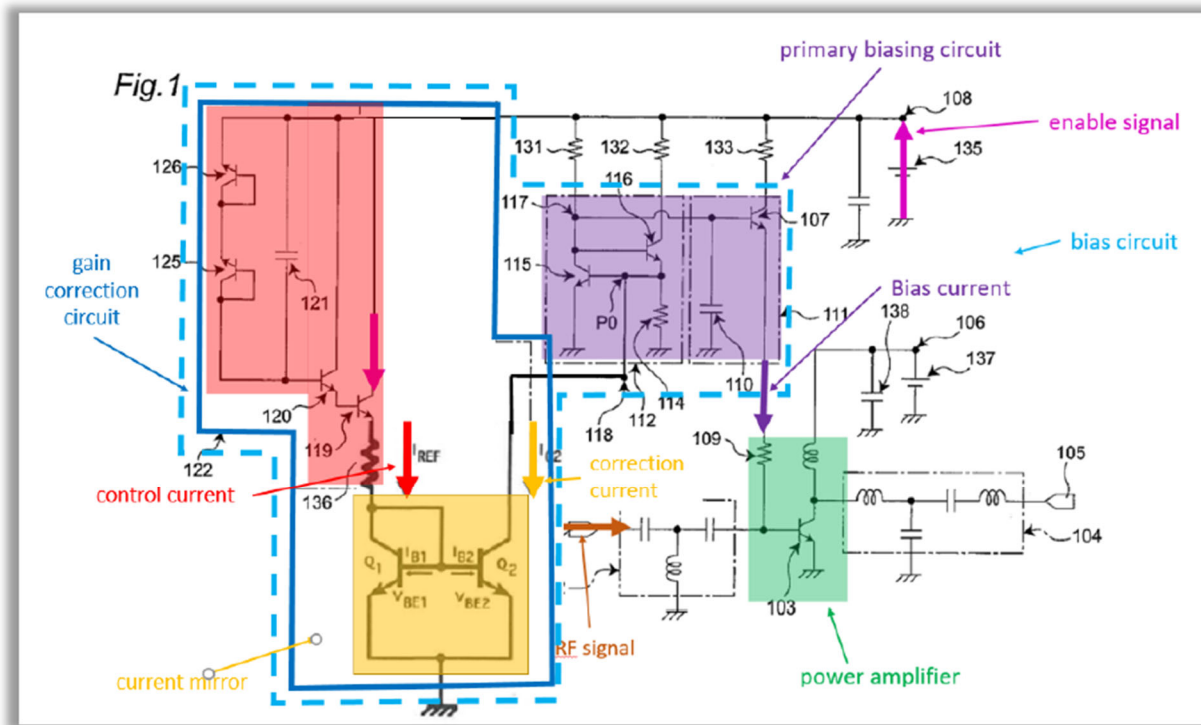
Third, Petitioner contends that Harrison's current mirror would “provid[e] an additional stage of fine tuning the current amplification,” “giv[ing] the designer an additional degree of freedom in designing the circuit,” “allow[ing] fine tuning in a final amplification stage that had better linearity, better control, and higher configurability” of its gain, and allowing the speedup circuit to be “reused and

adapted for different [power amplifier] applications and product lines.” Petitioner, 74-76. As discussed in Section V.A.1, Ishimaru uses BJT transistors (like transistors 119 and 120) that provide an uncontrolled, unpredictable, and variable level of current amplification when arranged as they are in Ishimaru, thus *teaching away* from the use of current mirrors which, as Petitioner acknowledges, “achieve granular, targeted levels of scaling that could advantageously be fine-tuned.” *Id.*, 72. A POSITA would only have been motivated to “fine tune” a level of amplification when achieving a specific amplification level is important—the opposite of an uncontrolled, unpredictable, and variable level of amplification as taught by Ishimaru.

Furthermore, adding a current mirror to the output of Ishimaru's transistor 119 cannot undo or compensate for the uncontrolled amplification of transistors 119 and 120. The current output by the current mirror in the modified circuit would continue to fluctuate uncontrollably, because it would be mirroring the uncontrolled current coming out of transistors 119 and 120. Thus, adding a current mirror to the output of transistor 119 will not allow for more precise or fine or granular tuning of the level of amplification provided, contrary to Petitioner's contentions. Finally, there is no indication in Ishimaru that its circuit of Figure 1 is only applicable to and can only be used for the specific example depicted in Figure

2, or that it is narrowly tailored to and only suitable for a specific power amplifier, specific layout, specific operating point, and specific use case. Therefore, a POSITA would not have been motivated to add a current mirror to Ishimaru's circuit and would not have had a reasonable expectation of success in doing so. EX2006-WentzloffRpt, ¶¶146-147, 180-181.

Notably, Petitioner's proposed modification to Ishimaru would require adding to Ishimaru's circuit at least two extra transistors (to form the current mirror), as shown in the yellow box below:



Petition, 70 (Petitioner's proposed modification of Ishimaru). Given the absence of any benefit to adding a current mirror to Ishimaru's circuit, a POSITA would

not have been motivated to add extra circuit components because doing so increases costs, complexity, and size of the circuit. For Ishimaru's circuit, which does not require the level of precise control of a current mirror, there especially would have been no motive to modify Ishimaru as proposed since there is no alleged deficiency or issue with Ishimaru's circuit. EX2006-WentzloffRpt, ¶¶142, 180-181.

Fourth, Petitioner incorrectly contends that the proposed modification to Ishimaru would involve no more than combining prior art elements according to known methods to yield predictable results. Petition, 77. Petitioner fails to address the problem of insufficient voltage "headroom," which would actually motivate a POSITA to *not* add a current mirror to Ishimaru's circuit as proposed. Voltage headroom refers to the amount of voltage available between the highest voltage point (node 108 in Ishimaru) and ground. Each transistor in the circuit that is between the highest voltage point (the voltage at node 108) and ground also needs a certain voltage difference across it, namely between its collector and emitter terminals (" V_{CE} "), and between its base and emitter terminals (" V_{BE} "), to operate as designed. In Ishimaru's circuit, the voltage drop across capacitor 121, the base-emitter voltage difference V_{BE} of transistor 120, V_{BE} of transistor 119, and the voltage drop across resistor 136 make up the total voltage difference between

node 108 and ground. A POSITA would not have been motivated to add transistor Q1 (of a current mirror) as Petitioner proposes because transistor Q1 also needs a certain voltage difference across it to operate as designed, but there may be insufficient voltage available to accommodate it, causing performance issues for all transistors 119, 120, and Q1. *See, e.g.*, EX1012-Gilbert, 274 (explaining when adding circuit components below a BJT's emitter should consider the headroom issue so that "where headroom considerations allow, it is usually preferable to use emitter degeneration to improve the ratio accuracy"). When there is a headroom voltage issue, the range of the affected transistor's output voltage may be clipped and the affected transistor's output current may be saturated. *See, e.g.*, EX2025-Razavi, 17 (explaining "a number of undesirable effects occur" with insufficient headroom voltage). This will in turn cause the affected transistor's output to be distorted, which is opposite to Ishimaru's design goal. *See, e.g.*, EX1004-Ishimaru, Abstract ("Accordingly, in the invention, it becomes possible to suppress distortion increases of an amplification signal due to heat generation at the start time without using any temperature sensing element."). This will also reduce the "range of voltages" and "range of amplification" that Petitioner alleges is a benefit of adding a current mirror (Petition, 68), rather than broadening them as alleged. Petitioner fails to address how a POSITA would successfully address headroom

voltage issues, created by adding a current mirror to Ishimaru's circuit, to ensure an operative circuit that achieves the desired purported improvements. As such, it is unclear and unpredictable whether Petitioner's proposed modified circuit would be operable or be able to achieve its intended purpose and design goals. EX2006-WentzloffRpt, ¶¶143-144, 180-181.

That it was not obvious to modify Ishimaru's circuit to add a current mirror is confirmed by the file history of the '563 patent, which shares the same specification as and claims priority to the '101 patent through a series of continuation applications. The Examiner during prosecution was aware of and considered Ishimaru's circuit, via Ishimaru (EX1004-Ishimaru, Fig. 1) and Wakita (EX2011-Wakita, Fig. 6), and current mirrors (EX2009-Alon, 6:52-54, Fig. 2). EX2012-563P, References Cited. The Examiner stated in the "reasons for allowance" that the prior art of record "fails to fairly teach or suggest the claimed circuit comprising, among other limitations and unobvious limitations of '... and to mirror the control current to generate a correction current...' structurally and functionally interconnected with other limitations in the manner as cited in the claim." EX2008-563FH, 33-34 (Notice of Allowance, 2-3) (underlining in original).

VI. Conclusion

Patent Owner respectfully requests denial of institution.

Dated: May 21, 2025

Respectfully submitted,

/Haixia Lin/
Haixia Lin
Reg. No. 61,318

PATENT OWNER'S EXHIBIT LIST

Exhibit No.	Description
2001	Order No. 33 in Inv. No. 337-TA-1413 (Hearing Date)
2002	Order No. 20 in Inv. No. 337-TA-1413 (Scheduling Order)
2003	Complaint in 8:24-cv-00974-FWS-ADS (C.D.C.A)
2004	Complaint in Inv. No. 337-TA-1413
2005	Redacted Opening Expert Report of David Ricketts Regarding the Invalidity of U.S. Patent Nos. 8,717,101 and 9,917,101
2006	Redacted Rebuttal Expert Report of David Wentzloff Regarding the Validity of U.S. Patent Nos. 8,717,101 and 9,917,101
2007	Order Granting Defendants' Unopposed Motion for Automatic Stay Under 28 U.S.C. §1659(A)
2008	Excerpts from File History for U.S. Patent No. 9,917,563
2009	U.S. Patent No. 7,869,775 to Alon ("Alon")
2010	Amended Appendix A - Invalidity Contentions for U.S. Patent No. 8,717,101 based on Ishimaru
2011	U.S. Patent No. 8,692,619 to Wakita ("Wakita")
2012	U.S. Patent No. 9,917,563 ("563 patent")
2013	RESERVED
2014	RESERVED
2015	RESERVED

Exhibit No.	Description
2016	Excerpts of Gray et al., Analysis and Design of Analog Integrated Circuits (5th ed. 2009)
2017	Excerpts of Roland E. Thomas et al., The Analysis & Design of Linear Circuits, (7th ed. 2012)
2018	ADI HMC7748 Datasheet
2019	RESERVED
2020	RESERVED
2021	RESERVED
2022	Excerpts of Steven M. Kaplan, "Electrical and Electronics Engineering Dictionary" (2004)
2023	RESERVED
2024	RESERVED
2025	Excerpts of Behzad Razavi, Design of analog CMOS integrated circuits (2nd ed. 2015)

CERTIFICATE OF COMPLIANCE

I hereby certify that the foregoing Patent Owner's Preliminary Response contains 9,277 words as measured by the word processing software used to prepare the document, in compliance with 37 C.F.R. § 42.24(d), excluding the parts exempted from the word count by 37 C.F.R. § 42.24(a)(1).

By: /Jungyeon Kim/
Jungyeon Kim
Reg. No. 82,377

CERTIFICATE OF SERVICE

I hereby certify that on May 21, 2025, I caused a true and correct copy of the following materials:

- Patent Owner's Preliminary Response
- Word Count Certification Under 37 CFR §42.24(d)
- Patent Owner's Exhibit List
- Exhibits 2011, 2012, 2016-2018, 2022, 2025

to be served via e-mail, as consented to by Petitioner, on the following attorneys of record:

jmbaird@duanemorris.com
pdmcperson@duanemorris.com

By: /Jungyeon Kim/
Jungyeon Kim
Reg. No. 82,377