A BiCMOS Analog Front-End Circuit for an FDM-Based ADSL System

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***Abstract*— This BiCMOS analog front-end (AFE) integrated circuit contains the analog transmit function and a low-noise receiver for FDM-based ADSL systems. The IC includes a current steered 14-bit 5-Msps D/A converter, laser trimmed third-order reconstruction and anti-alias filters, a programmable attenuator with 200-ohm output drive capability, 60-dB of RX programmable gain, and a serial interface. Trimmable thin-film resistors allow $\pm 4\%$ filter cutoff frequency and absolute gain accuracy. The multitone power ratio performance of the part is approximately 65 dB with a spurious free dynamic range >70 dBc. The CMRR of the RX channel is >90 dB @ 1.1 MHz. PSRR for transmit and receive are greater than 60 dB. The isolation features of the 1.2-μm BiCMOS technology allow transmit and receive to operate in full-duplex mode with greater than 80 dB of cross- talk isolation. The chip size is 25.8 mm^2 which includes bond pads and electrostatic discharge protection devices.**

***Index Terms*— ANSI standards, asymetric digital subscriber line, BiCMOS integrated circuits, continuous time filters, digital-analog conversion, distortion, modems, operational-amplifiers, signal reconstruction.**

I. Introduction

AN AYMMETRICAL digital subscriber line (ADSL) is being touted as a near-term solution for the high-speed Internet access bottle neck that is developing around the world [1]. This paper describes an analog front-end circuit (AFE) that can be used in frequency division multiplex (FDM) ADSL systems. The currently accepted ANSI standard for ADSL is a discrete multitone (DMT) line code. The DMT signal is a multicarrier signal where channel frequency allocations may overlap or be spectrally separated. Transmit (TX) and receive (RX) chains operate in full duplex mode. The two techniques used to separate the near-end transmit signal from the far-end receive signal are echo cancelling (EC) and FDM. Systems with nonoverlapping channel allocations are FDM systems which rely on bandpass filtering for channel separation. The bandwidth of the DMT signal is approximately 1.1 MHz. This bandwidth is divided into upstream (U/S) and downstream (D/S) channels. The D/S channel delivers data rates of 6–10 Mbps down existing copper twisted pair depending on the line condition and length. The U/S channel delivers approximately 220–640 Kbps.

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The DMT time-domain signal, being the aggregate of multiple carriers, is near-Gaussian in distribution. As such, the time-domain signal occasionally exceeds the full-scale value of the DAC. The ADSL standard requires a DAC clipping rate of less than 1 in 10^7 samples. Given this requirement the DAC is loaded with a peak to rms ratio of 5.33. Operating at this high crest factor or peak to average ratio (PAR) requires a large dynamic range with good linearity over a 1.1-MHz bandwidth. A 14-bit D/A converter, amplifier, and filter blocks with THD < -75 dB over a 1.1-MHz bandwidth are required in the TX and RX channels. A figure of merit for the linearity is multitone power ratio (MTPR). The MTPR is measured by generating a DMT waveform which has a specific crest factor with specific carriers missing. The waveform is then passed through the TX or RX chain. The total integrated power of the notch at the location of the missing carriers is measured with respect to the adjacent carriers. Notch depth is measured for several DMT waveforms with different PAR's. The notch depths for each DMT waveform are averaged to give an MTPR number. Much of the transistor- and system-level design of this IC is aimed at achieving high MTPR numbers. High MTPR correlates directly with low bit error rate (BER) and thus longer reach over the copper twisted pair.

Fig. 1 shows a block diagram of the IC. There are separate fully differential TX and RX paths. The gain control is provided through a four-wire serial interface. The IC is designed such that it can be used at the ATU-C (central office side) or the ATU-R (customer premise or user side). A typical application diagram is shown in Fig. 2. Band separation filters are off-chip between the output of the TX and at the input of the RX channel.

II. System Considerations

Discrete multitone (DMT) was selected as the line code for ADSL for several reasons. The premise behind DMT is the division of the available bandwidth into smaller bands or "bins" each of which is assigned a low-rate modulated carrier at the bin center. Over the smaller subbands the channel looks relatively benign, requiring minimal channel equalization, thus simplifying implementation of the demodulators. Because multiple carriers are used, the bit loading on each individual carrier can be adjusted based on the available signal-to-noise ratio (SNR) in that subband to maximize the aggregate data rate for the system. Given a maximum total power for all carriers, carriers in subbands with low noise are allocated more power, allowing higher bit loading, and those carriers in bins with high noise or external interferers

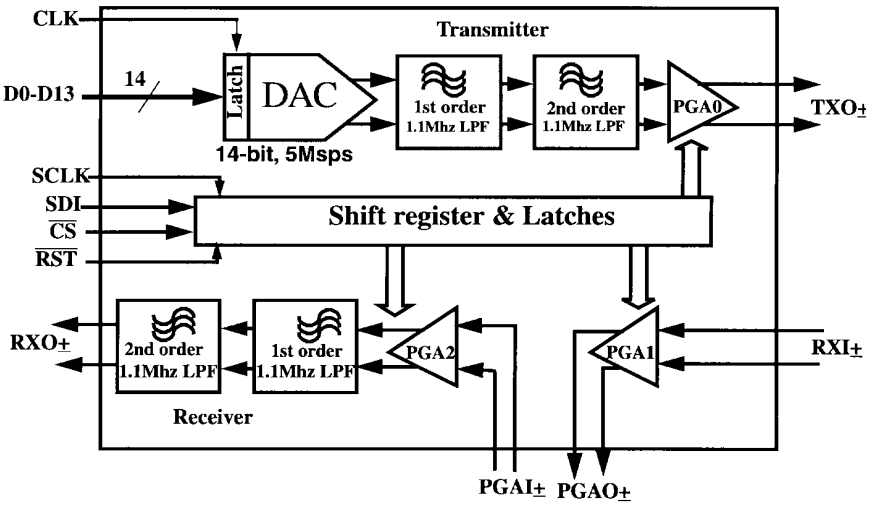

Fig. 1. Block diagram of AFE.

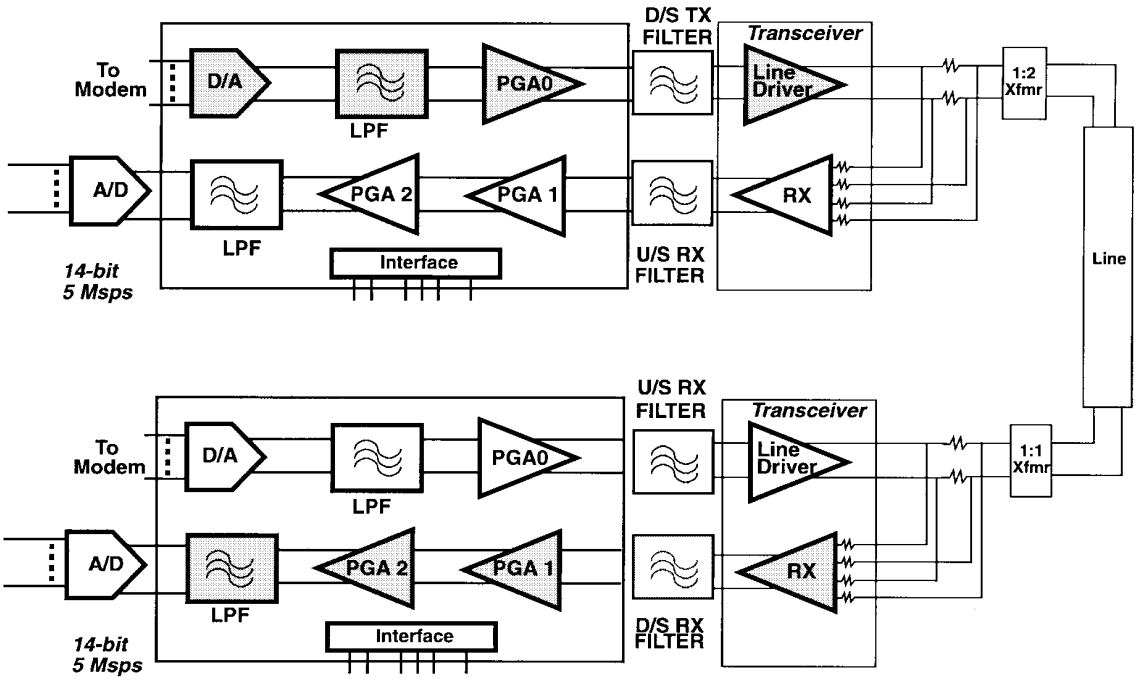

Fig. 2. Typical application diagram.

are allocated lower power. The ADSL standard allows over 200 downstream carriers (central office to customer premise), which permits the aggregate data rate to be matched very precisely to the to available line conditions.

Each of the subcarriers in the ADSL waveform is modulated with multilevel quadrature amplitude modulation (QAM). Each of the possible 255 carriers are on 4.313-kHz spacing for a total occupied bandwidth of 1.104 MHz. The drawback to DMT is the high peak-to-average ratio (PAR) of the waveform due to the instantaneous summation of up to 255 carriers. The theoretical limit on the PAR given constant envelope signaling on each DMT carrier is

$$\mathrm{PAR} = 10 \cdot \log_1 0(M) \tag{1}$$

where M = Number of DMT carriers.

The theoretical limit is very high (24 dB) for the downstream signal. Although this limit is rarely approached, the high PAR places severe circuit noise and linearity requirements on the analog front end (AFE).

Several mechanisms contribute to the noise in the AFE. Two major sources of noise are the quantization noise and overload noise in the digital-to-analog converters (DAC's) and analog-to-digital converters (ADC's). Both quantization noise and overload noise occur in the ADC due to quantization of a continuous analog waveform to discrete levels. Overload noise occurs when the analog waveform amplitude exceeds the peak input of the converter. Quantization and overload noise for the DAC actually occurs when the digital signal processor (DSP) truncates the precision of the transmit samples prior to appli-

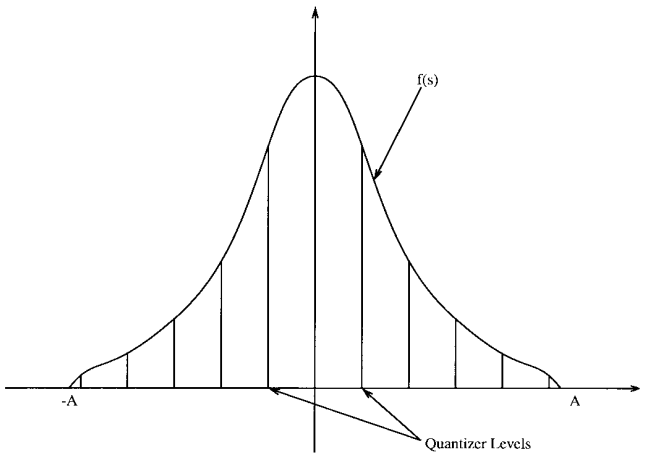

Fig. 3. Amplitude distribution of analog waveform.

cation to the DAC. To establish the number and fidelity of the quantizer levels for the converter, analysis of the quantization effects on the DMT waveform must be considered.

A. DMT Waveform

Given an analog waveform of a specific amplitude distribution as shown in Fig. 3, the noise due to quantization can be shown to be

$$N_q = \frac{A^2}{3 \cdot M^2} \tag{2}$$

where $A =$ peak amplitude and $M =$ number of quantizer levels.

Equation (2) assumes the amplitude distribution of the analog waveform lies totally within the range of the converter $(-A$ to $+A)$ [2]. Due to the high theoretical PAR of (1) the amplitude distribution of the ADSL waveform is truncated to reduce the requirements on the AFE linearity. The amplitude distribution of DMT results from the summation of a large number of carriers, which on a per sample basis can be shown to be Gaussian based on the central limit theorem [3]. Equation (2) then becomes

$$N_q = \frac{(k \cdot \sigma)^2}{3 \cdot M^2} + \xi(k) \tag{3}$$

where

- k number of standard deviations passed;
- σ standard deviation of waveform;
- M number of quantizer levels;
- $\xi(k)$ overload noise.

Note that $k * \sigma = A$.

For a Gaussian amplitude pdf the overload noise can be shown to be [3]

$$\xi(k) = \sqrt{\frac{2}{\pi}} \cdot \frac{\sigma_s^2}{k} \cdot \left(1 + \frac{2 \cdot k^2}{3 \cdot M^2}\right) \cdot e^{-k^2/2} \tag{4}$$

where

- σ standard deviation of the voltage waveform;
- k number of standard deviations passed;
- M number of quantizer levels.

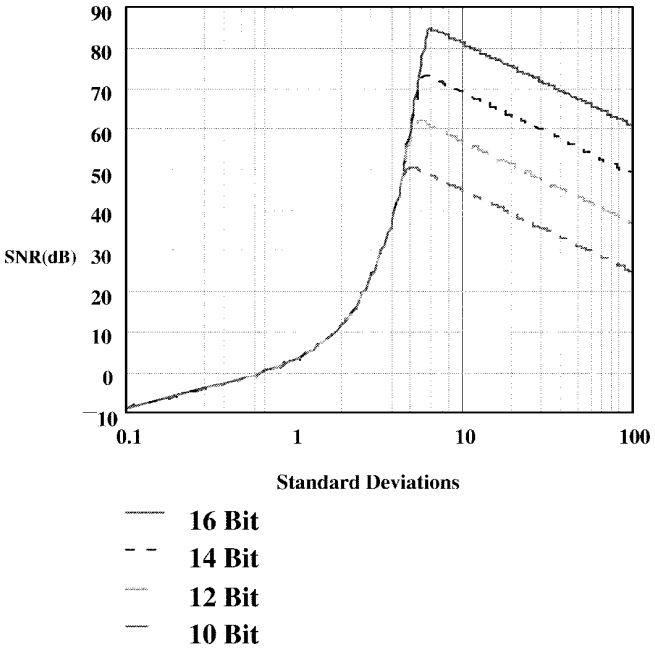

Fig. 4. SNR versus k for various quantizer levels.

B. Converter Requirements

Clearly, for a specified number of quantizer levels there is a tradeoff between quantizer noise and overload noise. As the overload noise is reduced by allowing more of the waveform to pass (k is larger), the quantization noise will begin to increase after a certain point. As k gets larger the upper quantizer levels are used less frequently due to the Gaussian amplitude pdf. This results is less quantizer levels being available for that part of the amplitude pdf which occurs most frequently. The converse is also true, as the overload noise is increased by making k smaller, the quantizer noise is reduced as more levels are available for quantizing that part of the waveform which occurs more frequently.

Derivation of an expression for SNR dependent on the number of standard deviations k allows one to plot the tradeoff between overload noise and quantization noise for a Gaussian amplitude pdf.

Let

$$\text{SNR} = \frac{\sigma^2}{N_q} \tag{5}$$

where $\sigma =$ standard deviation of the voltage waveform.

Then

$$\text{SNR} = \frac{\sigma_s^2}{\dfrac{(k \cdot \sigma_s)^2}{3 \cdot M^2} + \sqrt{\dfrac{2}{\pi}} \cdot \dfrac{\sigma^2}{k} \cdot \left(1 + \dfrac{2 \cdot k^2}{3 \cdot M^2}\right) \cdot e^{-k^2/2}}. \tag{6}$$

If (6) is plotted verses k for various quantizer levels the trade between quantizer levels and k is readily apparent, as shown in Fig. 4.

From Fig. 4, it can be seen that for any quantizer, there is an optimum number of standard deviations k that maximizes the SNR for a Gaussian amplitude pdf.

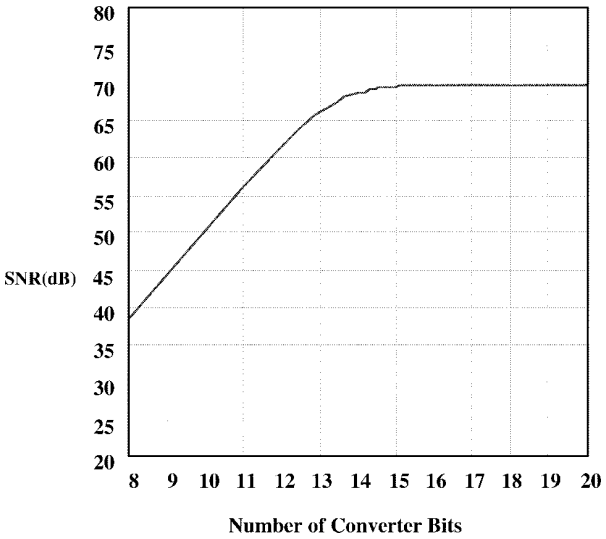

Fig. 5. SNR versus number of converter bits.

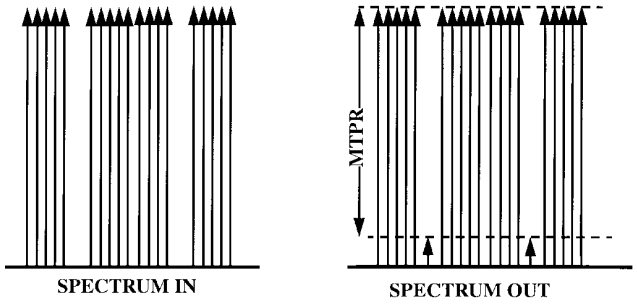

Fig. 6. MTPR test vector spectrum.

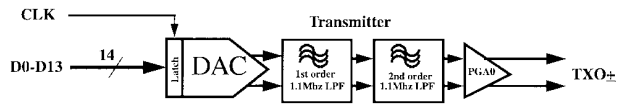

Fig. 7. TX chain.

Whenever the waveform is "truncated" to some number of standard deviations "k" the result is clipping in the analog front end. The clipping or overload noise will occur for those few samples which are outside the bounds of the converter. The upper levels in the communications protocol must take in account the periodic clipping to ensure proper bit-error rate (BER) performance. This is usually handled through interleavers and various coding methods in the MODEM's. For the ADSL DMT waveform the clipping rate is specified in the T1E1.413 standard as one in 10^7 samples. The clipping rate is also specified at a PAR of 5.33 : 1. To relate PAR to the previous analysis, let

$$\mathrm{PAR} = \frac{V_{\mathrm{PEAK}}}{V_{\mathrm{RMS}}} \tag{7}$$

where $V_{\mathrm{RMS}} = \sqrt{\mathrm{Power}}$.

For the Gaussian ADSL amplitude pdf, (7) can be reduced to

$$\mathrm{PAR} = \frac{k \cdot \sigma}{\sqrt{\sigma^2}} \tag{8}$$

where

$$k \cdot \sigma = \mathrm{Peak}$$
$$V_{\mathrm{RMS}} = \sqrt{\mathrm{Power}}$$
$$\sigma^2 = \mathrm{Power}$$

then

$$\mathrm{PAR} = k. \tag{9}$$

The number of standard deviations k is just the PAR of the Gaussian waveform. Using a PAR of 5.33 and Fig 4 it is apparent that a 12-bit quantizer is almost optimum (offers the highest SNR with the lowest number of quantizer levels). Larger quantizers offer only slightly higher SNR. If SNR is plotted verses a fixed k of 5.33 for various quantizer levels as shown in Fig. 5. it can be seen that above 12 bits the increase in SNR by adding more bits becomes less and less and reaches a theoretical limit of about 70-dB SNR.

It should be noted, however, that the previous analysis assumes perfect quantization (perfectly linear converter). In order to implement a converter with 12 effective bits a larger quantizer must be built to account for the nonlinearity of the converter. A 14-bit converter was implemented such that a minimum of 12 effective bits could be guaranteed.

C. Amplifier Requirements

Determining the linearity requirements for the amplifiers in the AFE is difficult using traditional methods due to the nature of the ADSL waveform previously discussed. Single-tone performance measures such as total harmonic distortion (THD) and two-tone intermodulation distortion (IMD) rely on sinusoids as the test signal. The amplitude pdf of a sinusoid is very different from the pdf of the ADSL waveform. Because of the zero mean Gaussian nature of the ADSL waveform, the most probable value for the waveform is 0 V. Amplifiers which exhibit crossover distortion would severely impact the spectral purity of ADSL, but would not necessarily impact a sinusoid to the same extent. Instead of attempting to relate classic measures of noise and distortion to the performance of ADSL, a new test waveform was devised which encompassed the linearity and noise measurements for the amplifier into a single test.

Modifying a classic technique from FDM analog technology for testing system linearity, the concept of a MTPR (multitone power ratio) test was defined. This test consists of a plethora of frequency domain impulse, uniformly spaced over a bandwidth of interest, with the characteristic that periodically a frequency impulse is "missing" giving the appearance of a spectral notch. The time series representation of the waveform for the case where every sixteenth tone is absent is given as

$$s(k) = \sum_{i}^{L} \cos(\Omega_i k + \theta), \qquad i \neq 16, 32, \text{etc.} \tag{10}$$

where $L = 256$ for ADSL, $\Omega_i = 2\pi/L$, and the term θ_i represents the starting phase of the ith tone. Fig. 6 represents the spectrum of this test vector. Notice that the comb spectrum

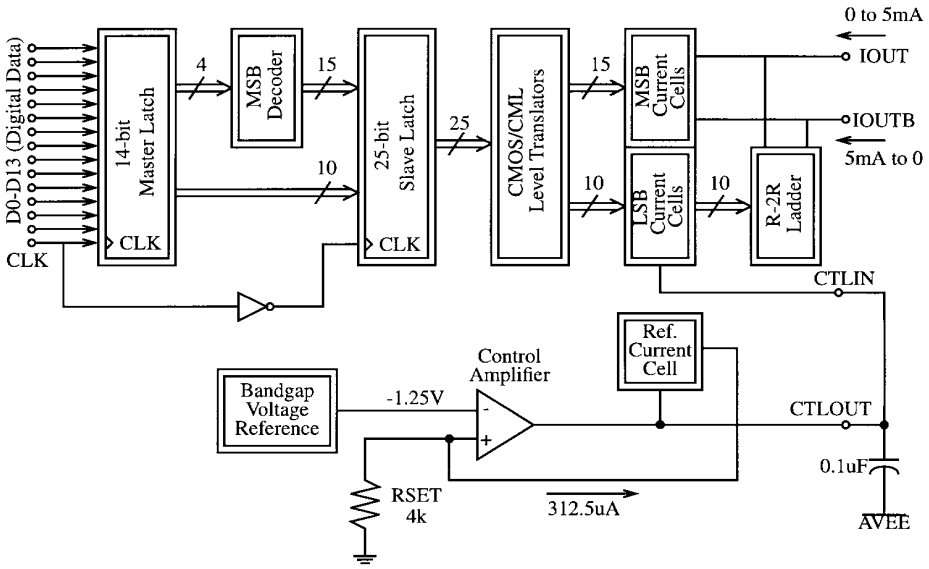

Fig. 8. D/A functional block diagram.

has suppressed tones located periodically in the spectrum. The frequency impulses are separated by the DMT carrier spacing [4] and each carrier of the comb is given a controlled starting phase θ_i [5] to constrain the PAR. Specifically, each tone's starting phase is adjusted to establish a PAR and the average signal level of the test vector is adjusted for a certain "backoff level" below full scale.

The object of the test is to pass this test waveform through the amplifier under test and observe at the output the depth of the "Notches" with respect to the level of the adjacent carriers. Factors that contribute to "filling-in" of the output notches are the intermodulation characteristics of the analog amplifier and the residual noise floor. It is felt that this testing technique better represents the actual scenario present in the case of the DMT/OFDM spectrum, where it is important to maintain a high signal–to-distortion ratio in each of the frequency bins.

Because the amplifier noise and nonlinearities are super imposed on that of the converter, an MTPR goal can be established for the entire AFE. The MTPR is essentially a measure of SNR within a frequency bin. If we assume the noise is spectrally flat as is the signal, the SNR for a frequency bin will be the same as the SNR for the entire waveform. If we construct an MTPR test signal with a PAR of 5.33 and apply it to the front end such that the waveform peak is just within the converter limits no overload noise will occur. Based on (5) and (3), the SNR is then

$$\mathrm{SNR} = \frac{\sigma_s^2}{\dfrac{(k \cdot \sigma_s)^2}{3 \cdot M^2}}. \tag{11}$$

Equation (11) can then be reduced to

$$\mathrm{SNR} = \frac{3}{k^2} \cdot M^2. \tag{12}$$

With $M = 4096$ (12 bits effective) and $k = 5.33$, the MTPR design goal for the AFE was 62.5 dB minimum.

III. Transmit Chain

The TX chain is shown in Fig. 7. It consists of a 14-bit current steered D/A converter, a reconstruction/bandshaping filter, and a programmable attenuator.

A. Functional Description 14-bit D/A Converter

The TX path begins with CMOS input buffers which are compatible with both 3- and 5-V logic. The data is then sent to a 14-bit 5-MHz current steered D/A converter based on a previous 14-bit 100-MHz D/A converter architecture [6]. The functional block diagram of the DAC is given in Fig. 8. Input data first passes through the master latches then the MSB's are decoded by a 4–15-thermometer decoder. Next, the data is resynchronized by the slave latches and finally translated to control 25 precision current cells. Ten LSB cells connect to the R-2R ladder, controlled by $D0$–$D9$, while the remaining 15 connect directly to the outputs, controlled by $D10$–$D13$. One additional precision current cell is connected in a feedback configuration with the bandgap voltage reference and control amplifier to establish the full-scale output current (I_{FS}). The resistor which sets the full-scale output current (R_{SET}) is included on-chip in order to track the I–V conversion resistors following the DAC.

Segmentation of the four most significant bits (MSB's) into 15 equally weighted current sources is a standard technique used to reduce DNL, glitch, and harmonic distortion. A 0.1 μF external capacitor is connected from the control amplifier output to the analog -5.2 V supply to reduce output noise and improve settling time [7].

B. CMOS/CML Level Translator

Aside from reducing I_{FS} from 20.48 to 5 mA, all digital logic was implemented in CMOS rather than CML to reduce power dissipation compared to the 100-MHz version [6]. Otherwise, the two designs are essentially identical except for the CMOS/CML level translator shown in Fig. 9. In this circuit $V\mathrm{Bias1} = 0.3$ V and $V\mathrm{Bias2}$ is temperature compensated so

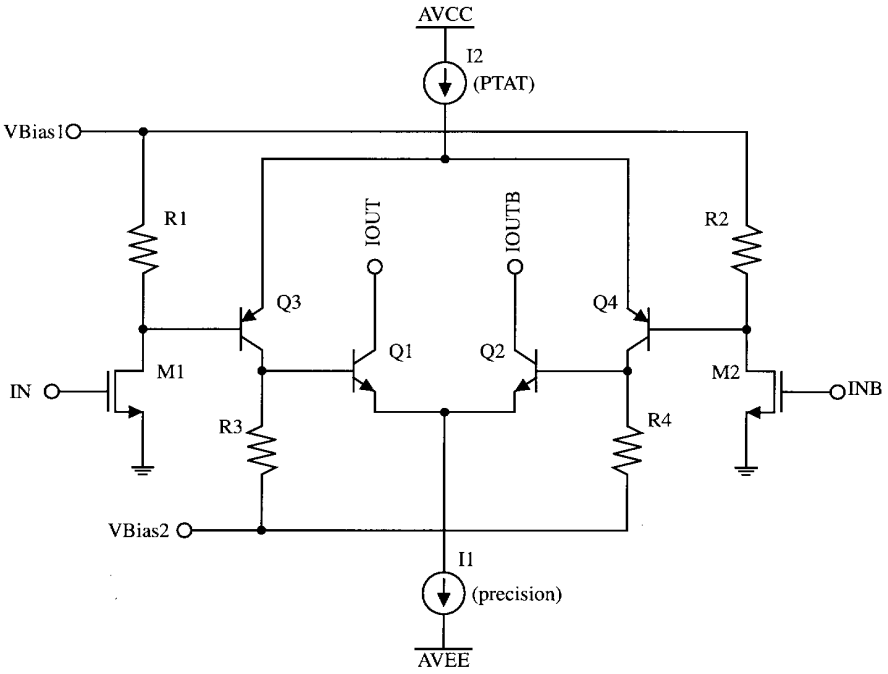

Fig. 9. D/A CMOS/CML level translator.

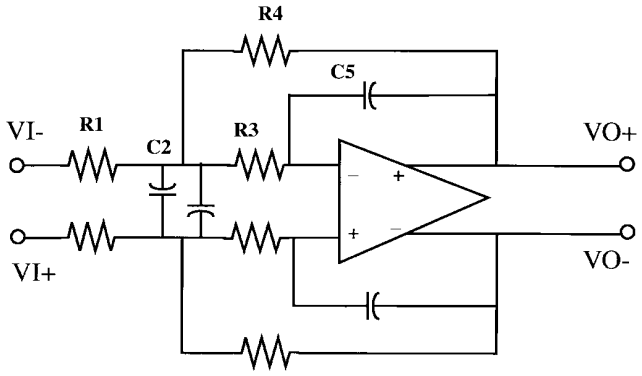

Fig. 10. Rauch biquad.

that the "high" voltage at the base of $Q1$ or $Q2$ is always 1.5 V. This helps to maximize VCE of $Q1, Q2$ and the BJT in precision current source $I1$ over the operating temperature range of the chip. Input devices $M1$ and $M2$ are sized as small as possible to minimize capacitive coupling of the 0–5 and 5–0 V input swings to the bases of $Q3$ and $Q4$ while maintaining a ± 0.25 V minimum differential output voltage swing. As in the 100-MHz version, current source $I2$ is proportional to absolute temperature (PTAT) in order to eliminate the temperature dependence of the $I_{\mathrm{OUT}}/I_{\mathrm{OUT}B}$ ratio, thereby giving the least possible glitch energy over temperature [7]. Finally, the value of resistors $R1$–$R4$ has been chosen to minimize power dissipation while maintaining adequate switching speed for 5-MHz operation.

C. Reconstruction Filters

The current output of the D/A is converted to a voltage by a third-order active R-C Chebyshev filter. This filter acts to reconstruct the sample and held signal of the D/A. The filter cutoff frequency and gain are trimmed by using NiCr links

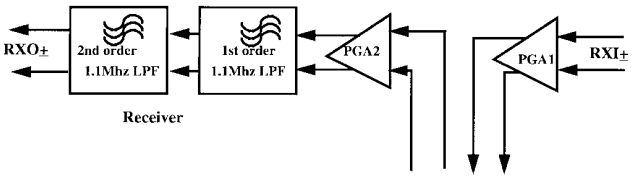

Fig. 11. RX chain.

for the resistive sections of the filter network. The third-order filter is constructed of a single-order section and a biquad. This third-order configuration allows independent setting of the gain and frequency response. The second order section is a Rauch biquad, shown in Fig. 10, utilizing only one amplifier with no positive feedback thus minimizing the required gain bandwidth product. The amplifier used for these filter sections is described below. The Rauch topology minimizes the number of opamps in the transmit chain thus lowering the power and reducing the noise and distortion contributors. The first-order section can be reconfigured into a second-order section with a limited number of mask changes to achieve a fourth-order response. The filter cutoff frequency is trimmed to within $\pm 4\%$ of the theoretical value.

D. TX Power Control

The final stage of the TX chain is a programmable attenuator (-12 to 0 dB) that is capable of driving a 220-ohm differential load at 12 $V_{p\text{-}p}$ diff. This attenuator is used to adjust the TX power levels depending on the line length and FCC transmission requirements.

IV. Receive (RX) Chain

The RX path contains programmable gain and attenuation and an anti-aliasing filter. The gain and attenuation are programmed to achieve maximum SNR while meeting the

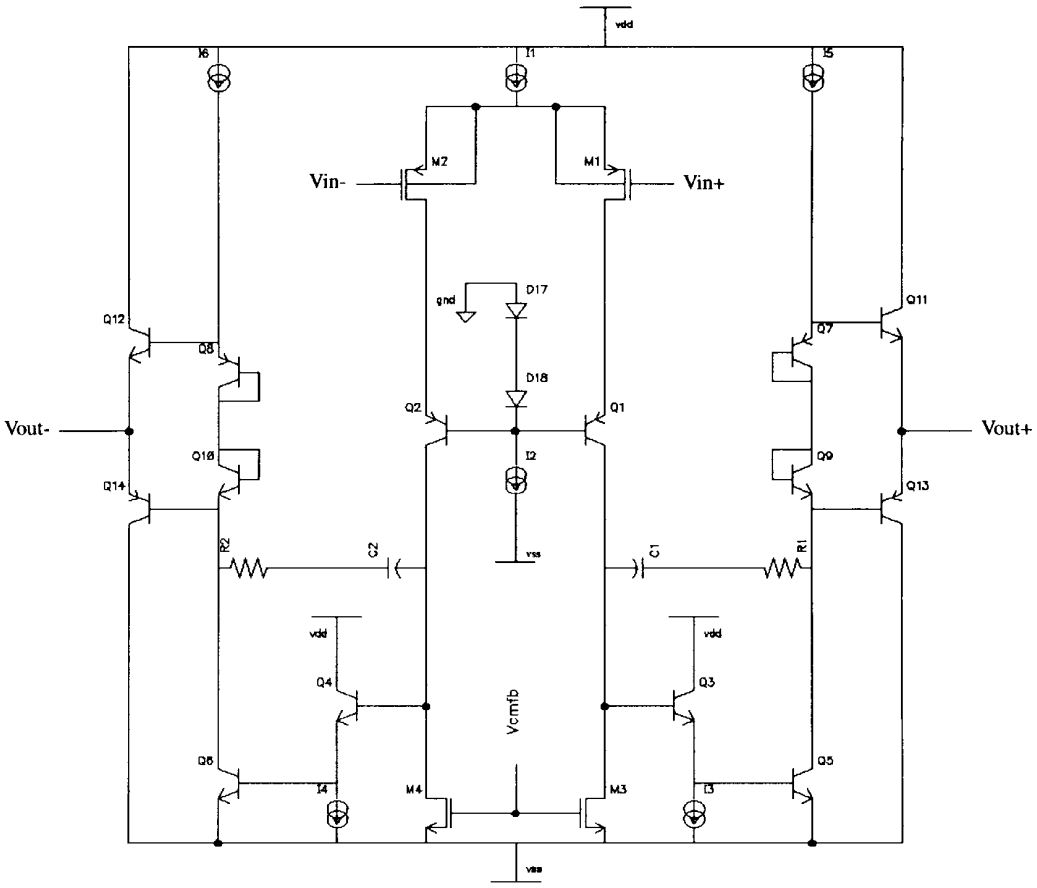

Fig. 12. Schematic of opamp.

dynamic range requirements of the A/D converter (4 $V_{p\text{-}p}$ diff). The PGA settings cover a wide range of line types and lengths. A block diagram of the RX chain is shown in Fig. 11.

A. PGA

The input PGA (PGA1) is a high-impedance (MOS input) with 0–24 dB of programmable range. The input referred noise density of this RX chain is 12 nV/$\sqrt{\text{Hz}}$. The output of PGA1 goes off-chip such that AC coupling and or additional filtering can be added. There can be line cases where the composite in band and out-of-band energy would exceed the dynamic range of the second PGA (PGA2), thus additional filtering between the PGA's can be used to avoid this problem. The signal then comes back on chip to PGA2 with -9 to $+18$ dB of gain. This stage is programmed to maximize the received signal or reduce it to fit into the dynamic range of the ADC.

B. Anti-Alias Filter

The next block is a third order anti-alias filter constructed in a similar fashion to the TX reconstruction filter. This block is trimmed for RX absolute gain error and cutoff frequency accuracy.

V. Operational Amplifier Design

Spectral purity is critical for any amplifier in the signal path of an ADSL analog front end circuit. Any source of spectral contamination can degrade the MTPR performance of the system and thus lower the ability of the system to handle worst case conditions, specifically very short or very long transmission loops. To maximize the MTPR performance, the operational amplifiers for the transmit chain and receive chain must have excellent THD, CMRR, PSRR, and noise performance. Power consumption is important as several amplifiers are used in the reconstruction filters, the anti-alias filters, and the programmable gain amplifiers in both the TX and RX chains. In order to obtain high linearity over the 1.1-MHz signal bandwidth, the amplifiers were designed with a 70-MHz nominal gain bandwidth product which provides $>$35 dB of loop gain at 1 MHz. Nonlinearities due to the amplifier are reduced by 35 dB by the feedback.

A simplified diagram of the amplifiers used is shown in Fig 12. To minimize distortion due to second-order harmonics and avoid substrate coupling, the amplifiers were built fully differential. The amplifier consists of a PMOS input pair $(M1$–$M2)$, PNP cascode transistors $(Q1$–$Q2)$, buffer emitter followers $(Q3$–$Q4)$, second gain stage common-emitter NPN transistors $(Q5$–$Q6)$, and class A-B output driver stages $(Q7$–$Q14)$.

The input differential pair $(M1$–$M2)$ was chosen to be PMOS for three reasons. First, the amplifier was used in an active R-C filter which had input resistances on the order of 2 kΩ. At these impedance levels the noise contribution of the

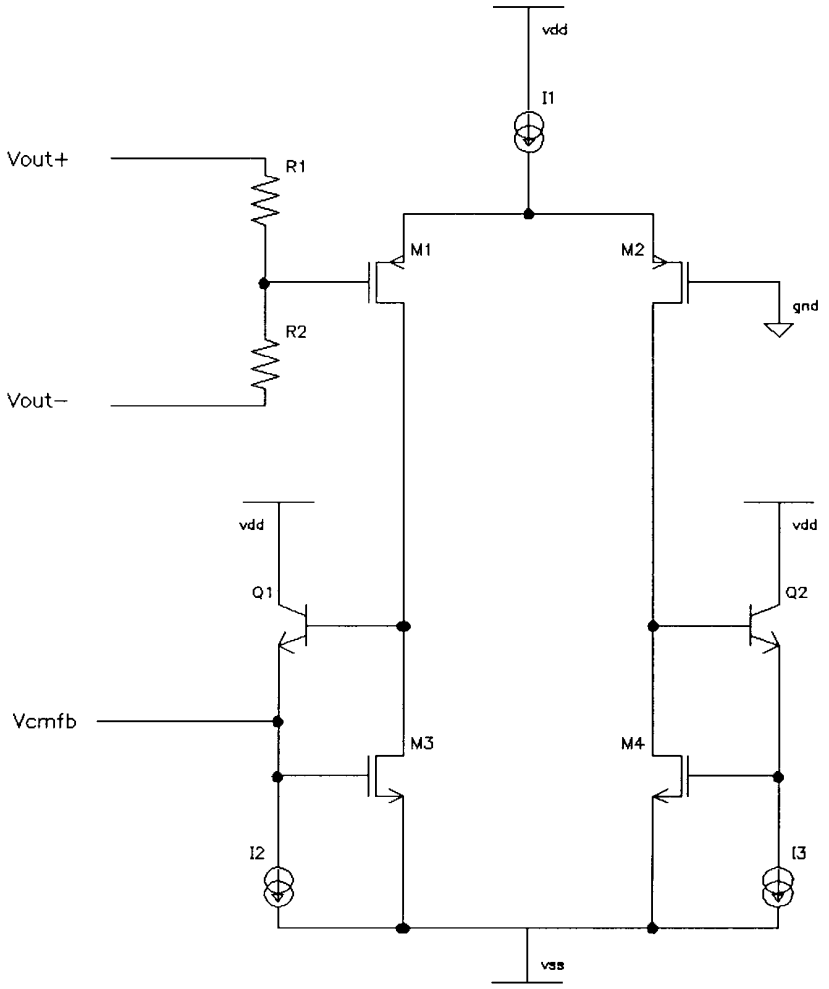

Fig. 13. Common mode feedback circuit.

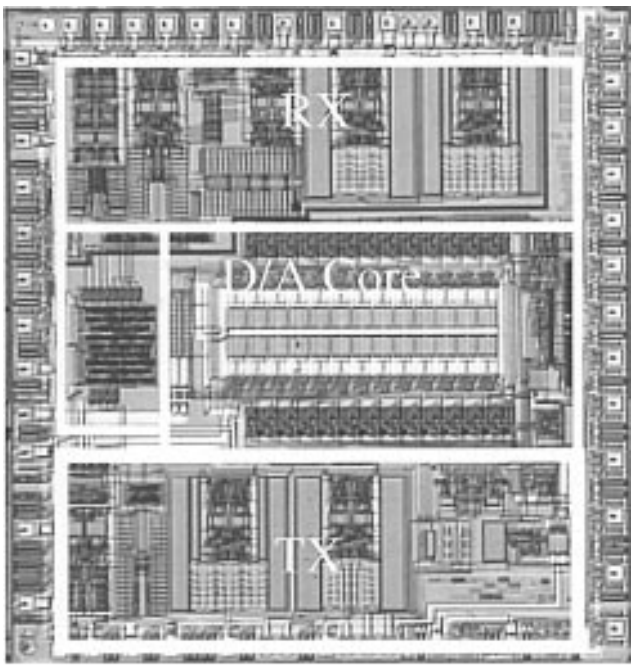

Fig. 14. Die photomicrograph.

input current noise of a BJT differential pair and active load was too large. PMOS transistors were used to reduce this input referred current noise contribution. PMOS, instead of NMOS, transistors were used due to their lower $1/f$ noise corner. The final advantage was the large transconductance ratio between the second gain stage bipolar transistors $(Q5$–$Q6)$ and the input pair MOS transistors $(M1$–$M2)$ allowed for smaller compensation capacitors $(C1$–$C2)$. The body connections for the input pair were tied to their respective sources to maximize the power supply rejection ratio (PSRR) of this stage. A differential output signal can be generated by the power supply due to device mismatch in the differential pair and the modulation of the back gate by the supply if the body is tied to the supply. Tying the bodies to the source prevents the supply from modulating the threshold voltages of the differential pair. In order to maximize the bandwidth of the differential pair, a cascode pair of PNP transistors $(Q1$–$Q2)$ was used to remove the impact of the miller capacitance that would appear at the gates of differential pair. These cascode transistors also improve CMRR and PSRR [8]. It is important to note that a straight cascode was used and not a folded cascode stage. This was done for two reasons, the primary of which was to avoid the extra leg of current which would be necessary to

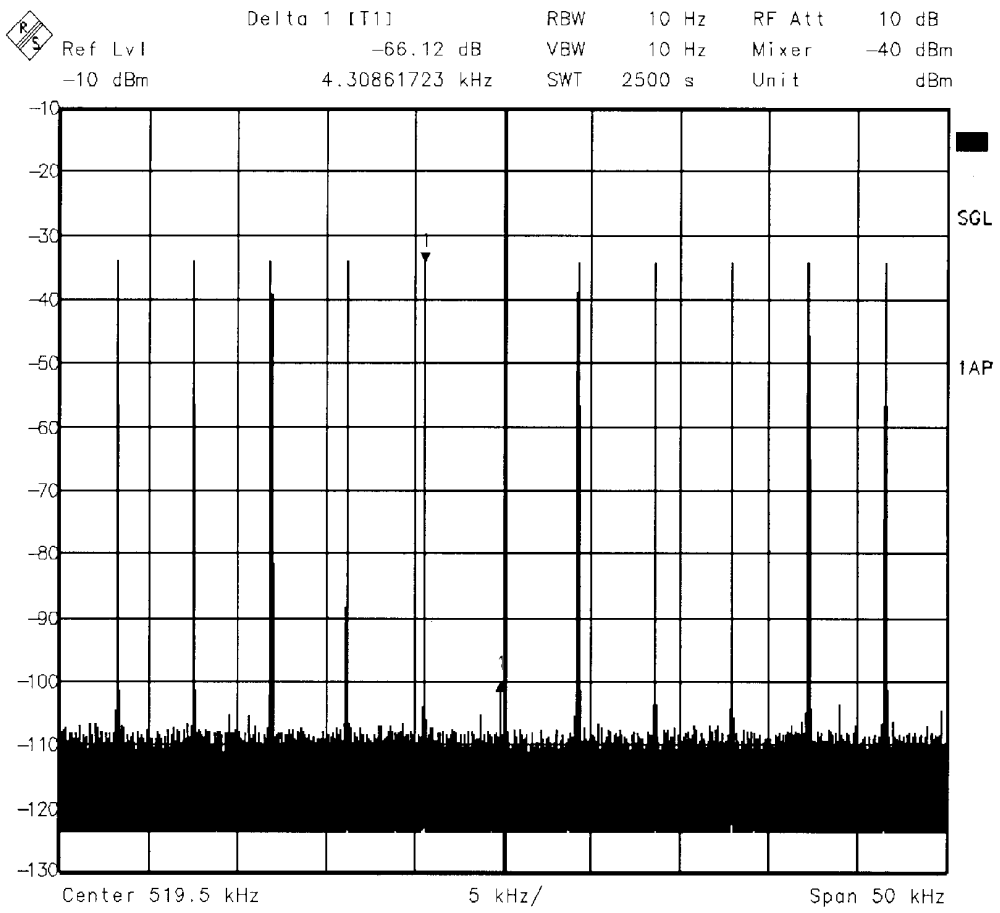

Fig. 15. TX MTPR.

bias the folded device, thus lowering the power necessary to achieve the same bandwidth. The second reason the straight cascode was used was that the dynamic range needed for the input differential pair was very small due to the fact that the amplifiers were all to be used in fully differential systems. The input dynamic range can be quite large for single-ended amplifier architectures, especially some noninverting unity gain buffer configurations where both input terminals track the input voltage. In fully differential amplifiers, there is no equivalent circuit to the typical noninverting unity gain buffer—only circuits where both inputs stay at a virtual ground potential.

The input referred offset was reduced by using low-voltage NMOS devices as the active load of the input pair. The low-voltage devices exhibit better matching (with slightly reduced output impedance) than the high-voltage devices due to the absence of the extension implant. The low-voltage devices can be used in this case as the drain voltage is clamped and the common mode feedback circuit takes out dc errors.

Emitter follower devices ($Q3$–$Q4$) were needed to maintain a high dc gain over process variation. Most of the gain of the amplifier comes from the high impedance node at the collector of devices $Q1$&$Q2$. Without these devices here, the bases of $Q5$–$Q6$ would be attached to the collectors of $Q1$–$Q2$, respectively. The Beta of PNP devices $Q13$–$Q14$ varies greatly over process and causes the impedance of second gain stage $Q5$–$Q6$ to vary equally. This made it difficult to derive a high gain from the second stage, so the majority of the gain was moved to the first gain stage by increasing the impedance at the collectors of $Q1$–$Q2$ with the buffers $Q3$–$Q4$. The insertion of these devices also lead to problems with gain margin due to additional parasitics which caused some peaking beyond the gain bandwidth of the amplifier. The amplifiers were compensated across the second gain stage with pole-splitting miller capacitors $C1$–$C2$ and right-half plane zero cancelling resistors $R1$–$R2$. This compensation network is the same network used to compensate the common mode feedback circuit.

The output drivers consisting of devices $Q7$–$Q14$ are a standard single stage class A-B resistive drive output stage. The amplifiers were required to drive resistive loads from 220 Ω to 2 kΩ. A two-stage A-B buffer would have increased the output dynamic range by one diode drop and improved THD. Unfortunately this configuration would require two extra legs of current to bias the emitter–follower devices. The tradeoff in favor of lower power consumption was made in this case.

The common-mode feedback circuit (shown in Fig. 13) was uncomplicated because of the resistive drive capability of the amplifiers. The common mode output is sensed with a simple pair of resistors $R1$–$R2$, and compared with a reference voltage which in this case is ground. The comparison circuit drives the diode-connected NMOS $M3$–$M4$ which sets the gate voltage for $M3$–$M4$ in Fig. 12. The buffer device (Fig. 13) $Q1$ acts to move the parasitic pole at the gate

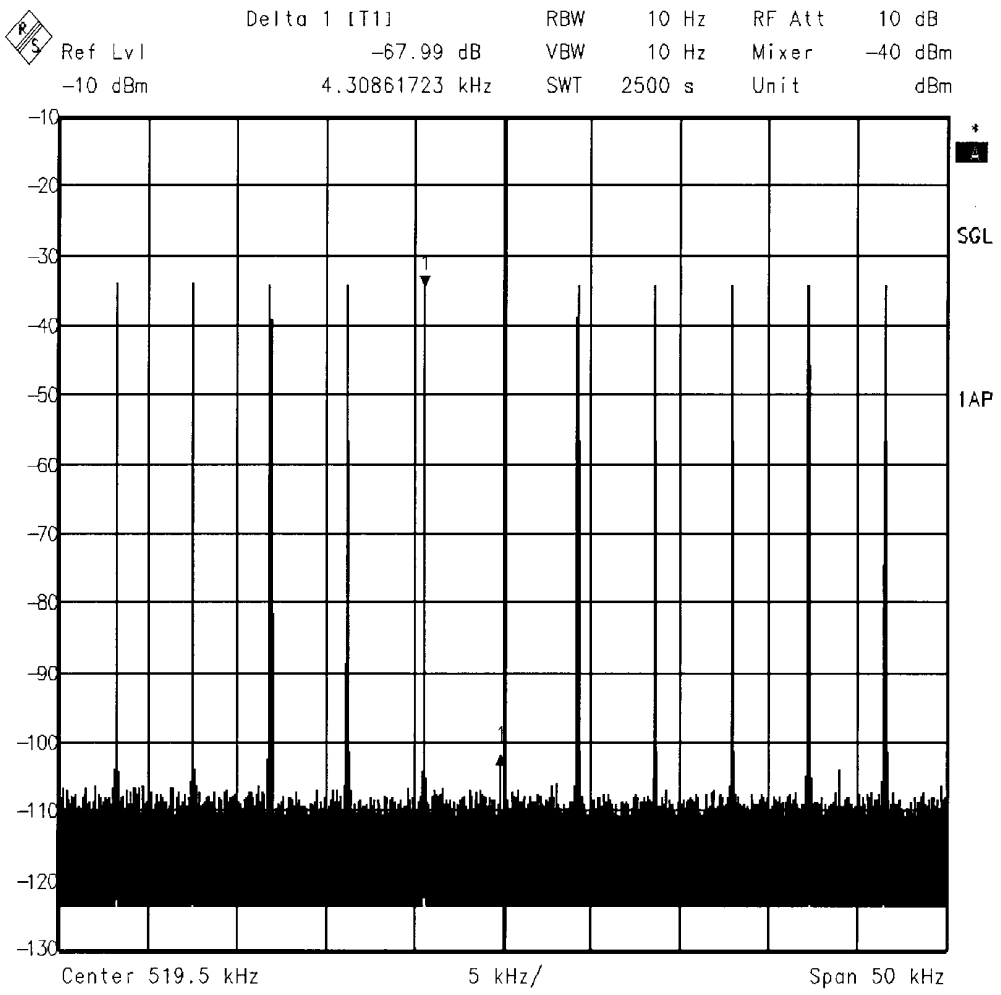

Fig. 16. RX MTPR.

TABLE I
SUMMARY PERFORMANCE DATA

Parameter	Measured	Units
Supply Voltage	±5	V
Signal frequency range	.01 - 1.1	MHz
Quiescent Power Dissipation	750	mW
TX MTPR	65	dB
RX MTPR	65	dB
Maximum Output Level	12	Vppdiff
Absolute TX gain accuracy at 0 dB setting	1	%
Output Gain Adjust Relative Accuracy	0.285	dB
RX input referred noise	12	nV/rthz
RX CMRR	>90	dB
RX PSRR	>60	dB
TX PSRR	>60	dB
TX-RX isolation	>80	dB

of $M3$ out in frequency so that the dominant pole in the compensation of the common-mode feedback loop is set by the same dominant pole as the compensation for the amplifier.

The input referred offset was reduced by using low-voltage NMOS device as the active load of the input stage. The low-voltage device can be used in this application as the drain voltage is clamped and the common mode feedback circuit takes out dc errors.

VI. INTEGRATION CONSIDERATIONS AND EXPERIMENTAL RESULTS

A photomicrograph of the die is shown in Fig. 14. measuring 25.8 mm^2 in area. Key integration considerations center around integration of the TX and RX chains on a single substrate. Of particular importance are nonlinear leakage paths, which would bypass band separation filtering. The other coupling problem is substrate noise caused by the relatively high-speed operation of the digital portion of the D/A converter. The output driver of the TX chain is designed to deliver 12 $V_{p\text{-}p}$ diff into a 220-ohm load while maintaining 65-dB MTPR. This requires a technology which supports 10 V.

Spurious energy and cross-talk issues are addressed with circuit design techniques and process isolation. Fully differential circuit techniques are used. Separate supplies are used for the D/A, TX chain and RX chain and the serial interface.

Table I shows a summary of the AFE. Total power dissipation is about 750 mW. Figs. 15 and 16 show typical MTPR results from a section of the TX and RX spectrum.

Thermal noise, quantization noise, INL of the D/A converter and other sources of harmonic distortion theoretically limit the MTPR to 74 dB. The thermal noise floor of the part limits the MTPR further to 68 dB. Other degradation is due to harmonic distortion of opamps or test equipment limitations.

VII. Conclusion

This BiCMOS analog front-end (AFE) IC combines a 14-bit D/A converter with the analog TX and RX functions for an FDM-based ADSL modem. The IC features 14-bit TX performance, low noise, and high MTPR. The MTPR performance is achieved through a combination of good CMRR, PSRR, and low THD. The combination of high linearity and low noise maximizes the length of twisted pair copper wire over which the system can transmit while maintaining low BER.

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References

[1] E. Healy and G. Sheppard, "Communications semiconductor applications worldwide," Dec. 11, 1995, pp. 1–10.
[2] M. Kanefsky, *Communication Techniques for Digital and Analog Signals.* New York: Harper & Row, 1985, pp. 183–187.
[3] J. A. C. Bingham, "Multicarrier modulation for data transmission: An idea whose time has come," *IEEE Commun. Mag.*, May 1990, pp. 5–14.
[4] D. R. Gimlin and C. R. Patisaul, "On minimizing the peak-to-average power ratio for the sum of N sinusoids," *IEEE Trans. Commun.*, pp. 631–635, Apr. 1993.
[5] N. Al-Dhahir and J. Cioffi, "On the uniform ADC bit precision and clip level computation for a Gaussian signal," *IEEE Trans. Signal Processing*, pp. 434–438, Feb. 1996.
[6] B. J. Tesch and J. C. Garcia, "A low glitch 14-bit 100-MHz D/A converter," *IEEE J. Solid-State Circuits*, vol. 32, pp. 1465–1469, Sept. 1997.
[7] D. Mercer, "A 16-b D/A converter with increased spurious free dynamic range," *IEEE J. Solid-State Circuits*, vol. 29, pp. 1180–1185, Oct. 1994.
[8] R. C. Jaeger, "Unifying the concepts of offset voltage and common-mode rejection ratio" (corresp.); J-SC 76 Aug. 557-561 (2C11).

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