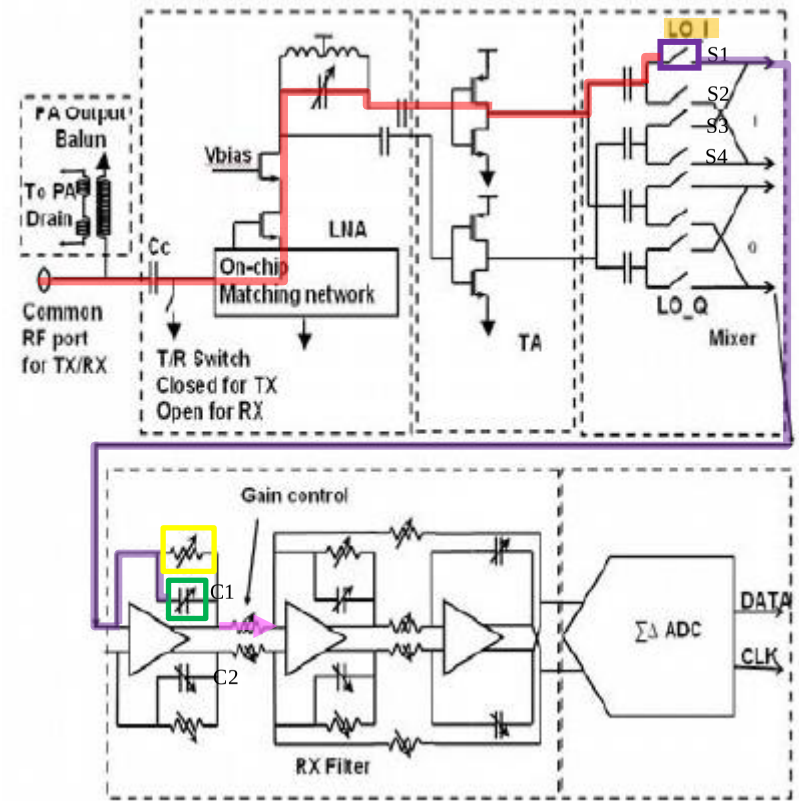
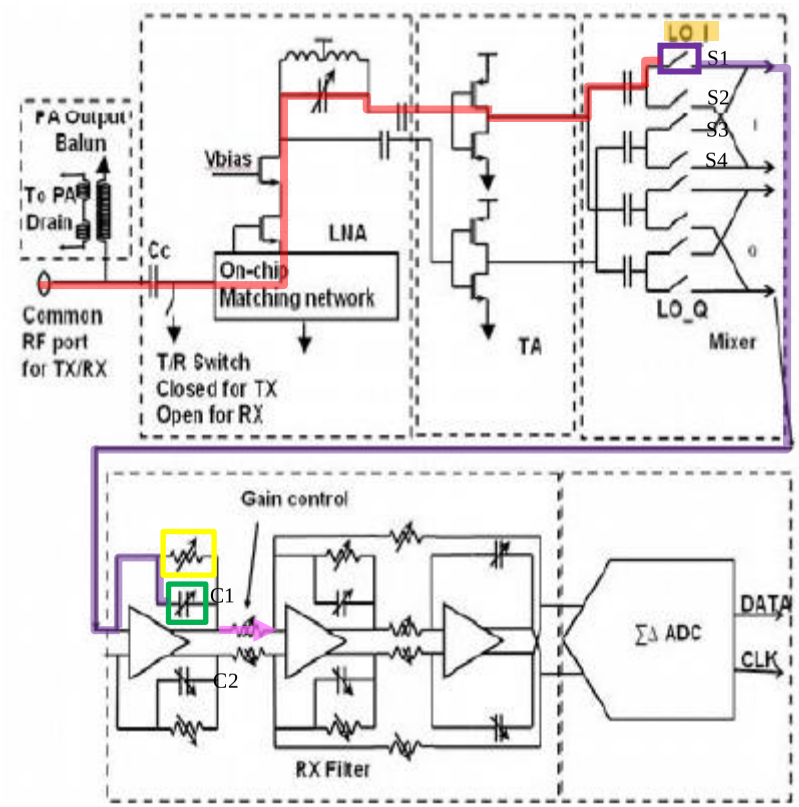
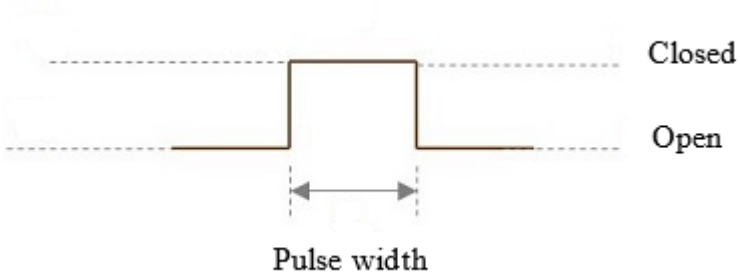
Claim Chart For Infringement of U.S. Patent No. 7,865,177 by TI Chips

Claim 14	TI Chips
A method for down-converting an electromagnetic signal, comprising:	TI directly infringes (literally and/or under the doctrine of equivalents) the '177 patent by making, using, selling, offering for sale, and/or importing in/into the United States products covered by at least claim 14 of the '177 patent. TI products that infringe claim 14 of the '177 patent include TI wireless chips (e.g., cellular, Wi-Fi and/or Bluetooth chips) including, without limitation, the AFE76XX series, AFE77XX series, AFE79XX series, AFE80XX series transceivers, and any other TI chip (collectively, "TI Chips") that is capable of down-converting an electromagnetic signal as claimed in the '177 patent. On information and belief, each TI Chip includes at least one or more switches/transistors that sample a carrier signal, one or more capacitors that store non-negligible amounts of energy from a carrier signal, and one or more resistors providing a low impedance load(s). On information and belief, the structure, function, and operation of TI Chips are substantially similar to one another with respect to the claims at issue. On information and belief, the TI Chips are described, in part, in the IEEE paper entitled "A Fully Integrated 2×2 b/g and 1×2 a-Band MIMO WLAN SoC in 45nm CMOS for Multi-Radio IC," by R. Kumar et al., *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers*, San Francisco, CA, USA, 2013, pp. 328-329 (hereinafter referred to as the 2013 IEEE paper). On information and belief, each TI Chip performs a method for down-converting an electromagnetic signal (e.g., high frequency RF signal) to a lower frequency signal (e.g., baseband signal). The method is performed on the receiver side of each TI Chip. For example, the AFE76XX "is a family of high performance, quad/dual channel, 14-bit, integrated RF sampling analog front ends (AFEs) with 9 GSPS DACs and 3 GSPS ADCs, capable of synthesizing and digitizing wideband signals."[1] Accordingly, each TI Chip is configured to receive an electromagnetic signal (e.g., high frequency RF signal). In order to process such a signal, each TI Chip must necessarily down-convert the electromagnetic signal to a baseband signal.

[1] https://www.ti.com/lit/ds/symlink/afe7686.pdf?ts=1701875653400&ref_url=https%253A%252F%252Fwww.ti.com%252Fproduct%252FAFE7686; *see also, e.g.*, https://www.ti.com/lit/ds/symlink/afe8004.pdf?ts=1701875867735&ref_url=https%253A%252F%252Fwww.google.com%252F; https://www.ti.com/lit/ds/symlink/afe7799.pdf?ts=1701875830461&ref_url=https%253A%252F%252Fwww.ti.com%252Fproduct%252FAFE7799; https://www.ti.com/lit/ds/symlink/afe7920.pdf?ts=1701876119308&ref_url=https%253A%252F%252Fwww.google.com%252F.

receiving an input signal at a first matched filtering /correlating module;	Each TI Chip receives an input signal (e.g., RF signal, represented by the red path) at a first matched filtering/correlating module (e.g., linear time-variant circuit, including a switch S1 (shown in the purple box), capacitor C1 (shown in the green box), and low impedance load (e.g., feedback resistor(s), shown in the yellow box), shown along the purple path).  Figure 19.1.4 of 2013 IEEE paper. The first matched filtering/correlating module receives the input signal RF along the red path.

down converting said input signal at said first matched filtering/correlating module according to a first control signal and outputting a first down-converted signal;	Each TI Chip down-converts the input signal (e.g., RF, represented by the red path) at the first matched filtering/correlating module (e.g., linear time-variant circuit, including a switch S1 (shown in the purple box), capacitor C1 (shown in the green box), and low impedance load (e.g., feedback resistor(s), shown in the yellow box), shown along the purple path) according to a first control signal (e.g., LO_I+, represented by LO_I in the orange box) and outputs a first down-converted signal (e.g., represented by the pink arrow).  Figure 19.1.4 of 2013 IEEE paper.

4	Switch S1 (purple box) includes transistors that operate as a switch with switching frequency and duty cycles controlled by LO_I+ (orange box). In particular, switch S1 (purple box) periodically opens and closes, thereby controlling the current flow of RF (red path) in the circuit. The time period for which switch S1 (purple box) is open/closed is determined by LO_I+ (orange box). Specifically, LO_I+ (orange box) enables (i.e., closes) switch S1 (purple box) during an aperture thereof. An aperture describes the pulse width of the control signal (i.e., the length of activation within the signal) when the switch is closed. The diagram below represents an exemplary waveform of control signal LO_I+.  When switch S1 (purple box) is ON (closed), current can pass through the switch S1; when the switch is OFF (opened), current is blocked from passing through the switch. The switch S1 is turned ON (closed) by sending control signal LO_I+ to the switch at an independent control input. The switch is kept ON (kept closed) for the duration of the signal pulse (i.e., during a sampling aperture of the pulse). On information and belief, the pulses of control signal LO_I+ have a non-negligible, periodic aperture (e.g., nominal 25% duty cycle). *See* N. Klemmer et al., "A 45nm CMOS RF-to-Bits LTE/WCDMA FDD/TDD 2×2 MIMO Base-Station Transceiver SoC with 200MHz RF Bandwidth," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2016, pp. 164-165; N. Klemmer (2016, February 2). *A 45nm CMOS RF-to-Bits LTE/WCDMA FDD/TDD 2×2 MIMO Base Station Transceiver SoC with 200MHz RF Bandwidth* [PowerPoint]. ISSCC, San Francisco, CA, USA; C. Yeh et al., "Multi-band, Multi-mode, Low-power CMOS Receiver Front-end for Sub-GHz ISM/SRD Band with Narrow Channel Spacing," *Proceedings of the IEEE 2012 Custom Integrated Circuits Conference*, San Jose, CA, USA, 2012, pp. 1-4.

	Successive pulses of LO_I+ (orange box) therefore recursively close/open switch S1 (purple box), which samples the RF signal (red path). The recursive closing/opening of switch S1 (purple box) periodically couples the RF signal (red path) to capacitor C1 (green box). During an aperture of LO_I+ (orange box), for example, switch S1 (purple box) closes and energy from RF (red path) is directed to capacitor C1 (green box) and load circuitry (e.g., feedback resistor(s), yellow box). On information and belief, non-negligible amounts of energy from the input signal are accumulated (e.g., in one or more capacitors) and transferred to a low impedance load (e.g., one or more feedback resistors) during an aperture period (e.g., when the switch is closed (ON)). Between apertures of LO_I+ (orange box), switch S1 (purple box) remains open, preventing the flow of energy through the switch and consequently discharging energy stored in capacitor C1 (green box) to load circuitry. In this way, real power from the input signal is transferred to the low impedance load and produces a down-converted signal with enhanced signal-to-noise power ratio. The sampling, charging, and discharging process outputs the first down-converted signal (e.g., pink arrow). Each TI Chip meets wireless telecommunication standards. *See, e.g.*, 2013 IEEE paper (discussing IEEE 802.11a, 802.11b, 802.11g, and 802.11n Wi-Fi standards); "AFE79xx Quad-Channel RF Transceiver with Feedback Path," TEXAS INSTRUMENTS, https://www.ti.com/lit/ds/symlink/afe7920.pdf?ts=1701878816296&ref_url=https%253A%252F%252Fwww.google.com%252F (discussing 3G/4G/5G cellular standards).

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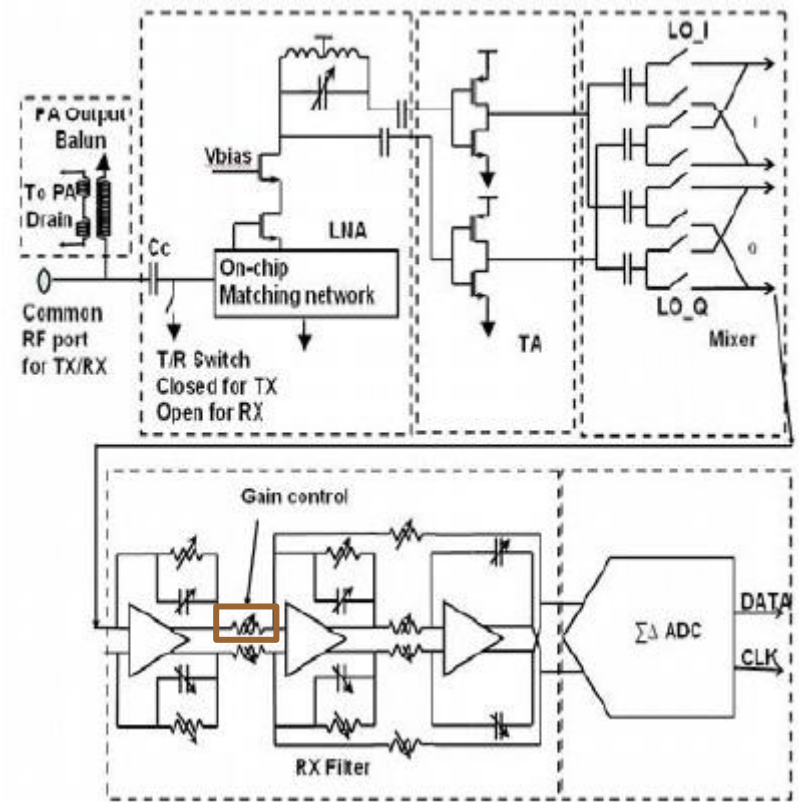
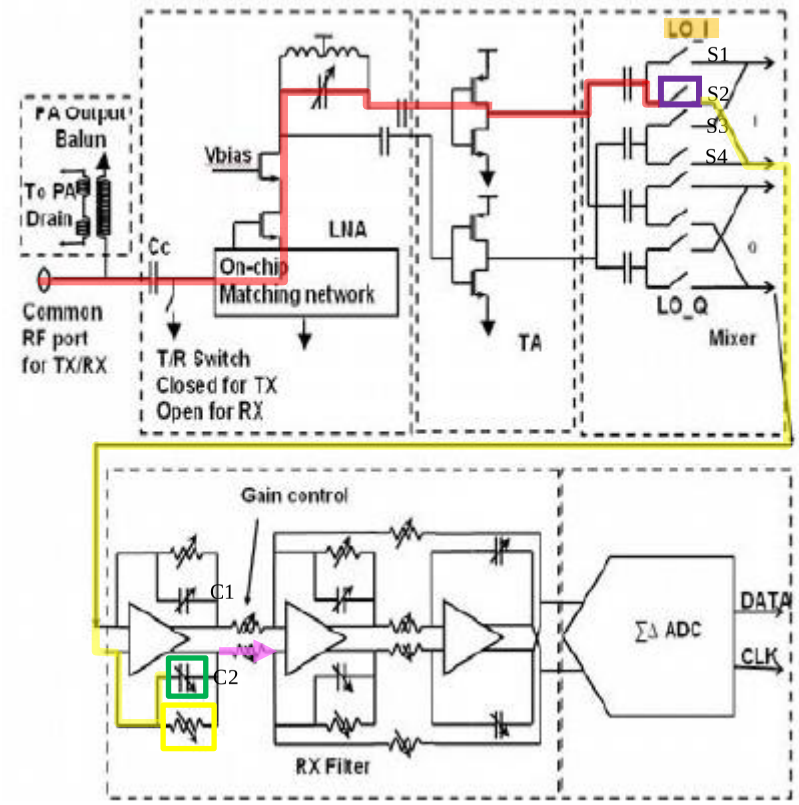
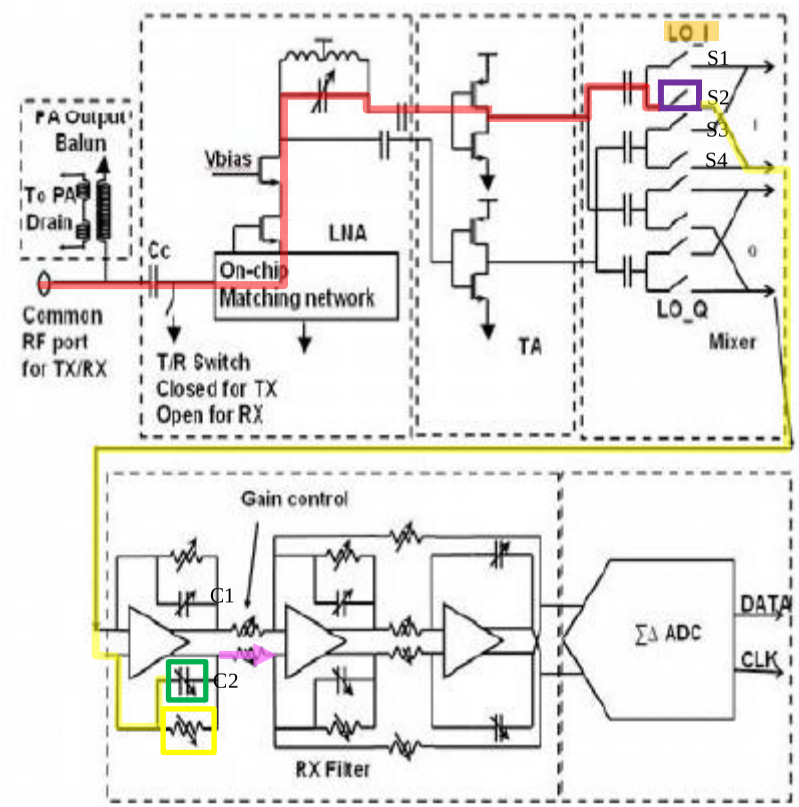
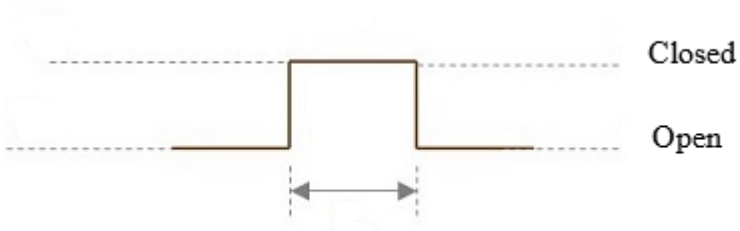
9	Alternatively, in addition to, or instead of the load circuitry shown above, the load includes the load circuitry shown in the brown box below.  Figure 19.1.4 of 2013 IEEE paper.

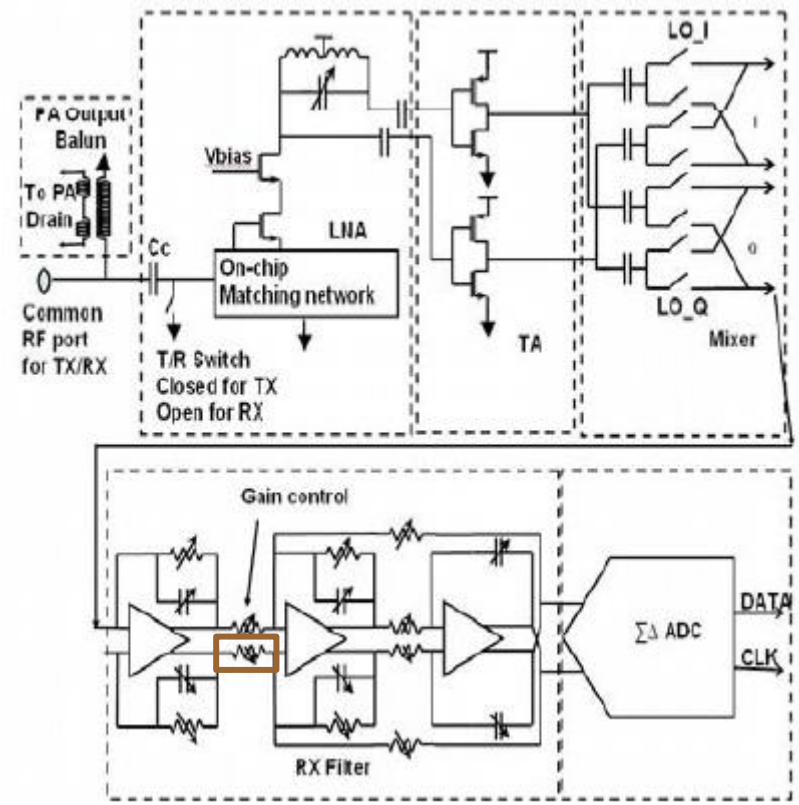
receiving said input signal at a second matched filtering/correlating module;	Each TI Chip receives the input signal (e.g., RF, represented by the red path) at a second matched filtering/correlating module (e.g., linear time-variant circuit, including a switch S2 (shown in the purple box), capacitor C2 (shown in the green box), and low impedance load (e.g., feedback resistor(s), shown in the yellow box), shown along the yellow path).  Figure 19.1.4 of 2013 IEEE paper. The second matched filtering/correlating module receives the input signal RF along the red path.

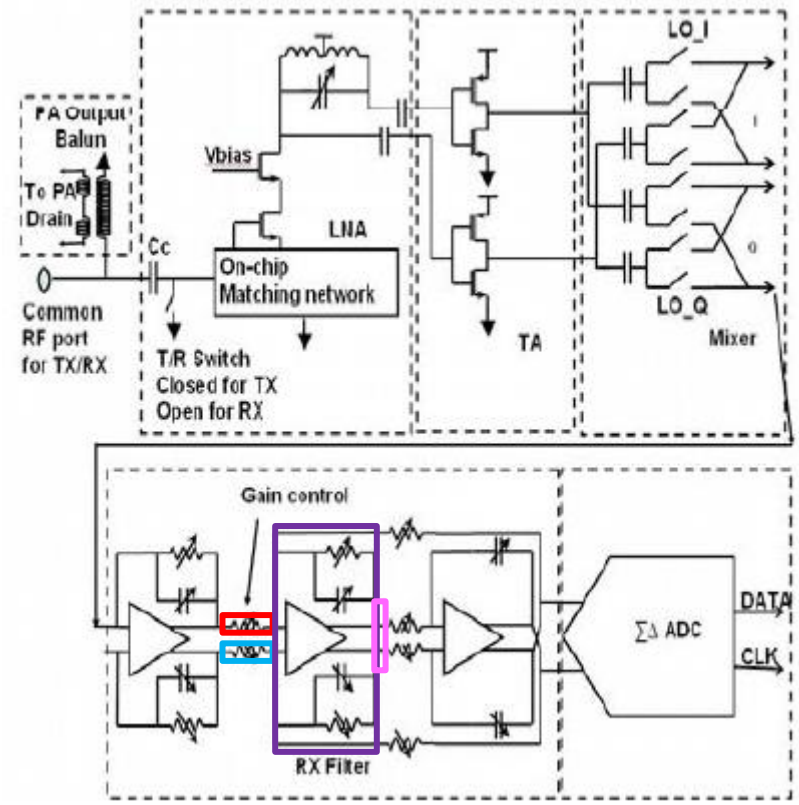
down-converting said input signal at said second matched filtering/correlating module according to a second control signal and outputting a second down-converted signal; and	Each TI Chip down-converts the input signal (e.g., RF, represented by the red path) at the second matched filtering/correlating module (e.g., linear time-variant circuit, including a switch S2 (shown in the purple box), capacitor C2 (shown in the green box), and low impedance load (e.g., feedback resistor(s), shown in the yellow box), shown along the yellow path) according to a second control signal (e.g., LO_I-, represented by LO_I in the orange box) and outputs a second down-converted signal (e.g., represented by the pink arrow).  Figure 19.1.4 of 2013 IEEE paper.

6	Switch S2 (purple box) includes transistors that operate as a switch with switching frequency and duty cycles controlled by LO_I- (orange box). In particular, switch S2 (purple box) periodically opens and closes, thereby controlling the current flow of RF (red path) in the circuit. The time period for which switch S2 (purple box) is open/closed is determined by LO_I- (orange box). Specifically, LO_I- (orange box) enables (i.e., closes) switch S2 (purple box) during an aperture thereof. An aperture describes the pulse width of the control signal (i.e., the length of activation within the signal) when the switch is closed. The diagram below represents an exemplary waveform of control signal LO_I-.  When switch S2 (purple box) is ON (closed), current can pass through the switch S2; when the switch is OFF (opened), current is blocked from passing through the switch. The switch S2 is turned ON (closed) by sending control signal LO_I- to the switch at an independent control input. The switch is kept ON (kept closed) for the duration of the signal pulse (i.e., during a sampling aperture of the pulse). On information and belief, the pulses of control signal LO_I- have a non-negligible, periodic aperture (e.g., nominal 25% duty cycle). *See* N. Klemmer et al., "A 45nm CMOS RF-to-Bits LTE/WCDMA FDD/TDD 2×2 MIMO Base-Station Transceiver SoC with 200MHz RF Bandwidth," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2016, pp. 164-165; N. Klemmer (2016, February 2). *A 45nm CMOS RF-to-Bits LTE/WCDMA FDD/TDD 2×2 MIMO Base Station Transceiver SoC with 200MHz RF Bandwidth* [PowerPoint]. ISSCC, San Francisco, CA, USA; C. Yeh et al., "Multi-band, Multi-mode, Low-power CMOS Receiver Front-end for Sub-GHz ISM/SRD Band with Narrow Channel Spacing," *Proceedings of the IEEE 2012 Custom Integrated Circuits Conference*, San Jose, CA, USA, 2012, pp. 1-4.

	Successive pulses of LO_I- (orange box) therefore recursively close/open switch S2 (purple box), which samples the RF signal (red path). The recursive closing/opening of switch S2 (purple box) periodically couples the RF signal (red path) to capacitor C2 (green box). During an aperture of LO_I- (orange box), for example, switch S2 (purple box) closes and energy from RF (red path) is directed to capacitor C2 (green box) and load circuitry (e.g., feedback resistor(s), yellow box). On information and belief, non-negligible amounts of energy from the input signal are accumulated (e.g., in one or more capacitors) and transferred to a low impedance load (e.g., one or more feedback resistors) during an aperture period (e.g., when the switch is closed (ON)). Between apertures of LO_I- (orange box), switch S2 (purple box) remains open, preventing the flow of energy through the switch and consequently discharging energy stored in capacitor C2 (green box) to load circuitry. In this way, real power from the input signal is transferred to the low impedance load and produces a down-converted signal with enhanced signal-to-noise power ratio. The sampling, charging, and discharging process outputs the second down-converted signal (e.g., pink arrow). Each TI Chip meets wireless telecommunication standards. *See, e.g.*, 2013 IEEE paper (discussing IEEE 802.11a, 802.11b, 802.11g, and 802.11n Wi-Fi standards); "AFE79xx Quad-Channel RF Transceiver with Feedback Path," TEXAS INSTRUMENTS, https://www.ti.com/lit/ds/symlink/afe7920.pdf?ts=1701878816296&ref_url=https%253A%252F%252Fwww.google.com%252F (discussing 3G/4G/5G cellular standards).

10

11	Alternatively, in addition to, or instead of the load circuitry shown above, the load includes the load circuitry shown in the brown box below.  Figure 19.1.4 of 2013 IEEE paper.

combining said second down-converted signal and said first down-converted signal to output a first channel down-converted signal.	Each TI Chip uses a differential amplifier circuit (e.g., differential amplifier circuit including operational amplifier (op-amp) with resistor-capacitor feedback, shown in the purple box) to combine the second down-converted signal (shown in the blue box) and the first down-converted signal (shown in the red box) to output a first channel down-converted signal (e.g., shown in the pink box).  Figure 19.1.4 of 2013 IEEE paper.

13	The differential amplifier circuit (purple box) receives two inputs, the first down-converted signal (e.g., shown in the red box) and the second down-converted signal (e.g., shown in the blue box), and outputs a down-converted signal (e.g., shown in the pink box), which is a function of the difference between the inputs. In particular, the differential amplifier circuit combines the first down-converted signal (red box) with the second down-converted signal (blue box) and outputs a down-converted signal (e.g., shown in the pink box) that is a function of the combination of the first and second down-converted signals.

10.1.2 Differential Signals

Let us return to the circuit of Fig. 10.2(a) and recall that the duplicate stage consisting of Q_2 and R_{C2} remains "idle," thereby "wasting" current. We may therefore wonder if this stage can provide signal amplification in addition to establishing a reference point for V_{out}. In our first attempt, we directly apply the input signal to the base of Q_2 [Fig. 10.3(a)]. Unfortunately, the signal components at X and Y are in phase, canceling each other as they appear in $v_X - v_Y$:

$$v_X = A_v v_{in} + v_\dagger \tag{10.5}$$

$$v_Y = A_v v_{in} + v_\dagger \tag{10.6}$$

$$\Rightarrow v_X - v_Y = 0. \tag{10.7}$$

For the signal components to *enhance* each other at the output, we can *invert* one of the input phases as shown in Fig. 10.3(b), obtaining

$$v_X = A_v v_{in} + v_\dagger \tag{10.8}$$

$$v_Y = -A_v v_{in} + v_\dagger \tag{10.9}$$

and hence

$$v_X - v_Y = 2A_v v_{in}. \tag{10.10}$$

B. Razavi, *Fundamentals of Microelectronics* at p. 439

Energy, power, current, voltage, resistance/impedance, and time relationships can be expressed as follows:

Energy Power Current Voltage Resistance Impedance Time Relationships

$$E = \left(\frac{J}{\Delta t}\right) \cdot \Delta t$$

$$P = \left(\frac{J}{\Delta t}\right)$$

$$E = P \cdot \Delta t$$

Where:

E is Energy in Joules
P is Power in Watts*
t is Time in Seconds
I is Current in Amperes
V is Voltage in Volts
R is Resistance or Impedance (Z) in Ohms

*Power is the rate of energy transfer

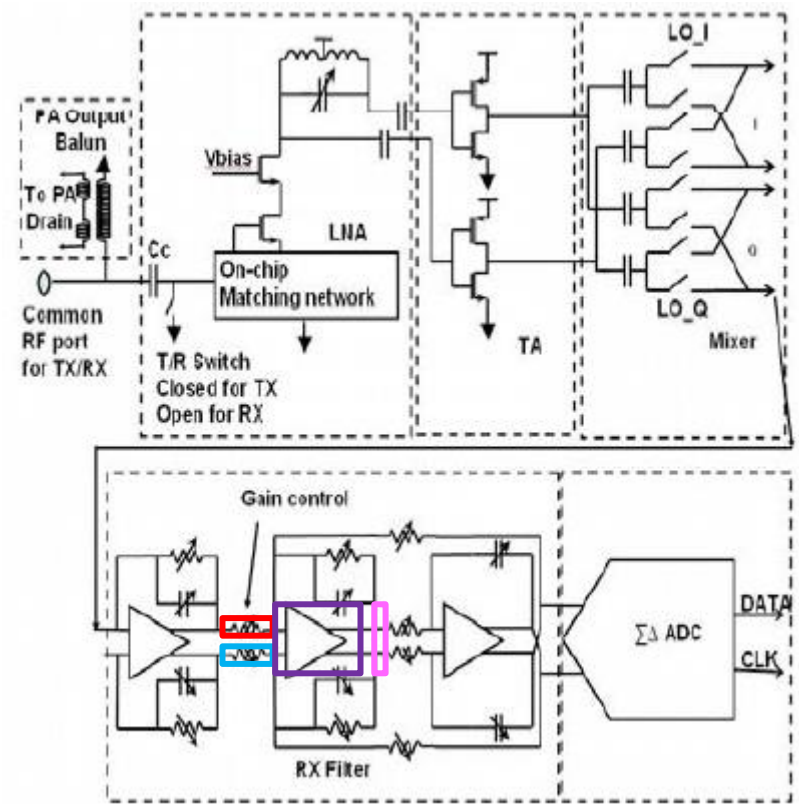
$$P = V \cdot I \qquad P = \left(\frac{V^2}{R}\right) \qquad P = I^2 \cdot R$$

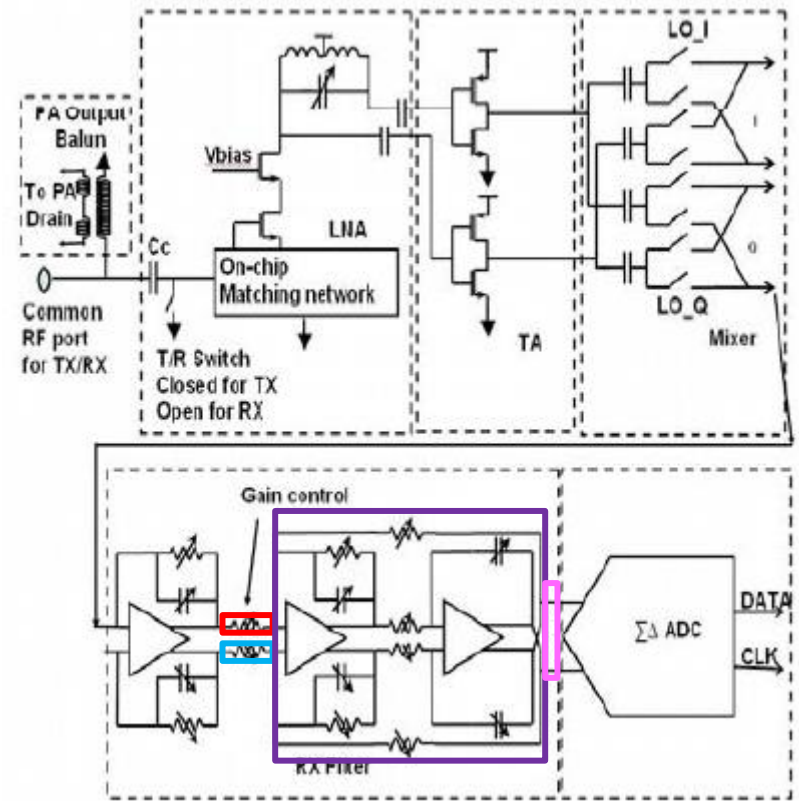
$$E = V \cdot I \cdot \Delta t \qquad E = \left(\frac{V^2}{R}\right) \cdot \Delta t \qquad E = I^2 \cdot R \cdot \Delta t$$

$$V = \left(\frac{E}{I \cdot \Delta t}\right) \qquad V = \sqrt{\left(\frac{E \cdot R}{\Delta t}\right)} \qquad I = \sqrt{\left(\frac{E}{R \cdot \Delta t}\right)}$$

$$I = \left(\frac{E}{V \cdot \Delta t}\right)$$

14

15	Alternatively, each TI Chip includes a differential amplifier circuit (e.g., differential amplifier including an operational amplifier (op-amp), shown in the purple box) that subtracts the second down-converted signal (e.g., shown in the blue box) from the first down-converted signal (e.g., shown in the red box) and outputs a first channel down-converted signal (e.g., shown in the pink box).  Figure 19.1.4 of 2013 IEEE paper.

16	Alternatively, each TI Chip includes a differential amplifier circuit (e.g., differential amplifier including an operational amplifier (op-amp) with resistor-capacitor feedback, shown in the purple box) that subtracts the second down-converted signal (e.g., shown in the blue box) from the first down-converted signal (e.g., shown in the red box) and outputs a first channel down-converted signal (e.g., shown in the pink box).  Figure 19.1.4 of 2013 IEEE paper.