UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BOE Technology Group Co., Ltd.
Petitioner

v.

Optronic Sciences LLC
Patent Owner

Inter Partes Review No.: IPR2025-00238

DECLARATION OF DR. R. JACOB BAKER IN REGARDING CLAIMS 1, 4, 6, 9, 12, 14, 17, and 18 OF U.S. PATENT NO. 8,604,471

I hereby declare under penalty of perjury under the laws of the United States of America that the following is true and correct, and that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true. I understand that willful false statements are punishable by fine or imprisonment or both under Section 1001 of Title 18 of the United States Code.

February 8, 2025
Date

Dr. R. Jacob Baker

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1005	U.S. 2010/0148175 (“**Godo**”)
1006	U.S. 2009/0184898 (“**Yamashita**”)
1007	Solid State Electronic Devices 4th Edition by Ben Streetman
1008	Handbook of Optics 2nd Edition Volume II by Michael Bass et al.
1009	KR 10-0853543B1
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CHART OF CLAIMS
[1pre] A semiconductor structure, disposed on a substrate, and comprising:
[1a] a gate electrode, disposed on the substrate;
[1b] a gate insulating layer, disposed on the substrate, and covering the gate electrode;
[1c] a channel layer, disposed on the gate insulating layer and located above the gate electrode, wherein the channel layer has a channel length L along a channel direction and has a first side and a second side opposite to the first side;
[1d] a source electrode and a drain electrode, located at the two opposite sides of the channel layer, and electrically connected to the first side and the second side of the channel layer, respectively;
[1e] a dielectric layer, covering the source electrode, the drain electrode and the channel layer; and
[1f] a conductive light-shielding pattern layer, disposed on the dielectric layer, and overlapped to a portion of the source electrode and a portion of the channel layer in a vertical projection, wherein the conductive light-shielding pattern layer does not overlap to the drain in the vertical projection, and the conductive light-shielding pattern layer and the channel layer have an overlapping length d1, and $0.3 \leqq d1/L \leqq 0.85$.
[4] The semiconductor structure as claimed in claim 1, wherein the conductive light-shielding pattern layer has a third side and a fourth side along the channel direction, the fourth side is overlapped to the channel layer in the vertical projection, wherein the overlapping length d1 is equal to a distance between the fourth side and the first side of the channel layer along the channel direction.
[6] The semiconductor structure as claimed in claim 1, wherein the source electrode and the drain electrode respectively cover a portion of the channel layer.
[9pre] An organic electroluminescence device, disposed on a substrate, and comprising:
[9a] a gate electrode, disposed on the substrate;
[9b] a gate insulating layer, disposed on the substrate, and covering the gate electrode;
[9c] a channel layer, disposed on the gate insulating layer and located above the gate electrode, wherein the channel layer has a channel length L along a channel direction and has a first side and a second side opposite to the first side;
[9d] a source electrode and a drain electrode, located at the two opposite sides of the channel layer, and electrically connected to the first side and the second side of the channel layer, respectively;

CHART OF CLAIMS
[9e] a dielectric layer, covering the source electrode, the drain electrode and the channel layer;
[9f] a conductive light-shielding pattern layer, disposed on the dielectric layer, and overlapped to a portion of the source electrode and a portion of the channel layer in a vertical projection, wherein the conductive light-shielding pattern layer does not overlap to the drain in the vertical projection, and the conductive light-shielding pattern layer and the channel layer have an overlapping length d1, and $0.3 \leqq d1/L \leqq 0.85$;
[9g] a lower electrode, disposed on the dielectric layer and electrically connected to the drain electrode;
[9h] an organic light emitting layer, disposed on the lower electrode; and
[9i] an upper electrode, disposed on the organic light emitting layer.
[12] The organic electroluminescence device as claimed in claim 9, wherein the conductive light-shielding pattern layer has a third side and a fourth side along the channel direction, the fourth side is overlapped to the channel layer in the vertical projection, wherein the overlapping length d1 is equal to a distance between the fourth side and the first side of the channel layer along the channel direction.
[14] The organic electroluminescence device as claimed in claim 9, wherein the source electrode and the drain electrode respectively cover a portion of the channel layer.
[17] The semiconductor structure as claimed in claim 1, wherein the conductive light-shielding pattern layer and the drain electrode are spaced by a distance along the channel direction in the vertical projection.
[18] The organic electroluminescence device as claimed in claim 9, wherein the conductive light-shielding pattern layer and the drain electrode are spaced by a distance along the channel direction in the vertical projection.

I. INTRODUCTION

I, R. Jacob Baker, declare as follows:

1. My name is R. Jacob Baker. I have been asked by Petitioner BOE Technology Group Co. Ltd. ("Petitioner") to provide my expert opinions in support of the above-identified petition for *inter partes* review of claims 1, 4, 6, 9, 12, 14, 17, and 18 ("Challenged Claims") of U.S. Patent No. 8,604,471 ("471 patent," EX1001), owned by Optronic Sciences LLP ("PO"), pursuant to 35 U.S.C. §§311–19 and 37 C.F.R. §42.100.

2. I currently hold the opinions set forth in this declaration.

3. In summary, it is my opinion that the references cited below render obvious the Challenged Claims. My detailed opinions on the claims are set forth below.

4. I am being compensated for my time at the rate of $765 per hour. This compensation is not contingent upon my performance, the outcome of this matter, or any issues involved in or related to this matter.

II. BACKGROUND AND QUALIFICATION

5. My qualifications generally are set forth in my Curriculum Vitae, which is attached as EX1016 and also includes a list of the publications I have authored and a list of the other cases in which I have testified during the last four years.

6. I have been working as an Engineer since 1985 and I have been teaching Electrical and Computer Engineering courses since 1991. I am currently a Professor Emeritus of Electrical and Computer Engineering at the University of Nevada, Las Vegas ("UNLV").

7. I received B.S. and M.S. degrees in Electrical Engineering from UNLV in 1986 and 1988, respectively. I received my Ph.D. in Electrical Engineering from the University of Nevada, Reno, in 1993.

8. My doctoral research, culminating in the award of a Ph.D., investigated the use of power MOSFETs in the design of very high peak power, and high-speed, instrumentation. I developed techniques to reliably stack power MOSFETs to switch higher voltages, that is, greater than 1,000 V and 100 Amps of current with nanosecond switching times. This work was reported in the paper entitled "Transformerless Capacitive Coupling of Gate Signals for Series Operation of Power MOSFET Devices," published in the IEEE Transactions on Power Electronics. The paper received the Best Paper Award in 2000.

A. Industry Experience

9. I have done technical and expert witness consulting for over 200 companies and their subsidiaries since I started working as an engineer in 1985. From 1985 to 1993, I worked for EG&G Energy Measurements and the Lawrence Livermore National Laboratory designing nuclear diagnostic instrumentation for

underground nuclear weapon tests at the Nevada test site. During this time, I designed, and oversaw the fabrication of, over 30 electronic and electro-optic instruments, including high-speed cable and fiber-optic receiver/transmitters, PLLs, frame and bit-syncs, data converters, streak-camera sweep circuits, Pockel's cell drivers, micro-channel plate gating circuits, charging circuits for battery backup of equipment for recording test data, and analog oscilloscope electronics.

10. My work during this time, as one example, had a direct impact on my doctoral research work using power MOSFETs, subsequent publishing efforts, and industry designs. In addition to the 2000 Best Paper Award from the IEEE Power Electronics Society, I published several other papers in related areas while working in industry. I hold a patent, Patent No. 5,874,830, in the area of power supply design, titled, "Adaptively biased voltage regulator and operating method," which was issued on February 23, 1999. I have designed dozens of linear and switching power supplies for commercial products and scientific instrumentation.

11. I am a licensed Professional Engineer and have extensive industry experience in circuit design, fabrication, and manufacture of Dynamic Random Access Memory (DRAM) semiconductor integrated circuit chips, Phase-Change Random Access Memory (PCRAM) chips, and CMOS Image Sensors (CISs) at Micron Technology, Inc. ("MTI") in Boise, Idaho. I spent considerable time working on the development of flash memory chips while at MTI. My efforts

resulted in more than a dozen patents relating to flash memory. One of my projects at MTI included the development, design, and testing of circuit design techniques for a multi-level cell (MLC) flash memory using signal processing. This effort resulted in higher-density memories for use in solid-state drives and flash memory cards having an ATA interface that are ubiquitous in consumer electronics, including cameras and data storage systems. Further, the use of higher-density memory can result in fewer changes in the flash translation layer for logical-to-physical addressing, less need for garbage collection, and larger data segments that can improve a computing system's performance. Another project I worked on at MTI focused on the design of buffers for high-speed double-data rate DRAM, which resulted in around 10 U.S. patents in buffer design. Among many other experiences, I led the development of the delay locked loop (DLL) in the late 1990s so that MTI DRAM products could transition to the DDR memory protocol, used in mobile and non-mobile (server, desktop, cell phones, tablets, etc.) computing systems as main computer memory, for addressing and controlling accesses to memory via interprocess communications (IPC) with the memory controller (MC). I provided technical assistance with MTI's acquisition of Photobit during 2001 and 2002, including transitioning the manufacture of CIS products into MTI's process technology. Further, I did consulting work at Sun Microsystems and then Oracle on the design of memory modules during 2009 and

2010. This work entailed the design of low-power, high-speed, and wide interconnection methods with the goal of transmitting data to/from the memory module and the MC at higher speeds.

12. I have extensive experience in the development of instrumentation and commercial products in a multitude of areas including: integrated electrical/biological circuits and systems, array (memory, imagers, and displays) circuit design, CMOS analog and digital circuit design, diagnostic electrical and electro-optic instrumentation for scientific research, CAD tool development and online tutorials, low-power interconnect and packaging techniques, design of communication/interface circuits (to meet commercial standards such as USB, firewire, DDR, PCIe, SPI, etc.), circuit design for the use and storage of renewable energy, and power electronics. For example, a part of my research at Boise State, for many years, focused on the use of Thru-Silicon-Vias (TSVs), aka Thru-Wafer Vias (TWVs), for high-density 3D packaging. These packaging techniques were utilized in the memory module development work I did with Sun Microsystems and Oracle. As another example, I designed circuitry for use in implementing Universal Serial Bus (USB) interface circuits while I did consulting at Tower Semiconductor. I designed PCI communication circuits for IPC between a Graphics Processor Unit (GPU) and memory while consulting for Rendition, Inc. From 1994 to 1996, I worked on the design of displays at Micron Display and

Micron Technology, Inc. (“Micron”) in Boise, Idaho. This work was at a time when cathode ray tubes (CRTs) were still the dominant type of display. Flat panel displays were being developed with the hope of replacing CRTs in the consumer market. I worked on flat panel displays which resulted in 5 patents: 5,598,156, 5,638,085, 5,818,365, 5,894,293, and 5,909,201. I worked on the design of the pixels, both active and passive, as well as the supporting electronics for processing video signals. I was also involved with the evaluation of display technologies including liquid crystal displays (LCDs), light-emitting diodes, plasma displays, and organic light emitting diode (OLED) displays; the display technologies that were looking to displace CRTs in the consumer market. I was involved with the packaging of the displays including the vacuum sealing and deposition of the phosphors for light wavelength conversion. I also taught display design as a topic in my courses and did display design consulting again in industry for Cirque in 2013.

13. My current research work is focused in part on the design of integrated circuits for wireless sensing using LIDAR (LIght Detection And Ranging). I have worked with several companies in the development of these circuits and systems including Freedom Photonics, Aerius Photonics, and FLIR. In the early 1990s, I worked on wireless systems for wideband impulse radar while at Lawrence Livermore Laboratory. Further, part of my research for several years

focused on the digitization of IQ channels using delta-sigma modulation. The knowledge and experience gained from this effort are reflected in my textbook CMOS Mixed-Signal Circuit Design and a presentation, which I have present-ed at several universities and companies, http://cmosedu.com/jbaker/papers/talks/BP_DSM_talk.pdf.

B. Academic Experience

14. I was an adjunct faculty member in the Electrical Engineering departments of UNLV and UNR from 1991-1993. From 1993 to 2000, I served on the faculty at the University of Idaho as an Assistant Professor and then as a tenured Associate Professor of Electrical Engineering. In 2000, I joined a new Electrical and Computer Engineering program at Boise State University ("BSU"), where I served as department chair from 2004 to 2007. At BSU, I helped establish graduate programs in Electrical and Computer Engineering including, in 2006, the university's second Ph.D. degree. In 2012, I re-joined the faculty at UNLV. Over the course of my career as a professor, I have advised more than 100 masters and doctoral students.

15. I have been recognized for my contributions as an educator in the field. While at Boise State University, I received the President's Research and Scholarship Award (2005), Honored Faculty Member recognition (2003), and Outstanding Department of Electrical Engineering Faculty recognition (2001). In

2007, I received the Frederick Emmons Terman Award (the "Father of Silicon Valley"). The Terman Award is bestowed annually upon an outstanding young electrical/computer engineering educator in recognition of the educator's contributions to the profession. In 2011, I received the IEEE Circuits and Systems Education Award. I received the Tau Beta Pi Outstanding Electrical and Computer Engineering Professor Award every year it was awarded while I have been back at UNLV.

16. I have authored several books and papers in the electrical and computer engineering area. My published books include CMOS Circuit Design, Layout, and Simulation (Baker, R.J., Wiley-IEEE, ISBN: 9781119481515 (4th ed., 2019)) and CMOS Mixed-Signal Circuit Design (Baker, R.J., Wiley-IEEE, ISBN: 9780470290262 (2nd ed., 2009) and ISBN: 9780471227540 (1st ed., 2002)). I co-authored DRAM Circuit Design: Fundamental and High-Speed Topics (Keeth, B., Baker, R.J., Johnson, B., and Lin, F., Wiley-IEEE, ISBN: 9780470184752 (2008)), DRAM Circuit Design: A Tutorial (Keeth, B. and Baker, R.J., Wiley-IEEE, ISBN: 0-7803-6014-1 (2001)), and CMOS Circuit Design, Layout and Simulation (Baker, R.J., Li, H.W., and Boyce, D.E., Wiley - IEEE, ISBN: 9780780334168 (1998)). I contributed as an editor and co-author on several other electrical and computer engineering books.

C. Other Relevant Experience

17. I have performed technical and expert witness consulting for more than 200 companies and their subsidiaries and given more than 50 invited talks at conferences, companies, and universities. Further, I am the author or co-author of more than 100 papers and presentations in the areas of electrical and computer engineering design, fabrication, and packaging.

18. I currently serve, or have served, as a volunteer on the IEEE Press Editorial Board (1999-2004); as editor for the Wiley-IEEE Press Book Series on Microelectronic Systems (2010-2018); as the Technical Program Chair of the 2015 IEEE 58th International Midwest Symposium on Circuits and Systems (MWSCAS 2015); on the IEEE Solid-State Circuits Society (SSCS) Administrative Committee (2011-2016); as a Distinguished Lecturer for the SSCS (2012-2015); the Technology Editor (2012-2014) and Editor-in-Chief (2015-2020) for IEEE Solid-State Circuits Magazine; IEEE Kirchhoff Award Committee (2020-2023); and advisor for the student branch of the IEEE at UNLV (2013-2024). These meetings, groups, and publications are intended to allow researchers to share and coordinate research. My active participation in these meetings, groups, and publications allowed me to see what other researchers in the field have been doing.

19. In addition to the above, I am an IEEE Fellow for contributions to semiconductor memory design and a member of the honor societies Eta Kappa Nu and Tau Beta Pi.

III. DOCUMENTS AND OTHER MATERIALS RELIED UPON

20. In forming the opinions set forth in this declaration, I have reviewed the documents in the following table:

Exhibit No.	Description
1001	U.S. Pat. No. 8,604,471 (**"the 471 Patent"**)
1003	File History of 8,604,471 (13/208,360)
1004	U.S. 2008/0158108 ("**Hwang**")
1005	U.S. 2010/0148175 ("**Godo**")
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1008	Handbook of Optics 2nd Edition Volume II by Michael Bass et al. ("**HandbookII**")
1009	KR 10-0853543B1 ("**Lee543**")
1010	Certified translation of Lee543
1011	KR 10-0659756B1 ("**Lee756**")
1012	Certified translation of Lee756
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1014	Schaum's Outline of Theory and Problems of Basic Circuit Analysis 2nd Edition by John O'Malley
1015	U.S. Pat. No. 5,838,399
1016	Curriculum Vitae of Dr. R. Jacob Baker
1017	Initial Infringement Contentions for U.S. Patent No. 8,604,471
	IPR2021-01541 Paper 39 (Final Written Decision) Home Depot USA, Inc. v. Lynk Labs, Inc.
	IPR2022-00023 Paper 40 (Final Written Decision) Home Depot USA, Inc. v. Lynk Labs, Inc.
	U.S. 2008/0278435
	U.S. 2011/0215337

Exhibit No.	Description
	U.S. 2011/0198607
	U.S. 2007/1076554

21. Additionally, I have utilized my own experience and expertise, including regarding the knowledge and capabilities of a person of ordinary skill in the relevant art in the timeframe of the claimed priority date of the 471 patent.

IV. STATUTORY GROUNDS FOR CHALLENGE

22. In this declaration, I offer opinions on the following grounds that are the basis for this IPR proceeding:

Ground	Claims	Basis	Prior Art
1	1, 4, 6, 9, 12, 14, 17, 18	§103	Hwang
2	Same	§103	Hwang and Godo
3	Same	§103	Hwang and Yamashita
4	Same	§103	Hwang, Godo and Yamashita

V. RELEVANT PATENT LAW AND LEGAL STANDARDS

A. Date of Invention

23. I have been asked to use the date of the filing of the earliest application to which priority is claimed (i.e., May 24, 2011) as the date of invention for purposes of my analysis.

B. Anticipation

24. I am informed and understand that a patent claim is invalid under 35 U.S.C. § 102 if a prior art disclosure teaches every element required by the claim,

either expressly or inherently. The identical invention must be shown in as complete detail as is contained in the claim. When a claim covers several structures or compositions, either generically or as alternatives, the claim is deemed anticipated if any of the structures or compositions within the scope of the claim is known in the prior art.

C. Obviousness

25. I am informed and understand that a patent claim is invalid under 35 U.S.C. § 103 if the differences between the invention and the prior art are such that the subject matter as a whole would have been obvious at the time of the invention to a person having ordinary skill in the art to which the subject matter pertains. Obviousness, as has been explained to me, is based on (i) the scope and content of the prior art, (ii) the differences between the prior art and the claim, (iii) the level of ordinary skill in the art, and (iv) any secondary indicia of non-obviousness (*e.g.*, "secondary considerations" such as commercial success in the marketplace of the claimed invention), to the extent that they exist.

26. I further understand that obviousness may be demonstrated by showing that it would have been obvious to combine the teachings of more than one item of prior art. In determining whether a piece of prior art could have been combined with other prior art or with other information within the knowledge of a

person having ordinary skill in the art, the following are examples of approaches and rationales that may be considered:

- Combining prior art elements according to known methods to yield predictable results;
- Simple substitution of one known element for another to obtain predictable results;
- Use of a known technique to improve similar devices (methods, or products) in the same way;
- Applying a known technique to a known device (method or product) ready for improvement to yield predictable results;
- Applying a technique or approach that would have been obvious to try (choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success);
- Known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations would have been predictable to a person having ordinary skill in the art; and
- Some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art

reference or to combine prior art reference teachings to arrive at the claimed invention.

27. I further understand that an invention may be obvious if one of ordinary skill in the art, facing a wide range of needs created by developments in the field, would have seen an obvious benefit to the solutions tried by the applicant. When there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, it may be obvious to a person of ordinary skill to try the known options. If a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique would have been obvious.

28. I further understand that a person of ordinary skill in the art is a hypothetical person who is presumed to be aware of all of the relevant art at the time of the invention. The person of ordinary skill may be able to fit together the teachings of multiple patents and/or printed publications employing ordinary creativity and the common sense that familiar items may have uses in another context or beyond their primary purposes.

29. I also understand that when considering the obviousness of a patent claim, one should consider whether a teaching, suggestion, or motivation to combine the references exists so as to avoid impermissibly applying hindsight

when combining or modifying the prior art. I understand this test should not be applied rigidly, but that the test can be important to avoid such hindsight.

30. I also understand that one of ordinary skill in the art must have a reasonable expectation of success in combining or modifying prior art references.

31. I also understand that all elements of a claim must be considered in an obviousness analysis.

D. Claim Construction

32. I understand that claims are construed from the perspective of a person of ordinary skill as of the effective filing date of the patent application. A "person of ordinary skill in the art" is a hypothetical person who is presumed to have known the relevant art at the time of the invention.

33. I understand that persons of ordinary skill in the art are deemed to read the claims in the context of the entire patent, including the specification and prosecution history. In other words, the terms are not considered in a vacuum.

34. I understand that the claims define the invention and the terms used in the claims are generally given the plain and ordinary meanings they would have to a person of ordinary skill in the art at the time of the effective filing date of the application. The context of a claim can be particularly helpful, and other claims may inform the meaning of a term in a particular claim.

35. I understand that claim terms are normally used consistently throughout a patent. Thus, the meaning of a term may help inform the meaning of the same term in other claims. Differences between claims may also help define the terms, although this may not be the case where the specification or prosecution history indicate that such differences do not impact the scope of the claims.

36. I understand that a patentee can act as its own lexicographer by defining a term, in the patent specification, to have specific meaning. It is my understanding that statements made to the patent office by the patentee or its legal representative during prosecution can serve to illuminate, or possibly narrow the proper scope of claim terms, and that such statements must be considered when construing the claim terms. This is sometimes referred to as disclaimer. I have taken into account these principles in my analysis.

37. I understand that reference materials that were publicly available at the time that the patent application was filed, such as dictionaries, treatises or other technical references, may provide context and background for deciphering how one of ordinary skill in the art would have considered the terms used in the claims.

38. However, I understand that such references, as well as testimony (including this report) are generally known as “extrinsic evidence,” and are accorded less weight than evidence found within the patent and prosecution history. In addition, I understand that extrinsic evidence that is inconsistent with

the claims, specification, or prosecution history should not be considered in the claim construction process.

E. Section 112(f) Means Plus Function

39. I understand that under pre-America Invents Act (AIA) 35 U.S.C. § 112(6) and post-AIA § 112(f) "An element in a claim for a combination may be expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof."

40. I understand that when claim terms use the words "means . . . for" and recites a function, and the term does not recite any structure for performing that function, the term should be construed pursuant to Section 112(f) looking for a corresponding structure, material, or act described in the specification and equivalents.

F. Section 112 Definiteness

41. I understand that "[t]he specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention."[1]

[1] I understand that the quoted text comes from the patent statute, 35 U.S.C. § 112 ¶ 2.

42. I understand that that claims must be definite. This means that the claims must particularly point out and distinctly claim the subject matter that the applicant regards as her invention. I understand that indefiniteness is evaluated from the perspective of a person of ordinary skill in the art at the time of a patent's filing. I understand that a patent claim is indefinite if the claim, when read in light of the specification and the prosecution history, fails to inform, with reasonable certainty, a person of ordinary skill in the art of the scope of the invention. Absolute or mathematical precision in claim language is not required and even if more than one interpretation is presented for a claim term, the term may still be definite if an informed and confident choice is available among the contending alternative definitions.

G. Standard of Proof

43. I understand that the standard to prove unpatentability in an *inter partes* review proceeding is by a preponderance of the evidence, which means more likely than not.

VI. THE 471 PATENT

A. Overview of the 471 Patent

44. The 471 patent was filed on August 12, 2011, claiming priority to a foreign application filed on May 24, 2011, and issued on December 10, 2013. EX1001, Face of Patent.

45. The 471 patent purports to improve the quality of a display by utilizing a light-shielding layer which overlaps channel layer of a thin film transistor to reduce the adverse effects of light irradiation including drain induced barrier lowering (DIBL) and associated current leakages. EX1001, 1:33-39, 3:8-21, 6:29-51.

46. The 471 patent discloses a semiconductor structure as shown in the embodiments in Figs. 1A-4B. Exemplary Figure 4A includes the components as follows: a substrate (12), channel layer (430), gate insulating layer, gate electrode, source electrode (440), drain electrode (450), dielectric layer, and conductive light-shielding pattern layer.

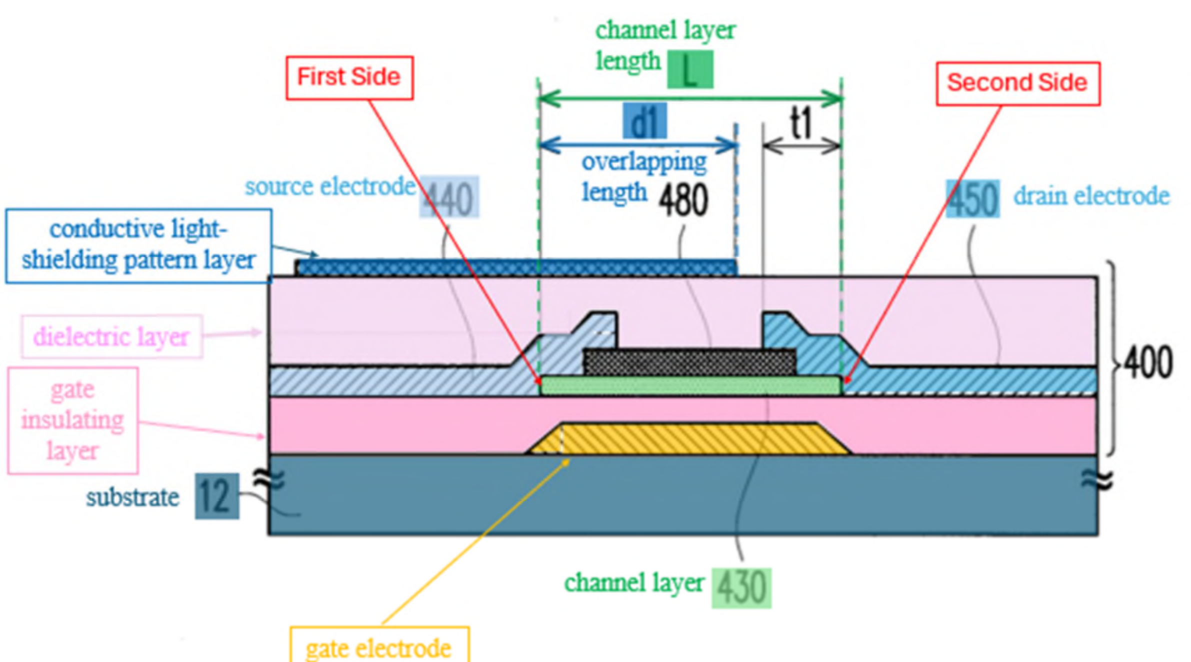


FIG. 4A

EX1001, Fig. 4A, 4:06-23, 5:55-6:07.

47. The purported key innovation is reducing the DIBL effect by including a conductive light-shielding pattern layer that overlaps, in part, a channel layer. EX1001, Fig. 5A-5B, 6:22-39. The 471 patent defines the length "L" of the channel layer[2] and the length "d1" of the overlapping portion of the conductive light-shielding pattern layer as shown Fig. 4A, and claim a range of overlap based on d1/L. EX1001, 4:06-23, 5:31-34, 5:46-50, 6:22-39, claims [1f][3], 4, [9f], 12. The structures of the disclosed and claimed embodiments are discussed in more detail below with respect to claim construction.

B. Overview of the 471 patent's File History

48. The 471 patent was filed as Appl. No. 13/208,360 on August 12, 2011. EX1001, Face of Patent.

49. On Mar. 29, 2013, the examiner rejected all claims in the original application. EX1003, 46-53. The examiner rejected claims 1 and 4 over Song et al. (2008/0278435) in view of Egami (2011/0215337) in view of Mori (2011/0198607), stating it would have been obvious to a POSITA to "include the required relationship among light shield, channel, source and drain…in order to

[2] As used in the 471 patent, the "channel layer" includes the portions of the layer that are above (or under) the source and drain electrodes (e.g., length t1). *See, e.g.,* EX1001, Figs. 1A, 3A, 4A, and claims 5, 6, 8. Thus, the "channel layer" is not limited to only the channel region of the thin film transistor.

[3] *See* definition of limitation in the chart of claims.

have a semiconductor device with low leakage." EX1003, 47-48. The examiner rejected claims 9 and 12, over Song in view of Kwak (2007/1076554) in view of Mori with the same reasoning. EX1003, 50-51.

50. On June 28, 2013, the applicant amended exemplary claim [1f] as follows:

> a conductive light-shielding pattern layer, disposed on the dielectric layer, and overlapped to a portion of the source electrode and a portion of the channel layer in a vertical projection, wherein the conductive light-shielding pattern layer does not overlap to the drain in the vertical projection, and the conductive light-shielding pattern layer and channel layer have an overlapping length d1, and $0.3 \leq d1/L \leq 0.85$.

EX1003, 30, 32, 35-40.

51. On Sept. 16, 2013, the examiner allowed the amended claims because the "prior art failed to establish the amended conductive light shielding pattern that does not overlap [sic] with the drain electrode." EX1003, 13. The claims issued on December 10, 2013. EX1001, Face of Patent. The prior art asserted herein discloses the limitation that was the basis for allowance (and all the others) as shown below.

C. Person of Ordinary Skill in the Art

52. A person of ordinary skill in the art at the time of the alleged invention of the 471 patent (the earliest claimed priority date of May 24, 2011)

("POSITA") would have had a Bachelor's degree in electrical or a comparable field of study, plus approximately one or more years of professional experience with electronic and optoelectronic system design. Additional graduate education could substitute for professional experience, and significant experience in the field could substitute for formal education.

VII. CLAIM CONSTRUCTION UNDER 37 C.F.R. § 42.104(B)(3)

53. The Challenged Claims are interpreted using the same claim construction standard that is used to construe the claim in a civil action in federal district court. 37 C.F.R. § 42.100(b).

54. Because the prior art asserted herein discloses the preferred embodiment within the indisputable scope of the claims, the Board need not construe the outer bounds of the claims as part of these proceedings. *See, e.g.*, *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017).

55. Any claim terms not listed below should be construed according to their plain and ordinary meaning to a POSITA at the time of the 471 patent.

1. "a conductive light-shielding pattern layer"

a. Primary Construction

56. This term is entitled to its ordinary meaning, which is not limited to any particular degree of conduction or light-shielding. For example, there is no claimed minimum level of electrical conductivity or percent optical opacity. The

prior art applied herein discloses (or at last renders obvious) a significant amount of conductivity and light-shielding. Thus, it is not necessary for the Board to construe the outer bounds of these limitations.

57. As for "conductive," the specification states several times that the pattern layer is "conductive" and makes clear that "conductive" refers to electrical conductivity. EX1001, 4:40-5:9 (disclosing the conductive light-shielding pattern is made from the same metal material as the lower electrode of the LED device). But the amount of conductivity is not discussed in the specification. Thus, there is no definition or disclaimer that could properly limit the claim. Nor is there a disclosed level of conductivity that could improperly be read into the claim.

58. As for "light-shielding," the specification describes that the pattern layer "can mitigate the DIBL effect, and shield a certain amount of the light (for example, an ultraviolet (UV) light) in the light irradiation step to reduce the influence on the channel layer 130 caused by the light irradiation." EX1001, 4:6-24. The "irradiation step" is performed during packaging. *Id.*, 1:29-33. The ordinary meaning of this limitation is not limited to a) the intended purpose of mitigating the DIBL effect, b) the intended (and indefinite) "certain amount" of light shielding, c) the intended type of light-shielding (UV irradiation during packaging), or d) the intended shielded object (the channel layer). This limitation

does not recite those limitations and there is no disclaimer or definition that could properly limit this limitation to those purposes.

59. I am informed and understand that these intended purposes should not be read into the claim because it is improper to do so. *See, e.g.*, Paper 39 (Final Written Decision) *Home Depot USA, Inc. v. Lynk Labs, Inc.* IPR2021-01541, at 16-17 (refusing to read in "light enhancing" or any degree of reflectivity into the limitation "reflective substrate"); Paper 40 (Final Written Decision) *Home Depot USA, Inc. v. Lynk Labs, Inc.* IPR2022-00023, at 12-14 ("Neither Claim 1 nor any of the dependent claims 2–4 require that the "reflective material" reflect any minimum amount of light.")

60. Here, it would be improper to read in a "certain amount" of light-shielding for the additional reason that the specification does not disclose what the "certain amount" is, so reading in a "certain amount" would render the claims indefinite.

61. The intrinsic record is clear that the claims merely recite the physical arrangement of a conductive light-shielding pattern relative to certain other claimed components. As long as the claimed physical arrangement is satisfied, and as long as the pattern layer has some amount of conductivity and light-shielding, nothing else is required by the ordinary meaning of the claim.

62. The only other guidance in the specification is that a layer made of "metal" in the claimed physical arrangement is an example of a conductive light-shielding pattern layer. EX1001, 3:58-61, 4:40-5:9. Accordingly, a POSITA would have understood that a metal layer which satisfies the claimed physical arrangement to be within the scope of this limitation.

b. Alternative Construction

63. I have been asked to consider the validity of the claims under the alternative construction of "a layer that the designer subjectively intends to serve the purpose of being electrically conductive and shielding the channel layer from some light." I am informed that Petitioner offers this alternative construction out of an abundance of caution in case PO attempts to argue that some aspects of the specification should be read into the claim.

64. This construction reads in the unclaimed but disclosed intended purpose of shielding the channel layer from some light (which would result in some mitigation of the DIBL effect) and that the designer intend that purpose. This construction does not read in the intended wavelength of light (UV) or the intended step during which the light shielding occurs (during packaging). This construction also does not read in any degree of conductivity or light shielding, because there is no sufficiently definite teaching in the specification that could be read into the claim.

65. As explained below, in Grounds 1 and 2, it would have been inherent, or at least obvious, for Hwang's metal layer 162a to perform the function of light-shielding. In Grounds 3 and 4, based on the teachings of Yamashita, it would have been obvious for the designer to intend that Hwang's metal layer 162a serve that purpose.

VIII. OVERVIEW OF THE PRIOR ART REFERENCES

A. EX1004 – Hwang

66. US 2008/0158108 to Hwang et al. ("**Hwang**") was published on July 3, 2008 and is prior art under at least Pre-AIA Section 102(b).

67. Hwang generally relates to OLED devices. EX1004, Abstract, [0002]. Hwang's device architecture involves OLEDs arranged above drive transistors that are bottom-gate thin film transistors ("TFTs"). EX1004, [0014]-[0016], Figs, 6A-6D. Hwang addresses a problem in art where the current applied to the OLED element induces an electric field that affects the channel region of a drive transistor. *Id*. Hwang discloses a solution to the problem by including a metal shielding layer overlying the channel and source regions (but not the drain region) of the driver transistor underneath to shield them from the electric field generated by the LED. EX1004, [0017]-[0020], [0050], [0072], [0101]. By incorporating the shielding layer, the image quality of the overall luminescent display device is

improved, such as by preventing brightness reduction or unintended brightness non-uniformity. EX1004, [0141]-[0142].

B. EX1005 – Godo

68. US 2010/0148175 to Godo et al. ("Godo") was published on June 17, 2010, filed on Dec. 8, 2009, and is prior art under at least Pre-AIA Sections 102(a) and (e).

69. Godo generally relates to TFTs (including bottom gate transistors) used in LED display devices. EX1005, Abstract, [0001]-[0002], Figs. 18A/B. Godo addresses a problem with light leakage current in TFTs that arises when the semiconductor layer in the TFT is irradiated by incident light. EX1005, [0003]-[0005]. Godo discloses a solution to this problem is to provide a metallic light-blocking material arranged to shield the channel region in the TFT from incident light. EX1005, [0006]-[0008], [0012], [0015]-[0016]; [0045]. By addressing the light leakage current, the performance of the display device can be improved with a high contrast ratio and low power consumption. EX1005, [0016]. Although suitable dimensions for TFTs to drive LED devices are generally well known in the art (as evidenced by the general lack of specificity in disclosed TFT dimensions in prior art patent documents, demonstrating that its express disclosure is unnecessary to provide an enabling disclosure), Godo provides some specific dimensions that would be suitable for bottom gate thin film drive transistors. EX1005, Figs. 20A/B.

C. EX1006 – Yamashita

70. US 2009/0184898 to Yamashita at el. ("Yamashita") was published on July 23, 2009 and is prior art under at least Pre-AIA Section 102(b).

71. Yamashita also relates to electroluminescent display devices with TFT drive transistors. EX1006, Abstract, [0002]-[0009]. Yamashita addresses a problem arising from light irradiation into the channel region of TFT's, namely, the shift in threshold voltage and carrier mobility that leads to unintended variations in the LED brightness. EX1006, [0012]-[0016], [0035]-[0038]. Yamashita teaches that the source of light irradiation on a TFT in one pixel can even originate from LED devices in adjacent pixels. EX1006, [0036]-[0037], Fig. 7. Similar to Godo, Yamashita also teaches to solve this problem by including a metallic light-shielding layer to prevent the internally scattered light from entering the channel region of the TFT and shifting the TFT threshold voltage. EX1006, [0046]-[0049], [0093]-[0100], Fig. 13.

D. Analogous Art

72. Each of Hwang, Godo, Yamashita and the other references discussed herein is analogous art to the 471 patent because each is related to semiconductor structures for a light emitting device. EX1001, 1:18-20.

IX. GROUND 1: HWANG

A. Hwang

73. The determination of obviousness is always made from the perspective of a POSITA. As discussed below, the teachings of Hwang would have rendered the claims obvious in view of the knowledge of a POSITA.

B. Knowledge of POSITA regarding light shielding

74. As discussed below for limitation [1f]/[9f], the teachings of Hwang would have rendered the claims obvious in view of the knowledge of a POSITA.

75. The problems associated with light entering a channel region of a transistor and the adverse impacts on transistor performance are well-known and extensively documented in the prior art. Some exemplary references are summarized herein. Light can create electron-hole pairs ("EHPs") in semiconductors and thus alter the density of charge carriers in the material. EX1007, 96-97, 103; *see generally* Chapter 4. These EHPs alter the electrical properties of the semiconductor (and thus the device), including *e.g.*, the threshold voltages in transistors and/or increase leakage current. These problems are especially acute for optoelectronic devices due to the presence of light generating elements integrated with, and in close proximity to, such transistors.

76. This problem is discussed in Yamashita. Yamashita relates to organic electroluminescent devices that incorporates transistor circuitry. EX1006, [0009]-[0010]. Yamashita addresses the known problem in the art when light enters the

channel region of a transistor and causes a shift in the threshold voltage of the transistor. EX1006, [0036]-[0038]. Yamashita discloses that in such devices, light can enter a channel region of a transistor (even one located in an adjacent pixel) due to internal scattered light from repeated reflections. EX1006, [0035]-[0037], Fig. 7. Such shifts in the threshold voltage are undesirable in drive transistors for organic light emitting diodes ("OLEDs") as they lead to unintended fluctuations in the drive current, and therefore fluctuations in the brightness of the OLED element. EX1006, [0013]-[0015], [0038]-[0042], Figs. 8-9. Yamashita discloses a solution to this problem is to form a light-shielding layer that is arranged above the channel region of the TFT in order to shield it from light. EX1006, [0045]-[0048], [0052], [0095]-[0099] (disclosing "the light shield pattern 67 should preferably be so arranged as to cover the sampling transistor T1 as well as the entire channel layer of the driving transistor T2"), Fig. 13. Yamashita discloses that while any material that reduces the amount of scattered light entering the thin-film transistor would help address the problem, metal materials are superior. EX1006, [0048]-[0049], [0136]-[0137]. Yamashita further teaches that the metal light-shielding layer should be electrically connected to a constant potential line. EX1006, [0047], [0101]-[0103].

77. Similarly, Godo discloses that it is well-known in the art that when semiconductor material (in a transistor of a display device) is irradiated with light,

light leakage current will be generated due to the photovoltaic effect and deteriorates the display quality. EX1005, [0004]. Godo discloses that mitigation techniques such as shielding the semiconductor layer from light were known. *Id.*, [0004]-[0006]. Reducing the leakage current can be accomplished by shielding the semiconductor layer with a conductive electrode made with various metals and their alloys. *Id.*, [0012]; [0015]-[0016]; [0045].

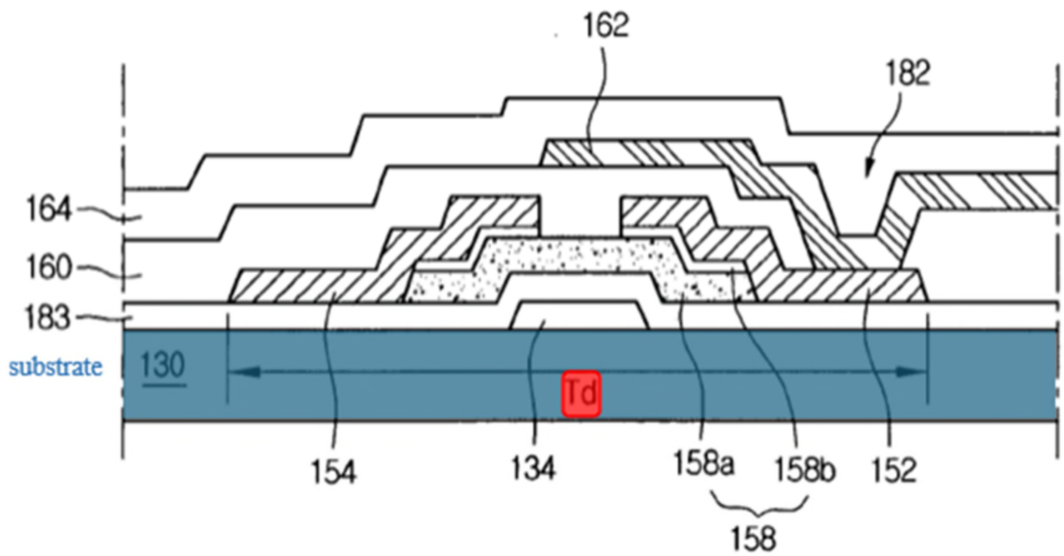
78. KR100853543 likewise discloses the use of a light-blocking film in an OLED display to stop light (external or from an adjacent pixel) from entering the semiconductor layer of a TFT to ensure stable driving properties for the transistor. EX1010, Abstract, <9>, <16>, <38>, <39>. KR100853543 explains that this light can generate a photocurrent in the semiconductor layer and adversely impact the driving properties of the TFT. EX1010, <15>.

79. KR100659756 is yet another reference that discloses the problem with light entering the semiconductor layer of a TFT, particularly those with a bottom-gate structure. EX1012, 5. KR100659756 discloses to use one or more metals (including aluminum and molybdenum that are good light reflectors and good electrical conductors) as suitable materials for forming a light-blocking film to prevent both external light as well as internally generated light (*e.g.* from the OLED) from causing a negative effect on the TFT. EX1012, 7.

C. Claim 1

1. [1pre] A semiconductor structure, disposed on a substrate, and comprising:

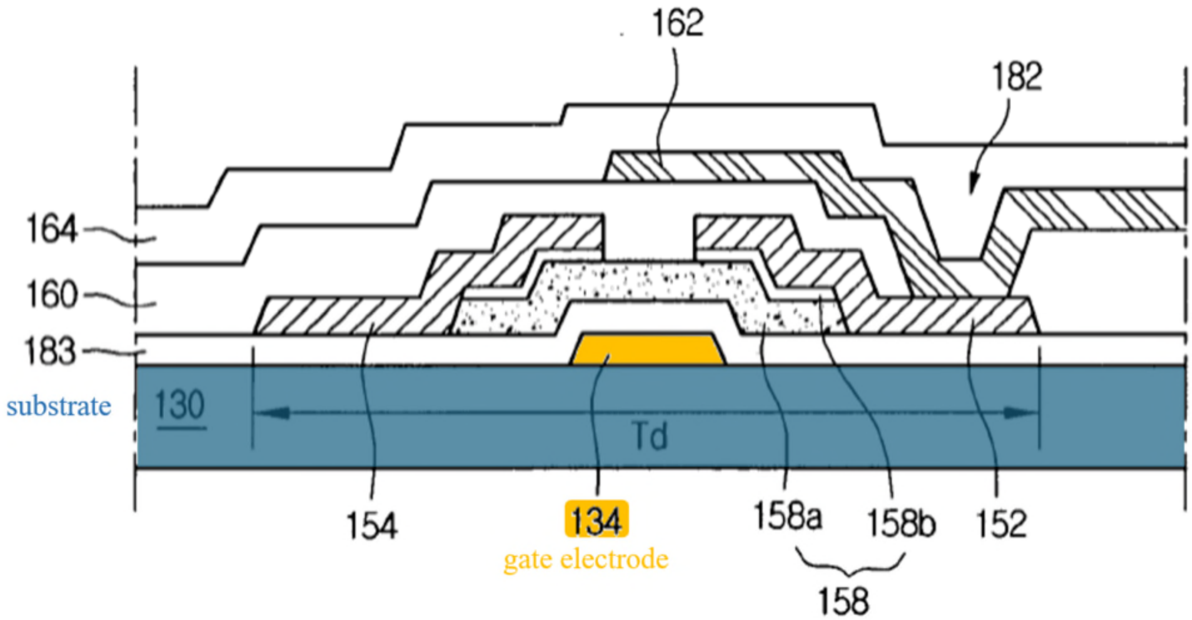
80. Hwang discloses "a semiconductor structure (a transistor, Td, driving an OLED), disposed on a substrate (130), and comprising (see claim1)."



81. EX1004, Fig. 6c (annotated); Figs. 6a-6d, 9; [0019], [0075]-[0095] (describing the manufacturing process for an organic electroluminescence device that includes at least a driving transistor and an OLED).

2. [1a] a gate electrode, disposed on the substrate;

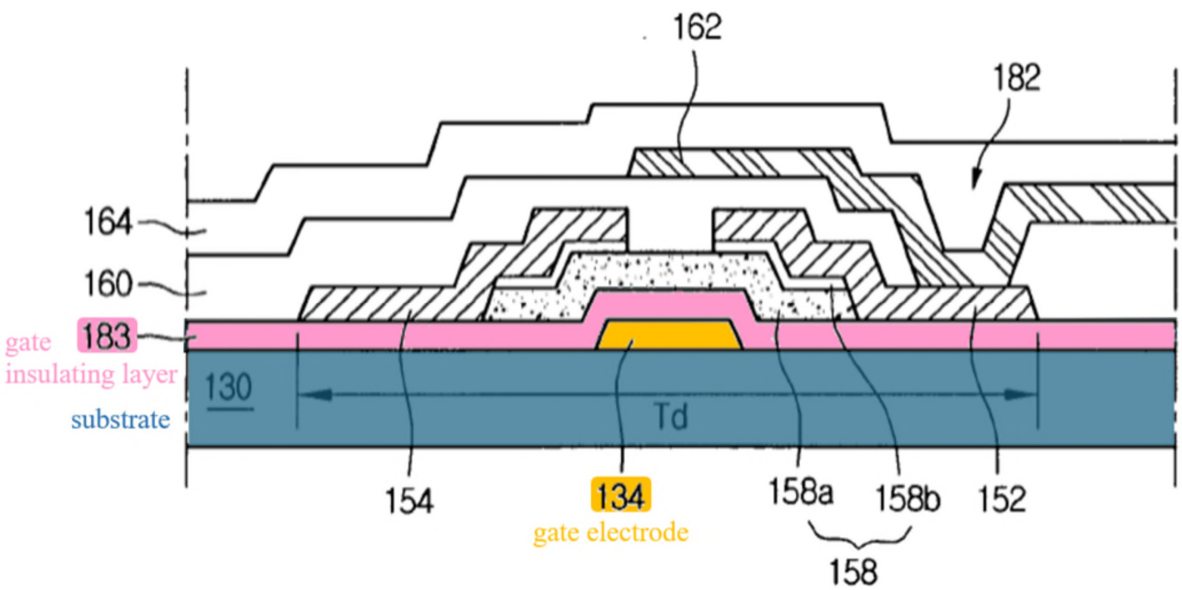
82. Hwang discloses "a gate electrode (134), disposed on the substrate (130)."



83. EX1004, Fig. 6c (gate electrode annotated in orange). Hwang discloses patterning a deposited metal layer on the substrate to form gate electrode 134. EX1004, [0076].

3. [1b] a gate insulating layer, disposed on the substrate, and covering the gate electrode;

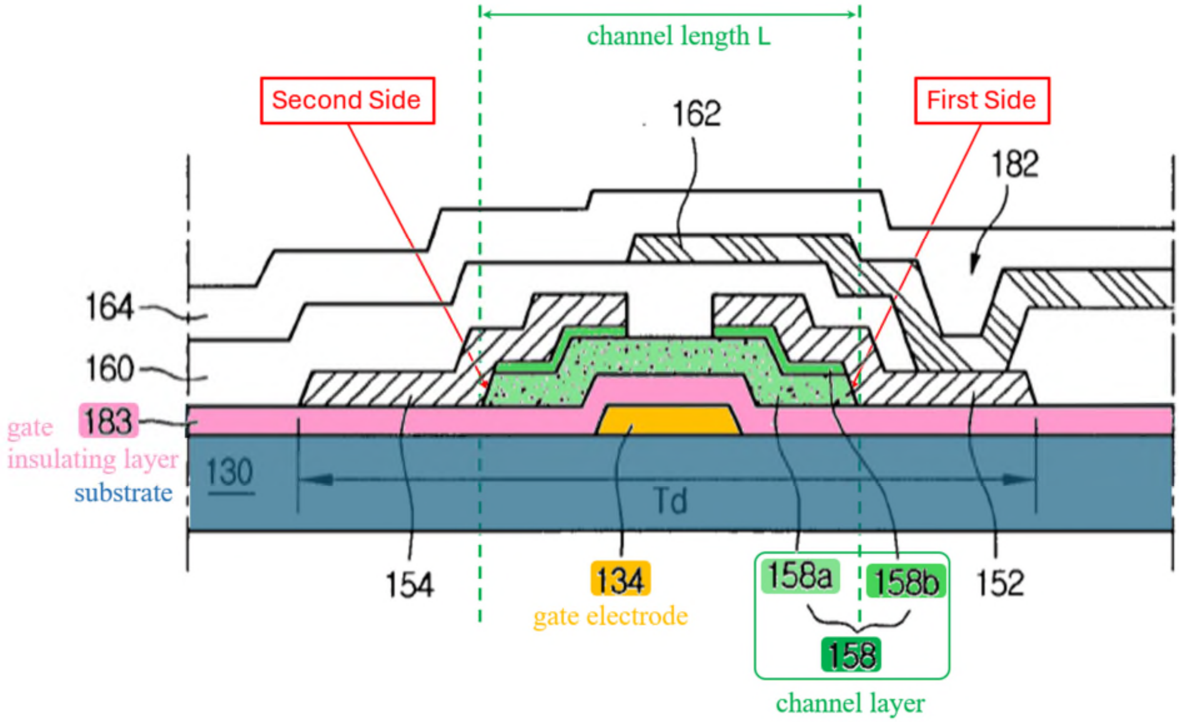
84. Hwang discloses "a gate insulating layer (183), disposed on the substrate (130), and covering the gate electrode (134)."



85. EX1004, Fig. 6c (gate insulating layer annotated in pink). Hwang discloses depositing an insulating material over the entire surface of the substrate (including the previously-formed gate electrode) to form the gate insulating layer. EX1004, [0077].

4. [1c] a channel layer, disposed on the gate insulating layer and located above the gate electrode, wherein the channel layer has a channel length L along a channel direction and has a first side and a second side opposite to the first side;

86. Hwang discloses "a channel layer (158), disposed on the gate insulating layer (183) and located above the gate electrode (134), wherein the channel layer has a channel length L along a channel direction and has a first side and a second side opposite to the first side."



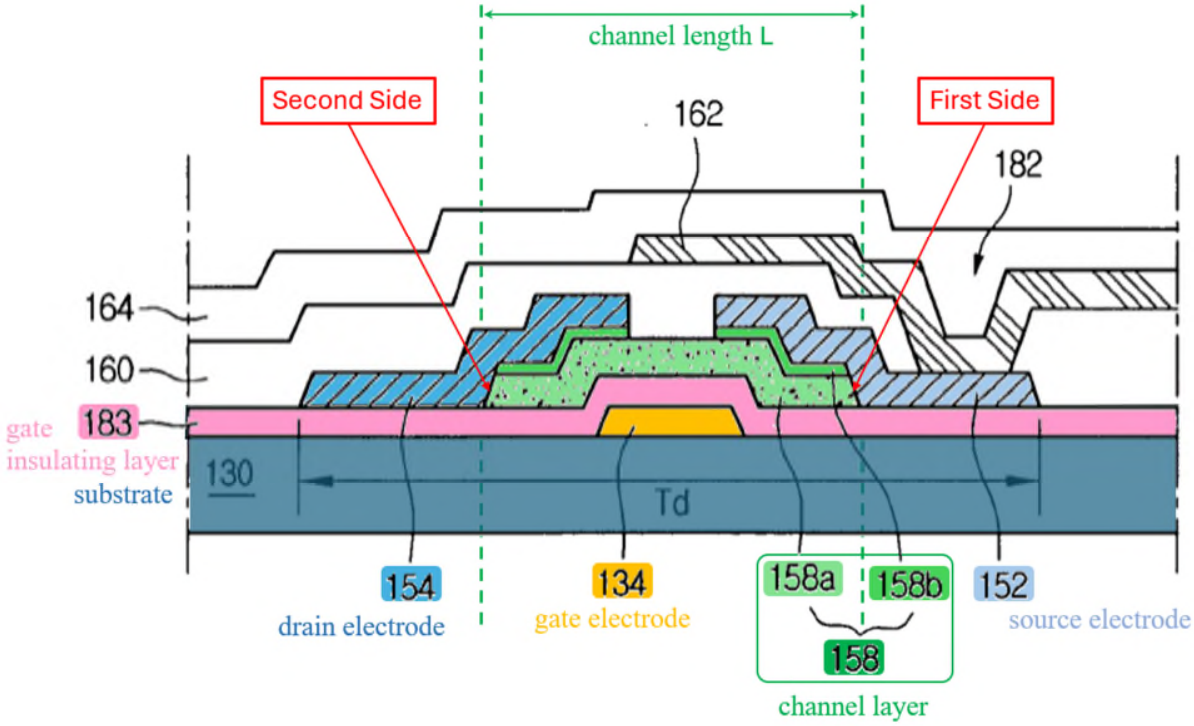
87. EX1004, Fig. 6c (channel layer annotated in green). Hwang discloses patterning amorphous silicon layers deposited on the gate insulating layer to form active layer 158a and ohmic contact layer 158b. EX1004, [0078]. A POSITA would have understood that the claimed "channel layer" to include at least layer 158a that serves as the active semiconductor layer for the drive transistor, with the first and second sides as annotated. Further, the source of the drive transistor is on the right and the drain is on the left (EX1004, [0078]-[0080]), and thus a POSITA would have recognized that the channel layer has a channel length "L" along the channel direction as annotated.

88. A POSITA would have further recognized that ohmic contact layers 158b are semiconductor layers that are part of the drive transistor whose presence

allows the metal-semiconductor junction (source/drain electrode interface to the source/drain region of the transistor) to have linear *I-V* (current-voltage) characteristics. EX1007, 187-189. Therefore, they would be considered part of the claimed channel layer. However, in the Hwang configuration where layers 158a and 158b are vertically stacked, the channel length would be the same regardless of whether the ohmic contact layers are considered part of the claimed channel layer.

5. [1d] a source electrode and a drain electrode, located at the two opposite sides of the channel layer, and electrically connected to the first side and the second side of the channel layer, respectively;

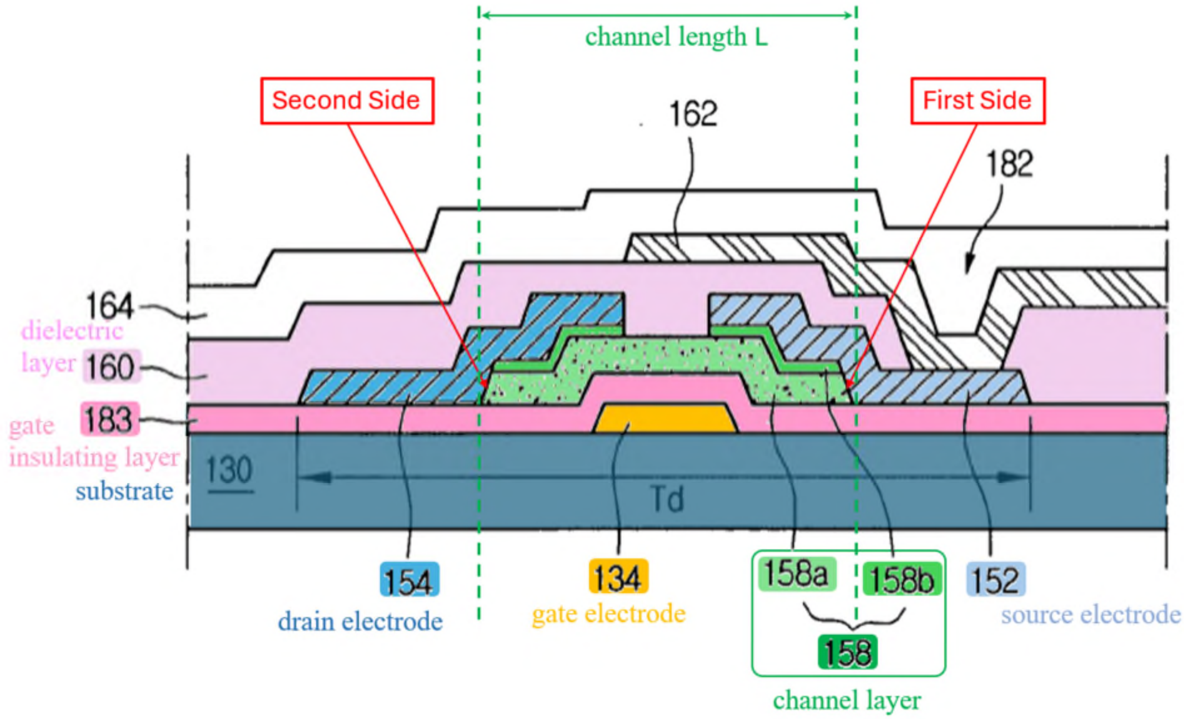
89. Hwang discloses "a source electrode (152) and a drain electrode (154), located at the two opposite sides of the channel layer (158), and electrically connected to the first side and the second side of the channel layer, respectively."



90. EX1004, Fig. 6c (source and drain electrodes annotated in light and dark blue shading). Hwang discloses depositing a metal layer and patterned on the substrate (and in contact with semiconductor layer 158) to form source electrode 152 and drain electrode 154. EX1004, [0079]. The source and drain electrodes are electrically connected to the first and second sides of the channel layer because they are in direct contact with the first and second sides as shown in the annotated figure.

6. [1e] a dielectric layer, covering the source electrode, the drain electrode and the channel layer; and

91. Hwang discloses "a dielectric layer (160), covering the source electrode (152), the drain electrode (154) and the channel layer (158)."

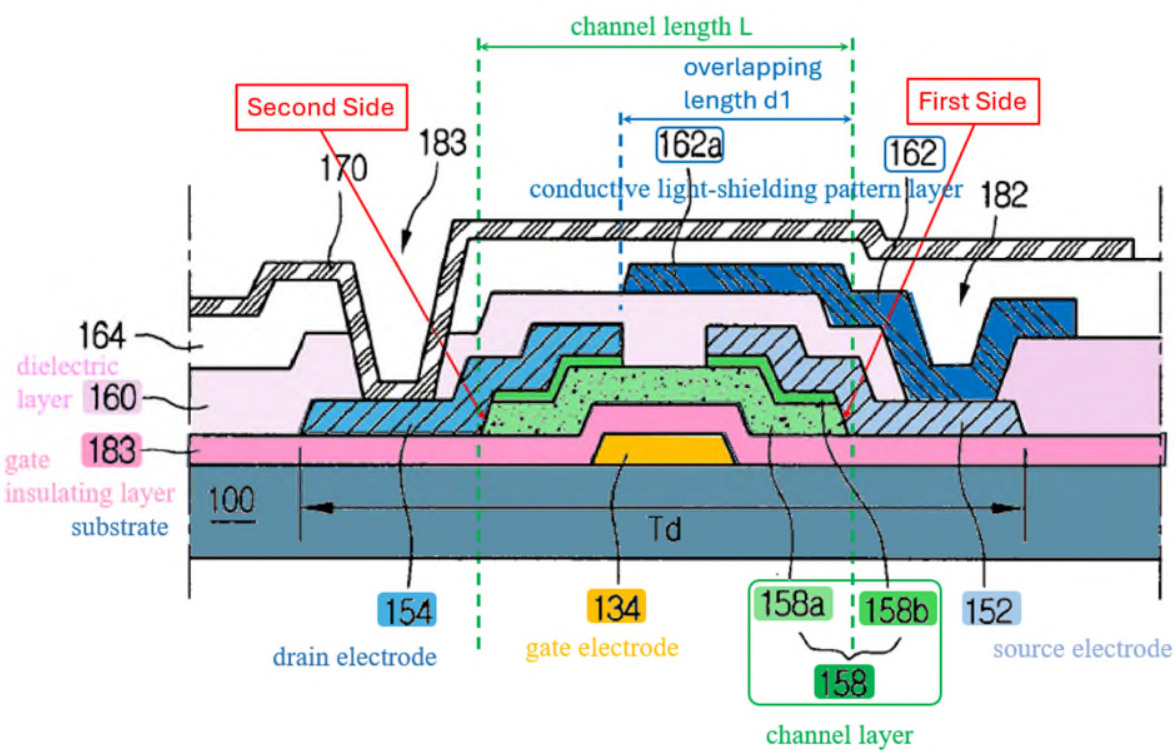


92. EX1004, Fig. 6c (dielectric layer annotated in light pink). Hwang discloses depositing a dielectric material 160 over the entire substrate and thus covers the channel layer and the source and drain electrodes. EX1004, [0081].

93. As explained in Figures 2, 3, 6b, 6c and accompanying text, via's are later made through the dielectric material 160 to allow for electrical connections to upper layers. The "cover" limitation does not preclude such openings. Claim 9 requires an OLED and "a lower electrode, disposed on the dielectric layer and electrically connected to the drain electrode." EX1001, claim 9. The specification explains this claimed connection is through a "contact window." EX1001, 4:34-40. Thus, a POSITA would have understood that "cover" does not preclude such openings.

7. **[1f] a conductive light-shielding pattern layer, disposed on the dielectric layer, and overlapped to a portion of the source electrode and a portion of the channel layer in a vertical projection, wherein the conductive light-shielding pattern layer does not overlap to the drain in the vertical projection, and the conductive light-shielding pattern layer and the channel layer have an overlapping length d1, and 0.3≦d1/L≦0.85.**

94. Hwang discloses "a conductive light-shielding pattern layer (162/162a), disposed on the dielectric layer (160), and overlapped to a portion of the source electrode (152)and a portion of the channel layer (158) in a vertical projection, wherein the conductive light-shielding pattern layer does not overlap to the drain in the vertical projection, and the conductive light-shielding pattern layer and the channel layer have an overlapping length d1, and 0.3≦d1/L≦0.85."



95. EX1004, Fig. 6d (conductive light-shielding pattern layer annotated in dark blue). Hwang discloses patterning a deposited metal layer on dielectric layer 160 to form ground line 162 that also includes an extended portion 162a (“auxiliary electrode) over part of and shields the drive transistor. EX1004, [0083]-[0087]. As shown in the annotated figure above, the length of the overlap between layer 162/162a and the channel layer in a vertical projection (*i.e.*, a direction perpendicular to the plane of the substrate) is annotated as d1 where layer 162/162a does not overlap the drain electrode 154. EX1004, [0048] and [0050] (disclosing auxiliary electrode 162a does not overlap the drain electrode 154). Further, Hwang expressly discloses aluminum, aluminum alloy, tungsten, copper, molybdenum and titanium as exemplary metals suitable for layer 162/162a (ground line and auxiliary electrode). EX1004, [0101], claim 13.

a. Material properties of layer 162/162a are electrically conductive and light-shielding (optically opaque)

96. As discussed in the Claim Construction Section on “a conductive light-shielding pattern layer”, the 471 patent discloses “metal” as the broad class of materials suitable for the conductive light-shielding pattern layer. EX1001, 3:58-61, 4:40-5:9. A POSITA would have readily recognized that the exemplary metals and metal alloys disclosed by Hwang have high electrical conductivity because they are well-known metal materials used for interconnects in semiconductor devices. This recognition is further reinforced by the fact that layer 162 serves as

the electrical ground line, and thus would be fabricated with a material that is a good electrical conductor.

97. While Hwang does not explicitly teach that layer 162/162a serves the intended purpose of light-shielding, a POSITA would have understood that the layer formed using any one of these exemplary metals would have light-shielding properties for multiple reasons. First, a POSITA would have recognized that these exemplary metals are good reflectors of light. Therefore, most of the light incident on these metal materials are reflected rather than transmitted through the material. *See e.g.,* Paper 39 (Final Written Decision) *Home Depot USA, Inc. v. Lynk Labs, Inc.* IPR2021-01541, at 32 (holding "Aluminum, for example, indisputably reflects light."). Light incident on these exemplary metallic surfaces would instead be reflected back, as is well known to those of skill in the art.

98. Second, with respect to any light that is not reflected back (which will be a small fraction of the incident light), most of it will be absorbed by these metal materials well before it can travel through the thickness of the material. EX1008, 35.6. A POSITA would have recognized that the absorption rate of light (*i.e.*, an electromagnetic field) as it propagates within a metal material is characterized by its "skin depth," a parameter indicating the distance where the light intensity has attenuated by about 86.5% due to absorption in the material. EX1008, 35.3-35.7. In other words, after accounting for incident light being reflected at the surface, less

than 14% of the light intensity will penetrate past the skin depth, with the light intensity continuing to decrease the further the distance it propagates into the material.

99. The skin depth parameter δ is given by the formula $\delta = \sqrt{\frac{2}{\omega\mu\sigma}}$, where ω is the frequency of the electromagnetic wave, μ is the magnetic susceptibility of the material, and σ is the electrical conductivity. EX1008, 35.6 (equation 11). This equation shows that the skin depth (or the penetration depth) of an electric field through a material depends inversely on its frequency and on the conductivity of the material, meaning the skin depth will decrease as frequency increases or as conductivity increases. As is well known, metals have high electrical conductivity (as discussed above), and light oscillates at very high frequencies (light in the visible spectrum is in the Terahertz range, where 1 Terahertz (THz) is 10^{12} oscillations per second). Therefore, both factors contribute to a very small penetration depth for light incident on a metal. Indeed, at optical frequencies, the skin depth of most metals is only approximately 50 nanometers (where one nanometer is one billionth of a meter). EX1008, 35.6.

100. The skin depth equation also shows that as the frequency of the electric field decreases, the skin depth parameter increases, meaning the electric field can penetrate deeper into the metal. Thus, to effectively limit the penetration of a lower frequency electromagnetic wave (*e.g.* microwave radiation that

oscillates at $10^6 – 10^9$ Hz) using the same material, a thicker layer of that material is required (when compared to a higher frequency electromagnetic wave such as light in the optical spectrum). This is relevant because in Hwang's embodiment of Fig. 6d (shown above), Hwang expressly teaches that auxiliary electrode 162a must shield the channel region of the TFT from the influence of the time-varying electric field caused by electrode 170 when the OLED is driven at different electrical currents to produce different levels of brightness. EX1004, [0014]-[0020], [0050], [0065]-[0068], [0072], [0101]. The frequency bandwidth of these electrical drive signals would be well below optical frequency range, reaching at most the microwave frequency range. As expressly taught by Hwang, auxiliary electrode 162a in Fig. 6d must be sufficiently thick in order to be effective at shielding these relatively low frequency electric fields propagating from electrode 170 when driving the OLED. Because light oscillates at a higher frequency, it will not penetrate Hwang's auxiliary electrode 162a as deeply as the lower frequency electric field induced by the OLED drive signal. Thus, a POSITA would understand that because Hwang's auxiliary electrode 162a is effective at shielding low frequency electric fields from electrode 170 (as expressly disclosed by Hwang), it must necessarily be effective at "shielding" light also. Accordingly, Hwang's patterned layer 162/162a qualifies as a conductive light-shielding pattern layer, at least because most if not all of the incident light is either reflected back or absorbed by the metal material.

101. Third, it is expressly known in the art that metals such as aluminum, aluminum alloy, tungsten, copper, molybdenum and titanium are conductive materials with light-shielding (or light blocking) properties suitable for shielding a semiconductor from light. EX1005, [0006] and [0012] (explaining the use of a gate electrode to shield a semiconductor layer in a TFT from light), [0045] (disclosing the use of metal materials including aluminum, tungsten, copper, molybdenum, titanium and their alloys for the gate electrode); EX1006, [0046] (use of metal wiring layer to shield a TFT from light), [0096] (disclosing the use of aluminum and molybdenum for the light-shielding pattern); EX1012, 7 (disclosing the use of aluminum and molybdenum for the light-shielding pattern); EX1015, 12:35-44 (disclosing that an aluminum film has high light shielding properties).

102. Lastly, to the extent there is any doubt that Hwang's auxiliary electrode 162a is indeed light-shielding, it would have been obvious, and a POSITA would have been motivated to configure electrode 162a to be light-shielding as set forth in Ground 3 below.

b. Ratio d1/L is between 0.3 and 0.85

103. As discussed for [1c] *supra*, Hwang's semiconductor layer 158 has length L in the channel direction. Layer 158 comprises the source, channel and

drain regions of the drive transistor Td (in the form of a TFT) for the OLED device. EX1004, [0075]-[0080]. As depicted in Fig. 6a-6d, the source, channel and drain regions of Hwang's transistor Td is symmetric with respect to the center of the channel region such that the length[4] of the source and drain regions is the same. Further, Hwang depicts drive transistor Td has a channel region (*i.e.*, the part of layer 158 not covered by ohmic contacts 158b, EX1004 [0080]) whose length is no greater than that of the source or the drain regions.

104. Thus, a POSITA would review the disclosure in Hwang and at once envisage a commonly-used TFT configuration in which (a) the source and drain regions are equal in length, and (b) where the length of the channel region is no greater than that of the source (or drain) region. At a minimum, Hwang's disclosure would have rendered obvious such a TFT configuration. A POSITA would have recognized this as a common TFT configuration for OLED drive transistors because a shorter channel region length typically allows higher current and faster switching speeds, whereas lithography limits and the necessity for forming highly conductive source/drain contacts typically result in source/drain regions that are similarly sized but larger than the channel region (*i.e.*, condition (b)). Once the source/drain regions are large enough to accommodate electrical

[4] Unless other specified, the term "length" with respect to the source, channel and drain regions as used herein refers to the length in the channel direction.

connection to highly conductive contacts, TFT drive transistor designs would not further increase those dimensions unnecessarily. This is because a general design goal would be to increase pixel density in an OLED display panel (thus leaving the source and drain regions equally sized, *i.e.*, condition (a)). Thus, a POSITA would have recognized the figures in Hwang to at least render obvious (if not outright depict) a well-known and common TFT drive transistor configuration having relative proportional dimensions as set forth above.

105. Based on these two conditions for this common (or at least obvious) TFT configuration, a POSITA can ascertain the range for the length of the drain region as a fraction of the total length L. For fixed L, the drain region length reaches a value of approximately 0.33L where the source, channel and drain regions are of equal lengths. A POSITA would have recognized that transistor performance generally improves (*e.g.*, higher speed and greater power efficiency) when the length of the channel region is reduced. EX1013, 33-37. This performance improvement is the basis for the drive towards miniaturization of semiconductor devices, manifesting itself as the well-known Moore's Law. Accordingly, a POSITA would have recognized that common transistor designs may have a channel region length that is less than the length of the source/drain regions due to the advantages of a decreased channel region length. EX1013, 33-37. Since the drain region length is equal to 0.33L (when the source, drain and

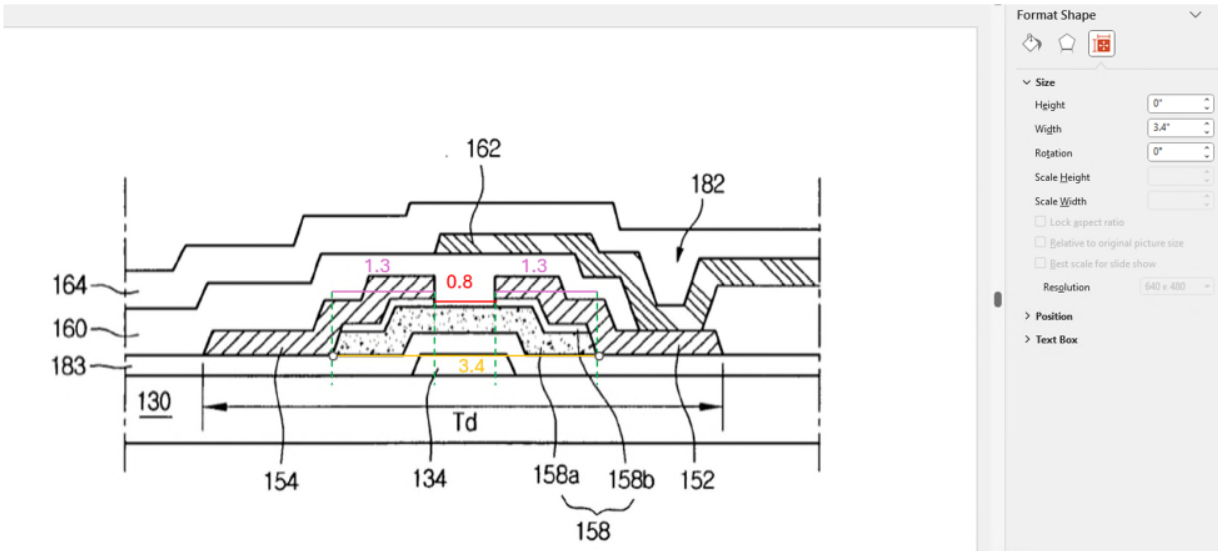
channel regions are equal lengths), decreasing the length of the channel region relative to the source/drain region would lead to a corresponding increase in the source/drain region length such that it is greater than 0.33L. Therefore, a POSITA would have recognized that for many common transistor configurations, 0.33L would be a typical lower bound for the drain channel length. Of course, a POSITA would also have recognized that the channel region length cannot be reduced too much because of fabrication tolerances and also because of the well-known short channel effect. EX1007, 298-299, 325-327. However, even if we consider an extreme hypothetical design where the channel region length is negligibly small relative to the equally-sized source and drain regions (such that each of these regions make up 50% of the semiconductor layer 158), the drain region length would still reach a maximum value of no greater than 0.5L. Thus, the relative size of the drain region is bounded between 0.33L and 0.5L. Since the source region is the same size as the drain region, its length is likewise bounded between 0.33L and 0.5L. The length of the channel region would make up the difference (*i.e.*, L - length of source - length of drain), thus ranging between approximately 0L (in the extreme hypothetical case) to 0.33L.

106. Hwang discloses the conductive light-shielding pattern layer 162/162a to overlap both the source and channel regions, but not the drain region. Therefore, the overlapping length d1 is (L – length of drain) which is between 0.5L and

0.67L. Accordingly, a POSITA would have recognized that any TFT drive transistor Td so configured would result in a d1/L ratio to fall between 0.5 to 0.67, the entirety of which falls within the claimed range of 0.3 to 0.85.

107. Alternatively, it would have been obvious to a POSITA to take the figures in Hwang at face value and glean therefrom relative dimensions for the length of the source, drain and channel regions of driving transistor Td to be approximately 0.38L, 0.38L and 0.24L respectively.

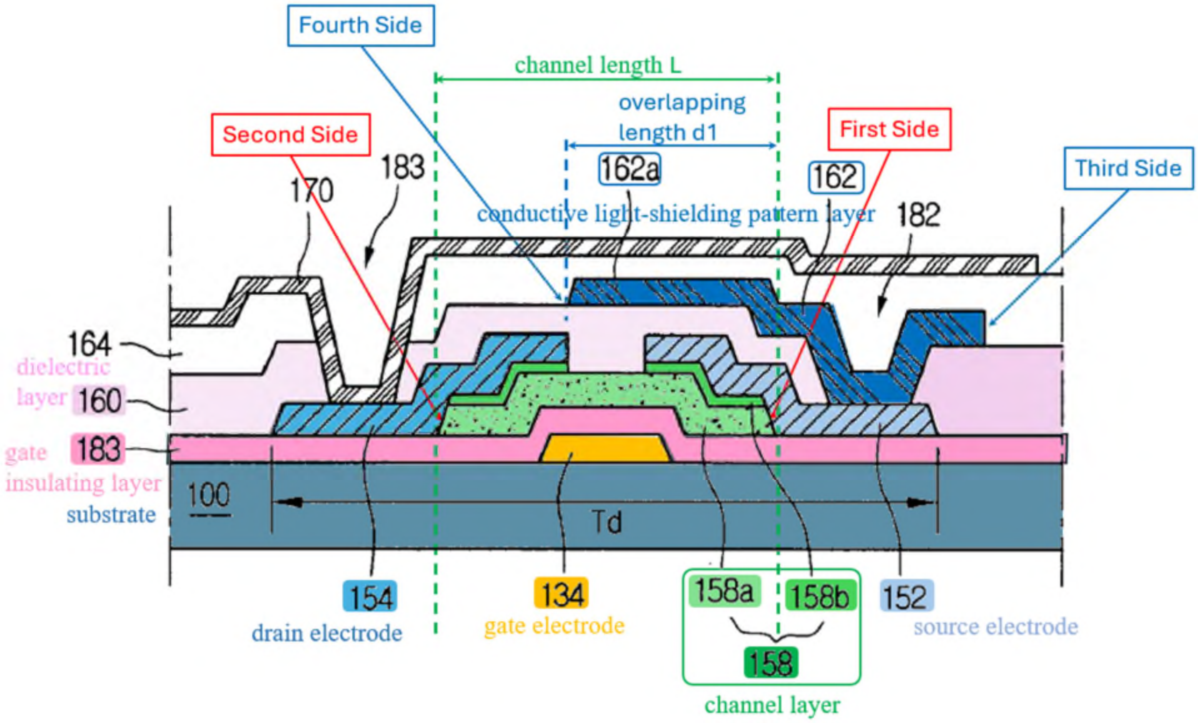
108. I estimated these relative proportions for the transistor dimensions by comparing a copy of Hwang's Fig. 6c overlaid with lines drawn within PowerPoint that overlap with Hwang's source, drain and channel regions to determine the relative dimensions of the three regions. An exemplary screenshot showing the estimate for the length of the channel layer dimension is shown below (with the gold line selected and viewing the "Size" parameters in the "Format Shape" feature in PowerPoint).



109. A POSITA applying the teachings of Hwang regarding layer 162/162a to not overlap with the drain region of driving transistor Td would arrive at a conductive light-shielding pattern layer having a d1/L value of 0.62L, which falls well within the claimed range of 0.3 to 0.85.

D. Claim 4. The semiconductor structure as claimed in claim 1, wherein the conductive light-shielding pattern layer has a third side and a fourth side along the channel direction, the fourth side is overlapped to the channel layer in the vertical projection, wherein the overlapping length d1 is equal to a distance between the fourth side and the first side of the channel layer along the channel direction.

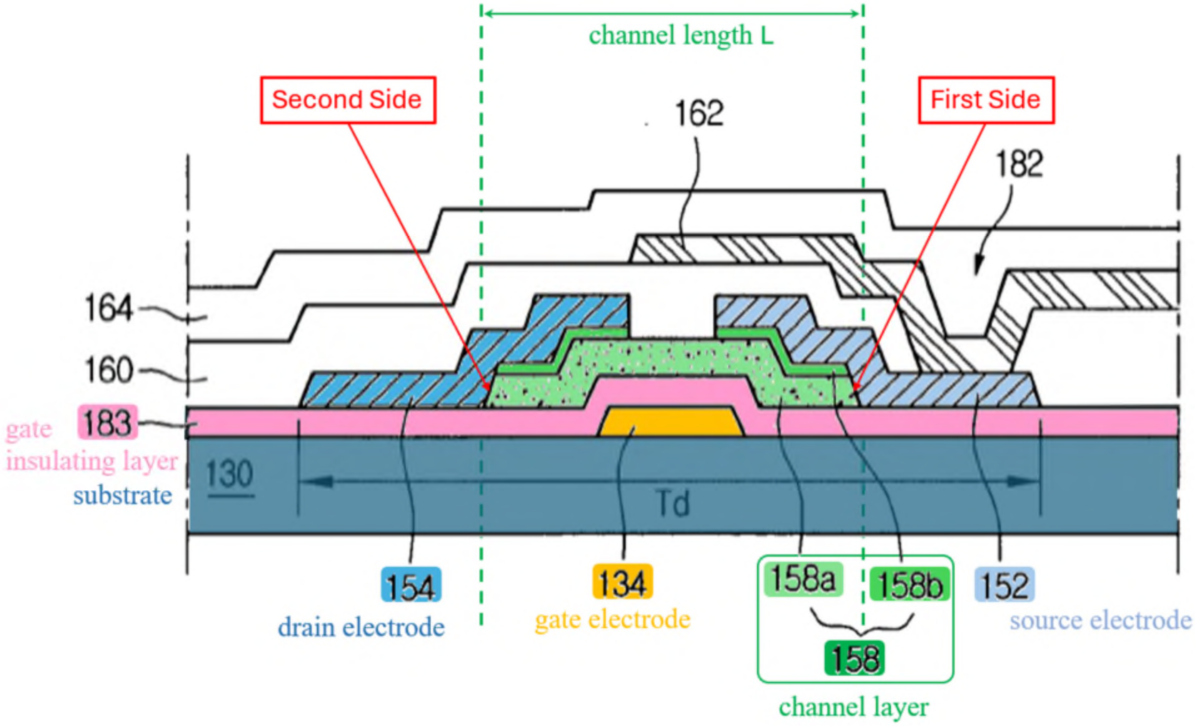
110. Hwang discloses "the conductive light-shielding pattern layer (162/162a) has a third side and a fourth side along the channel direction, the fourth side is overlapped to the channel layer in the vertical projection, wherein the overlapping length d1 is equal to a distance between the fourth side and the first side of the channel layer along the channel direction."



111. EX1004, Fig. 6d (annotations added identifying length d1 between fourth side of layer 162/162a and the first side of channel layer 158).

E. Claim 6. The semiconductor structure as claimed in claim 1, wherein the source electrode and the drain electrode respectively cover a portion of the channel layer.

112. Hwang discloses "the source electrode (152) and the drain electrode (154) respectively cover a portion of the channel layer (158)."



113. EX1004, Fig. 6c annotated showing the source and drain electrodes cover a portion of the channel layer.

F. Claim 9

1. [9pre] An organic electroluminescence device, disposed on a substrate, and comprising.

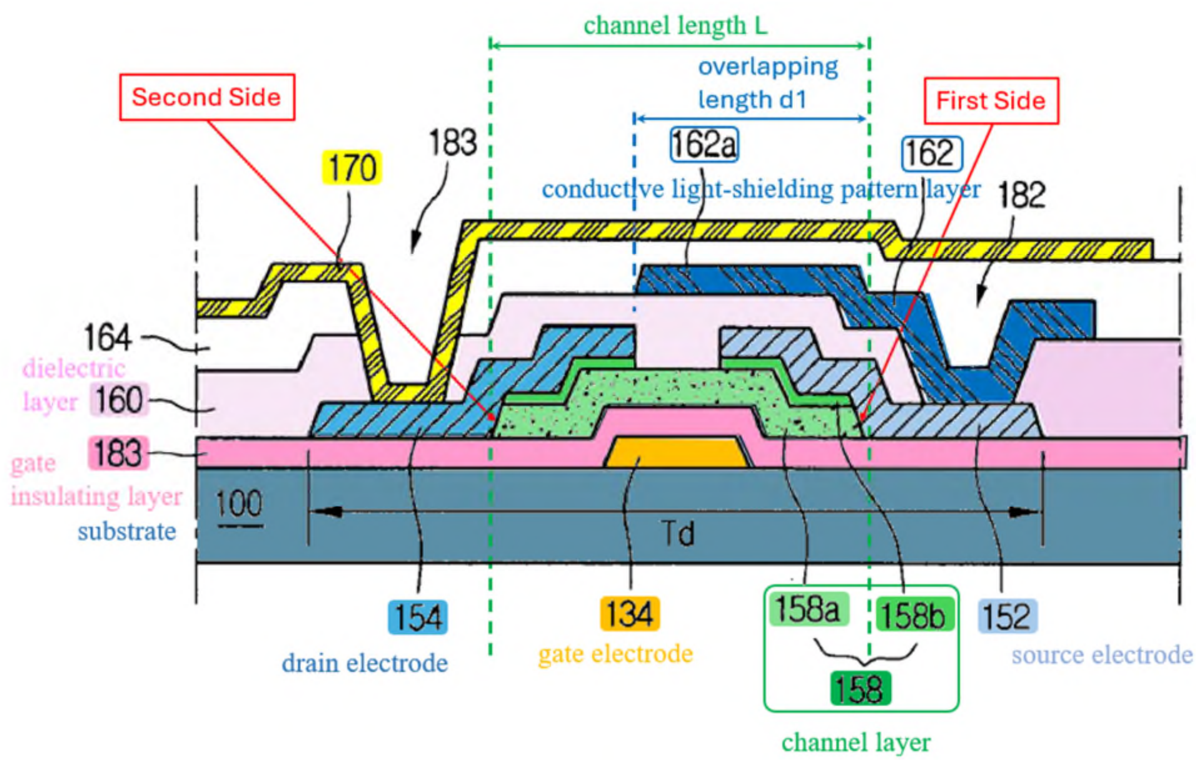
114. *See* [1pre], [9a]-[9i] (including drive transistor and organic light emitting layer of the OLED that are part of the organic electroluminescence device).

2. [9a]-[9f];

115. *See* [1a]-[1f].

3. [9g] a lower electrode, disposed on the dielectric layer and electrically connected to the drain electrode;

116. Hwang discloses "a lower electrode (170), disposed on the dielectric layer (160) and electrically connected to the drain electrode (154)."

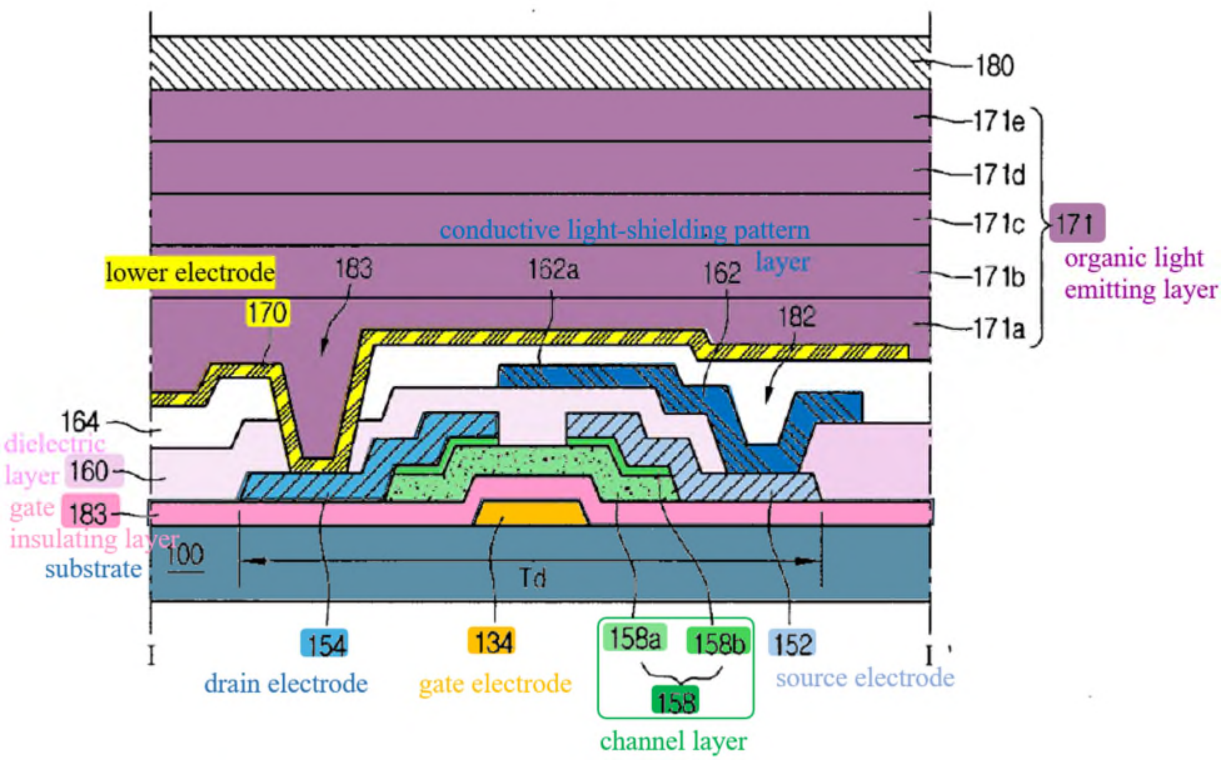


117. EX1004, Fig. 6d (lower electrode 170 annotated in yellow shading, disposed on dielectric layer 160 and in contact with drain electrode 154). A POSITA would have recognized that electrode 170 is disposed on dielectric layer 160 because of the sloped openings formed within layer 160 to allow electrode 170 to make direct contact with the drain electrode 154. Thus, within at least that sloped opening, electrode 170 is directly disposed on the sidewalls of layer 160. Further, a POSITA would have recognized that electrode 170 is indirectly disposed

on layer 160 in other areas, since it is formed above layer 160, albeit with intervening layers therebetween, such as layer 164. Hwang discloses that lower electrode 170 serves as the cathode for the OLED device. EX1004, [0089]-[0095].

4. [9h] an organic light emitting layer, disposed on the lower electrode; and

118. Hwang discloses "an organic light emitting layer (171), disposed on the lower electrode (170)."

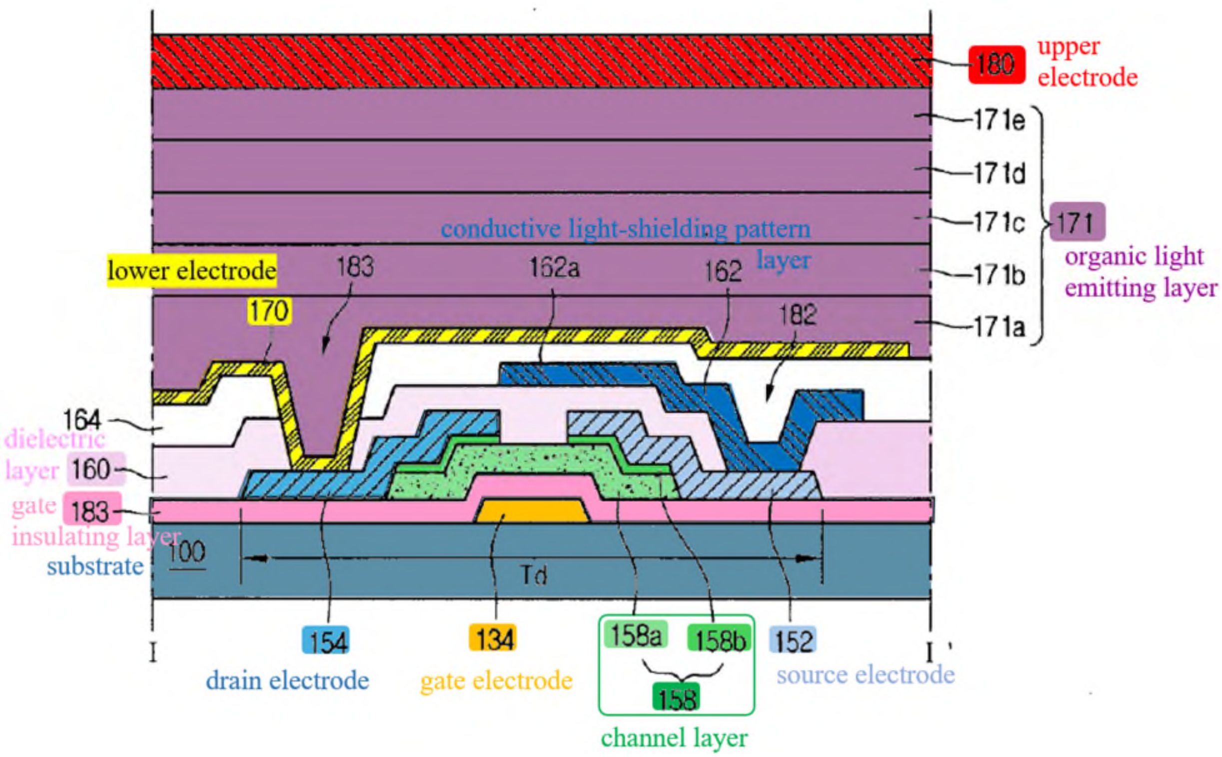


119. EX1004, Fig. 3 (annotated). The first embodiment in Hwang (Figures 1-6 and accompanying text) discloses that the embodiment depicted therein includes an organic light emitting layer (171) formed on the first electrode 170. EX1004, Fig. 3 (showing 171 disposed on 170), [0053]-[0054] ("An organic light

emitting layer 171 … are formed on the first electrode 170."), [0093]-[0095] (light emitting layer 171 may be a single layer or multiple layers).

5. [9i] an upper electrode, disposed on the organic light emitting layer.

120. Hwang discloses "an upper electrode (180), disposed on the organic light emitting layer (171)."



121. EX1004, Fig. 3 (annotations added). The first embodiment in Hwang (Figures 1-6 and accompanying text) discloses that the embodiment depicted therein includes an organic light emitting layer (171) formed on the first electrode 170. EX1004, Fig. 3 (showing 180 disposed on 171), [0053]-[0057] ("An organic light emitting layer 171 and a second electrode 180 are formed on the first

electrode 170."), [0061], [0093]-[0094] ("The second electrode serves as an anode"), [0095] (light emitting layer may be a single layer or multiple layers).

G. Claim 12.

122. *See* claim 9, claim 4.

H. Claim 14.

123. *See* claim 9, claim 6.

I. 17. The semiconductor structure as claimed in claim 1, wherein the conductive light-shielding pattern layer and the drain electrode are spaced by a distance along the channel direction in the vertical projection.

124. Hwang renders obvious "the semiconductor structure as claimed in claim 1 (*see* claim 1), wherein the conductive light-shielding pattern layer (162/162a), and the drain electrode (154) are spaced by a distance along the channel direction in the vertical projection."

125. Hwang teaches layer 162/162a should cover the channel region but not overlap the drain electrode 154. EX1004, [0048]. As illustrated in Figure 6d, Hwang teaches that in the vertical projection, there may be very little space between the end of the drain electrode 154 and electrode 162a. EX1004, Fig. 6d. To the extent Figure 6d does not expressly disclose electrode 162a and drain electrode 154 are "spaced by a distance in the vertical projection," Hwang also teaches that, while electrode 162a covers the channel region to block the influence of electrode 170, it could be shortened, depending on need. EX1004, [0050]

("auxiliary electrode 162a. . . does not overlap the second drain electrode 154. The auxiliary electrode 162a may be … shorter… upon need."). One exemplary need disclosed by Hwang is to prevent short circuit between the auxiliary electrode 162a and the drain electrode 154. EX1004, [0050]. Thus, Hwang teaches that electrode 162a (which still should cover the channel region to block the influence of electrode 170) can be shortened (*i.e.*, spacing apart in the vertical projection) by a small amount to account for fabrication variances in order to mitigate a potential short circuit to the drain electrode. Because this claim does not require a particular minimum amount of distance for the "spaced apart" limitation, Hwang's wholistic teaching that electrode 162a covers the channel, does not overlap the second drain electrode and can, in fact, be even shorter expressly discloses this claim to a POSITA.

126. Additionally or alternatively, claim 17 is obvious in view of Hwang. A POSITA would have understood that Hwang's teaching in paragraph [0050] related to shortening electrode 162a would not expose the entire channel region entirely, but only to shorten electrode 162a to the extent needed. This is because the disclosed function of the auxiliary electrode 162a is to shield the channel region from the electric potential at the cathode 170. Indeed, this shielding of the channel region from the cathode voltage specifically solves the problem that Hwang's invention sought to overcome. EX1004, [0016]. Specifically, shielding

the channel region overcomes the problems of brightness deterioration and non-uniformity. EX1004, [0072]; *see also id.*, [0069]-[0074] and Fig. 5. Therefore, a POSITA would have understood that shielding the channel region remains important, even though there may be other design tradeoffs that need to be considered.

127. For example, as disclosed in Hwang, increasing the spacing would help prevent an unintentional short circuit between auxiliary electrode 162a (which is electrically connected to and thus on the same node as the source electrode) and the drain electrode 154. EX1004, [0050], [0066]. Additionally or alternatively, a POSITA would have recognized that unintended parasitic capacitance between the source and drain has an adverse impact on the transistor performance. EX1007, 323. Thus, a POSITA would have been motivated to mitigate unintended capacitive coupling to the drain electrode 154 by increasing the spacing (in the vertical projection) between electrode 162a and drain electrode 154 for a given dielectric material 160 to increase the distance therebetween, thereby reducing the resulting capacitance. EX1014, 153-154.

128. A POSITA would have recognized that even though electrode 170 is electrically connected to drain electrode 154, capacitive coupling between electrode 162a and electrode 170 can be mitigated by increasing the properties (*e.g.*, thickness and/or dielectric constant) of dielectric layer 164. However, this

does not fully resolve the potential capacitive coupling to the drain electrode, thus potentially requiring additional spacing between electrode 162a and drain electrode 154 (as expressly taught by Hwang). Thus, the extent of the overlap of electrode 162a with the channel region requires a tradeoff between mitigating unintentional short circuits and/or the capacitive coupling to the drain, and shielding the effects of the cathode on the channel region. Any decrease in the overlap length would necessarily cause electrode 162a and drain electrode 154 to be spaced by a distance along the channel direction in the vertical projection.

129. As for quantifying the decrease in electrode 162a, a POSITA would have recognized from the teachings of Hwang that the primary emphasis remains to provide as much shielding to the channel region as possible in order to reap the benefits of the Hwang invention. EX1004, [0069]-[0074]; Fig. 5. Therefore, this would have suggested to a POSITA that at least half of the channel region should remain shielded (if not more) in balancing these other considerations while still preserving the main teachings in Hwang for improving performance by shielding the channel region. This results in a minimum d1/L ratio of 0.5 with no change to the maximum d1/L ratio (0.67), which remains within the range claimed in [1f].

J. 18. The organic electroluminescence device as claimed in claim 9, wherein the conductive light-shielding pattern layer and the drain electrode are spaced by a distance along the channel direction in the vertical projection.

130. *See* claim 9, claim 17.

X. GROUND 2: HWANG AND GODO

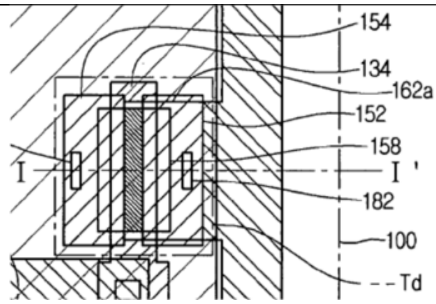
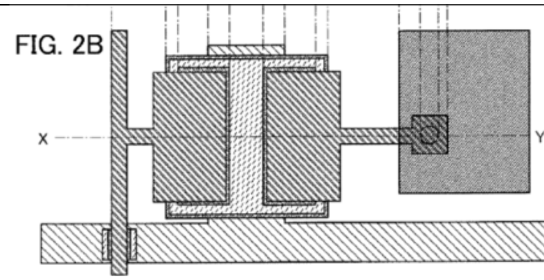
A. Relationship to Ground 1

131. Hwang renders obvious the claims as set forth above for Ground 1 which is incorporated herein by reference.

132. In the alternative, to the extent the claimed relative dimensions of the source, channel and drain regions of a TFT are not taught or rendered obvious to a POSITA by Hwang alone such that the resulting device would meet the claimed d1/L ratio (as set forth in [1f] and [9f]), those dimensions would have been rendered obvious over the combination of Hwang and Godo. As discussed below, Godo discloses specific dimensions for bottom gate TFTs. EX1005, [0199], [0201], Figs. 1A, 1B, 2A, 2B, 4A, 4B, 20A and 20B.

B. The Combination

133. Hwang broadly discloses an arrangement of semiconductor materials to form a TFT, and metallic materials for shielding the channel region in the transistor in an organic luminescent device. The combination of Hwang and Godo modifies Hwang's general teachings for a broad genus of TFTs with Godo's disclosure of more particular species of TFTs (with specific dimensions for the source, channel and drain regions for the transistor) according to known methods to yield predictable results. Compare, e.g., EX1004, Fig. 2 (top-down view of drive transistor Td) and EX1005, Fig. 2B; (*see also* Figs. 4B and 20B).

 EX1004, Fig. 2 (Excerpt)	 EX1005, Fig. 2B

As discussed in Ground 1, [1f], suitable dimensions for such transistors would have been well known in the art, and a POSITA would have immediately recognized Hwang's Figures 6a-6d to at least disclose a broad class of TFTs with at least known ranges of relative proportions for the dimensions of the source, channel and drain regions of the transistor. Nevertheless, to the extent a POSITA, upon reviewing Hwang's disclosure, would have remained unaware of suitable dimensions for the drive transistor, the POSITA would have been motivated to investigate known suitable dimensions in the art for transistors suitable for driving an LED device and been led to Godo's disclosures of appropriate dimensions. EX1005, [0150], [0161], [0163] (disclosing TFT 420 is a drive transistor), [0165] (disclosing TFT 420 drives LED element 430), [0199], [0201]; Figs. 1A-2B, 4A, 4B, 18A, 18B, 20A (with one set of dimensions) and 20B (another set of dimensions).

134. A POSITA would have recognized that Godo's Fig. 4B TFT design shares the most similarities with Hwang's Fig. 6 TFT design: a single amorphous Si channel layer and a bottom gate electrode whose length in the channel direction is less than the length of the amorphous Si layer. Therefore, it would have been obvious to a POSITA to use Godo's Fig. 4B dimensions, at least as a starting point, and potentially consider using Godo's other disclosed dimensions as well. As will be demonstrated below, the resulting d1/L ratios for each of Godo's disclosed TFTs meet the claimed range for limitations [1f] and [9f]. Therefore, regardless of which set of TFT dimensions a POSITA uses from Godo to modify Hwang, limitations [1f] and [9f] are still rendered obvious.

135. A POSITA would have had a reasonable expectation of success in making the proposed combination because techniques such as photolithography for defining patterns for forming transistor elements with the disclosed dimensions were well known in the art. Patterning feature sizes that are in the micron (μm) resolution were well within the ordinary state of the art. Further, the relevant transistors disclosed in both Hwang and Godo are both bottom gate TFTs. EX1004, Figs. 6a-6d; EX1005, Figs. 1A-2B, 4A-B. Thus, the only "modification" of Hwang is to supplement Hwang with the specific geometric dimensions taught in Godo to form Hwang's lithography masks, then perform the same standard and routine TFT fabrication steps to thereby form a transistor with the dimensions as

disclosed in Godo. The proposed combination would not have required undue experimentation and would have yielded the predictable result, namely, a drive transistor with the dimensions as disclosed in Godo. Once the drive TFT is formed, Hwang's layer 162/162a with the shielding auxiliary electrode can be formed thereafter as taught by Hwang.

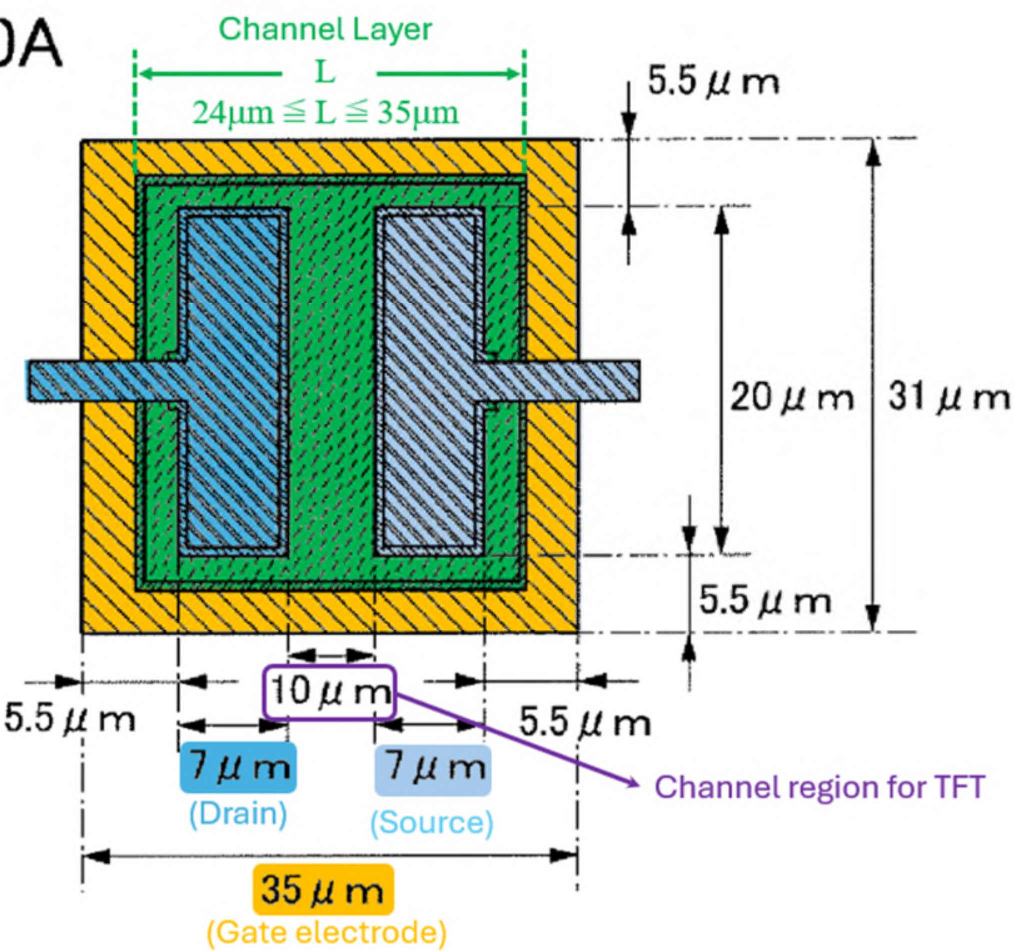
C. "… an overlapping length d1, and 0.3≦d1/L≦0.85" ([1f], [9f])

136. Godo discloses the dimensions for the source, channel, and drain regions for TFTs suitable for driving an LED device. EX1005, Figs. 20A, 20B; *see also id.*, [0150], [0161], [0199], [0201] (explaining the dimensions shown for Figs, 20A and 20B apply to the transistors of Figs. 1A-2B, 4A and 4B); Figs. 1A-2B, 4A, 4B, 18A, 18B. To the extent a POSITA, having reviewed Hwang's disclosure, required additional express guidance on suitable TFT dimensions, the POSITA would have been motivated to seek out those teachings in the art and it would have been obvious to use the TFT dimensions disclosed in Godo as explained above. As will be shown below, forming a drive transistor Td (using either Godo's Fig. 20A or Fig. 20B dimensions), and thereafter forming layer 162/162a that shields the source and channel regions of drive transistor Td would result in 0.3≦d1/L≦0.85 as required by this limitation.

1. Godo's Fig. 20A dimensions render obvious claimed d1/L ratio

137. The TFT shown in Godo's Fig. 20A has a channel direction that runs left/right, and the length of source and drain regions along the channel direction are 7µm. The length of the channel region is 10µm.

FIG. 20A



EX1005, Fig. 20A (annotations added). The length of the channel layer ("L" as claimed in [1c] and [9c]) is not expressly disclosed, but a POSITA would have understood that the disclosed dimensions necessarily bound the range of L. In particular, L must be less than 35µm (the length of the gate electrode), but also greater than the sum of the source[5], channel and drain regions (7µm + 10µm + 7µm = 24µm), *i.e.*, 24µm ≦ L ≦35µm.

138. As for the d1 dimension, as discussed in [1f] for Ground 1, Hwang's layer 162/162a has overlap length d1 that shields at least the source and channel regions. Thus, applying Godo's dimensions, the minimum value for d1 is 17µm (the sum of source region and channel region lengths). Further, based on the teachings of Hwang that the drain electrode should not be shielded by layer 162/162a), the maximum value for d1 would be the entire channel layer <u>except</u> for the drain, *i.e.*, d1 ≦ L - 7µm.

	d1 (µm)	L (µm)
Minimum	17	24
Maximum	L-7	35

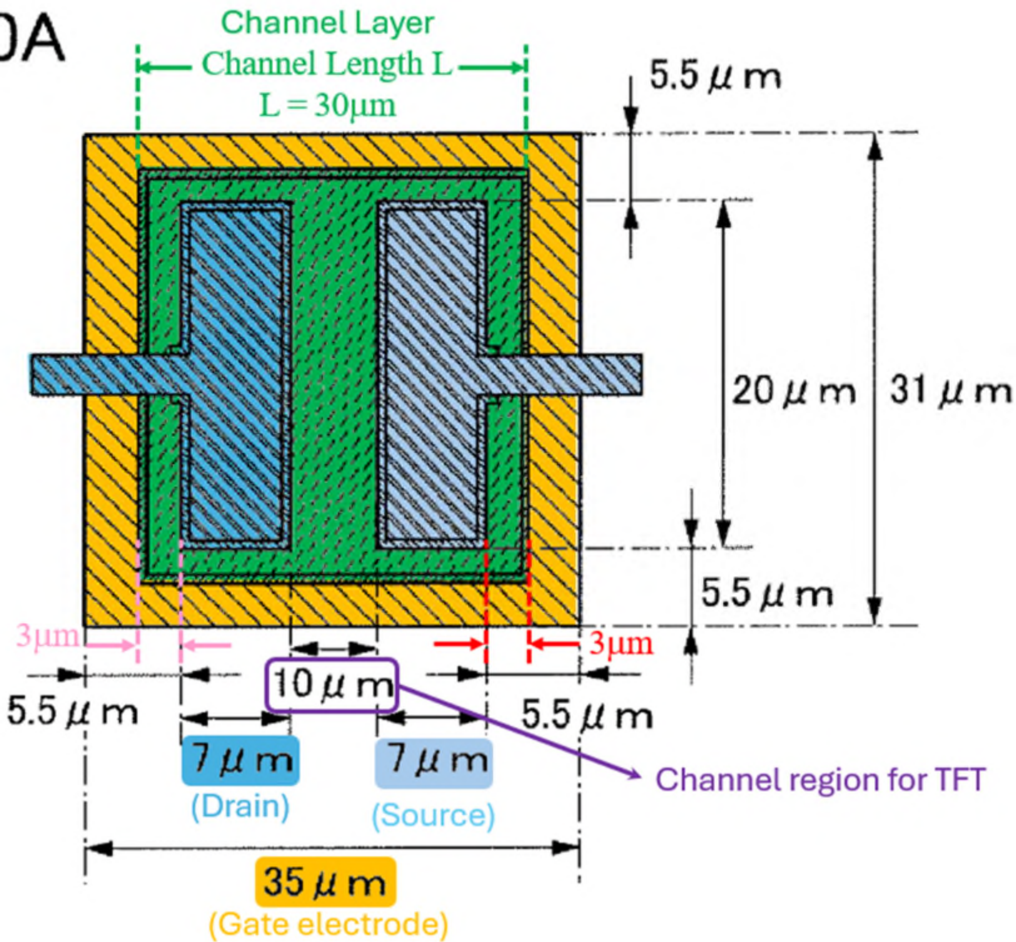
139. Based on these allowable ranges for d1 and L, the allowable range of d1/L can be determined. The minimum value for the fraction d1/L is achieved when the numerator d1 is minimized and the denominator L is maximized, *i.e.*, $d1_{min}/L_{max}$ is 17µm/35µm = 0.48. To maximize d1/L, the maximum value for d1 is

[5] In this calculation, I am including only the lengths for the source region, channel region and drain region as disclosed in Godo because I am calculating the lower bound for L. In other words, for a transistor to be consistent with the Godo disclosure, the length L must be large enough to accommodate the three expressly disclosed lengths, which is 24µm.

L-7μm as shown above. Substituting, the ratio $d1_{max}/L = (L-7μm)/L = 1-7/L$. Thus, d1/L is maximized when 7/L is minimized, *i.e.*, when L is maximized where L = 35μm. Thus, the maximum d1/L ratio is 1-7/35 = 1-0.2 = 0.8. Accordingly, using Godo's dimensions as disclosed in Fig. 20A, the resulting d1/L must be between 0.48≦d1/L≦0.8, wholly within the range as claimed in [1f] and [9f]. Stated differently, applying Hwang's teachings regarding shielding layer 162/162a on any transistor that is sized consistent with the express dimensions disclosed in Godo's Fig. 20A will necessarily result in d1/L between 0.48≦d1/L≦0.8.

140. Consider the following illustrative example that is consistent with the dimensions of Godo's Fig. 20A, where the TFT layout dimensions have mirror symmetry about the center of the channel region, and where L is 30μm (which is near the middle of the allowed range).

FIG. 20A

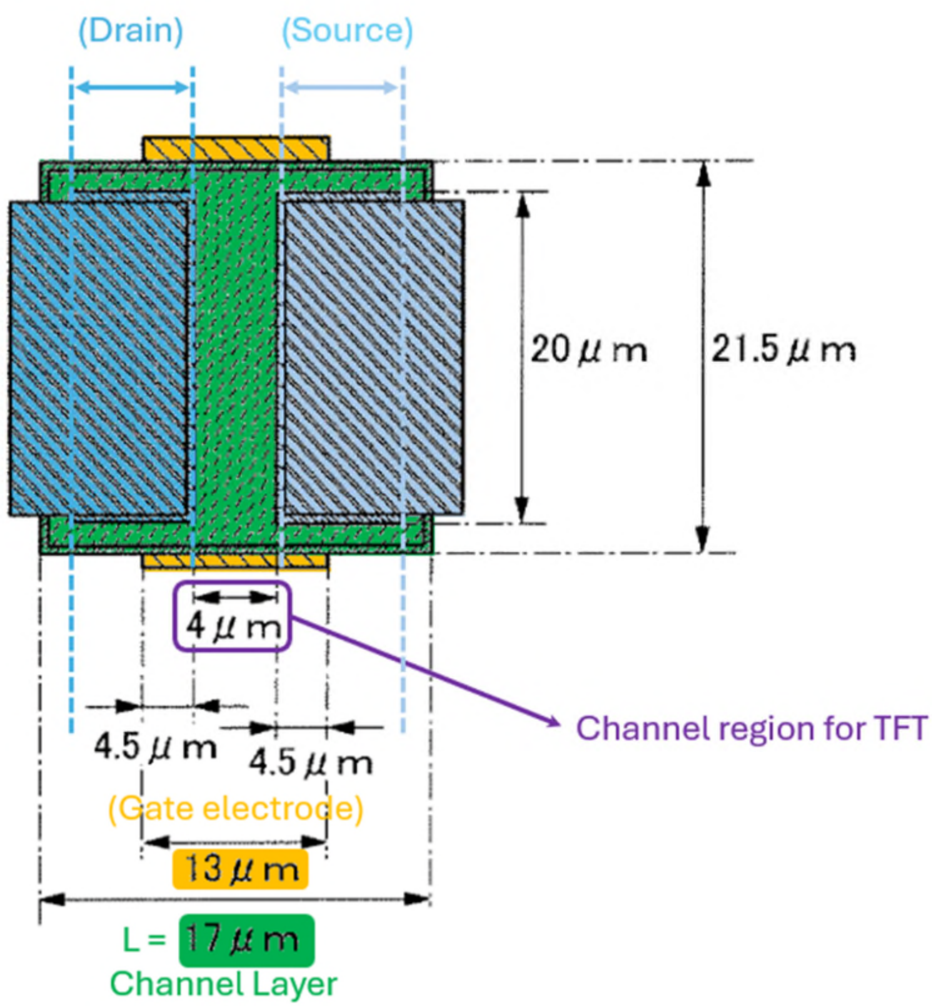


EX1005, Fig. 20A (annotations added). Mirror symmetry means the length between the right-edge of the source region to the right-edge of the (green) channel layer is 3μm (*i.e.*, the length between the two dotted red lines), which is also the length between the left-edge of the drain region to the left-edge of the channel layer (*i.e.*, the length between the two dotted pink lines). Hwang discloses that shielding layer 162/162a would extend from the right-edge of channel layer, covering the source region and the channel region and stopping at the drain region. This means d1 = 3μm+7μm+10μm = 20μm, while L = 30 μm. This leads to an illustrative value of d1/L of 0.67, which falls within the claimed range. Of course, this is but one illustrative example, whereas the more general analysis shows that any TFT with dimensions consistent with Godo's Fig 20A necessarily result in a d1/L within the claimed range.

2. Godo's Fig. 20B dimensions render obvious claimed d1/L ratio

141. The TFT shown in Godo's Fig. 20B has a channel direction that runs left-right, and the length of the channel layer is 17μm.

FIG. 20B



EX1005, Fig. 20B (annotations added). The channel region has length 4μm, but the exact lengths of the source/drain regions are not expressly disclosed, only that they are at least 4.5μm. The maximum source/drain length can be determined because the sum of the lengths of the source, channel and drain regions cannot exceed the channel layer length of 17μm. Thus, the maximum length for the source region is 8.5μm (taking the length of drain at the minimum 4.5μm), and the maximum length for the drain is 8.5μm (minimizing the source).

142. As for the d1 dimension, as discussed in [1f] for Ground 1, Hwang's layer 162/162a has overlap length d1 that shields at least the source and channel regions. Thus, applying Godo's Fig. 20B dimensions, the minimum value for d1 is 8.5μm (the sum of channel region length and the minimum source region length). Further, based on the teachings of Hwang that the drain electrode should not be shielded by layer 162/162a, the maximum value for d1 would be the entire channel layer <u>except</u> for the drain length (which should be minimized), *i.e.*, d1 ≦ 17 – 4.5μm.

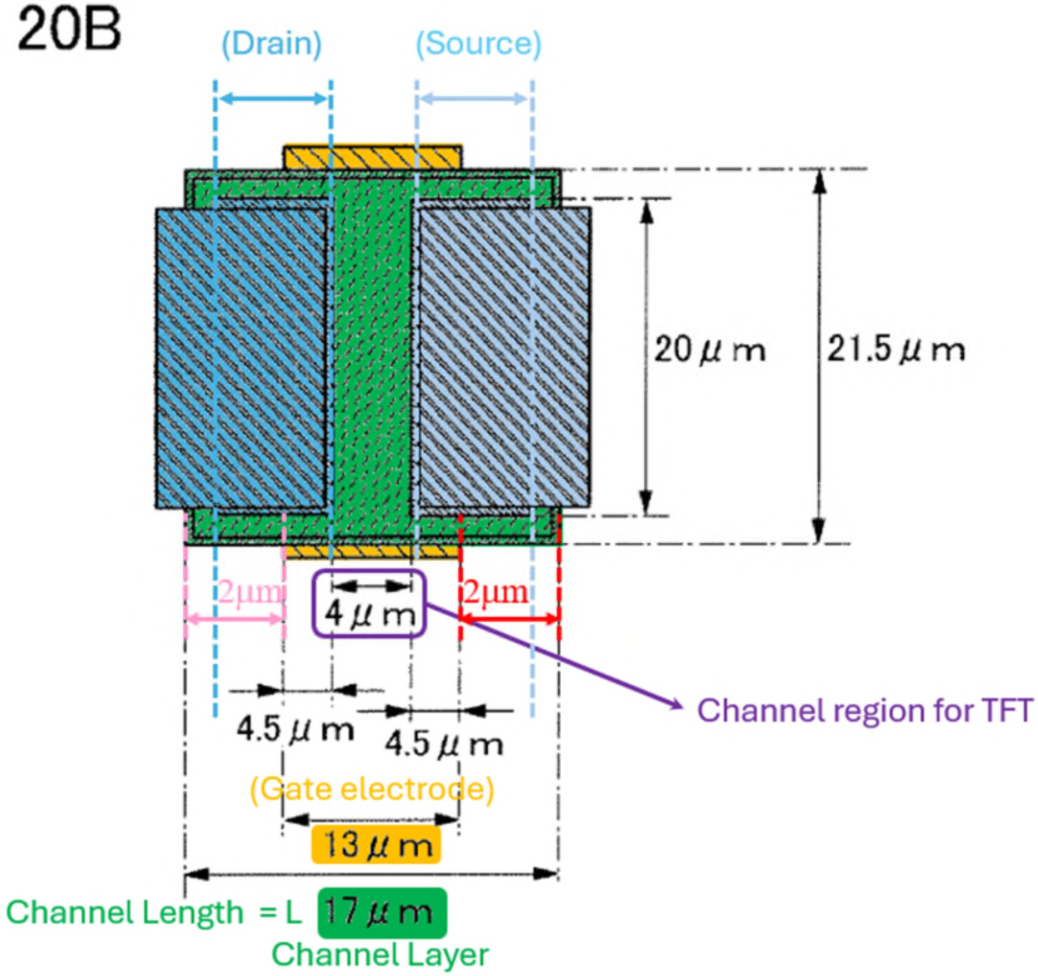
	d1 (μm)	L (μm)
Minimum	8.5	17
Maximum	12.5	17

143. Based on these allowable d1 values and the disclosed L dimension, the ratio d1/L must be between 8.5/17 and 12.5/17, or 0.5≦d1/L≦0.735, wholly within the range as claimed in [1f] and [9f]. Stated differently, applying Hwang's

teachings regarding shielding layer 162/162a on any transistor that is sized consistent with the express dimensions disclosed in Godo's Fig. 20B will necessarily result in d1/L between 0.5≦d1/L≦0.735.

144. Consider the following illustrative example that is consistent with the dimensions of Godo's Fig. 20B, where the TFT layout dimensions have mirror symmetry about the center of the channel region.

FIG. 20B



EX1005, Fig. 20A (annotations added). Mirror symmetry means the length between the right-edge of the gate electrode to the right-edge of the (green) channel layer is 2μm (*i.e.*, the length between the two dotted red lines), which is also the length between the left-edge of the gate electrode to the left-edge of the channel layer (*i.e.*, the length between the two dotted pink lines). Hwang discloses that shielding layer 162/162a would extend from the right-edge of channel layer, covering the source region and the channel region and stop at the drain region. This means d1 = 2μm+4.5μm+4μm = 10.5μm, while L = 17μm. This leads to an illustrative value of d1/L of 0.62, which falls within the claimed range. Of course, this is but one illustrative example, whereas the more general analysis shows that any TFT with dimensions consistent with Godo's Fig 20B necessarily result in a d1/L within the claimed range.

145. Accordingly, Hwang in combination with Godo discloses the d1/L dimensional ratio limitation recited in [1f] and [9f], and thus renders obvious claims 1 and 9.

146. Dependent claims 4, 6, 12 and 14 are not impacted by the d1/L ratio and therefore the limitations recited therein are disclosed by Hwang or rendered obvious for the same reasons as set forth in Ground 1.

D. Claims 17 and 18: "… wherein the conductive light-shielding pattern layer and the drain electrode are spaced by a distance along the channel direction in the vertical projection."

147. Regarding dependent claims 17 and 18, the antecedent basis for the conductive light-shielding pattern layer recited therein comes from limitation [1f]

or [9f]. Therefore, layer 162/162a meets the limitations recited in those dependent claims for at least the same reasons set forth above. Further, regarding the "spaced by a distance…" limitation, Hwang teaches that depending on need, some designs may shorten electrode 162a thus leading to the conductive light-shielding pattern layer and the drain electrode to be spaced by a distance along the channel direction in the vertical projection. *See* discussion in Ground 1, Claim 17 regarding EX1004, [0050], incorporated by reference herein. As discussed therein, a POSITA would have applied Hwang's teachings about shortening electrode 162a in Hwang's paragraph [0050] (based on balancing different needs of a particular design) such that more than half of the channel region remains shielded.

148. Shortening electrode 162a would decrease the d1 parameter and thereby reduce the d1/L ratio. Therefore, the upper bound for d1/L will still remain within the claimed range for [1f] and [9f]. To investigate the impact of the modification on the lower bound of d1/L, we use the relative proportions of the transistor dimensions as disclosed in Godo's Fig. 20A and shorten electrode 162a as set forth above (shielding half of the channel region). Thus, the minimum overlap length d1 is equal to the sum of the length of the source region (7μm) and half the length of the channel region (5μm), or 12μm. The allowable range for length L is unchanged (with a range between 24μm and 35μm), leading to $0.34 \leqq d1/L \leqq 0.5$, which remains within the claimed range of [1f] and [9f].

149. Using the relative proportions of the transistor dimensions as disclosed in Godo's Fig. 20B and shortening electrode 162a as set forth above, the overlap length d1 is decreased by half of the length of the channel region, *i.e.*, 2μm.

	Revised d1 (μm)	L (μm)
Minimum	8.5 – 2 = 6.5	17
Maximum	12.5 – 2 = 10.5	17

150. This leads to a ratio of d1/L such that 0.38≦d1/L≦0.62, which remains within the claimed range of [1f] and [9f].

151. Therefore, by configuring the conductive light-shielding pattern layer and the drain electrode such that they are spaced apart by a distance along the channel direction in a vertical projection, the d1/L ratio will decrease (compared to if the entire channel region is shielded), but the resulting d1/L ratio still lies within the range as recited in claims 1 and 9 from which claims 17 and 18 respectively depend. Accordingly, claims 17 and 18 are obvious in view of Hwang in combination with Godo.

XI. GROUND 3: HWANG AND YAMASHITA

A. Relationship to Ground 1

152. Hwang renders obvious the claims as set forth above for Ground 1. In the alternative, to the extent the light-shielding layer limitations are not inherent, taught, or otherwise rendered obvious to a POSITA by Hwang alone, they would

have been rendered obvious over the combination of Hwang and Yamashita. Ground 3 addresses the alternative, narrower construction of "conductive light-shielding pattern layer."

B. The Combination

153. The combination involves practicing the express teachings in Hwang as set forth in Ground 1, then adding the mental recognition that Hwang's layer 162/162a would indeed serve the intended design purpose of shielding the semiconductor layer from being exposed to light, to the extent Hwang does not inherently disclose or otherwise render obvious actually performing the light-shielding function. The recognition would have been obvious because it was well known and documented in the art that light can interact with semiconductors and adversely impact electrical performance of TFTs. The problem is exacerbated for transistors in devices like Hwang due to the proximity of integrated light emitting elements (either within the same pixel or in adjacent pixels). *See* Ground 1, Section related to the Knowledge of POSITA regarding light shielding.

154. A POSITA would have had a reasonable expectation of success in making the proposed combination because no modification to Hwang's device is necessary. Such a combination would have merely required express recognition that Hwang's layer 162/162a is not merely capable of but actually is intended to perform a light-shielding function, explained below. Further, a POSITA would

have recognized relevant similarities between Hwang and Yamashita. For example, both the light-shielding layer 67 in Yamashita and layer 162/162a in Hwang are electrically held at a constant potential. *Compare* EX1006, [0101], EX1004, [0085]-[0086]. *See also* illustrative light scattering paths, to be described further below.

C. "a conductive light-shielding pattern layer" ([1f], [9f], 4, 12, 17, 18)

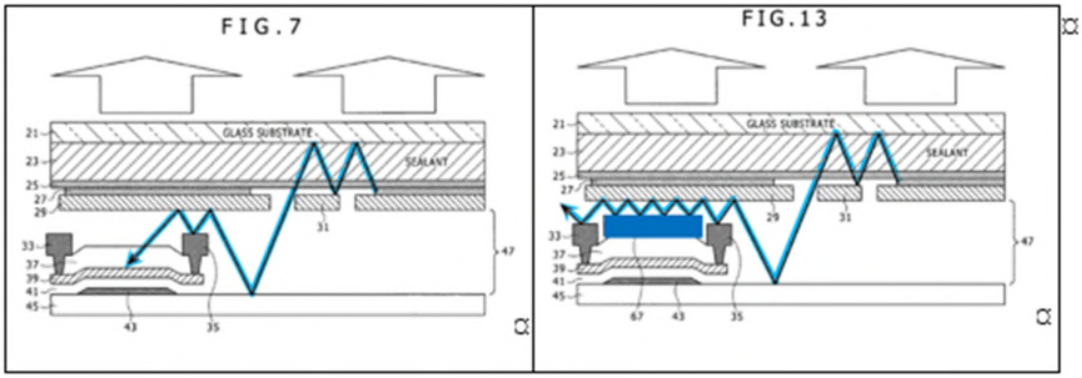
155. As shown in Ground 1, [1f], Hwang's layer 162/162a is the "conductive light-shielding pattern layer" with both conductive and light shielding properties. As designed by Hwang, layer 162/162a is intended to be electrically conductive since it serves as the electrical ground. EX1004, [0083]-[0087]. Although Hwang does not expressly state that an intended purpose of layer 162/162a is to perform a light-shielding function, it would have been obvious to POSITA for it to perform that intended purpose. For example, a POSITA would have recognized that since these devices are not fabricated in complete darkness, once layer 162/162a is formed, light will be incident on the device. Thus, layer 162/162a actually shields underlying structures (including drive transistor Td) from incident light.

156. Further, Hwang discloses that after layer 162/162a is formed, insulating layer 164 (made with optically transparent SiO_2 glass) is deposited and patterned thereon. EX1004, [0088]. Patterning layer 164 involves photolithography

that exposes the device to light. Thus, layer 162/162a actually shields Td from light during that fabrication step as well.

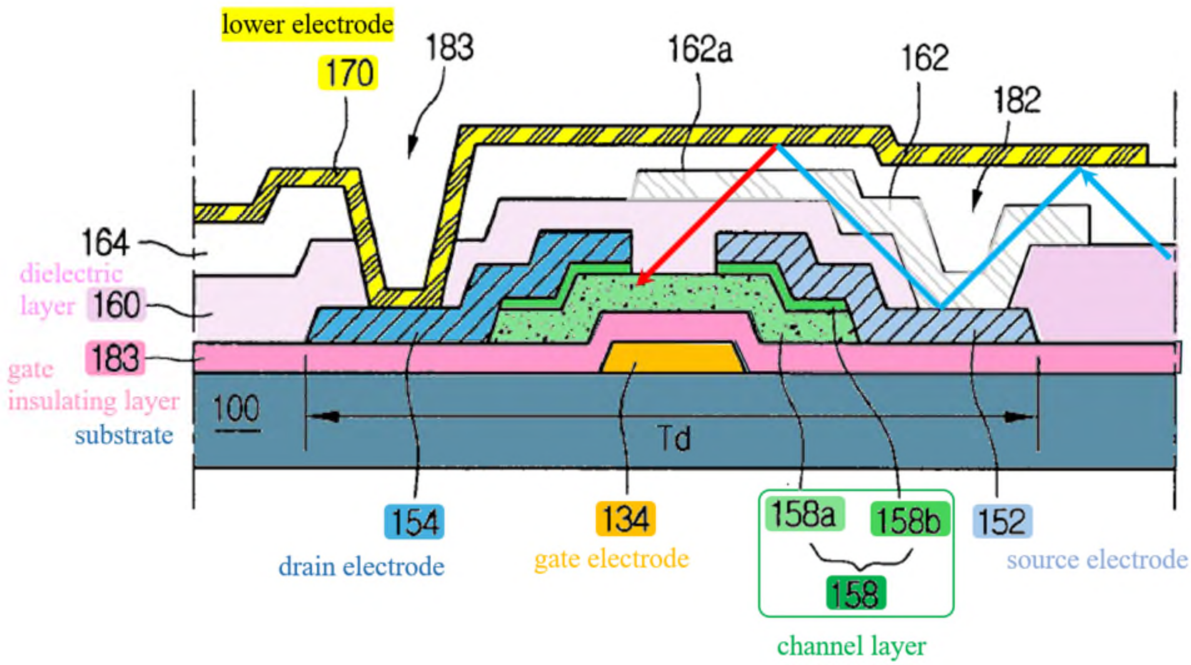
157. Moreover, Yamashita discloses that during operation, light generated by the LED's in adjacent pixels can be scattered internally enter channel region of TFTs integrated into the same chip and adversely impact device performance. EX1006, [0037]. *See* discussion of Yamashita in Ground 1, B (Knowledge of a POSITA). Figure 7 of Yamashita is an exemplary illustration[6] showing a "light ray" whereby light can be scattered into the channel region of a TFT. EX1006, Fig. 7, [0035]-[0037]. Yamashita teaches using a patterned metal layer (67) to shield the transistor from the scattered light. EX1006, [0095]-[0099]; compare Figs. 7 and 13 (annotations added to show scattered light with and without the light shield layer 67).

[6] A POSITA would have recognized that the illustrated light path is merely exemplary, and additional pathways exist for light to scatter into the channel region of the TFT. Further, while different devices may have arrangements of the reflective layers, the different arrangements of the reflective layers would merely lead to different pathways whereby light can reach the TFT channel regions. Thus, Fig. 7 of Yamashita illustrates the more general teachings that motivate the need for shielding the transistor from scattered light.



See also KR100853543 (EX1010, Abstract, <9>, <16>, <38>, <39>) disclosing the problem of light generated from an adjacent pixel adversely impacting a drive TFT, as discussed in Section IX.B (Knowledge of POSITA regarding light shielding).

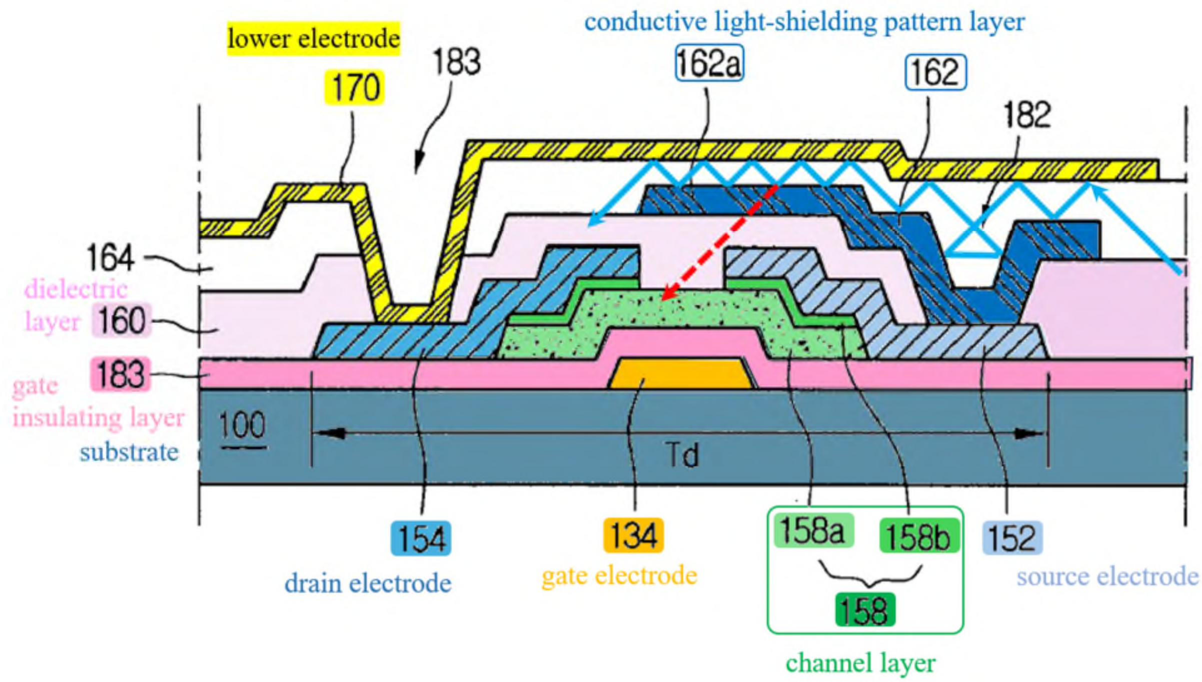
158. Thus, based on the teachings in Yamashita, a POSITA would have recognized that light generated by Hwang's LEDs can be internally scattered and enter the channel region of transistor Td, in the absence of metal layer 162/162a. This is illustrated using two versions of Fig. 6d reproduced below. The first version shows an exemplary optical pathway, with light (in light blue) originating from the right side then scattering within the structure (including by reflecting off lower electrode 170, similar to the reflection off electrode 29 in the configuration as disclosed in Yamashita) and reaching the channel region of Td (in red).



EX1004, Fig. 6d (annotations added with metal layer 162/162a partially obscured to illustrate light path[7] if it is absent).

159. The second version shows light originating from the same source, but the scattered light is repeatedly blocked by the light-shielding layer 162/162a from reaching the channel region of transistor Td.

[7] Note that layer 160 and layer 164 may be made of a material with the same index of refraction. EX1004, [0081], [0088]. Thus, the light path illustrated assumes negligible refractive effect at the interface of the two layers (in accordance with Snell's law). A POSITA would have recognized that depending on particular values of the indices of refraction of the two materials, the particular trajectory where light can irradiate the channel region may vary, but the illustration demonstrates that there are pathways for light from adjacent pixels to enter into the channel region of the drive transistor.



EX1004, Fig. 6d (annotations added) with red dotted arrow showing one exemplary light ray that is shielded from the channel region. Accordingly, in view of the Yamashita's teachings, a POSITA would have recognized Hwang's layer 162/162a as designed would serve the additional intended purpose of actually shielding light from the channel region of transistor Td (*i.e.*, part of the channel layer) and meet the limitation [1f]/[9f] even under the alternative construction.

160. Regarding dependent claims 4, 12, 17, 18, the antecedent basis for the conductive light-shielding pattern layer recited therein comes from limitation [1f] or [9f]. Therefore, layer 162/162a meets the limitations recited in those dependent claims for the same reasons set forth above. Dependent claims 6 and 14 are not impacted by the alternative construction for "conductive light-shielding pattern

layer" and therefore the limitations recited therein are disclosed by Hwang or rendered obvious for the same reasons as set forth in Ground 1.

XII. GROUND 4: HWANG, GODO AND YAMASHITA

A. Relationship to Grounds 1-3

161. Hwang renders obvious the claims as set forth above for Ground 1. In the alternative, to the extent the dimensional or light-shielding layer limitations are not taught or rendered obvious to a POSITA by Hwang alone, they would have been rendered obvious over the combination of Hwang and Godo, or Hwang and Yamashita, as set forth for Grounds 2 and 3 respectively. Ground 4 addresses an additional alternative where both the light-shielding layer limitations (under the narrower construction) and the dimensional limitations are not taught or rendered obvious to a POSITA by Hwang alone. Each of the challenged claims would have been obvious over the combination of Hwang in view of Godo and Yamashita.

B. The Combination

162. The motivation to combine Hwang and Godo is addressed in Ground 2, Section B, and the combination of Hwang and Yamashita is addressed in Ground 3, Section B. For the reasons set forth in Ground 3, Section B, adding Yamashita to the combination of Hwang and Godo would have required no modification to Hwang's layer 162/162a other than the designer intend that layer 162/162a perform the light-shielding function. Thus, a POSITA would have been motivated to combine these references, and would have had a reasonable

expectation of success for the same reasons set forth in Ground 2, Section B and Ground 3, Section B.

C. "a conductive light-shielding pattern layer… the conductive light-shielding pattern layer and the channel layer have an overlapping length d1, and 0.3≦d1/L≦0.85" ([1f], [9f], 4, 12, 17, 18)

163. *See* discussion in Ground 3, Section C discussing the "conductive light-shielding pattern layer" limitation and Ground 2, Section C discussing the d1/L dimensional ratio limitation and Ground 2, Section D discussing the "spaced by a distance…" limitation. Therefore, claims 1, 4, 6, 9, 12, 14, 17 and 18 are rendered obvious by Hwang in view of Godo for the reasons set forth therein.