

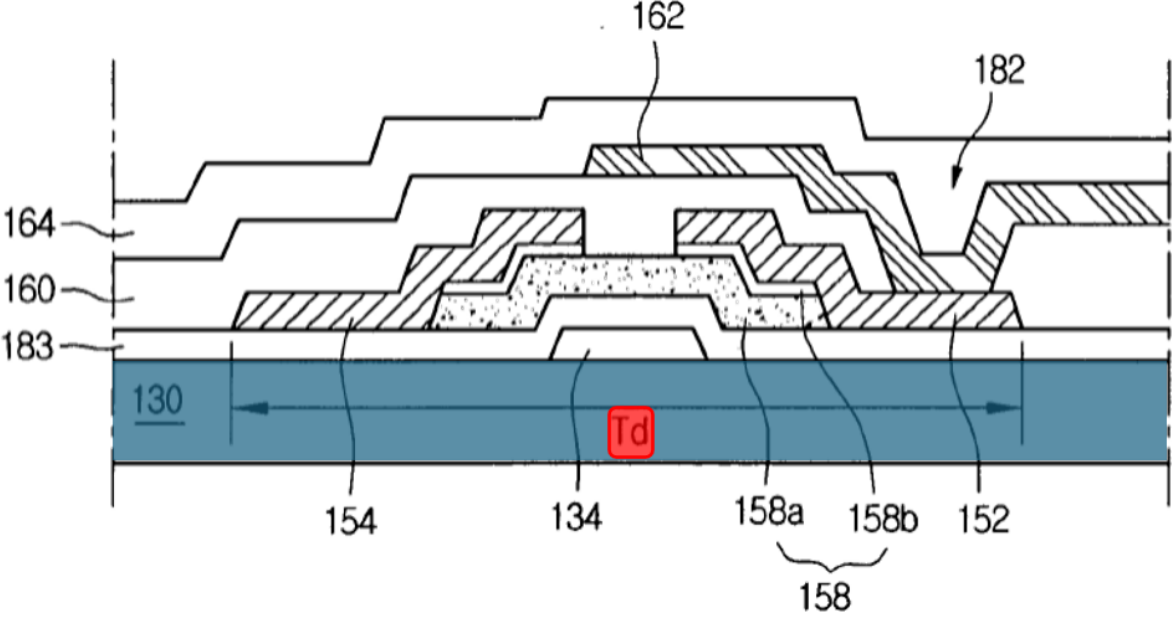
## Exhibit D-2

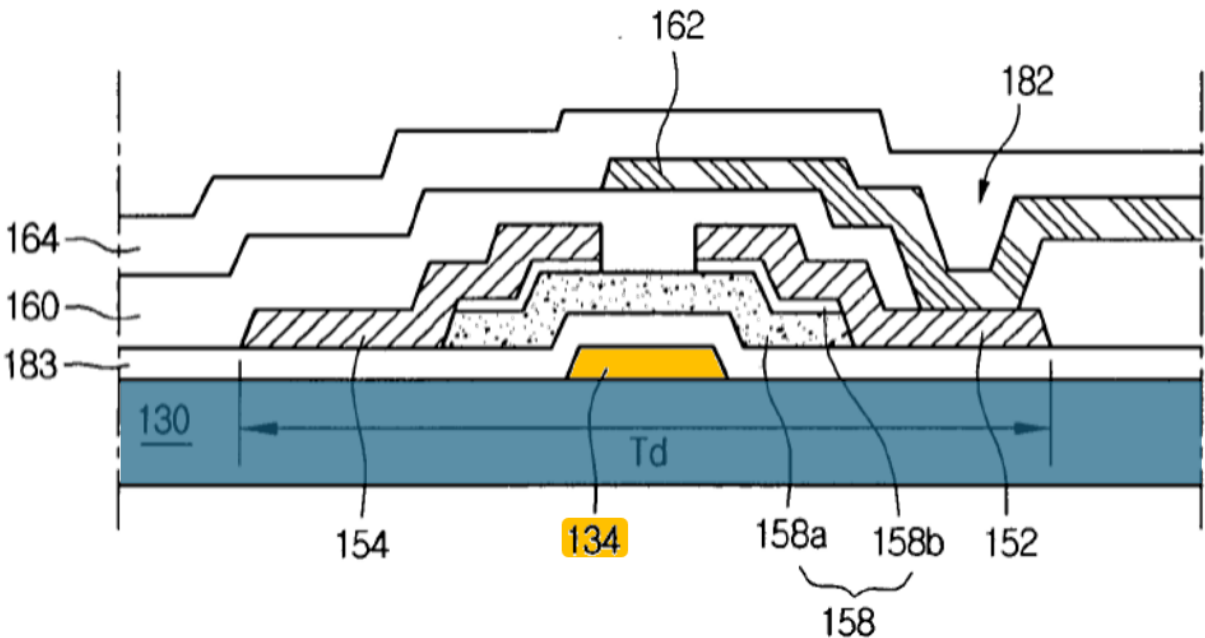
### US 2008/0158108 to Hwang et al. (“Hwang”) applied to U.S. Patent No. 8,604,471 (“471 patent”)

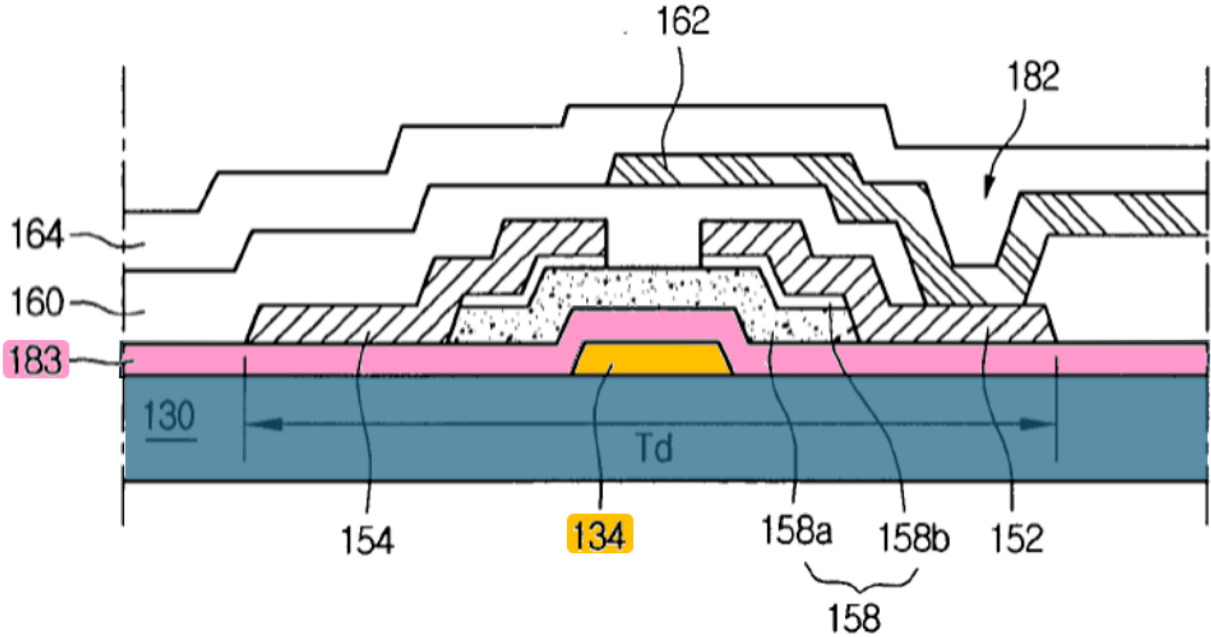
As demonstrated in the chart below, claims 1 and 17 of the 471 patent are anticipated by Hwang, and/or rendered obvious by Hwang (in combination with itself, the secondary references identified below, and/or the knowledge of a person of ordinary skill in the art). Hwang was published on July 3, 2008 and qualifies as prior art at least under pre-AIA 35 U.S.C. § 102(b). *See also*, materials from IPR2025-00238 incorporated herein by reference.

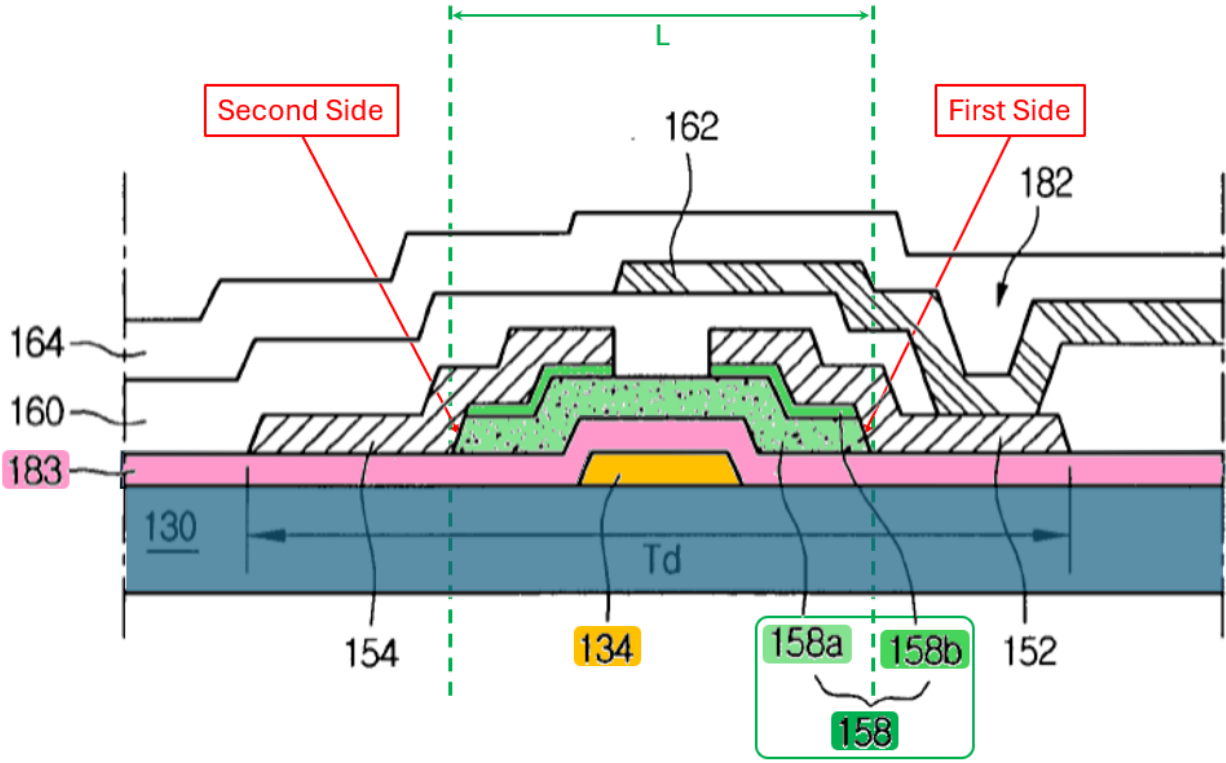
#### Secondary References:

- US 5838399 to Someya (“Someya”) was published on November 17, 1998 and qualifies as prior art at least under pre-AIA 35 U.S.C. § 102(b).
- Solid State Electronic Devices 4<sup>th</sup> Edition by Ben Streetman (“Streetman”) was published in 1995 and qualifies as prior art at least under pre-AIA 35 U.S.C. § 102(b).
- Handbook of Optics 2<sup>nd</sup> Edition Volume II by Michael Bass et al. (“HandbookII”) was published in 1995 and qualifies as prior art at least under pre-AIA 35 U.S.C. § 102(b).
- U.S. 2010/0148175 (“Godo”) published on June 17, 2010, filed on Dec. 8, 2009 and qualifies as prior art at least under pre-AIA 35 U.S.C. § 102(a), (b) and (e).
- U.S. 2009/0184898 (“Yamashita”) published on July 23, 2009 and qualifies as prior art at least under pre-AIA 35 U.S.C. § 102(b).
- KR100659756 published on December 19, 2006 and qualifies as prior art at least under pre-AIA 35 U.S.C. § 102(b).
- KR100853543 published on August 14, 2008 and qualifies as prior art at least under pre-AIA 35 U.S.C. § 102(b).
- Introduction to VLSI Systems by Carver Mead and Lynn Conway (“Mead”) was published in 1980 and qualifies as prior art at least under pre-AIA 35 U.S.C. § 102(b).
- Schaum’s Outline of Theory and Problems of Basic Circuit Analysis 2<sup>nd</sup> Edition by John O’Malley (“Schaum”) was published in 1992 and qualifies as prior art at least under pre-AIA 35 U.S.C. § 102(b).
- JP H09-90425A to Masumitsu (“Masumitsu”) was published on April 4, 1997 and therefore qualifies as prior art at least under pre-AIA 35 U.S.C. § 102(b).
- Galaxy S, that on information and belief, was on sale or offered for sale prior to August 12, 2010, and therefore qualifies as prior art at least under pre-AIA 35 U.S.C. § 102 (a), (b).

Claim Language	Exemplary Citations in Hwang
<p>[1pre] A semiconductor structure, disposed on a substrate, and comprising:</p>	<p>Hwang discloses “a semiconductor structure (a transistor, <b>Td</b>, driving an OLED), disposed on a substrate (130), and comprising (see claim1).”</p>  <p>Hwang at Fig. 6c (annotated); Figs. 6a-6d, 9; [0019], [0075]-[0095] (describing the manufacturing process for an organic electroluminescence device that includes at least a driving transistor and an OLED).</p>

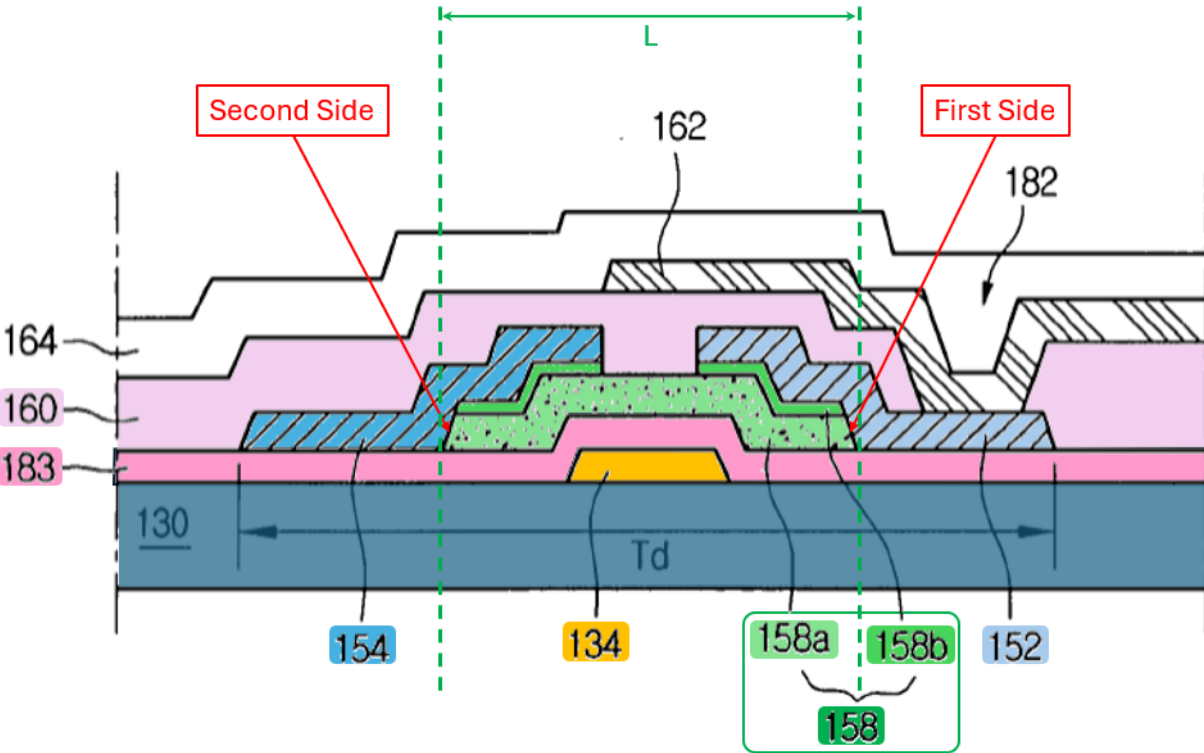
Claim Language	Exemplary Citations in Hwang
<p>[1a] a gate electrode, disposed on the substrate;</p>	<p>Hwang discloses “a gate electrode (134), disposed on the substrate (130).”</p>  <p>Hwang at Fig. 6c (gate electrode annotated in orange). Hwang discloses patterning a deposited metal layer on the substrate to form gate electrode 134. Hwang at [0076].</p>
<p>[1b] a gate insulating layer, disposed on the substrate, and covering the gate electrode;</p>	<p>Hwang discloses “a gate insulating layer (183), disposed on the substrate (130), and covering the gate electrode (134).”</p>

Claim Language	Exemplary Citations in Hwang
	 <p data-bbox="667 987 1900 1092">Hwang at Fig. 6c (gate insulating layer annotated in pink). Hwang discloses depositing an insulating material over the entire surface of the substrate (including the previously-formed gate electrode) to form the gate insulating layer. Hwang at [0077].</p>
<p data-bbox="191 1144 667 1321">[1c] a channel layer, disposed on the gate insulating layer and located above the gate electrode, wherein the channel layer has a channel length L along a channel direction</p>	<p data-bbox="667 1144 1921 1250">Hwang discloses “a channel layer (158), disposed on the gate insulating layer (183) and located above the gate electrode (134), wherein the channel layer has a channel length L along a channel direction and has a first side and a second side opposite to the first side.”</p>

Claim Language	Exemplary Citations in Hwang
<p>and has a first side and a second side opposite to the first side;</p>	 <p>Hwang at Fig. 6c (channel layer annotated in green). Hwang discloses patterning amorphous silicon layers deposited on the gate insulating layer to form active layer 158a and ohmic contact layer 158b. Hwang at [0078]. A POSITA would have understood that the claimed “channel layer” to include at least layer 158a that serves as the active semiconductor layer for the drive transistor, with the first and second sides as annotated. Further, the source of the drive transistor is on the right and the drain is on the left (Hwang at [0078]-[0080]), and thus a POSITA would have recognized that the channel layer has a channel length “L” along the channel direction as annotated.</p>

Claim Language	Exemplary Citations in Hwang
	<p>A POSITA would have further recognized that ohmic contact layers 158b are semiconductor layers that are part of the drive transistor whose presence allows the metal-semiconductor junction (source/drain electrode interface to the source/drain region of the transistor) to have linear <math>I-V</math> (current-voltage) characteristics. Streetman at 187-189. Therefore, they would be considered part of the claimed channel layer. However, in the Hwang configuration where layers 158a and 158b are vertically stacked, the channel length would be the same regardless of whether the ohmic contact layers are considered part of the claimed channel layer.</p>
<p>[1d] a source electrode and a drain electrode, located at the two opposite sides of the channel layer, and electrically connected to the first side and the second side of the channel layer, respectively;</p>	<p>Hwang discloses “a source electrode (152) and a drain electrode (154), located at the two opposite sides of the channel layer (158), and electrically connected to the first side and the second side of the channel layer, respectively.”</p>



Claim Language	Exemplary Citations in Hwang
<p>[1e] a dielectric layer, covering the source electrode, the drain electrode and the channel layer; and</p>	<p>Hwang discloses “a dielectric layer (160), covering the source electrode (152), the drain electrode (154) and the channel layer (158).”</p>  <p>The diagram is a cross-sectional view of a semiconductor device. At the bottom is a substrate (130) with a thickness <math>T_d</math>. A layer (183) is on top of the substrate. Above this is a channel layer (158) with two sub-regions, 158a and 158b. A drain electrode (154) is on the left, and a source electrode (152) is on the right. A gate stack (162) is positioned over the channel layer. A dielectric layer (160) covers the source and drain electrodes and the channel layer. A layer (164) is on top of the dielectric layer. A layer (182) is on the right side. A length <math>L</math> is indicated between two vertical dashed lines. A yellow box (134) is located under the channel layer.</p>

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	<p>Hwang at Fig. 6c (dielectric layer annotated in light pink). Hwang discloses depositing a dielectric material 160 over the entire substrate and thus covers the channel layer and the source and drain electrodes. Hwang at [0081].</p> <p>As explained in Figures 2, 3, 6b, 6c and accompanying text, via's are later made through the dielectric material 160 to allow for electrical connections to upper layers. The "cover" limitation does not preclude such openings. Claim 9 of the '471 patent requires an OLED and "a lower electrode, disposed on the dielectric layer and electrically connected to the drain electrode." '471 patent, claim 9. The specification explains this claimed connection is through a "contact window." <i>Id.</i> at 4:34-40. Thus, a POSITA would have understood that "cover" does not preclude such openings.</p>
<p>[1f] a conductive light-shielding pattern layer, disposed on the dielectric layer, and overlapped to a portion of the source electrode and a portion of the channel layer in a vertical projection, wherein the conductive light-shielding pattern layer does not overlap to the drain in the vertical projection, and the conductive light-shielding pattern layer and the channel layer have an</p>	<p>Hwang discloses "a <a href="#">conductive light-shielding pattern layer (162/162a)</a>, disposed on the <a href="#">dielectric layer (160)</a>, and overlapped to a portion of the <a href="#">source electrode (152)</a> and a portion of the <a href="#">channel layer (158)</a> in a vertical projection, wherein the conductive light-shielding pattern layer does not overlap to the drain in the vertical projection, and the conductive light-shielding pattern layer and the channel layer have an <a href="#">overlapping length d1</a>, and <math>0.3 \leq d1/L \leq 0.85</math>."</p>



Claim Language	Exemplary Citations in Hwang
	<p>aluminum alloy, tungsten, copper, molybdenum and titanium as exemplary metals suitable for layer 162/162a (ground line and auxiliary electrode). Hwang at [0101], claim 13.</p> <p>The '471 patent discloses “metal” as the broad class of materials suitable for the conductive light-shielding pattern layer. '471 patent at 3:58-61, 4:40-5:9. A POSITA would have readily recognized that the exemplary metals and metal alloys disclosed by Hwang have high electrical conductivity because they are well-known metal materials used for interconnects in semiconductor devices. This recognition is further reinforced by the fact that layer 162 serves as the electrical ground line, and thus would be fabricated with a material that is a good electrical conductor.</p> <p>To the extent Hwang does not expressly or inherently disclose this limitation, this limitation is rendered obvious in view of Hwang alone, or Hwang in view of Yamashita, or Hwang in view of Godo, or Hwang in view of Yamashita and Godo, or Hwang in view of the references cited in this limitation with the knowledge of a POSITA.</p> <p>While Hwang does not explicitly teach that layer 162/162a serves the intended purpose of light-shielding, a POSITA would have understood that the layer formed using any one of these exemplary metals would have light-shielding properties for multiple reasons. First, a POSITA would have recognized that these exemplary metals are good reflectors of light. Therefore, most of the light incident on these metal materials are reflected rather than transmitted through the material. <i>See e.g.</i>, Paper 39 (Final Written Decision) <i>Home Depot USA, Inc. v. Lynk Labs, Inc.</i> IPR2021-01541, at 32 (holding “Aluminum, for example, indisputably reflects light.”). Light incident on these exemplary metallic surfaces would instead be reflected back, as is well known to those of skill in the art.</p> <p>Second, with respect to any light that is not reflected back (which will be a small fraction of the incident light), most of it will be absorbed by these metal materials well before it can travel through the thickness of the material. HandbookII at 35.6. A POSITA would have recognized that the absorption rate of light (<i>i.e.</i>, an electromagnetic field) as it propagates within a metal material is characterized by its “skin depth,” a parameter indicating the distance where the light</p>

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	<p>intensity has attenuated by about 86.5% due to absorption in the material. HandbookII at 35.3-35.7. In other words, after accounting for incident light being reflected at the surface, less than 14% of the light intensity will penetrate past the skin depth, with the light intensity continuing to decrease the further the distance it propagates into the material.</p> <p>The skin depth parameter <math>\delta</math> is given by the formula <math>\delta = \sqrt{\frac{2}{\omega\mu\sigma}}</math>, where <math>\omega</math> is the frequency of the electromagnetic wave, <math>\mu</math> is the magnetic susceptibility of the material, and <math>\sigma</math> is the electrical conductivity. HandbookII at 35.6 (equation 11). This equation shows that the skin depth (or the penetration depth) of an electric field through a material depends inversely on its frequency and on the conductivity of the material, meaning the skin depth will decrease as frequency increases or as conductivity increases. As is well known, metals are highly conductive, and light oscillates at very high frequencies (light in the visible spectrum is in the Terahertz range, where 1 Terahertz (THz) is <math>10^{12}</math> oscillations per second). Therefore, both factors contribute to a very small penetration depth for light incident on a metal (due to its high conductivity), thus motivating the use of a conductive light shielding layer. Indeed, at optical frequencies, the skin depth of most metals is only approximately 50 nanometers (where one nanometer is one billionth of a meter). HandbookII at 35.6.</p> <p>The skin depth equation also shows that as the frequency of the electric field decreases, the skin depth parameter increases, meaning the electric field can penetrate deeper into the metal. Thus, to effectively limit the penetration of a lower frequency electromagnetic wave (e.g. microwave radiation that oscillates at <math>10^6 - 10^9</math> Hz) using the same material, a thicker layer of that material is required (when compared to a higher frequency electromagnetic wave such as light in the optical spectrum). This is relevant because in Hwang's embodiment of Fig. 6d (shown above), Hwang expressly teaches that auxiliary electrode 162a must shield the channel region of the TFT from the influence of the time-varying electric field caused by electrode 170 when the OLED is driven at different electrical currents to produce different levels of brightness. Hwang at [0014]-[0020], [0050], [0065]-[0068], [0072], [0101]. The frequency bandwidth of these electrical drive signals would be well below optical frequency range, reaching at most the microwave frequency range. As expressly taught by Hwang, auxiliary electrode 162a in Fig. 6d must be sufficiently thick in</p>

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	<p>order to be effective at shielding these relatively low frequency electric fields propagating from electrode 170 when driving the OLED. Because light oscillates at a higher frequency, it will not penetrate Hwang's auxiliary electrode 162a as deeply as the lower frequency electric field induced by the OLED drive signal. Thus, a POSITA would understand that because Hwang's auxiliary electrode 162a is effective at shielding low frequency electric fields from electrode 170 (as expressly disclosed by Hwang), it must necessarily be effective at shielding light also. Accordingly, Hwang's patterned layer 162/162a qualifies as a conductive light-shielding pattern layer, at least because most if not all of the incident light is either reflected back or absorbed by the metal material.</p> <p>Third, it is expressly known in the art that metals such as aluminum, aluminum alloy, tungsten, copper, molybdenum and titanium are conductive materials with light-shielding (or light blocking) properties suitable for shielding a semiconductor from light. Godo at [0006] and [0012] (explaining the use of a gate electrode to shield a semiconductor layer in a TFT from light), [0045] (disclosing the use of metal materials including aluminum, tungsten, copper, molybdenum, titanium and their alloys for the gate electrode); Yamashita at [0046] (use of metal wiring layer to shield a TFT from light), [0096] (disclosing the use of aluminum and molybdenum for the light-shielding pattern); KR100659756 at 7 (disclosing the use of aluminum and molybdenum for the light-shielding pattern); Someya at 12:35-44 (disclosing that an aluminum film has high light shielding properties).</p> <p>To the extent Hwang does not inherently disclose or otherwise render obvious actually performing the light-shielding function, it would have been obvious to configure Hwang's layer 162/162a to indeed serve the intended design purpose of shielding the semiconductor layer from being exposed to light. This would have been obvious because it was well known and documented in the art that light can interact with semiconductors and adversely impact electrical performance of TFTs. The problem is exacerbated for transistors in devices like Hwang due to the proximity of integrated light emitting elements (either within the same pixel or in adjacent pixels).</p>

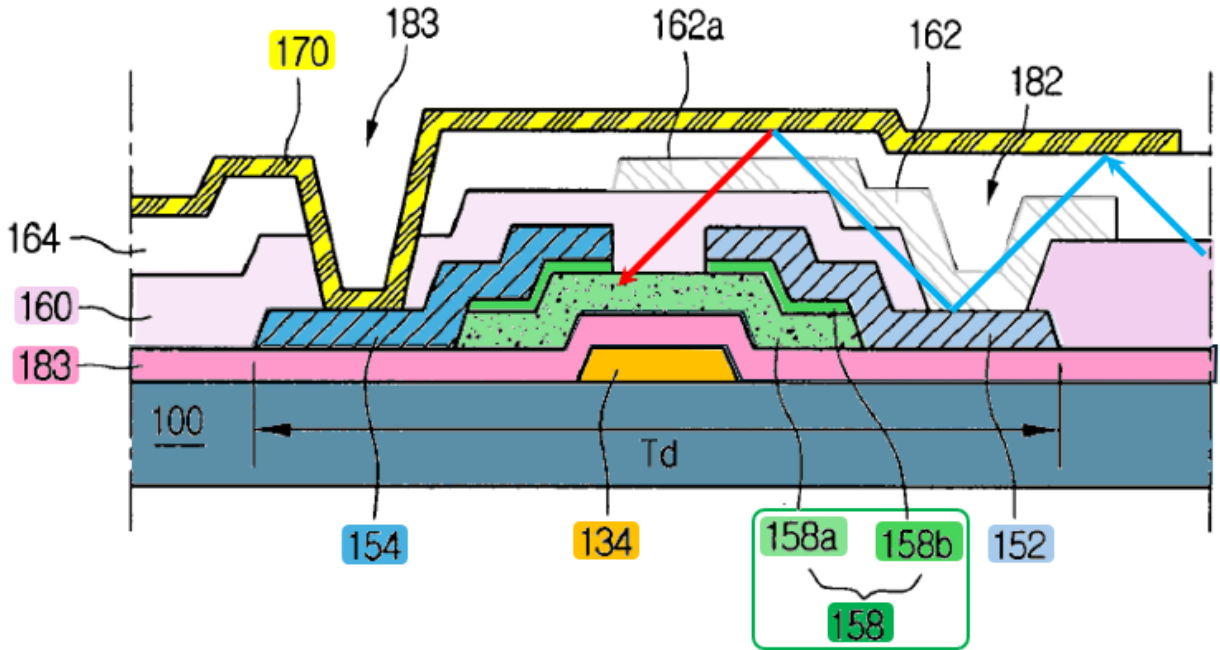
Claim Language	Exemplary Citations in Hwang
	<p>It would have been obvious to include a conductive light shielding pattern layer to overlap with a portion of the channel layer for light shielding. The problems associated with light entering a channel region of a transistor and the adverse impacts on transistor performance are well-known and extensively documented in the prior art. Some exemplary references are summarized herein. Light can create electron-hole pairs (“EHPs”) in semiconductors and thus alter the density of charge carriers in the material. Streetman at 96-97, 103; <i>see generally</i> Chapter 4. These EHPs alter the electrical properties of the semiconductor (and thus the device), including <i>e.g.</i>, the threshold voltages in transistors and/or increase leakage current. These problems are especially acute for optoelectronic devices due to the presence of light generating elements integrated with, and in close proximity to, such transistors.</p> <p>This problem is discussed in Yamashita. Yamashita relates to organic electroluminescent devices that incorporates transistor circuitry. Yamashita at [0009]-[0010]. Yamashita addresses the known problem in the art when light enters the channel region of a transistor and causes a shift in the threshold voltage of the transistor. Yamashita at [0036]-[0038]. Yamashita discloses that in such devices, light can enter a channel region of a transistor (even one located in an adjacent pixel) due to internal scattered light from repeated reflections. Yamashita at [0035]-[0037], Fig. 7. Such shifts in the threshold voltage are undesirable in drive transistors for organic light emitting diodes (“OLEDs”) as they lead to unintended fluctuations in the drive current, and therefore fluctuations in the brightness of the OLED element. Yamashita at [0013]-[0015], [0038]-[0042], Figs. 8-9. Yamashita discloses a solution to this problem is to form a light-shielding layer that is arranged above the channel region of the TFT in order to shield it from light. Yamashita at [0045]-[0048], [0052], [0095]-[0099] (disclosing “the light shield pattern 67 should preferably be so arranged as to cover the sampling transistor T1 as well as the entire channel layer of the driving transistor T2”), Fig. 13. Yamashita discloses that while any material that reduces the amount of scattered light entering the thin-film transistor would help address the problem, metal materials are superior. Yamashita at [0048]-[0049], [0136]-[0137]. Yamashita further teaches that the metal light-shielding layer should be electrically connected to a constant potential line. Yamashita at [0047], [0101]-[0103].</p>

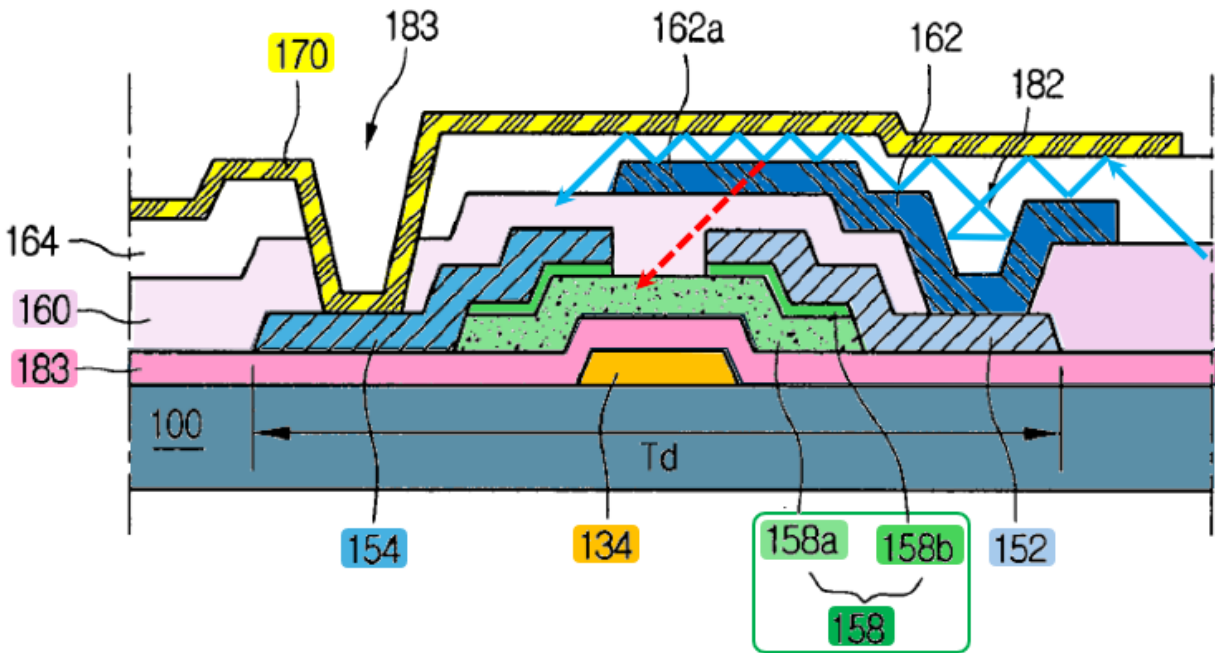
Claim Language	Exemplary Citations in Hwang
	<p>Similarly, Godo discloses that it is well-known in the art that when semiconductor material (in a transistor of a display device) is irradiated with light, light leakage current will be generated due to the photovoltaic effect and deteriorates the display quality. Godo at [0004]. Godo discloses that mitigation techniques such as shielding the semiconductor layer from light were known. <i>Id.</i>, [0004]-[0006]. Reducing the leakage current can be accomplished by shielding the semiconductor layer with a conductive electrode made with various metals and their alloys. <i>Id.</i>, [0012]; [0015]-[0016]; [0045].</p> <p>KR100853543 likewise discloses the use of a light-blocking film in an OLED display to stop light (external or from an adjacent pixel) from entering the semiconductor layer of a TFT to ensure stable driving properties for the transistor. KR100853543 at Abstract, &lt;9&gt;, &lt;16&gt;, &lt;38&gt;, &lt;39&gt;. KR100853543 explains that this light can generate a photocurrent in the semiconductor layer and adversely impact the driving properties of the TFT. KR100853543 at &lt;15&gt;.</p> <p>KR100659756 is yet another reference that discloses the problem with light entering the semiconductor layer of a TFT, particularly those with a bottom-gate structure. KR100659756 at 5. KR100659756 discloses to use one or more metals (including aluminum and molybdenum that are good light reflectors and good electrical conductors) as suitable materials for forming a light-blocking film to prevent both external light as well as internally generated light (<i>e.g.</i> from the OLED) from causing a negative effect on the TFT. KR100659756 at 7.</p> <p>This well-known problem (as documented by any one or more of these references) would have provide a POSITA with the motivation to incorporate light shielding.</p> <p>A POSITA would have had a reasonable expectation of success in making the proposed combination because no modification to Hwang’s device is necessary. Such a combination would have merely required express recognition that Hwang’s layer 162/162a is not merely capable of but actually is intended to perform a light-shielding function. Further, a POSITA would have recognized relevant similarities between Hwang and Yamashita. For example, both the light-shielding layer 67 in Yamashita and layer 162/162a in Hwang are electrically held at a constant</p>

Claim Language	Exemplary Citations in Hwang
	<p>potential. <i>Compare</i> Yamashita at [0101] with Hwang at [0085]-[0086]. <i>See also</i> illustrative light scattering paths, to be described further below.</p> <p>As shown above, Hwang’s layer 162/162a is the “conductive light-shielding pattern layer” with both conductive and light shielding properties. As designed by Hwang, layer 162/162a is intended to be electrically conductive since it serves as the electrical ground. Hwang at [0083]-[0087]. Although Hwang does not expressly state that an intended purpose of layer 162/162a is to perform a light-shielding function, it would have been obvious to POSITA for it to perform that intended purpose. For example, a POSITA would have recognized that since these devices are not fabricated in complete darkness, once layer 162/162a is formed, light will be incident on the device. Thus, layer 162/162a actually shields underlying structures (including drive transistor Td) from incident light.</p> <p>Further, Hwang discloses that after layer 162/162a is formed, insulating layer 164 (made with optically transparent SiO<sub>2</sub> glass) is deposited and patterned thereon. Hwang at [0088]. Patterning layer 164 involves photolithography that exposes the device to light. Thus, layer 162/162a actually shields Td from light during that fabrication step as well.</p> <p>Moreover, Yamashita discloses that during operation, light generated by the LED’s in adjacent pixels can be scattered internally enter channel region of TFTs integrated into the same chip and adversely impact device performance. Yamashita at [0037]. Figure 7 of Yamashita is an exemplary illustration<sup>1</sup> showing a “light ray” whereby light can be scattered into the channel region of a TFT. Yamashita at Fig. 7, [0035]-[0037]. Yamashita teaches using a patterned metal layer (67) to shield the transistor from the scattered light. Yamashita at [0095]-[0099]; compare</p>

<sup>1</sup> A POSITA would have recognized that the illustrated light path is merely exemplary, and additional pathways exist for light to scatter into the channel region of the TFT. Further, while different devices may have arrangements of the reflective layers, the different arrangements of the reflective layers would merely lead to different pathways whereby light can reach the TFT channel regions. Thus, Fig. 7 of Yamashita illustrates the more general teachings that motivate the need for shielding the transistor from scattered light.

Claim Language	Exemplary Citations in Hwang
	<p data-bbox="674 289 1894 358">Figs. 7 and 13 (annotations added to show scattered light with and without the light shield layer 67).</p> <div data-bbox="674 391 1915 813"> </div> <p data-bbox="674 886 1843 956"><i>See also</i> KR100853543 at Abstract, &lt;9&gt;, &lt;16&gt;, &lt;38&gt;, &lt;39&gt; disclosing the problem of light generated from an adjacent pixel adversely impacting a drive TFT.</p> <p data-bbox="674 992 1915 1243">Thus, based on the teachings in Yamashita, a POSITA would have recognized that light generated by Hwang’s LEDs can be internally scattered and enter the channel region of transistor Td, in the absence of metal layer 162/162a. This is illustrated using two versions of Fig. 6d reproduced below. The first version shows an exemplary optical pathway, with light (in light blue) originating from the right side then scattering within the structure (including by reflecting off lower electrode 170, similar to the reflection off electrode 29 in the configuration as disclosed in Yamashita) and reaching the channel region of Td (in red).</p>

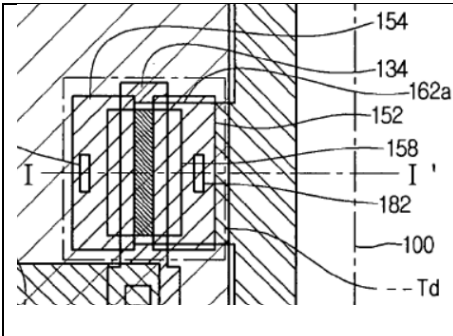
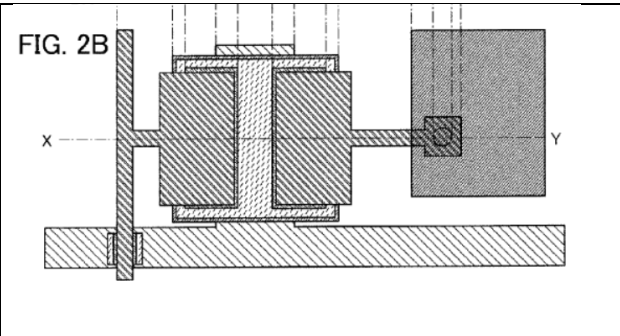
Claim Language	Exemplary Citations in Hwang
	 <p data-bbox="667 1027 1900 1101">Hwang at Fig. 6d (annotations added with metal layer 162/162a partially obscured to show light path if it is absent).</p> <p data-bbox="667 1133 1900 1239">The second version shows light originating from the same source, but the scattered light is repeatedly blocked by the light-shielding layer 162/162a from reaching the channel region of transistor Td.</p>

Claim Language	Exemplary Citations in Hwang
	 <p data-bbox="667 990 1921 1177">Hwang at Fig. 6d (annotations added) with red dotted arrow showing one exemplary light ray that is shielded from the channel region. Accordingly, in view of the Yamashita's teachings, a POSITA would have recognized Hwang's layer 162/162a as designed would serve the additional intended purpose of actually shielding light from the channel region of transistor Td (<i>i.e.</i>, part of the channel layer) and meet the limitation [1f].</p> <p data-bbox="667 1209 1921 1351">As discussed for [1c] <i>supra</i>, Hwang's semiconductor layer 158 has length L in the channel direction. Layer 158 comprises the source, channel and drain regions of the drive transistor Td (in the form of a TFT) for the OLED device. Hwang at [0075]-[0080]. As depicted in Fig. 6a-6d, the source, channel and drain regions of Hwang's transistor Td is symmetric with respect to the</p>

Claim Language	Exemplary Citations in Hwang
	<p>center of the channel region such that the length<sup>2</sup> of the source and drain regions is the same. Further, Hwang depicts drive transistor Td has a channel region (<i>i.e.</i>, the part of layer 158 not covered by ohmic contacts 158b, Hwang at [0080]) whose length is no greater than that of the source or the drain regions.</p> <p>Thus, a POSITA would review the disclosure in Hwang and at once envisage a commonly-used TFT configuration in which (a) the source and drain regions are equal in length, and (b) where the length of the channel region is no greater than that of the source (or drain) region. At a minimum, Hwang’s disclosure would have rendered obvious such a TFT configuration. A POSITA would have recognized this as a common TFT configuration for OLED drive transistors because a shorter channel region length typically allows higher current and faster switching speeds, whereas lithography limits and the necessity for forming highly conductive source/drain contacts typically result in source/drain regions that are similarly sized but larger than the channel region (<i>i.e.</i>, condition (b)). Once the source/drain regions are large enough to accommodate electrical connection to highly conductive contacts, TFT drive transistor designs would not further increase those dimensions unnecessarily. This is because a general design goal would be to increase pixel density in an OLED display panel (thus leaving the source and drain regions equally sized, <i>i.e.</i>, condition (a)). Thus, a POSITA would have recognized the figures in Hwang to at least render obvious (if not outright depict) a well-known and common TFT drive transistor configuration having relative proportional dimensions as set forth above.</p> <p>Based on these two conditions for this common (or at least obvious) TFT configuration, a POSITA can ascertain the range for the length of the drain region as a fraction of the total length L. For fixed L, the drain region length reaches a value of approximately 0.33L where the source, channel and drain regions are of equal lengths. A POSITA would have recognized that transistor performance generally improves (<i>e.g.</i>, higher speed and greater power efficiency) when the length of the channel region is reduced. Mead at 33-37. This performance improvement is the basis for the drive towards miniaturization of semiconductor devices, manifesting itself as the</p>

<sup>2</sup> Unless other specified, the term “length” with respect to the source, channel and drain regions as used herein refers to the length in the channel direction.

Claim Language	Exemplary Citations in Hwang
	<p>well-known Moore's Law. Accordingly, a POSITA would have recognized that common transistor designs may have a channel region length that is less than the length of the source/drain regions due to the advantages of a decreased channel region length. Mead at 33-37. Since the drain region length is equal to <math>0.33L</math> (when the source, drain and channel regions are equal lengths), decreasing the length of the channel region relative to the source/drain region would lead to a corresponding increase in the source/drain region length such that it is greater than <math>0.33L</math>. Therefore, a POSITA would have recognized that for many common transistor configurations, <math>0.33L</math> would be a typical lower bound for the drain channel length. Of course, a POSITA would also have recognized that the channel region length cannot be reduced too much because of fabrication tolerances and also because of the well-known short channel effect. Streetman at 298-299, 325-327. However, even if we consider an extreme hypothetical design where the channel region length is negligibly small relative to the equally-sized source and drain regions (such that each of these regions make up 50% of the semiconductor layer 158), the drain region length would still reach a maximum value of no greater than <math>0.5L</math>. Thus, the relative size of the drain region is bounded between <math>0.33L</math> and <math>0.5L</math>. Since the source region is the same size as the drain region, its length is likewise bounded between <math>0.33L</math> and <math>0.5L</math>. The length of the channel region would make up the difference (<i>i.e.</i>, <math>L</math> - length of source - length of drain), thus ranging between approximately <math>0L</math> (in the extreme hypothetical case) to <math>0.33L</math>.</p> <p>Hwang discloses the conductive light-shielding pattern layer 162/162a to overlap both the source and channel regions, but not the drain region. Therefore, the overlapping length <math>d1</math> is (<math>L</math> - length of drain) which is between <math>0.5L</math> and <math>0.67L</math>. Accordingly, a POSITA would have recognized that any TFT drive transistor <math>Td</math> so configured would result in a <math>d1/L</math> ratio to fall between 0.5 to 0.67, the entirety of which falls within the claimed range of 0.3 to 0.85.</p> <p>Alternatively, it would have been obvious to a POSITA to take the figures in Hwang at face value and glean therefrom relative dimensions for the length of the source, drain and channel regions of driving transistor <math>Td</math> to be approximately <math>0.38L</math>, <math>0.38L</math> and <math>0.24L</math> respectively. Hwang at Fig. 6d. A POSITA applying the teachings of Hwang regarding layer 162/162a to not overlap</p>

Claim Language	Exemplary Citations in Hwang
	<p>with the drain region of driving transistor Td would arrive at a conductive light-shielding pattern layer having a d1/L value of 0.62L, which falls well within the claimed range of 0.3 to 0.85.</p> <p>In the alternative, to the extent the claimed relative dimensions of the source, channel and drain regions of a TFT are not taught or rendered obvious to a POSITA by Hwang alone such that the resulting device would meet the claimed d1/L ratio (as set forth above), those dimensions would have been rendered obvious over the combination of Hwang and Godo. As discussed below, Godo discloses specific dimensions for bottom gate TFTs. Godo at [0199], [0201], Figs. 1A, 1B, 2A, 2B, 4A, 4B, 20A and 20B.</p> <p>Hwang broadly discloses an arrangement of semiconductor materials to form a TFT, and metallic materials for shielding the channel region in the transistor in an organic luminescent device. The combination of Hwang and Godo modifies Hwang's general teachings for a broad genus of TFTs with Godo's disclosure of more particular species of TFTs (with specific dimensions for the source, channel and drain regions for the transistor) according to known methods to yield predictable results. Compare, e.g., Hwang at Fig. 2 (top-down view of drive transistor Td) and Godo at Fig. 2B (see also Figs. 4B and 20B).</p> <div style="display: flex; justify-content: space-around; align-items: center;">   </div> <p>As discussed above, suitable dimensions for such transistors would have been well known in the art, and a POSITA would have immediately recognized Hwang's Figures 6a-6d to at least disclose a broad class of TFTs with at least known ranges of relative proportions for the dimensions of the source, channel and drain regions of the transistor. Nevertheless, to the extent a</p>

Claim Language	Exemplary Citations in Hwang
	<p>POSITA, upon reviewing Hwang’s disclosure, would have remained unaware of suitable dimensions for the drive transistor, the POSITA would have been motivated to investigate known suitable dimensions in the art for transistors suitable for driving an LED device and been led to Godo’s disclosures of appropriate dimensions. Godo at [0150], [0161], [0163] (disclosing TFT 420 is a drive transistor), [0165] (disclosing TFT 420 drives LED element 430), [0199], [0201]; Figs. 1A-2B, 4A, 4B, 18A, 18B, 20A (with one set of dimensions) and 20B (another set of dimensions).</p> <p>A POSITA would have recognized that Godo’s Fig. 4B TFT design shares the most similarities with Hwang’s Fig. 6 TFT design: a single amorphous Si channel layer and a bottom gate electrode whose length in the channel direction is less than the length of the amorphous Si layer. Therefore, it would have been obvious to a POSITA to use Godo’s Fig. 4B dimensions, at least as a starting point, and potentially consider using Godo’s other disclosed dimensions as well. As will be demonstrated below, the resulting d1/L ratios for each of Godo’s disclosed TFTs meet the claimed range for limitation [1f]. Therefore, regardless of which set of TFT dimensions a POSITA uses from Godo to modify Hwang, limitation [1f] is still rendered obvious.</p> <p>A POSITA would have had a reasonable expectation of success in making the proposed combination because techniques such as photolithography for defining patterns for forming transistor elements with the disclosed dimensions were well known in the art. Patterning feature sizes that are in the micron (<math>\mu\text{m}</math>) resolution were well within the ordinary state of the art. Further, the relevant transistors disclosed in both Hwang and Godo are both bottom gate TFTs. Hwang at Figs. 6a-6d; Godo at Figs. 1A-2B, 4A-B. Thus, the only “modification” of Hwang is to supplement Hwang with the specific geometric dimensions taught in Godo to form Hwang’s lithography masks, then perform the same standard and routine TFT fabrication steps to thereby form a transistor with the dimensions as disclosed in Godo. The proposed combination would not have required undue experimentation and would have yielded the predictable result, namely, a drive transistor with the dimensions as disclosed in Godo. Once the drive TFT is formed, Hwang’s layer 162/162a with the shielding auxiliary electrode can be formed thereafter as taught by Hwang.</p>

Claim Language	Exemplary Citations in Hwang
	<p>Godo discloses the dimensions for the source, channel, and drain regions for TFTs suitable for driving an LED device. Godo at Figs. 20A, 20B; <i>see also id.</i>, [0150], [0161], [0199], [0201] (explaining the dimensions shown for Figs, 20A and 20B apply to the transistors of Figs. 1A-2B, 4A and 4B); Figs. 1A-2B, 4A, 4B, 18A, 18B. To the extent a POSITA, having reviewed Hwang's disclosure, required additional express guidance on suitable TFT dimensions, the POSITA would have been motivated to seek out those teachings in the art and it would have been obvious to use the TFT dimensions disclosed in Godo as explained above. As will be shown below, forming a drive transistor Td (using either Godo's Fig. 20A or Fig. 20B dimensions), and thereafter forming layer 162/162a that shields the source and channel regions of drive transistor Td would result in <math>0.3 \leq d1/L \leq 0.85</math> as required by this limitation.</p> <p>The TFT shown in Godo's Fig. 20A has a channel direction that runs left/right, and the length of source and drain regions along the channel direction are <math>7\mu\text{m}</math>. The length of the channel region is <math>10\mu\text{m}</math>.</p>



Claim Language	Exemplary Citations in Hwang									
	<p>necessarily bound the range of L. In particular, L must be less than 35<math>\mu\text{m}</math> (the length of the gate electrode), but also greater than the sum of the source<sup>3</sup>, channel and drain regions (7<math>\mu\text{m}</math> + 10<math>\mu\text{m}</math> + 7<math>\mu\text{m}</math> = 24<math>\mu\text{m}</math>), <i>i.e.</i>, 24<math>\mu\text{m}</math> <math>\leq</math> L <math>\leq</math> 35<math>\mu\text{m}</math>.</p> <p>As for the d1 dimension, as discussed above, Hwang's layer 162/162a has overlap length d1 that shields at least the source and channel regions. Thus, applying Godo's dimensions, the minimum value for d1 is 17<math>\mu\text{m}</math> (the sum of source region and channel region lengths). Further, based on the teachings of Hwang that the drain electrode should not be shielded by layer 162/162a, the maximum value for d1 would be the entire channel layer <u>except</u> for the drain, <i>i.e.</i>, d1 <math>\leq</math> L - 7<math>\mu\text{m}</math>.</p> <table border="1" data-bbox="940 654 1654 865"> <thead> <tr> <th></th> <th>d1 (<math>\mu\text{m}</math>)</th> <th>L (<math>\mu\text{m}</math>)</th> </tr> </thead> <tbody> <tr> <td>Minimum</td> <td>17</td> <td>24</td> </tr> <tr> <td>Maximum</td> <td>L-7</td> <td>35</td> </tr> </tbody> </table> <p>Based on these allowable ranges for d1 and L, the allowable range of d1/L can be determined. The minimum value for the fraction d1/L is achieved when the numerator d1 is minimized and the denominator L is maximized, <i>i.e.</i>, d1<sub>min</sub>/L<sub>max</sub> is 17<math>\mu\text{m}</math>/35<math>\mu\text{m}</math> = 0.48. To maximize d1/L, the maximum value for d1 is L-7<math>\mu\text{m}</math> as shown above. Substituting, the ratio d1<sub>max</sub>/L = (L-7<math>\mu\text{m}</math>)/L = 1-7/L. Thus, d1/L is maximized when 7/L is minimized, <i>i.e.</i>, when L is maximized where L = 35<math>\mu\text{m}</math>. Thus, the maximum d1/L ratio is 1-7/35 = 1-0.2 = 0.8. Accordingly, using Godo's dimensions as disclosed in Fig. 20A, the resulting d1/L must be between 0.48 <math>\leq</math> d1/L <math>\leq</math> 0.8, wholly within the range as claimed in [1f]. Stated differently, applying Hwang's teachings regarding</p>		d1 ( $\mu\text{m}$ )	L ( $\mu\text{m}$ )	Minimum	17	24	Maximum	L-7	35
	d1 ( $\mu\text{m}$ )	L ( $\mu\text{m}$ )								
Minimum	17	24								
Maximum	L-7	35								

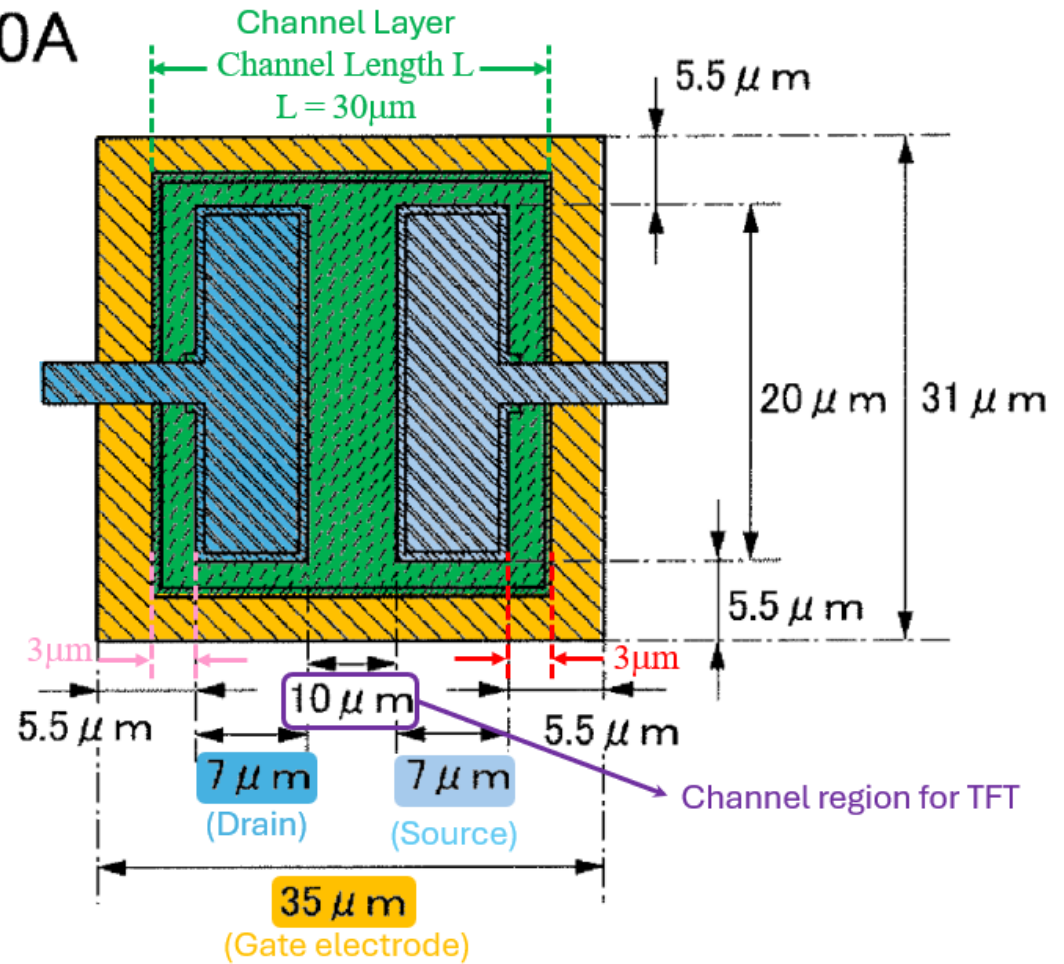
<sup>3</sup> This calculation includes only the lengths for the source region, channel region and drain region as disclosed in Godo because it seeks the lower bound for L. In other words, for a transistor to be consistent with the Godo disclosure, the length L must be large enough to accommodate the three expressly disclosed lengths, which is 24 $\mu\text{m}$ .

Claim Language	Exemplary Citations in Hwang
	<p>shielding layer 162/162a on any transistor that is sized consistent with the express dimensions disclosed in Godo's Fig. 20A will necessarily result in <math>d1/L</math> between <math>0.48 \leq d1/L \leq 0.8</math>.</p> <p>An illustrative example of a TFT layout consistent with the dimensions of Godo's Fig. 20A is provided below, where the exemplary layout has mirror symmetry about the center of the channel region, and where L is <math>30\mu\text{m}</math> (which is near the middle of the allowed range).</p>

Claim Language

Exemplary Citations in Hwang

FIG. 20A



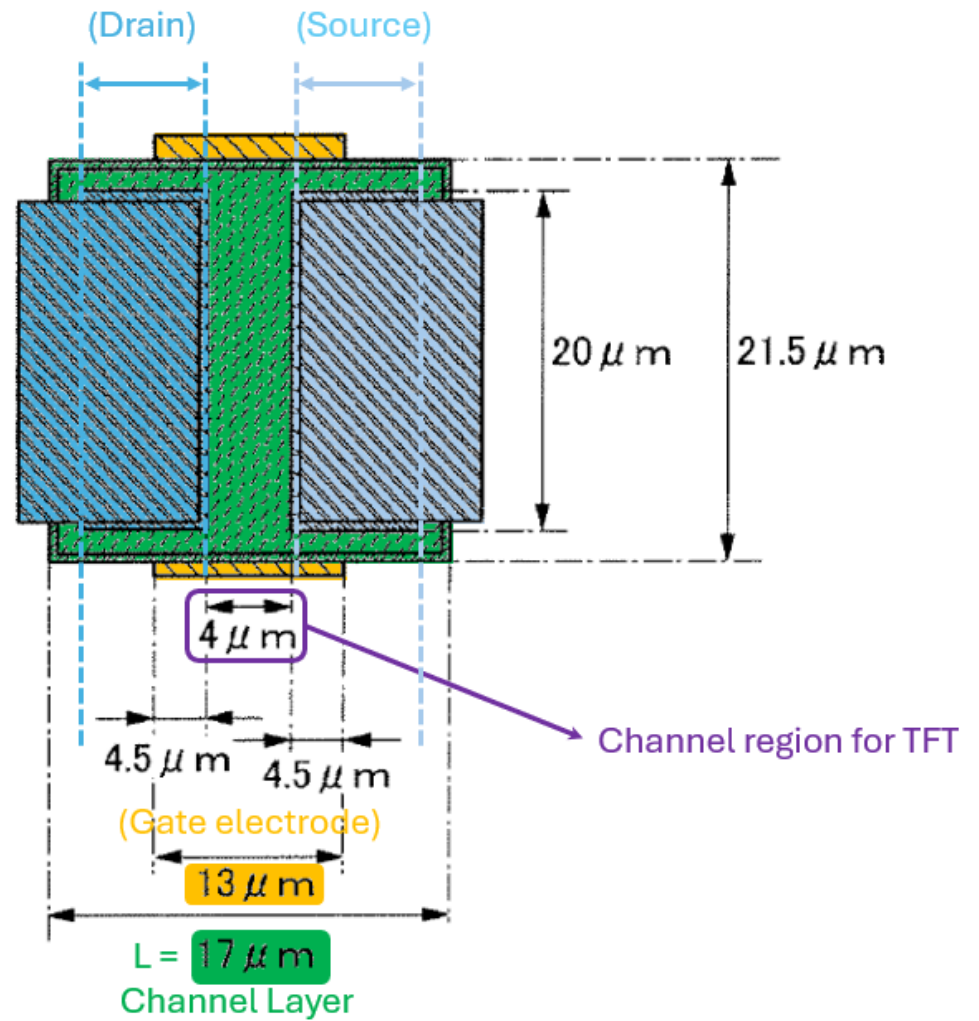
Godo at Fig. 20A (annotations added). Mirror symmetry means the length between the right-edge of the source region to the right-edge of the (green) channel layer is 3 μm (*i.e.*, the length between the two dotted red lines), which is also the length between the left-edge of the drain region to the

Claim Language	Exemplary Citations in Hwang
	<p>left-edge of the channel layer (<i>i.e.</i>, the length between the two dotted pink lines). Hwang discloses that shielding layer 162/162a would extend from the right-edge of channel layer, covering the source region and the channel region and stopping at the drain region. This means <math>d1 = 3\mu\text{m} + 7\mu\text{m} + 10\mu\text{m} = 20\mu\text{m}</math>, while <math>L = 30\mu\text{m}</math>. This leads to an illustrative value of <math>d1/L</math> of 0.67, which falls within the claimed range. Of course, this is but one illustrative example, whereas the more general analysis shows that any TFT with dimensions consistent with Godo's Fig 20A necessarily result in a <math>d1/L</math> within the claimed range.</p> <p>The TFT shown in Godo's Fig. 20B has a channel direction that runs left-right, and the length of the channel layer is <math>17\mu\text{m}</math>.</p>

Claim Language

Exemplary Citations in Hwang

FIG. 20B



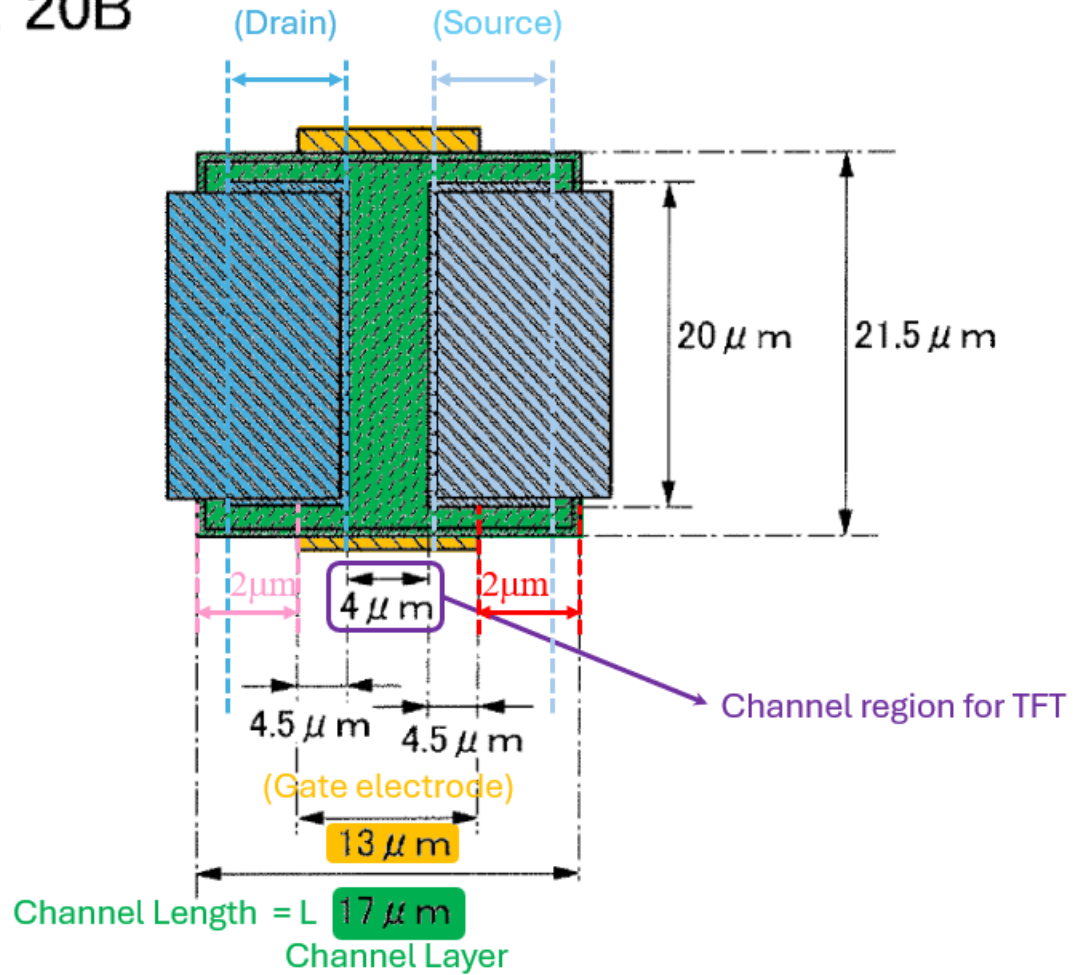
Claim Language	Exemplary Citations in Hwang									
	<p>Godo at Fig. 20B (annotations added). The channel region has length <math>4\mu\text{m}</math>, but the exact lengths of the source/drain regions are not expressly disclosed, only that they are at least <math>4.5\mu\text{m}</math>. The maximum source/drain length can be determined because the sum of the lengths of the source, channel and drain regions cannot exceed the channel layer length of <math>17\mu\text{m}</math>. Thus, the maximum length for the source region is <math>8.5\mu\text{m}</math> (taking the length of drain at the minimum <math>4.5\mu\text{m}</math>), and the maximum length for the drain is <math>8.5\mu\text{m}</math> (minimizing the source).</p> <p>As for the <math>d1</math> dimension, as discussed above, Hwang's layer 162/162a has overlap length <math>d1</math> that shields at least the source and channel regions. Thus, applying Godo's Fig. 20B dimensions, the minimum value for <math>d1</math> is <math>8.5\mu\text{m}</math> (the sum of channel region length and the minimum source region length). Further, based on the teachings of Hwang that the drain electrode should not be shielded by layer 162/162a, the maximum value for <math>d1</math> would be the entire channel layer <u>except</u> for the drain length (which should be minimized), <i>i.e.</i>, <math>d1 \leq 17 - 4.5\mu\text{m}</math>.</p> <table border="1" data-bbox="940 805 1654 1016"> <thead> <tr> <th></th> <th><math>d1</math> (<math>\mu\text{m}</math>)</th> <th><math>L</math> (<math>\mu\text{m}</math>)</th> </tr> </thead> <tbody> <tr> <td>Minimum</td> <td>8.5</td> <td>17</td> </tr> <tr> <td>Maximum</td> <td>12.5</td> <td>17</td> </tr> </tbody> </table> <p>Based on these allowable <math>d1</math> values and the disclosed <math>L</math> dimension, the ratio <math>d1/L</math> must be between <math>8.5/17</math> and <math>12.5/17</math>, or <math>0.5 \leq d1/L \leq 0.735</math>, wholly within the range as claimed in [1f]. Stated differently, applying Hwang's teachings regarding shielding layer 162/162a on any transistor that is sized consistent with the express dimensions disclosed in Godo's Fig. 20B will necessarily result in <math>d1/L</math> between <math>0.5 \leq d1/L \leq 0.735</math>.</p>		$d1$ ( $\mu\text{m}$ )	$L$ ( $\mu\text{m}$ )	Minimum	8.5	17	Maximum	12.5	17
	$d1$ ( $\mu\text{m}$ )	$L$ ( $\mu\text{m}$ )								
Minimum	8.5	17								
Maximum	12.5	17								

<b>Claim Language</b>	<b>Exemplary Citations in Hwang</b>
	An illustrative example of a TFT layout consistent with the dimensions of Godo's Fig. 20B is provided below, where the exemplary layout has mirror symmetry about the center of the channel region.

Claim Language

Exemplary Citations in Hwang

FIG. 20B



Godo at Fig. 20A (annotations added). Mirror symmetry means the length between the right-edge of the gate electrode to the right-edge of the (green) channel layer is 2 $\mu\text{m}$  (*i.e.*, the length

Claim Language	Exemplary Citations in Hwang
	<p>between the two dotted red lines), which is also the length between the left-edge of the gate electrode to the left-edge of the channel layer (<i>i.e.</i>, the length between the two dotted pink lines). Hwang discloses that shielding layer 162/162a would extend from the right-edge of channel layer, covering the source region and the channel region and stop at the drain region. This means <math>d1 = 2\mu\text{m} + 4.5\mu\text{m} + 4\mu\text{m} = 10.5\mu\text{m}</math>, while <math>L = 17\mu\text{m}</math>. This leads to an illustrative value of <math>d1/L</math> of 0.62, which falls within the claimed range. Of course, this is but one illustrative example, whereas the more general analysis shows that any TFT with dimensions consistent with Godo's Fig 20B necessarily result in a <math>d1/L</math> within the claimed range.</p> <p>Accordingly, Hwang in combination with Godo discloses the <math>d1/L</math> dimensional ratio limitation recited in [1f], and thus renders obvious claim 1.</p> <p>Additionally or alternatively, adding Yamashita to the combination of Hwang and Godo would have required no modification to Hwang's layer 162/162a other than the designer intend that layer 162/162a perform the light-shielding function. Thus, a POSITA would have been motivated to combine Hwang, Godo and Yamashita, and would have had a reasonable expectation of success for the same reasons set forth above.</p> <p>See also citations to this limitation in Ex. D-3 (Masumitsu).</p>
<p>[17] The semiconductor structure as claimed in claim 1, wherein the conductive light-shielding pattern layer and the drain electrode are spaced by a distance along the channel direction in the vertical projection.</p>	<p>Hwang discloses, or at least renders obvious, "the semiconductor structure as claimed in claim 1 (<i>see</i> claim 1), wherein the <b>conductive light-shielding pattern layer (162/162a)</b>, and the <b>drain electrode (154)</b> are spaced by a distance along the channel direction in the vertical projection."</p> <p>Hwang teaches layer 162/162a should cover the channel region and not overlap the drain electrode 154. Hwang at [0048]. As illustrated in Figure 6d, Hwang teaches that in the vertical projection, there may be very little space between the end of the drain electrode 154 and electrode 162a. Hwang at Fig. 6d. To the extent Figure 6d does not expressly disclose electrode 162a and drain electrode 154 are "spaced by a distance in the vertical projection," Hwang also teaches that, while electrode 162a covers the channel region to block the influence of electrode 170, it could be shortened, depending on need. Hwang at [0050] ("auxiliary electrode 162a. . .</p>

Claim Language	Exemplary Citations in Hwang
	<p>does not overlap the second drain electrode 154. The auxiliary electrode 162a may be ... shorter... upon need.”). One exemplary need disclosed by Hwang is to prevent short circuit between the auxiliary electrode 162a and the drain electrode 154. Hwang at [0050]. Thus, Hwang teaches that electrode 162a (which still should cover the channel region to block the influence of electrode 170) can be shortened (<i>i.e.</i>, spaced apart in the vertical projection) by a small amount to account for fabrication variances in order to mitigate a potential short circuit to the drain electrode. Because this claim does not require a particular minimum amount of distance for the “spaced apart” limitation, Hwang’s wholistic teaching that electrode 162a covers the channel, does not overlap the second drain electrode and can, in fact, be even shorter expressly discloses this claim to a POSITA.</p> <p>Additionally or alternatively, claim 17 is obvious in view of Hwang. A POSITA would have understood that Hwang’s teaching in paragraph [0050] related to shortening electrode 162a would not expose the entire channel region entirely, but only to shorten electrode 162a to the extent needed. This is because the disclosed function of the auxiliary electrode 162a is to shield the channel region from the electric potential at the cathode 170. Indeed, this shielding of the channel region from the cathode voltage specifically solves the problem that Hwang’s invention sought to overcome. Hwang at [0016]. Specifically, shielding the channel region overcomes the problems of brightness deterioration and non-uniformity. Hwang at [0072]; <i>see also id.</i>, [0069]-[0074] and Fig. 5. Therefore, a POSITA would have understood that shielding the channel region remains important, even though there may be other design tradeoffs that need to be considered.</p> <p>For example, as disclosed in Hwang, increasing the spacing would help prevent an unintentional short circuit between auxiliary electrode 162a (which is electrically connected to and thus on the same node as the source electrode) and the drain electrode 154. Hwang at [0050], [0066]. Additionally or alternatively, a POSITA would have recognized that unintended parasitic capacitance between the source and drain has an adverse impact on the transistor performance. Streetman at 323. Thus, a POSITA would have been motivated to mitigate unintended capacitive coupling to the drain electrode 154 by increasing the spacing (in the vertical projection) between</p>

Claim Language	Exemplary Citations in Hwang
	<p>electrode 162a and drain electrode 154 for a given dielectric material 160 to increase the distance therebetween, thereby reducing the resulting capacitance. Schaum at 153-154.</p> <p>A POSITA would have recognized that even though electrode 170 is electrically connected to drain electrode 154, capacitive coupling between electrode 162a and electrode 170 can be mitigated by increasing the properties (<i>e.g.</i>, thickness and/or dielectric constant) of dielectric layer 164. However, this does not fully resolve the potential capacitive coupling to the drain electrode, thus potentially requiring additional spacing between electrode 162a and drain electrode 154 (as expressly taught by Hwang). Thus, the extent of the overlap of electrode 162a with the channel region requires a tradeoff between mitigating unintentional short circuits and/or the capacitive coupling to the drain and shielding the effects of the cathode on the channel region. Any decrease in the overlap length would necessarily cause electrode 162a and drain electrode 154 to be spaced by a distance along the channel direction in the vertical projection.</p> <p>As for quantifying the decrease in electrode 162a, a POSITA would have recognized from the teachings of Hwang that the primary emphasis remains to provide as much shielding to the channel region as possible in order to reap the benefits of the Hwang invention. Hwang at [0069]-[0074]; Fig. 5. Therefore, this would have suggested to a POSITA that at least half of the channel region should remain shielded (if not more) in balancing these other considerations while still preserving the main teachings in Hwang for improving performance by shielding the channel region. This results in a minimum <math>d1/L</math> ratio of 0.5 with no change to the maximum <math>d1/L</math> ratio (0.67), which remains within the range claimed in [1f].</p> <p>Alternatively, claim 17 is rendered obvious in view of Hwang and Godo, or Hwang and Yamashita, or Hwang and Yamashita and Godo, or Hwang in view of the references as cited in claims and 17 with the knowledge of POSITA. The antecedent basis for the conductive light-shielding pattern layer recited therein comes from limitation [1f]. Therefore, layer 162/162a meets the limitations recited in this claim for at least the same reasons set forth above for [1f]. Further, regarding the “spaced by a distance...” limitation, Hwang teaches that depending on need, some designs may shorten electrode 162a thus leading to the conductive light-shielding pattern layer and the drain electrode to be spaced by a distance along the channel direction in the</p>

Claim Language	Exemplary Citations in Hwang									
	<p>vertical projection. As discussed above, a POSITA would have applied Hwang's teachings about shortening electrode 162a in Hwang's paragraph [0050] (based on balancing different needs of a particular design) such that more than half of the channel region remains shielded.</p> <p>Shortening electrode 162a would decrease the d1 parameter and thereby reduce the d1/L ratio. Therefore, the upper bound for d1/L will still remain within the claimed range for [1f]. To investigate the impact of the modification on the lower bound of d1/L, the relative proportions of the transistor dimensions as disclosed in Godo's Fig. 20A can be used, and then auxiliary electrode 162a shortened as set forth above (<i>i.e.</i>, shielding half of the channel region). Thus, the minimum overlap length d1 is equal to the sum of the length of the source region (7μm) and half the length of the channel region (5μm), or 12μm. The allowable range for length L is unchanged (with a range between 24μm and 35μm), leading to <math>0.34 \leq d1/L \leq 0.5</math>, which remains within the claimed range of [1f].</p> <p>Using the relative proportions of the transistor dimensions as disclosed in Godo's Fig. 20B and shortening electrode 162a as set forth above, the overlap length d1 is decreased by half of the length of the channel region, <i>i.e.</i>, 2μm.</p> <table border="1" data-bbox="884 938 1709 1149"> <thead> <tr> <th></th> <th>Revised d1 (μm)</th> <th>L (μm)</th> </tr> </thead> <tbody> <tr> <td>Minimum</td> <td><math>8.5 - 2 = 6.5</math></td> <td>17</td> </tr> <tr> <td>Maximum</td> <td><math>12.5 - 2 = 10.5</math></td> <td>17</td> </tr> </tbody> </table> <p>This leads to a ratio of d1/L such that <math>0.38 \leq d1/L \leq 0.62</math>, which remains within the claimed range of [1f].</p> <p>Therefore, by configuring the conductive light-shielding pattern layer and the drain electrode such that they are spaced apart by a distance along the channel direction in a vertical projection,</p>		Revised d1 (μm)	L (μm)	Minimum	$8.5 - 2 = 6.5$	17	Maximum	$12.5 - 2 = 10.5$	17
	Revised d1 (μm)	L (μm)								
Minimum	$8.5 - 2 = 6.5$	17								
Maximum	$12.5 - 2 = 10.5$	17								

Claim Language	Exemplary Citations in Hwang
	<p>the d1/L ratio will decrease (compared to if the entire channel region is shielded), but the resulting d1/L ratio still lies within the range as recited in claim 1 from which claim 17 depends.</p> <p>See also citations to this limitation in Ex. D-3 (Masumitsu).</p>