UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No.: IPR2025-00119
U.S. Patent No. 10,879,254
Issue Date: December 29, 2020

Title: THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 10,879,254 PURSUANT TO 35 U.S.C. §§311-319 and 37 C.F.R. §42

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1023	U.S. Patent Publ. No. 2019/0081061 A1 to Tessariol et al. ("Tessariol")
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1025	Hwang, "Atomic Layer Deposition for Semiconductors," Springer (2014) ("Hwang")
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1037	Weste, "Principles of CMOS VLSI Design," Addison-Wesley (1993) ("Weste")
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1042	Wolf, "Silicon Processing for the VLSI Era, Volume 1-Process Technology," Lattice Press (1986) ("Wolf Vol. 1")
1043	Wolf, "Silicon Processing for the VLSI Era, Volume 1-Process Integration," Lattice Press (1990) ("Wolf Vol. 2")
1044	U.S. Patent No. 10,714,341 to Cohen et al.

LISTING OF CHALLENGED CLAIMS

Ref. #	Listing of Challenged Claims
Claim 1:	
[1.PRE]	A method for forming a three-dimensional (3D) memory device, comprising:
[1.A]	forming a stack comprising a plurality of dielectric/sacrificial layer pairs on a substrate;
[1.B]	forming a channel structure extending vertically through the stack;
[1.C]	forming a first opening extending vertically through the stack;
[1.D]	forming a spacer on a sidewall of the first opening;
[1.E]	forming a through array contact (TAC) extending vertically through the stack by depositing a conductor layer over the spacer in the first opening; and
[1.F]	after forming the TAC, forming a slit extending vertically through the stack.
Claim 2:	
[2]	The method of claim 1, further comprising prior to forming the first opening, forming a dummy channel structure extending vertically through the stack.
Claim 3:	
[3]	The method of claim 1, wherein forming the first opening comprises simultaneously etching the first opening through the stack and a second opening outside of the stack.
Claim 4:	
[4]	The method of claim 3, wherein forming the TAC comprises depositing the conductor layer in the first opening to form the TAC and in the second opening to form a peripheral contact.

Ref. #	Listing of Challenged Claims
Claim 5:	
[5.PRE]	The method of claim 1, wherein forming the spacer on the sidewall of the first opening comprises:
[5.A]	depositing a dielectric layer on the sidewall and a bottom surface of the first opening; and
[5.B]	removing part of the dielectric layer that is deposited on the bottom surface of the first opening.
Claim 6:	
[6]	The method of claim 5, wherein the deposition of the dielectric layer comprises atomic layer deposition (ALD), and the removal of the part of the dielectric layer comprises anisotropic etching on the bottom surface of the first opening.
Claim 7:	
[7.PRE]	The method of claim 1, wherein forming the spacer on the sidewall of the first opening comprises:
[7.A]	forming a plurality of shallow recesses by removing parts of the sacrificial layers abutting the sidewall of the first opening;
[7.B]	depositing a dielectric layer filling in the shallow recesses and on the sidewall and a bottom surface of the first opening; and
[7.C]	removing part of the dielectric layer that is deposited on the bottom surface of the first opening.
Claim 8:	
[8]	The method of claim 7, wherein the removal of the part of the dielectric layer comprises isotropic etching on the sidewall and the bottom surface of the first opening.

Ref. #	Listing of Challenged Claims
Claim 9:	
[9.PRE]	The method of claim 1, wherein forming the first opening comprises:
[9.A]	simultaneously etching the first opening through the stack, a second opening outside of the stack, and a third opening through the stack,
[9.B]	wherein a lateral dimension of the third opening is smaller than lateral dimensions of the first and second openings.
Claim 10:	
[10.PRE]	The method of claim 9, wherein forming the spacer on the sidewall of the first opening comprises:
[10.A]	depositing a dielectric layer (i) fully filling in the third opening to form a dummy channel structure and (ii) partially filling in the first opening and the second opening; and
[10.B]	removing parts of the dielectric layer that are deposited on a bottom surface of the first opening and on a bottom surface of the second opening.
Claim 11:	
[11.PRE]	A method for forming a three-dimensional (3D) memory device, comprising:
[11.A]	forming a stack comprising a plurality of dielectric/sacrificial layer pairs on a substrate;
[11.B]	forming a channel structure extending vertically through the stack;
[11.C]	forming a dummy channel structure extending vertically through the stack;
[11.D]	simultaneously etching a first opening through the stack and a second opening outside of the stack;

Ref. #	Listing of Challenged Claims
[11.E]	simultaneously forming a first spacer on a sidewall of the first opening and a second spacer on a sidewall of the second opening;
[11.F]	depositing a conductor layer (i) filling in the first opening to form a through array contact (TAC) and (ii) filling in the second opening to form a peripheral contact; and
[11.G]	after forming the TAC and peripheral contact, forming a slit extending vertically through the stack.
Claim 12:	
[12.PRE]	The method of claim 11, wherein forming the first spacer on the sidewall of the first opening comprises:
[12.A]	depositing a dielectric layer on the sidewall and a bottom surface of the first opening; and
[12.B]	removing part of the dielectric layer that is deposited on the bottom surface of the first opening.
Claim 13:	
[13]	The method of claim 12, wherein the deposition of the dielectric layer comprises atomic layer deposition (ALD), and the removal of the part of the dielectric layer comprises anisotropic etching on the bottom surface of the first opening.
Claim 14:	
[14.PRE]	The method of claim 11, wherein forming the first spacer on the sidewall of the first opening comprises:
[14.A]	forming a plurality of shallow recesses by removing parts of the sacrificial layers abutting the sidewall of the first opening;
[14.B]	depositing a dielectric layer filling in the shallow recesses and on the sidewall and a bottom surface of the first opening; and

Ref. #	Listing of Challenged Claims
[14.C]	removing part of the dielectric layer that is deposited on the bottom surface of the first opening.
Claim 15:	
[15]	The method of claim 14, wherein the removal of the part of the dielectric layer comprises isotropic etching on the sidewall and the bottom surface of the first opening.
Claim 17:	
[17]	The method of claim 11, wherein the dielectric layers in the dielectric/sacrificial layer pairs comprise silicon oxide, the sacrificial layers in the dielectric/sacrificial layer pairs comprise silicon nitride, and the first and second spacers comprise silicon oxide.
Claim 18:	
[18.PRE]	A method for forming a three-dimensional (3D) memory device, comprising:
[18.A]	forming a stack comprising a plurality of dielectric/sacrificial layer pairs on a substrate;
[18.B]	forming a channel structure extending vertically through the stack;
[18.C]	simultaneously etching a first opening through the stack, a second opening outside of the stack, and a third opening through the stack, wherein a lateral dimension of the third opening is smaller than lateral dimensions of the first and second openings;
[18.D]	depositing a dielectric layer (i) fully filling in the third opening to form a dummy channel structure and (ii) partially filling in the first opening and the second opening;
[18.E]	removing parts of the dielectric layer that are deposited on a bottom surface of the first opening and on a bottom surface of the second opening;

Ref. #	Listing of Challenged Claims
[18.F]	depositing a conductor layer (i) filling in the first opening to form a through array contact (TAC) and (ii) filling in the second opening to form a peripheral contact; and
[18.G]	after forming the TAC and peripheral contact, forming a slit extending vertically through the stack.
Claim 20:	
[20]	The method of claim 18, further comprising prior to etching the first, second, and third openings, forming a staircase structure at one side of the stack.

I. INTRODUCTION

Petitioner Micron Technology, Inc. ("Petitioner") respectfully requests *inter partes* review of claims 1-15, 17-18, and 20 (the "Challenged Claims") of U.S. Patent No. 10,879,254 (Ex. 1001, the "'254 Patent") assigned to Yangtze Memory Technologies Co., Ltd. ("YMTC", "Patent Owner" or "PO").

The '254 Patent relates to three-dimensional (3D) memory devices with "through array contacts" ("TACs"). The '254 Patent alleges that there are issues with forming TACs through a "barrier structure." Ex. 1001, 4:55-5:20. The figure below depicts such a barrier structure, i.e., a large oxide rectangular block (232):

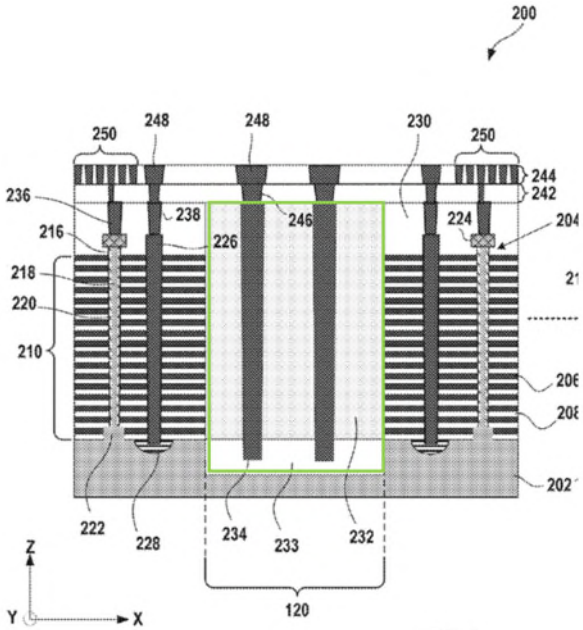


FIG. 2

Ex. 1007 (U.S. Pat. 10,658,378), Fig. 2 (partial) (annotated)[1]. Instead of using a barrier structure, the '254 Patent teaches employing a thin spacer (138) to isolate each TAC.

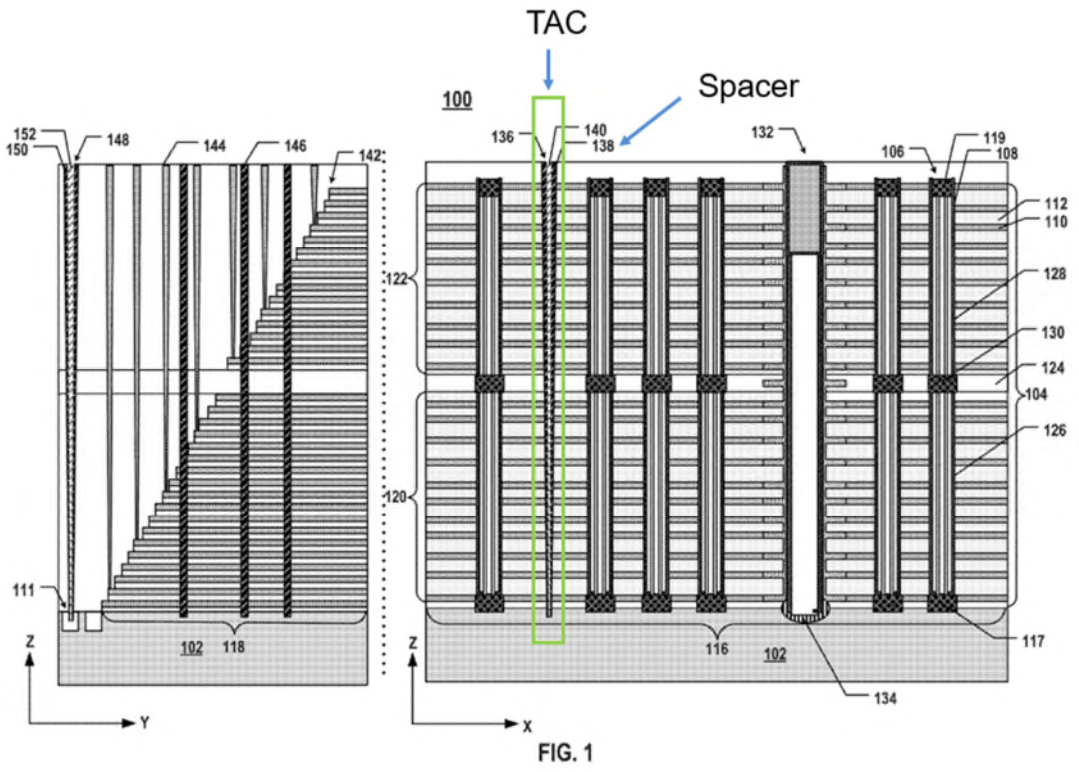


FIG. 1

Ex. 1001, Abstract, 4:55-5:20, Fig. 1. In addition, the '254 Patent teaches forming a slit (element 132 above)—a structure that was textbook material when the application leading to the '254 patent was filed—***after*** forming the TAC. The slit extends in the y-direction (into the page or screen) and can separate the array into blocks.

[1] Annotations added throughout unless noted.

Claim 1 is representative. It recites forming a stack of alternating dielectric and sacrificial gates—a basic building block of 3D NAND devices. It then recites the basic manufacturing steps of forming a TAC: (1) forming an opening, (2) forming a spacer on the sidewall, and (3) forming the TAC by filling the remaining hole with conductive material. Finally, after forming the TAC, it recites forming a slit. The file history includes no substantive Office Actions. But the Notice of Allowance suggests this final temporal requirement was the alleged point of novelty. *See* §VI.

The Petition demonstrates that TACs with a spacer were, in fact, well known in the prior art. What's more, it was known to form slits ***after*** forming such TACs. The Petition relies on one primary reference: Fujiki. Fujiki was not before the Examiner during prosecution.

Just like the '254 Patent, Fujiki discloses TACs (94) that do not extend through a barrier structure:

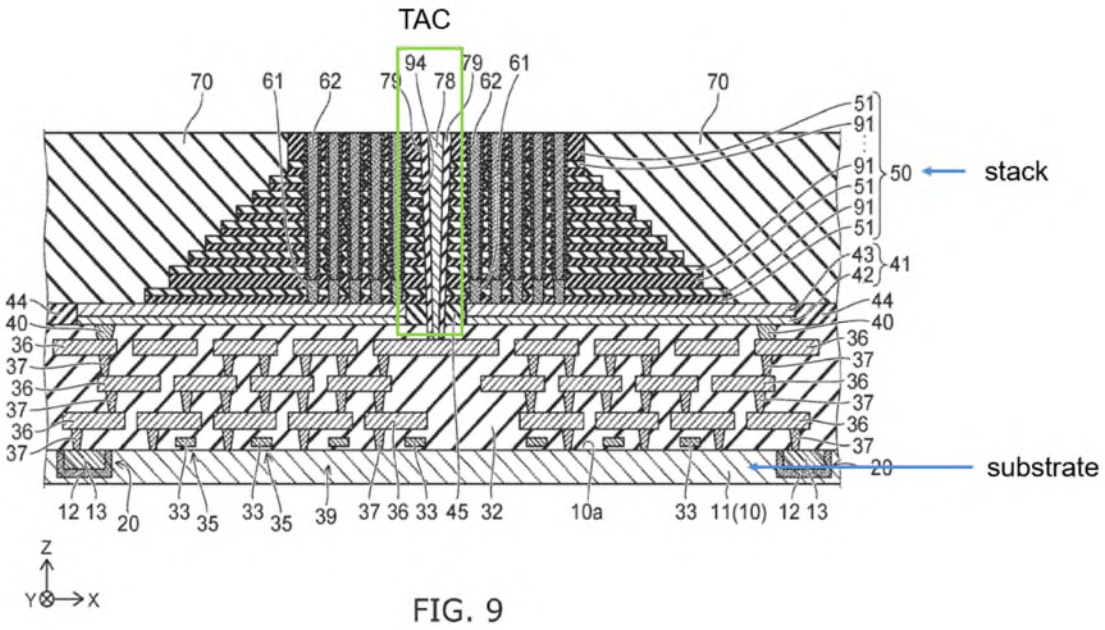


FIG. 9

Ex. 1006 ("Fujiki"), Fig. 9 (annotated). And Fujiki discloses the exact same steps to form the TAC: "a through-via hole 94 is formed to pierce the stacked body 50 . . . . Then, the insulating film 79 is formed on the inner surface of the through-via hole 94; and the through-via 78 is formed on the inner surface of the insulating film 79." *Id.*, [0053].

What's more, after forming the TAC as shown in Figure 9, Fujiki discloses "[c]ontinuing as shown in FIG. 10 and FIG. 3, . . . ***slits 96 are formed to pierce the stacked body 50***." Fujiki, [0054].[2]

The dependent claims simply recite (1) additional basic, well-known 3D NAND structures, e.g., dummy channels, and (2) additional basic, well-known 3D

[2] Emphasis added unless otherwise noted.

NAND manufacturing steps, e.g., forming two holes at once and atomic-layer deposition. Some of these features are taught by Fujiki, while the rest were well within the knowledge of a POSITA.

Petitioner requests that the Board institute trial and find the Challenged Claims unpatentable under §103.

II. MANDATORY NOTICES

A. Real Party-in-Interest

Petitioner Micron Technology, Inc. and its subsidiaries, including Micron Consumer Products Group LLC, are the real parties-in-interest.

B. Related Matters

According to USPTO assignment records, the ’254 Patent is currently assigned to YMTC. On July 12, 2024, YMTC asserted the ’254 Patent and U.S. Patent Nos. 10,672,711, 10,879,164, 10,886,291, 11,101,276, 11,145,666, 11,450,604, 11,482,532, 11,568,941, 11,581,322, and 12,010,838 against Micron (the “YMTC2 case”). On August 21, 2024, the YMTC2 case was consolidated with *Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC*, Case No. 3:23-cv-05792-RFL (N.D. Cal., filed November 9, 2023) (“Co-Pending Litigation”).

In addition to this Petition, Petitioner is filing (or has filed) petitions for *inter partes* review of each asserted patent in the Co-Pending Litigation:

Patent	PTAB Proceeding	Wave
10,658,378 (claims 15-17 and 19-20)	IPR2024-00788	Wave 1 Petitions
10,861,872 (claims 1-6 and 11-13)	IPR2024-00789	
10,868,031	IPR2024-00790	
10,937,806 (claims 8-9 and 11-12)	IPR2024-00791	
10,950,623	IPR2024-00794	
11,468,957	IPR2024-00792	
11,501,822	IPR2024-00795	
11,600,342 (claims 1-6 and 8-20)	IPR2024-00793	
10,658,378 (claims 1-7 & 18)	IPR2024-00909	Wave 2 Petitions
10,861,872 (claims 7-10)	IPR2024-00910	
10,937,806 (claim 10)	IPR2024-00911	
11,600,342 (claim 7)	IPR2024-00912	
10,672,711	IPR2025-00117	Wave 3 Petitions
10,879,164	IPR2025-00118	
10,879,254	IPR2025-00034	
10,886,291	IPR2025-TBD	
11,101,276	IPR2025-TBD	
11,145,666	IPR2025-TBD	
11,450,604	IPR2025-00035	
11,482,532	IPR2025-TBD	
11,568,941	IPR2025-TBD	

Patent	PTAB Proceeding	Wave
11,581,322	IPR2025-TBD	
12,010,838	IPR2025-TBD	

Micron filed a first Petition challenging all 18 of the Challenged Claims, advancing a single ground (Nakajima). IPR2025-00034. Concurrently filed herewith, Micron's Explanation for and Ranking of Two Petitions explains the basis for filing this second Petition, which also advances a single ground (Fujiki) against all 18 of the Challenged Claims.

The Director and the Board should allow this Petition under 35 U.S.C. §314(a), 35 U.S.C. §325(d), and/or 37 C.F.R. §42.108(a).

C. Counsel, Service, and Fee Information

Petitioner designates the following counsel:

Lead Counsel	**Back-Up Counsel**
Jeremy Jason Lang Registration No. 73,604 (jlang@orrick.com) Postal & Hand-Delivery Address: Orrick, Herrington & Sutcliffe LLP 1000 Marsh Road Menlo Park, CA 94025-1015 T: 650-614-7400; F: 650-614-7401	Thomas James Registration No. 74,109 (tjames@orrick.com) Postal & Hand-Delivery Address: Orrick, Herrington & Sutcliffe LLP 353 N Clark Street Suite 3600 Chicago, IL 60654 T: 312-924-9800 F: 312-924-9899 Jared Bobrow *Pro Hac Vice* to be submitted (jbobrow@orrick.com) Postal & Hand-Delivery Address: Orrick, Herrington & Sutcliffe LLP 1000 Marsh Road Menlo Park, CA 94025-1015 T: 650-614-7400; F: 650-614-7401

Petitioner consents to service by electronic mail at the following addresses: PTABDocketJJL2@orrick.com, PTABDocketT6J1@orrick.com, PTABDocketJ3B3@orrick.com, and Micron-YMTC_ohs@orrick.com. Pursuant to 37 C.F.R. §42.10(b), Petitioner's Power of Attorney is attached.

The USPTO is authorized to charge the fee specified by 37 C.F.R. §42.15(a), and any other required fees, to Deposit Account No. 15-0665.

III. REQUIREMENTS FOR *INTER PARTES* REVIEW

A. Grounds for Standing

Petitioner certifies that the '254 Patent is available for IPR, and that Petitioner is not barred or estopped from requesting this IPR. Petitioner was served with a complaint alleging infringement of the '254 Patent on July 12, 2024. This Petition was filed within 1 year of this date.

B. Identification of Challenge and Statement of Precise Relief Requested

This Petition assumes that the '254 Patent is entitled to its earliest-listed priority date: August 21, 2018. Ex. 1001, 2.

This Petition advances U.S. Patent Publication 2019/0198524 ("Fujiki") (Ex. 1006) as the primary reference. Fujiki was filed on September 12, 2018, and claims priority to JP 2017-247987 (Exs. 1039-40), which was filed on December 25, 2017. Fujiki, Cover. Section IX.B demonstrates that Fujiki was effectively filed on December 25, 2017. Fujiki is thus prior art under at least AIA §102(a)(2).

Ground	Claim(s)	Prior Art Asserted
1	1-15, 17-18, and 20	Obvious under §103 based on Fujiki and the knowledge of a POSITA

IV. INSTITUTION SHOULD BE GRANTED

Petitioner has established a reasonable likelihood of success on the merits. All other requirements for IPR have been met. The Board should institute IPR.

A. There are No Grounds for a §314 Discretionary Denial in this Case

There is a pending district court action involving the '254 Patent. The PTAB has explained that it "will not … discretionarily deny institution in view of parallel district court litigation where a petition presents compelling evidence of unpatentability." 6/21/22 Interim Procedure, 2, 4-5. Petitioner submits that it presents a compelling case here: the claims of the '254 Patent are unambiguously unpatentable.

Petitioner also notes that the factors considered by the Board when assessing whether to institute IPR in light of a parallel proceeding collectively weigh in favor of institution. *See Apple Inc. v. Fintiv, Inc.*, Case No. IPR2020-00019, Paper No. 11 (Mar. 20, 2020) (precedential). In particular: the district court may stay the case, if any potential trial will occur years from now, little district court work has occurred, petitioner diligently prepared this petition, and the petition is substantively strong.

1. Possibility of a Stay

Petitioner intends to seek a stay if the Board institutes IPR. Until this issue is adjudicated, any attempt to predict the outcome would require speculation. This factor is neutral. *See Sand Revolution II, LLC v. Continental Intermodal Grp. – Trucking LLC*, IPR2019-01393, Paper 24, 7 (PTAB June 16, 2020) (informative); *Fintiv*, 6-9, 12 (similar).

2. Proximity of the Court's Trial Date

On September 18, 2024, the district court entered a scheduling order which set a trial date of June 15, 2026. *See* Ex. 1033. As a result, if IPR proceedings are instituted, they should be completed before the scheduled trial date. *See also* Ex. 1034 (statistics indicating that it takes on average 48.9 months to reach trial in district court). This weighs strongly in favor of institution.

3. Investment in the Parallel Proceeding

Regarding the Co-Pending Litigation, to date, the parties and the district court have invested very little in the parallel proceeding. Indeed, beyond engaging in some motion practice regarding the pleadings and consolidation, little substantive progress has been made. *See* §II.B. Virtually no progress has been made on the Wave 3 patents (which includes the '254 Patent). The parties are approximately two weeks away from completing the exchange of contentions for the Wave 3 patents (from the YMTC2 case) and have not taken any depositions in the entire Co-Pending Litigation. Fact discovery is in its infancy. No claim construction positions have been exchanged for the Wave 3 patents, no claim construction order has issued, no infringement or invalidity expert discovery has occurred, and no summary judgment motions have been filed. This weighs in favor of institution. *See Sand Revolution*, 10-11.

The Board also has explained that institution is appropriate where "the

petitioner filed the petition expeditiously…." *Fintiv*, 11. Here, on July 12, 2024, PO asserted eleven Wave 3 patents against Petitioner and subsequently asserted 149 claims across those eleven patents. Ex. 1035. Petitioner proceeded with diligence, starting the filing of petitions covering each patent approximately three months after being served with the YMTC2 complaint. Ex. 1036. This Petition is being filed less than 4 months after YMTC first asserted it against Micron. This also weighs strongly in favor of institution.

4. Issue Overlap

Should the Board institute, Micron stipulates that it will not advance in District Court any ground asserted in this Petition. Micron submits that this eliminates any potential overlap in issues between the proceedings here and in District Court. The Board has found that such stipulations weigh in favor of institution. *Sand Revolution,* 11-12.

5. Party Overlap

Both Petitioner and Patent Owner are parties in the parallel proceeding. This, however, is of little moment as there is often party overlap when there is a parallel proceeding.

6. Other Circumstances

Here, Petitioner submits that its petition has significant substantive merit. It is premised on clear, understandable prior art that the Patent Office did not previously consider. Thus, this factor also weighs in favor of institution.

B. Denial Under §325(d) Would Be Inappropriate

The Examiner did not consider Fujiki, and thus denial under §325(d) would be inappropriate. Moreover, the '254 Patent's apparent point of novelty is forming the slits after the TACs. *See* §VI. Fujiki discloses exactly that. *See* §IX.A.

V. TECHNOLOGY BACKGROUND

The '254 Patent relates to three-dimensional (3D) NAND flash memory. Initially, a NAND flash memory was "planar," that is, two-dimensional (2D). In 2D NAND flash memory, all memory cells lie on a 2D plane (*i.e.*, the x-y plane) on the surface of a memory chip as shown below:

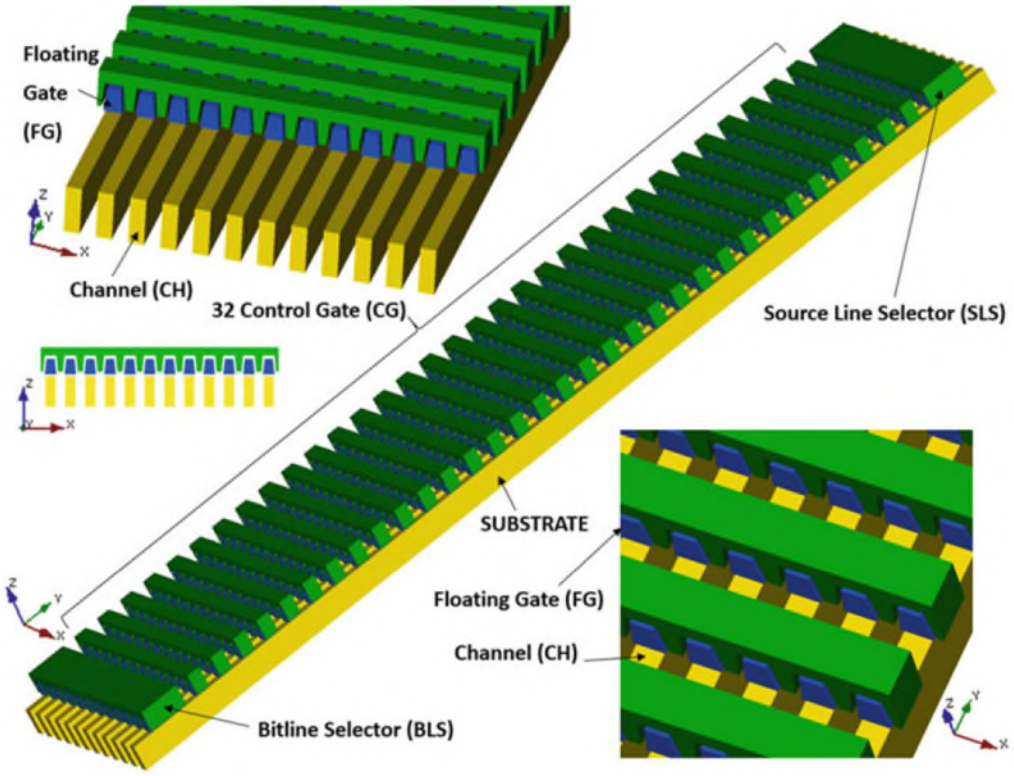


Fig. 3.9 Bird's-eye view of a planar NAND string

Ex. 1008, 86.

Well before the priority date of the '254 Patent, Petitioner and others had developed techniques for manufacturing 3D NAND flash memory. In a 3D NAND flash memory, memory cells are formed in vertical, cylindrical NAND flash "strings":

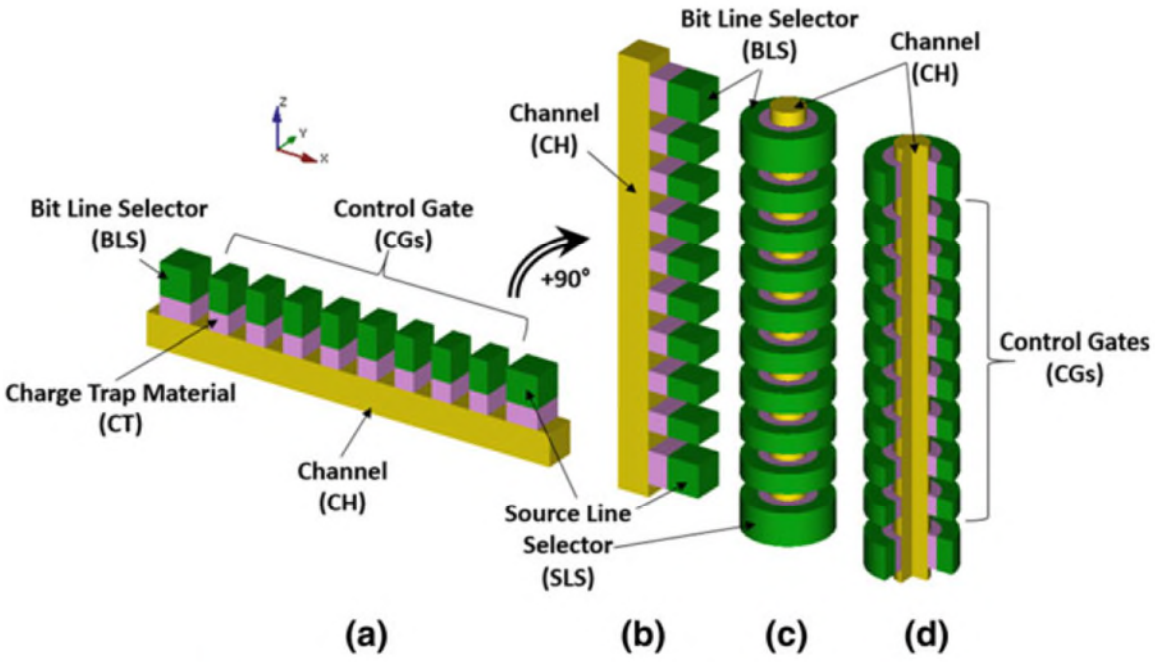


Fig. 4.1 NAND Flash string with horizontal gate and vertical channel: **a** planar, **b** planar rotated by 90°, **c** vertical channel with cylindrical shape and **d** its cross section

Ex. 1008, 102. As labeled in Figure 4.1, above, each NAND string includes a "cylindrical channel." *Id.*, 58; Lee, ¶¶ 39-48.

A number of architectures for constructing a memory device out of NAND strings were known in the art. For example, in the well-known BiCS (Bit Cost Scalable) architecture, various "contacts," that is, electrical connections, are on top

of the memory array. These include source line contacts (for providing a ground connection to the memory cells):

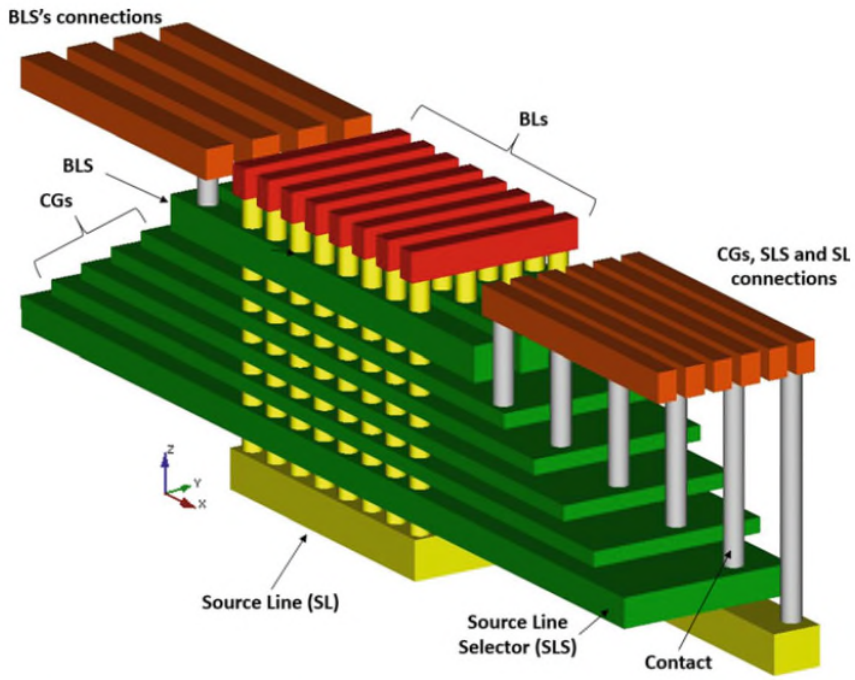


Fig. 4.13 Top bird's eye view of BiCS with gate connections

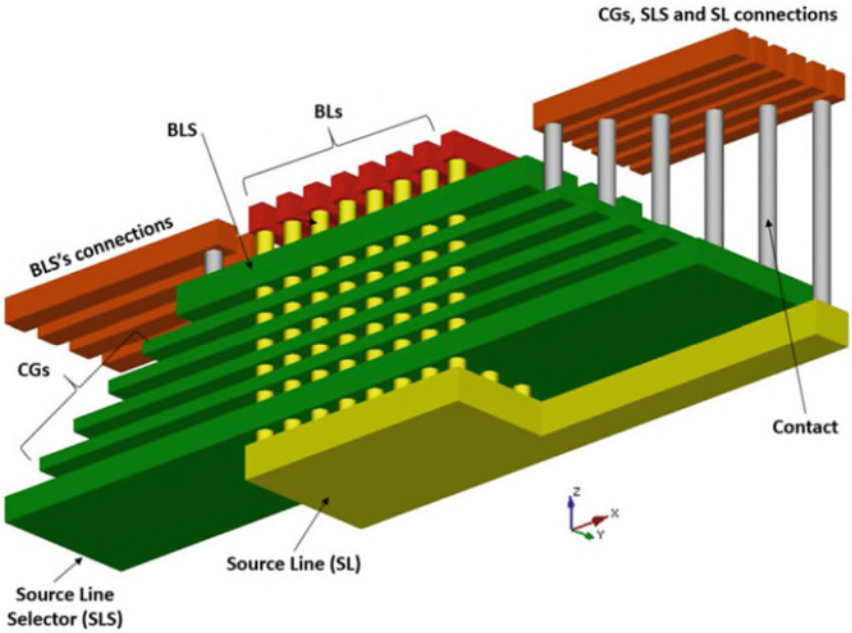


Fig. 4.14 Bottom bird's-eye view of BiCS with gate connections

Ex. 1008, 109-110. The above illustrates source line contacts that extend from the top of the device to the bottom, but do not travel through the stack. It was well known, however, to form such contacts directly through the memory stack. The below provides several examples:

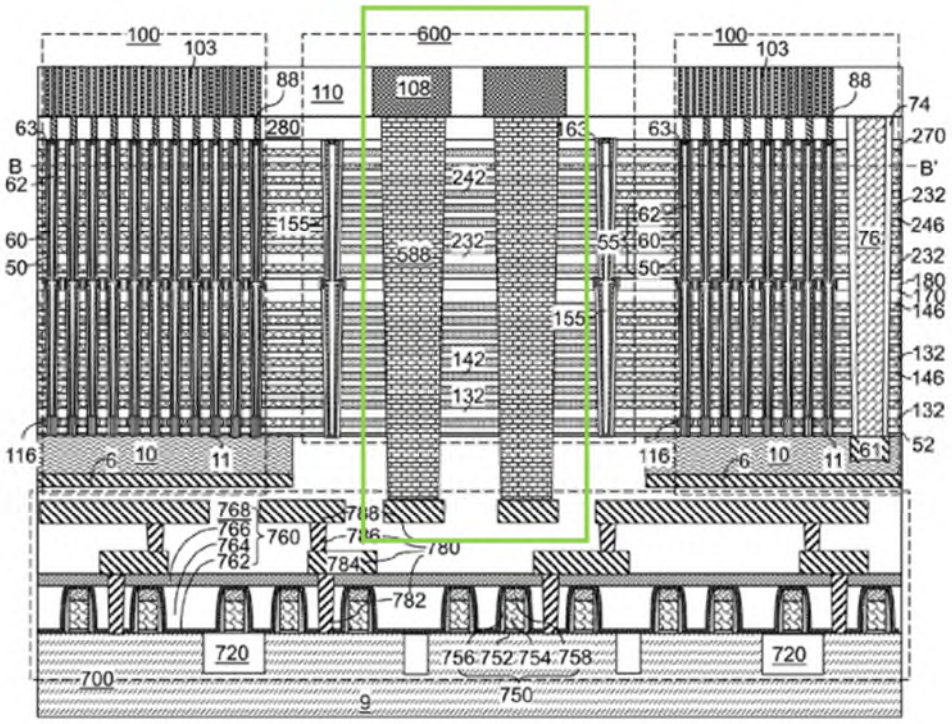


FIG. 69A

Ex. 1009 (U.S. Pat. Pub. 2017/0179026, Toyama), Title ("Through-Memory-Level Via Structures"), [0367], Fig. 69A (588).

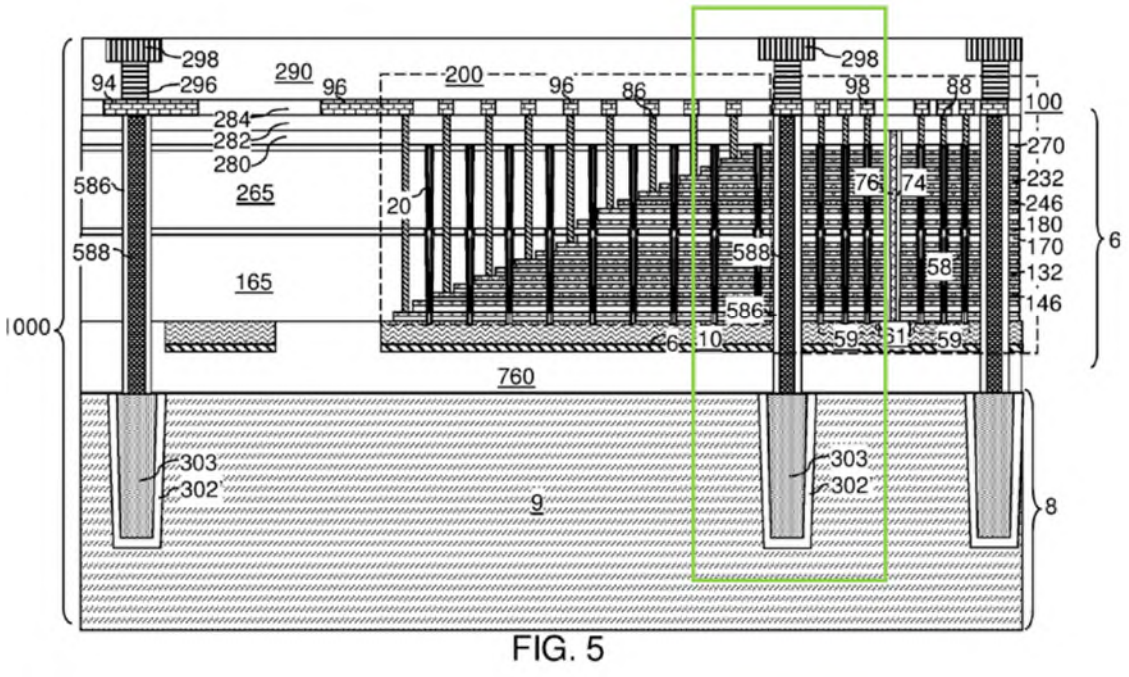


FIG. 5

Ex. 1010 (U.S. Pat. 10,354,980, Mushiga), 10:31-58, Fig. 5 (588).

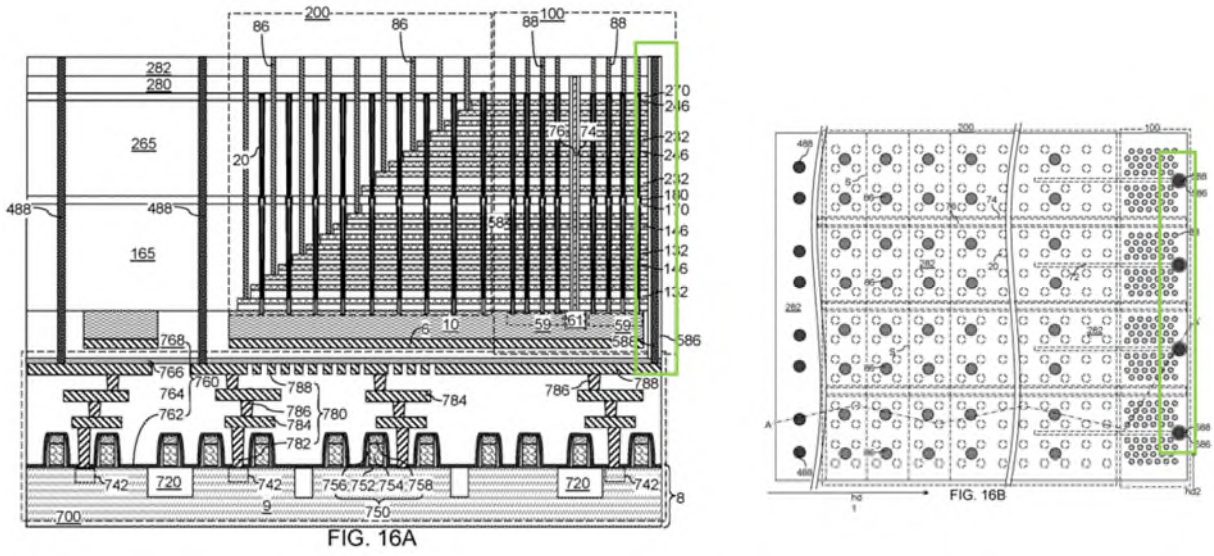


FIG. 16A

FIG. 16B

Ex. 1011 (U.S. Pat. Pub. 2019/0229125), [0189], Figs. 16A, 16B (588). Indeed, in other prior art patents, the assignee of the '254 Patent discloses forming through-

array contacts through the array. *E.g.*, Ex. 1012 (WO 2019/042103) (Fig. 2, 248) and Ex. 1013 (U.S. Pat. 10,679,721), Fig. 1 (110), Abstract ("TAC"); Lee, ¶¶ 49-50.

The memory cells' control gates form a staircase structure as shown below:

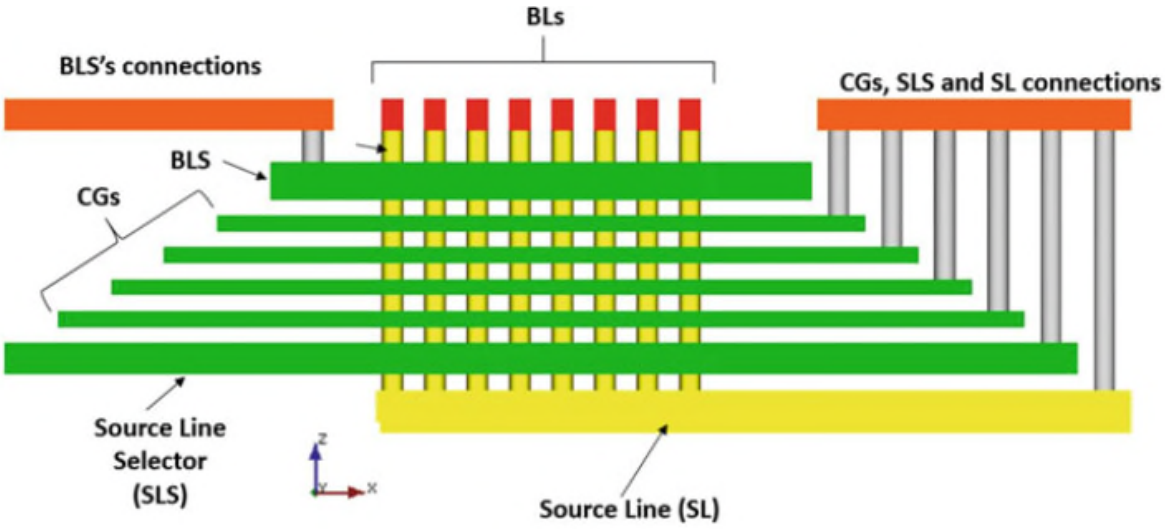


Fig. 4.12 Vertical cross section of BiCS with gate connections

Ex. 1008, 109 (green control gates forming a staircase). Each control gate delivers a control signal to a number of memory cells at the same horizontal level in the 3D NAND memory device. The memory cells that a single control gate controls are together a "word," and the control gate is a "word line." Ex. 1014 (Aritome), 38-40. Reflecting this, the grey columns contacting the top surface of the control gates (shown above in green) are "word line contacts." Lee, ¶¶ 51-52.

Various modifications to the BiCS structure were known, including the use of slit structures, which extend vertically through the memory stack and extend laterally through the device, to serve as source line contacts for the NAND strings. As can be seen, these slits also segment the array into blocks:

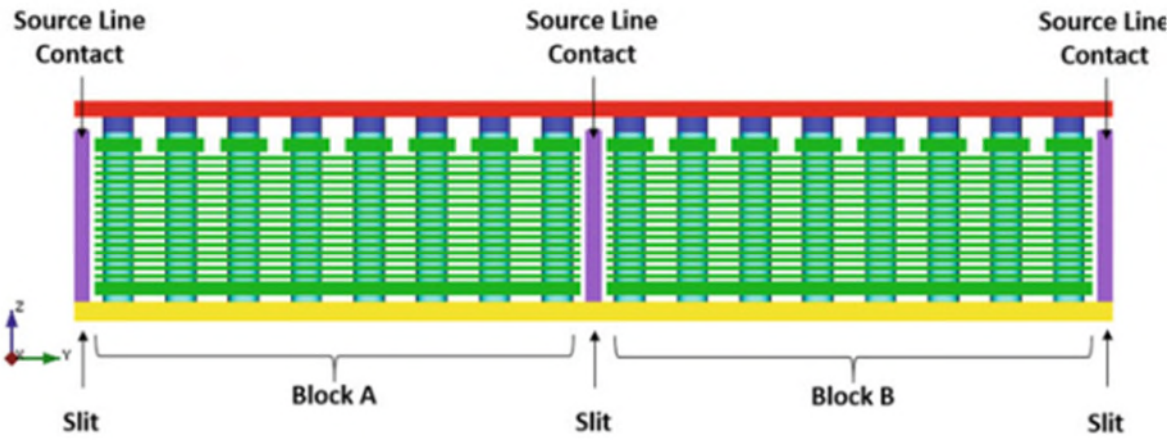


Fig. 6.8 Side view of Fig. 6.7

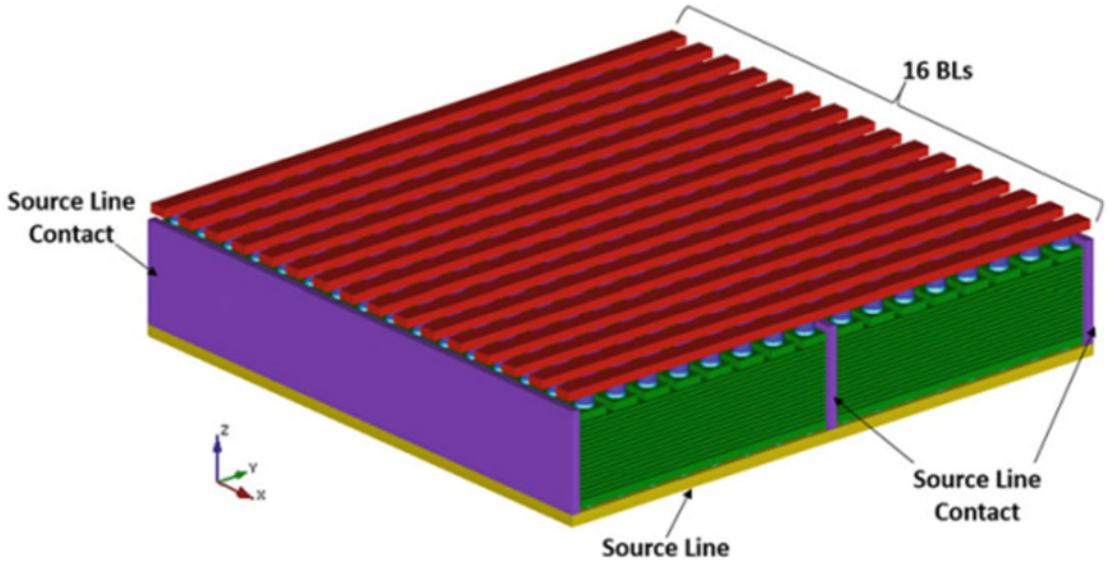


Fig. 6.7 Array slits

Ex. 1008, 185.

In each of the above figures, there are various gaps between the depicted structures. In a real 3D NAND memory device, these gaps are not merely empty space, but instead are filled with an insulating material (also known as a "dielectric"). One purpose of the dielectric is to prevent electrical signals in one conductive

structure from interfering with the electrical signals in other structures. Another purpose of the dielectric is to provide structural support to prevent the conductive structures from collapsing. The stack of alternating gate layers (word lines) and insulating layers is known as the memory stack. Lee, ¶¶ 53-54.

In sum, techniques for manufacturing 3D NAND memory stacks, TACs, and slits were well-known in the art before the '254 Patent's priority date. Lee, ¶¶ 55-58.

VI. THE '254 PATENT AND ITS PROSECUTION HISTORY

The '254 Patent primarily relates to "through array contacts" in a 3D memory device. The '254 Patent refers to contacts that extend through the memory stack as "through array contacts" ("TACs"). Ex. 1001, 8:28-60. The '254 Patent alleges there are issues with forming TACs through a "barrier structure." *Id.*, 4:55-5:20. The '254 Patent does not depict a barrier structure (or a barrier structure with TACs). But a "barrier structure" appears to refer to rectangular block of oxide, i.e., after etching out a rectangular area of the stack, filling that void with oxide (providing an insulating structure for pure conductive core TACs) to form the barrier structure. Such a structure from another YMTC patent (the assignee of the '254 Patent) is shown below:

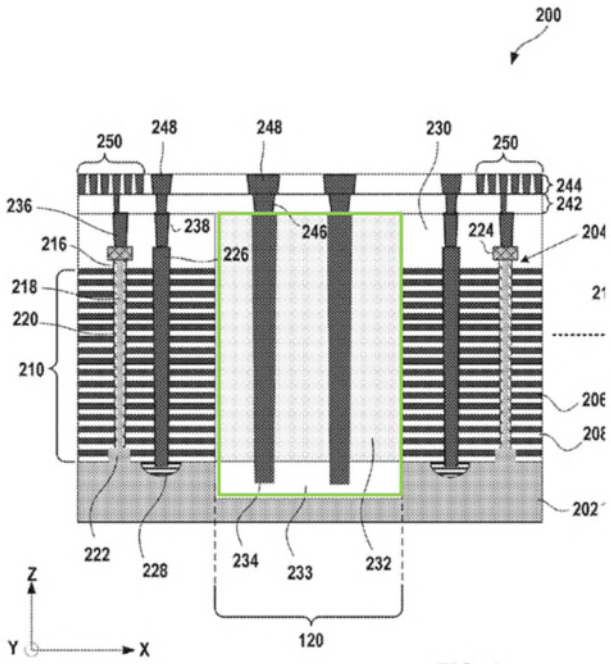


FIG. 2

Ex. 1007 (U.S. Pat. 10,658,378), Fig. 2 (120).

As an alternative to such structures, the ’254 Patent teaches employing a thin spacer (138) to isolate each TAC.

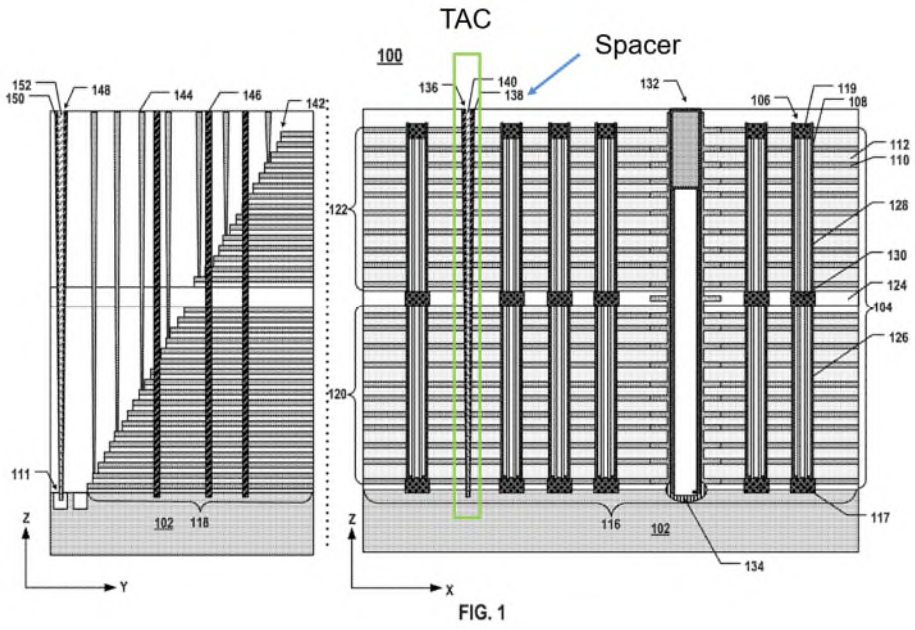


FIG. 1

Ex. 1001, Abstract, 4:55-5:20. The TACs include a dielectric spacer (138) to insulate the TAC from the memory stack (e.g., the conductive gate layers) and a conductive core (140). *Id.*, 8:45-60. The conductive core enables the TAC to connect devices above and below the array. *Id.*, 4:55-59. But as §V discusses, contacts that extend through the memory stack—with a spacer instead of a barrier structure—were well known. Lee, ¶¶ 61-63.

As the below file history summary demonstrates, the '254 Patent's alleged point of novelty appears to be forming a slit ***after*** the TACs. Indeed, the Abstract highlights this timing requirement—which is a limitation of each independent claim. Ex. 1001, Abstract. Like TACs, slits were well known. *See* §V. Shown below in red, the slit structure (which fills the open slit) can include a conductor core and dielectric spacer, and thereby interconnect a source voltage (above the array) to a common source in the substrate (below the array). *Id.*, 8:1-27. The slit can extend laterally (in the Y-direction, into the page) and therefore segment the array into blocks. *Id.* The slit (while a void) can be used in the gate replacement process to replace the sacrificial gates with conductive gates. *Id.*, 14:44-62.

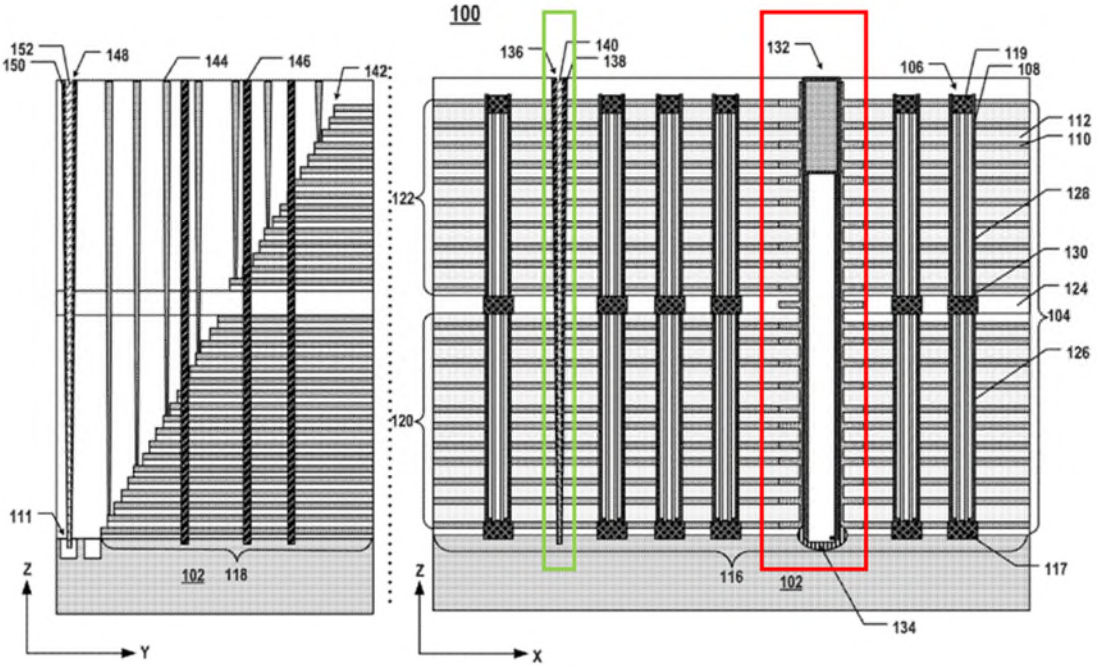


FIG. 1

Id., Fig. 1; Lee, ¶¶ 64-65.

Figure 6 depicts the ’254 Patent’s process flow and illustrates that the ’254 Patent describes forming the slits ***after*** forming the TACs:

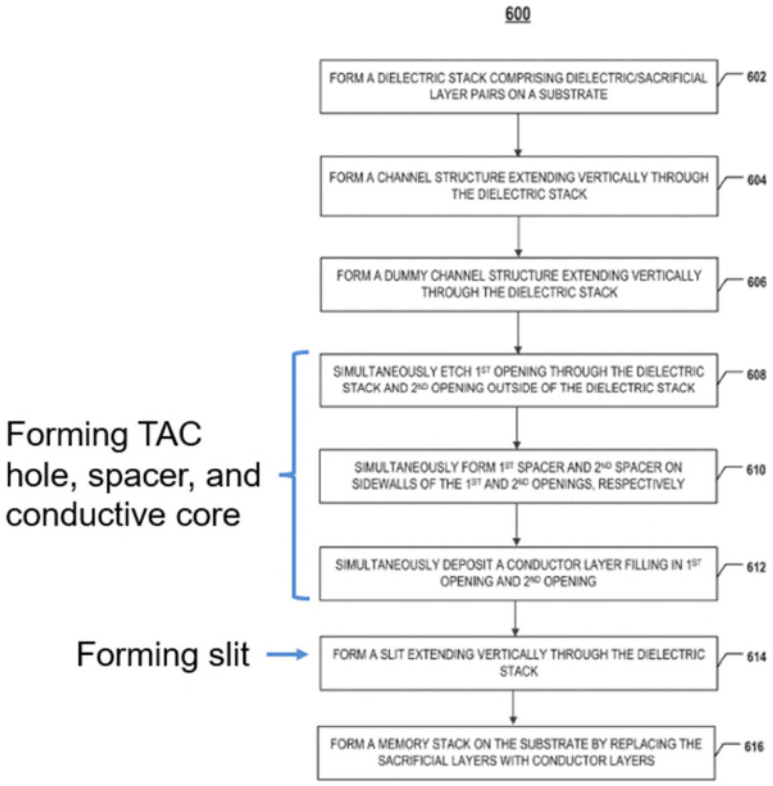


FIG. 6

Ex. 1001, Fig. 6; *see also id.*, Fig. 3B, 12:24-63 (forming TACs holes), Fig. 3C-E, 12:64-14:19 (various ways to form spacer), Fig. 3F, 14:20-43 (forming conductive core for TAC), Fig. 5A, 14:44-15:12 (forming slit), Fig. 5A, 15:12-24 (filling slit); Lee, ¶ 66.

There were no substantive Office Actions in the ’254 Patent’s file history (only approval of a terminal disclaimer on 10/12/2020) or in the file history of the ’254 Patent’s parent application. On 10/26/2020, the claims were allowed, and the Notice of Allowance indicates that the alleged point of novelty is “forming a spacer on a sidewall of the first opening; forming a through array contact (TAC) extending

vertically through the stack by depositing a conductor layer over the spacer in the first opening; and after forming the TAC, forming a slit extending vertically through the stack." Ex. 1002, 133-34; Lee, ¶ 67.

VII. CLAIM CONSTRUCTION

For purposes of this Petition, Petitioner submits that the terms of the '254 Patent's claims do not require further construction and should receive their plain and ordinary meaning. Lee, ¶¶ 68-71.

VIII. LEVEL OF ORDINARY SKILL IN THE ART

A POSITA in the field of the '254 Patent would have had a bachelor of science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (e.g., researching, designing, or teaching) monolithic 3D structures and NAND memory devices, or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience). This POSITA would have been aware of and generally knowledgeable about 3D NAND's structure, how it is manufactured, and its component parts. Lee, ¶¶ 34-38.

IX. DESCRIPTION OF THE PRIOR ART

A. Fujiki

Just like the alleged point of novelty of the '254 Patent, Fujiki discloses forming a TAC through the memory stack and then forming the slit.

Fujiki discloses that "a through-via hole 94 is formed to pierce the stacked body 50, the insulating film 45, and the upper portions of the insulating film 32 and reach a portion of the interconnect 36. Then, the insulating film 79 is formed on the inner surface of the through-via hole 94; and the through-via 78 is formed on the inner surface of the insulating film 79. The through-via 78 is connected to the interconnect 36." Fujiki, [0053].

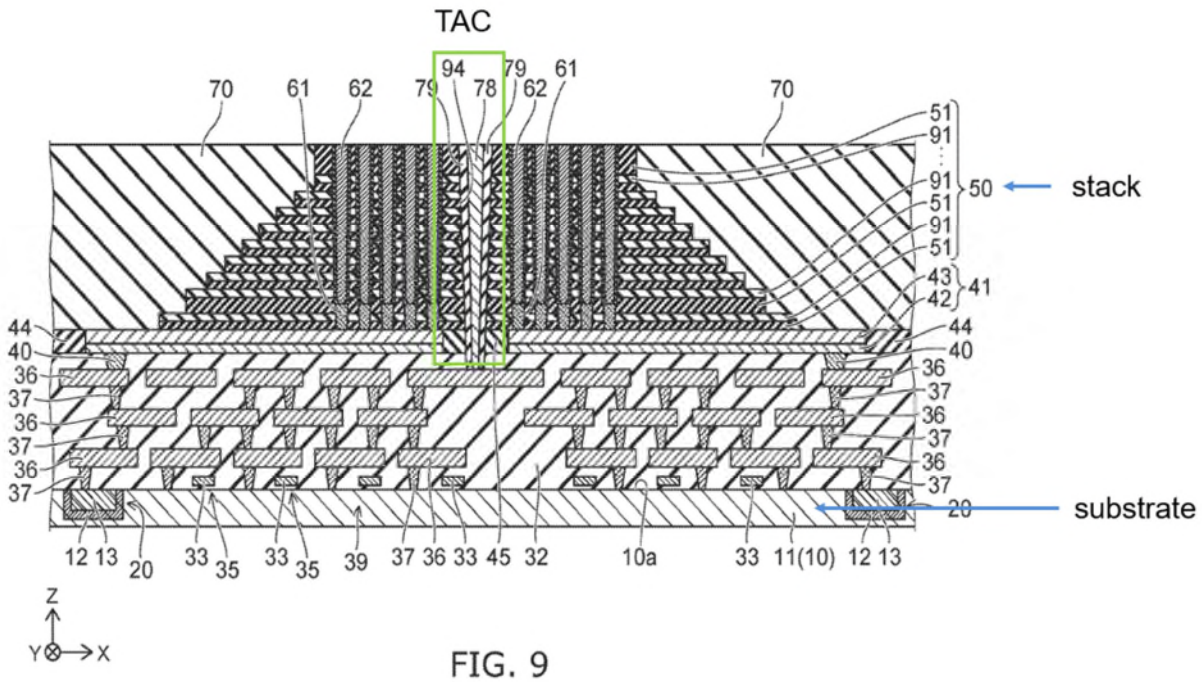


FIG. 9

Id., Fig. 9; Lee, ¶¶ 74-75.

Fujiki discloses that after forming the TAC as shown in Figure 9, "[c]ontinuing as shown in FIG. 10 and FIG. 3, slits 95 are formed to pierce the insulating film 70 and the source electrode film 41; and ***slits 96 are formed to pierce the stacked body 50***." Fujiki, [0054]; Lee, ¶ 76.

B. Fujiki (the US Appl.) Was Effectively Filed on December 25, 2017

All of the Fujiki disclosures upon which this Petition relies are entitled to a December 25, 2017 priority date. Fujiki claims priority to JP 2017-247987, which was filed on December 25, 2017, and has been available in the WIPO Digital Access Service since December 26, 2017. Ex. 1040, 1-2; Ex 1039, 1-2; Ex. 1006, cover. Pursuant to 35 U.S.C. § 102(d)(2) and 35 U.S.C. § 119, Fujiki may rely on the JP 2017-247987 priority date (Japan is a WTO member) and the JP 2017-247987 application was identified to the PTO during prosecution of Fujiki.[3] *See* 35 U.S.C. § 119(a)-(b). 35 U.S.C. § 102(d) provides that Fujiki "shall be considered to have been effectively filed, with respect to any subject matter described in the patent or application …, as of the filing date of the earliest such application that describes the subject matter," including foreign applications. *See also* 35 U.S.C. § 102(d)(2). As the below demonstrates, JP 2017-247987 describes all subject matter of Fujiki upon which this Petition relies. Lee, ¶¶ 78-79. Specifically, the table below correlates the disclosures in Fujiki with JP 2017-247987.

[3] JP 2017-247987 was filed with the Patent Office. Ex. 1041 (the Fujiki file history), 91-122.

Fujiki US 2019/0198524 and corresponding support in JP 2017-247987 (*see* Ex. 1039 (JP App.) and Ex. 1040, 10/21/24 certified translation)

US 2019/0198524 (Ex. 1006)	JP 2017-247987 (Exs. 1039-40)	Comment
Foreign Application Priority data (30) (Cover)	Date of Application (Certificate of Availability page); Application Number (Certificate of Availability page); Submission date (Cover)	Same
Title (54) (Cover)	Name of invention (Cover)	Substantively the same[4]
Abstract (Cover)	Methods of solving the problems [0005]	Substantively the same[5]
Drawings/Figures	Drawings/Figures	The US includes an additional figure upon which the Petition does not rely, namely, fig. 13. Figure 13, however, is only a top-down view of the third-embodiment, in which the translation describes the same without the additional

[4] Generally, throughout Ex. 1006 (Fujiki US App.) and 1040 (translation), the Fujiki US App. uses "memory device" and the translation uses "storage device."

[5] Generally, throughout Ex. 1006 (Fujiki US App.) and Ex. 1040 (translation), the Fujiki US App. uses "stacked" and the translation uses "laminated."

US 2019/0198524 (Ex. 1006)	**JP 2017-247987 (Exs. 1039-40)**	**Comment**
		top-down view. Thus, the Fujiki JP Appl. does support figure 13. Otherwise, the figures are the same. Aligning US figures to JP: • Figures 1-12 are the same. • Fujiki US App. figure 14 corresponds to translation's figure 13. • Fujiki US App. figure 15 corresponds to translation's figure 14.
Field [0002]	Technical Field [0001]	Substantively the same
Background [0003]	Background Art [0002]	Substantively the same
Brief Description of the Drawings [0004] – [0018]	Brief Description of the Drawings [0007]	The US includes an additional figure (Fig. 13 [0016]). Otherwise, the figures and descriptions are the same.
Detailed Description [0019]	Methods of solving the problems [0006]	Substantively the same

US 2019/0198524 (Ex. 1006)	**JP 2017-247987 (Exs. 1039-40)**	**Comment**
First embodiment [0020] – [0059]	First embodiment [0008] – [0040]	Substantively the same
Second embodiment [0060] – [0066]	Second embodiment [0041] – [0045]	Substantively the same
Third embodiment [0067] – [0068]	Third embodiment [0046]	Substantively the same
Third embodiment cont. [0069] – [0070]	Third embodiment cont. [0047]	Substantively the same[6] The Fujiki US App. also references the top-down view of fig. 13. Again, figure 13 is simply the top-down view of figure 12.
Third embodiment cont. [0071] – [0072]	Third embodiment cont. [0048]	Substantively the same
Third embodiment cont. [0073]	Third embodiment cont. [0049]	The Fujiki US App. also describes contacts 82 and 84. These contacts, however, are shown in Figures 2 and 3 of the first embodiment (source and peripheral contacts). *See* Ex. 1040, Figs 2-3, [0026]. Thus, the Fujiki JP

[6] From this point forward, recall that the Fujiki US App. Figure 14 corresponds to translation's Figure 13 and Fujiki US App. figure 15 corresponds to translation's Figure 14.

US 2019/0198524 (Ex. 1006)	**JP 2017-247987 (Exs. 1039-40)**	**Comment**
		App. fully supports this paragraph.
Third embodiment cont. [0074] – [0082]	Third embodiment cont. [0050] – [0057]	Substantively the same
Third embodiment cont. [0083]	Third embodiment cont. [0058]	Substantively the same. Note that the Fujiki US App. references the top-down view of Figure 13.
Third embodiment cont. [0084] – [0085]	Third embodiment cont. [0059]	Substantively the same
Third embodiment cont. [0086]	Third embodiment cont. [0060]	Substantively the same. Note that the Fujiki US App. references the top-down view of Figure 13.
Third embodiment cont. [0087] – [0090]	Third embodiment cont. [0061] – [0063]	Substantively the same
Claim 1	Claim 1	Substantively the same
Claim 4	Claim 2	Substantively the same
Claim 10	Claim 3	Fujiki JP App. lists additional elements.
Claim 16	Claim 4	Substantively the same.
Claim 19	Claim 5	Substantively the same (while Fujiki US App. lists all the elements, Fujiki JP App. incorporates claim 4).

X. GROUND 1: FUJIKI IN VIEW OF THE KNOWLEDGE OF A POSITA RENDER OBVIOUS CLAIMS 1-15, 17-18, AND 20

A. Claim 1:

1. [1.PRE] "A method for forming a three-dimensional (3D) memory device, comprising:"

To the extent the preamble is limiting, Fujiki discloses it. Fujiki, [0025] ("stacked NAND flash memory"), [0046] ("method for manufacturing"); Lee Decl., ¶ 81.

2. [1.A] "forming a stack comprising a plurality of dielectric/sacrificial layer pairs on a substrate;"

Fujiki discloses forming a stack (50) comprising a plurality of dielectric/sacrificial layer pairs (51/91) on a substrate (10 or 43).

The '254 Patent defines "on" and "substrate" broadly. Ex. 1001, 3:52-61 ("It should be readily understood that the meaning of 'on,' 'above,' and 'over' in the present disclosure should be interpreted in the broadest manner such that 'on' not only means 'directly on' something but also includes the meaning of 'on' something with an intermediate feature or a layer therebetween"), 4:6-15 ("As used herein, the term 'substrate' refers to a material onto which subsequent material layers are added. The substrate itself can be patterned. Materials added on top of the substrate can be patterned or can remain unpatterned. Furthermore, the substrate can include a wide array of semiconductor materials, such as silicon, germanium, gallium arsenide,

indium phosphide, etc. Alternatively, the substrate can be made from an electrically non-conductive material, such as a glass, a plastic, or a sapphire wafer.").

Fujiki discloses "substrate 10" (though the claimed substrate could be layer 43, because it is material upon which subsequent material layers are added). Fujiki, [0028], [0033]. On this substrate 10, Fujiki forms "stacked body 50 … by alternately depositing the insulating films 51 made of silicon oxide and insulative sacrificial films 91 made of silicon nitride (SiN)." *Id.*, [0050].

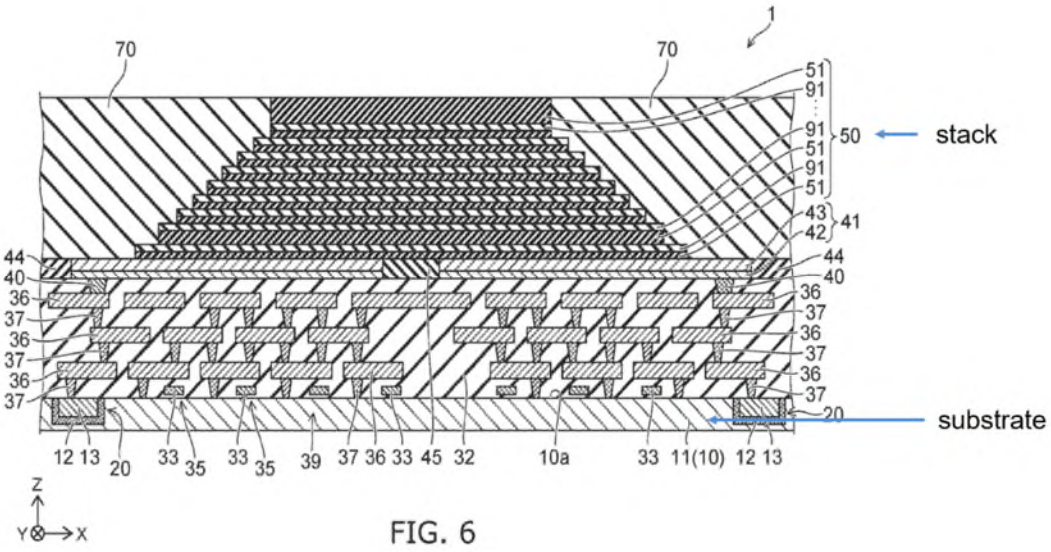


FIG. 6

Id., Fig. 6; Lee, ¶¶ 82-87.

3. [1.B] "forming a channel structure extending vertically through the stack;"

Fujiki discloses forming a channel structure (61, 62, 64-67) extending vertically through the stack (50).

Fujiki discloses "memory cell[s] … at each crossing portion between the electrode films 52 and the silicon pillars 62." Fujiki, [0044]. "FIG. 5 is a cross-sectional view showing a memory cell." *Id.*, [0008]; *see also id.*, [0044] ("channel").

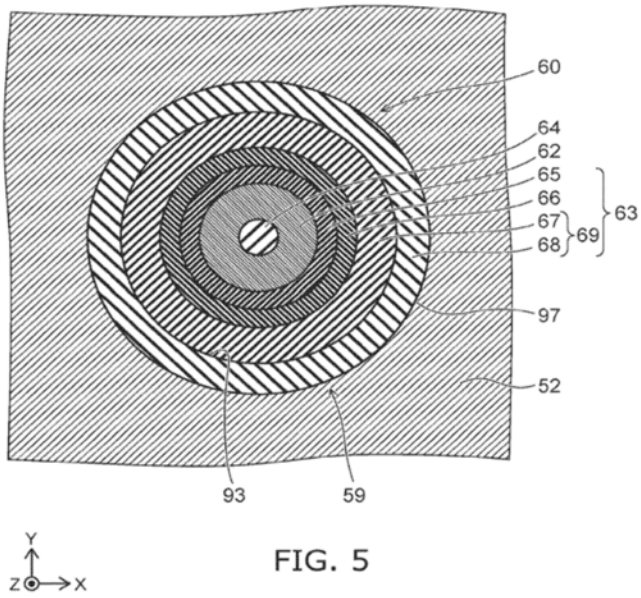


FIG. 5

Id., Fig. 5.

Fujiki forms memory holes through the stack that extends to layer 41 (Fujiki, [0051-52]) and then fills them with the memory layers (*id.*, [0053]).

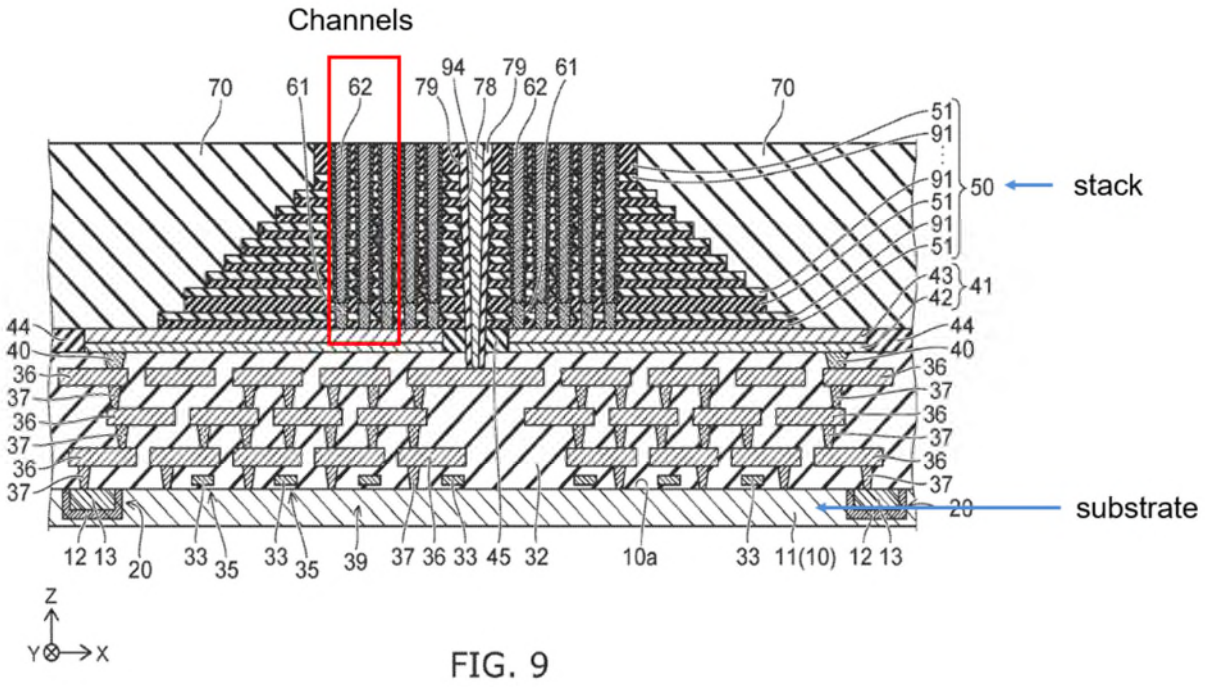


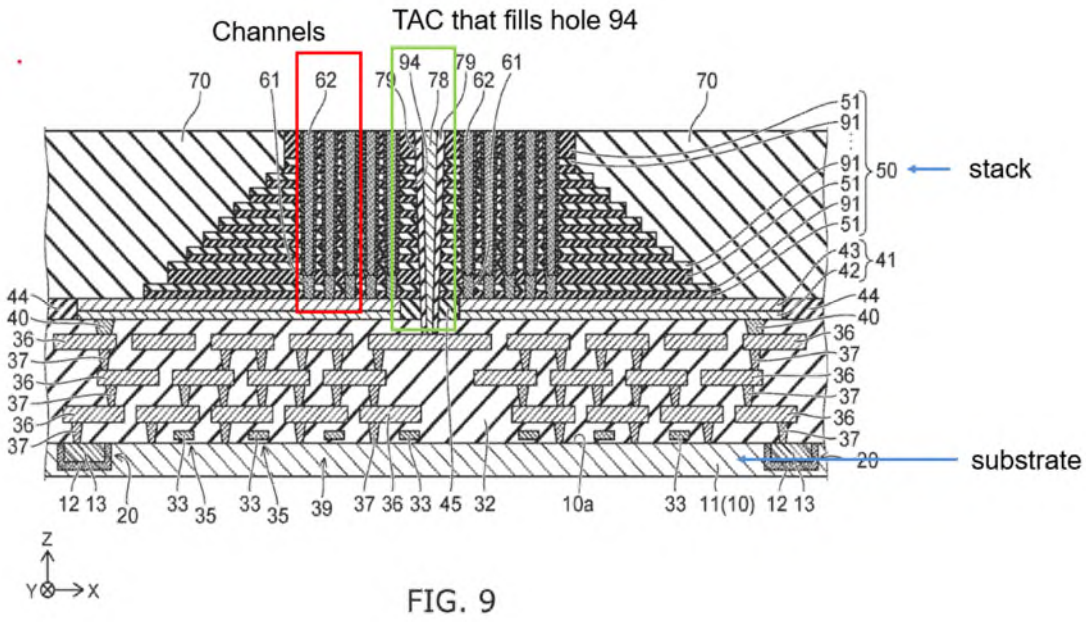
FIG. 9

Id., Fig. 9; Lee, ¶¶ 88-91

4. [1.C] "forming a first opening extending vertically through the stack;"

Fujiki discloses forming a first opening (94) extending vertically through the stack (50).

Fujiki discloses that "a through-via hole 94 is formed to pierce the stacked body 50, the insulating film 45, and the upper portions of the insulating film 32 and reach a portion of the interconnect 36." Fujiki, [0053].

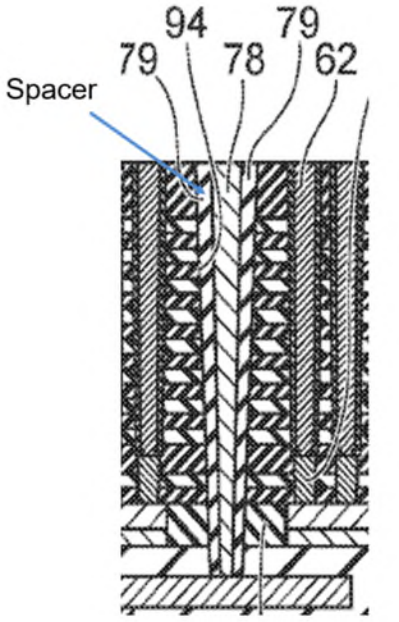


Id., Fig. 9; Lee, ¶¶ 92-93.

5. [1.D] "forming a spacer on a sidewall of the first opening;"

Fujiki discloses forming a spacer (79) on a sidewall of the first opening (94).

Fujiki discloses "the insulating film 79 is formed on the inner surface of the through-via hole 94." Fujiki, [0053]. The insulating film 79 insulates the through-via (see next limitation) from the conductive gate layers and source electrode film. *Id.*, [0042]. This is the same function of the "spacer" of the '254 Patent. Ex. 1001, 8:52-54.

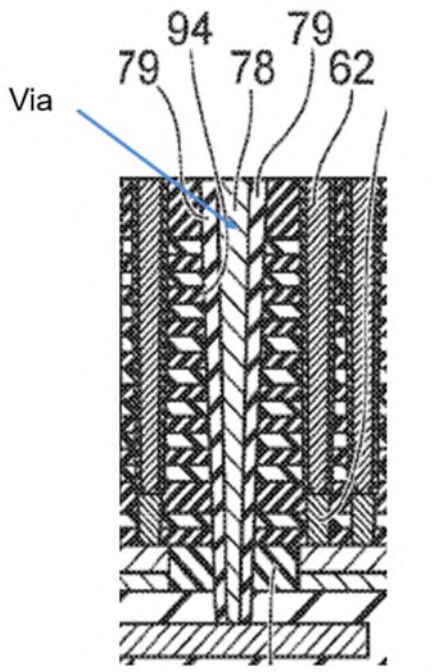


Fujiki, Fig. 9 (partial); Lee, ¶¶ 94-96.

6. [1.E] "forming a through array contact (TAC) extending vertically through the stack by depositing a conductor layer over the spacer in the first opening; and"

Fujiki discloses, or at least renders obvious, forming a through array contact (TAC) (78/79) extending vertically through the stack (50) by depositing a conductor layer (78) over the spacer (79) in the first opening (94). Fujiki, [0053].

Fujiki discloses "the through-via 78 is formed on the inner surface of the insulating film 79. The through-via 78 is connected to the interconnect 36." Fujiki, [0053].



Id., Fig. 9 (partial).

It would have been understood, and certainly obvious, that "through-via 78" is a conductor layer.

First, Fujiki discloses that "[t]he through-via 78 is insulated from the electrode films 52 and the source electrode film 41 by the insulating film 79." Fujiki, [0042]. In other words, through-via 78 is conductive, because it requires an insulating film to prevent short circuits to the conductive gate layers. Second, a "via" is a well-known term that signifies a conductive contact between levels. Ex. 1037 (Weste), 157. Third, Fujiki provides a "control circuit" under the array. Fujiki, [0032]. The through-via connects this circuit to upper-level devices via lower interconnect 36, plug 77, and upper layer interconnect 80. *Id.*, [0042], Fig. 1. Thus, the via must be

conductive to accomplish the connection. Indeed, it would be advantageous for it to be conductive, as that would enable the "control circuit" under the array to connect to the upper-level devices, and routine to implement because it simply involves a conductive fill. Lee, ¶¶ 97-103.

7. [1.F] "after forming the TAC, forming a slit extending vertically through the stack."

Fujiki discloses, or at least renders obvious, after forming the TAC (78/79), forming a slit (96) extending vertically through the stack (50).

After forming the TAC as shown in Figure 9, Fujiki discloses "[c]ontinuing as shown in FIG. 10 and FIG. 3, slits 95 are formed to pierce the insulating film 70 and the source electrode film 41; and ***slits 96 are formed to pierce the stacked body 50***. … Then, the sacrificial films 91 (referring to FIG. 9) are removed by performing wet etching via the slits 96. As a result, spaces 97 are formed where the sacrificial films 91 are removed." Fujiki, [0054]; Lee, ¶¶ 104-05.

Note that slits 96 are not shown in Figure 10. Importantly, Fujiki uses "pierce" to refer to the slit extending through a particular component, e.g., slits 95 "pierce" and thus extend through "electrode film 41":

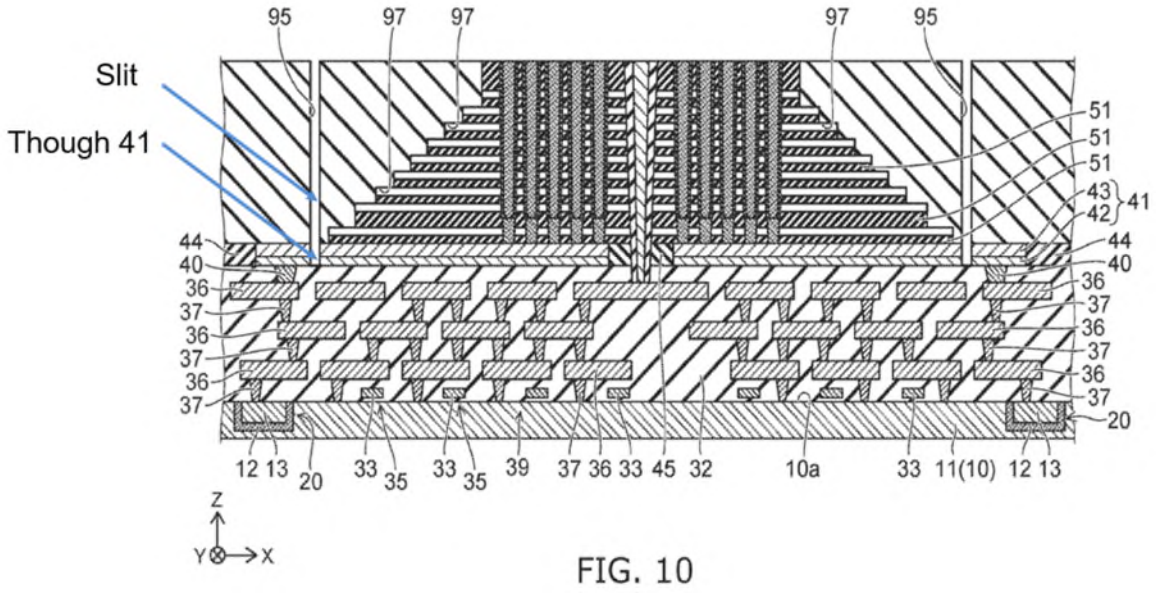


FIG. 10

Fujiki, Fig. 10.

Thus, the slits 96 extend through the stack, because Fujiki states "slits 96 are formed to pierce the stacked body 50." Fujiki, [0054]; Lee, ¶ 106. The slits 96 serve as voids for the gate replacement process and ultimately become insulative slit structures 72. Fujiki, [0055]. The slits 96 and slit structures 72 are shown in in Figure 3:

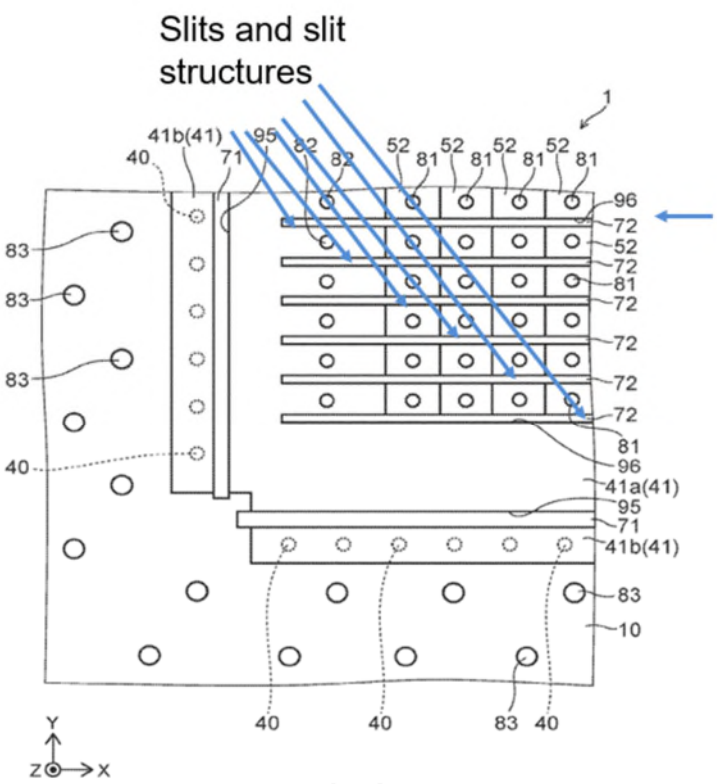


FIG. 3

Id., Fig. 3.

Further, the third embodiment provides more detail on slits 96. The third embodiment simply provides films 54-55 and plugs 56 to connect the slits structures (71 and 72) that fill slits 95 and 96. Of note is the additional film 54 under the stack:

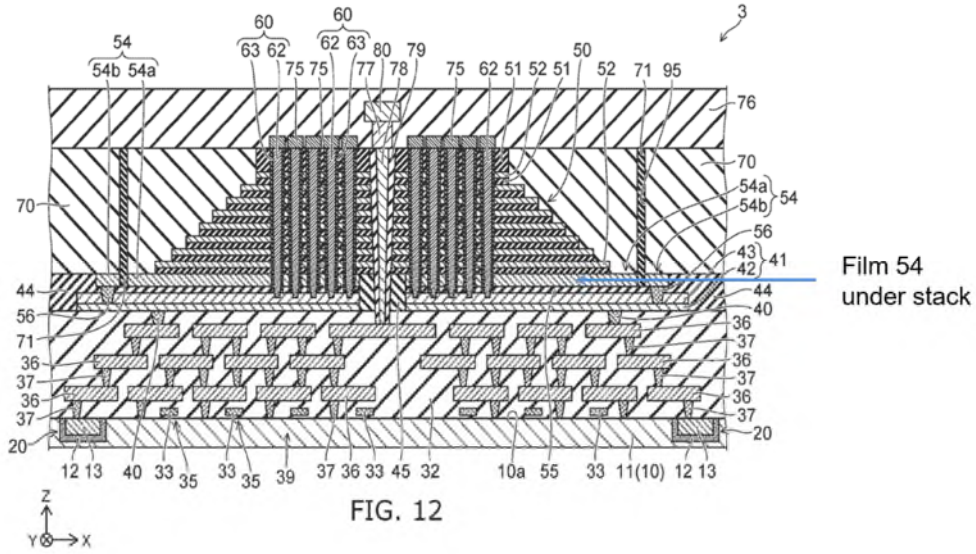


FIG. 12

Fujiki, Fig. 12. In this embodiment, Fujiki describes that the slits "pierce the silicon film 54" to make the connection between slits 95 and 96. Thus, it would have been understood that in the first embodiment, the slits 96 pierce through the entire stack, whereas in the third embodiment, the slits 96 extend past the stack and through the film 54. Lee, ¶¶ 107-110.

At the very minimum, it would have been obvious that the slits extend through the entire stack for the reasons above and in view of the knowledge of a POSITA. First, it was well known that slits are often the voids that the gate replacement process uses to etch out the sacrificial gates, and provide pathways for the replacement gate material to fill the void areas in the stacked body region (50). Fujiki uses slits 96 for both of these processes. Fujiki, [0055]. That process involves creating slits through the entire stack. Ex. 1005 ("Nakajima"), 8:12-15, Fig. 11.

Second, it was well known that creating the slits may involves an RIE etch. *Id.* That etch has to ensure that the slit extends through the stack to ensure that the slit is usable to replace the bottom gate. The layer underlying the stack acts as a buffer of sorts, that is, it ensures that the etch creates the slit through the stack but does not etch any layer underlying the layer, e.g., silicon, supporting the stack. The slits extend through the entire stack to ensure that the void interfaces each sacrificial layer, thereby enabling the etching of the sacrificial gates and deposition of replacement gates. In other words, an etch that did not extend through the stack would prevent replacement of, for example, the bottom sacrificial gates. Thus, a POSITA would have been motivated and had a high expectation of success given that such etches were textbook material, to perform the etch all the way through the stack to, in effect, etch into a buffer to ensure proper gate replacement. Lee, ¶¶ 110-13.

B. Claim 2:

1. [2] "The method of claim 1, further comprising prior to forming the first opening, forming a dummy channel structure extending vertically through the stack."

Fujiki in view of the knowledge of a POSITA renders this limitation obvious.

First, Fujiki discloses forming channel structures before the TAC (which involves "forming the first opening"). Fujiki discloses forming the channels and states "[t]hen, a through-via hole 94 is formed …." Fujiki, [0053].

Second, a POSITA would have been motivated, with a high expectation of success, to also form dummy channels. To start, recall that Fujiki uses a gate replacement process. Fujiki, [0055]. It was known that to perform this gate replacement process, "support pillars" were necessary. Ex. 1018 (U.S. Pat. 8,945,996), 5:64-6:2, 7:19-23. As demonstrated below, it was well known that one common option for such support pillars were dummy channels. Lee, ¶¶ 119-21.

Kai, for example, confirms the knowledge of a POSITA. Kai discloses forming active and dummy channels, which provide structural support. Ex. 1015 (U.S. Pat. 10,290,643, Kai), 9:23-26 (defining "support opening" as "a structure in which a support structure (such as a support pillar structure) that mechanically supports other elements is subsequently formed"), 9:45-48 ("support openings 19" extend through stack), 10:20-27 (forming channels in support openings). Kai refers to the dummy channels as "support pillar structure 20" and active channels as "memory stack structures." *Id.*, 16:28-38; Fig. 15A, 25:58-63 (dummy support channels (20) have no connection to the upper level, whereas the active channel structures (55) include contacts (88)). Park, likewise, discloses active and dummy, supporting channels. Ex. 1016 (U.S. Pat. 9,859,297, Park), 6:19-26, 7:45-51. Kim, too, forms active channels and dummy channels through the stack at the same time. Ex. 1017 (U.S. Pat. Pub. 2018/0308559, Kim) [0047] ("The stack structure ST may be penetrated with a plurality of dummy holes DH on the connection region CTR,"

"DS may physically support," and listing same materials as channels), [0071] ("The channel holes CH and the dummy holes DH may be formed at the same time."), [0072] (same time), Fig. 13 (DH through stack on edge).

A POSITA would have been motivated to form dummy channels through the stack for several reasons. First, it is advantageous to use dummy channels as support structures because they can be made by the same process and at the same time as the active channels. Ex. 1015 (Kai), 10:20-27; Lee, ¶ 122. Second, dummy channels do not require connections to the upper-level devices, thereby not consuming space above the structures while also serving as support structures. Ex. 1016 (Park), 8:55-65; Lee, ¶ 122. Third, it was well known to include dummy support members, including ones that travel through the entire stack or partially through the stack. Ex. 1015 (Kai), Fig. 6A (support members 20), 16:28-38. It was well known that adding additional dummy channels "provide[s] additional structural support during replacement of the [sacrificial gate layers]." Ex. 1019 (U.S. Pat. 10,115,632), 30:14-27; *see also id.*, 15:3-22 (structures 20 are dummy channel structures); Lee, ¶¶ 119-21. Fourth, adding dummy structures would result in reducing the likelihood of defective bits on the edge of the memory cell region, because the inclusion of the additional rows extends the memory cell pattern for those respective columns into the dummy region. *Id.* ¶ 117. It was well known that when a pattern abruptly stops (instead of extending into the dummy region), defects occur on the edge. *Id.* (citing

Ex. 1020 (U.S. Pat. 5,945,717), 8:47-53 and Ex. 1021 (U.S. Pat. 10,347,487), 2:20-43 to explain the edge effect). Fifth, adding dummy structures would result in an overall more uniform feature pattern, which reduces processing issues. Lee, ¶ 118 (citing Ex. 1022 (Ronse), 11 to explain this processing issue).

Adding dummy structures would have been routine and a POSITA would have had a high expectation of success. First, as discussed above, Fujiki already discloses forming channel structures, and the same materials are used for dummy channels. Second, for the reasons above, the additional dummy channel structures would actually reduce processing issues. Third, as the above demonstrates, dummy channels were commonplace. Lee, ¶ 123.

C. Claim 3:

1. [3] "The method of claim 1, wherein forming the first opening comprises simultaneously etching the first opening through the stack and a second opening outside of the stack."

Fujiki discloses, or at least renders obvious, this limitation.

Fujiki discloses forming "contacts 81 to 83" outside of the stack. Fujiki, [0043]. These include contacts 82 and 83 that extend through insulating layer 70, either of which is in a "a second opening":

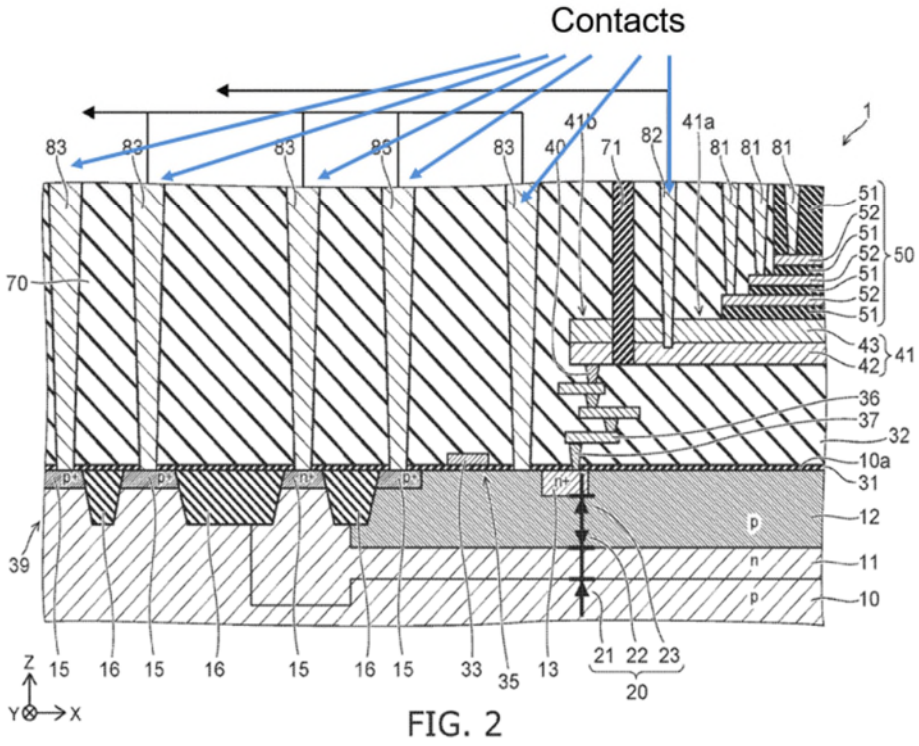


FIG. 2

Id., Fig. 2.

In the manufacturing description of embodiment one, however, Fujiki only describes forming one through-via. Fujiki, [0050]. As explained below, it would have been understood, and certainly obvious, that Fujiki would (or could) simply etch all contact holes for Fujiki's TAC and contacts 82 or 83 at once, just as Fujiki does with its channel holes. *Id.*, [0052]; Lee, ¶¶ 124-26.

As an initial matter, insulating film 70 surrounds the stacked body and the contacts. Fujiki, [0040]. When forming the TAV, insulating film 70 is already in place, enabling simultaneous etching of contact holes for the TAV and 82 and 83 contact holes. *Id.*, Figs. 8-10; Lee, ¶ 127.

A POSITA would have been highly motivated to do so with a high expectation of success.

First, it would have been known to reduce processing time, because only one etch process would be necessary to process all contact holes. That is why it was known to form openings for different structures at the same. *E.g.*, Ex. 1023 (U.S. Pat. Pub. 2019/0081061, Tessariol), [0037] ("dummy-structure openings 56 and via openings 54 are formed at the same time (i.e., simultaneously)"), Fig. 9. This was widely known in the art. Because of this well-known benefit, process technologies, e.g., etch chemistries, that achieve simultaneous etching of different holes—including holes of different sizes—became textbook material. *E.g.*, Ex. 1043 (Wolf Vol. 2), 47; Lee, ¶¶ 128-29

For example, Mushiga discloses forming holes for through-array contacts (588) (as well the insulating spacers and conductive cores) at the same time:

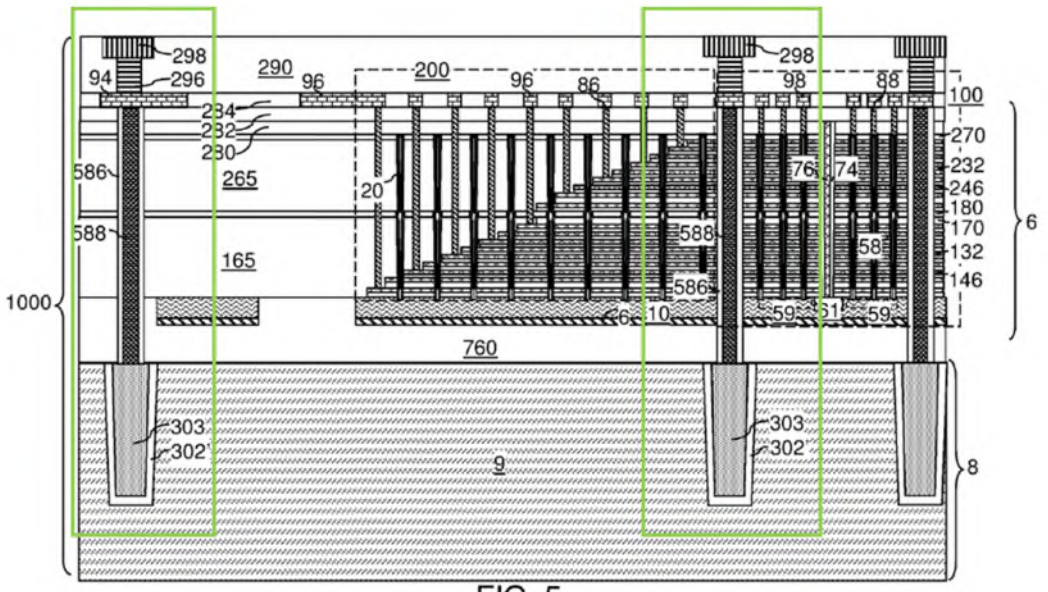


FIG. 5

Ex. 1010 (Mushiga), Fig. 5, 10:31-58.

By way of another example, Masamori discloses forming holes for contacts (as well as the conductive fill) at the same time as well as support structures and multiple contacts at the same time:

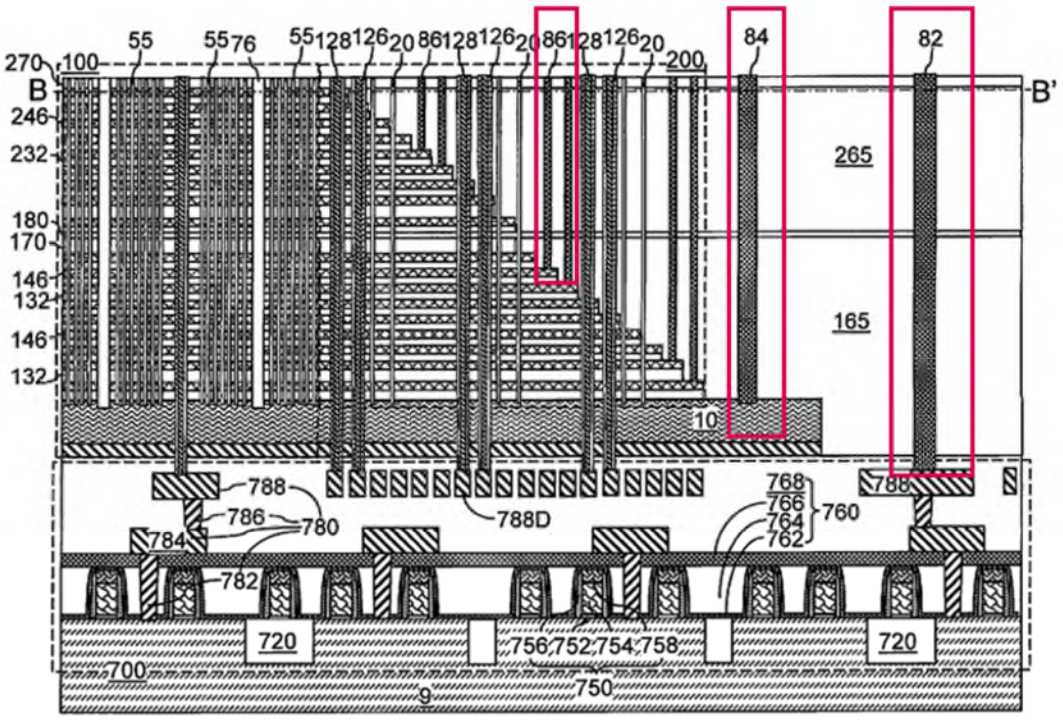


FIG. 13A

Ex. 1019 (U.S. Pat. 10,115,632), Fig. 13A, 24:22-29 ("Alternatively, two or more types of contact via structures (82, 84, 86) may be formed employing a common set of patterning processes and fill processes provided that the anisotropic etch process therein can control vertical extent of cavities at target height levels for each type of cavities that are simultaneously formed."). Notably, the contact holes extend down to conductive gate layer (86), the substrate (84), and a metal interconnect (82). But Masamori describes using a timed anisotropic etch to control the target heights. *Id.*

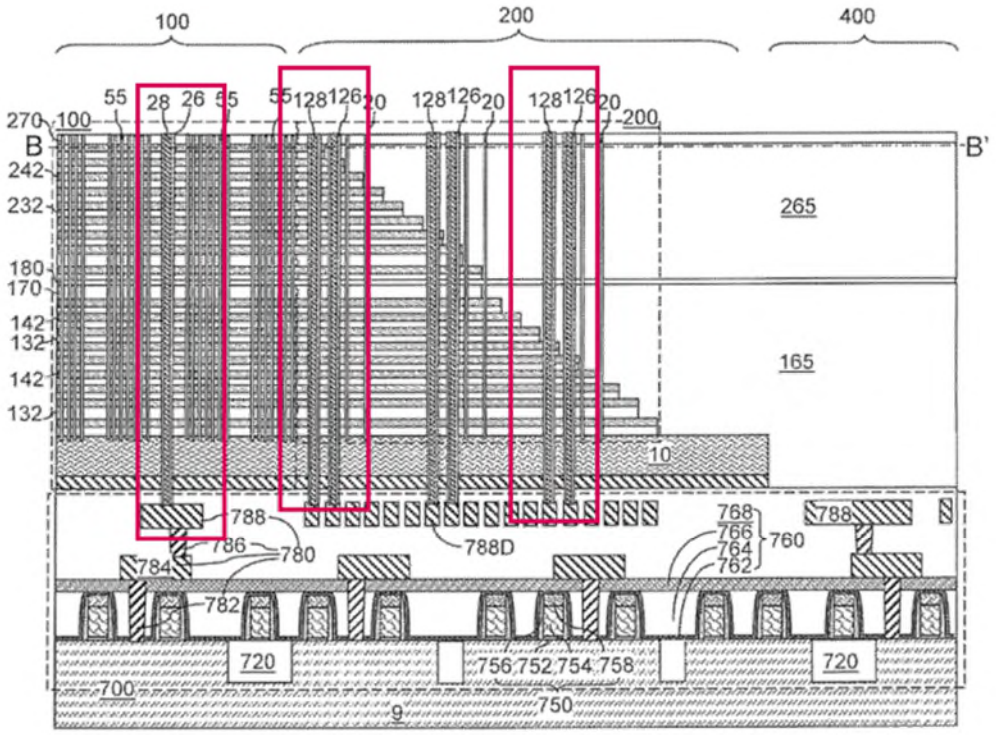


FIG. 8A

Id., Fig. 8A, 17:51-54 ("In one embodiment, the laterally-insulated support structures (126, 128) can be formed concurrently with the laterally-insulated conductive via structures (26, 28) and can have the same structure.").

By way of another example, Kai II discloses forming openings for various contacts and memory structure openings in a single step:

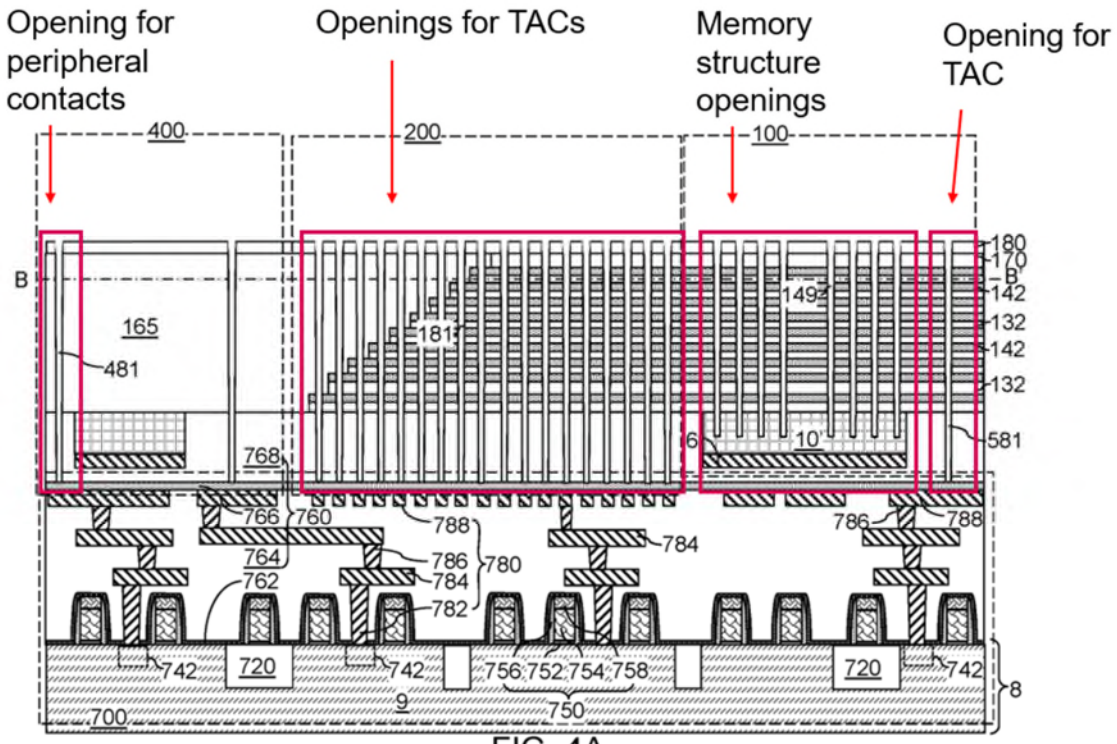


FIG. 4A

Ex. 1038 (U.S. Pat. 10,388,666, Kai II), Fig. 4A, 17:30-44 ("The pattern of openings in the photoresist layer can be transferred through the inter-tier dielectric layer 180 and the first-tier structure (132, 142, 170, 165) and into the in-process source-level material layers 10′ and the at least one second dielectric layer 768 by a first anisotropic etch process to form the various first-tier openings (149, 181, 481, 581) concurrently, i.e., during the first anisotropic etch process. The various first-tier openings (149, 181, 481, 581) can include first-tier memory openings 149, first-tier staircase-region openings 181, first-tier array-region openings 581, and first-tier peripheral-region openings 481."). Notably, the memory structure openings (149)

extend into the substrate (as shown above), while the other openings extend down to the metal interconnects. *E.g.*, *id.*, 17:48-58, 18:9-21 (181 and 581 openings extending to interconnect). Like Masamori, Kai II employs an anisotropic etch. *Id.*, Fig. 4A, 17:30-44; Lee, ¶¶ 130-34.

Indeed, because Fujiki describes one process for forming the through-vias, it would have been understood that Fujiki describes forming multiple contacts simultaneously. Specifically, Fujiki states that the shown components are "fewer than the actual components." Fujiki, [0024]. And it was known when implementing TACs, the typical configuration includes multiple TACs. *E.g.*, Ex. 1010 (Mushiga), Fig. 5, 10:31-58; Nakajima, Figs. 1, 2 (multiple TACs, i.e., C4s), 7:26-8:11. It was typical to describe a process for creating a single contact even though that process actually forms multiple contacts simultaneously. Nakajima, Figs. 1, 2 (multiple TACs, i.e., C4s), 7:26-8:11; Lee, ¶ 126. Thus, Fujiki already discloses the ability to form multiple contacts (including the openings) at the same time.

And it would have been routine and highly predictable to simultaneously etch multiple holes. Etches that simultaneously etch holes, regardless of whether some of the holes extend through all of the stack and other holes extend through only a portion (or none) of the stack, were well known and routine to implement. *E.g.*, Nakajima, 7:37-43 (forming holes for C4 contacts), Fig. 2 (TACs, C4, through in various locations); Ex. 1023 (Tessariol), [0037] ("dummy-structure openings 56 and

via openings 54 are formed at the same time (i.e., simultaneously)"), Fig. 9 (extending through different number of stack layers). And as the above describes, controlling the target depth, even if the target depth interfaces to a different material, was well known. For example, a process forms multiple holes in a mask before the etch that simultaneously creates the holes and other factors, such as time and etch chemistries, control the depth of, e.g., an anisotropic etch. *E.g.*, Ex. 1043 (Wolf Vol. 2), 47; Lee, ¶ 136.

D. Claim 4:

1. [4] "The method of claim 3, wherein forming the TAC comprises depositing the conductor layer in the first opening to form the TAC and in the second opening to form a peripheral contact."

Fujiki discloses, or at least renders obvious, this limitation.

The claim [1.E] analysis demonstrates that Fujiki deposits the conductor layer in the first opening. Contacts 82 and 83 are "peripheral contact[s]," because the contacts are outside of the array. Ex. 1001, 10:2 (peripheral contact 148), Fig. 1. And Fujiki deposits a conductor layer in the second opening to form contacts 82 and 83. Fujiki, [0043]; Lee, ¶ 137.

To the extent that PO argues that this filling must occur simultaneously (the claim does not recite such a requirement), Fujiki would have been understood, or at least render obvious, such simultaneous deposition for the following reasons.

As the claim 3 analysis demonstrates, it would have been understood, or at least obvious, to etch the first (for the through-via) and second holes (for contacts 82 or 83) at the same time. For effectively the same reasons, it would have been understood, or at least obvious, to form the conductive layers at the same time. First, Fujiki only describes forming one through-via. Fujiki, [0052]. The claim [1.E] analysis demonstrates that Fujiki discloses depositing a conductor layer in the holes to form the through-vias. Thus, it would have been understood, and at least obvious, that Fujiki would simply use this process for forming the conductive layer of the through-vias and contacts 82 or 83. Second, as claim [3] demonstrates, simultaneous etching and conductive layer fill has the significant benefit of saving processing time. Third, as claim [3] demonstrates, forming such contacts, including the hole, insulating layer (at least for the TAC), and conductive core was routine and highly predictable. Lee, ¶¶ 138-40.

E. Claim 5:

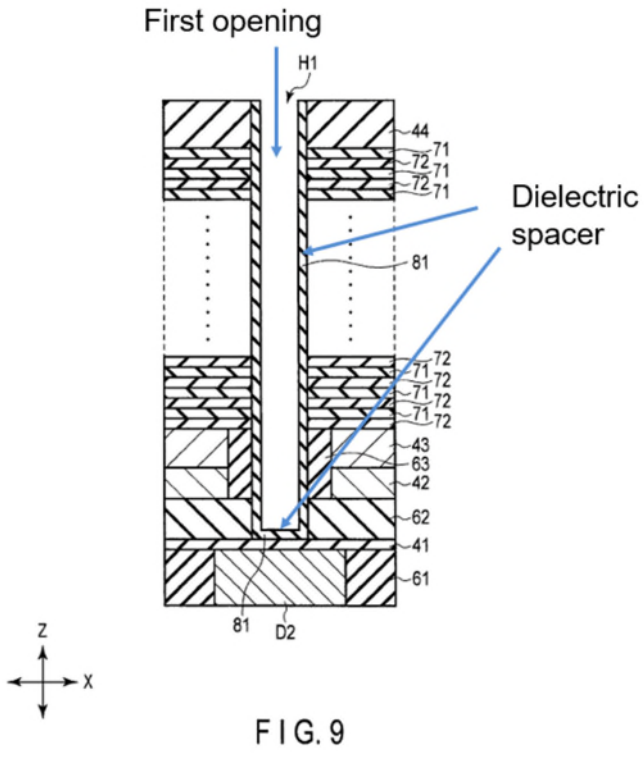
1. [5.PRE] "The method of claim 1, wherein forming the spacer on the sidewall of the first opening comprises:" [5.A] "depositing a dielectric layer on the sidewall and a bottom surface of the first opening; and"

Fujiki renders this limitation obvious in view of the knowledge of a POSITA.

Fujiki does not detail the process of forming the through-via. However, it was well known, and obvious, that to form a material, including an insulator liner, on only the sidewall of a hole, the typical approach involves deposition of material on

all surfaces of the hole and then an etch to remove the deposition on the bottom surface. Ex. 1028 (U.S. Pat. 9,728,546), 34:62-35:3 ("The dielectric liners 141 can be formed, for example, by formation of a dielectric material layer including a first dielectric material, and by a subsequent anisotropic etch (such as a reactive ion etch) that removes horizontal portions of the dielectric material layer to form dielectric spacers 141"), 17:41-46 ("Each first semiconductor channel portion 601 can be formed on inner sidewalls of each memory film 50 by deposition of a semiconductor material layer and a subsequent anisotropic etch of the semiconductor material layer."). Lee Decl., ¶¶ 141-43.

By way of another example, Nakajima discloses that in forming a spacer: "silicon oxide layer 81 is conformally formed along the bottom and the side surface of the hole H1." Nakajima, 7:44-49.



F I G. 9

Id., Fig. 9; Lee Decl., ¶¶ 144-45.

A strong motivation for the process that creates the dielectric portion on the bottom is providing a conformal liner. Nakajima, 7:44-49. The typical conformal process for forming a conformal spacer involves forming the conformal dielectric layer along the sides and bottom surface. *Id.*, ("silicon oxide layer 81 is conformally formed along the bottom and the side surface of the hole H1"). Otherwise, it would be difficult to form the conformal layers on the sidewall. As dimensions shrink in semiconductor devices, conformal liners are critical, and in fact, led to the popularity of ALD processes. Ex. 1025 (Hwang), 12 ("better conformality over three-

dimensional (3D) structures"), 13 ("unprecedented conformality over the 3D structures"). Lee Decl., ¶¶ 145-46.

Such techniques, including ALD, were highly predictable, as they were textbook material and routine to implement. Again, the process for forming a spacer that creates the bottom portion was well known and understood, involving basic depositions (e.g., ALD) and etches (e.g., anisotropic etch). *E.g.*, Nakajima, 7:44-61 (deposition and etch to form spacer); Ex. 1028 (U.S. Pat. 9,728,546), 17:41-46, 34:62-35:3 (same); Ex. 1009 (Toyama), [0226], [0313] (ALD for spacers); Ex. 1023 (Tessariol), [0038], [0063] (recognizing multiple suitable deposition and etch types for spacers); Lee Decl., ¶ 147.

2. [5.B] "removing part of the dielectric layer that is deposited on the bottom surface of the first opening."

Fujiki renders this limitation obvious in view of the knowledge of a POSITA.

Again, Fujiki does not detail the process of forming the through-via, but the analysis of claim [5.A] above demonstrates that it was well known that when depositing an insulating layer such as silicon oxide in a contact hole, that oxide will typically form on the bottom of the hole, which is necessary to remove. By way of example, Nakajima demonstrates this: "Next, as shown in FIG. 10, a portion of the silicon oxide layer 81 that is located at the bottom of the hole H1 is removed by, for example, RIE using a mask layer not shown in the drawing, so that the silicon nitride layer 41 is exposed." Nakajima, 7:50-53.

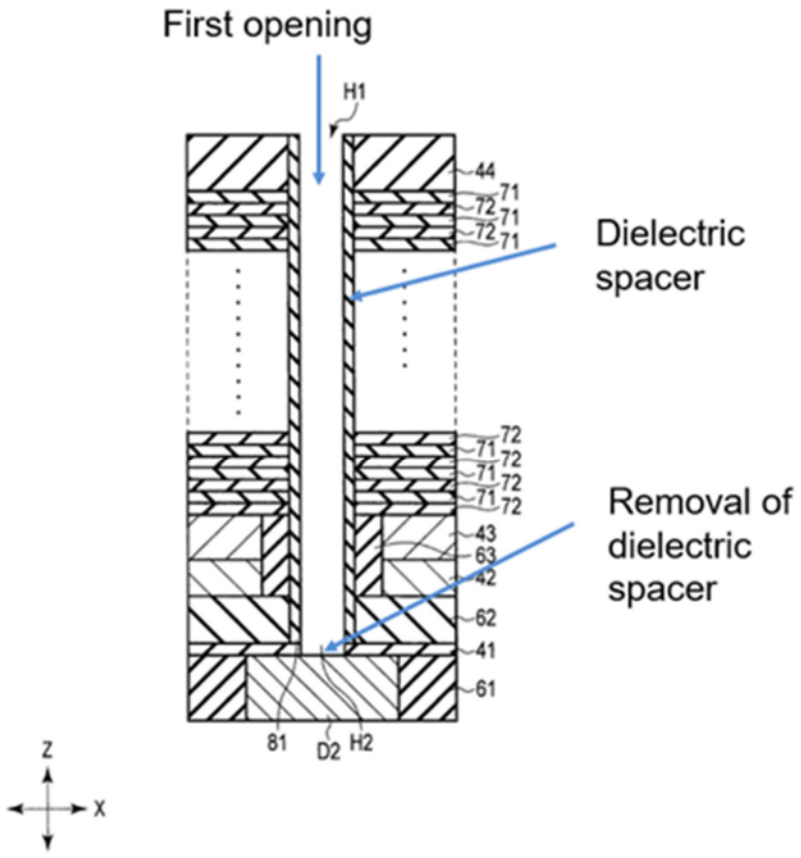


FIG. 10

Nakajima, Fig. 10; Lee Decl., ¶¶ 148-49.

Note that once the bottom of the hole in Fujiki is covered by an oxide layer, it must be removed because the through-via must connect to lower interconnect 36. Fujiki, [0042], Fig. 1. Put simply, a POSITA would have been motivated to remove the bottom oxide so that the TAC can electrically couple to an underlying device or local interconnect. Lee Decl., ¶ 149.

Again, such techniques, including an etch to remove the bottom portion, were highly predictable, as they were textbook material and routine to implement. *E.g.*, Nakajima, 7:44-61 (deposition and etch of bottom dielectric to form spacer);

Ex. 1028 (U.S. Pat. 9,728,546), 17:41-46, 34:62-35:3 (same). Thus, it would have been obvious to apply such textbook etches, e.g., RIE, to remove the bottom oxide. Lee Decl., ¶¶ 149-50.

F. Claim 6:

1. [6] "The method of claim 5, wherein the deposition of the dielectric layer comprises atomic layer deposition (ALD), and the removal of the part of the dielectric layer comprises anisotropic etching on the bottom surface of the first opening."

Fujiki renders this limitation obvious in view of the knowledge of a POSITA.

ALD

Fujiki does not detail the type of deposition technique that it uses to deposit the insulating film 79 (spacer) for the through-via (TAC). Fujiki, [0053]; *see also* [1.D] analysis. The claim 5[PRE-B] analysis demonstrates, however, that it was well known, obvious, and beneficial to form a conformal spacer. Nakajima, 7:44-49; *see also* [5.PRE-A] analysis. It was well known to deposit a conformal dielectric spacer, e.g., a silicon oxide spacer, in a hole or trench through a memory stack using ALD. Ex. 1009 (Toyama), [0226] (backside trench 79), [0313] (moat trenches 579); Ex. 1024 (U.S. Pat. 9,620,514), 35:51-61 (forming "dielectric spacer" by first forming "silicon oxide layer" via "ALD"); Ex. 1023 (Tessariol), [0063] (ALD), [0038] (conductive vias 58). A POSITA would have been motivated to employ ALD given that Fujiki employs a spacer that was known to be made by conformal

deposition and given that ALD is ideal to deposit thin dielectric layers (which an insulating spacer is). *E.g.*, ALD became popular in large part due to its ability to deposit material conformally for 3D structures. Ex. 1025 (Hwang), 12 ("better conformality over three-dimensional (3D) structures") 13 ("unprecedented conformality over the 3D structures"). And ALD was highly predictable, as it was textbook material and routine to implement before the '254 patent was filed. *Id.*; *see also* Ex. 1009 (Toyama), [0226], [0313]; Ex. 1023 (Tessariol), [0063], [0038]; Lee Decl., ¶¶ 152-57.

Anisotropic Etching

The analysis for claim [5.B] demonstrates that it would have been obvious to remove the bottom portion of the dielectric spacer, thereby enabling formation of Fujiki's through-via that connects to an underlying component. *See* claim [5.B] analysis. Anisotropic etching is an obvious technique to remove that bottom dielectric portion. For example, Nakajima discloses an anisotropic RIE etch to remove the bottom dielectric portion. Nakajima, 7:50-53 (RIE anisotropic etch). Note that directional RIE etches are anisotropic. Ex. 1026 (U.S. Pat. 10,515,799), 6:63-65 ("anisotropic reactive ion etching (RIE)"); Ex. 1027 (U.S. Pat. 9,570,460), 11:55-58 ("RIE or another suitable anisotropic wet or dry etching method"). Lee Decl., ¶¶ 158-60.

A POSITA would have been motivated to employ an anisotropic etch because the etch is directional, and the target portion to remove is at the bottom of a high-aspect ratio hole. Nakajima, 7:50-53 (employing anisotropic etch to remove bottom dielectric portion in high aspect ratio hole). Another benefit is that the directional etch mitigates the risk of etching through the sidewall dielectric. Removing too much of the sidewall dielectric spacer may expose a conductive gate layer, leading to a short circuit. Lee Decl., ¶ 161.

A POSITA would have had a reasonable expectation of success in employing an anisotropic etch. Such etches were routine for this very application. *E.g.*, Nakajima, 7:50-53 (RIE anisotropic etch). And more generally, anisotropic etches were well understood. *E.g.*, Ex. 1042 (Wolf Vol. 1), 32-36 (discussing anisotropic etches); Ex. 1026 (U.S. Pat. 10,515,799), 6:63-65 ("anisotropic reactive ion etching (RIE)"); Ex. 1027 (U.S. Pat. 9,570,460), 11:55-58 ("RIE or another suitable anisotropic wet or dry etching method"); Lee Decl., ¶ 162.

G. Claim 7:

1. [7.PRE] "The method of claim 1, wherein forming the spacer on the sidewall of the first opening comprises:" [7.A] "forming a plurality of shallow recesses by removing parts of the sacrificial layers abutting the sidewall of the first opening;"

Fujiki renders this limitation obvious both under PO's incorrect interpretation and under the correct interpretation.

As an initial matter, the '254 Patent makes clear that these limitations relate to an intentional etch that forms actual recesses in the sacrificial layers. Ex. 1001, 13:47-61, Fig. 3D. For infringement, however, PO interprets this claim to include largely undetectable and unintentional alleged recesses. Ex. 1029 (Ex. A-2, YMTC's Contentions). As is well known, a typical etch through a stack of silicon oxide and silicon nitride layers does not have the exact same selectivity towards each of silicon oxide and silicon nitride, and will result in uneven sidewalls, such that there are recesses in either the oxide layers or the nitride (sacrificial) layers. Ex. 1030 (U.S. Pat. 11,075,084), 2:59-67 (In "3D NAND memory, it is important to have an etching gas which can etch both SiO_2 and SiN layers (or both SiO_2 and p-Si layers) without selectivity. In another words, ***it is a challenge to find an etch gas that has similar high etch rates of SiO_2 and SiN in terms of getting a smooth sidewall*** of high aspect ratio holes in 3D NAND memory."). Thus, under PO's apparent interpretation, these various prior art etches that would form the hole for through-via would create these unintentional "shallow recesses," which may be in the silicon nitride sacrificial layers depending on the etch type. Ex. 1030 (U.S. Pat. 11,075,084), 2:59-67; Lee Decl., ¶ 164.

PO's Incorrect Claim Interpretation

Fujiki discloses etching through a silicon nitride and silicon oxide stack (*see* claim [1.A], [1.C]). And typical prior art etches that were both well known and

beneficial in creating holes through the stack, e.g., for contacts, were also known to result in lateral recesses in either the dielectric spacers or sacrificial layers. Ex. 1030 (U.S. Pat. 11,075,084), 2:59-67. Thus, Fujiki renders this limitation obvious under PO's incorrect claim interpretation, because such unintentional recesses would naturally result from Fujiki's etch. Lee Decl., ¶ 165.

The Correct Claim Interpretation

Fujiki renders this limitation obvious in view of the knowledge of a POSITA. It was well known that an option for a TAC or other through-memory structures was to have a ribbed shape, that is, forming recesses in one of the stack layers. For example, Cui (U.S. Pat. 10,304,852, Ex. 1031) discloses contacts 183 that travel through the staircase and through the entire array. Ex. 1031 (Cui), Fig. 14A, 25:51-53 (e.g., 183 contact on right of region 200); *see also* Ex. 1015 (Kai), 11:9-34 ("laterally recessed"). Cui depicts an embodiment in which the sidewalls of this contact are straight ("cylindrical via cavity"). Ex. 1031 (Cui), Fig. 15A, 25:63-26:22. And it depicts an alternative embodiment that intentionally creates large recesses in the insulating layers ("ribbed via cavity"). *Id.*, Fig. 16A, 26:23-32.

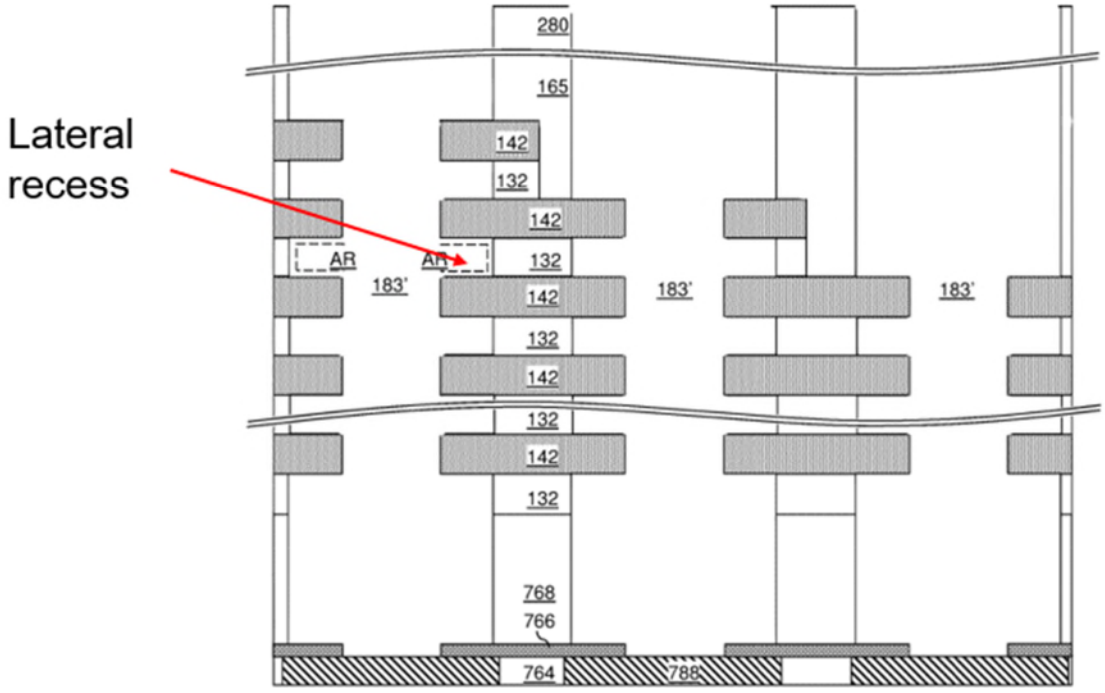


FIG. 16A

Id., Fig. 16A; Lee Decl., Lee Decl., ¶ 166.

The ribbed via cavity serves the same purpose as the '254 Patent, namely, providing additional area for the dielectric liner. Ex. 1001, 13:48-61. In other words, there is additional space for the insulating spacer that surrounds the through-via. Ex. 1031 (Cui), 27:54-28:8. Accordingly, in view of the knowledge of a POSITA, it would have been obvious, and a POSITA would have been motivated, to create a ribbed via cavity in Fujiki's through-array via holes. First, it was known to create lateral recesses to form "rib regions." *Id.*, 26:23-32. This advantageously creates additional area for the insulating spacer. Lee Decl., ¶ 167. Second, there are only two options for creating such rib regions: in the sacrificial (or conductive) gates or

in the dielectric layers. Both were known and result in a common benefit. Ex. 1031 (Cui), Fig. 16A, 26:23-32 (recesses in the insulating layers); Ex. 1015 (Kai), 11:9-34 (recesses in sacrificial gates). Lee Decl., ¶ 168. A POSITA would have had a high expectation of success in forming the rib regions because the isotropic and selective etches were well known. *E.g.*, Ex. 1031 (Cui), 26:33-45; Ex. 1015 (Kai), 11:9-34; Lee Decl., ¶ 169. Indeed, the '254 Patent provides virtually no explanation on how to create these known rib regions. Ex. 1001, 17:46-56.

2. [7.B] "depositing a dielectric layer filling in the shallow recesses and on the sidewall and a bottom surface of the first opening; and"

Fujiki renders this limitation obvious. For the reasons set forth above for claim [7.PRE-A], it would have been obvious to form the shallow recesses in Fujiki's through-via holes, and Fujiki discloses forming a dielectric liner (spacer) in that hole. *See* Claim [5.PRE-5.B]; Lee Decl., ¶ 170. Recall that Fujiki would have been understood to deposit, and at least renders it obvious to deposit, a conformal liner, and thus the liner will fill the shallow recesses. *Id.*

3. [7.C] "removing part of the dielectric layer that is deposited on the bottom surface of the first opening."

Fujiki renders this limitation obvious in view of the knowledge of a POSITA. For the reasons set forth above for claim [7.PRE-B], it would have been obvious to form a liner in the hole with shallow recesses, and Fujiki renders obvious removing

the bottom portion of that dielectric liner (spacer). *See* Claim [5.B]; Lee Decl., ¶ 171.

H. Claim 8:

1. [8] "The method of claim 7, wherein the removal of the part of the dielectric layer comprises isotropic etching on the sidewall and the bottom surface of the first opening."

Fujiki renders this limitation obvious in view of the knowledge of a POSITA.

First, the '254 Patent describes using an isotropic etch because the dielectric material will be thinner on the bottom relative to the sidewalls, thereby allowing for a non-directional etch that removes the bottom oxide before removing the oxide on the sidewalls. Ex. 1001, 14:1-19. It was well known that an isotropic etch is suitable when attempting to remove a material from an area (here, oxide on the bottom) if there is less material on that area relative to the other areas in which the etch chemical will contact. *E.g.*, Ex. 1044 (U.S. Pat. 10,714,341), 1:48-62 ("Furthermore, since the sacrificial material is removed using an isotropic etch process, the use of a thick sacrificial material, which is needed to form a thick metal film on the substrate, will require the formation of a large lateral overhang, since the vertical etch rate of the sacrificial material is the same as lateral etch rate of the sacrificial material."). That difference in the material thickness is what makes the non-directional isotropic etch suitable. Lee Decl., ¶ 173.

Second, the benefits and tradeoffs between isotropic (non-directional) and anisotropic (directional) were textbook material decades before the filing of the '254 Patent. *E.g.*, Ex. 1042 (Wolf Vol. 1), 32-36 (isotropic and anisotropic etching). For example, isotropic etch does not pose the same potential damage issues as anisotropic etches. *Id.*; Lee Decl., ¶ 174.

Third, claims [5.PRE-B] and [6] describe various deposition techniques, including the desire to deposit conformal layers. If a deposition, however, leaves significantly less oxide on the bottom, then the above illustrates the obvious application and benefits from an isotropic etch. This claim does nothing more than recite a condition (from a non-conformal deposition) from which it would have been obvious in view of decades-old textbook to employ an isotropic etch. Lee Decl., ¶ 175.

A POSITA would have had a high expectation of success, because isotropic etches were generally well known, including for this very application. *E.g.*, Ex. 1042 (Wolf Vol. 1), 32-33 (isotropic etching); Lee Decl., ¶ 176.

I. Claim 9:

1. [9.PRE] "The method of claim 1, wherein forming the first opening comprises:" [9.A] "simultaneously etching the first opening through the stack, a second opening outside of the stack, and a third opening through the stack,"

Fujiki renders these limitations obvious in view of the knowledge of a POSITA.

First, as the claim [3] analysis explains, Fujiki discloses, or renders obvious, simultaneously etching the hole for the through-via ("a first opening") and the holes for 82 or 83 contacts (either "a second opening") at the same time, including the first hole (for the through-via, i.e., TAC) all the way through the stack and the second opening (for the 82 or 83 contact) outside the stack.

Second, the claim [2] analysis demonstrates that it would have been obvious to further etch dummy holes, including dummy channel holes. Such a hole through the array constitutes a "third hole."

Third, for the same reasons as claim [3], it would have been obvious to etch all these holes at the same time, because it was well known that such simultaneous etching saves processing time. Lee Decl., ¶ 179. Also note that the ability to form memory openings, such as dummy memory openings, and contact openings at the same time was also well known and provides the same benefit of saving process time. The claim 3 analysis demonstrates this with respect to Kai II:

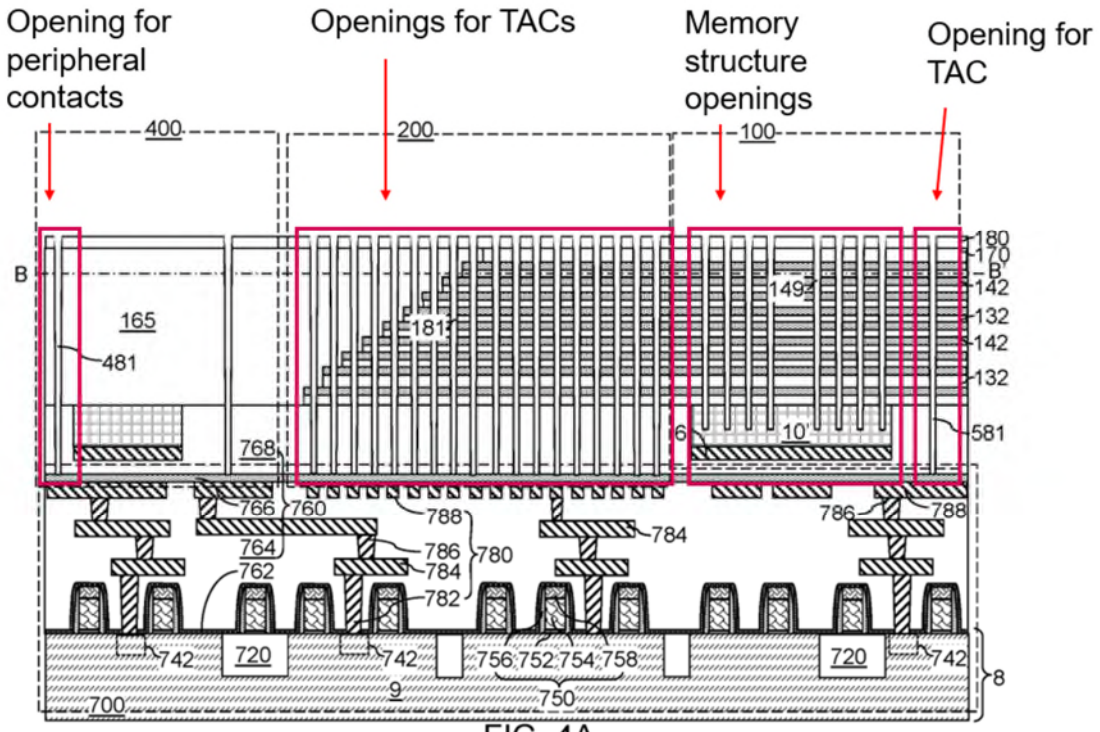


FIG. 4A

Ex. 1038 (Kai II), Fig. 4A, 17:30-44 ("The pattern of openings in the photoresist layer can be transferred through the inter-tier dielectric layer 180 and the first-tier structure (132, 142, 170, 165) and into the in-process source-level material layers 10´ and the at least one second dielectric layer 768 by a first anisotropic etch process to form the various first-tier openings (149, 181, 481, 581) concurrently, i.e., during the first anisotropic etch process. The various first-tier openings (149, 181, 481, 581) can include first-tier memory openings 149, first-tier staircase-region openings 181, first-tier array-region openings 581, and first-tier peripheral-region openings 481.").

Note that the claim 2 analysis demonstrates that forming dummy openings can use the same process as forming memory channel openings, and thus Kai II demonstrates forming dummy openings at the same time as contact openings. Kai, for example, confirms the knowledge of a POSITA. Ex. 1015 (Kai), 9:23-26 (defining "support opening" as "a structure in which a support structure (such as a support pillar structure) that mechanically supports other elements is subsequently formed"), 9:45-48 ("support openings 19" extend through stack), 10:20-27 (forming channels in support openings); Ex. 1016 (Park), 6:19-26, 7:45-51 (same); Ex. 1017 (Kim), [0047], [0071], [0072] (same); Lee Decl., ¶¶ 180-81.

2. [9.B] "wherein a lateral dimension of the third opening is smaller than lateral dimensions of the first and second openings."

Fujiki renders this limitation obvious in view of the knowledge of a POSITA.

To start, the lateral dimensions of via structures typically get smaller towards the array, because the array contains millions or billions of channel structures. Lee Decl., ¶ 183. Fujiki demonstrates this below:

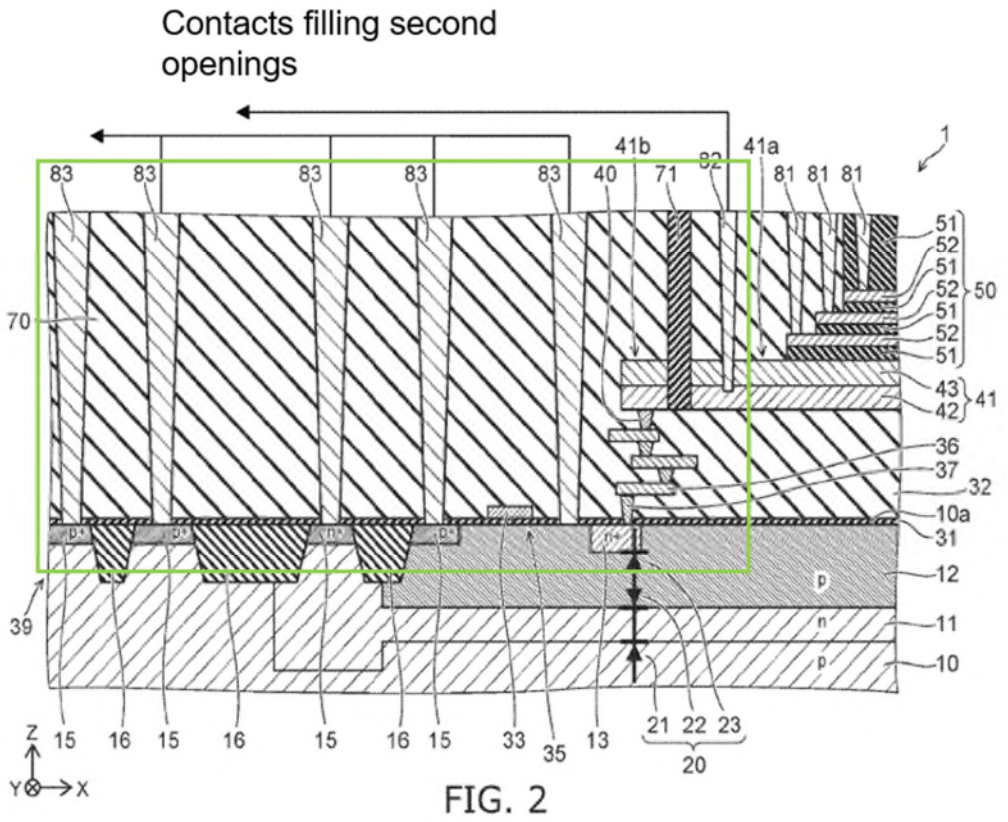
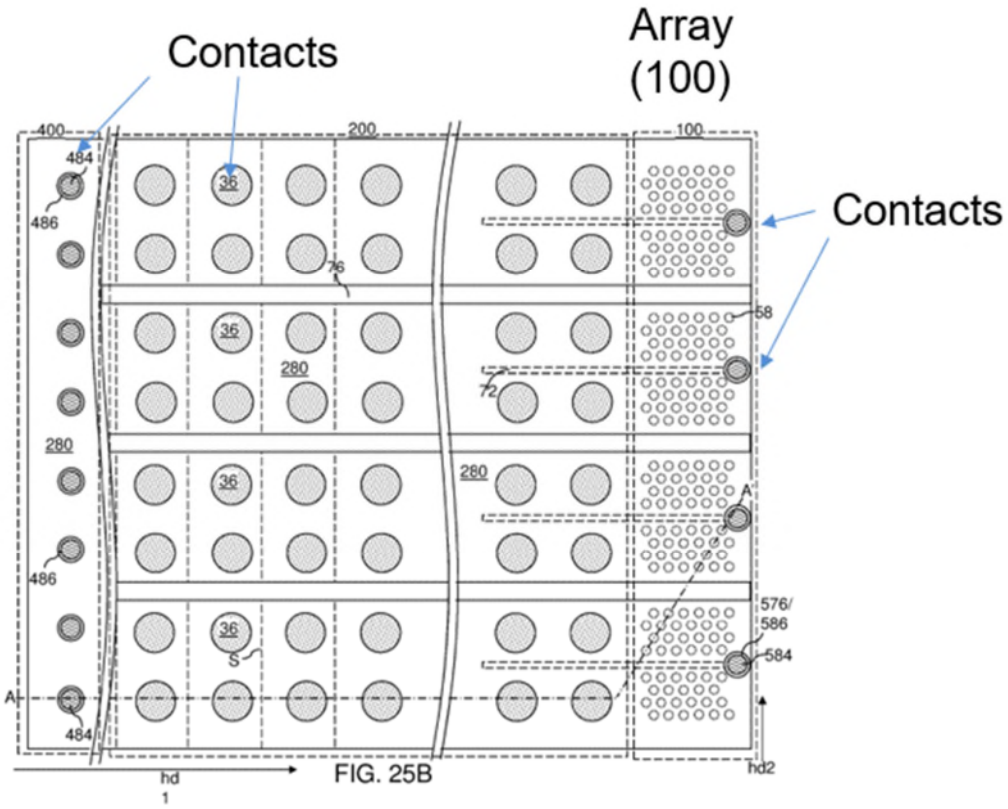


FIG. 2

Ex. 1006 (Fujiki), Fig. 2. Thus, it would have been obvious that the second hole, which is outside of the array, can have the largest lateral dimension, consistent with Fujiki's figure 2. Outside the array, there is more room to operate without creating issues, such as short circuits, so using larger structures (e.g., that have less resistance) is possible and desirable due to larger process margins Lee Decl., ¶ 183. It was also common to make contacts the same size. Ex. 1043 (Wolf Vol. 2), 47.

Importantly, it would have been obvious that the third hole will have the smallest lateral dimensions. Per the claim [9.A] analysis, the third hole is a dummy hole, e.g., a dummy channel hole. Channel holes are miniscule in size relative to

contacts (the first and second holes). Dummy channel holes will generally have the same size as channel holes to maintain a uniform pattern and reduce the edge effect issues (that is, repeating the uniform pattern). For example, below is a top-down view showing channel structures in region 100 versus various contacts in regions 200 and 400:



Ex. 1031 (Cui), Fig. 25B; Lee, ¶ 184.

A POSITA would have understood the above figure to illustrate that features in the dense array are relatively smaller than features in the less dense peripheral region. Lee Decl., ¶ 184. Also note the height difference of the features in Figure 2 above. The contacts 83 are longer than contacts 82, and as a natural result of etches

that create tapered holes (as shown in Figure 2), the lateral width at the top of the contact is naturally wider than at the bottom and the size of the top of the contact will therefore grow with the depth to maintain a minimum opening size at the bottom. *Id.* Further, the third holes are dummy holes. This means that an active structure, such as a channel structure, will not fill the dummy hole. As a result, such features do not present process margin issues, and employing smaller feature (namely, a smaller lateral dimension) is not an issue. For example, as claim [10] demonstrates, a simple insulator fill may occupy the dummy hole.

J. Claim 10:

1. [10.PRE] "The method of claim 9, wherein forming the spacer on the sidewall of the first opening comprises:" [10.A] "depositing a dielectric layer (i) fully filling in the third opening to form a dummy channel structure and (ii) partially filling in the first opening and the second opening; and"

Fujiki renders this limitation obvious in view of the knowledge of a POSITA.

First, the claim [1.D] analysis demonstrates that Fujiki discloses depositing a dielectric liner in the first opening.

Second, while Fujiki says little about the peripheral contacts (which are in the second opening), it would have been obvious to include a liner, because regardless of its location, it would have been standard practice to include a liner so that the same process can be used to make each contact, as shown below:

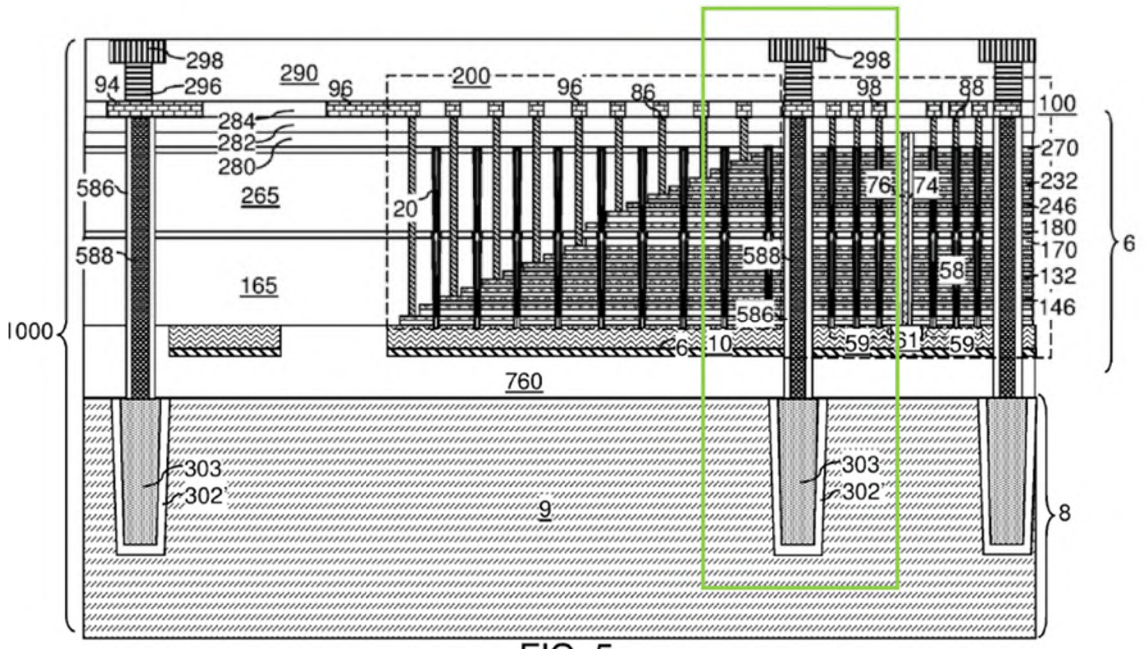


FIG. 5

Ex. 1010 (Mushiga), 10:31-58, Fig. 5 (588). This was known to be beneficial, because a single deposition step could be used for all holes, and it was routine because it simply involved not masking the holes during the deposition of the spacers. Lee, ¶ 187. More importantly, Fujiki does not detail its entire 3D NAND. In typical 3D NAND, various contacts may need to travel through conductive elements before reaching the target depth, and in such cases, dielectric liners are necessary to prevent short circuiting the contact to other elements. For example, the contacts below show connections through the substrate to underlying elements:

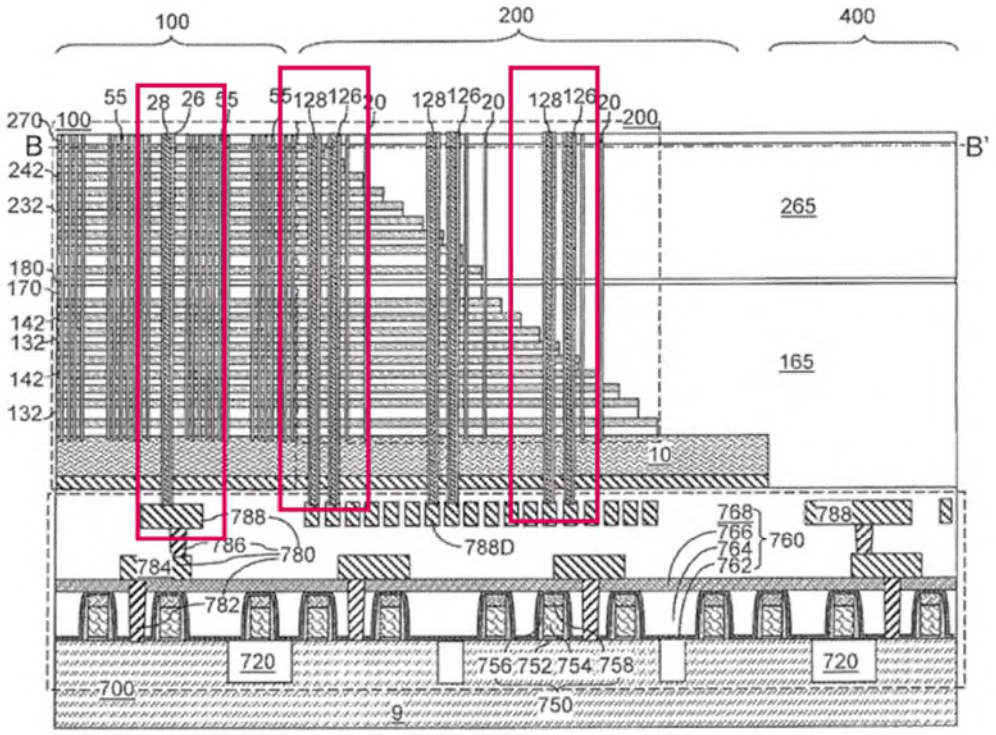


FIG. 8A

Ex. 1019 (U.S. Pat. 10,115,632), Fig. 8A, 17:51-54; Lee, ¶ 188.

Third, one way to fill a dummy hole was to completely fill it with an oxide, here the insulating liner. As the claim [2] analysis demonstrates, one known beneficial use of dummy structures was as support pillars. A common support pillar was a solid dielectric, e.g., oxide, pillar. Ex. 1032 (U.S. Pat. 9,793,139), 15:21-36 ("dielectric support pillar 7P"). A known benefit of the complete fill was that it provides more support relative to partial fill. *Id.*; Lee, ¶ 189.

2. [10.B] "removing parts of the dielectric layer that are deposited on a bottom surface of the first opening and on a bottom surface of the second opening."

Fujiki renders this limitation obvious in view of the knowledge of a POSITA.

The claim [5.B] analysis demonstrates that Fujiki renders obvious removing the bottom portion of the dielectric spacer, and it would have been obvious to do so for each contact, so that the proper interconnection path can be made with electrical coupling between components above and below the array. Lee, ¶ 190.

K. Claim 11:

1. [11.PRE] "A method for forming a three-dimensional (3D) memory device, comprising:"

This limitation is identical to claim [1.PRE] and Fujiki discloses it for the same reasons.

2. [11.A] "forming a stack comprising a plurality of dielectric/sacrificial layer pairs on a substrate;"

This limitation is identical to claim [1.A] and Fujiki discloses it for the same reasons.

3. [11.B] "forming a channel structure extending vertically through the stack;"

This limitation is identical to claim [1.B] and Fujiki discloses it for the same reasons.

4. [11.C] "forming a dummy channel structure extending vertically through the stack;"

Fujiki renders obvious forming a dummy channel structure that extends vertically through the stack for the reasons set forth in claim [2].

5. [11.D] "simultaneously etching a first opening through the stack and a second opening outside of the stack;"

This limitation is present in claim [3], and Fujiki discloses it, or renders it obvious, for the same reasons.

6. [11.E] "simultaneously forming a first spacer on a sidewall of the first opening and a second spacer on a sidewall of the second opening;"

The analysis of claims [3]-[4] demonstrates that Fujiki discloses, or renders obvious, forming the through-vias and 82 or 83 contacts at the same time, and thus forming the spacers in the first hole (for the through-via) and second hole (either for contact 82 or 83) at the same time. The analysis under claim [10.PRE-A] demonstrates that it would be obvious to form spacers on both the through-via holes and peripheral contacts 82 or 83 as well. Lee Decl., ¶ 197.

7. [11.F] "depositing a conductor layer (i) filling in the first opening to form a through array contact (TAC) and (ii) filling in the second opening to form a peripheral contact; and"

This limitation is substantively the same as claim [4] (but recites "depositing" instead of "filling," which is an inconsequential difference), and Fujiki discloses it, or renders it obvious, for the same reasons (as shown it completely fills the hole). Indeed, decades before the filing of the '254 Patent, techniques to complete fill contact holes, e.g., with tungsten, to obtain the benefits thereof were well known. *E.g.*, Ex. 1043 (Wolf Vol. 2), 52, 135; Lee Decl., ¶ 199.

8. [11.G] "after forming the TAC and peripheral contact, forming a slit extending vertically through the stack."

This limitation is substantively the same as claim [1.F] (the above demonstrates it would have been obvious to form all TACs at the same time), and Fujiki discloses it for the same reasons.

L. Claim 12:

1. [12.PRE] "The method of claim 11, wherein forming the first spacer on the sidewall of the first opening comprises:"

2. [12.A] "depositing a dielectric layer on the sidewall and a bottom surface of the first opening; and"

3. [12.B] "removing part of the dielectric layer that is deposited on the bottom surface of the first opening."

These limitations are substantively the same as claim [5.PRE-B] ("first spacer" here refers to the TAC through the array of claim 5), and Fujiki discloses them for the same reasons.

M. Claim 13:

1. [13] "The method of claim 12, wherein the deposition of the dielectric layer comprises atomic layer deposition (ALD), and the removal of the part of the dielectric layer comprises anisotropic etching on the bottom surface of the first opening."

This limitation is identical to claim [6], and Fujiki renders it obvious for the same reasons.

N. Claim 14:

1. [14.PRE]-[14.C]

These limitations are effectively identical to claim [7.PRE-7C], and Fujiki renders them obvious for the same reasons. These limitations recite "first" to require that the steps apply to the TAC. Claim 7's steps are on the TAC.

O. Claim 15:

1. [15] "The method of claim 14, wherein the removal of the part of the dielectric layer comprises isotropic etching on the sidewall and the bottom surface of the first opening."

This limitation is identical to claim [8], and Fujiki renders it obvious for the same reasons.

P. Claim 17:

1. [17] "The method of claim 11, wherein the dielectric layers in the dielectric/sacrificial layer pairs comprise silicon oxide, the sacrificial layers in the dielectric/sacrificial layer pairs comprise silicon nitride, and the first and second spacers comprise silicon oxide."

Fujiki renders this limitation obvious in view of the knowledge of a POSITA.

On substrate 10, Fujiki forms "stacked body 50 … by alternately depositing the insulating films 51 made of silicon oxide and insulative sacrificial films 91 made of silicon nitride (SiN)." Fujiki, [0050].

Fujiki discloses that "[a]n insulating film 79 that is made of, for example, silicon oxide is provided at the periphery of the through-via 78." Fujiki, [0042].

Recall that the analysis of claims [3]-[4], [10.PRE-A] demonstrates that Fujiki discloses, or renders obvious, forming the through-vias and 82 or 83 contacts at the same time, including the spacers (here, silicon oxide). Lee Decl., ¶ 208.

Q. Claim 18:

1. [18.PRE] "A method for forming a three-dimensional (3D) memory device, comprising:"

This limitation is identical to claim [1.PRE], and Fujiki discloses it for the same reasons.

2. [18.A] "forming a stack comprising a plurality of dielectric/sacrificial layer pairs on a substrate;"

This limitation is identical to claim [1.A], and Fujiki renders it obvious for the same reasons.

3. [18.B] "forming a channel structure extending vertically through the stack;"

This limitation is identical to claim [1.B], and Fujiki renders it obvious for the same reasons.

4. [18.C] "simultaneously etching a first opening through the stack, a second opening outside of the stack, and a third opening through the stack, wherein a lateral dimension of the third opening is smaller than lateral dimensions of the first and second openings;"

This limitation is identical to claim [9.A-B], and Fujiki renders it obvious for the same reasons. Technically, these limitations refer to "a first opening" instead of "the first opening," but refer to the same element.

5. [18.D] "depositing a dielectric layer (i) fully filling in the third opening to form a dummy channel structure and (ii) partially filling in the first opening and the second opening;"

This limitation is identical to claim [10.A], and Fujiki renders it obvious for the same reasons.

6. [18.E] "removing parts of the dielectric layer that are deposited on a bottom surface of the first opening and on a bottom surface of the second opening;"

This limitation is identical to claim [10.B], and Fujiki renders it obvious for the same reasons.

7. [18.F] "depositing a conductor layer (i) filling in the first opening to form a through array contact (TAC) and (ii) filling in the second opening to form a peripheral contact; and"

This limitation is virtually identical to claim [4], and Fujiki discloses it, or renders it obvious, for the same reasons (again, this claim recites "a conductor layer" instead of "the conductive layer" and recites "filling") (as shown Fujiki completely fills the hole).

8. [18.G] "after forming the TAC and peripheral contact, forming a slit extending vertically through the stack."

This limitation is substantively the same as claim [1.F] but also recites forming the slit after the peripheral contact. As the above illustrates, Fujiki renders obvious forming these contacts at the same time, and thus the claim [1.F] analysis

demonstrates that Fujiki discloses it is obvious for the same reasons, because Fujiki discloses forming the slit after the through-via contacts.

R. Claim 20:

1. [20] "The method of claim 18, further comprising prior to etching the first, second, and third openings, forming a staircase structure at one side of the stack."

Fujiki discloses this limitation.

Right after making the stack, and before etching contact holes, Fujiki discloses forming the staircase. Fujiki, [0050].

XI. SECONDARY CONSIDERATIONS

Petitioner is unaware of any applicable secondary considerations of nonobviousness. None were identified during prosecution. *See* generally Ex. 1002 (the '254 FH). Even if such considerations existed, none would overcome the strong *prima facie* showing of obviousness.

XII. CONCLUSION

Petitioner respectfully requests that the Board enter a final written decision finding the Challenged Claims unpatentable.

Respectfully submitted,

Dated: November 7, 2024 ORRICK, HERRINGTON & SUTCLIFFE LLP

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CERTIFICATE OF COMPLIANCE

The undersigned certifies that the foregoing PETITION FOR *INTER PARTES* REVIEW complies with the type volume limitation in 37 C.F.R. §42.24(a). According to the utilized word-processing system's word count, the petition—excluding the caption, table of contents, table of exhibits, mandatory notices, certificate of word count, and certificate of service—contains 12,083 words.

Dated: November 7, 2024

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CERTIFICATE OF SERVICE

The undersigned hereby confirms that the foregoing Petition for *Inter Partes* Review and associated documents and exhibits were caused to be served on November 7, 2024 via overnight courier upon the following counsel of record for Patent Owner:

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