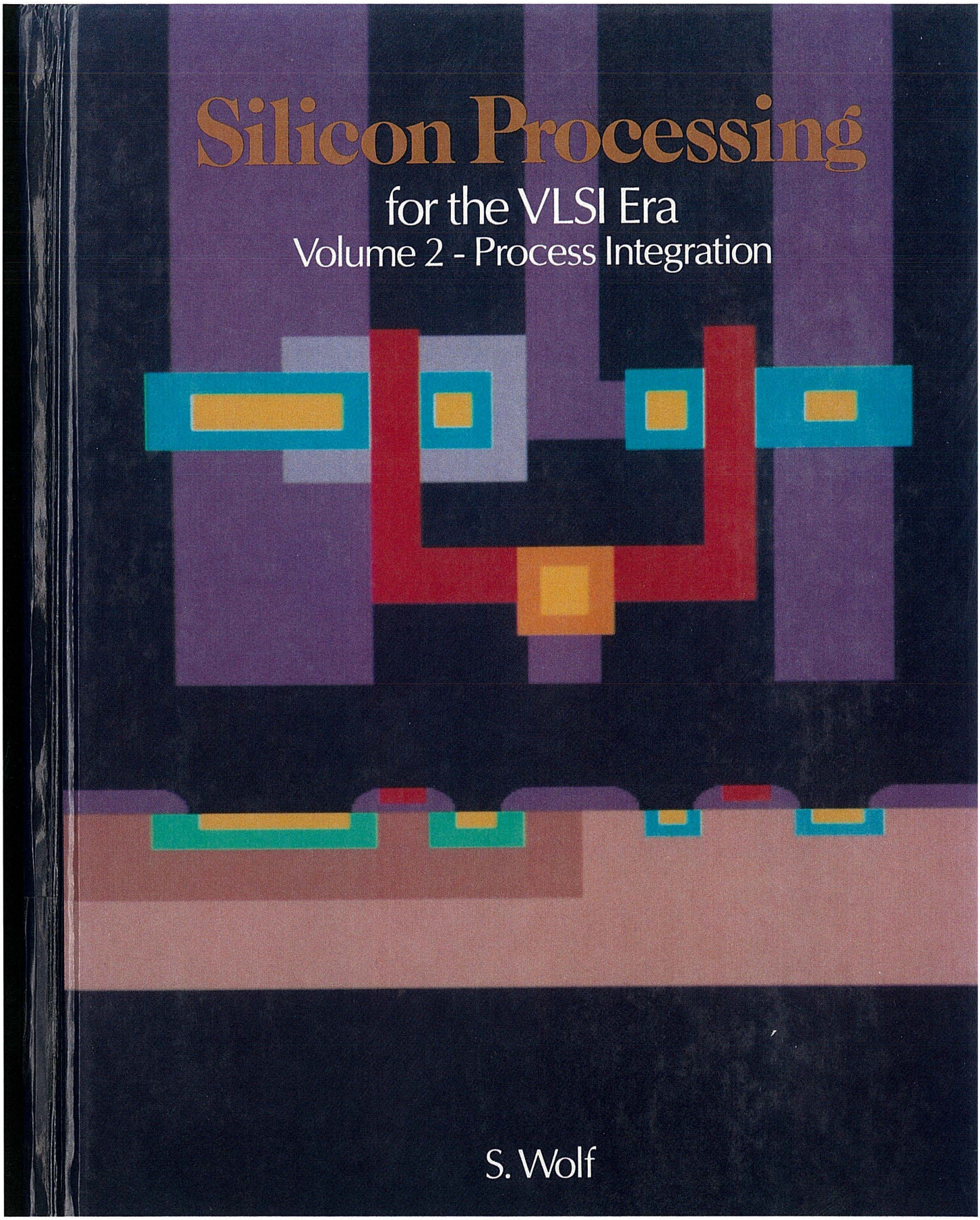
Silicon Processing

for the VLSI Era

Volume 2 - Process Integration



S. Wolf

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SILICON PROCESSING

FOR

THE VLSI ERA

VOLUME 2:

PROCESS INTEGRATION

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THE VLSI ERA

VOLUME 2:

PROCESS INTEGRATION

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Sunset Beach, California

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Published by:

Lattice Press,
Post Office Box 340
Sunset Beach, California 90742, U.S.A.

Cover design by Roy Montibon, Visionary Art Resources, Inc., Santa Ana, CA.

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Library of Congress Cataloging in Publication Data
Wolf, Stanley

Silicon Processing for the VLSI Era
Volume 1 : Process Integration

Includes Index
1. Integrated circuits-Very large scale integration. 2. Silicon. I. Title

86-081923

ISBN 0-961672-4-5

9 8 7 6 5

PRINTED IN THE UNITED STATES OF AMERICA

To my wife, Carrol Ann,
and my children, Jennifer Laura and Stanley Charles Ross

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CHAPTER 3

CONTACT TECHNOLOGY AND LOCAL INTERCONNECTS FOR VLSI

When silicon integrated circuits are fabricated, isolated active-device regions are created within the single-crystal substrate (see chap. 2). The technology used to connect these isolated devices through specific electrical paths employs high-conductivity, thin-film structures, fabricated above the SiO_2 insulator that covers the silicon surface. Wherever a connection is needed between a conductor film and the Si substrate, an opening in the SiO_2 must be provided to allow such *contacts* to occur.

Interconnections in *ideal* electric circuits are assumed to exhibit zero impedance to the flow of electric current. Although the finite impedance of *real* conductor structures can be ignored in some applications, in others such parasitic effects can significantly impact circuit performance, and must therefore be considered during circuit analysis or design. The same is true with integrated circuits. The electrical characteristics of interconnects and contacts must be studied in order to determine under what circumstances their parasitic behavior can significantly impact circuit performance.

In this chapter we will focus primarily on *ohmic contacts* between metal or metal-silicide thin films and single-crystal silicon substrates. We will also briefly describe metal-Si Schottky contacts, polysilicon-to-single-crystal Si contacts, and local-interconnect technology. The topics of metal-to-metal and metal-to-metal-silicide contact properties will be covered in chapter 4.

3.1 THE ROLE OF CONTACT STRUCTURES IN DEVICE AND CIRCUIT BEHAVIOR

Parasitic resistances exist in the path between the metal-to-Si substrate interface and the region in the device where the actual transistor action begins. In this chapter we are concerned with the processing of metal-silicon contact structures, and thus are interested in the fraction of this device parasitic resistance due to the contacts. In order to see how

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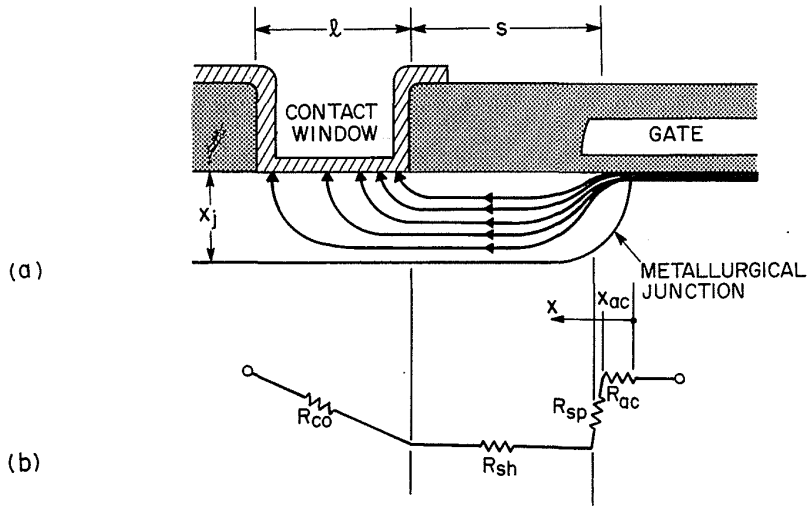

Fig. 3-1 Schematic drawing showing (a) current paths within the source and drain regions, of a planar MOSFET and (b) their corresponding representative series resistance components.[84] (© 1986 IEEE).

this part of the parasitic resistance is extracted from the total value, the physical structure of planar MOSFETs and bipolar transistors must be examined.

3.1.1 Contact Structures in Planar MOSFETs and Bipolar Transistors

In the planar MOSFET, the device region in which transistor action occurs is the *channel region under the gate.* The current flowing from the metal-interconnect lines to these channel regions must be transported from the metal-Si contact to the edge of the channel through the source or drain regions (Figs. 3-1 and 5-1). In the planar bipolar transistor, the region of transistor action is the *intrinsic-base region.* Base current from the external circuit must be transported from the base contact through the extrinsic-base region to reach the intrinsic base (Fig. 3-2).

In the MOSFET, current enters the contact perpendicular to the wafer surface, and then travels parallel to the surface in order to reach the channel. The parasitic series resistance, R_S, of the current path from the contact to the edge of the channel can be modeled by the sum of four components,

$$R_S = R_{co} + R_{sh} + R_{sp} + R_{ac} \qquad (3\text{-}1)$$

where R_{co} is the contact resistance between the metal and the source/drain region, R_{sh} is the sheet resistance of the bulk region of the source and drain, R_{sp} describes the resistance of the current lines crowding near the channel end of the source, and R_{ac} is the accumulation-layer resistance. Qualitatively, for a nonabrupt junction, R_{ac} and R_{sp}

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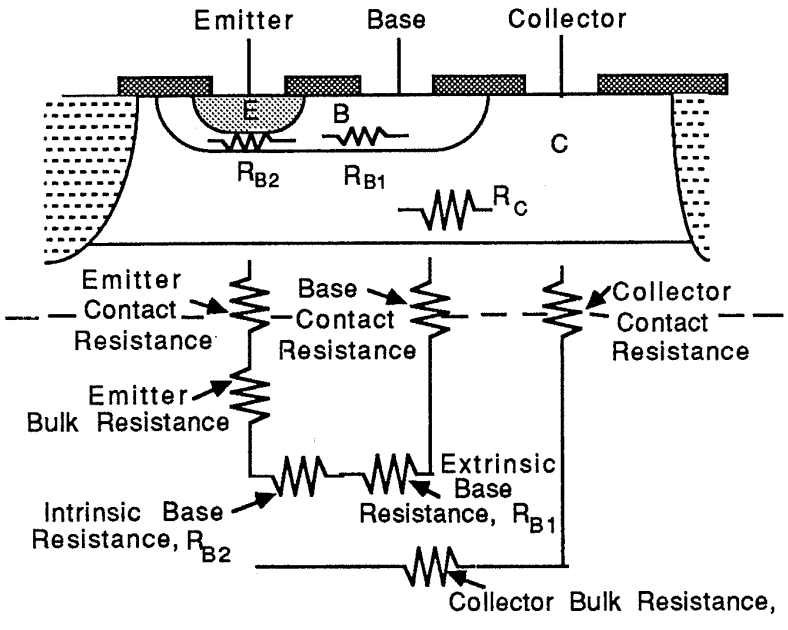

Fig. 3-2 Schematic drawing of the parasitic series-resistance components in planar bipolar transistors.

arise because, after leaving the channel, the current does not immediately spread into the bulk of the source-drain regions (the parasitic resistance effect in these bulk regions is R_{sh}). Thus R_{ac} and R_{sp} exist because the accumulation-layer conductance is much higher than the semiconductor conductance in the vicinity of the junction.

In the *planar bipolar transistor*, the series resistance of the base region, R_B, is the sum of the contact resistance, R_{co}, and the resistance of the current path of the extrinsic base, R_{B1}, and the intrinsic base, R_{B2} (Fig. 3-2). Again, the base current enters the base contact perpendicular to the wafer surface but must travel parallel to the wafer surface in order to reach the intrinsic-base region. The emitter current experiences a series resistance that is basically due only to the contact resistance of the emitter contact because the emitters are so shallow. In this case the current flow is perpendicular to the wafer surface.

We will quantitatively describe the impact of R_S on the device and circuit behavior of MOS devices in detail later in this chapter. (The effect on bipolar devices will be described in chap. 7.) At this point we merely want to make the point that R_{co} is always one of the parasitic-series-resistance components whenever metal-to-semiconductor contacts are made. In addition, as semiconductor device dimensions shrink both vertically and laterally, device currents and current densities increase. Hence, if the metal-to-semiconductor contact area is also scaled, R_{co} also increases. Since this may significantly degrade device performance, techniques for accurately determining R_{co} need to be available (both from measurements and by simulation).

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3.2 THEORY OF METAL-SEMICONDUCTOR CONTACTS

Ideal nonrectifying contacts would exhibit no resistance to the flow of current in either direction through the contact, and their I-V characteristic would appear as shown in Fig. 3-3a. In general, however, when metal-to-semiconductor contacts are fabricated, they possess *non-ohmic* I-V characteristics (Fig. 3-3b). Nevertheless, it is possible to fabricate contacts with electrical characteristics that approach those of the ideal. We will refer to real metal-semiconductor contacts as low-resistance *ohmic contacts* if they exhibit a near-linear current-voltage characteristic in both directions of current flow, and negligible resistance when compared to the bulk resistance (Fig. 3-3c). It is the ohmic contact that is normally fabricated for the purpose of interconnecting devices in an IC. Non-ohmic, rectifying metal-semiconductor contacts (*Schottky contacts*) find some application in ICs, and they are described in section 3.7.

The reason that metal-semiconductor contacts generally exhibit non-ohmic I-V characteristics is that the work functions of the metal and the semiconductor (φ_m and φ_s) are not equal, and in most metal-silicon contacts φ_m is greater than φ_s (Fig. 3-4a). When such metal and semiconductor materials are in contact at equilibrium (i.e., no current flows), the Fermi level must be constant throughout the system (which in this case includes both materials). If φ_m is not equal to φ_s, a potential-energy barrier must exist between the metal and the semiconductor at equilibrium, and the height of this barrier, $q\varphi_b$ (assuming $\varphi_m > \varphi_s$) is given by:

$$q\varphi_b = q(\varphi_m - \chi_s) \qquad (3-2)$$

where χ_s is the electron affinity of the semiconductor (Fig. 3-4b). The effect of the barrier on current flow under bias is similar to that of the barrier that exists in a *pn* junction; hence the I-V characteristic of a metal-semiconductor contact, in general, exhibits rectifying properties that are essentially like those of a *pn* junction.

For an ohmic-contact structure to be created, the effect of the barrier on carrier flow must be made negligible. In theory, this could be achieved by making φ_b very small

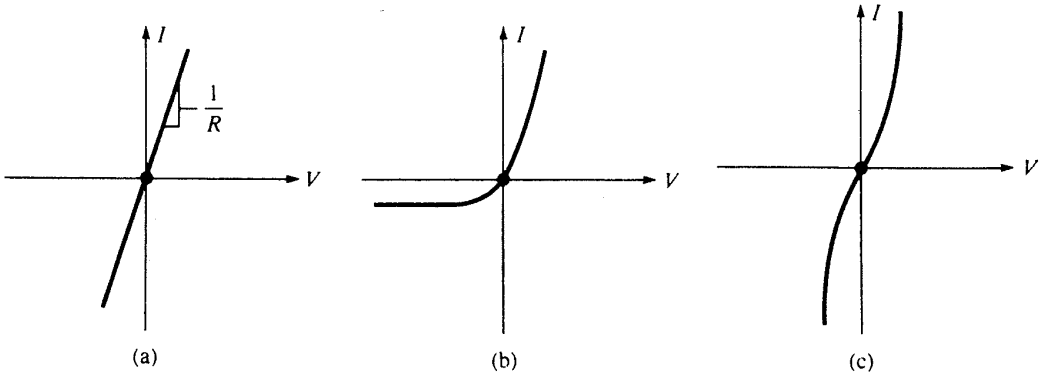

Fig. 3-3 I-V characteristics of contacts between metal and semiconductor in integrated circuits. (a) Ideal ohmic contact. (b) Rectifying contact. (c) Practical nonlinear "ohmic" contact.

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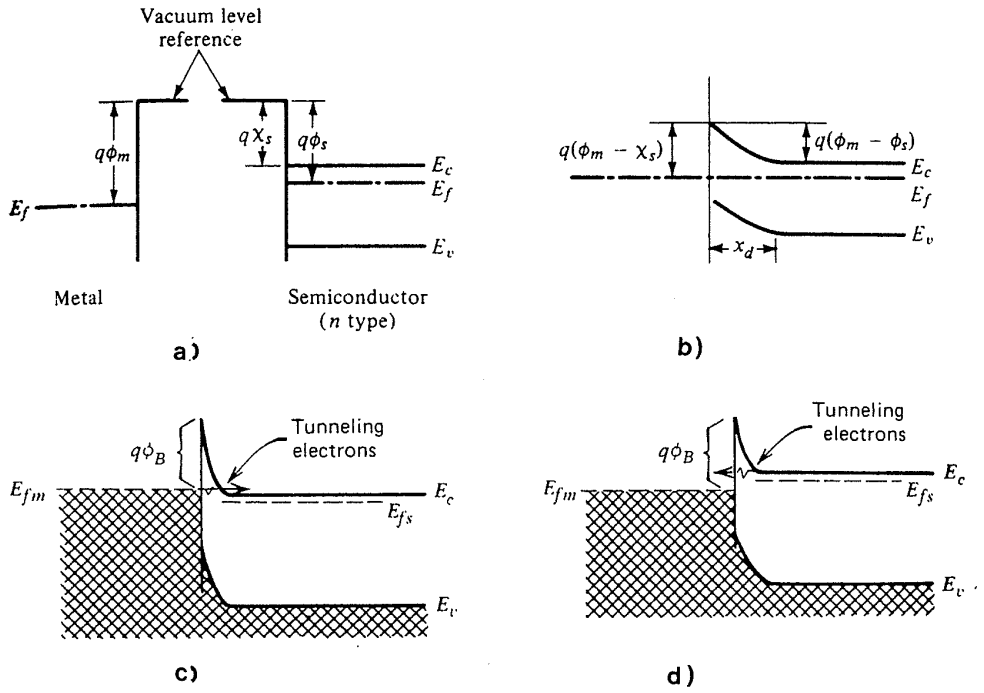

Fig. 3-4 Energy band diagram of a metal-semiconductor contact with $\phi_m > \phi_s$: (a) before contact and (b) after contact and at thermal equilibrium.[130] From E. S. Yang, *Microelectronic Devices*. Copyright 1988 McGraw-Hill. Reprinted with permission. Metal-semiconductor barrier with a thin space-charge region through which tunneling can take place. (c) tunneling from metal to semiconductor, (d) tunneling from semiconductor to metal. From R. S. Muller and T. I. Kamins, 2nd Ed., *Device Electronics for Integrated Circuits*. Copyright 1986, John Wiley & Sons. Reprinted with permission.

(i.e., by using a metal that would give a low φ_b when in contact with Si). Most carriers would then have enough energy to overcome the barrier, and current would flow easily when a bias was applied. Unfortunately, this is not a viable option in Si devices, because the smallest value of φ_b for a metal-to-*n*-type Si contact is about 0.5 V. Such large values of φ_b end up yielding contact-resistance values on lightly doped *n*-type Si that are far too large to be of practical use for ohmic contacts to MOS or bipolar devices.

Another approach would be to use a heavily doped n^+ or p^+ surface in the silicon. This technique is effective since the charge transport across a metal-semiconductor contact can be indirectly influenced by the doping concentration in the semiconductor. That is, when the doping concentration is low ($N_D < 10^{19}$ cm^{-3}), only carriers that have energies greater than the barrier height can overcome the barrier (i.e., through the phenomenon of thermionic emission). If the doping concentration exceeds this value, carrier transport becomes dominated by *quantum-mechanical tunneling* (i.e., the carriers go *through* the potential barrier).

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Significant tunneling between two regions can occur if the width of the potential-energy barrier that separates them is small. At a metal-silicon interface, the width of the potential energy barrier is essentially equal to that of the depletion-region width in the semiconductor, W. When the silicon is heavily doped, W is very thin - only a few nanometers thick. (The following relation is used to compute W: $W = \sqrt{2\,\varepsilon_s\,\varphi_i/qN_D}$, where φ_i is the voltage across the space charge region of the semiconductor, and N_D is the dopant concentration.) For such small values of W, carriers with less energy than the barrier height are still able to pass through the barrier in either direction by the mechanism of tunneling.

As shown in Fig. 3-4c, if the metal is biased negatively with respect to the semiconductor, electrons in the metal can tunnel through the barrier to the lower-energy conduction-band states in the semiconductor. Similarly, if the metal is biased positively with respect to the semiconductor, the electrons from the semiconductor can tunnel into the lower-energy electronic states in the metal (Fig. 3-4d). Thus, an essentially symmetrical I-V curve for both forward and reverse bias is realized. In addition, since there is a high electron concentration in both the metal and the conduction band of a heavily doped semiconductor, many electrons are available to take part in these processes. Consequently, currents increase very steeply as bias is applied, and low-resistance contacts can be achieved.

The physical parameter that characterizes the incremental resistance of a metal-to-semiconductor interface is the *specific contact resistivity*, ρ_c. That is, ρ_c is a measurement-independent quantity that describes the incremental resistance of an infinitely small area of such an interface. The units of ρ_c are therefore V-cm^2/A or Ω-cm^2. The values of ρ_c are commonly expressed in these units, or their equivalent, Ω-μm^2. Since ρ_c of the ohmic contacts used in IC technology is typically in the 10^{-6}-10^{-8} Ω-cm^2 range (and 1 μm = 10^{-4} cm), the latter units are often considered more convenient. (Of course, the goal is to fabricate ohmic contacts with as small a value of ρ_c as possible.)

The contact resistance, R_{co}, on the other hand, is a macroscopic quantity that depends not only on ρ_c, but also on the contact size, the semiconductor sheet resistance, and the contact geometry. Since ρ_c is the single measurement-independent parameter that describes the quality of the interface, it is the proper parameter on which to focus attention when seeking to optimize a contact structure. The following section describes techniques that allow ρ_c to be extracted from measurements of special contact test structures. In the present section we consider how material parameters can be quantitatively varied to produce contacts with minimum values of ρ_c.

The values of ρ_c derived from experimental measurements are found to be well modeled by the theoretical expression

$$\rho_c \approx \exp\left(\frac{4\pi\sqrt{\varepsilon_{si} m_e \varphi_b}}{h\sqrt{N_D}}\right) \qquad (3\text{-}3)$$

where m_e is the *tunneling effective mass*. In Figure 3-5, this equation is plotted for φ_b = 0.85, 0.6, and 0.5 eV and for various doping levels in the silicon substrate.[1] In addition, experimental data points for Al-*n*Si and for PtSi-*n*Si contacts (where φ_b = 0.72

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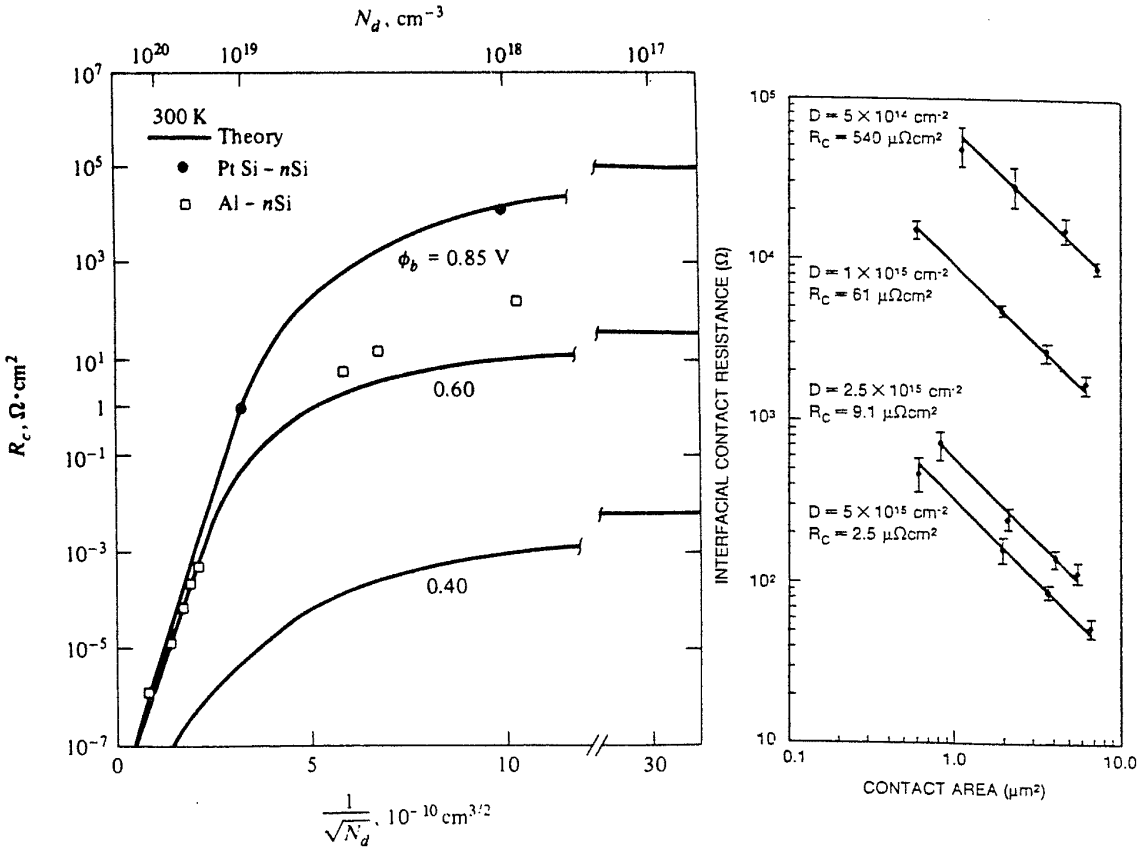

Fig. 3-5 (a) Theoretical and experimental values of specific contact resistance.[1] (© 1971 Solid State Electronics). (b) Specific contact resistivity vs. implant dose.[2] (© 1985 IEEE).

eV and 0.84 eV, respectively) are also plotted. It can be seen that Eq. 3-3 quite accurately predicts the measured values of ρ_c as a function of doping. For doping concentrations of $N_D > 10^{20}$ cm^{-3}, it is predicted that ρ_c values as low as $\approx 10^{-7}$ Ω-cm^2 can be obtained.

In practice, the doping concentration in the silicon can be increased through diffusion and/or ion-implantation methods. Figure 3-5b plots the value of ρ_c versus increases in implant dose into *n*-type Si.[2] It can be seen that ρ_c decreases inversely with the square root of the implant dose, again fitting well with Eq. 3-3's premise that $\rho_c \sim 1/\sqrt{N_D}$.

When the doping concentration in the semiconductor is decreased, the depletion region is wider, and this reduces current due to tunneling. Eventually, as doping further decreases, the current-flow mechanism due to thermionic emission over the barrier becomes dominant. Hence, a rectifying I-V curve is generally exhibited by contacts fabricated between metal and lightly doped Si. The I-V curve of a rectifying contact is similar to that of a *pn* junction, which is used as a diode. Hence, the contact structure of a metal to lightly doped Si can be used as a diode as well; such devices are known as *Schottky diodes*.

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Aluminum is the most common and important metal used in IC interconnections. "Ohmic" contacts between Al and *n*-type Si can be made if the surface concentration of dopant in the Si is high (e.g., $>10^{19}$ cm^{-3}). However, when Al is deposited directly onto less heavily doped *p*-Si and is subsequently sintered (i.e., heated to ~450°C following deposition to ensure good contact formation), a low value of ρ_c is still observed, even for Si as lightly doped as 10^{16} cm^{-3}. This occurs because Al is a *p*-type dopant, and some of the Al diffuses into the Si during the sinter step; a heavily doped *p*-region is thus established under the Al-Si contact region.

In the fabrication of actual contacts, the values of ρ_c that are obtained are also strongly dependent on the condition of the Si surface. That is, if the surface is not clean (e.g., if there is a thin polymer or native SiO_2 film on it), the value of ρ_c that is obtained can be much higher than that predicted by Eq. 3-3. Such phenomena will be described in more detail in the section dealing with the practical issues of fabricating metal-semiconductor contacts.

Note that metal-to-metal contacts must also be made when fabricating ICs. The contact resistance of such contacts is usually negligibly small compared to that of metal-Si contacts, and hence is normally ignored. In some cases, however, metal-to-metal contact resistance may be significantly large (e.g., if contact is made to an Al film that has a native Al_2O_3 layer on the surface, or when contact is made between CVD W and Al films), and measures must be taken to reduce it. Issues dealing with metal-to-metal contact resistance are discussed in chapter 4.

3.3 EXTRACTING VALUES OF SPECIFIC CONTACT RESISTIVITY FROM MEASUREMENTS

In order to analyze the effects of R_{co} on the device characteristics of bipolar and MOS transistors, the value of R_{co} in specific device structures must be known. However, the measured value of R_{co} depends not only on ρ_c but also on the contact size, the semiconductor sheet resistance, and the contact geometry. As a result, the measured value of R_{co} in a test structure may not by itself provide an accurate estimate of R_{co} in real FET and bipolar transistor contacts which have different dimensions than those in the test structure (especially in the smaller contacts of future generations of devices).

The general procedure used to determine R_{co} instead involves the extraction of the contact-size-independent parameter ρ_c from test-structure measurements. This procedure is tedious, but once an accurate value of ρ_c has been obtained, it can be used to calculate the R_{co} in actual devices with contacts of various sizes (based on the specific contact size, semiconductor sheet resistivity, and contact geometry).

The flow chart in Fig. 3-6 shows that a measured value of V/I for a given test structure is first obtained; next the extraction procedure is used to get ρ_c; finally the value of ρ_c is used together with the other factors to get R_{co} in an actual device. A 2-D device simulator, such as PISCES (see chap. 9), can be used to accurately calculate R_{co} for a specific contact structure once ρ_c is available.

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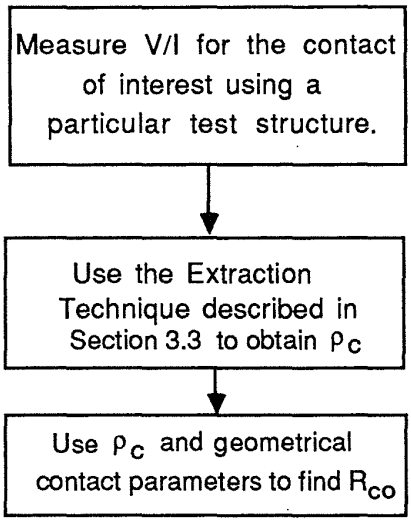

Fig. 3-6 Flow chart that illustrates how to obtain accurate values of R_{co} in an actual contact.

Since each metal-semiconductor contact (uniquely defined by the metal and semiconductor type, as well as by the doping concentration) exhibits its own value of ρ_c, values of R_{co} for different contact structures can also be compared if they are based on accurate values of ρ_c.

3.3.1 Extraction of the Specific Contact Resistivity from an Ideal Contact Structure

To understand how values of ρ_c can be extracted, consider once again the current that flows into the contacts of MOSFETs and bipolar transistors. If the current density over the entire area, A, of the contact were uniform (an ideal case), the value of ρ_c could be extracted from a measurement of the voltage across the contact interface, V, and the current through the contact, I. The measured value of V/I would then yield a value, R_k, and ρ_c would be found from the following expression:

$$\rho_c = R_k / A \qquad (3-4)$$

However, in most cases the current density is not uniform across the entire area of the contact, and hence this simple expression is usually not valid for extracting ρ_c from R_k. Nevertheless, many reports in the literature have used this equation to extract values of ρ_c from test-structure measurements; unfortunately such reported values of ρ_c are usually in error. In general, Eq. 3-4 is useful for providing an estimate of the *upper bounds* to the value of ρ_c. Hence, when Eq. 3-4 is used to determine ρ_c, the reported value is actually greater than the correct value. The more recently reported values of ρ_c

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for various contact structures (for which the more correct models may have been used to extract ρ_c) have usually been lower than the earlier reported values.

3.3.2 Current Flow in Actual Contact Structures

The reason that current flow in actual MOS (and bipolar base) contact structures is not uniform over the entire contact area can be explained through a simple, one-dimensional perspective (Fig. 3-1). In such contacts the laterally moving current in the semiconductor flows in a region that has a finite resistance (characterized by the value of its sheet resistance, ρ_{sh} [in Ω/sq]), and the much lower-resistivity metal is assumed to be an equipotential. The parasitic resistance offered to lateral current flow is therefore smallest for current entering the metal at the leading edge of the contact, and this resistance effectively increases as the current flows laterally under the contact before entering the metal. The density of current entering the contact is thus greatest at the leading edge and smallest at the trailing edge. This phenomenon is termed *current crowding*.

Such current crowding is increased as ρ_{sh} is increased (or ρ_c decreased), making it useful to define a quantity known as the *transfer length*, l_t, in terms of these parameters. l_t is defined as the distance from the edge of the contact at which the value of the current density has dropped to 1/e of its value at the leading edge. The value of l_t is calculated from

$$l_t = \sqrt{\frac{\rho_c}{\rho_{sh}}} \qquad (3-5)$$

This equation implies that if the length of the contact were made much longer than l_t, most of the current would flow into the contact near the leading edge, and there would be almost none in the rest of the contact. In such a contact, only a small fraction of the area of the contact would be used to carry the current. If a value of ρ_c was extracted from the measurement of R_k in such a long contact using Eq. 3-4, and this value of ρ_c was used to estimate the contact resistance, R_{co}, of a much smaller (and therefore shorter contact), the resulting estimate of R_{co} in the smaller contact would not be accurate.

The value of l_t in typical device contacts can be estimated by considering a contact in which $\rho_c = 10^{-6}$ Ω-cm^2 and $\rho_{sh} = 100$ Ω/sq. Equation 3-5 predicts the value of l_t of such a contact to be 1 μm. (If ρ_c is even smaller, l_t will also be smaller.) Thus, in actual tests, the use Eq. 3-4 to extract values of ρ_c and R_{co} from contact structures whose lengths are 3 μm or longer is likely to produce erroneous values, since l_t values of 1 μm or less would cause significant current-crowding effects in such larger contacts.

One of the earliest papers that reported this effect was published in 1983.[3] In it, the measured values of R_k versus contact size (using the cross-bridge Kelvin resistor described in the next section) was compared to the values of R_{co} predicted by the value of ρ_c extracted from a large contact (e.g., 5 μm x 5 μm) using Eq. 3-4. With Eq. 3-4 used to extract ρ_c from the R_k measured in a large contact, the dotted line in Fig. 3-7 gives the estimated value of R_{co} of smaller contacts, based on the extracted value of ρ_c.

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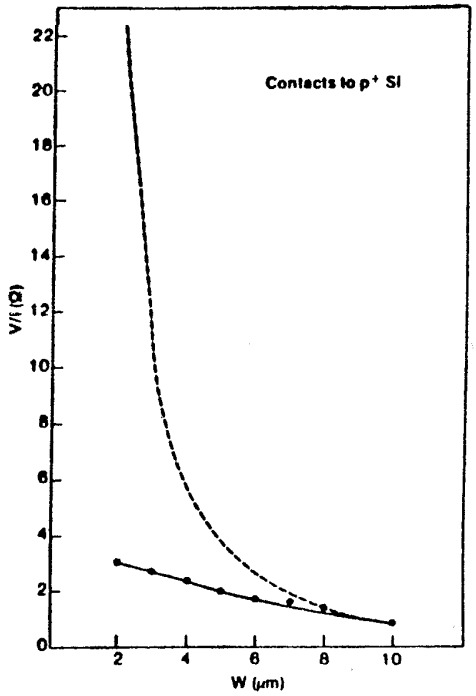

Fig. 3-7 Values of R_{co} for small contacts predicted by Eq. 3-4 compared to measured values.[3] Reprinted by permission of the publisher, The Electrochemical Society, Inc.

The *observed* value of R_k in the actual smaller contacts, however, was much smaller, as shown by the solid line.

Thus, the value of ρ_c extracted from the large contact using Eq. 3-4 does not allow accurate values of R_{co} to be estimated in smaller contacts. The reason for the discrepancy is that since the current density over the area of the contact is not uniform, it yields an erroneous value of ρ_c if Eq. 3-4 is used to extract it. A more accurate procedure for extracting ρ_c from contact-test-structure measurements must therefore be provided.

3.3.3 Contact Structures Used to Extract ρ_c

Several test structures have been developed for extracting ρ_c from electrical measurements. The three most commonly used are: the *cross-bridge Kelvin resistor* (CBKR, Fig. 3-8a);[4] the *contact end-resistor* (CER, Fig. 3-8b);[5] and the *transmission-line tap resistor* (TLTR, Fig. 3-8c).[6] In all of these structures, a specific current is sourced from the diffusion level up into the metal level through the contact window. A voltage is measured between the two levels using two other terminals. The contact resistance measured for each structure is this voltage divided by the source current.

Since each of the test structures measures the voltage at a different position along the contact, as shown in Fig. 3-8, the contact resistance values measured are different, and they must therefore be distinguished from one another. The resistances measured by the

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CBKR, the CER, and the TLTR structures are, respectively, R_k (Kelvin), R_e (end), and R_f (front). The 1-D equations used to extract ρ_c from the measured resistance values are derived from the distributed-resistor network that is used to model the current-crowding effects described in the previous section. In addition, in deriving these equations it is assumed that the diffusion width, w is equal to the contact width. (In the absence of a "diffusion overlap" of the contact, the current flow is uniform across the diffusion area width; that is the current flow is one-dimensional). The 1-D model equations used to extract ρ_c from each of the test structures are as follows:

$$R_k = V_{14} / I_{32} = \rho_c / l^2 \qquad (3\text{-}6a)$$

$$R_e = \frac{V_{43}}{I_{12}} = \frac{\sqrt{\rho_{sh}\rho_c}}{w \sinh\left(l\sqrt{\rho_{sh}\rho_c}\right)} \qquad (3\text{-}6b)$$

$$R_f = \frac{\left(\frac{V_{56}}{I_{23}}\right) l_1 - \left(\frac{V_{45}}{I_{12}}\right)}{2\,(l_1 - l_2)}$$

$$= \frac{V_{43}}{I_{12}} = \frac{\sqrt{\rho_{sh}\rho_c}}{w \tanh\left(l\sqrt{\rho_{sh}\rho_c}\right)} \qquad (3\text{-}6c)$$

where the subscripts in V and I denote the pad numbers shown in the diagrams, and w and l are the width and length of the contact window.

Several problems arise, however, if these equations are used to extract a value of ρ_c from practical test structures in which the contact is smaller than the diffusion area. First, if a value of ρ_c is extracted from same-type contacts with identical dimensions using two different types of structures, the extracted values often yield disagreeing estimates of ρ_c. Second, when the CBKR structure is used and contact resistance is plotted against area, a sublinear behavior is observed, instead of the expected inverse linear behavior. Third, the extracted values of ρ_c from experimental data based on the 1-D models appear to be not only contact-size dependent, but also appear to be a function of diffusion sheet resistance, ρ_{sh} (even if the active surface-dopant concentrations are identical). This is a serious problem, since the variations are often more than an order of magnitude!

To account for and explain these results, the current flow *around* the contact must be included, and a 2-D model must be employed instead of the 1-D model that results in Eqs. 3-6. Such a 2-D model has been rigorously derived and is described in ref. 7. This model provides a basis for extracting the value of ρ_c from any of the three contact test structures; the value of ρ_c that is obtained can then be used to calculate the value of R_{co} in contact structures of any size. When the validity of this model was being checked, it was found to yield identical values of ρ_c, even when contacts of different dimensions and from different test structures on the same wafer were used. Thus, it is claimed that when

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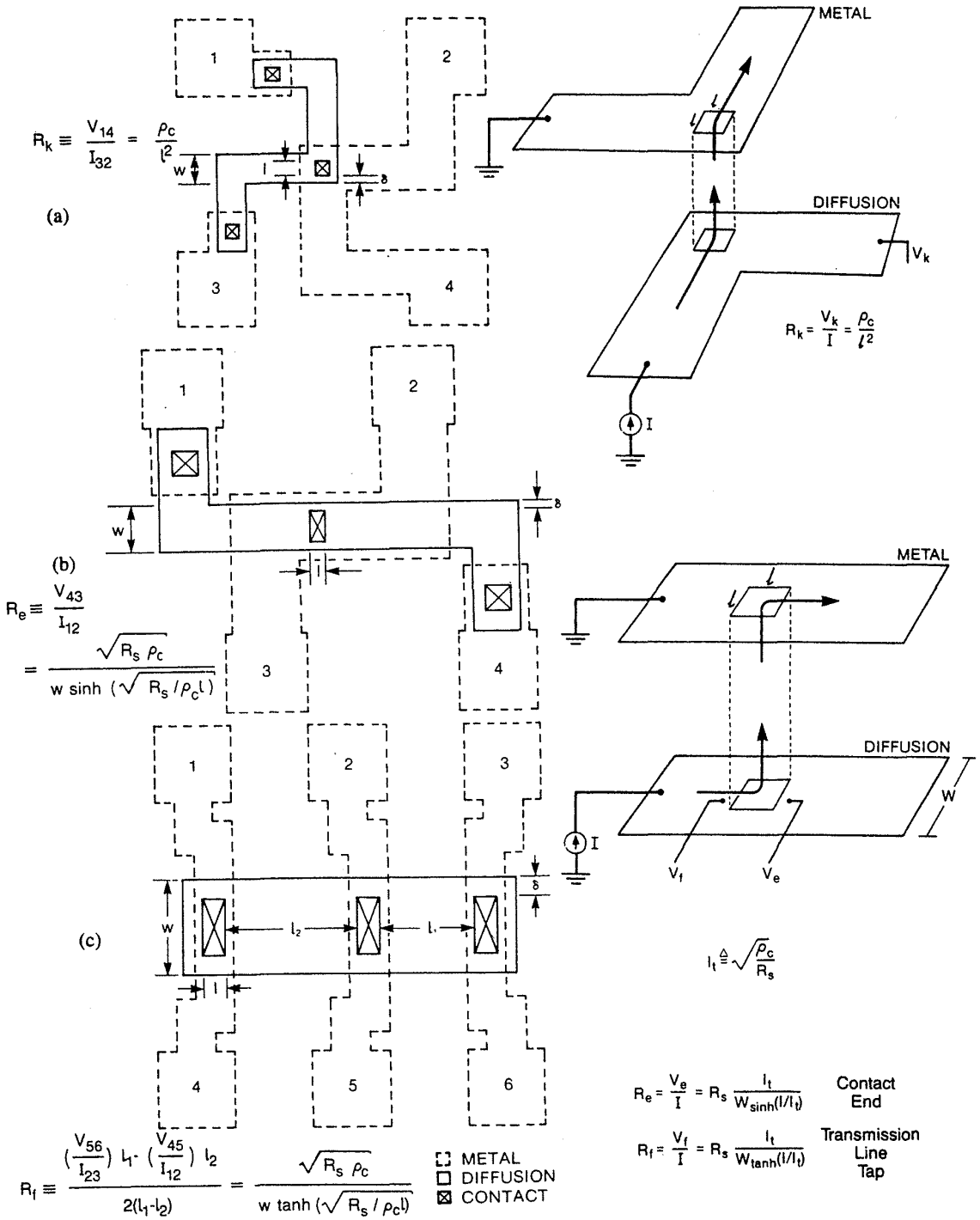

Fig. 3-8 The layouts and 3-D depictions of the three test structures used for measuring contact resistance. (a) Cross bridge Kelvin resistor (CBKR). (b) Contact end resistor (CER). (c) Transmission line tap resistor (TLTR).[7] (© 1987 IEEE).

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this model is used to extract ρ_c, the values obtained are accurate, self-consistent, and independent of geometry and test structure type.

The results of the 2-D model are presented in a universal form so that values of ρ_c can be extracted without the need to perform any additional computer simulations. The method for using the results of this model to extract values of ρ_c from data obtained from the CBKR test structure is presented in the following section.

3.3.4 Procedure for Accurately Extracting ρ_c from CBKR Test Structures

The procedure for accurately extracting ρ_c using the CBKR method and the universal CBKR curves of Loh et al.[7] is described in this section. The CBKR structure has been selected to illustrate the procedure because it is the structure recommended in reference 7; similar procedures to extract ρ_c using the other test structures can also be used.

1. Needed are two sets of CBKR test structures of varying contact sizes, l (e.g., two sets of 10 contacts each, varying in length from 1 to 25 μm), with at least two diffusion region overlaps, δ, for each set of structures (Fig. 3-9). (Note that in reference 1 δ values of 1.25 μm and 2.5 μm are used to generate an exhaustive set of curves for extracting ρ_c values. Thus, if this reference is to be closely followed, these same δ values might suffice.) The diffused region under the contacts should be fabricated to closely emulate the junctions that will be built in the devices for which the contact structures are being evaluated. If contacts to both p^+ and n^+ Si will be studied, both p^+ on n and n^+ on p junctions will need to be produced. The value of the sheet resistance of the diffused layers, ρ_{sh}, is first measured.

2. After the contacts to the Si have been fabricated, the value of the Kelvin contact resistance, $R_k = V/I$, of each contact is measured (on an appropriate number of samples). Then the value of $\log_{10}(R_k/\rho_{sh})$ is calculated for each contact.

3. The value of $\log_{10}(l/\delta)$ is calculated for each contact.

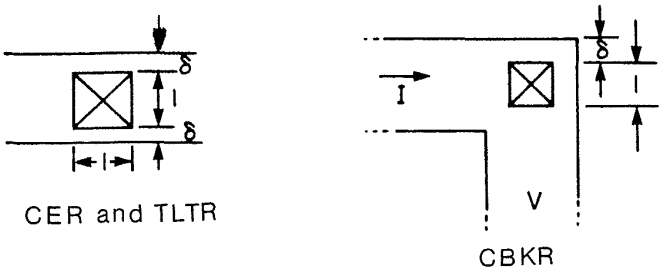

Fig. 3-9 Diffusion region overlap in the three test structures used for measuring contact resistance.[7] (© 1987 IEEE).

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4. The values of $\log_{10}(R_k/\rho_{sh})$ versus $\log_{10}(l/\delta)$ are plotted on the graph containing the universal CBKR curves (Fig. 3-10a). (In reference 7, this is done first for the set of contacts in which $\delta = 1.25\ \mu m$, and then for the set of contacts in which $\delta = 2.5\ \mu m$.)

5. Each of these two sets of data points should lie along one of the universal curves. Two values of $y = l_t/\delta$ should be extractable from the curves in this way.

6. Since the values of δ are known, the value of l_t can be found from $l_t = y\,\delta$.

7. Since $l_t = \sqrt{\rho_c/\rho_{sh}}$, the value of ρ_c is found from $\rho_c = l_t^2\,\rho_{sh}$.

As an example, if R_k is obtained for two sets of contacts, and these data are used to plot $\log_{10}(R_k/\rho_{sh})$ on the universal CBKR curves (as shown in Fig. 3-10b), it is found that

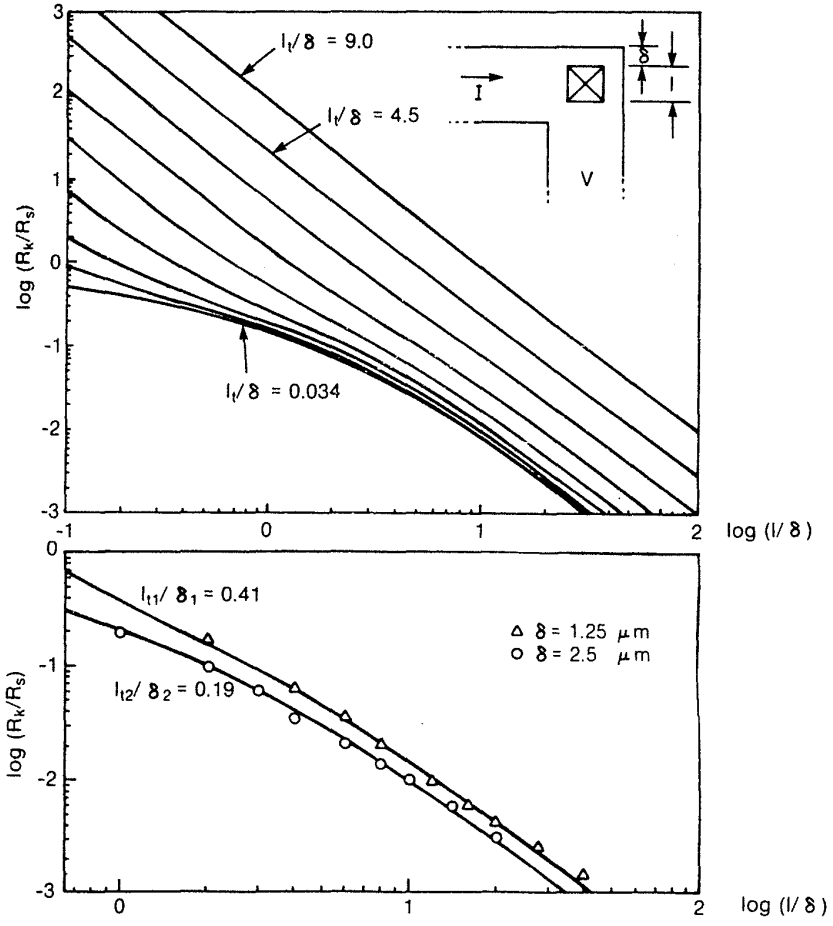

Fig. 3-10 (a) Generalized universal curves for the CBKR. Curves show l_t/δ approximately in octave steps. (b) Illustration of the use of the CBKR universal curve to extract l_t from devices with a different overlap δ on the same wafer, $l_t = 0.5\ \mu m$ for all points.[7] (© 1987 IEEE).

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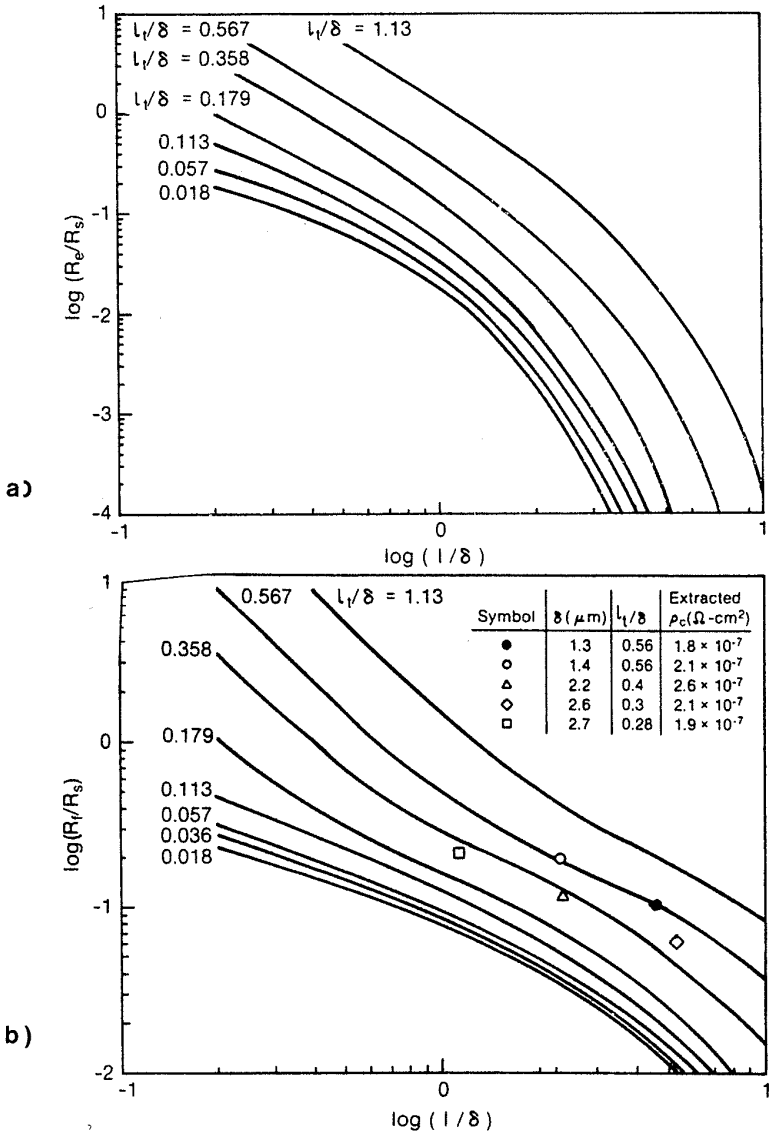

Fig. 3-11 Generalized universal curves for (a) the CER. (b) the TLTR. (Curves show l_t/δ approximately in octave steps).[7] (© 1987 IEEE).

these values of R_k lie on the curves for which y = 0.41 and y = 0.19. (Note that in this figure, only the two curves from Fig. 3-10a for the particular y values 0.41 and 0.19 are shown). If in this example the values of the diffusion-region overlaps, δ, are 1.25 μm and 2.5 μm, and ρ_{sh} = 44.4 Ω/sq, we determine that l_t = 0.5 μm for both sets of contact structures. As a result, ρ_c is found to be (0.5 μm)^2 44.4 Ω/sq = 11.1 Ω-μm^2.

The sets of universal curves from reference 7 that allow ρ_c to be extracted from TLTR and CER test structures (in the same manner as outlined above) are presented in Figs. 3-11a and 3-11b. The values of ρ_c extracted from measurements using these structures should be the same as those extracted from CBKR test structure measurements.

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Therefore, if a set of TLTR or CER test structures is available, they can be used instead of the CBKR structures.

Loh, however, recommends the use of the CBKR test structures over the others. In the TLTR method, linear extrapolation is needed to eliminate the diffusion potential drop; this can result in large errors when ρ_c is extracted. In the CER method, parasitic components usually dominate the potential contribution from the contact end, again making the extraction of ρ_c difficult. The CBKR therefore emerges as the best compromise in almost all cases between extraction ease and sensitivity to errors in the diffused layer and overlap-width dimensions, especially when it is aided by 2-D simulations.

3.3.5 Reported Values of ρ_c for Various Contact Structures

Table 3-1 presents the values of ρ_c for various contact structures using the procedure outlined in the previous section. It should be noted that these values generally represent the minimum values of ρ_c that have been reported in the literature; higher values of ρ_c have been reported by other workers. In some cases, such previously reported values overstated ρ_c because the values were extracted using the simpler models that did not account for parasitic current-flow effects in the contact structures. In others, however, a lower value may also have been due to alternative process-fabrication procedures (e.g., variations in the annealing temperature, contact cleaning procedure, and doping of the Si under the contact).

Thus, while the values of ρ_c in Table 3-1 may represent the "best case" that can be achieved under well-controlled laboratory conditions, the values obtained by means of a specific contact-fabrication sequence in a production environment may be significantly higher. Therefore, if the value of R_{co} is considered to be one of the critical parameters that may limit device performance, it is important that each contact-fabrication process be characterized using the ρ_c-extraction procedure presented earlier. In particular, the

Table 3.1 Specific Contact Resistivities of Various Metal-Si Contacts

Metal-Si	ρ_c (Ω-μm^2)	Reference
Al:Si to n^+ Si	15	6
Al:Si - TiN - n^+Si	1.0	62
Al:Si - TiN - p^+Si	20	62
PtSi to n^+Si	5	7
CVD W to n^+ Si	11	7
Al - Ti:W - $TiSi_2$ - p^+ Si	60-80	153
Al - Ti:W - $TiSi_2$ - n^+ Si	13-25	153

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effect of changing (especially reducing) the doping concentration at the surface of the Si (e.g., by varying the implant doses, the implanted species, and the dopant-activation-annealing steps following implant) has been reported to have a potentially significant negative impact on the value of ρ_c exhibited by a particular contact structure.

Finally, it should also be noted that if ρ_c values of 10 Ω-μm^2 or less can be obtained, then the value of R_{co} in devices with such contacts will probably not have much adverse effect on performance behavior, regardless of how small they are scaled. This important conclusion will be considered in more detail in section 3.8.

3.3.6 Use of a Simple Contact-Chain Structure to Monitor Contact Resistance

It should be briefly noted that an accurate value of R_{co} generally cannot be extracted from resistance data obtained from a simple *contact-chain structure.* That is, to determine R_{co} from the measurement of the total resistance of the contact chain shown in Fig. 3-12, the resistances of the metal-interconnect lines and the diffused region of the semiconductor must be subtracted from the measured reistance value. Since these resistances amount to a large fraction of the total measured value, the total contact resistance of the chain of contacts is obtained by subtracting two large numbers to obtain a smaller one. Such experimental data are therefore subject to large experimental errors.

Nevertheless, these kinds of contact chains are useful as test structures that can provide rapid monitoring of the contact-fabrication process. As long as the total measured-resistance value of such a contact chain is less than the specified value following a contact anneal step, the contact-fabrication process has probably been successfully performed.

3.4 THE EVOLUTION OF CONVENTIONAL METAL-TO-SILICON CONTACTS

Like other aspects of IC processing, the technology for fabricating metal-to-silicon contacts has had to evolve in order to keep pace with other advances in the process sequence. The technology we refer to as *conventional contact fabrication* involves the

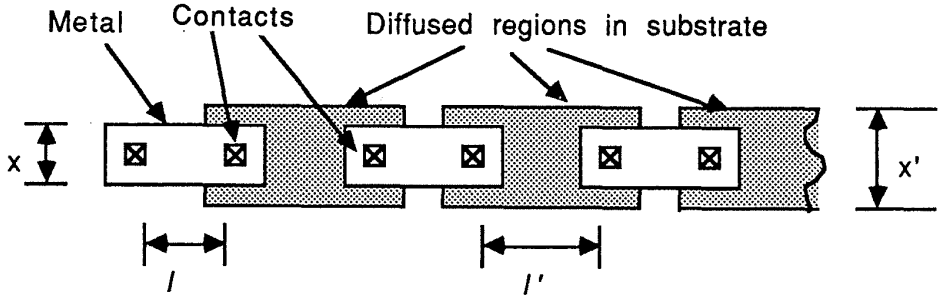

Fig. 3-12 Contact-chain. A test vehicle for monitoring contact resistance.

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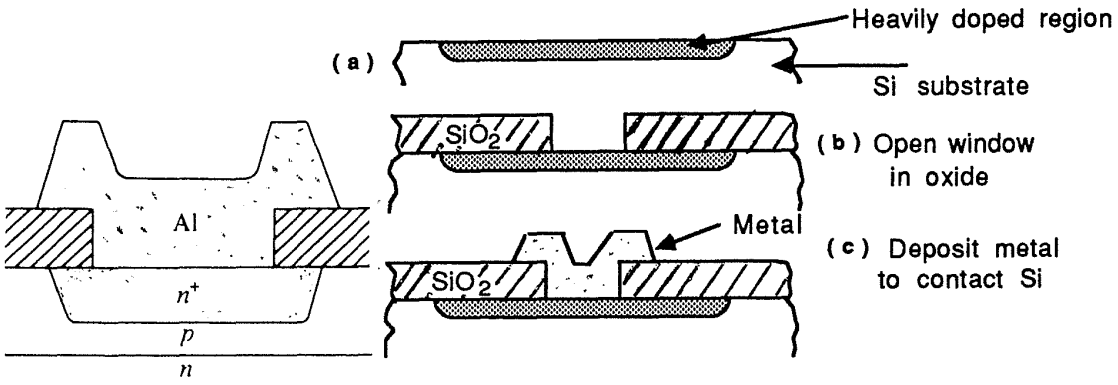

Fig. 3-13 Process sequence for forming conventional metal-semiconductor contact structure, in which the metal is deposited over a window in the passivating surface oxide.

fabrication of a contact to silicon at locations where a window has been etched in the oxide that covers and passivates the silicon surface (Fig. 3-13). While this type of contact has been used since integrated circuits were first invented, alternative contact structures have also been implemented recently. In this section we describe the evolution of the conventional contact structure, and show the reasons why alternative technologies were developed.

3.4.1 The Basic Process Sequence of Conventional Ohmic-Contact Structures to Silicon

Following is the basic sequence of steps involved in the formation of a metal-to-silicon contact structure for an integrated circuit:

1. Heavily doped regions, which extend relatively deeply into the silicon, are created in the silicon substrate in the locations where contacts are to be established.

2. A window (or *contact hole*) is etched in the oxide that covers the silicon wafer surface (typically, this is a thermal oxide or a CVD oxide/thermal oxide layer). The etching can be done using either wet or dry etching techniques.

3. Prior to deposition of the metal, the surface of the silicon is cleaned to remove the thin native-oxide layer that rapidly forms on a silicon surface whenever it is exposed to an oxygen-containing ambient.

4. The metal film is deposited onto the wafer surface and makes contact with the silicon wherever contact holes have been created in the oxide. In the simplest contact structures, the deposited metal is Al (or an Al:Si alloy). A variety of procedures have been developed to ensure that the deposited-metal

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films adequately cover the sidewalls of the contact windows without severe thinning (i.e., thereby achieving good *step coverage* into the contact windows).

5. After deposition, the contact structure is subjected to a thermal cycle known as *sintering* or *annealing*. The purpose of this step is to bring the metal and the silicon surfaces into intimate contact. In the case of Al contacts, during sintering the Al film will consume any residual native oxide by chemically reacting with it (assuming that this residual film is not too thick).

3.4.2 Additional Details Concerning the Processing Steps

3.4.2.1 Formation of the Heavily Doped Regions in the Silicon. As described earlier, in order for an ohmic contact to be formed at a metal-semiconductor interface, the surface of the semiconductor must be heavily doped, with the dopants having been usually selectively introduced through ion implantation or diffusion. A masking layer is used to restrict the introduction of dopants to the desired locations on the silicon surface. Such heavily doped regions may also form part of the transistor device structure (e.g., the source and drain regions in MOSFETs and the emitter regions in bipolar transistors).

The contact resistance is inversely proportional to the surface concentration of the dopant, and thus as heavy a doping as possible would seem desirable. However, the maximum doping concentration is limited by the solid solubility at the temperature at which the dopant is introduced. Clustering effects may also reduce the concentration of the electrically active impurities below the concentration of deposited dopant atoms. For example,[8] arsenic atoms undergo such clustering if their concentration is above 10^{20} cm^{-3}. A model for As clustering is described in reference 9.

In advanced IC processing, it is necessary to form heavily doped regions that extend into the silicon to very shallow depths only. Since higher implant doses result in deeper junction depths, the dose cannot be chosen independently of the device design. The topic of shallow-junction formation and the problems associated with the fabrication of contacts to shallow junctions is explored in section 3.10.

3.4.2.2 Formation of Contact Openings (Etching). The formation of contact holes in the oxide that covers the wafer surface is also a key step in the fabrication of contact structures. The minimum size of the contact holes is usually determined by the minimum-resolution capability of the patterning technology, because this results in the smallest device sizes. As a result the patterning technology is generally pushed to its limits in the patterning of contact holes.

When the contact holes are larger than ~2.0 μm, wet etching has often been used to open them. Even in such contact holes, however, wetting and reactant product removal can be a problem. To partially overcome the wetting problem and to ensure better material flow into the vicinity of the reacting surface, mechanical or ultrasonic agitation

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was introduced. Such wet-etching technology of SiO_2 films is described in more detail in Volume 1, chapter 15.

The isotropic nature of wet etching, however, made it ineffective for the patterning of smaller-sized contact holes. As a result, development of SiO_2 dry-etching processes had to be pursued (see Vol. 1, chap. 16). Dry etching, however, introduced a new set of problems, including polymer contamination, damage of the Si surface, and decrease of oxide etch rate with decrease in contact size. One consequence of the former effect was that either gases with less propensity for forming polymeric products would have to be found, or more complex processes to remove the polymers from the contact holes after etch, would have to be developed. Dry etching also exhibited selectivity problems, which became more significant as junctions grew shallower.

Several approaches were also proposed to alleviate the problems of damage to the silicon surface and redeposition of nonvolatile by-products from the chamber surfaces and wafer holders. One was to use isotropic (ion-bombardment-free) dry etching to remove surface damage and contaminants.[10] Another combined a dry-etch step (to remove the first 80% of the contact oxide layer) and a buffered HF wet etch (to etch the remainder of the oxide film). This method, however, still presents the problem of wetting in small contact holes. One proposed solution to the wetting difficulty is to use an anhydrous-HF gas to remove the final oxide layer.[11,134]

A process has been reported that uses a CHF_3/CO_2 dry-etch process to open the contact holes, followed by a two-step dry-etch cleaning procedure to remove the residual damage.[12,13] Finally, an RTP process that repairs the silicon-crystal damage in the contact hole has also been described.[14]

As the contact hole size decreases below 1 μm there is a strong decrease in etch rate with contact size dimension. To avoid long overetch times, contact holes of identical dimension would need to be used if this problem was not solved. Reference 156 describes a dry-etch process which overcomes this limitation. By adding 10% Cl_2 to a CHF_3 plasma the effective fluorine to carbon ratio in small holes is kept constant, maintaining uniform etch rates, independent of contact hole size. Nevertheless, it is very common that only one contact size is used. Larger contacts are implemented with multiple contact windows.

3.4.2.3 Sidewall Contouring of the Contact Holes by Reflow. In addition to the need to ensure that the contact holes are opened and that silicon-surface damage and contamination are minimized, it is also important to give the contact hole a shape that will result in good step coverage by the metal that is deposited into it. In general, better step coverage will be obtained if the walls of the contact opening are sloped and the top corners are rounded, and several different approaches have been pursued to achieve these desired sidewall profiles.

One of the most popular involves *reflow of the contact hole dielectric layer.* Wafers are exposed to a high-temperature step after the contact holes have been opened. This causes the CVD doped-SiO_2 layer to flow slightly, producing rounded corners and sloped sidewalls in the contact holes (see Vol. 1, chap. 6). *Borophosphosilicate glass* (BPSG) flows at the lowest temperatures (800-850°C at atmospheric pressures), and even lower-

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temperature reflow cycles (using high-pressure conditions) have reportedly been developed.[15] Reflow using RTP has also been investigated.[16] A recently introduced LPCVD reactor allows BPSG film deposition to be followed by an in situ flow step, which eliminates a process step and reduces the overall cycle time (although reflow must still be performed after contact holes have been opened).[141] A study of the reflow mechanisms in BPSG films presented in reference 138. It indicates that reflow in BPSG film will cause sidewall overhang and reentrant angles at the base of the contact hole if the aspect ratio of the contact hole is larger than 0.393.

It has also been mentioned that it can be useful to grow a thin-oxide layer over the contact hole following patterning, but prior to reflow. The function of this oxide is to prevent autodoping of the contact regions during reflow by the BPSG film. This oxide would be grown at a lower temperature (e.g., 8 minutes in steam at 800°C) than the reflow temperature (e.g., 900°C).[135] Alternatively, the reflow can be done in a dry O_2 ambient to simultaneously grow the thin protective-oxide layer.[140]

H. Ozaki et al., however, have described how the B_2O_3 in the BPSG film can react with the PH_3 (used as part of the gas ambient during reflow to redope the contacts in NMOS technology) to form a volatile compound of boron. This boron is then taken up by the oxide film that is grown in the contact openings during the reflow, resulting in a much thicker oxide in the contact hole following reflow.[17] Consequently, another suggested approach for preventing contact-degradation effects during the reflow step is the deposition of diffusion-barrier materials (e.g., silicon nitride or TiN) over the opened contacts prior to the reflow step.[15]

3.4.2.4 Sidewall Contouring by Etching. Other sidewall-contouring processes involve the etching procedure used to pattern the contact holes. The first of these uses a wet etch (which is isotropic) to partially etch the oxide, and follows this with an anisotropic dry etch.[18] The method yields a contact hole whose profile is sloped at the top but is vertical at the bottom. While good step coverage can be achieved in some applications, difficulty may be encountered in obtaining good wetting, especially for very small contacts. In addition, the sidewall profile may still have a sharp corner at the upper edge, which gives rise to step-coverage problems. A variation of this method is to use a triple layer (oxide/nitride/oxide). The top oxide is wet etched to provide a sloped contact-hole sidewall, and the nitride serves as an etch stop. The remaining nitride and oxide are then etched with a vertical dry-etch step.[19]

Another general approach involves the controlled erosion of photoresist (PR) that has been baked to produce a sloped PR wall.[20,21] In this method, PR images of the contacts are exposed and developed using standard lithographic techniques. Following develop, the resist images are subjected to a postdevelop bake of ~150°C (Fig. 3-14a). The resist flows during the bake, relaxing the vertical resist profile. Etching the resist and oxide at approximately the same rate replicates the tapered-resist profile into the contact sidewall. While the bake-to-slope process is quite adequate for large contacts or vias (>2 μm), it is not easily scalable to smaller geometries. For such smaller contacts resist baking step becomes critical. Too little baking results in vertical contact profiles, while excessive baking can result in closed contacts. Furthermore, continued etching of

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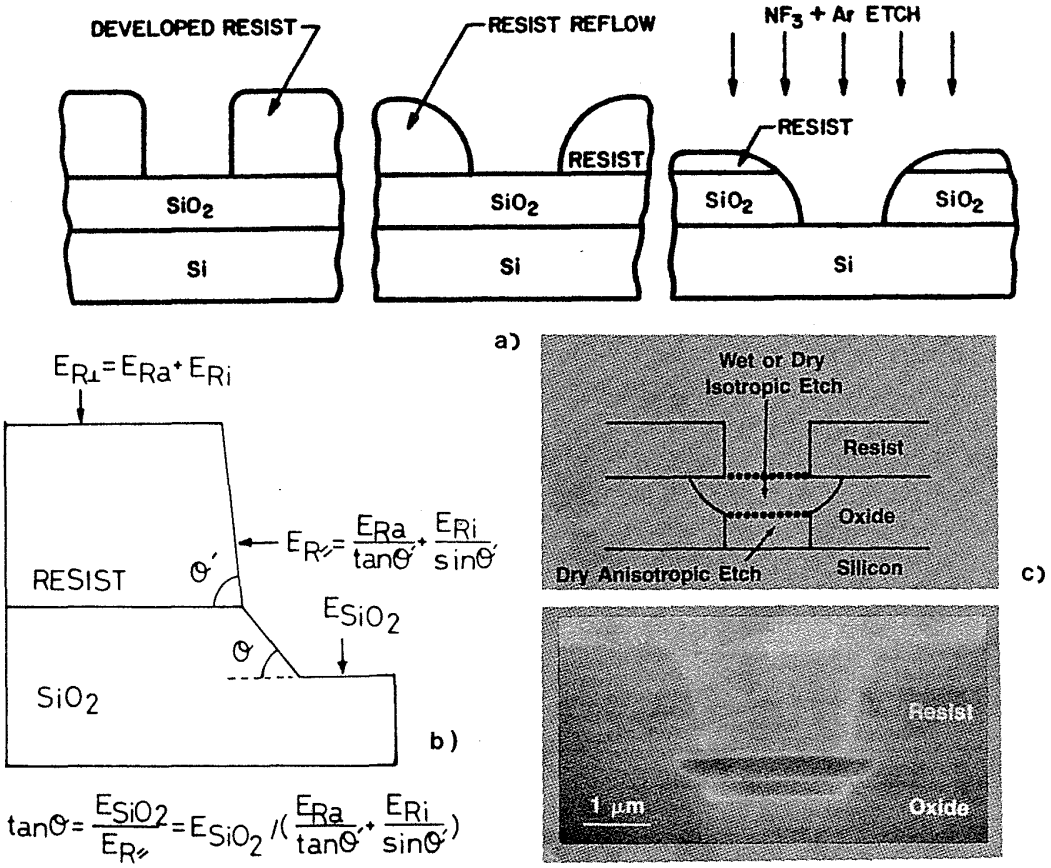

Fig. 3-14 (a) Tapered contact-hole etching by reflowing resist profile with a resist bake, followed by a dry etch to transfer the resist profile into the oxide. (b) Tapering of contact-window sidewall by optimizing the lateral to vertical etch rates of the resist mask.[25] Reprinted by permission of the publisher, The Electrochemical Society, Inc. (c) Sloping oxide sidewalls using a triode dry etcher.[152] Reprinted with permission of Solid State Technology.

the contact results in continued growth in the contact diameter (although this effect can be alleviated somewhat by using a two-step etch process).[22]

Several other, more controllable resist-erosion techniques have subsequently been described. In one, the effect of resist faceting (see Vol. 1, chap. 10) caused by the preferential sputtering of the resist corners was used to produce tapered-contact sidewalls.[23] Another method, developed by Jillie et al.,[24] uses a single-wafer etcher, and a two-step etch process to etch a multilevel-resist layer (i.e., consisting of a thin positive resist, an antireflection coating, and a thick PMMA). Good control over the sidewall slope has been reported, and a reflow step has also been used to round the top corners of the sidewall. The drawback to this approach is increased process complexity.

A third resist-erosion approach was reported by Kudoh et al.[25] In this procedure, etching of the contact oxide is carried out with a PR mask that has vertical sidewalls.

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Oxygen is added to the CHF_3 gases being used to etch the oxide. The oxygen attacks the PR at a controlled rate, thereby producing lateral as well as vertical etching of the PR mask. More of the top SiO_2 is slowly exposed as vertical etching of the SiO_2 proceeds, and a sloped oxide sidewall is produced (Fig. 3-14b). Taper angles of 40-85° were obtained by varying the oxygen concentration.

Another technique for tapering contact-hole sidewalls without using resist erosion involves implantation of the surface of the oxide following deposition. This damages the top layer of the oxide and causes it to etch more rapidly, even when dry etching is used. The faster- etching top-surface layer causes a slope in the sidewalls.

A final group of processes utilizes two or more dry-etch steps to obtain tapered-sidewall profiles. In one example, a high-rate isotropic SiO_2 etch (i.e., with a lateral-to-vertical etch-rate ratio of 0.9 to 1 being exhibited for doped oxides) is used to etch the top portion of the contact-oxide layer, and an anisotropic-etch process is used to remove the oxide from the bottom of the contact hole.[26] In another, a downflow etcher operated at 2.45 GHz is used to etch part of a doped SiO_2 layer in an isotropic manner using a $CF_4 + O_2$ mixture; this is followed by an RIE step to give a vertical profile for the bottom portion of the layer.[27] A method that uses a tri-electrode dry-etch chamber for this type of process is described in reference 152 (Fig. 3-14c).

The problem of end-point detection for contact holes can also be difficult. That is, if a timed etch is used, a sufficient overetch must be allowed to ensure that all the contacts are opened. However, this demands a high selectivity to the Si to prevent too much Si from being consumed during the overetch. End-point detection is difficult, because the total area of the contacts being etched is significantly smaller compared to other layers. A technique for electronically enhancing the weak end-point signal produced when the contacts are finally opened is described in reference 144.

3.4.2.5 Removal of the Native-Oxide Layer Prior to Metal Deposition. Before the metal is deposited into the contact openings, it is necessary to ensure that the exposed silicon surface is as free as possible of contamination or of a native-oxide layer. Silicon will grow a thin native oxide within a matter of seconds upon exposure to an oxygen-containing ambient or an oxidizing solution. This native oxide can represent an impediment to current flow through the contact interface, result-

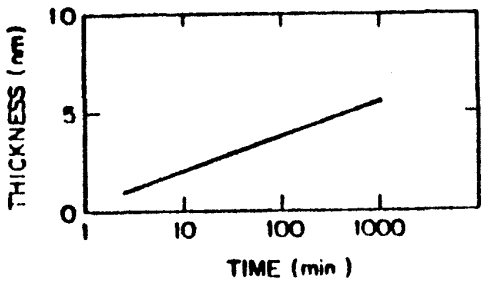

Fig. 3-15 Native oxide growth rate on Si exposed to room air.[28] Copyright 1984. Reprinted with permission of the AIOP.

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ing in high resistance for ohmic contacts. Oxide films of minimum thickness (2–5Å) do not present a problem, since many contact metals (e.g., Al, Ti, Pt) can consume such thin oxide layers during the sinter step. Nevertheless, as shown in Fig. 3-15, the native-oxide layer can grow thicker than this value in 30 to 60 minutes* if the Si is exposed to atmosphere at room temperature.[28,139] Consequently, techniques must normally be employed to remove native oxide layers on Si, and the metal must be deposited quickly enough after such premetal cleaning that the film does not have enough time to regrow.

A variety of techniques have been suggested for cleaning the Si prior to metal deposition. Polymers deposited during a dry-etch step used to etch the contact oxide are typically removed through a final oxygen-ashing step. This step may, however, may create a thin oxide layer on the exposed Si. The most widely used method for removing native-oxide layers on the Si involves dipping the wafer in a dilute H_2O:HF (100:1) solution for ~1 minute, followed by rinsing and drying and immediate insertion into the sputter or evaporation chamber. (The HF dip also serves to remove heavy-metal contamination that might occur as a result of the dry-etch process.)

It is acknowledged that this method is not perfect, since some SiO_2 will regrow on the Si during the rinse-and-dry step, and inadequate wetting may prevent complete removal of the native oxide in small-geometry contacts. Therefore, a technique of sputter-etching the contacts in the sputter chamber and depositing the metal before reexposing the contacts to atmospheric conditions is also frequently used in addition to the HF dip. Most sputtering systems currently provide the capability for performing such sputter etching.

However, some concerns have also been raised about sputter etching. For small, high-aspect-ratio contact holes, sputtering and redeposition of material from the contact sidewalls and the wafer surface may cause more oxide to be deposited onto the Si than is removed through the sputter-etch process (Fig. 3-16).[29] Two alternative procedures to overcome these concerns have therefore been suggested. The first involves an in situ, chemically driven dry-etch step to remove the native oxide. While this would eliminate the resputtering effect, it would require that sputtering equipment be designed with this extra capability; no such products have yet been commercially introduced. In the second approach, an anhydrous-HF gas could be used to remove the native oxide, as described in a previous section.

The effect of "dirty" Si surfaces prior to Al deposition has been studied by Faith et al.[30] These researchers showed that if the Si surface is not successfully cleaned prior to Al deposition, the post-sinter contact resistance will be an order of magnitude higher than if an effective pre-metal clean had been used. They also noted that clean contacts

*A recent report indicates that both moisture and oxygen must be present in air in order for the oxide to grow. Furthermore, if oxygen is present in DI water, a native oxide will also grow when Si wafers are immersed in it. Since the growth rate of native oxide decreases with the concentration of moisture, this may provide an approach to the control of native-oxide films on Si.[147] For example, virtually no native oxide was observed to grow during a seven day period of time when Si wafers were stored in air containing < 0.1 ppm moisture.

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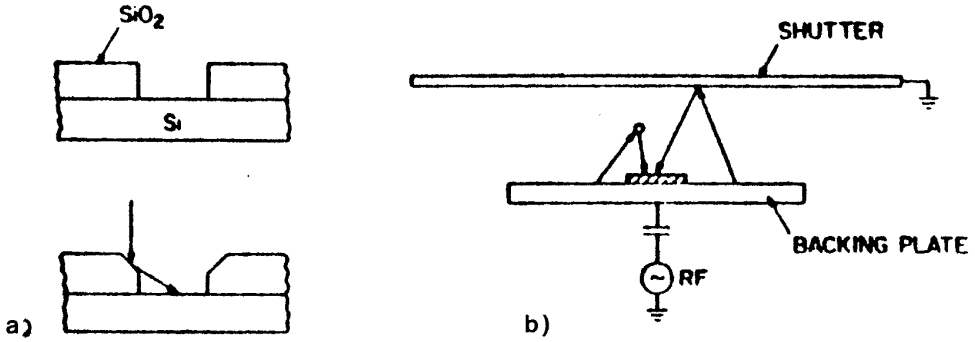

Fig. 3-16 Sources of contamination of Si surface at the bottom of the contact hole as a result of RIE. (a) Faceting occurs during anisotropic etching of contact openings. Material sputtered from the facet deposits in the contact opening at a rate that may exceed the rate of removal of the material from the bottom of the opening. (b) Backscattering of material sputtered from the backing plate may occur due to collisions with gas molecules of the glow discharge or from reflection from the shutter.[28] Copyright 1984. Reprinted with permission of the AIOP.

exhibit a lower contact resistance than dirty ones *prior* to the sinter step, and that this effect could be exploited to test the contacts prior to sintering. If a dirty interface were detected at that point, a decision to strip and rework the metal might still be possible, whereas this option would no longer be available once sintering had been performed. As described in the following section on contact sintering, ion-beam mixing has also been proposed as a way to disperse any native-oxide layers at the interface.

3.4.2.6 Metal Deposition and Patterning. The major issue in the deposition of metal for fabricating contacts is ensuring that adequate step coverage is obtained into the contact holes. When contact-hole sizes are comparable to the oxide thickness (i.e., when the holes have high aspect ratios), good step coverage can be difficult to achieve. The deposition process, as well as the profile of the contact-hole sidewalls, can significantly impact the quality of the step coverage. Several aspects of the metal- deposition procedure can also play a role in this issue.

First, the type of process selected for deposition is significant. Some CVD processes can completely fill high-aspect-ratio contact holes, even those with nearly vertical sidewalls, while physical vapor deposition (PVD) methods are not apt to fill the holes so well. This advantage has been exploited in filling contact holes with CVD W (selectively and through blanket deposition). Polysilicon and selectively grown epitaxial layers of Si are other CVD processes that have been reported for such contact-filling applications.

If films are needed that cannot be deposited by CVD, the conditions of the PVD process can be selected to give improved step coverage (see chap. 4 in this volume, and Vol. 1, chap. 10). For example, heating of the wafers to ~300-350°C has been shown to significantly improve the step coverage of sputtered Al films into contact holes. Full planarization (i.e., complete filling of the holes) has also been demonstrated by applying

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even higher temperatures during sputter deposition (400-500°C). Laser planarization of Al films following deposition has also been developed to improve step coverage into contacts (see chap. 4).

In addition, sputtered Ti:W films have also been reported to give excellent step coverage. This method can be used to enhance the overall step coverage of contact structures – for example, if such a Ti:W film is used under a layer of Al. On the other hand, the problem of film thinning at the bottom corners of the contact window can produce reliability problems in contacts. Even if the top layer of Al appears to have been deposited with adequate step coverage, the diffusion-barrier layer, for instance might have been deposited with thin spots at these edges (Fig. 3-17). As a result, the contact could fail because the barrier layer was not thick enough at these locations to survive the sintering steps following deposition of the metal (see section 3.5).

The issues dealing with the patterning of the metallization layers used in contact structures are described in further detail in Volume 1, chapter 16.

3.4.2.7 Sintering the Contacts. As described earlier, the sintering or annealing of contacts (i.e., the alloying of contacts through treatment at an elevated temperature) is performed to allow any interface layer that exists between the metal and the Si to be consumed by a chemical reaction, and to allow the metal and Si to come into intimate contact through interdiffusion. The details of the various reactions that occur at specific metal-Si interfaces during the sinter cycle are described in the following sections examining the properties of each contact type. In this section we merely mention the several methods by which such intermixing of materials at the interface is performed.

The traditional method carries out the sinter step in a diffusion furnace, usually at 400-500°C for 10 to 30 minutes in the presence of H_2 or a *forming gas* {a mixture of H_2 (5-10 at%) and N_2 (95-90 at%)}. Such gases are used because many metals are

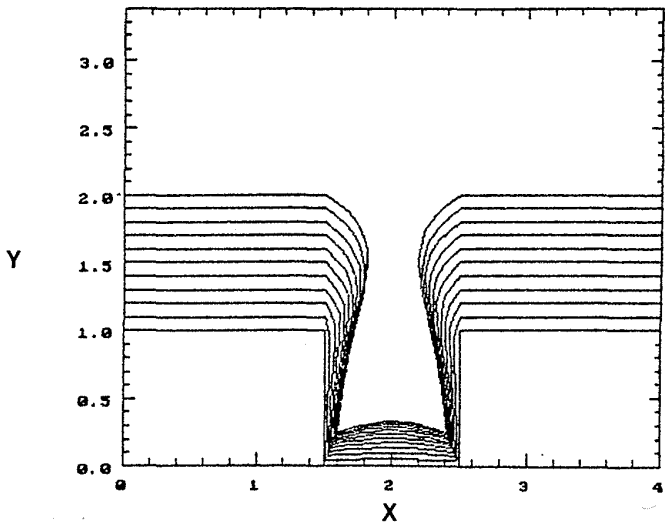

Fig. 3-17 Simulated metal coverage of a contact hole with vertical sidewalls, showing thinning at the bottom corners.

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sensitive to oxygen at elevated temperatures, and because this step is also used to anneal out the surface states (i.e., interface traps at the oxide-Si interface) by tying up the dangling Si and oxygen bonds. The hydrogen is responsible for passivating and deactivating the interface traps.

More recently, alternative methods – including RTP, laser annealing, isothermal e-beam sintering, and ion-beam mixing – have also been investigated for performing this step. Although ion-beam mixing does not subject the contacts to elevated temperature, the chemical outcome is very similar to that in an alloying process. The technique involves the implantation of a relatively high dose of ions at an energy that is high enough to allow full penetration through the metal layer and into the Si substrate. If the species that is implanted is the same as the dopant of the junction to be formed, the junction and the contact can be fabricated simultaneously.[31] Normally, the implant is followed by a furnace step (conventional or RTP) to repair the implant damage, and possibly to form a silicide or to distribute the implanted dopant.

3.4.3 Aluminum-Silicon Contact Characteristics

The contact structure consisting of pure Al deposited directly onto Si was adopted in the earliest stages of silicon technology primarily because of its simplicity, but also because it exhibits some other advantages. Al and Al alloy thin films are still the most common interconnect materials in silicon ICs today. Al-to-Si ohmic contacts can be fabricated with low values of contact resistance to both n^+ and p^+ Si, and both the contact and the interconnect structure can be fabricated through a single deposition step. Al is desirable as an interconnect material because it exhibits low resistivity ($\rho_{Al} = 2.7$ $\mu\Omega$-cm) and offers excellent compatibility with SiO_2 (i.e., Al will readily react with SiO_2 to form a thin layer of Al_2O_3 at the interface, thus promoting strong adhesion between the Al and the SiO_2). The Al thin films used for interconnects are typically 0.5-1.5 μm thick.

However, the Al-to-Si contact exhibits some poor contact characteristics and also introduces some limitations into the processing sequence. Because the melting point of Al (660°C) and the eutectic temperature of Al and Si mixtures (577°C) are so low, Al is a problematic material with respect to the maintenance of contact stability. Thus, the simple contact structure of pure Al-to-Si has had to be modified, especially for VLSI applications. In addition, Al must be introduced into the IC process sequence after all high-temperature processing has been completed.

3.4.3.1 The Kinetics of the Al-Si Interface During Sintering. We noted earlier that a sinter step is performed after a contact metal film has been deposited and patterned. In the case of Al-Si contacts, such sintering causes the Al to react with the native-oxide layer that forms on the silicon surface. In the case of e-beam-evaporated Al films on MOS devices, sintering also anneals out the radiation damage at the SiO_2/Si (gate oxide/Si) interface from the x-rays generated by the evaporation process; see Vol. 1, chap. 9. As the Al reacts with the thin SiO_2 layer, Al_2O_3 is formed, and in a good ohmic contact, the native oxide is eventually completely

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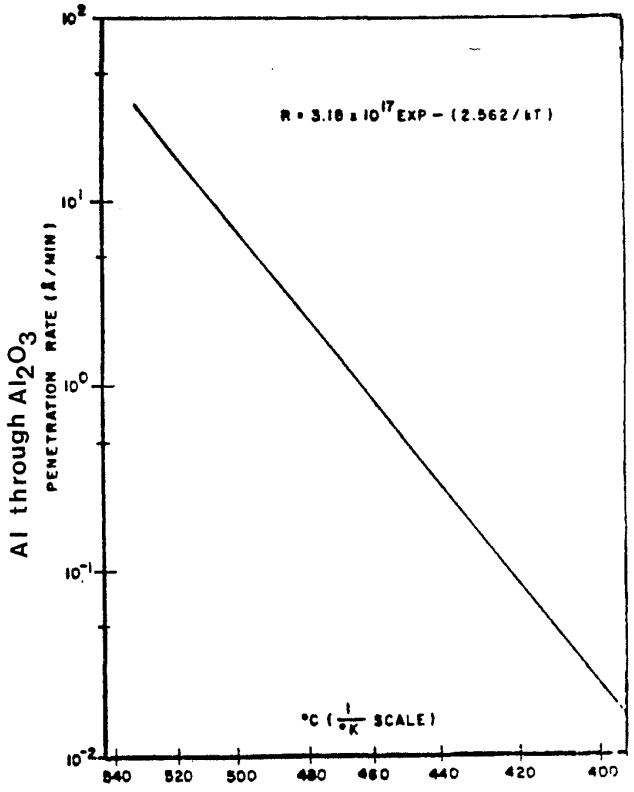

Fig. 3-18 Rate of reaction for Al + SiO_2 --> Al_2O_3 + Si.

consumed. Thereafter, Al diffuses through the resultant Al_2O_3 layer to reach the Si surface, forming an intimate metal-Si contact.

Note that Al must diffuse through the Al_2O_3 layer to reach the remaining SiO_2. As the Al_2O_3 layer increases in thickness, it takes longer for the Al to penetrate it. Thus, if the native-oxide layer is too thick, the Al_2O_3 layer eventually also becomes too thick for Al to diffuse through it. In this case, not all of the SiO_2 will be consumed, and a poor ohmic contact will result (i.e., one that exhibits a high specific contact resistivity).

Figure 3-18 shows the penetration rate of Al through Al_2O_3 as a function of temperature. For acceptable sinter temperatures and sinter times (e.g., 450°C and 30 min.) the thickness of the Al_2O_3 should be in the 5-10 Å thickness range. Since the maximum Al_2O_3 thickness is of the order of the thickness of the native oxide that is consumed, an approximate upper limit to the allowable thickness of the native-oxide layer is set. The longer the silicon surface is exposed to an oxygen-containing ambient the thicker the native oxide will be (Fig. 3-15). This explains why surface-cleaning procedures in most contact processes are performed just prior to loading of the wafers into the deposition chamber for metal deposition.

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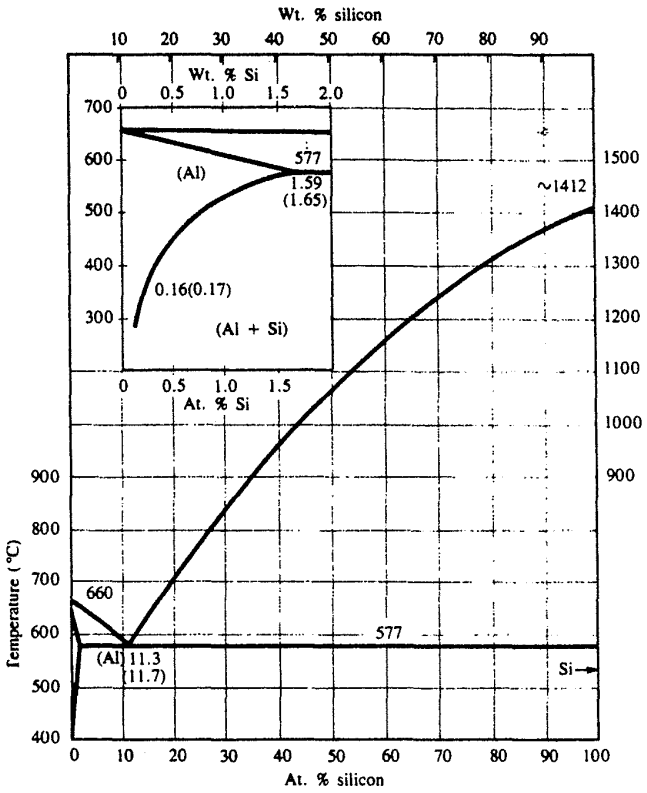

Fig. 3-19 Phase diagram of the aluminum-silicon system. The silicon-aluminum eutectic point occurs at a temperature of 577 °C. At contact-alloying temperatures between 450 and 500 °C, aluminum will absorb from 0.5 to 1% silicon. Copyright 1958, McGraw-Hill Book Company, with permission from ref. [161].

Since the use of a sinter step is inevitable when Al-Si contacts are fabricated, the other effects of this thermal cycle on the contact structure must also be considered. The phase diagram of the aluminum-silicon system (Fig. 3-19), indicates that the solubility of silicon in aluminum rises as the temperature increases (e.g., it is ~0.5 at% at 450°C, and ~1 at% at 500°C). This means that if a pure Al film were heated to 450°C and a source of silicon were provided, the Al would take up the silicon in solution until a concentration of 0.5 at% of Si was reached. The substrate serves as such a source, and and the silicon will enter the Al by diffusion at such elevated temperatures. If silicon diffusion were slow and the contact was maintained at the elevated temperature for only a short time, not much silicon would enter the Al, so there would be no problem.

In the actual case of Al thin films (which are polycrystalline in structure), the grain boundaries of the polycrystalline Al film provide very fast diffusion paths for the Si at temperatures above 400°C. Figure 3-20 shows the diffusivity of Si in Al as a function of temperature, for both bulk and thin-film Al.[32] The diffusivity in the thin-film Al is seen to be much faster. As a result, if a large volume of Al is available, a significant quantity of the Si from below the Al-silicon interface can diffuse into the Al film. Simultaneously, the Al from the film will move rapidly to fill the voids created by the

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departing Si (Fig. 3-21). If the penetration of the Al is deeper than the *pn*-junction depth below the contact, the junction will exhibit large leakage currents or even become electrically shorted. This effect is referred to as *junction spiking*.

The depth to which Si is consumed and Al penetrates into the Si substrate can be calculated as a function of the thickness and width of a long Al line, the contact area, and the temperature and time of the sintering. As shown in Fig. 3-20, at temperatures in excess of 400°C the diffusion length in one minute exceeds 10 μm. The effect of the diffusion with respect to an actual contact structure is illustrated in Fig. 3-21. As a result of such diffusion, the silicon in a 16 μm^2 Al-Si contact would be consumed to a depth of ~0.3 μm if the contact was exposed to a temperature of 500°C for 30 min (assuming uniform Si consumption across the contact area).[33] Consequently, junctions with depths of less than 0.3 μm would be shorted, rendering the devices inoperable.

In fact, since the Si consumption is not uniform across the entire contact area, the situation is even more severe than is portrayed by the above example. The native oxide that exists at the Si surface is not uniform in thickness but has local thin spots, or defects, as shown in Fig. 3-21. Thus, when the native oxide is consumed during sintering, it will first be removed at these thin spots, and Si will therefore be able to dissolve into the Al at these points. As a result, Al penetration, or *spikes* can occur to a depth of more than 1 μm. In (100)-oriented Si substrates, such spikes tend to move perpendicularly to the surface and are bounded by (111) planes. In addition, Al spiking occurs preferentially at the contact-hole edges, where stresses present in the Si lead to enhanced dissolution of the Si during contact sintering. If the Al is stripped after such sintering, the Si pits appear as shown in Fig. 3-22.

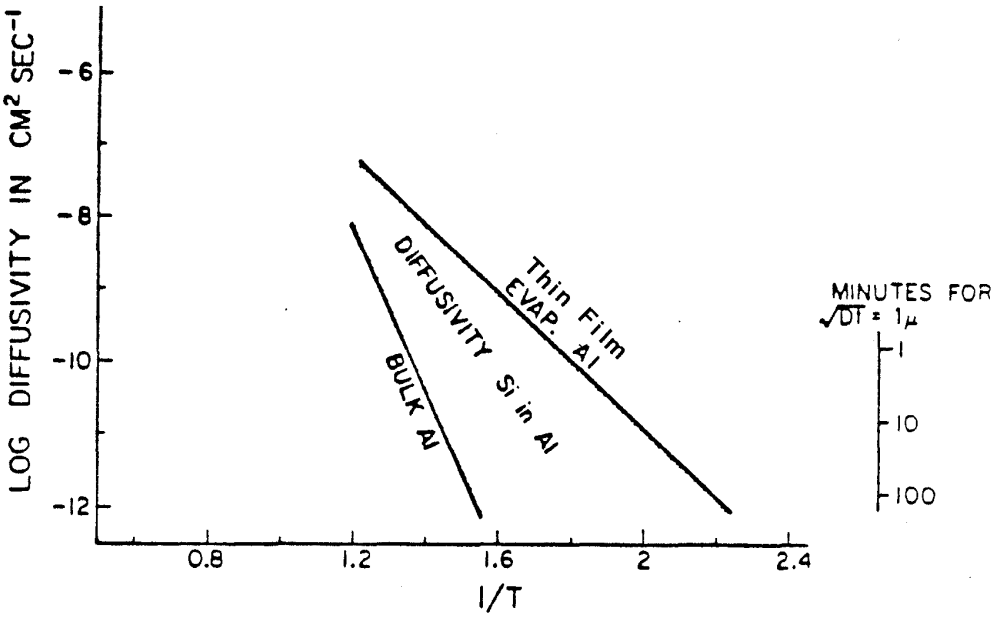

Fig. 3-20 Diffusivity of silicon in bulk and thin film aluminum.[32] Copyright 1974. Reprinted with permission of the AIOP.

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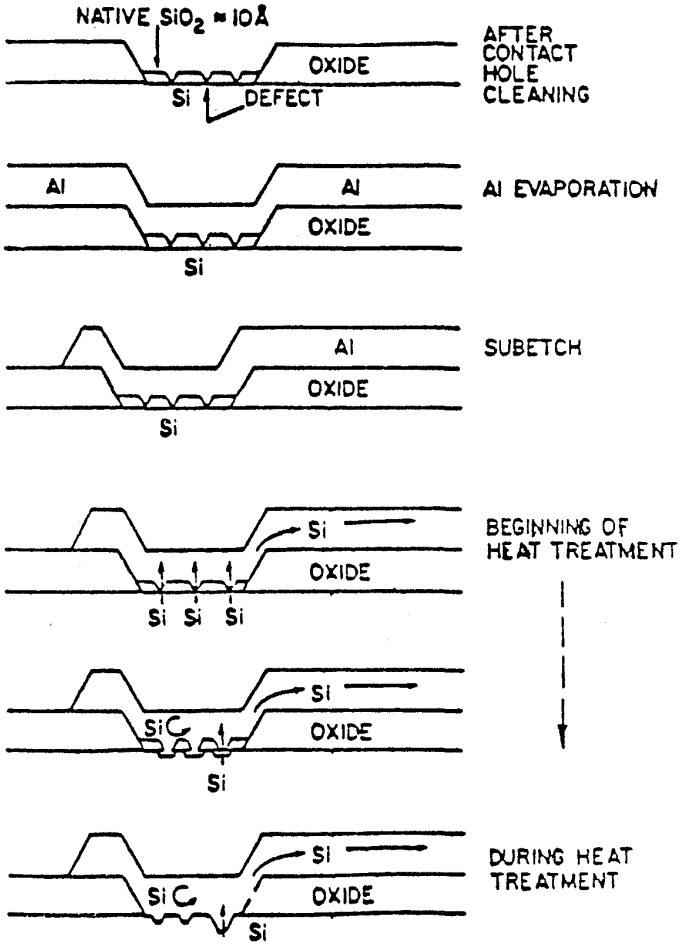

Fig. 3-21 Sequence of events during the sintering of Al-Si contacts that leads to Al junction spiking.

The pit dimensions is also observed to increase as the area of the contact hole is decreased.[34] This effect imposes a severe limitation on the usable combination of

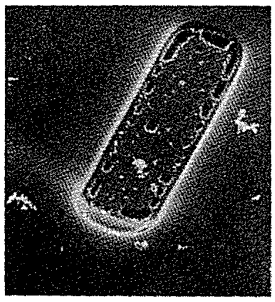

Fig. 3-22 SEM micrograph of Si pitting that exists after sintering of an Al-covered contact. (Al has been stripped after the sinter step.)[165]

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junction depth, x_j, and contact-hole size, d, or $x_j >> 4.7d^{-0.8}$. More concisely, since junction depths of less than 200 nm are being utilized in advanced ICs, this type of contact cannot be used.

3.4.4 Use of Aluminum-Silicon Alloys to Reduce Junction Spiking

To alleviate the problem of junction spiking at contacts without abandoning the advantages of the simple Al-to-Si contact structure, Si can be added to the Al film as it is deposited. This is typically accomplished by sputter depositing the film from a single target containing both Al and Si, although coevaporation of Si and Al has also been used. If enough Si is added to the Al so that the concentration exceeds the Si solubility at the maximum process temperature, diffusion of Si into the Al will no longer occur, and junction spiking can be prevented. The amount of Si that must be added to accomplish such *presaturation* of Al with Si therefore depends on the maximum process temperature to which the contact structure will be exposed. Since this maximum temperature is normally less than 500°C, in most cases slightly more than 1 wt% Si is added. The change in resistivity of the Al, $\Delta\rho$, caused by such additions of Si is very small (i.e., $\Delta\rho$ for each percentage of Si added is only 0.07 $\mu\Omega$-cm, and $\rho_{\text{pure Al}} = 2.7\ \mu\Omega$-cm).

Such Al:Si alloys were widely adopted for fabricating the contacts and interconnects of NMOS integrated circuits. To improve the reliability of such contact structures, deeper junctions immediately below the contact opening were also employed in some processes. (These deep junctions were created by redoping the Si with phosphorus after the contacts were opened. Such redoping can be accomplished during the reflow step, by performing the reflow in an $N_2/PH_3/O_2$ ambient.[17] Doing so allows the source/drain regions near the channel to be kept shallow for good device performance, while providing a deep junction under the contact to prevent junction spiking. This method cannot of course be used in the shallow source/drain regions of devices fabricated in the wells of CMOS structures (see chap. 6 on CMOS device structures).

Although the use of Al:Si instead of pure Al prevented junction spiking, it also introduced other problems. During the cooling cycle of a thermal anneal, the solid solubility of silicon in Al decreases with decreasing temperature. The aluminum thus becomes supersaturated with Si, which causes nucleation and growth of Si precipitates out of the Al:Si solution. Such precipitation occurs both at the Al-SiO_2 interface and the Al-Si interface in the contacts (preferentially around the contact hole edges where solid-phase epitaxial growth occurs easily). These precipitates consist of p-type silicon (since Al is a p-type dopant in Si), doped with Al to a concentration of ~$5x10^{17}$ cm^{-3}.

If such precipitates form at a p^+Si-Al contact interface, they do not degrade the contact properties. On the other hand, if they form at the contact interface to n^+Si, an undesirable increase in contact resistance results. In practice, for contacts sizes of 3 x 3 μm or greater, such effects are not significant, and Al:Si alloys can be used effectively. For smaller contacts, however, the increase in resistivity can be excessive.

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In addition, the Si precipitates formed within the Al interconnect lines can increase the susceptibility of the lines to electromigration failure. That is, in narrow Al lines the precipitates can be large enough to obstruct a large fraction of the cross-sectional area of the metal line at random locations.[35,36] The size of the Si precipitates in Al:1% Si alloys is about 0.4 μm; if the films are cooled slowly, the precipitates can grow to be as large as 1.5 μm. At locations where such precipitates are formed, a large flux-divergence in the current is produced. This can lead to early failure of the conductor by an electromigration-induced open circuit.

Al-Si contacts exhibit two other important limitations that would prevent their use in advanced VLSI applications, even if the problems above could be overcome. First, in IC technologies in which small-sized contacts and shallow junctions must both be used, Al:Si alloys cease to be completely effective in preventing junction spiking. The precipitation that occurs during the cooldown from the first thermal cycle (e.g., the sinter step) can cause the Al near the contact interface to contain an Si concentration that is lower than that needed for solid solubility during subsequent processing steps. When the wafer is heated again (e.g., during the deposition of the passivation film or during the die-attach or packaging process), Si from the substrate can diffuse into the Al.

Second, when high current densities are passed through Al-Si contacts, the electron current leads to the transport of Si from the contacts into the Al. This leads to spiking of the junction at the negative terminal and deposition of Si at the positive terminal. Such susceptibility to *contact electromigration failures* also increases as the contact area is reduced.

In summary, the simple Al-Si contact structure that was used extensively for NMOS IC fabrication has become increasingly less suitable for advanced CMOS and bipolar integrated circuits, even if an Al:Si alloy is used for the metallization. As a result, more elaborate contact structures that can overcome the limitations of the Al-Si contact have had to be developed.

3.4.5 Platinum Silicide-to-Silicon Contacts

An early approach to overcoming the junction-spiking problem of Al-Si contacts used a platinum-silicide layer (PtSi) between the Si and Al in the contact structure. Not only could such contacts withstand temperatures of 350-400°C without junction spiking, but they also exhibited two other advantages over Al-Si contacts: (1) they offer a self-alignment capability, which restricts the formation of the PtSi layer to the region in the contact hole without there being a need for additional masking steps; and (2) they exhibit excellent electrical characteristics, due to the mechanism by which the silicide is formed. That is, the PtSi layer is formed by reacting a Pt layer in contact with Si at low temperatures (250-400°C). Rapid diffusion and reaction of the Pt occur at such low temperatures, allowing the silicide to be produced. During the growth process, the original contaminants from the Pt-Si interface are swept to the surface of the newly formed silicide, and the PtSi-Si interface is buried beneath the original Si surface. As a result, an absolutely clean and intimate silicide-silicon contact is formed.[39]

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Platinum-silicide layers are able to provide low contact resistivity for ohmic contacts to both n^+ and p^+ Si (approximately a factor of two lower than the Al-to-Si contacts described in an earlier section), and they provide a film that is stable with respect to the silicon substrate for process temperatures in excess of 500°C. They also exhibit relatively high conductivities. For example, PtSi films of 60-nm thickness exhibit a sheet resistivity of ~34 $\mu\Omega$-cm.

The first application of PtSi contacts to silicon technology was reported by Hosack in 1972.[37] Since that time, numerous other noble and near-noble silicides (e.g., Pd_2Si, $CoSi_2$, and NiSi), and refractory metal silicides ($TiSi_2$, WSi_2, $MoSi_2$, and $TaSi_2$) have also been investigated for this purpose. The electronics industry, by and large, early on adopted PtSi-Si for Schottky diodes and ohmic contacts to bipolar transistors. (PtSi Schottky contacts will be described in section 3.7.) The properties and fabrication technology of $CoSi_2$ and $TiSi_2$ will also be described later, as these two silicides have been incorporated into advanced contact structures. A recent study on the applicability of Pd_2Si ohmic contacts has indicated that they may also offer many attractive benefits for VLSI applications.[38]

3.4.5.1 Process Sequence Used to Form PtSi-Si Contacts. The process sequence used to form the PtSi layer in the contact hole (Fig. 3-23) includes the following steps:

1. After an opening is etched in the SiO_2 layer, the surface of the silicon is subjected to an additional cleaning step, such as a dip in dilute HF just prior to loading of the wafers into the sputter chamber, or preferably, an in situ sputter etch. This step is important, because a smooth PtSi-Si interface of uniform penetration requires a Si surface that is free of contaminants and has a minimal native oxide. (i.e., planar, very shallow PtSi-Si interfaces are needed to prevent junction penetration of shallow junctions by the growing silicide layer.) Figure 3-24 shows the effect of the surface quality on the smoothness of the PtSi-Si interface; it can be seen that a contaminated Si surface leads to a PtSi layer of irregular depth.[40,41] It has also been reported that as long as the native oxide on the Si surface is less than 20 Å thick, the PtSi layer will form and, in doing so, will break up the oxide layer and sweep the oxygen to the PtSi surface. On the other hand, thicker native-oxide layers will inhibit the formation of PtSi.

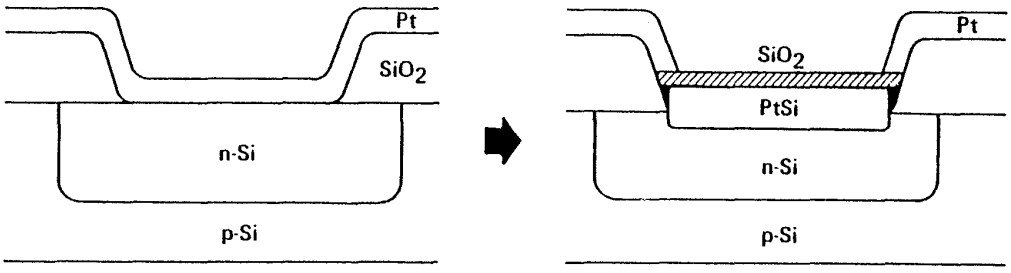

Fig. 3-23 Formation of self-aligned PtSi-Si contacts.

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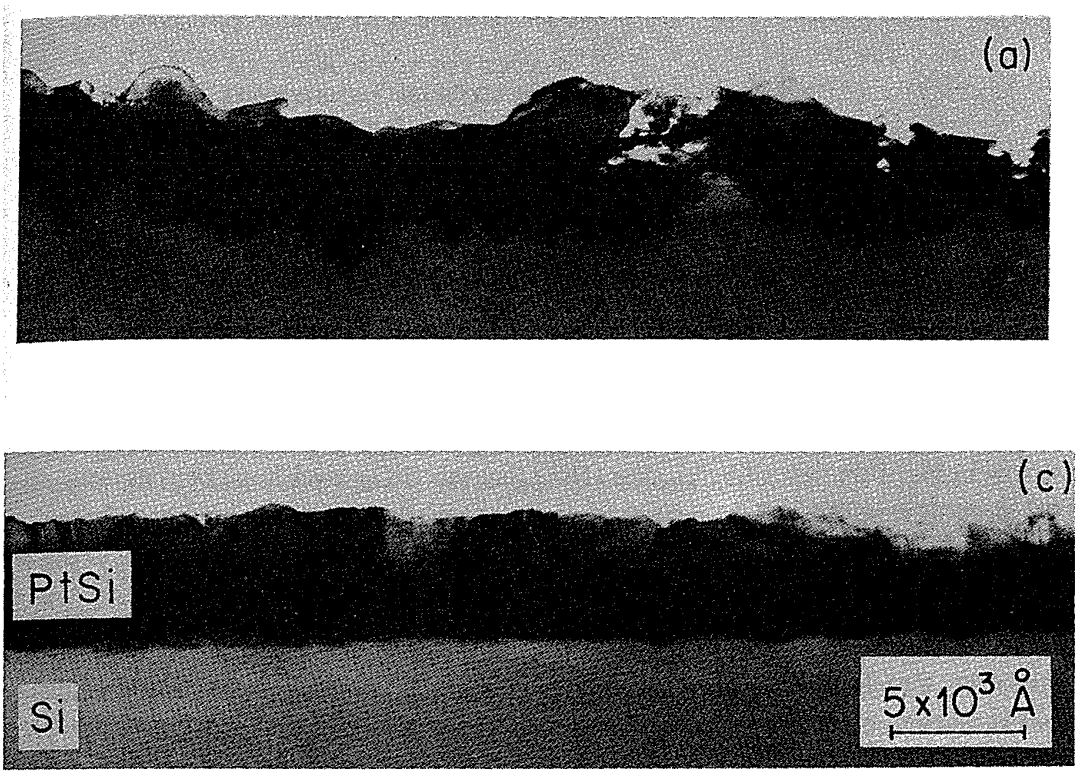

Fig. 3-24 The effect of the surface quality on the smoothness of the PtSi-Si interface. It can be seen that a contaminated Si surface leads to a PtSi layer of irregular depth. (a) shows the rough PtSi -Si interface grown from a severely contaminated surface. (c) shows a smooth, uniform PtSi-Si interface that results when the PtSi is formed on a clean Si film.[40] Copyright 1984. Reprinted with permission of the AIOP.

2. A thin Pt film is then sputter deposited onto the wafer surface to a thickness of 30-60 nm. This thickness range produces silicide layers thick enough to provide good contact properties but without consuming an excess amount of Si below the contact. In forming the silicide layer, Si is consumed to about the same depth as the thickness of the Pt film (e.g., 50 nm of Pt will react with ~60 nm of Si to form a 100-nm-thick PtSi film). A slow sputter-deposition technique (such as *rf sputtering*) is commonly employed in order to maintain adequate thickness control for such thin Pt layers. A clean Si surface (i.e., with a native oxide no thicker than ~10 Å) and a deposition process that does not allow oxygen to be incorporated into the Pt film are both critically important, since the growth of the PtSi layer can be inhibited by the presence of oxygen.

3. The silicide is then formed by heating the wafers in an N_2 ambient. During the annealing process, the Pt reacts with the Si in the contact hole to form

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PtSi, but it does not react wherever it is in contact with the SiO_2. Toward the end of this annealing step, some oxygen is introduced into the furnace. This causes a thin film of SiO_2 to grow on the surface of the just formed PtSi, but no such oxide is grown on the unreacted Pt regions. Various temperatures have reported for the annealing process, but 550°C for 10 minutes is typical. Chang et al., however, have reported that a three-temperature sequence at 200°-350°-550°C yields PtSi films with improved properties. (The formation and properties of the passivating-oxide film on top of the PtSi under various annealing conditions are also described by Chang.)[42] An RTP process for reacting the Pt has also been published.[41]

4. The unreacted Pt is then stripped from the wafer surface by etching in a dilute aqua regia solution at 85°C. The aqua regia, however, does not attack the PtSi because of the protective layer of SiO_2 that was grown on it during the last part of the annealing process. Note that this SiO_2 layer must be removed prior to deposition of the next layer of metal onto the (sputter etching, e.g., has been effectively used for removal of this film).[43]

3.4.5.2 Limitations of the PtSi-Si Contact Structure. Junctions under PtSi-Si interfaces exhibit no degradation (e.g., leakage or shorting) up to temperatures of 800°C. Unfortunately, when an Al layer is deposited onto the PtSi, such junctions undergo junction spiking failures if temperatures exceed 350°C. This occurs because above this temperature, the Al begins to react with the underlying PtSi, causing it to decompose and form various Pt-Al-Si intermetallic compounds. Once the aluminum-silicide reaction front reaches the silicide-Si interface, silicon pits and aluminum spikes are created almost immediately, and shallow junctions rapidly become shorted.

In the early days of IC processing, when device junctions were 0.5 μm in depth (or deeper) and the contact areas were >10 μm^2, such (Al-PtSi-Si) contacts were nevertheless able to maintain adequate junction stability if the annealing temperatures following metallization were limited to 400°C. When the device junctions became shallower than 0.25 μm, however, the Al-PtSi-Si contact (and all other near-noble silicide contacts) could no longer prevent junction spiking at annealing temperatures of 400°C. As a result, it became necessary to introduce yet another barrier layer between the PtSi and the Al to allow the contacts to survive temperatures exceeding 400°C (see Fig. 3-26a). Such so-called *diffusion barriers* will be described in the next section.

PtSi also has two other characteristics that also need to be mentioned. First, because PtSi layers agglomerate at temperatures above 800°C, post-Pt deposition temperatures are limited. Second, the formation of the PtSi occurs in a lateral, as well as a vertical direction. Thus, a 100-nm-thick PtSi layer also penetrates ~100 nm under the edge of the contact oxide window. In the case of a MOSFET with a gate length of 1.0 μm, this would reduce the nominal gate length by 20%. Several approaches have been investigated to minimize this effect, including the deposition of Si and Pt together and the deposition of an alloy of Pt and W (Fig. 3-25). These approaches are reviewed by Tu in reference 44.

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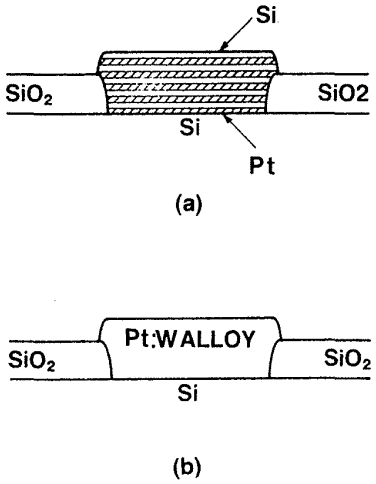

Fig. 3-25 Two approaches investigated to minimize the effect of excess Si consumption during PtSi formation: (a) the deposition of Si and Pt together, and (b) the deposition of an alloy of Pt and W.[44] Copyright 1981. Reprinted with permission of the AIOP.

3.5 DIFFUSION BARRIERS

3.5.1 Theory of Diffusion Barrier Layers

The intermixing of materials from two layers in contact (such as Al and Si) can be prevented by sandwiching another material between them (Fig. 3-26). The role of this third material is to prevent (or ar least retard) the diffusion of the two original materials into each other, or to resist the tendency of a chemical reaction to form a new phase between the adjoining materials. In practice, the available diffusion barrier materials are not perfect: they are capable of extending the life of devices only to some degree, not indefinitely. The efficiency of such a diffusion barrier is therefore determined by how long it can extend the lifetime of the contact structure under various thermal treatments, compared to its lifetime without a diffusion barrier. End-of-contact-life (or *contact failure*) occurs when the junction under the contact is short-circuited (e.g., by junction spiking) or when the contact exhibits open-circuit or high-resistance behavior.*

A diffusion barrier used in IC fabrication is a thin film (i.e., material X between materials A and B in Fig. 3-26b) inserted between an overlying metal and an underlying

* Note that diffusion barriers are also used in many other applications besides microelectronics. For example, the paint on wood, the galvanizing on metal, and the wax coating on cardboard containers all serve the same purpose – that is, such barriers are used to protect the underlying materials by preventing diffusion of substances, such as moisture, that would degrade their properties.

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semiconductor material, or between two metals in multilevel metal systems. Such diffusion barriers should have the following characteristics:

- The diffusion of A and B through the barrier should be low.
- The barrier layer should be stable in the presence of A and B, so that very little of the barrier itself is lost through such mechanisms as diffusion into A or B or reaction with A or B.
- The barrier material should adhere well to A and B and should have a low contact resistivity to A and B.
- The barrier should either be compatible insofar as the coefficients of thermal expansion of A and B are concerned, or it should be very resistant to thermal and mechanical stresses.
- Good electrical conductivity (maximum allowable resistivity ~200 $\mu\Omega$-cm).

In practice, the contact-metallization systems of mainstream IC technologies are subjected to maximum temperatures of ~500°C in the course of the final IC fabrication and packaging processes. As a result, some diffusion barriers need to maintain the integrity of contacts at 500°C for 30-60 minutes in order to be useful for such IC technologies. It should be noted that it is difficult to get all of the above listed characteristics in a single material. Since the ideal material, X, is not yet available, compromises must be sought among these characteristics when a diffusion-barrier material is selected.

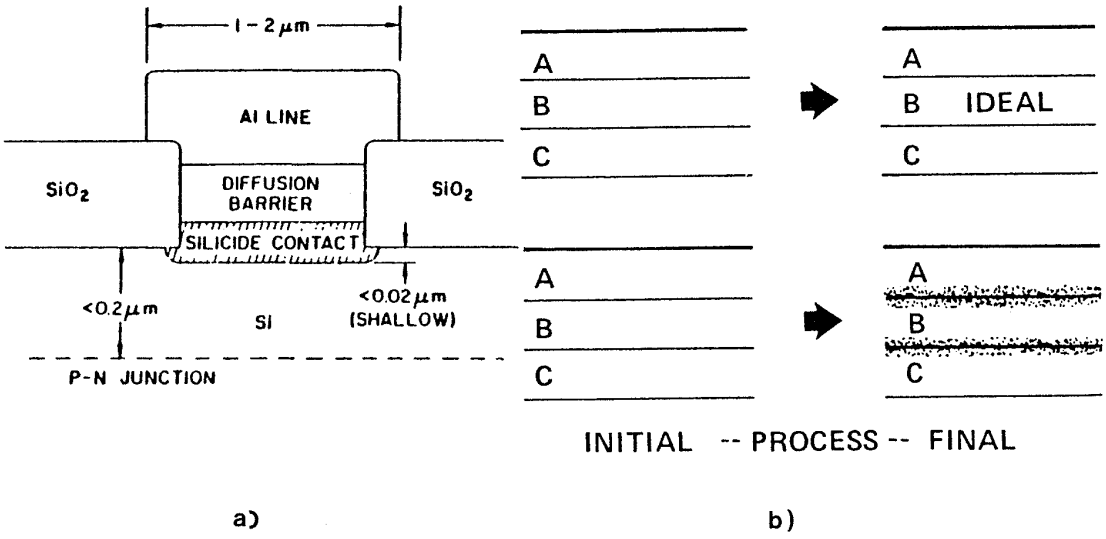

Fig. 3-26 (a) Addition of another layer of material (the diffusion barrier) between the Al and the silicide (or just the Si) to prevent degradation of the contact properties under high temperature processing. (b) Diffusion barrier (material X) reduces intermixing of A and B.

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Nicolet has classified diffusion barriers into three types, according to the mechanisms by which they prevent or retard the diffusion process: *passive barriers, sacrificial barriers,* and *stuffed barriers.*[45]

A *passive barrier* is chemically inert with respect to A and B and has a low solubility for A and B. Materials that generally make good passive diffusion barriers are those that have strong bonds and therefore possess good chemical stability while in contact with other materials. The passive barrier is considered to be probably the ideal diffusion barrier. Nitrides (e.g., TiN), carbides, and borides are examples of materials that could act as such passive barriers, since they exhibit good electrical conductivity, high melting points, chemical inertness, and strong atomic bonds.

A *sacrificial barrier*, on the other hand, is not inert, but it reacts with either A or B. As a result, it can maintain a separation between A and B, but only for a predictable amount of time at a given temperature of operation. The materials A and/or B diffuse into X and form compounds (or material X may diffuse into A or B). If the reaction or diffusion rate is sufficiently slow at the temperature of operation, the expected lifetime of the sacrificial barrier can exceed the predicted lifetime of the device. Once the barrier layer has been totally consumed by the formation of compounds with A and B (or has been dissipated by diffusion into A or B), the barrier characteristic may no longer exist. Polysilicon and titanium films are two examples of sacrificial barriers that have been used in IC fabrication.

A *stuffed barrier* exists when the grain boundaries of the diffusion-barrier films are filled with some other material that blocks diffusion. These grain boundaries would normally be fast diffusion paths, as described earlier in the section on the diffusion of Si in Al polycrystalline films. However, if certain materials are introduced into the film (e.g., during deposition), these materials can become located at the grain boundaries. When the grain boundaries are thereby filled (or "stuffed") with a material, the fast diffusion paths are rendered inoperable. Typically, thin-film impurity concentrations on the order of 1,000 ppm are required to significantly reduce the diffusion rate. An example of a stuffed-diffusion-barrier material is the alloy Ti (10wt%):W, which has been sputter deposited in an ambient containing nitrogen. Nitrogen is thereby incorporated into the film and is thought to stuff the grain boundaries in the manner described.

It is frequently easier to evaluate the efficiency of a diffusion barrier than to establish unequivocally the mechanism by which it operates.[46] Often more than one mechanism may contribute to the effectiveness of a particular barrier material, as is likely the case for the Ti:W diffusion barrier films cited above. That is, once the fast diffusion paths have been preempted (such as by being stuffed with nitrogen in the case of Ti:W), the barrier properties may be more of a function of the inherently high chemical stability of the material. Then the material the material behaves as a highly effective passive barrier.

It should be noted that care must be taken when a barrier layer is deposited into deep, high-aspect-ratio contact windows, to ensure that the minimum required barrier-layer thickness is maintained at the window edges. Thinning at such locations can result in contacts that will fail at lower temperatures than expected. Ultimately, CVD may be needed to provide adequate barrier-layer deposition processes for such applications.

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3.5.2 Materials Used as Diffusion Barriers

Of the various materials investigated as diffusion barriers in ICs, those that have achieved the widest adoption have been Ti:W (sputter deposited), Ti (sputter deposited), polysilicon, TiN, and CVD W.[47] Their properties will be described in more detail here; a brief mention of some other experimental diffusion-barrier materials will also be made at the close of this section.

3.5.2.1 Sputter-Deposited Titanium-Tungsten (Stuffed Barrier).

Titanium tungsten (Ti:W) was among the first materials to be employed as a diffusion barrier, although Ti:W thin films were in fact first introduced by Cunningham et al. in 1970 to improve the thermal stability and corrosion resistance of contacts with gold wire bonding and thermal packaging.[48] In 1978 Ghate et al. described the use of Ti:W as a contact barrier for the ohmic contact structures of bipolar integrated circuits. The shallow emitter-base junctions of bipolar devices were more susceptible to Al spiking than were the NMOS source/drain junctions of that time. Ti:W diffusion barriers were eventually considered for CMOS use when the source/drain junctions of the well devices approached the same shallow depths as those of the bipolar emitter-base junctions.[49]

A typical ohmic contact structure that uses a Ti:W diffusion barrier is shown in Fig. 3-27a. A PtSi layer (50-100 nm thick) is in direct contact with the heavily doped Si regions and is covered with a sputter-deposited Ti:W layer (100-200 nm thick). Finally, a layer of Al (or an Al alloy) is deposited on the Ti:W. When the metal is patterned, the Ti:W remains under the Al layer and thus becomes part of the interconnect structure as well.

While tungsten is by itself a fairly good diffusion barrier,* the Ti is added for several reasons. First, Ti improves the adhesion of the tungsten to SiO_2. Second, it protects the tungsten from corrosion by forming a thin layer of titanium oxide on the surface, making the tungsten an even better diffusion barrier. Finally, the maximum temperature that the contacts can withstand is increased to ~500°C.[47]

Ti:W diffusion-barrier layers are deposited by sputtering, normally from a single target. Such targets are now available in MOS grade – that is, with an alkali metal content as low as that available in Al (1%Si) targets. The nominal composition of the target used in the sputter deposition of Ti:W films is $Ti_{0.3}W_{0.7}$ (10:90wt%). Films deposited from such targets exhibit resistivities of 60-100 $\mu\Omega$-cm, depending on the deposition conditions.

The sputter-deposition process is commonly carried out in an Ar-N_2 ambient, so that nitrogen is incorporated into the Ti:W film.[50] The nitrogen is believed to improve the barrier properties of the film by "stuffing" the grain boundaries, thereby substantially reducing the rate of interdiffusion. In addition, it may decrease the reactivity of the titanium in the film through the formation of TiN. Each of these effects acts to extend

* Reference 47 presents data that contacts made with W as the barrier layer can withstand temperatures of up to 450°C.

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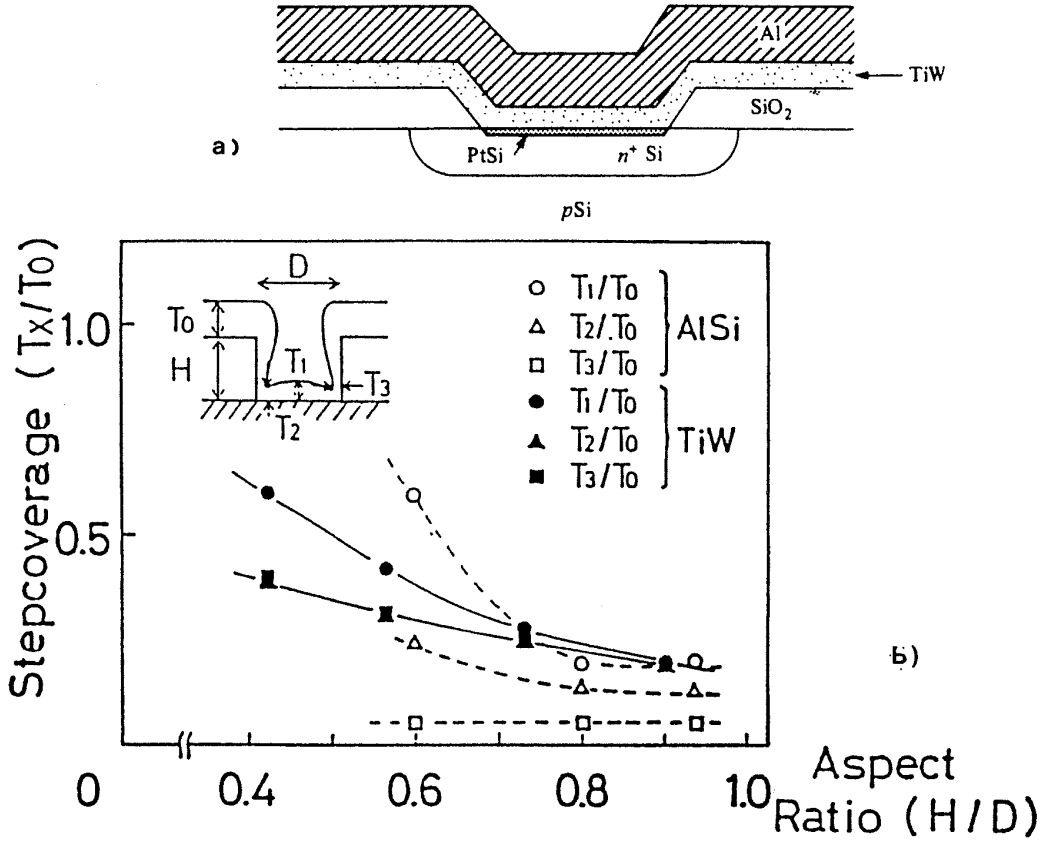

Fig. 3-27 (a) IC contact structure using Ti:W as a diffusion barrier to prevent reaction between PtSi and Al. (b) Comparison of the step coverage of Ti:W (0.6 μm thick) and Al:Si (0.9 μm thick) deposited into a 1.2-μm-wide vertically sided, 0.9-μm-deep contact hole.[143]

the lifetime of the layer. The resistivity of Ti:W is found to increase from 75 $\mu\Omega$-cm in a pure film to 200 $\mu\Omega$-cm when the nitrogen content in the film is 25 at%.[50] This is not of consequence, however, since the resistance of a 100-nm-thick film with this resistivity in a 1-μm^2 contact hole would still be only 0.2 Ω.

The sputter-deposited Ti:W films also exhibit another important advantage for contact structure fabrication. Good step coverage results when these films are sputter-deposited into high-aspect-ratio contact holes. This improves the reliability of the metal interconnects fabricated with Ti:W underlayers.[54] Figure 3-27b illustrates the step coverage of sputtered Ti:W as a function of the aspect ratio of the contact hole opening and shows its superiority with respect to step coverage by sputtered Al.[143]

In the contact-metallization system just described, the Ti:W does not act as a perfect barrier. During annealing, the following reactions with the Al occur:

$$Ti + 3Al \rightarrow TiAl_3 \ (400°C) \qquad (3\text{-}7a)$$
$$W + 12Al \rightarrow WAl_{12} \ (450\text{-}500°C) \qquad (3\text{-}7b)$$

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Interdiffusion is the dominant process that destroys these contact structures. A detailed failure analysis performed by Canali et al.[53] shows that Al begins to diffuse through the Ti:W barrier at 500°C and decomposes the underlying PtSi layer to form the intermetallic compound Al_2Pt with the platinum. At the same time, WAl_{12} forms at the Al/Ti:W interface. Volume expansion due to the Al_2Pt formation causes the Ti:W layer to break up, leading to the dissolution of Si and the growth of WSi_2 and $Ti_xW_{1-x}Si_2$ ternary compounds. It has been observed, however, that little degradation of the contacts occurs when a nitrogen-stuffed Ti:W diffusion layer is subjected to up to a 525°C anneal for 30 minutes.

If the Ti:W is used as a contact layer (i.e., without an underlying PtSi layer) with an overlying Al layer, the incorporation of nitrogen is also found to reduce the contact resistance to n^+ Si but to increase the contact resistance to p^+ Si. In one report, a 550°C anneal was needed before a Ti:W layer deposited directly on Si could dissolve the native-oxide layer.[51] Alloying at a temperature of 625°C was necessary to obtain the lowest value of specific contact resistivity to p^+ Si. This annealing temperature would be problematic if an Al layer were present on the Ti:W. It was also noted that low contact resistivity by Ti:W to n^+ Si was nevertheless achievable at the lower annealing temperature of 400°C.

In another report, a multistep surface-preparation routine (after contact holes have been dry-etched in SiO_2) was used to reduce the contact resistance of Ti:W in direct contact with Si by a factor of 4. The specific contact resistivity of Ti:W to p^+ Si was reduced to $\sim 1 \times 10^{-6}\ \Omega\text{–cm}^2$ following a 450°C anneal.[14] The silicon surface at the bottom of the contact holes was first cleansed of any polymers (that may have been deposited during the contact opening process through an oxygen plasma), and then was subjected to a 1000°C RTP anneal for 10 seconds in nitrogen. This served to repair any surface damage that might have been produced during dry etching. Next, the wafer was dipped in a 1% HF solution for 1 minute just prior to being loaded into the sputter chamber for metal deposition. Another paper reported low contact resistance between Ti:W and n^+ and p^+ Si following furnace anneals of 440°C in N_2 for 30 minutes.[52]

However, the use of Ti:W also has a major drawback for VLSI and ULSI processing, in that the film is quite brittle and highly stressed upon being deposited. Although these stresses can be sufficiently reduced so that problems on the wafer can be avoided, the film that is deposited on the walls of the sputtering chamber eventually reaches a thickness at which the stress causes it to begin to flake off (or *spall*). Such particulates can significantly reduce yield; for large chips this effect may produce unacceptably large yield loss.

3.5.2.2 Polysilicon (Sacrificial Barrier). A thin layer of polysilicon can be used to separate the Al and single-crystal Si substrate (Fig. 3-28).[55] The polysilicon layer in such contact structures serves as a sacrificial diffusion barrier that protects junctions beneath the contact from undergoing contact-electromigration failure. Under high current stresses, Si from the polysilicon (rather than from the substrate) is transported into the Al. Consequently, void formation in the substrate (which would lead to junction spiking) is prevented. This contact structure is attractive because it

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exploits a technology already developed for buried contacts, and because it avoids the use of materials other than Al and Si. The phosphorus-doped polysilicon film (200-300 nm thick) is deposited following the opening of the contact holes, but prior to the deposition of Al:Cu (0.5 wt%). After the Al:Cu-polysilicon film has been patterned, the contact structure is annealed.

Although this structure alleviates the problem of contact-electromigration failure of Al:Si-Si contacts to some degree, such failures still occur at rates higher than those due to interconnect electromigration failures. In addition, the contact resistance of the n^+-doped polysilicon to Si is ~50 times as large as that exhibited by Al:Si-to-Si after a 450°C anneal,[56] and the interconnect structures are still prone to the problems caused by silicon precipitates in the Al lines. Furthermore, while this contact structure is easy to integrate into NMOS technology, it is not as compatible with CMOS. In order for it to be used it with CMOS, the polysilicon underlayer must be doped p-type wherever contacts to p-channel devices are needed. This requirement introduces all of the problems associated with the use of dual-doped polysilicon, as described in chapter 6.

3.5.2.3 Titanium (Sacrificial Barrier). Titanium films have also been used as diffusion barrier. Ti is an oxygen-gettering material and oxide-reducing agent, which causes it to dissolve the native oxide layer on the Si surface during annealing and to adhere well to both Si and SiO_2. In addition, because the Schottky-barrier height of Ti on n-Si is about half the silicon band gap, Ti can form good ohmic contacts to both types of heavily doped Si. In fact, the contact resistivities of Al-Ti-Si contacts are comparable to those of PtSi-Si contacts.

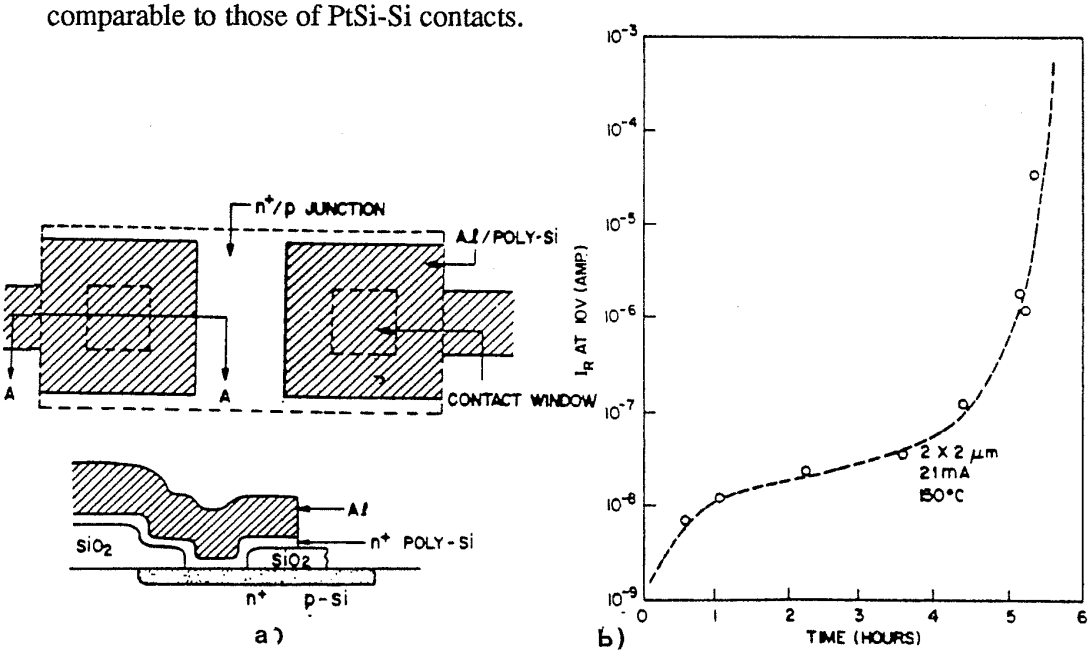

Fig. 3-28 Al-polysilicon-Si contact structure. (a) Layout and cross section. (b) Junction leakage after passing 21 mA at 150 °C through a 2 x 2 μm contact hole versus time.[55] Copyright 1981. Reprinted with permission of the AIOP.

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The Ti layer between Si and Al behaves as a sacrificial barrier because it reacts with Al to form $TiAl_3$ at temperatures above 400°C. Ti is a reasonably good diffusion barrier for Si below 500°C, and as long as the Ti is not completely consumed, this barrier property is maintained. Although Ti is not as good a diffusion barrier for Al, the diffusion of Al through the Ti into the Si does not lead to the destruction of the contact since the diffusivity and solid solubility of Al in Si are quite low. Once the Ti has completely reacted to form $TiAl_3$, however, its diffusion barrier properties are lost, and the contacts rapidly fail. The reaction kinetics of Al and Ti were first described by Bower in 1973.[57]

If Ti is selected as a diffusion barrier, a thick enough layer must be used to ensure an adequate lifetime at given fabrication and operating conditions. It has been determined that a 100-nm-thick Ti film can withstand 500°C for 15 minutes and 477°C for 30 minutes;[58] at 425°C, contact failure was observed after 6 hours.[59]

3.5.2.4 Titanium Nitride (Passive Barrier). The use of the TiN layer as a diffusion barrier was first proposed by Nelson in 1969.[60] The first successful application in devices was reported in 1979 by Garceau et al., who used TiN between Ti and Pt in the Au-Pt-Ti-Si beam-lead metal system.[61] Wittmer reported on the diffusion-barrier properties of TiN for silicon devices in 1980.[62]

TiN is an attractive material as a contact diffusion barrier in silicon ICs because it behaves as an impermeable barrier to silicon, and because the activation energy for the diffusion of other impurities is high (e.g., the activation energy for Cu diffusion into TiN thin films is 4.3 eV, whereas the normal value for diffusion of Cu into metals is only 1 to 2 eV). TiN is also chemically and thermodynamically very stable, and it exhibits one of the lowest electrical resistivities of the transition metal carbides, borides, or nitrides (all of which are chemically and thermally stable compounds).

The specific contact resistivity of TiN films to Si is somewhat higher than that of Ti or PtSi ($\sim 10^{-5}\ \Omega\text{-cm}^2$), and as a result it is ordinarily not used to make direct contact to Si. Instead, it has most commonly been used in a contact structure consisting of Al-TiN-Ti-(or $TiSi_2$)-Si. Such contact structures exhibit very low specific contact resistivities to Si and remarkably high thermal stability, with the ability to withstand temperatures up to 550°C without contact failure. The methods used to form TiN are described in section 3.6.2, which details the characteristics of Al-TiN-Ti-Si contacts. A report on the barrier properties of reactively sputter-deposited TiN as a function of deposition conditions, however, is given in reference 63. Another report indicates that the incorporation of oxygen into TiN films increases the barrier properties of these films, at the expense of a somewhat increased contact resistivity.[64] Al-TiN-Ti-Si contacts have also been reported to exhibit much less susceptibility than Al:Si-Si contacts to contact electromigration failure.

3.5.2.5 CVD Tungsten. Chemically vapor-deposited tungsten (CVD W) has been investigated for a variety of applications in both metal-Si contacts and interconnect structures. In this section we consider both its applicability as a diffusion barrier and its

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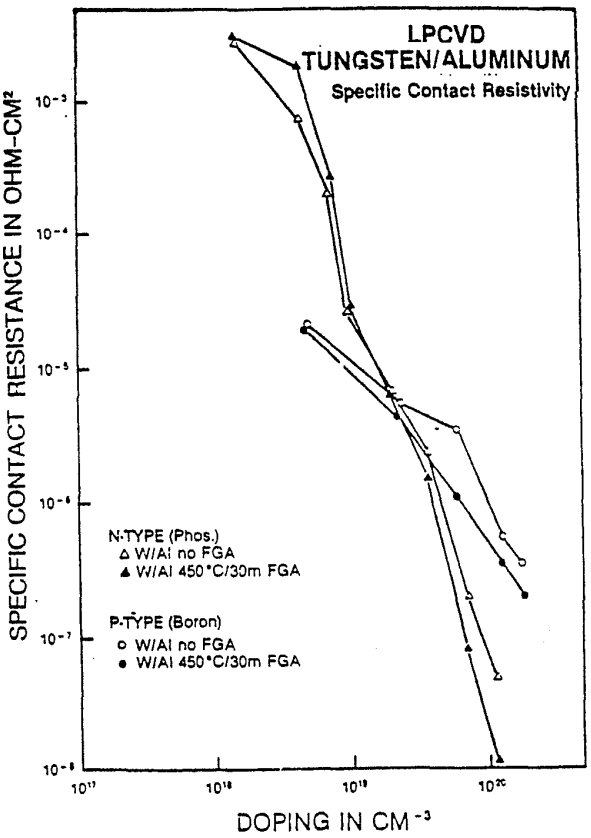

Fig. 3-29 Specific contact resistivity of LPCVD tungsten (covered with an Al layer) to n-type and p-type Si.[162] (© 1984 IEEE).

usefulness as a material for making direct contact to Si. The details of CVD W deposition and etching, as well as the application of CVD W as an interconnect material and as a material for filling contact holes and vias, will be considered in chapter 4.

Selective CVD W has been investigated for direct contact formation to Si (Fig. 3-29). This process appears attractive for many reasons. First, specific contact resistivity can be very low to n^+ Si, and reasonably low to p^+ Si.*

* Such low contact-resistivity with selective CVD W is achieved only if the silicon surface is clean and reasonably free of a native-oxide layer. If the native oxide is less than 10°A thick, low-resistance contacts will be reliably fabricated, and the Si consumed during the deposition process is self-limited to ~100 °A. (Note that if the native oxide is removed from a Si surface by an HF dip, it takes ~2 hours for it to regrow to a thickness of 10 °A. Thus, if the wafers are loaded into the CVD chamber and W is selectively deposited within that time, good contacts can be repeatably produced.) However, if the native oxide is >10 °A thick, not only will the selective CVD W process produce higher resistance contacts, but the W film will be rough and more Si will be consumed from the substrate (up to 300 Å).

The polymer film that is produced when contact holes are opened by dry etching must also be removed prior to CVD W deposition. If the polymer film is allowed to remain in place,

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Second, the W can simultaneously serve as a barrier layer. CVD W layers covered with Al have been found to be able to withstand temperatures of up to 500°C without undergoing significant reaction with the Al.[65] Third, selectively deposited W can partially or completely fill contact holes, thereby easing the problem of step coverage by the first-level metal layer into the contact hole. Finally, as mentioned in the footnote, the Si consumption is self-limiting at ~100 °A if the native oxide layer is less than 10 °A thick. This is an advantage over $TiSi_2$ and $CoSi_2$ contacts (see section 3.9.1). That is, when such silicide contacts are formed, the Si consumption is not self-limiting, but depends on the thickness of the Ti or Co that is deposited before the silicide reaction is carried out.

In spite of the significant benefits offered by the selective CVD W process, concerns have been expressed about some of the side effects observed under certain deposition conditions. Specifically, when W is selectively deposited by the hydrogen reduction of WF_6, lateral encroachment of the W under the Si-SiO_2 interface can occur, and wormholes are occasionally observed at the Si surface (see Vol. 1, chap. 11). Both of

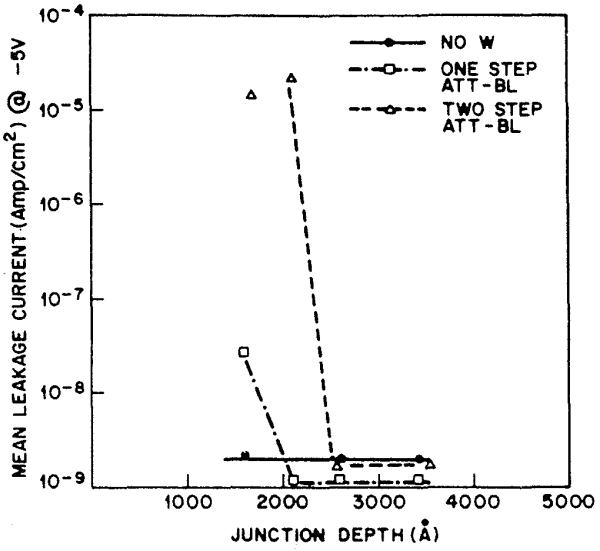

Fig. 3-30 Comparison of mean leakage current density vs. n^+ (As/P) junction depth in Si for contacts fabricated with no W and for W deposited with the hydrogen reduction process.[70] This paper was originally presented at the Spring 1988 Meeting of The Electrochemical Society, Inc. held in Atlanta, GA.

poor contacts are likely to be formed. To ensure polymer layer removal, a slight silicon etch that removes ~100 °A of Si is recommended. (It is not clear whether the etch undercuts the polymer layer, or removes it directly, but at the end of this so-called *silicon polishing procedure*, the polymer layer is gone.) The silicon polishing procedure should be performed in situ as the last step of the dry etch process used to etch the contact holes. This will also ensure good CVD W-to-polysilicon contacts when such contacts are opened at the same time as those to the Si substrate.[157]

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these effects can produce junction leakage (Fig. 3-30).

A variety of techniques for reducing wormhole formation,[66] and encroachment have been studied.[67] One of the most promising approaches involves formation of selectively deposited W films using SiH_4 reduction of WF_6 (see chap. 4, section 4.5.4.1).[68,69] This process results in minimal erosion of the Si and minimal encroachment of the Si contacts, as well as the formation of W films with smoother surfaces than those obtainable by the hydrogen reduction process. Although it has been reported that leakage may still occur when junction depths are less than 200 nm deep,[70] more recently, other evidence has been presented that this problem can be eliminated in such shallow junctions using silane reduction of WF_6. Thus, selective CVD W appears to be a very promising technique for forming contacts directly to Si in submicron IC technologies.

Two other aspects of selective CVD W should also be mentioned. First, commercial equipment must be available in which the silane reduction of WF_6 process can be performed. Several equipment vendors have introduced new models with this capability, and others are sure to follow suit. Second, the value of ρ_c of CVD W to p^+Si is still significantly higher than that of Al:Si or PtSi to p^+Si; a lower value would improve the characteristics of CVD W as a contact material.

3.5.2.6 Experimental Diffusion Barrier Materials. Among other experimental materials that have demonstrated diffusion barrier capabilities are Mo_xNi_{1-x}[71] and $Fe_{0.45}W_{0.55}$.[72] Note that these materials may be good for high-temperature applications, together with the transition-metal carbides (e.g., Ti_xC, $x = 3.1$)[73] and the transition-metal borides (e.g., TiB_2).[46]

An additional category of materials being investigated for use as diffusion barriers is that of *amorphous thin-film* materials.[74] These are unlike the other diffusion-barrier materials thus far considered, which are polycrystalline in structure (and hence contain grain boundaries, which represent potential paths for rapid diffusion). Amorphous materials can exhibit smaller diffusion coefficients than comparable polycrystalline materials. For example, at 400°C, the diffusion coefficient of Au in amorphous $Ni_{0.45}Nb_{0.55}$ is reduced to less than 10^{-21} cm^2/sec, from 1.6×10^{-15} cm^2/sec in a poly-crystalline alloy of $Ni_{0.45}Nb_{0.55}$. The absence of grain boundaries is also expected to reduce the susceptibility of the contact structures to failure due to electromigration effects.

3.6 MULTILAYERED OHMIC-CONTACT STRUCTURES TO SILICON

Earlier, we showed why the simple Al-to-Si contact structure had to evolve into a variety of more complex contact structures. In some such structures, the material used as the diffusion barrier is also utilized to form a direct contact to Si (e.g., Al-polySi-Si, Al-Ti-Si, Al-Ti:W-Si, and Al-CVD W-Si). These have been discussed previously. In

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the most complex contact structures, more than one material is used to separate the Al and Si. This section will describe those of the latter type that have been widely adopted.

3.6.1 Al-Ti:W-PtSi-Si Contacts

The Al-Ti:W-PtSi-Si system (Fig. 3-27) has been a workhorse contact structure for bipolar ICs since the late 1970s. It exhibits low contact resistance to n^+ and p^+ Si, and it can withstand temperatures of up to 500°C. It also provides excellent protection against contact electromigration failure. The main reasons that MOS technologies did not adopt such contact structures were the higher defect density associated with Ti:W deposition, the increased process complexity needed to form the contact structures, and the nonavailability of low-Na Ti:W sputtering targets (although such targets now exist).

3.6.2 Al-TiN-Ti-Si Contacts

This contact structure (with the Ti layer ranging from 30-80 nm in thickness, and the TiN from 100-200 nm) has recently been studied with a great deal of interest. When TiN is used as a diffusion barrier between Ti and Al, the thermal stability of the contacts is excellent (annealing temperatures of 500°C or more can be tolerated), and the contact resistivity is good (10^{-6} Ω-cm^2), although not quite as low as with contacts that use PtSi.

The Ti promotes good adhesion to SiO_2, and it forms $TiSi_2$ by reacting with the Si substrate during the anneal step. During this step, however, large quantities of dopant from the Si substrate (particularly boron) can be absorbed by the $TiSi_2$ as it is being formed. If this dopant loss is not controlled, high contact resistance can result. (This is an especially serious problem if $TiSi_2$ is used to connect *n*-type to *p*-type polysilicon.) It is possible to limit the dopant loss by minimizing the the amount of $TiSi_2$ allowed to form. This can be achieved by using a very thin layer of Ti covered with the TiN diffusion layer.[137]

The TiN layer can be formed in one of five ways: by evaporating the Ti in an N_2 ambient;[47] by reactively sputtering the Ti in an Ar + N_2 mixture;[75] by sputtering from a TiN target in an inert (Ar) ambient;[76] by sputter depositing Ti in an Ar ambient and converting it to TiN in a separate plasma nitridation step;[77] or by CVD.[126] The simultaneous formation of $TiSi_2$ and TiN following a deposition of Ti is also described in several reports.[78]

In another variation of this contact structure, a layer of Ti (75 nm) and a layer of W (100 nm) are sequentially sputter deposited, followed by an anneal in N_2 at 650°C for 20 minutes. The Ti at the Si interface is converted to $TiSi_y$, and the Ti near the W interface to TiN_x. Such contacts exhibit good stability even after an eight-hour anneal at 400°C.[79]

In some other processes, improved filling of the contact holes is achieved by coating the wafers with a nonselective CVD W layer that results in good step coverage in the contact holes.[19] An etchback step is performed to remove this W film in the SiO_2 field regions and to achieve a planar surface at the contact holes. When the CVD W plug

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process is not used, the Ti-TiN is patterned and becomes a part of the Metal 1 film as well. A report on the behavior of such contacts (both with and without the additional W film), under high current stressing (to induce contact-electromigration failures) is given by Fu and Pyle.[80]

In another article, it was reported that if the Al-TiN-Ti-Si contact is made to a shallow BF_2^+-implanted region, high leakage currents could result as a result of the thinning effect of the TiN at the contact-hole edges. That is, Al can react with the Si through pinholes in the TiN at these locations. If the Al is replaced with Al:Si, however, excellent leakage characteristics are observed.[81] In addition, it has been observed that the Ti layer in such contacts should be between 50 and 80 nm thick when used with a 0.2-μm-deep junction. In this case, the $TiSi_2$ that is formed will be thick enough to entirely consume the damaged Si layer caused by the BF_2 implant, but not so thick as to penetrate beyond the 0.2-μm-thick junction.

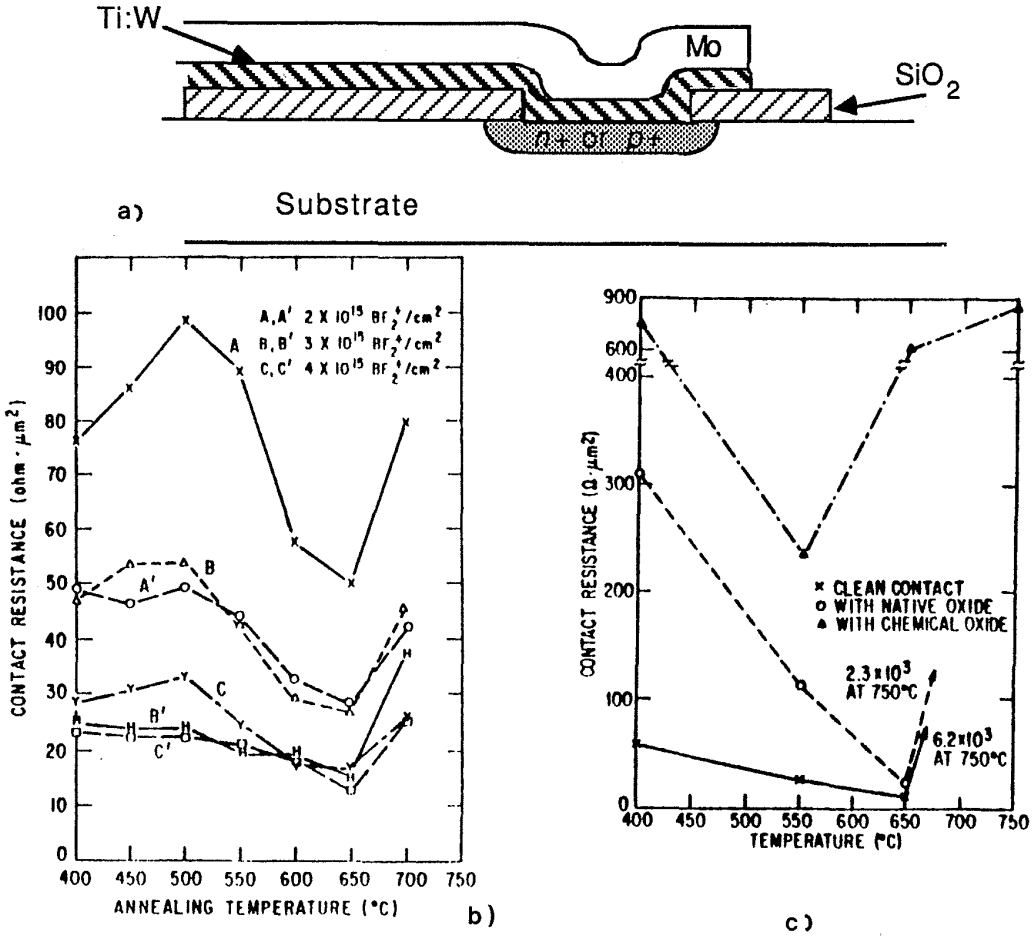

Fig. 3-31 Mo-Ti:W-Si contacts. (a) Structure cross section. (b) Effect of isochronal annealing on the p^+ contact resistance versus BF_2^+ implant dose. (c) Contact resistance change to n^+ Si as a function of isochronal annealing temperature with and without interface oxide.[82] Reprinted by permission of the publisher, The Electrochemical Society, Inc.

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3.6.3 Mo-Ti:W-Si and Mo-Ti-Si Contacts

The contact structures described in sections 3.6.1 and 3.6.2 exhibit satisfactory contact properties for VLSI applications, but at the price of increased process complexity. Somewhat simpler contact structures that exhibit equally good characteristics would therefore be attractive. The Mo-Ti:W-Si[82] and Mo-Ti-Si[83] systems have been suggested as two alternative candidates (Fig. 3-31), since such structures exhibit good stability when exposed to temperatures exceeding 500°C (i.e., up to 650°C), and both are able to form low-resistance ohmic contacts to Si. The double-layer film that constitutes the contact structure can also serve as an interconnect layer, provided that it is restricted to the first level of a multilevel-metal scheme. The difficulty of bonding to Mo thin films requires that Al be used for the final metal (i.e., bonding-pad) layer.

In the Mo-Ti:W-Si contacts, an 80-nm-thick Ti:W film is sputter deposited; this is followed by the deposition of a 300-nm-thick Mo layer, in one pump-down. The wafers are allowed to cool before being exposed to atmosphere in order to prevent formation of an oxide on the Mo. After the patterning of the bilayer, the contacts are sintered. It is reported that the ρ_c of Ti:W to p^+Si reaches a minimum after a 625°C anneal (50 Ω–μm^2). Since such a high-temperature-anneal step must be used, a metal other than Al must be selected as the top layer of this structure (Fig. 3-31b). Since Mo has a melting point of 2620°C, it can successfully replace Al for this application. Both the leakage current of the contact structure and the sheet resistance of the bilayer remain low after the 625°C anneal. The Ti:W appears to be capable of dissolving up to 1.5 nm of native oxide during the contact-annealing step, allowing the low-resistance ohmic contacts to Si to be formed.

In the more recently reported Mo-Ti-Si contacts, a 40-80-nm-thick sputtered Ti layer is used instead of Ti:W and is covered with a sputtered Mo layer. This bilayer is etched by means of an RIE process using a mixture of SF_6 and O_2 gas. After being subjected to a 600°C anneal, these contacts exhibit lower ρ_c values than do the Mo-Ti:W-Si contacts (ρ_c = 10 Ω–μm^2 to n^+Si and 20 μm^2 to p^+Si). In addition, the Ti layer dissolves native-oxide layers more reliably than does Ti:W. Finally, a pure Ti sputter target can be used instead of a Ti:W target. Ti:W targets are generally fabricated from a hot-pressed mixed powder, which has a greater probability of being impure than a single-element Ti target: the Ti:W target can also occasionally produce particles.[83]

3.7 SCHOTTKY-BARRIER CONTACTS

Schottky barriers are used in a variety of device and circuit applications. One of the most important utilizes the *Schottky-barrier diode* to increase the switching speed of bipolar transistors. Figure 3-32 shows how it is connected in parallel with the collector-base junction of the transistor for this purpose. In this configuration, the *turn-on voltage*, V_F, of the Schottky diode is lower than that of a silicon *pn* diode (i.e., V_F is the voltage at which a particular current, I_F – for example 1 mA – flows through the diode). The lower value of V_F and the charge-storage properties of the metal-semicon-

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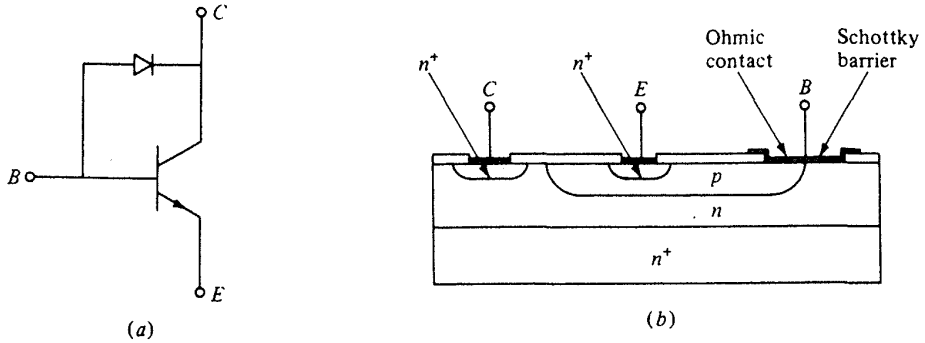

Fig. 3-32 Schottky clamped transistor: (a) circuit representation and (b) integrated structure.

ductor junction are exploited to reduce the transistor switching speed. (Additional information on Schottky-barrier applications in bipolar integrated circuits is given in chap. 7.)

The forward I-V characteristics of a Schottky-barrier diode are given by:

$$I = I_s \{ [\exp(qV/n\,kT)] - 1 \} \qquad (3-8)$$

where

$$I_s = RT^2A \exp\{ -q\,\varphi_b/kT \} \qquad (3-9)$$

and I is the current through the Schottky diode, V is the external voltage applied across it, A is the area of the diode, T is the temperature (in kelvins), R is Richardson's constant (120 $A/cm^2\text{-}K^2$), φ_b is the Schottky-barrier potential difference, and n is the ideality factor.

For the case of $V > 3kT/q$

$$I \approx I_s \exp\{qV/nkT\} = RT^2A \exp\{ (q/kT)(V - \varphi_b) \} \qquad (3-10)$$

or

$$(\varphi_b - V) = (kT/q) \ln\{ (RT^2A)/I \} \qquad (3-11)$$

For design purposes, it is necessary that Schottky diodes exhibit a stable value of V_F. Therefore, from Eq. 3-11 we can see that if φ_b is not stable (i.e., if it varies for some reason, possibly due to a dependence on the maximum thermal anneal temperature, on the Si surface-contamination condition, or on time during normal operating conditions), the value of V_F for a fixed value of I_F would have to vary as well. As a result, it must be possible to produce a constant barrier height for a Schottky-barrier diode in a production environment, and that barrier height value must remain stable under further device fabrication and operating conditions.

PtSi is the material most commonly used for fabricating Schottky-barrier diodes to lightly doped *n*-Si (i.e., when $N_c \leq 10^{17}$ cm^{-3}). This is due to the overall reliability with which PtSi-Si contacts can be fabricated, compared to the other candidate structures. Since any contaminants that are present at the original Si interface are swept up to the silicide surface during the formation reactions, a very clean silicide-Si interface is formed, ensuring the reproducibility of the Schottky-barrier height. In addition, the

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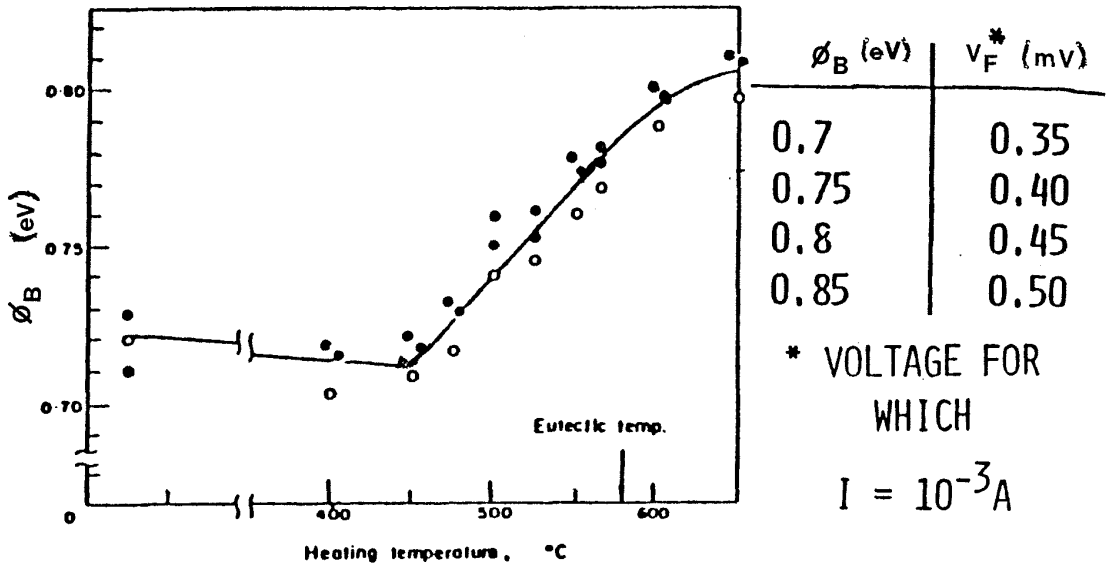

Fig. 3-33 (a) Barrier heights of Al-Si Schottky barrier diodes as a function of the heating temperature. (b) V_F (voltage at which the forward bias current in a Schottky diode = 1 mA) as a function of ϕ_b.

agglomeration of PtSi layers occurs at ~825°C, whereas, for example, Pd_2Si layers agglomerate at lower temperatures (700°C).

The Al-Si system forms a poor Schottky-barrier contact because its Schottky-barrier height varies with heating temperature (as shown in Fig. 3-33). This is due to the interdiffusion of Al and Si, as described in an earlier section of this chapter. Figure 3-33 also shows how V_F would change as the barrier height of the Al-Si Schottky contact varied from 0.7 to 0.85 V, eliminating such structures from being considered for Schottky diode applications in IC production.

The Schottky-barrier height of PtSi to *n*-Si has a value of 0.84 eV. This value will remain stable to temperatures of 500°C or more if a suitable diffusion barrier (such as Ti:W or TiN) is interposed between the PtSi and Al. In a bipolar *npn* transistor, a PtSi layer can therefore be used to form an excellent Schottky barrier to the lightly *n*-doped collector region, as well as to form an exemplary ohmic contact to the heavily *p*-doped base region (as shown in Fig. 3-32). Both of these contacts can be fabricated simultaneously by means of a single, maskless metallization procedure (akin to the one described in the earlier section on PtSi-Si ohmic contacts). It should also be noted, however, that the low Schottky-barrier height of PtSi to *p*-type Si (0.25 eV) causes such contacts to exhibit ohmic behavior even when the Si is relatively lightly *p*-doped. This has prevented Schottky contacts to *p*-type Si from being implemented in IC technologies.

Three examples of Schottky-barrier device structures are shown in Fig. 3-34. In the first (Fig. 3-34a), ideal Schottky-barrier characteristics are not obtained because of the sharp edge and the positive fixed charges that exist at the Si-SiO_2 interface. These conditions create a high electric field in the depletion region in the semiconductor near

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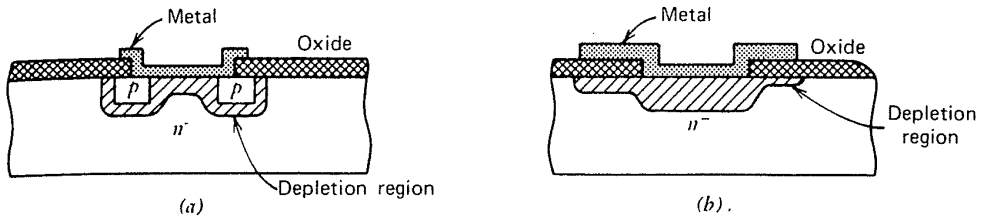

Fig. 3-34 Special processing techniques improve the performance of Schottky diodes. (a) The diffused guard ring leads to a uniform electric field and eliminates breakdown at the junction edge. (b) The field plate is an alternative means for achieving the same effect. From R. S. Muller and T. I. Kamins, 2nd Ed., *Device Electronics for Integrated Circuits*. Copyright 1986, John Wiley & Sons. Reprinted with permission.

the periphery, which leads to excess current at the corners, a soft reverse-bias characteristic, and a low breakdown voltage. Such problems can be eliminated by allowing the metal to overlap the oxide (Fig. 3-34b) or by diffusing a p^+ guard ring around the periphery of the Schottky structure (Fig. 3-34c). The overlapped metal structure is preferred in IC processes because it is less complex to fabricate.

3.8 THE IMPACT OF THE INTRINSIC SERIES RESISTANCE ON MOS TRANSISTOR PERFORMANCE

The intrinsic series-resistance components of metal-to-Si contact structures were introduced earlier in this chapter, and a discussion followed on how to establish the value of R_{co}. In this section we undertake a discussion of the remaining intrinsic series components of the MOSFET (R_{sh}, R_{ac}, and R_{sp}) and describe under what circumstances these effects (when combined with R_{co}), significantly impact device performance. The impact of the parasitic series-resistance effects on the bipolar transistor is presented in chapter 7.

3.8.1 The Impact of R_S on MOSFET Performance

The series resistance, R_S, of the MOS source and drain regions should be small compared to the resistance of the channel, R_{ch}, in order for degradation of the device characteristics to be avoided. In the past, when larger design rules were used, R_S was a minor component of the total MOS resistance of a turned-on device. As devices got smaller, the channel impedance became smaller, while R_S grew larger (because of shrinking contact sizes and shallower source/drain junction depths). It therefore became necessary to determine whether R_S might become a significant fraction of the total MOS resistance. Under such circumstances, R_S would degrade the device performance in a number of ways. For example, I_{Dsat}, g_{msat}, V_{GS}, and V_T would all be reduced (see chap. 5).

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Since the benefits of making devices with smaller channel lengths are so vital, it is important to find ways to design devices so that these smaller lengths can be obtained without degrading device performance through an increase in the value of R_S. The maximum value of R_S (relative to R_{ch}) that can be tolerated in MOS devices should thus be identified, and then process and device technology developed to achieve such allowable R_S values. One proposed constraint is that R_S be kept at less than 10% of R_{ch}. Although this 10% percent limit may seem arbitrary, it is approximately equal to the ratio of R_S to R_{ch} in MOS devices fabricated with a typical 1.0-μm process. Therefore, maintaining this ratio as devices shrink is a reasonable goal. We will report here on how the values of the component resistances of R_S are estimated to change as device dimensions are scaled.

To begin, we present a modified form of the relation used to calculate the *MOS channel resistance*, R_{ch} (normalized to unit width, and therefore expressed in units of Ω-μm), when the device is in the linear region of the MOS characteristics. The value of R_{ch} in the linear region is chosen because it is the worst case comparison with R_S (i.e., the channel resistance of an MOS device in saturation is larger than when the device is in the linear region; see chap. 5).

$$R_{ch\ (linear\ region)} = [L_{eff} + V_{DS}]/[\mu_o C_{ox} (V_{GS} - V_T - 0.5\ V_{DS})] \qquad (3 - 12)$$

The terms in this equation are defined in chapter 5, but for the case at hand we merely graph the values of R_{ch} versus channel length for NMOS devices and PMOS devices (Fig. 3-35), assuming $V_{GS} = 5$ V. We also show the 10% value of R_{ch} in these figures. We note that as the devices get smaller, the value of R_{ch} also decreases. These graphs indicate that the maximum allowed values for R_S for submicron devices will be in the 300-500 Ω-μm range.

3.8.2 Estimates of R_{sh}, R_{sp}, R_{ac}, and R_{co}

Let us examine the components of R_S in Eq. 3-1 (R_{sh}, R_{ac}, R_{sp}, and R_{co}), and see how their estimated values compare with the maximum allowed values of R_S. The information used to estimate the values of these parasitic resistances is based on the analysis presented by Ng and Lynch in references 84 and 85.* Other analyses predicting R_S have also been performed, but an earlier model was used to estimate the values of R_{sp} and R_{ac} leading to somewhat different results from those given here.[86,87] Because it is believed that Ng and Lynch's model treats the effects of R_{sp} and R_{ac} more correctly, it is their conclusions that are presented here. The basis of their analysis is that as the devices are scaled, the physical and electrical parameters of the device will also be scaled. Figure 3-36 gives the values of these scaled parameters as the device channel length is reduced from 0.7 to 0.15 μm. This analysis also assumes that the power-supply voltage will scale as the square root of the channel length.

The *diffusion sheet resistance*, R_{sh}, is calculated using the formulas

$$R_{sh} = \rho_{sh}\, S/W \qquad (3 - 13)$$

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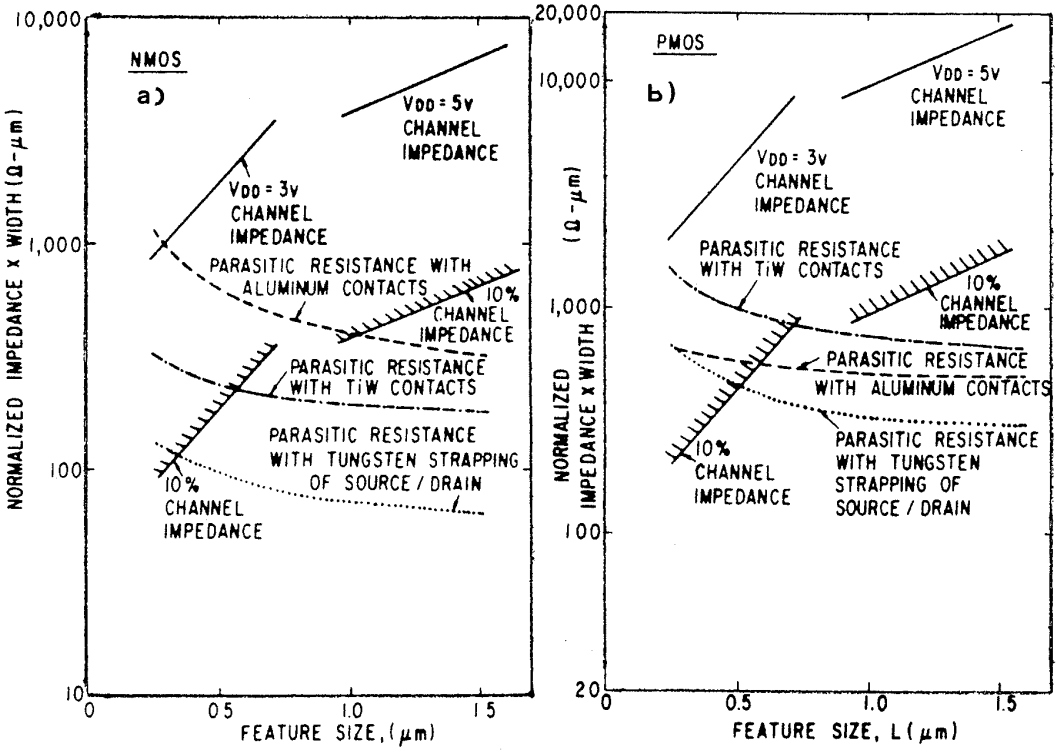

Fig. 3-35 Plot of minimum channel resistance and parasitic series resistance versus design rule feature for (a) NMOS, and (b) PMOS. The parasitic resistances are calculated for three different contact technologies: 1) Al - - - ; 2) Ti:W alloy - · - · ; and 3) self-aligned W strapping of source/drain ·····).[86] (© 1986 IEEE).

and

$$\rho_{sh} = \rho/X_j \qquad (3-14)$$

where ρ_{sh} is the sheet resistance in ohms per square, ρ is average bulk resistivity in the n^+ or p^+ layer, W is the device width, and S is the distance from the edge of the channel to the leading edge of the contact window (see Fig. 3-1). For example, in a PMOS device, R_{sh} is calculated to be ~65 Ω-μm if the device has an effective channel length of 0.7 μm, a minimum drawn channel length of 1.01 μm (which dictates that a value of W = 1.01 μm be used in Eq. 3-13), ρ_{sh} = 132 Ω/sq, and S = 0.5 μm.

The analysis of Ng and Lynch estimates that R_{sh} will not significantly contribute to R_S in submicron MOSFETs with gate lengths down to 0.15 μm because they predict that the bulk resistivities used in Eq. 3-13 will remain essentially constant, at the values of 0.001 and 0.0033 Ω-cm for n^+ and p^+ materials, respectively.[85] As a result, R_{sh} values are also predicted to remain essentially constant, at ~20 Ω-μm and ~60 Ω-μm in n- and p-channel MOSFETs, respectively, as the effective channel length is

* Measured values of the extrinsic drain resistance of MOSFETs with silicided p^+ and n^+ source/drain regions have recently been published.[166]

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SCALED PHYSICAL AND ELECTRICAL PARAMETERS USED IN THIS STUDY

L_c (μm)	V_{dd} (V)	V_t (V)	N_c (cm^{-3})	T_{ox} (Å)	X_j (μm)	L_{mask}* (μm)	K(scaled) (cm^{-1})	K(const) (cm^{-1})	S (μm)	$\rho_D(n^+)$ ($\Omega/\square$)	$\rho_D(p^+)$ ($\Omega/\square$)
0.70	3.00	0.75	5×10^{16}	276	0.25	1.01	2.0×10^{6}	2.0×10^{6}	0.5	40	132
0.60	2.78	0.70	6.5×10^{16}	225	0.22	0.82	2.3×10^{6}	2.0×10^{6}	0.4	45	150
0.50	2.54	0.64	8.9×10^{16}	175	0.20	0.65	2.5×10^{6}	2.0×10^{6}	0.35	50	165
0.40	2.27	0.57	1.3×10^{17}	129	0.17	0.48	2.9×10^{6}	2.0×10^{6}	0.3	59	194
0.30	2.00	0.50	2.2×10^{17}	86	0.14	0.32	3.6×10^{6}	2.0×10^{6}	0.25	71	236
0.20	1.60	0.40	4.5×10^{17}	48	0.10	0.18	5.0×10^{6}	2.0×10^{6}	0.2	100	330
0.15	1.40	0.35	7.8×10^{17}	31	0.07	0.12	7.1×10^{6}	2.0×10^{6}	0.15	143	471

Fig. 3-36 Scaled physical and electrical parameters in the study of parasitic series resistance components on MOS transistor performance.[85] (© 1987 IEEE).

scaled from 0.7 μm down to 0.15 μm. Note that since X_j and S are both scaled to the same extent, R_{sh} remains constant if ρ is assumed to stay constant. This result is graphed in Figs. 3-37a and 3-37b.

The values of the *accumulation-layer resistance*, R_{ac}, and *spreading resistance*, R_{sp}, were calculated together as a single quantity by Ng and Lynch,[84] using a model they derived. This model incorporates the doping gradient near the junction, whereas an earlier model assumed an abrupt doping profile.[88] Thus, their estimated values were significantly different than those obtained with the previous model. In particular, their results show that the values of (R_{sp} + R_{ac}) depend critically on the steepness of the doping profile, K. Specifically, in order to obtain minimum values of (R_{ac} + R_{sp}), the junction profile should be as steep as possible.

The model also estimates that (R_{ac} + R_{sp}) will decrease with shrinking channel length. The predicted values of (R_{ac} + R_{sp}) versus channel length are given in Fig. 3-37, both for the case in which K is maintained at the values that exist in the 0.7-μm technology (i.e., K is not scaled, but remains constant), and for the case in which future technological breakthroughs will permit the fabrication of a higher K (i.e., K is scaled). The advantage to scaling K – if this is in fact possible – is obvious from these results. It is also apparent that if the value of R_{co} is optimized, (R_{ac} + R_{sp}) can be the dominant component of R_S. In 0.5-0.7-μm devices the estimated values of (R_{ac} + R_{sp}) is >200 Ω-μm for NMOS devices and >300 Ω-μm for PMOS devices (assuming that K is not scaled).

The value of the *contact resistance*, R_{co}, can be accurately calculated using a 2-D device simulator, such as PISCES (see chap. 9). It can also be calculated by hand using the 1-D TLTR equation (Eq. 3-6c), with the value of ρ_{sh} obtained from measured data and the value of ρ_c extracted from test structure measurements (as described in section 3.3.4). Ng and Lynch's analysis assumes values for ρ_{sh} and ρ_c and calculates the range of values of R_{co} for the most probable assumed values. The minimum value of

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$R_{co(min)}$ is obtained if the contact length, l, is greater than 1.5 $[\sqrt{\rho_c/\rho_{sh}}]$. For a specific set of values of ρ_{sh}, ρ_c, and contact width (w), this value can be calculated from

$$R_{co(min)} \approx \frac{\sqrt{\rho_{sh}\,\rho_c}}{w} \qquad (3\text{-}15)$$

In such cases, the coth term in Eq. 3-6c will approach 1, and Eq. 3-6c will approach Eq. 3-15. In typical devices, this means that the contact length, l, will need to be one to four times the channel length in order to produce a metal-Si contact with the minimum value of R_{co} (for a given ρ_c and ρ_{sh}). This result indicates that the use of *self-aligned contacts* (as will be described in section 3.9) will be an important approach for minimizing R_{co}, since such contacts allow the contact length and width to be increased without there also being an increase in the size of the device that is fabricated using a conventional contact structure.

Figures 3-37a and 3-37b show the estimated values of $R_{co(min)}$ that will be attain-

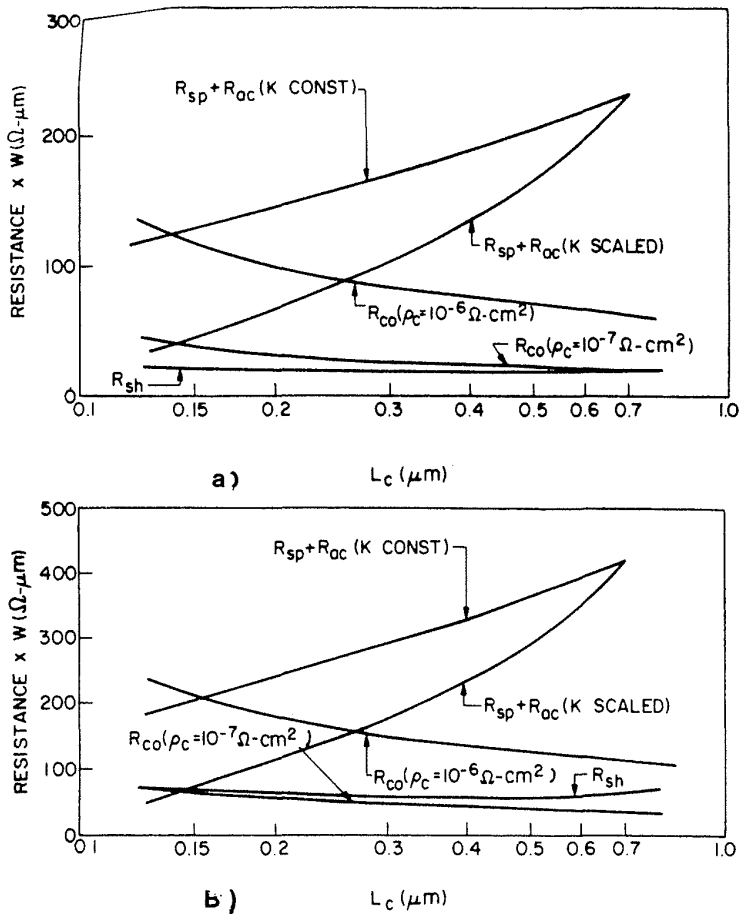

Fig. 3-37 The contributions of each resistance component as a function of channel length, L_c, for (a) n-channel and (b) p-channel MOSFETs.[85] (© 1987 IEEE).

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able for values of ρ_c between 10 and 100 Ω-μm^2 for NMOS and PMOS devices, respectively. This indicates that the values of $R_{co(min)}$ are smaller than ($R_{ac} + R_{sp}$) for devices with 0.5-0.7-μm channel lengths if such ρ_c values are used. Thus, by using sufficiently long contacts, R_{co} will not be the dominant component of R_S.

3.8.3 Impact of R_S on Device Characteristics

It was earlier proposed that R_S should be no larger than 10% of R_{ch}. Ng and Lynch, on the other hand, performed a more sophisticated analysis in which they estimated the reduction in switching speed as R_S was increased and L_{eff} decreased. They found that the circuit-speed degradation is technology dependent. That is, since the channel resistance in the linear region of operation of a MOSFET is smaller than the channel resistance in the saturation region of operation (see chap. 5), the impact of R_S will be different on enhancement-depletion (E/D) NMOS logic (i.e., more detrimental) than on CMOS logic. As we have moved into an era in which CMOS technology predominates, this helps solve the problem. The analysis of Ng and Lynch also indicates that as device size continues to shrink, performance will continue to improve, but that it will not be as good as it would be if the values of R_S obtained had been negligibly small.

3.8.4 Summary of the Impact of Intrinsic Series-Resistance Effects on MOSFET Performance

The following points summarize the results obtained by Ng and Lynch:

- Compared to the other components, R_{sh} contributes only a small value; for silicided source/drain regions, its effect should be negligible.

- R_{co} can be important in degrading MOS device performance in some cases, while in other cases it may not be significant. If the value of R_{co} is small relative to ($R_{sp} + R_{ac}$), it will not significantly impact device performance. R_{co} is essentially determined by the contact length l, and the value of ρ_c. The minimum value of R_{co} for a given ρ_c will be obtained for a contact length that is greater than the transfer length, l_t (Eq. 3-5). Therefore the main advantage of the self-aligned silicided source/drain regions will be an increase in the contact length that is sufficient to minimize R_{co}.

- An upper bound on a value of ρ_c that will still allow contacts with sufficiently small values of R_{co} is probably 100 Ω-μm^2, and this value appears to be attainable for the contact metallization systems in current use or under development. If ρ_c is smaller than 10 $\mu\Omega$-cm^2, the effect of R_{co} becomes insignificant. If ρ_c is between 10 and 100 Ω-μm^2, R_{co} is likely to be less important than ($R_{sp} + R_{ac}$). Nevertheless, the ρ_c value of a contact structure being used in production should be well characterized, especially as it can vary with implant dose, annealing conditions, contact premetal cleaning, etc.

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- The value of (R_{ac} + R_{sp}) is likely to dominate the value of R_S for MOS devices in which channel lengths are smaller than 0.5 μm. Minimum values of (R_{ac} + R_{sp}) are achieved by fabricating source/drain junctions with as steep a doping profile as possible.

Overall, Ng and Lynch predict that the intrinsic series-resistance effects will negatively impact the speed performance of MOS devices as these devices are scaled. Nevertheless, they foresee that it will be possible to build devices that will still demonstrate improvement of speed performance as they are scaled to 0.15 μm. The use of self-aligned, silicided source/drain regions to reduce R_{co} will be important, as will the development of processes that produce junctions with more steeply graded doping profiles. In addition, contact technologies that provide smaller ρ_c and lower values of ρ_{sh} of the diffusion layer under the contact window (or the silicided region) will need to be developed.

3.9 ALTERNATIVE (SELF-ALIGNED) CONTACT STRUCTURES FOR ULSI MOS DEVICES

As transistor dimensions approached 1 μm, the conventional contact structures used up to that point began to limit device performance in several ways. First, it was not possible to minimize the contact resistance if the contact hole was also of minimum size (as explained in section 3.8.2), and problems with cleaning the small contact holes became a concern. In addition, the area of the source/drain regions could not be minimized because the contact hole had be aligned to these regions with a separate masking step, and extra area had to be allocated for misalignment. (The larger area also resulted in increased source/drain-to-substrate junction capacitance, which slowed down device speed). Finally, when nonminimum-width MOSFETs were fabricated with conventional contacts, several small, uniform-sized contact holes were usually used rather than one wider contact hole. (The reason for this is that if all the contact holes are of identical size, they are more likely to clear simultaneously during the etching process.) The problem with using several small, equally sized contact holes rather than one wider one, was that the full width of the source/drain region was thus not available for the contact structure (see Fig. 3-38). As a result the device contact resistance was proportionally larger than it would have been in a device having minimum width.

A variety of alternative contact structures have been investigated in an effort to alleviate these problems. The most important that have emerged are the following:

- self-aligned silicides on the source/drain regions (when these silicides are formed at the same time as the polycide structure, the approach referred to as a *salicide process*);
- elevated source/drain or emitter regions (formed by Si deposition onto the exposed source/drain and emitter regions); and

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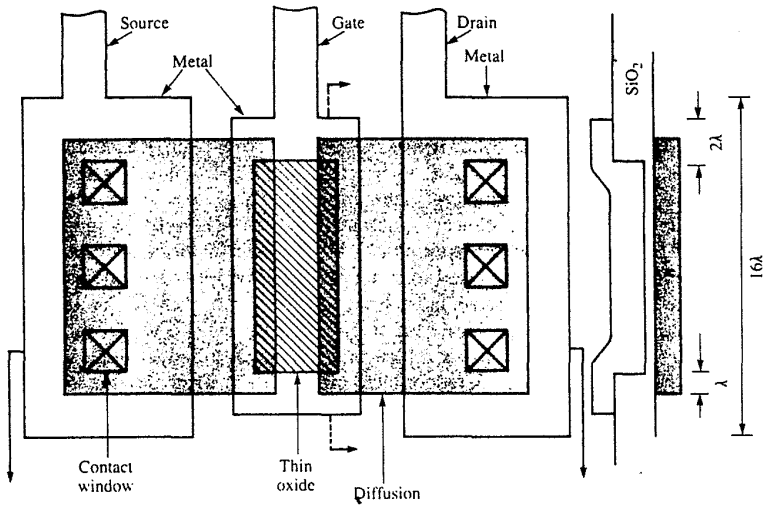

Fig. 3-38 In transistors that are wider than minimum width, conventional contacts may still be made using several contact holes of minimum size, rather than one wider contact hole.

- buried-oxide MOS (*BOMOS*) contacts
- selectively deposited layers of metal in the contact holes (either by CVD, as described in sections 3.5.2.5 and 4.5.4.3, or by electroless deposition, as discussed in section 4.5.6.3).

In this section we will describe the salicide and BOMOS contact approaches. In the last two sections of the chapter we will consider elevated source/drain contacts and the advantages these offer with regard to making contacts to shallow junctions. Mention will also be made of the important topics of *unframed contacts* and *vias*. The filling of contact holes and vias will be addressed in chapter 4, as part of the multilevel-interconnect discussion.

3.9.1 Self-Aligned Silicide Contacts

One alternative to using the conventional contact structure is to contact the entire source and drain regions of a MOSFET with a conductor film (Fig. 3-39). This approach becomes even more attractive if such a film can be formed using a self-aligned process that does not entail any additional masking steps, in a process sequence as follows:

1. After the source and drain regions have been implanted to form the source/drain junctions (Fig. 3-39a), the poly-Si sidewall spacers are formed (Fig. 3-39b).
2. The metal metal used to form the silicide is deposited.
3. The wafer is heated, which causes the silicide reaction to occur wherever the metal is in contact with the silicon. Everywhere else, the metal remains unreacted (Fig. 3-39c).

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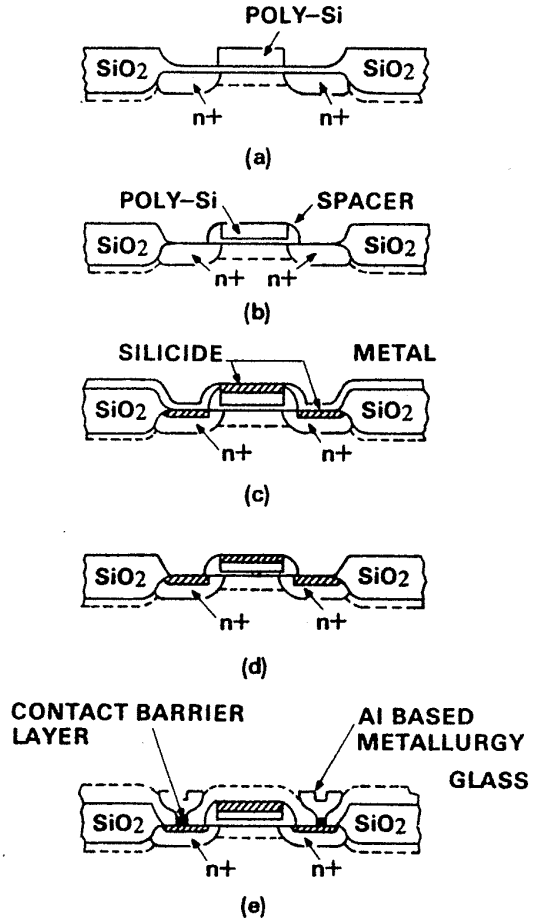

Fig. 3-39 Salicide processing steps and final structure.[163] (© 1984 IEEE).

4. The unreacted metal is selectively removed through the use of an etchant that does not attack the silicide, the silicon substrate, or the SiO_2 (Fig. 3-39d). As a result, each exposed source and drain region is now completely covered by a silicide film, but there is no film elsewhere.

5. A dielectric layer is deposited onto the silicide, and contact holes are opened in it down to the silicide layer.

6. Metal is deposited into the contact holes to make contact with the silicide (Fig. 3-39e).

The above contact-formation method offers several advantages over the conventional contact structure:

- The value of R_{sh} of Eq. 3-1 becomes negligibly small because the ρ_{sh} value of the silicide is typically 1-2 Ω/sq, whereas that of the diffused junction region alone is 40-120 Ω/sq.

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- The contact area of the silicide and the Si is much larger than that of the metal-Si area in a conventional contact in a device of the same total area. Thus, the value of R_{co} for the same ρ_c value is significantly lower.

- The contact hole is now used to make contact between the metal and the silicide, but the value of ρ_c exhibited by silicide-metal interfaces is typically $\leq 10^{-9}$ Ω-cm^2. This is two orders of magnitude lower than nominal metal-to-silicon specific contact resistivities, $\sim 10^{-7}$ Ω-cm^2, obtained at or near solid-solubility silicon doping limits. Hence, the contribution to R_{co} due to the metal-silicide contact resistance at the contact hole is usually negligibly small.

- In some processes the deposition of the metal and the formation of the silicide can occur simultaneously with the silicide formation process of the gate; hence, this step can be integrated into the process essentially for "free."

As it became apparent that a self-aligned contact structure would be beneficial for reducing the values of the parasitic series resistances of the conventional contact structure, some other processing trends also allowed a new group of materials to be considered as contact metals to Si. These materials were the group-VIII silicides (PtSi, Pd_2Si, $CoSi_2$, and $NiSi_2$) as well as $TiSi_2$. As it became necessary to fabricate shallow junctions, processing technology had to be performed at lower temperatures to avoid the formation of deep junctions. When it became possible to restrict the maximum temperature after the silicide formation to less than 900°C, this also opened the door to these silicides, since all of them are unstable at temperatures higher than 900°C.

There are several important reasons why $TiSi_2$ and the group-VIII metal silicides are especially attractive as candidates for self-aligned ohmic contacts and local interconnects to silicon. These are as follows:

- Such silicides exhibit lower resistivities than the refractory-metal silicides of W, Ta, and Mo (e.g., the respective resistivities of $TiSi_2$, $CoSi_2$, PtSi, Pd_2Si, and $NiSi_2$ are 13-20, 16-18, 28-30, 30-35, and 50 $\mu\Omega$-cm).

- All of the group VIII metals react with Si at 600°C or less, and, with the exception of Ti, there is no reaction of the metal with the masking oxide during the silicide formation. Even with Ti, the reaction is minimal, and the reaction products appear to be soluble in the Ti etch.[89]

- When the silicides are formed at such low temperatures, the metal atoms diffuse into the Si, and react with it. As the metal atoms diffuse into the SiO_2, no Si is available for reaction, and hence, the metal over device areas covered with SiO_2 remains unreacted. This also prevents lateral formation of the silicide over the narrow oxide-spacer region during the silicide formation step.*

*There is an exception to this statement. During $TiSi_2$ formation at temperatures above 600°C, Si diffuses into the Ti. The diffused Si then reacts to form $TiSi_2$ over the oxide-spacer regions, resulting in shorting of the gate and source/drain. Procedures for avoiding this effect are discussed in section 3.9.1.1.

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- Dopant atoms in the silicon are "snowplowed" into the silicon substrate as group-VIII-metal silicides are formed[138] (but not necessarily as $TiSi_2$ is formed).[98] Such snowplowing maintains a high doping concentration at the silicide-Si interface, which is beneficial for producing low resistance contacts.
- In all cases, after the silicide has been formed, the unreacted metal can be etched off from the oxide surface using chemical etchants that do not attack the oxide, the silicide, or the substrate silicon. This last characteristic allows self-aligned contacts to be formed through the use of these silicides.

Of this group of silicides, the two that have been the focus of most development for the salicide process are $TiSi_2$ and $CoSi_2$. These two silicides exhibit the lowest resistivities of the group and can withstand process temperatures in excess of 800°C (such temperatures are frequently used to reflow the doped glasses deposited over the salicided source/drain regions). Pd_2Si and PtSi, on the other hand, agglomerate when in contact with Si at high process temperatures (Pd_2Si at 700°C, and PtSi at ~800°C). The use of PtSi was not limited in conventional contacts because the self-aligned PtSi contacts were formed after the reflow step, but in the salicide process, reflow is done after silicide formation, making PtSi incompatible with reflow. $NiSi_2$ exhibits significantly higher resistivity, and the stresses formed in $NiSi_2$ films at low temperatures (400-600°C) seem high enough to cause mechanical instability.[90]

The salicide process exhibits a limitation related to the fact that the gate and the source/drain silicides are formed at the same time. On the gate, it is desirable for the silicide to have the lowest possible sheet resistance (so that the gate electrode will also possess a low interconnect resistance). To achieve this, a thick silicide layer is needed. Over the source/drain regions, however, the silicide can be only of limited thickness, in order to prevent excess consumption of the substrate silicon by silicide formation. Thus, a thicker silicide, though favorable at the gate level, is detrimental to contact formation, and vice versa. One solution is to use a two-step process[91] in which the silicide is formed on the gate level first, and on the contact regions at a later stage (and at a different thickness).

Another problem is that it is difficult to metallize shallow junctions (≤200 nm), because of the junction leakage that is observed when the silicidation process is used. The implant damage (caused during the source/drain junction formation) may not be sufficiently annealed-out by the lower-temperature silicide-formation step. This damaged region may remain within the depletion region of the shallow junction, giving rise to higher leakage. In addition, the RIE process used to open the contact holes in the doped oxide (deposited after silicide formation), may damage the silicide.[96] Techniques to reduce or eliminate this last set of problems are covered in section 3.10. A final problem of salicide technology is that it degrades the effectiveness of some electrostatic-discharge protection devices used with CMOS circuits (see chap. 6, section 6.7.1.4).

3.9.1.1 Self-Aligned Titanium Silicide Contacts. $TiSi_2$ is attractive for the salicide application because it exhibits low resistivity, and because it can reduce

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native-oxide layers (making it the only known refractory metal that can reliably form a silicide on both polycrystalline and single-crystal silicon through a thermal reaction). Furthermore, devices fabricated with titanium silicide on the gate electrode are more resistant to high-field-induced hot-electron degradation than are conventional poly-Si gate devices.[95] It is conjectured that the $TiSi_2$ is an effective getter for the hydrogen atoms introduced during the hydrogen anneal. Less hydrogen is thus incorporated into the gate oxide, and this improves the hot-electron reliability (see chap. 5, section 5.6.6).

Some aspects of the $TiSi_2$ process are not as favorable, including: (a) the reactivity of Ti with SiO_2 can cause unwanted reactions with the oxide spacers during the silicide-formation process; (b) $TiSi_2$ is less stable than WSi_2 or $MoSi_2$; and (c) because Ti films have a high propensity to oxidize, the silicide must be formed in ambients that are free of oxygen.

Oxide spacers at the edges of the polysilicon are formed to separate the silicided gate and source/drain regions, but these spacers are typically only 200-300 nm wide. Thus, any lateral formation of silicide can easily bridge the separation and cause the gate to be come shorted to the source/drain (this effect is referred to as *bridging*).

It has been observed that if the $TiSi_2$ is formed by conventional furnace annealing in an inert-gas atmosphere (e.g., Ar for ~30 min), lateral $TiSi_2$ formation occurs rapidly. This occurs because silicon diffuses into the Ti regions that cover the spacer oxide and subsequently reacts with the Ti. When annealing is performed in an N_2 ambient, the Ti absorbs a significant amount of nitrogen (e.g., more than 20 at%). The N_2 is absorbed preferentially at the Ti grain boundaries, which "stuffs" the grain-boundary diffusion paths. This reduces the diffusivity of Si in the Ti, and essentially suppresses the lateral silicide reaction. Annealing in pure N_2 or pure forming gas (95% N_2 + 5% H_2) thus results in $TiSi_2$ formation without bridging. It is also important that the N_2 ambient contains fewer than 5 ppma of oxygen or water to avoid unwanted oxidation of the Ti film.[130] The absorbed N_2 also reacts with the Ti to form TiN at the Ti surface.[89,130]

If the temperatures exceed 700°C during $TiSi_2$ formation, the Ti and the spacer SiO_2 can also react to form titanium oxides. Any residues of this reaction can degrade device performance by compromising the oxide integrity or producing bridging. To avoid such effects, it is recommended that the $TiSi_2$-formation temperature be held to <700°C, and that a minimum field-oxide thickness of 100 nm be utilized. In practice, a two-step formation process is typically used.[136] During the first step, the temperature is kept at ~650°C. Following selective etching and removal of the unreacted Ti in a room-temperature mixture of DI H_2O, 30% H_2O_2, and NH_4OH (5:1:1), a second temperature step of ~800°C in Ar is used to lower the $TiSi_2$ sheet resistance and to stabilize the $TiSi_2$ phase.[92]

Rapid thermal processing (RTP) at 600-800°C in Ar (with the specific reaction time depending on the temperature selected), has also been used to effect the silicide formation. Following selective removal of the unreacted Ti, a stabilization anneal of 1000°C for 30 seconds in Ar is conducted to reduce the $TiSi_2$ resistivity.

$TiSi_2$ in contact with Si was originally thought to be capable of being subjected to temperatures up to ~900°C ($TiSi_2$ agglomerates at higher temperatures). It has been observed, however, that if the temperature exceeds 800°C, the value of ρ_c to p^+ Si

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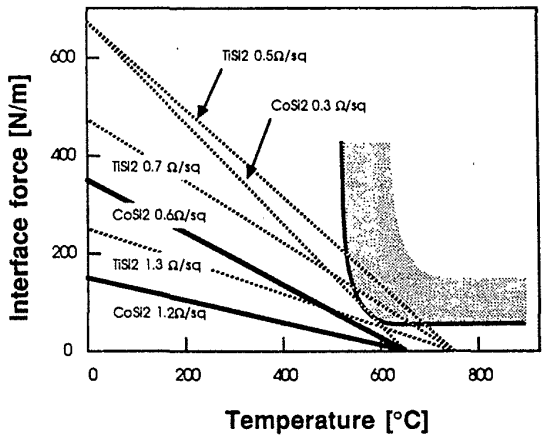

Fig. 3-40 Force at the silicide edge (silicide stress x silicide thickness) versus temperature acting during cooling after silicide formation for the various samples. (Dotted lines correspond with samples in which defects are observed.)[100] This paper was originally presented at the Spring 1988 Meeting of The Electrochemical Society, Inc., in Atlanta, GA.

becomes too large.[93] (However, the ρ_c of $TiSi_2$ to n^+Si can be less than 10^{-6} Ω-cm^2 for anneal temperatures of 800°C.) Even at anneal temperatures of 800°C, the value of ρ_c to p^+ Si is 10^{-5} Ω-cm^2, while at temperatures of 900°C, it increases to 10^{-3} Ω-cm^2. The cause of this problem is the rapid diffusion of the boron from the PMOS source/drain regions into the overlying silicide, causing dopant depletion at the silicide/junction interface (and consequently, high contact resistance between the junction and the silicide layer). Temperatures in excess of 800°C must thus be avoided following $TiSi_2$ formation in CMOS technologies. This may represent a problem if doped-glass reflow is used in a CMOS process.[94]

It has been reported that As from the Si substrate will also diffuse into the silicide during the silicide formation, leading to increased contact resistance. To minimize such As dopant redistribution, an RTP process was successfully used to form the silicide (700°C in N_2 for 20 seconds, followed by 10 seconds at 850°C after the unreacted Ti is removed, for a 60-nm-thick Ti film).[97] An extensive study of the effects of $TiSi_2$ formation on dopant redistribution is presented in reference 98.

Another reported method for enhancing the $TiSi_2$ formation process uses *ion-beam mixing*. In this method, Si atoms are implanted into the Ti film before it is annealed. The surface morphology of the silicide film is improved, and its sheet resistance is lowered by ~20%.[149]

Al-TiN-$TiSi_2$-Si contact structures were observed to undergo early electromigration failure if the current passing through the contact caused local heating such that the temperature exceeded 465°C. It was also found that thermal stresses due to even lower temperatures produced damage to the contacts, which also led to contact-electromigration failure.[99]

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Another problem associated with $TiSi_2$ contacts involves the generation of defects at the edge of the $TiSi_2$ film due to stresses in the film (Fig. 3-40).[100] Such defects are reported to begin occurring once the thickness of the $TiSi_2$ film exceeds 100 nm. Another report suggests that a Ti film no thicker than 70 nm should be used when $TiSi_2$ contacts to shallow junctions (0.2 μm) are being implemented.[142] Thicker Ti films would cause excessive silicon consumption and rough interfaces, and these in turn would produce increased junction-leakage current and high contact resistance.

The formation of CVD W plugs in contact with $TiSi_2$ salicide layers has also been investigated. Early reports indicated that an interfacial TiF_3 layer is formed between the W and the $TiSi_2$ if the W deposition is done in a hotwall process at 300-350°C, and that this layer inhibits good contact between the plug and the underlying silicide. Higher-temperature W depositions (600-700°C) were found to reduce the contact resistance;[101] nevertheless, random contacts exhibited a "crusting" or overgrowth problem when this process was used. An alternative method for overcoming the high contact resistance between $TiSi_2$ and CVD W is to deposit a thin bilayer of Ti and W before doing the CVD W deposition (with the Ti and W layers each being 10-30 nm thick). The underlying Ti forms a low resistance contact to the $TiSi_2$ (since any native SiO_2 on the silicide is consumed by reaction with the Ti), and the sputtered-W layer prevents the formation of the high-resistivity TiF_3 layer on the $TiSi_2$ during the CVD W process.[158]

3.9.1.2 Self-Aligned Cobalt Silicide Contacts. Although $TiSi_2$ has been the most widely implemented material for the salicide process, $CoSi_2$ has also received significant attention as an alternative candidate material. $CoSi_2$ exhibits the following attractive characteristics for this application:

- It offers the benefits of low resistivity (16-18 $\mu\Omega$-cm) and high temperature stability. For example, $CoSi_2$ films of 300-nm thickness exhibit a ρ_{sh} of 0.5 Ω/sq and remain stable when in contact with Si up to 900°C.[102,103] This demonstrates the compatibility of $CoSi_2$ with a 900°C glass-reflow step.

- It can be formed by the reaction of Co with Si in a single annealing step, with no lateral formation of the silicide or encroachment under the oxide (i.e., bridging is not a problem).

- The interface of the silicide and silicon is smooth, and low-resistance contacts to the silicon can be formed (as low as 15 Ω-μm^2 to both n^+ and p^+Si).

- Contacts to shallow As and B junctions can be successfully fabricated, and the dopant profiles in such junctions appear to be essentially unchanged after the silicide has been formed.

- A selective chemical etch exists that makes it possible to remove the Co without affecting the $CoSi_2$ (e.g., $HCl:H_2O_2$ [30%] in a volume ratio of 3:1 at room temperature).

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- $CoSi_2$ is far less susceptible to removal by plasma etching than $TiSi_2$. Hence there is negligible silicide loss during the overetch time that may be needed when dry-etching the contact openings through the glass overlayer.
- No competing reaction to the $CoSi_2$ formation reaction occurs, whereas when $TiSi_2$ is formed in nitrogen, TiN is simultaneously formed. In addition, lower shear forces (important to device integrity) are present in $CoSi_2$ than in $TiSi_2$ of the same thickness.[104]

The process sequence for forming the $CoSi_2$ polycide and the self-aligned contacts to Si is as follows:

1. The silicon and polysilicon surfaces are chemically cleaned by dipping the wafers in a dilute (100:1) solution of H_2O:HF for 2 minutes just prior to loading them into the sputtering chamber. Although in one report this step is followed with an rf backsputtering procedure to remove ~10 nm of the silicon surface,[103] in another the rf-backsputter step was observed to produce a rough interface following silicidation.[102] Nevertheless, the cleaning procedure is important, because cobalt is not able to reduce SiO_2 and because the presence of a native oxide can inhibit the silicidation reaction.

2. The cobalt is sputter deposited to the desired thickness. The thickness is selected based on how much of the silicon in the source/drain regions can be consumed, as well as what silicide sheet resistance value is needed. For example, 35.9 nm of Si is consumed by 10 nm of Co to form 35.9 nm of $CoSi_2$. To form a $CoSi_2$ layer with ρ_{sh} = 1.5 Ω/sq, a 30 nm thick layer of Co must be deposited. It should be noted that the Si consumption during $CoSi_2$ formation is about 25% greater than that during $TiSi_2$ formation. This constitutes one of the disadvantages of $CoSi_2$ compared to $TiSi_2$.

3. The $CoSi_2$ is formed by reacting the Co with the Si and polysilicon. The reaction kinetics are described in reference 103. Although the reaction can be accomplished through either a furnace anneal or RTP, the latter has emerged as the more attractive approach.[129] An 80-nm-thick Co film will be completely converted to $CoSi_2$ at 700°C for 30 seconds. The gas ambient must be kept free of oxygen to ensure that oxide-free silicide films are formed.

4. The unreacted Co is etched away using the etchant mentioned earlier.

5. Finally, the wafer is covered with a CVD glass layer. Note that when Al is contacted to the $CoSi_2$, the maximum anneal temperature must thereafter be limited to 400°C (since Al will react with $CoSi_2$ at temperatures in excess of 400°C). To allow a higher anneal temperature to be used, a diffusion barrier layer (such as Ti:W), must be used between the $CoSi_2$ and the Al layers.[105]

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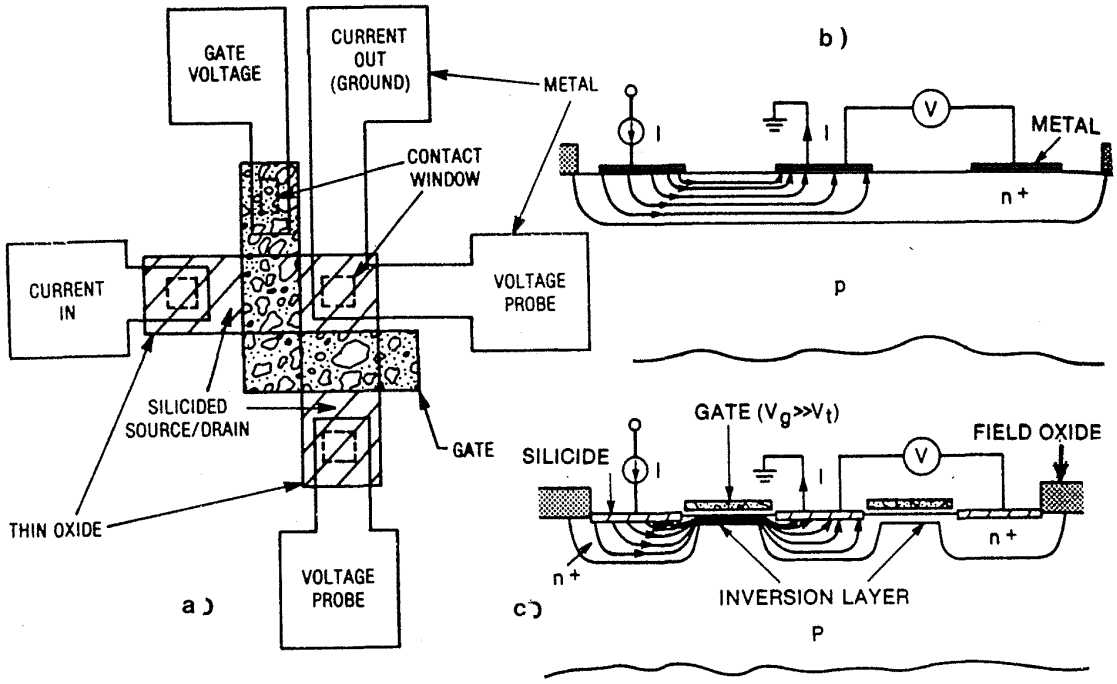

Fig. 3-41 Layout of the silicided test structure described in ref. 106. (b) Cross sections showing the current pattern in (a) the conventional Kelvin test structure, and the new silicided test structure.[106] (© 1988 IEEE).

A report describing the operation of 0.5-μm MOS devices built with $CoSi_2$ source/drains and $CoSi_2$/poly gates is presented in reference 148. Two studies comparing the properties of $TiSi_2$ and $CoSi_2$ for MOS salicide applications are given in references 150 and 151. Both reports identify $CoSi_2$ as a better candidate than $TiSi_2$ for use in the salicide process for the reasons listed above.

3.9.1.3 Measuring ρ_c of Self-Aligned Silicide Contacts. The standard CBKR test structure used to extract ρ_c of a conventional contact is not suitable for obtaining ρ_c for a self-aligned silicide contact. In the CBKR structure, three contacts are required over the same diffusion region (Fig. 3-41a). Therefore, it is possible to measure only the metal-to-silicide contact resistance, but not the silicide-to-Si contact resistance. To use the CBKR structure to measure the latter contact resistance value, the silicide formation must be restricted to the contact hole; however, this condition does not exist in the actual self-aligned contact. A test structure has therefore been suggested to overcome this difficulty.[106] A cross-section of this structure is shown in Fig. 3-41b. In addition to providing the ρ_c value, this structure can provide the value of ρ_{sh} beneath the silicide. Such structures can be directly integrated into production wafers with no modification of the process sequence. Additional details of how this structure is fabricated can be found in reference 106.

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3.9.2 Buried-Oxide MOS Contact Structure (BOMOS)

In the buried-oxide MOS (or BOMOS) method, the contact structure is formed after the field oxide, but before the gate oxide. Figure 3-42 shows the key steps of the BOMOS process sequence. The process is begun by growing and patterning the *first oxide film* (FOX 1), which underlies the polysilicon interconnect runners and the contact areas (Fig. 3-42b). This is followed by the simultaneous deposition of epitaxial single-crystal silicon in the exposed silicon areas and of polysilicon over the oxide.

The active areas on both the polysilicon and the epi regions are then defined by growing a second field-oxide layer. As this oxide is grown, it selectively consumes the polysilicon layer. To insure good isolation, it is necessary to completely oxidize this poly layer on top of FOX 1. The process is then completed with gate oxidation, gate patterning, and source/drain formation.

The BOMOS structure allows larger contact areas to polysilicon, since the contact hole is opened on top of the oxide (Fig. 3-43). In addition, p^+ and n^+ poly can abut on top of the oxide, and a shared contact can be made to this joined area. Finally, the source/drain areas can be made smaller than in MOSFETs with conventional contacts, which results in devices with smaller source/drain-to-substrate junction capacitances. Although the BOMOS structure is formed by means of a self-aligned contact process, it still suffers from the narrow-width effects associated with the use of LOCOS. In addition, there are alignment and topography limitations in the source/drain areas.

The original BOMOS process was proposed in 1977.[107] Since then, several improvements to it have been suggested, including the LID-MOS[108] and the COO-MOS[109] processes. The process sequence shown in Fig. 3-42 incorporates the improvements described in these two reports. An additional enhancement would involve siliciding the poly extensions to reduce the high sheet resistance of the poly.

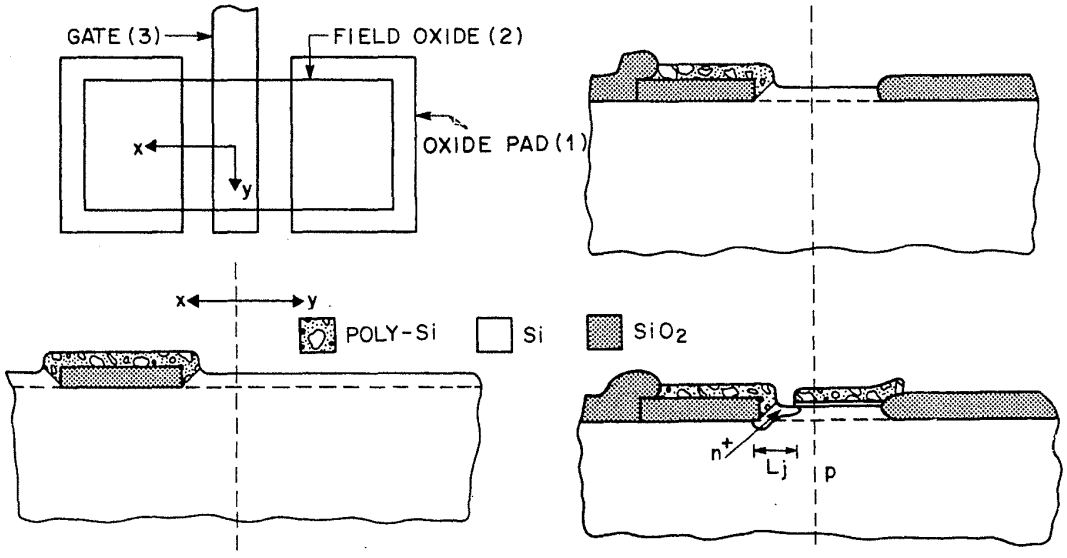

Fig. 3-42 The key process steps of the BOMOS self-aligned contact approach.[164] (© 1987 IEEE).

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3.10 FORMATION OF SHALLOW JUNCTIONS AND THEIR IMPACT ON CONTACT FABRICATION

As VLSI device structures shrink laterally in dimension, it becomes necessary to scale the vertical dimensions of the devices as well. One important vertical dimension is the depth of *pn* junctions. For example, in MOS devices with channel lengths of less than 0.8 μm, source/drain junction depths smaller than 250 nm are required to maintain adequate device performance.[110] In this section we will describe the technological approaches to forming shallow junctions.

3.10.1 Conventional Shallow-Junction Formation

The conventional approaches to forming shallow junctions involve ion implantation and annealing. Shallow n^+ layers for NMOS source/drain regions are relatively easy to form in this way. Arsenic is typically used to form such layers, since the projected range of As at implant energies of 75 keV is only 50 nm. In addition, the heavy As atoms tend to create amorphous layers at the Si surface during the implant step. Such amorphous layers prevent As from undergoing significant channeling during implant (see Vol. 1, chap. 9). The amorphous layers can also be annealed through solid-phase epitaxy regrowth at relatively low temperatures. Finally, since As diffuses relatively slowly, such layers remain relatively shallow during the high-temperature anneal steps that must be performed following the source/drain implantation. Sheet resistances as low as 26 Ω/sq in As implanted layers 200 nm thick have been reported.

The formation of shallow p^+ junctions, however, is more difficult. Boron is a light atom (B^{11}), and when B implants are carried out at room temperature, an amorphous surface layer is not formed. As a result, boron implants exhibit channeling tails that penetrate relatively deeply into the Si, producing deep, as-implanted junctions. While attempts to use very low implant energies (e.g., 1-2 keV) might be effective,[111] such efforts would require the availability of low-energy ion implanters and perhaps even new ion sources. In addition, sputtering of the surface by the ion beam would have to be considered. Finally, the crystalline-defect damage caused by boron implantation must be annealed at temperatures >900°C, leading to significant diffusion of the implanted atoms, and thus driving the junctions even deeper.

Several approaches have been developed to minimize the problems associated with implanting shallow boron-doped junctions. First, the implanted dopant profile can be moved closer to the Si surface by implanting through a thin (e.g., 20-nm-thick) screen oxide. While this shifts the peak of the B film closer to the surface by roughly the oxide thickness, this approach introduces the problem of recoiled oxygen atoms and also worsens the straggle of the implanted doping distribution. Furthermore, if the oxide film thickness is close to the projected range of the ions, it is difficult to accurately control the dose penetrating through to the Si.

Second, BF_2^+ is implanted instead of B, in which case the B^+ ion acquires 22% of the BF_2^+ energy. This reduces the depth to which the B atoms are implanted (e.g., the projected range of B atoms from a 50 keV BF_2^+ implantation is ~30 nm). While the

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fluorine ions damage the surface and thus reduce B channeling, significant B channeling may still occur. (Fluorine, however, does cause unwanted defects when BF_2^+ is implanted, which is a drawback to this technique.)[131] Consequently, a prior implantation step may be performed using Si^+, Sn^+, or Ge^+ to preamorphize the Si surface[112] as a way to minimize B channeling.* Although tilting of the wafers by 7 or 8° with respect to the ion beam has also been used to reduce channeling, this procedure can cause asymmetric implant effects in the source/drain regions. Such effects can significantly impact MOS device behavior, especially for PMOS devices in which lightly doped drains are used (see chap. 5, section 5.6.5.2). Hence, this procedure may no longer be feasible for deep-submicron (< 0.7 μm) PMOS device processes.

The redistribution of B atoms following implantation may still cause undesirably deep junctions, even when a BF_2^+ implant is performed. The use of *rapid thermal processing* to replace furnace annealing addresses this problem. In addition, the solubility of the dopant, and hence the conductivity of the junction region, depends rather strongly on the temperature of the anneal for high dose implants. The data presented by Ryssel[132] indicate an increase by a factor of two in B solubility at equilibrium for every increase of 100°C above 900°C. Finally, it has been observed that when B implants are annealed at temperatures close to 800°C, they give rise to very large diffusive motions.[133] Thus, simply lowering the temperature in a furnace anneal in an attempt to reduce profile motion could instead lead to a much deeper junction, depending on specific experimental conditions.

It was also observed in Ryssel's report that a pre-anneal at a higher temperature using RTP diminishes this transient annealing effect. Junction depths following an RTP anneal have been shown to be 25-35% as deep as those performed with a furnace anneal. Boron-doped junctions with depths of 0.2 μm and surface concentrations of $N_A = 10^{20}/cm^3$ have been reported (Fig. 3-43).[113] The modeling of diffusion in shallow junctions under RTP has been discussed by Fair.[114,155]

3.10.2 Alternative Approaches to Forming Shallow Junctions

Conventional techniques for forming B-doped shallow junctions require complex multistep processes with high-temperature annealing steps to remove the implant damage and activate the dopant. A variety of alternative techniques for forming shallow junctions in Si are being pursued in an attempt to overcome these limitations, includ-

* Note that pre-amorphizing of the surface with a vertical ion beam will not prevent lateral channeling of the boron, since the Si under the mask edge will not be amorphized. Hence, even though the pre-amorphization technique is effective in reducing the vertical junction depth, it does not help reduce the lateral junction depth. Such lateral channeling presents a serious problem in MOS devices with submicron gate lengths, since it causes a significant reduction in channel length. A reported technique for tackling this problem is a preamorphization implant carried out at a 30° tilt angle. This causes amorphization under the mask and thus significantly suppresses lateral channeling.[147]

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ing: implantation into silicide contact layers and diffusion of the dopant into the substrate; selective growth of Si over source/drain regions, followed by implantation into the epi Si and diffusion of the implanted dopants to form the junctions; deposition of doped layers by CVD, followed by diffusion to form the junctions; and gas immersion laser doping (GILD).

Implantation into already formed silicide layers has been described for a number of different silicides that are used to make contact to Si. These include WSi_2,[115] $CoSi_2$,[96] and $TiSi_2$.[116,149] In this method, virtually all of the implanted ions stop within the silicide layer and do not penetrate into the Si. The shallow junctions are formed by outdiffusion of the implanted dopant into the underlying Si. This approach has the following advantages:

- Since all the implanted ions stop in the silicide, no implant damage is created in the Si. As a result, leakage currents in the junction (caused by damage within the depletion region of the junction) are eliminated (Fig. 3-44).
- The processing temperature following implantation is no longer determined by the need to anneal out the implant damage (for B-doped junctions, this temperature would ordinarily be ≥900°C). Instead, very shallow (40-70-nm), uniform junctions can be fabricated by outdiffusing the junctions from the silicide at lower temperatures (e.g., 800°C).
- Diffusion results in steep dopant profiles without damage to the silicon lattice.
- Uniform dopant profiles can be achieved through outdiffusion of the dopants

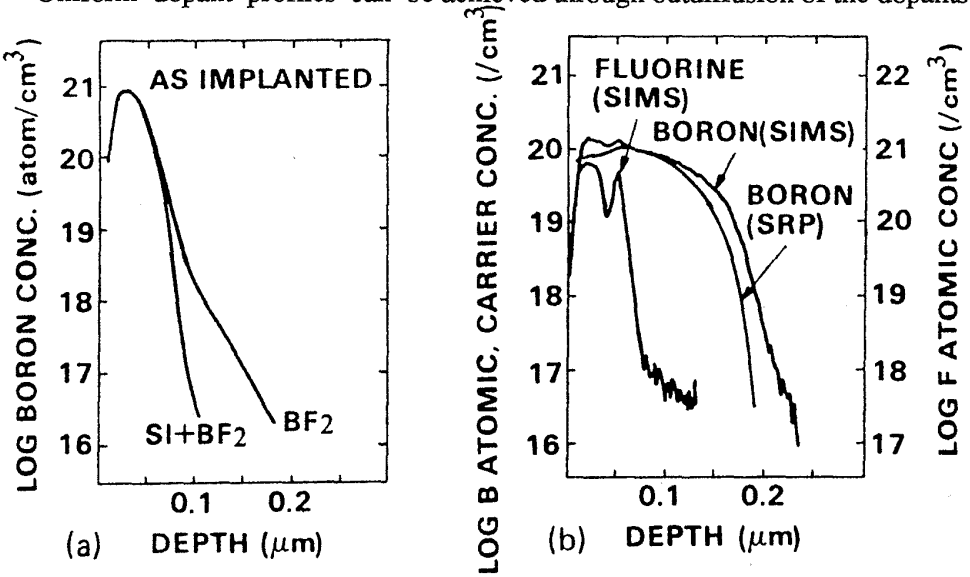

Fig. 3-43 (a) Measurements of the boron profiles after implanting BF_2 at 30 keV with a dose of $3x10^{15}$ cm^{-2} into monocrystalline and preamorphised silicon. Silicon implant parameters: 50 keV, $1x10^{15}$ cm^{-2}. (b) SIMS and spreading resistance (SRP) profiles for a BF_2 implant at 30 keV with a dose of $3x10^{15}$ cm^{-2} after rapid thermal annealing at 1150 °C for 5 sec.[113] Reprinted by permission of the publisher, The Electrochemical Society, Inc.

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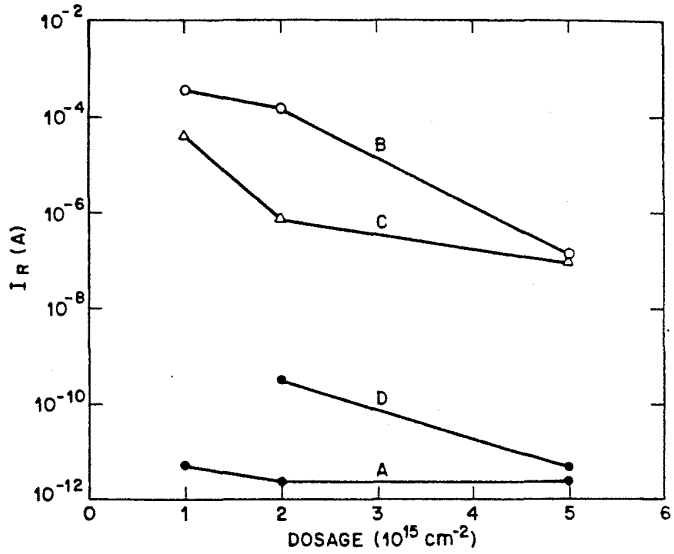

Fig. 3-44 Silicide junction leakage: (a) good n^+/p diode with no silicide, junction depth of 0.15 μm; (b) after forming 0.07 μm of $CoSi_2$, Si consumed 0.07 μm; (c) after $CoSi_2$ formation at 700 °C, Si consumed 0.11 μm; (d) after a second 900°C/30 min drive.[96] (© 1986 IEEE).

from the silicide, since anisotropy and shadowing effects are eliminated. That is, the dopant diffuses rapidly in the silicide, and this wipes out any nonuniform dopant concentrations produced in the silicide as a result of shadowing during implantation. For more details on these shadowing effects in short-channel MOSFETs see chap. 5, section 5.6.5.2.

- Silicide formation occurs before junction formation, and as a result the same silicide thickness is produced on both p and n channel devices (i.e., Si consumption during silicide formation is reportedly dependent on the Si doping type and concentration).[149]

Although a high surface concentration of dopants can be achieved, a sufficiently high implant dose must be used, as the silicide may retain a considerable amount of the dopant within its grains and grain boundaries to satisfy the solubility of the dopant in the silicide. In addition, it must be verified that the dopant drive-in step does not degrade the stability of the silicide. It has also been reported that the dopant can be implanted into the metal prior to silicide formation, and that the diffusion that forms the shallow junction occurs simultaneously with the silicide formation in a single subsequent anneal step.[117]

Selective growth of Si and diffusion of the implanted dopants to form the junctions has also been investigated by several groups.[118,119] In this approach (Fig. 3-45 and Fig. 6-43, chap. 6), silicon is selectively grown (SSG) over the source/drain regions of MOS devices to a depth of 200-400 nm, following the completion of oxide-spacer

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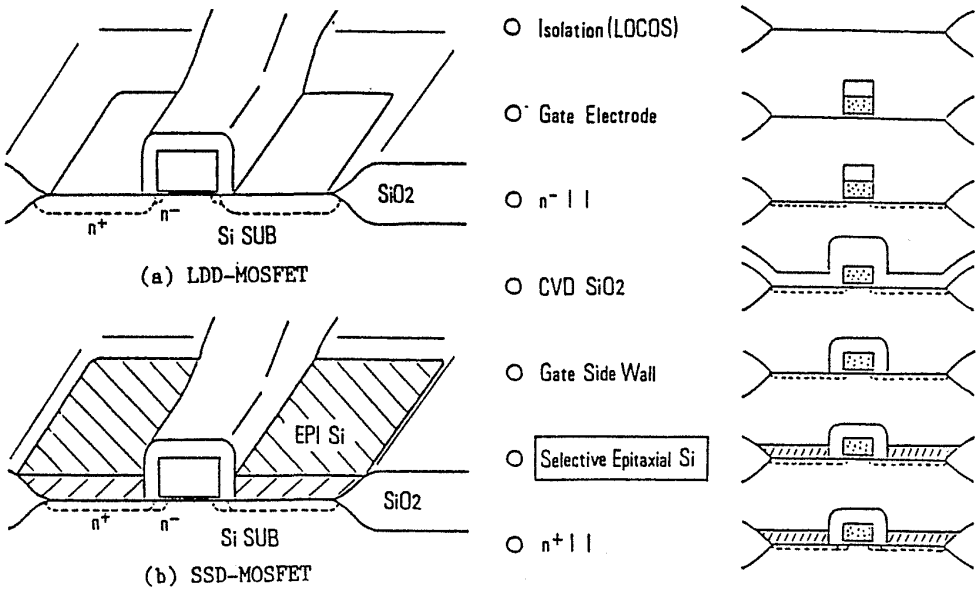

Fig. 3-45 Schematic diagram of (a) an LDD-MOSFET. (b) a stacked-source-drain (SSD) MOSFET using selective epitaxy. (c) Fabrication process flow of an SSD-MOSFET.[118] This paper was originally presented at the Spring 1988 Meeting of The Electrochemical Society, Inc. held in Atlanta, GA.

formation. A reduced-pressure, 900°C process using SiH_2Cl_2-HCl gas is employed for the SSG step. This produces raised source/drain regions. In one report, a BF_2^+ implant into the SSG film is followed by a 1050-1075°C RTP step to form a low resistance (60 Ω/sq) shallow junction (100 nm deep).[119] The RTP step is performed after a BPSG film has been deposited and contact holes in it have been opened. Thus, the RTP step also serves to reflow the contact holes. PMOS devices with gate lengths of 0.5 μm fabricated with this approach exhibited good device characteristics.

In the other report, a phosphorus implant into the SSG layer is performed so that a gradual-drain n^+ junction can be formed to reduce hot-carrier degradation. Non-selectively deposited polysilicon has also been used as a dopant source for shallow-junction formation: such processes are described in sections 3.11.2.4 and 3.11.2.5. Deposition of a *dopant source by CVD* and diffusion of dopant from it to form the junction has also been investigated.[120]

Gas-immersion laser doping (GILD) is another candidate process being evaluated for shallow-junction formation. In this process, the desired dopant species is incorporated into the Si during a melt/regrowth step that is initiated by a homogenized $\lambda = 308$ nm XeCl pulsed excimer laser beam (Fig. 3-46). A significant feature of this approach is that no high-temperature anneals are required following the source/drain doping step. Boron-doped junctions with depths of 25 - 150 nm and sheet-resistance values down to 20 Ω/sq (at a junction depth of 110 nm) have reportedly been fabricated using the GILD process (Fig. 3-47).[121] PMOS devices with gate lengths of 0.8 μm exhibiting good

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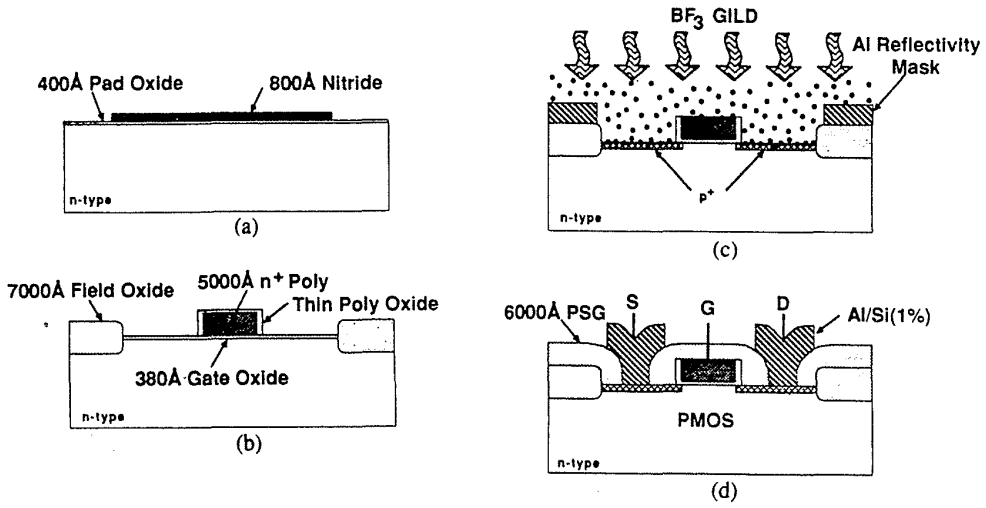

Fig. 3-46 Key steps in the GILD PMOS process: (a) active area definition, (b) after poly deposition, n^+ doping, patterning, and oxidation, (c) GILD laser doping step for p^+ source/drain formation, and (d) after PSG and Al/Si (1 %) deposition and etching.[121] (© 1988 IEEE).

performance have also been demonstrated using the GILD method.

A final novel technique for forming shallow junctions is *photo-enhanced epitaxy*. In this approach, a silicon epitaxial film is grown at low temperatures (<650°C) by the photo-enhanced dissociation of disilane under UV irradiation.[146] The UV radiation also

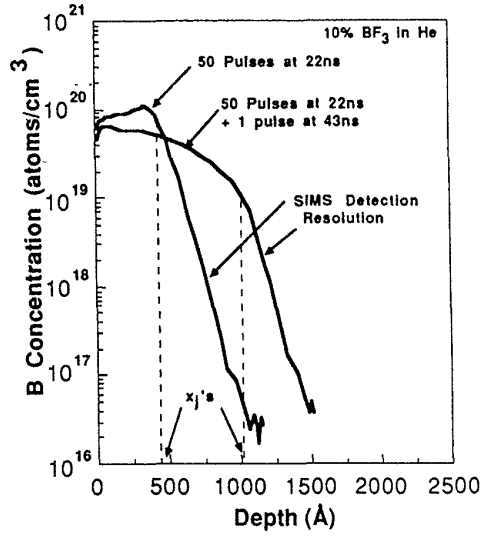

Fig. 3-47 SIMS profiles of boron (^{10}B plus ^{11}B) laser-doped junctions. The shallow profile received 50 laser pulses at 22-ns silicon melt, while the deeper profile received one additional pulse at 43-ns melt time. The actual junction depths are estimated to be 450 and 1000 Å, respectively.[121] (© 1988 IEEE).

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activates the boron that is incorporated in the epitaxial film during growth. Ultra-shallow (< 0.1 μm) p^+n junctions were reported to have been formed with photo-enhanced epitaxy.

3.10.3 Impact of Shallow Junctions on Contact Formation

The use of shallow junctions implies the need for planar contact interfaces that penetrate the original Si surface only slightly (or better, not at all), as well as a barrier layer to prevent Si from diffusing into any Al layers (which would thereby cause junction spiking). If a contact layer is used that consumes some Si during the contact formation (e.g., as occurs when PtSi, $TiSi_2$, $CoSi_2$, and CVD W layers are used to contact Si), measures must be taken to prevent excess Si from from being consumed. The considerations necessary for selecting the correct thickness of Ti in an Al-TiN-Ti-Si contact structure to 0.2-μm deep junctions are presented in reference 81. As noted earlier, CVD W seems to be adequate for making direct contact to junctions greater than 250 nm deep, if the silane reduction process is used.

The approach of diffusing the dopant from a polysilicon layer or a selectively grown epitaxial layer on the Si (described in the section on self-aligned contacts) offers another solution to the problem of how to form a reliable contact to shallow junctions. In such cases the metal makes contact to the deposited Si far from the original Si interface (and therefore away from the shallow junction as well).

3.11 BURIED CONTACTS AND LOCAL INTERCONNECTS

3.11.1 Butted Contacts and Buried Contacts

When silicon-gate technology was developed, a means had to be provided for making contact between the polysilicon layer and the single-crystal substrate. In early silicon-gate MOS circuits, such contacts were made by using either a metal link to interconnect the polysilicon and the substrate (Fig. 3-48), or by so-called *butted contacts*. The latter were subsequently replaced by *buried contacts*, which became a standard structure in NMOS ICs.

With the *butted contact*, polysilicon is aligned with the edge of the active-device area to which the contact will be established. This is done by patterning the polysilicon film after it has been deposited. After an insulating layer has been deposited to cover the poly, a contact window that overlaps both the poly and the substrate is opened, exposing both the poly layer and the substrate. Metal is deposited to fill the contact, thereby electrically strapping the two regions together (Fig. 3-49). The butted contact conserves area by eliminating the space required between the separate contact windows when the approach of Fig. 3-48 is used.

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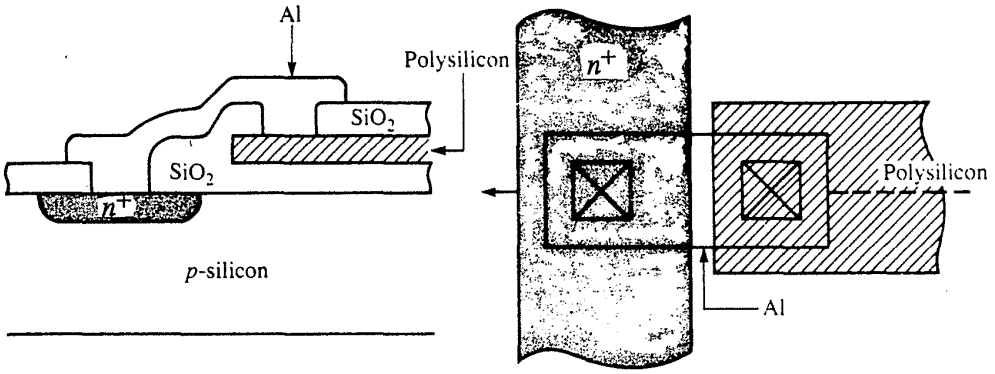

Fig. 3-48 Aluminum film link for connecting polysilicon and the silicon substrate with an intervening space. From R. C. Jaeger, *Introduction to Microelectronic Fabrication.* Copyright, 1988, Addison-Wesley. Reprinted with permission.

The term "butted contact" derives from the fact that the poly and the substrate edges butt up against one another, but do not actually make electrical contact. Since the poly is separated from the substrate by an oxide layer even when the contact window is opened, a linking metal film must still be deposited to electrically connect the poly and the substrate.

With the *buried contact*, direct contact is made between polysilicon and the substrate, eliminating the need for a metal link to form the contact (Fig. 3-50). In this structure, a window is opened in the thin gate oxide over the substrate area at which the contact is to be established. When the polysilicon is subsequently deposited, it is in direct contact with the substrate in these openings but is isolated from the substrate by the gate and field oxides everywhere else. An ohmic contact is formed at the poly-substrate Si interface by the diffusion into the substrate of dopant present in the polysilicon. This

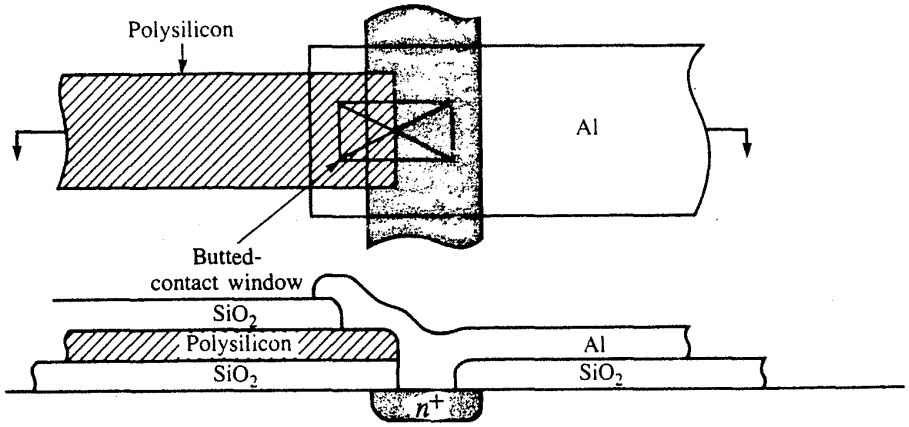

Fig. 3-49 Cross section of a butted-contact structure. From R. C. Jaeger, *Introduction to Microelectronic Fabrication.* Copyright, 1988, Addison-Wesley. Reprinted with permission.

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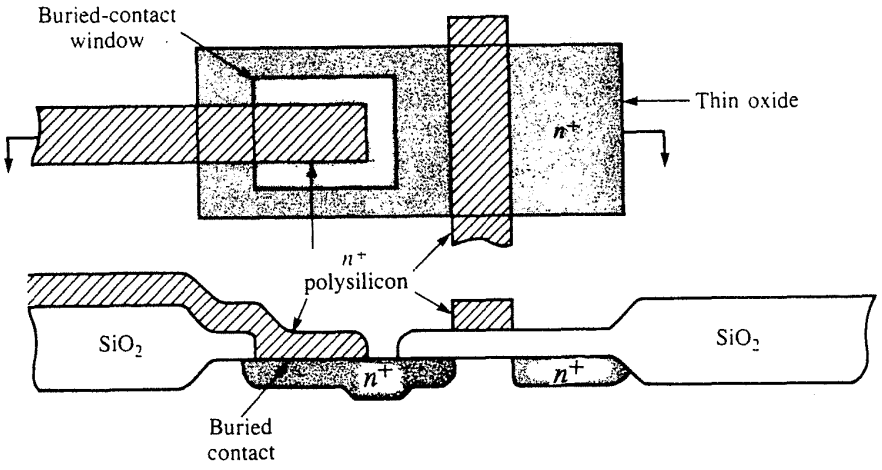

Fig. 3-50 Cross section of a buried-contact structure. From R. C. Jaeger, *Introduction to Microelectronic Fabrication*. Copyright, 1988, Addison-Wesley. Reprinted with permission.

in effect merges the two silicon regions. A CVD layer of insulating film is then deposited to cover the contact. The structure is called a "buried contact" because a metal layer can cross over the area of the substrate where a contact has been established without making an electrical connection to it.

The use of buried contacts in silicon-gate technology provides an important benefit in that it makes available an additional level of interconnect on the integrated circuit. This extra layer allows some of the circuit connections to be formed before the metal layer is deposited, and its availability adds significant interconnect routing flexibility to the design task. However, this additional interconnect level does not exist in technologies using butted contacts, since a metal link is needed to establish each poly/substrate contact.

3.11.2 Local Interconnects

Even when used with buried contacts, the polysilicon interconnect layer is not as universal as the metal interconnect layer because the sheet resistance of the polysilicon layer is much higher than that of Al. Furthermore, the poly layer is used both as a *gate material* and an *interconnect material*. Consequently, when the poly film acts as an interconnect structure, it cannot cross over regions where a transistor gate exists without making a contact to the gate. Therefore, unless such contacts are desired, gate locations represent areas on the wafer that cannot be crossed by poly films when these are being used as interconnect structures.

The metal layer, on the other hand, is allowed to pass over polysilicon gates (since these have been covered with SiO_2 before the deposition of the metal). That is to say, there are no areas of the chip surface over which the metal line is restricted from being routed. Such unrestricted interconnect levels are therefore referred to as *global interconnect levels* to distinguish them from such routing-restricted interconnect levels

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as the polysilicon with buried contacts. The routing-restricted levels have been termed *local interconnect (LI) levels*, because their higher resistivities make them best used for such short metallization runs as those that locally interconnect gates and drains in NMOS circuits.

Other materials besides polysilicon have been used to establish such local interconnects. For example, in NMOS, local interconnect structures were implemented using bilayer conductor structures, with a refractory metal-silicide layer (i.e., WSi_2, $TaSi_2$, $MoSi_2$, or $TiSi_2$) on top of a polysilicon layer. Such structures, referred to as *polycides*, were adopted as a means of reducing the relatively high resistivity of heavily doped polysilicon.

Establishing an LI level is more complex in CMOS than in NMOS, and most early CMOS processes did not implement a local interconnect level. The difficulties were these:

- The polysilicon layer in CMOS was normally doped *n*-type. Even when used just as an underlayer in a polycide structure, such poly could not be used to make buried contacts to the source/drain regions of PMOS devices.
- Phosphorus outdiffusion limits device isolation and buried-contact design rule scaling (Fig. 3-51).
- In the conventional buried-contact process, the gate oxide must be patterned before the poly is deposited. This patterning step can adversely impact yield if the oxide is scaled to 25 nm and below.

The fact that buried contacts were not implemented was one of the factors that historically kept the packing density of CMOS circuits less than that of NMOS circuits. Recently, however, several LI technologies for advanced CMOS have been reported, including selective formation of $TiSi_2$, Ti:W over $CoSi_2$, TiN over $TiSi_2$, and dual-doped polysilicon.

Despite the fact that LI levels cannot be used as universally as metal layers, their

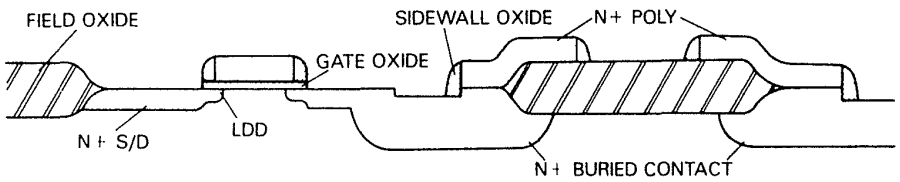

Fig. 3-51 Limitations of buried contacts: (1) Phosphorus outdiffusion limits device isolation and buried-contact-to-gate design-rule scaling. (2) The use of *n*-type polysilicon limits buried contacts in CMOS to *n*-channel transistors only.[124] (© 1987 IEEE).

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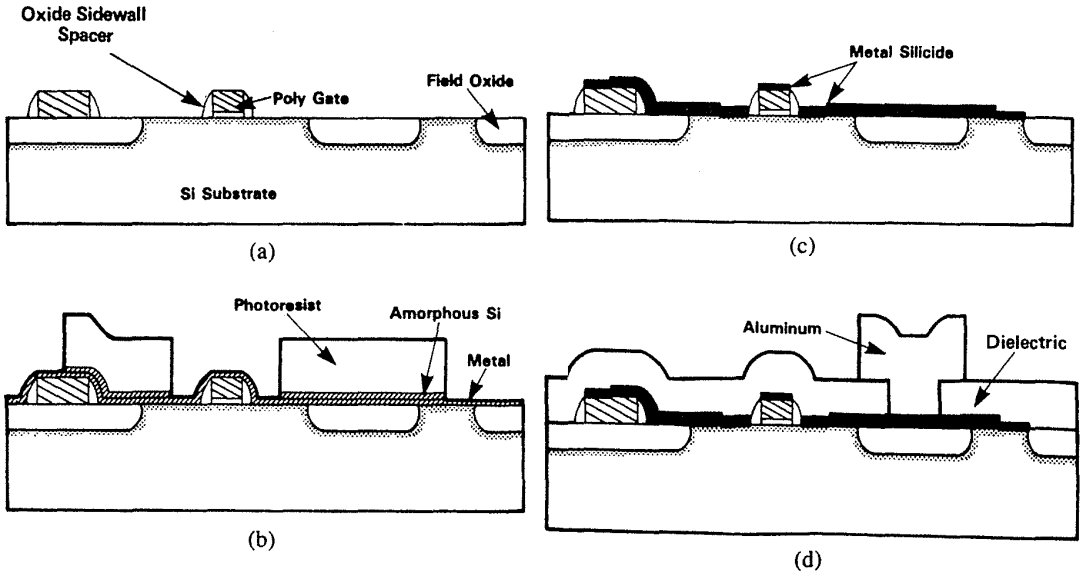

Fig. 3-52 Fabrication of HPSAC technology. Cross-sectional view after (a) sidewall spacer formation; (b) patterning and etching of amorphous silicon layer; (c) silicide formation; and (d) aluminum alloying.[122] (© 1984 IEEE).

implementation still allows significant chip-area savings for VLSI logic and SRAM designs. According to one report, SRAM cell layouts were reduced by up to 25% when an LI level was made available.[124] The reduction of cell size in such regular structures as SRAMs by use of local interconnects is considered in further detail in a more recent reference as well.[159]

3.11.2.1 Selectively Formed $TiSi_2$. The selective formation of $TiSi_2$ to form an LI level (Fig. 3-52) was first described in 1984, and the process is referred to as *high-performance self-aligned contact and local interconnection* (HPSAC).[122] In this approach, conventional MOS processing is carried out up to the formation of oxide sidewall spacers and the definition of source/drain regions (Fig. 3-52a). A layer of Ti is then deposited, followed by a layer of amorphous Si (e.g., 40-50 nm and 80-100 nm thick, respectively). The thickness of the Si layer is chosen so that the Si will react fully with the underlying Ti layer.

Both layers are sequentially sputter-deposited in one pumpdown to minimize the formation of an oxide on the Ti layer (which could retard silicide formation). The amorphous Si layer is then patterned, by means of a plasma-etching process that has high selectivity to the underlying Ti layer (so that as little of the Ti is removed during any overetch of the Si; see Fig. 3-52c).

Next, the silicide is formed in a 600°C anneal in N_2. The Ti in contact with the substrate reacts with that Si to form $TiSi_2$. The Ti on SiO_2 does not react unless it is covered by amorphous Si, in which case $TiSi_2$ is also formed. The unreacted Ti (on which a thin layer of TiN actually forms) is then selectively removed with an $H_2SO_4 + H_2O_2$ solution. A final 800°C anneal is used to reduce the resistivity of the $TiSi_2$.

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Since this process produces an LI layer of $TiSi_2$, as well as $TiSi_2$-Si contacts, it can be used to establish contacts between gate and source/drain regions (in addition to contacts between neighboring source/drain regions). Because the $TiSi_2$ layer in this structure has a sheet resistance of ~3 Ω/sq and is thin (<150 nm), metal-layer step-coverage problems are not significantly exacerbated. In addition, the ρ_c of $TiSi_2$ to Si is 20 Ω-μm^2 to n^+Si and 100 Ω-μm^2 to p^+Si.

A CVD layer of BPSG is then deposited, and openings are created in it so that an Al overlayer can make contact to the $TiSi_2$ LI layer. Such Al-$TiSi_2$ contacts can be made over field-oxide region because the $TiSi_2$ extends over these regions. However, if the Al-$TiSi_2$ contacts overlap the field oxide and source/drain region (as that shown in Fig. 3-53), a barrier metal such as Ti:W, needs to be inserted to prevent Al from diffusing through the silicide into the Si substrate.

Several processing challenges must nevertheless be overcome in order for the HPSAC process to be successfully implemented. First, the Si-to-Ti etch selectivity must be quite high so that Ti is not excessively removed over contact regions during the overetch of the amorphous Si. Second, the gate edges must be cleared of Si during the Si-removal step, and of Ti during the Ti-removal step. Third, low-leakage, shallow-junction processes must be incorporated (since the $TiSi_2$ consumes some Si during the Si contact formation). Fourth, as the amorphous Si that covers the Ti prevents nitrogen stuffing of the Ti grain boundaries, Si can rapidly diffuse along these grain-boundary paths at the same time that the Ti is reacting with the Si to form $TiSi_2$. This effect becomes a problem when a small area of the Si substrate is in contact with a larger area of Ti (>5x the area of the exposed Si substrate), because sufficient Si from the substrate can be "sucked out" by the Ti to cause pitting of the Si. Thus, the area of the Ti interconnect runner above the field oxide connected to a silicon contact must be restricted by design.[154] Finally, phosphorus has a high diffusivity in $TiSi_2$. Hence, under some conditions phosphorus from the polysilicon gate regions in contact with the $TiSi_2$ could diffuse through the $TiSi_2$ and counterdope p^+ junctions. To prevent this

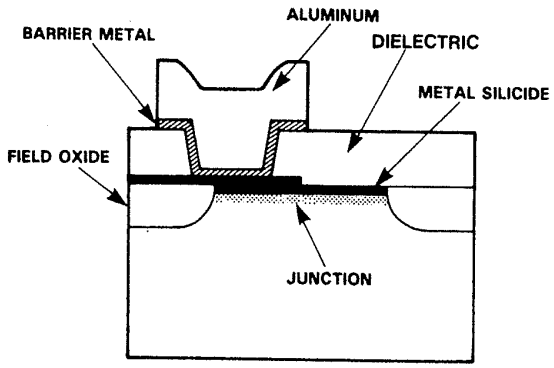

Fig. 3-53 HPSAC contact overlapping source-drain region and field oxide.[122] (© 1984 IEEE).

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occurrence, either the thermal budget following silicide formation must be appropriately restricted, or an alternative polysilicon electrode structure must be employed (see chap. 6, section 6.3).

3.11.2.2 Ti:W over $CoSi_2$. In this approach, a Ti:W layer is sputter-deposited over the entire wafer surface, including regions in which self-aligned contacts to Si by $CoSi_2$ are exposed. The sputter deposition is carried out in an ambient containing $Ar + N_2$, so that nitrogen is incorporated into the Ti:W film to improve its diffusion-barrier properties. The Ti:W film is then patterned to form the LI structure. The advantage of this method is that the Ti:W should be a better barrier to the diffusion of phosphorus than is the $TiSi_2$ film of the HPSAC process. Regions of n^+ and p^+ Si can therefore be connected with the Ti:W film with less concern about counterdoping of one type of poly by the other.[123] The implementation of a $CoSi_2$ layer as an LI was also studied.[123] However, because void formation at the $CoSi_2/SiO_2$ interface was observed, concerns were raised about possible adhesion problems between the $CoSi_2$ and SiO_2 materials.

3.11.2.3 TiN Formed over $TiSi_2$. In this process of LI formation for CMOS, first reported in 1985,[124] a TiN layer is formed on a layer of Ti as the reaction to form $TiSi_2$ is occurring. The process steps are the same as those used in the HPSAC process through the deposition of the Ti layer (Fig. 3-54a). At that point, instead of depositing an amorphous Si layer, the Ti (e.g., 100-nm thick) is annealed in an ambient containing

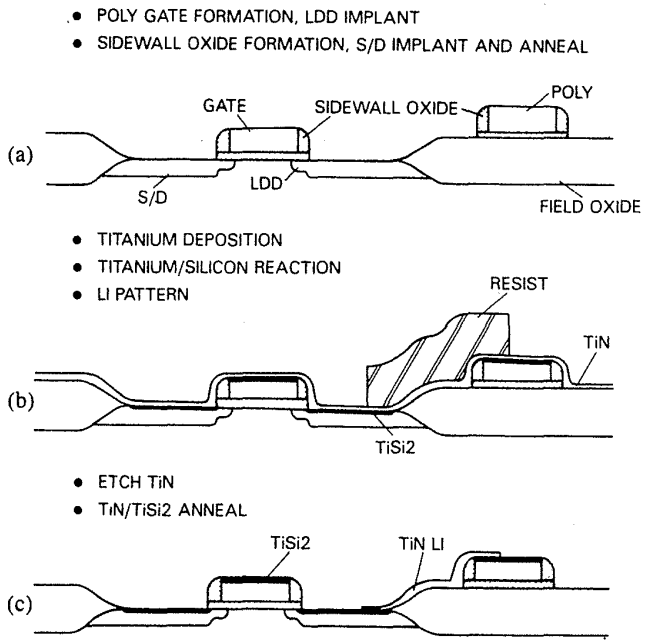

Fig. 3-54 Self-aligned $TiSi_2$ process showing the TiN LI patterning step.[124] (© 1987 IEEE).

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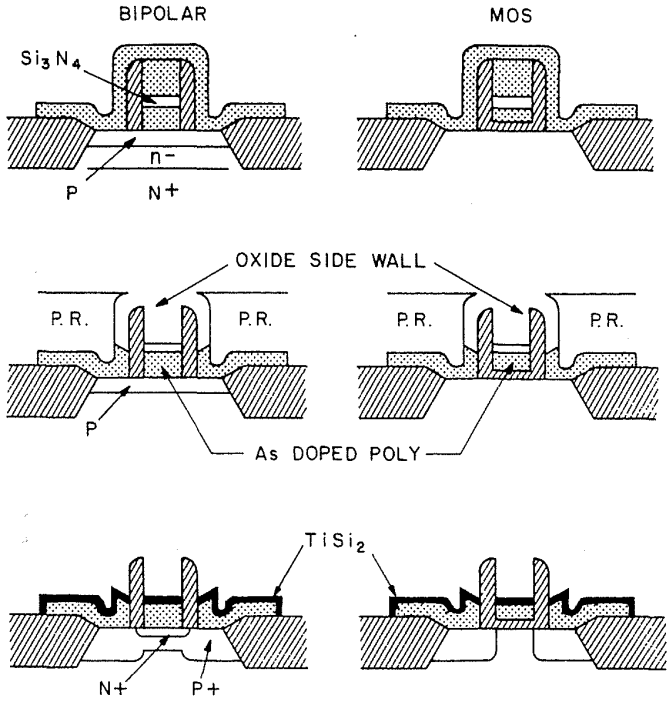

Fig. 3-55 (a) SDB poly is deposited over the wafer. (b) Planarization resist is etched back, exposing top of the gate/emitter stack. This figure depicts the structure after isotropic polysilicon etch. (c) This figure shows the devices after salicide process.[127] (© 1987 IEEE).

N_2 at 675°C. The Ti in contact with the SiO_2 reacts with the nitrogen to form a film of TiN ~110 nm thick. The Ti in contact with the Si forms a top layer of TiN that is ~40-nm thick: beneath this surface layer of TiN, a 150-nm-thick layer of $TiSi_2$ is formed. By varying the temperature and ambient gas during the anneal, it is possible to obtain various TiN-$TiSi_2$ thickness combinations.

Following this anneal step, the TiN is patterned with a two-step, dry/wet etch process (Fig. 3-54b). The fluorine-based dry-etch step removes the TiN from the unmasked SiO_2 regions, as well as from on top of the unmasked $TiSi_2$ regions (Fig. 3-54c). The wet portion of the etch process is used to remove any stringers of TiN that might remain at the base of the transistor sidewall oxide. Following the etch-and-resist strip, an 800°C anneal is performed to reduce the $TiSi_2$ and the TiN sheet resistivities to 1.0-1.5 Ω/sq and 10-20 Ω/sq, respectively.

This process has several advantages over the HPSAC process. First, the TiN LI layer can be formed without the need for any layers other than Ti to be deposited. Second, the TiN is an excellent diffusion barrier, and prevents phosphorus from n^+ poly from counterdoping p^+ junctions. Similarly, the TiN can serve as a diffusion-barrier material when contacts such as those shown in Fig. 3-53 are used.

3.11.2.4 Dual-Doped Polysilicon LI with Diffused Source/Drain Junctions. In the second dual-doped polysilicon LI process, some of the limitations

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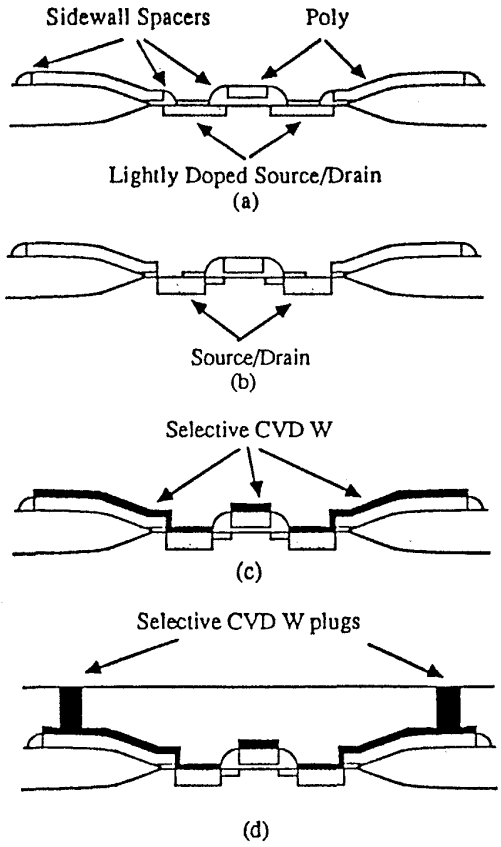

Fig. 3-56 Processing sequence of selective CVD W local interconnect technology. Cross sectional view after (a) sidewall spacer formation., (b) selective removal of sidewall spacer of local interconnect and source/drain formation, (c) selective CVD W deposition, and (d) selective CVD W plug filling.[128] (© 1988 IEEE).

of the first poly LI process are overcome, but at the cost of introducing a more complex process for formation of the gate structure.[124,127] In this approach, three separate polysilicon layers are deposited (Figure 3-55). The final poly layer makes direct contact with the exposed source/drain regions and is selectively doped by means of ion implantation after it is deposited.

An etch step is then used to remove part of poly 3 and all of poly 2, creating the gate structure shown in Fig. 3-55b. This structure has oxide sidewalls protruding 600 nm above the top of poly 1 (gate poly) and the remaining parts of poly 3 (source/drain dopant and LI poly). The dopants implanted in the poly are then driven into the Si substrate by means of a diffusion step, to simultaneously form the buried contacts and the source/drain junctions. All of the polysilicon (poly 3 and the gate poly) is then selectively clad with a $TiSi_2$ layer. The protruding oxide sidewalls prevent any bridging

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of $TiSi_2$ between gate and LI poly. It should be noted, however, that this approach requires increased process complexity, and the problem of dual-doped poly counterdoping through the silicide can still occur.

3.11.2.5 CVD W-Clad Polysilicon LI. Another LI process in which W is selectively deposited onto patterned polysilicon in the field regions and onto the exposed source/drain regions was recently described.[128] In this method, isolated polysilicon runners in the field regions are patterned at the same time as the polysilicon gate structures (Fig. 3-56). Following LDD and source/drain-region formation, a thin layer of CVD W is selectively deposited onto the gate poly, the exposed source/drain regions, and the LI poly runners in the field regions.

With this approach, it is not necessary to perform selective etching of the LI layer. In addition, redistribution of the dopants through the poly into the source/drain regions will not occur, since the LI poly is not in contact with the source/drain regions (instead, the LI poly and the source/drain regions are connected by the CVD W). Since the CVD W also straps the entire source/drain region, care must be taken to ensure that increased diode leakage currents are not produced. This is believed to be feasible if the CVD W is performed using the silane (SiH_4) reduction of WF_6, which has been shown to suppress encroachment and wormholes (two of the main sources of such leakage currents).

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PROBLEMS

3.1 An ohmic contact has an area of 10^{-3} cm^2. The ohmic contact is formed in an n-type silicon. If $N_D = 5x10^{19}$ cm^{-3}, $\phi_b = 0.8$ eV, and the tunneling effective mass is $0.26m_o$, find the voltage drop across the contact when a forward current of 1 A flows through it.

3.2 For a 0.5 μm n-channel MOSFET with t_{ox} = 20 nm, W = 10 μm, and μ_n (electron surface mobility) = 500 cm^2/V-sec, if the source/drain sheet resistance is 100 W/sq and the source or drain contact to poly-gate distance is 1.0 μm, calculate R_S and R_{ch}.

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3.3 Explain why the use of Eq. 3-4 to estimate the value of R_{co} in small contacts from data obtained using larger-sized contacts will lead to erroneous results.

3.4 Explain why the contact chain structure is not appropriate for obtaining accurate contact resistance data.

3.5 Assume that a 500x15 μm aluminum line makes contact with Si through a 10x10 μm contact window. The Al line is 1 μm thick and is annealed at 450 °C for 30 min. Assume also that the Si will saturate the Al up to a distance of $\sqrt{Dt}$ from the contact, where D = 0.04 cm^2/sec and E_A = 0.92 eV. If the Si is absorbed uniformly through the contact, and the density of the Al and the Si are taken to be equal, how deep will the Al penetrate into the Si (as a result of the Si departing to saturate the Al)?

3.6 If the sintering step of an Al-Si contact is 450C for 30 min, estimate the maximum thickness of the native oxide that will allow Al to diffuse and make intimate contact with the Si substrate (assuming that the Al_2O_3 that is formed is as thick as the native oxide that it consumes to form the Al_2O_3)?

3.7 Explain why use of Al:Si alloys to make contact to *n*-type Si can lead to contacts that exhibit large values of contact resistance.

3.8 Explain why the PtSi formed in the contact windows during the self-aligned PtSi contact process is not attacked by the aqua regia used to strip the unreacted Pt.

3.9 Compare the advantages and disadvantages of $TiSi_2$ and $CoSi_2$ for salicide applications.

3.10 Compare the HPSAC $TiSi_2$ local interconnect technique with the TiN-formed-over $TiSi_2$ technique for fabricating a local interconnect layer for CMOS or BiCMOS.

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CHAPTER 4

MULTILEVEL-INTERCONNECT TECHNOLOGY FOR VLSI AND ULSI

In order to build an integrated circuit, its necessary to fabricate many active devices on a single substrate. Initially, each of the devices must be electrically isolated from the others, but later in the fabrication sequence specific devices must be electrically interconnected so as to implement the desired circuit function. In chapter 2 we considered the technologies used to isolate the devices, and in chapter 3 we described the fabrication of *contacts* between the interconnect materials and the Si substrate. This chapter is concerned with the fabrication technology of the interconnect structures themselves.

Since both MOS and bipolar VLSI and ULSI devices invariably require more than one level of interconnect, much of this chapter deals with the issues involved in creating such *multilevel-interconnect* structures. The three main challenges in implementing such structures for submicron devices are the following:

1. Planarization of the intermetal dielectric layers,
2. Filling of high-aspect-ratio (and varying-depth) contact holes and vias, and
3. Integration of new conductor materials that exhibit low resistance, high reliability, and process compatibility.

4.1 EARLY DEVELOPMENT OF INTERCONNECT TECHNOLOGY FOR INTEGRATED CIRCUITS

4.1.1 Interconnects for Early Bipolar ICs

Robert N. Noyce invented the monolithic integrated-circuit concept while at Fairchild. His patent application in 1959 described how planar silicon bipolar transistors and resistors could be interconnected with thin and narrow aluminum lines over the surface-passivation oxide. The interconnects in the early generations of bipolar ICs typically consisted of a single level of metal (Al) and heavily doped diffused regions in the silicon

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substrate (although single-level-metal layers consisting of other materials – including the multilayer Ti/Pt/Au film – were also developed).* By the late 1960s, however, interconnects with two levels of metal were needed for bipolar SSI and MSI circuits, and these were implemented using Al for both levels of metal.

The *diffused regions in the silicon substrate* used in early ICs as interconnect paths (Fig. 4-1) were fabricated by selectively diffusing dopant impurities of the type opposite to those present in the substrate. In order for isolation to the substrate to be maintained, any voltage applied to such regions had to be of a polarity that kept the junctions under reverse bias. The relatively high sheet resistance and capacitance of such diffused regions, however, limited them to short-distance interconnection-path applications; the relatively large RC product of long diffused lines causes unacceptably large propagation delays for signals transmitted along them.

Such diffused regions have a minimum resistivity of ~1000 $\mu\Omega$-cm; much higher than that of Al (2.7 $\mu\Omega$-cm). In addition, the capacitance of the structure is that of a reverse-biased *pn* junction formed between the diffused region and the substrate. The capacitance can be calculated by treating the structure as a one-sided step junction in which the depletion layer extends primarily into the lighter doped substrate. The capacitance, C, per unit area is then given by

$$C = \sqrt{\frac{q N_s K_{si} \varepsilon_o}{2(\varphi_{bi} + V_R)}} \qquad (4-1)$$

$$\varphi_{bi} = \left[\frac{kT}{q} \ln\left(\frac{N_s}{n_i}\right)\right] + 0.56 \text{ V} \qquad (4-2)$$

where N_s is the substrate doping, φ_{bi} is the built-in potential of the junction, n_i is the intrinsic carrier concentration, and V_R is the reverse bias applied to the junction. In practice, the capacitance of the diffused regions is about 2.5 times as large as the capacitance of the polysilicon interconnects (~1×10^{-4} pf/μm^2 vs. ~0.4×10^{-4} pf/μm^2).

The term *metal pitch* is widely used to describe the dimensions of a metal system. The pitch of a metallization system is the minimum centerline-to-centerline dimension of two adjacent metal lines (Fig. 4-2a); consequently, it is also the sum of the minimum metal-line width and minimum spacing of a metal system. Figure 4-2b shows how the metal pitch has decreased as IC technology has evolved.[218]

* Jack S. Kilby of Texas Instruments made a working phase-shift oscillator on a single chip of Ge in September 1958 and filed a patent application for the integrated circuit in February 1959. He is generally regarded as an independent co-inventor of the integrated circuit. Because Kilby used gold wires to interconnect the devices in the Ge substrate, a U.S court of appeals ruled that Noyce was the inventor of the *monolithic* technique. It was recognized that Noyce's invention implemented the integrated circuit through the use of an adherent oxide, junction isolation, and Al-film interconnection lines – the latter which were also adherent to the oxide and were formed by deposition and photolithographic etching.

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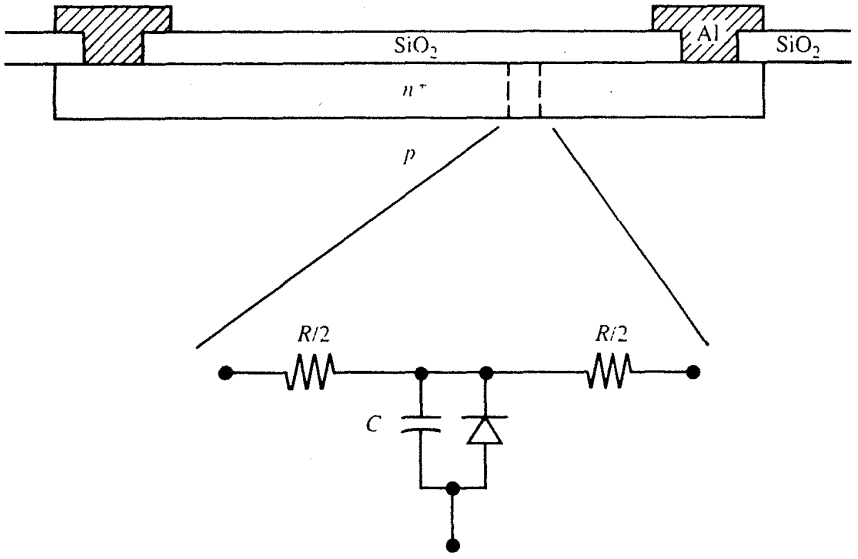

Fig. 4-1 A lumped circuit model for a small section of an n^+ diffusion. The RC delay limits the use of diffusions for high-speed signal distribution. From R. C. Jaeger, *Introduction to Microelectronic Fabrication.* Copyright, 1988, Addison-Wesley. Reprinted with permission.

4.1.2 Interconnects in Silicon-Gate NMOS ICs

Diffused regions and Al thin films were used as interconnection structures in early aluminum-gate MOS ICs. This did not significantly degrade their performance, since they were already relatively slower than their bipolar counterparts. With the advent of silicon-gate MOS technology, MOS ICs gained another level of interconnect – namely, heavily doped polysilicon (see chap. 5). With the implementation of buried contacts (see chap. 3), the polysilicon level could function as a local-interconnect level. This additional interconnect layer gave MOS devices an advantage in routing flexibility over bipolar ICs fabricated with only a single-metal interconnect level.

The major drawback of polysilicon is that its resistivity is comparable to that of the diffused regions, and is thus much higher than that of Al (i.e., 1000 $\mu\Omega$-cm vs. 2.7 $\mu\Omega$-cm). Polysilicon lines were nevertheless better suited than diffused regions to serve as interconnect paths because of their smaller capacitance per unit area. The development of double-polysilicon technologies (in which two levels of polysilicon are used) extended the use of polysilicon interconnects in ICs to the mid 1980s. For example, the double-poly process is needed to implement compact SRAM-cells that use polysilicon loads, as well as compact DRAM cells (see chap. 8). Such double-poly processes were used until the advent of the 64-kbit DRAM generation.

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Eventually, however, chip sizes became so large and MOS-device performance so much improved (primarily as a result of shrinking device dimensions) that the resistance of the polysilicon interconnect structures began to significantly degrade the speed of the circuits. As a result, *polycides* were developed as a means of retaining the advantages of polysilicon while reducing the impact of the large polysilicon resistivity (see Vol. 1, chap. 11). Through the formation a refractory-metal silicide on top of the polysilicon runners, a polycide structure (in which the resistivity was reduced to ~50-100 $\mu\Omega$-cm) became available as an interconnect and gate layer. Interconnect technologies that used one level of metal, one level of polycide, and one level of polysilicon were therefore common in NMOS ICs used to fabricate 16-bit microprocessors, as well as in MOS DRAMs of the 256-kbit and 1-Mbit generations.

4.1.3 Evolution of Interconnects for Bipolar ICs

As bipolar technology advanced, smaller device sizes and circuits with higher functional

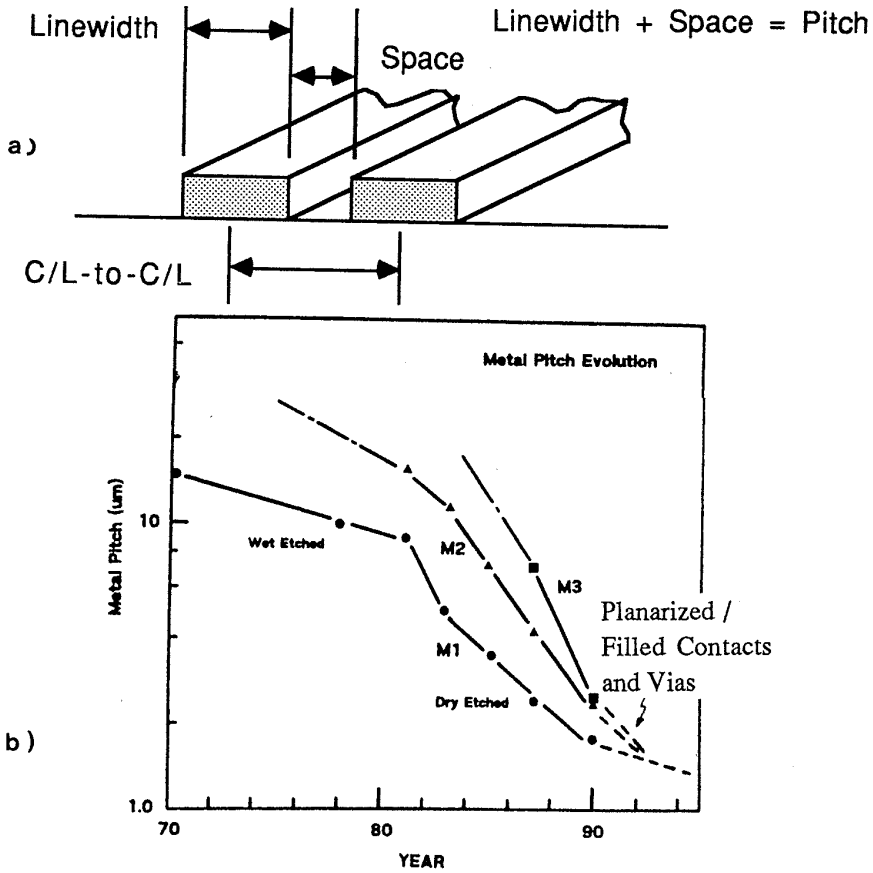

Fig. 4-2 (a) Definition of *metal pitch*. (b) Advanced process integration techniques have enabled the development of multilayer interconnects with tight pitches.[218] This paper was originally presented at the Spring 1989 Meeting of The Electrochemical Society, Inc. held in Los Angeles, CA.

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densities were implemented. In order to obtain the flexibility needed to interconnect larger numbers of devices, it became necessary to develop a second interconnect level. Since no equivalent to Si-gate technology evolved in bipolar IC processing, polysilicon did not have to be automatically accepted as the second interconnect level. In fact the speed penalty imposed by the use of polysilicon would have eliminated the chief advantage of bipolar technology over MOS ICs (higher speed); thus, two-level *metal* interconnect technologies had to be developed. These emerged during the late 1960s and the 1970s. The shallow emitter-base junctions of bipolar devices also forced manufacturers of bipolar ICs to develop diffusion barrier technology for contacts before barrier layers were needed for MOS contacts.

4.1.4 Evolution of Interconnects for CMOS ICs

When CMOS replaced NMOS as the leading MOS IC technology in the mid 1980s, the interconnect technology also had to be modified to fit the needs of CMOS. For example, the local interconnect level of polysilicon could not serve CMOS as effectively as NMOS; since polysilicon in CMOS is normally *n*-doped, it cannot be used to make ohmic contacts to the source and drain regions of PMOS devices. As a result, it became necessary to develop two-level-metal technologies to provide CMOS VLSI circuits with sufficient routing flexibility. The shallow junctions needed in 2 μm and smaller MOS technologies also forced the use of diffusion-barrier technology in the contacts of CMOS ICs.

Implementing a two-level-metal process is more difficult in CMOS than in bipolar technologies because the underlying wafer topography is more rugged in CMOS (due primarily to the field-oxide steps arising from the semirecessed LOCOS process, and to the steps caused by the polysilicon layer). Severe topography conditions give rise to step-coverage problems. Nevertheless, the significant benefits offered by multilevel metal-interconnect technology eventually forced the challenges of integrating it into CMOS processes to be undertaken.

4.2 THE NEED FOR MULTILEVEL-INTERCONNECT TECHNOLOGY

Throughout the evolution of integrated circuits, the aim of device scaling has been twofold: (1) to increase circuit performance (mainly by increasing circuit speed), and (2) to increase the functional complexity of the circuits. At the outset, scaling down of active device sizes was a very effective means of achieving these goals. Eventually, the scaling of active devices became less profitable, as the limitations of the circuit speed and maximum functional density came to depend more on the characteristics of the interconnects than on the scaled devices. In addition, the aspects of silicon utilization, chip cost, and ease and flexibility of IC design were also adversely affected by the interconnect-technology restrictions. The approaches to lifting these limitations have predominantly involved the implementation of multilevel-interconnect schemes.

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This section will first explain how the speed and functional density of ICs can be limited by the interconnect technology, and it will then indicate why multilevel interconnects are effective in counteracting this problem. Also, notation that is used throughout the chapter in descriptions of various features of a multilevel-interconnect structure will also be introduced.

4.2.1 Interconnect Limitations of VLSI

4.2.1.1 Functional Density. In the course of integrated-circuit evolution, the maximum number of devices per chip has steadily increased, mainly as a result of the increase in functional density (although the growth in chip area has also played a role). *Functional density* is defined as the number of interconnected devices per chip area, while the number of devices per chip area is referred to as the *active-device density*. As the minimum feature size on an IC decreases, the active device density increases. The functional density, however, also depends on how effectively these devices can be interconnected. Unless a larger number of the devices can be interconnected as the active-device density is increased, there will be no gain in functional density.

When integrated circuits contained only a relatively small number of devices per chip, the devices could be more easily interconnected. This situation persisted for some time, even as the active-device density steadily increased. Nevertheless, the area occupied by the interconnection lines on the chip surface grew more quickly than the area needed to accommodate the active devices. Eventually, the condition was reached in which the minimum chip area became interconnect-limited - that is, the area needed to route the interconnect lines between the active devices exceeded the area occupied by the active devices. At this point, continued shrinking of active devices produced less circuit-performance benefits.

One way to overcome such a limitation is to implement a multilevel-interconnection system in which the area needed by the interconnect lines is shared among two or more levels. This allows the fractional area of the chip occupied by active devices to be increased, leading to an increase in the functional density. The following is a simple example illustrating why the chip surface becomes interconnect-area-limited as the active-device density is increased.

Assume that devices are fabricated using a *single-level interconnect technology* on a chip of constant area, and that the active-device density is increased by a factor of 10 (e.g., the number of logic gates per chip is increased from 100 to 1,000). Furthermore, assume that the minimum line width of the metal lines is scaled by the same factor used to scale the size of the logic gates (i.e., by the square root of the area decrease). If the minimum metal line width is initially w, and B is the number of squares of metal in the total line length, the total line length is Bw, and the area of the chip covered by the metal will be Bw^2 (Fig. 4-3a).

When the condition of increased active-device density is considered, the scaled area of one minimum square of metal film is seen to be be $w^2/10$. In addition, the total length of the interconnection lines will also be increased, due to two factors: (1) since there are more gates, a larger number of connections between gates must be made, and (2) the

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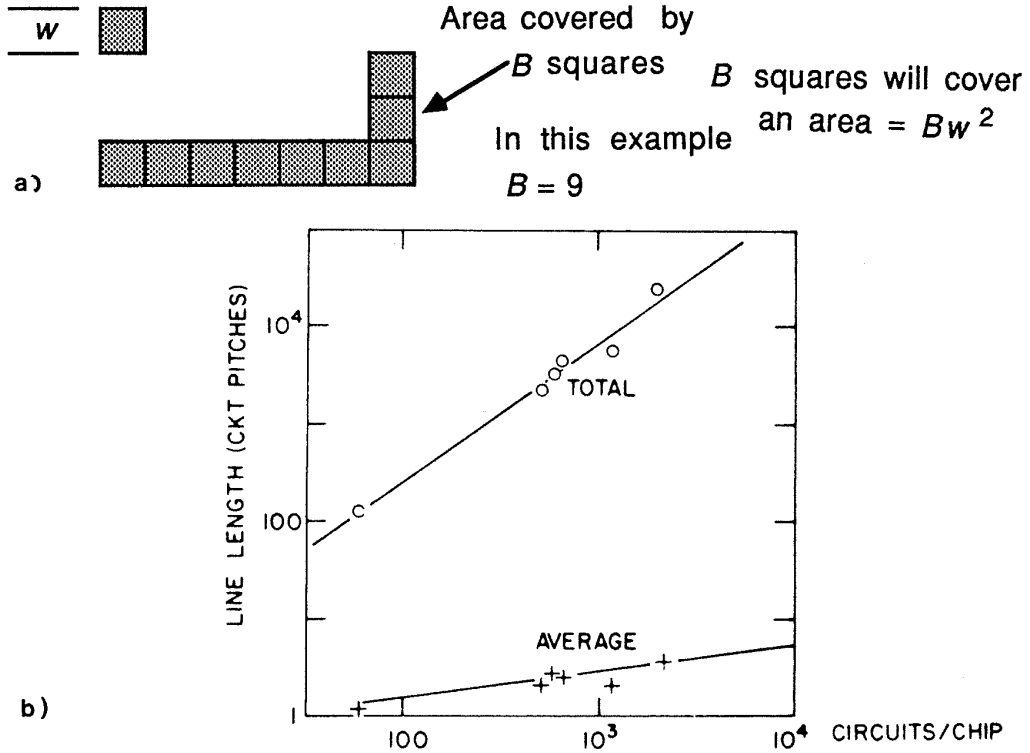

Fig. 4-3 (a) The area of a chip covered with B squares of metal whose sides are w wide, is Bw^2. (b) The average length of interconnect and the total wire length on a logic chip as a function of device density. The lengths are measured in circuit pitches, i.e., the square root of the area per circuit.[1] (© 1981 IEEE).

average length of the interconnection lines will increase. This latter effect is plotted in Fig. 4-3b.[1] The graph in Fig. 4-3 also shows the total line length as the number of logic gates is increased from 100 to 1000. (Note that the lengths are expressed in *circuit pitches* – that is, the graph actually indicates the number of squares that exist in the total line length.) Thus, the graph shows that the total number of squares in the interconnect lines for the condition of higher device density has increased by a factor of 100. The *absolute* total line length is therefore $100B(w/\sqrt{10})$. The area of the chip covered by the metal lines for the higher logic device density will then be:

$$100\,B\left(\frac{w}{\sqrt{10}}\right)\left(\frac{w}{\sqrt{10}}\right) = 10\,Bw^2 \qquad (4-3)$$

This illustrates that as the active-device density is increased by a factor of 10, *the area of the chip covered by the metal also increases by a factor of 10.* As a result, a condition is soon reached in which the metal must occupy more area than that occupied by the active devices, and the chip area becomes interconnect limited. Keyes cites the example of a bipolar chip with a gate count of 1500 gates, and a chip area of 0.29 cm^2, fabricated

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using a single-level metal with a pitch of 6.5 μm.[1] The total wiring area occupied by the metal is 0.26 cm^2, which is about 90% of the surface area of the chip.

4.2.1.2 Propagation Delay. As the minimum line width on an IC shrinks, the active-device density increases. For example, in 256-kbit DRAMs 2-μm lines are used, while in 1-Mbit, 4-Mbit, and 16-Mbit DRAMs, 1.2-μm, 0.8-μm, and 0.5-μm lines are used, respectively. At these dimensions, the MOS transistor switching speed itself no longer limits the logic delay or access time of the IC. Instead, the time required for the transistor to charge capacitive loads becomes the limit to the performance of the IC. That is, as the devices shrink, the device contribution to the propagation delay of a digital signal also decreases. On the other hand, the scaling of the interconnect line widths does not bring about a corresponding decrease in the propagation delay time through the interconnect lines. As the chip sizes increase, the interconnect-path lengths also increase, and in fact most large VLSI circuits have become interconnect propagation-delay-time limited.

For example, as pointed out by Sah,[2] the intrinsic gate delay caused by electrons drifting through a 2-μm channel at their phonon-scattering-limited velocity of 10^7 cm/sec is 20 ps,[3] while the delay of of a 256-kbit DRAM is ~100 ns. This is 5,000 times longer than the intrinsic gate delay. Thus, a chip with devices whose gate lengths are 2 μm or less cannot be limited by the intrinsic gate delay unless 5,000 devices are connected in series. This is certainly not the case in a memory chip, and it is highly unlikely that it would occur even in complex logic circuits.

The propagation delay exhibited by VLSI circuits is therefore almost always limited by the large RC delay of the interconnection lines. The delay resulting from various

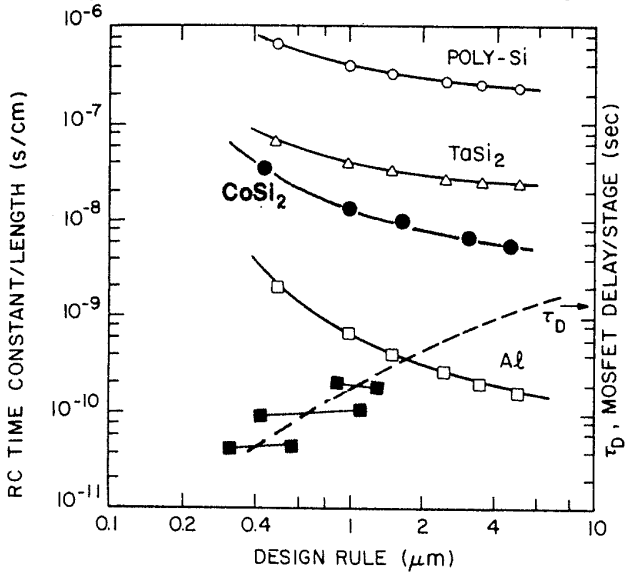

Fig. 4-4 RC time constant per unit length for several conductive materials as a function of feature size. Also shown is delay per stage of NMOS ring oscillators as a function of feature size. The RC time constant is calculated assuming a field oxide thickness of 1 μm.[258] Copyright 1981 AIOP. Reprinted with permission.

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interconnect materials per millimeter of length is given in Table 4-1, and is graphed for some of these materials (assuming a 1-cm-long interconnect line) in Fig. 4-4.* For example, if a polysilicon line having a 20 Ω/sq sheet resistance is used to connect one corner of a 0.7-x-0.7 cm chip to the diagonal corner, the data from Table 4-1 predict that the propagation delay will be 1.4 μs. Even if Al is used as the interconnect layer, the delay caused by 1-cm-long interconnection lines will limit the circuit speeds once device dimensions fall below ~2 μm.

The above indicates that in order for circuit performance to be increased as device dimensions shrink, two goals must be met. First, the materials used for transmitting signals over long distances on a chip must have the lowest possible resistance values. This has been the key motivation in the drive to replace polysilicon interconnects (20 Ω/sq) with polycide interconnects (1.7 Ω/sq for $TiSi_2$). It may eventually cause refractory metals (0.5 Ω/sq for W) to be used as the first-level interconnect layer in multilevel-interconnect systems. In addition, it also points outs why Al will continue to be used as an interconnect material, even as devices shrink further.

Second, the length of interconnect lines on a chip must be made as short as possible. The RC delay can be shown to be proportional to the *square* of the length of the interconnect line. That is,

$$R = (\rho\, l)/(w\ t_m) \qquad (4\text{-}4)$$

and

$$C = \varepsilon\, w\, l / t_{ox}, \qquad (4\text{-}5)$$

and therefore

$$RC = \frac{\rho\, \varepsilon l^2}{t_m\, t_{ox}} \qquad (4\text{-}6)$$

where ρ is the resistivity, l is the interconnect line length, w is the line width, ε is the permittivity, t_m is the thickness of the metal, and t_{ox} is the thickness of the oxide. A multilevel-interconnect structure is an effective way to allow the longest lines to be reduced in length.

There are several other propagation-delay-related considerations that make multilevel interconnects attractive. First, they make it more feasible to lay out all interconnect lines with as close to the average length as possible. This is important because if some lines are much longer than the rest, the overall delay time of the circuit will be increased. The length variation also introduces nonuniform on-chip RC response times, which can disturb the switch synchronization of the circuit.

Figure 4-5a shows a histogram of the line lengths of a typical single-level-metal IC.[4] Whereas most lines are short, a few are much longer (e.g., in this example ~6% of them are >7 mm long). Multilevel interconnects can help eliminate the incidence of the few long lines.

Second, as shown by McGreivy in Fig. 4-5b,[5] if the line spaces become smaller than ~0.6 μm the total parasitic capacitance of the interconnect lines will increase, because

* Note that in Fig. 4-4 a somewhat thicker field oxide is used, yielding a smaller value of C.

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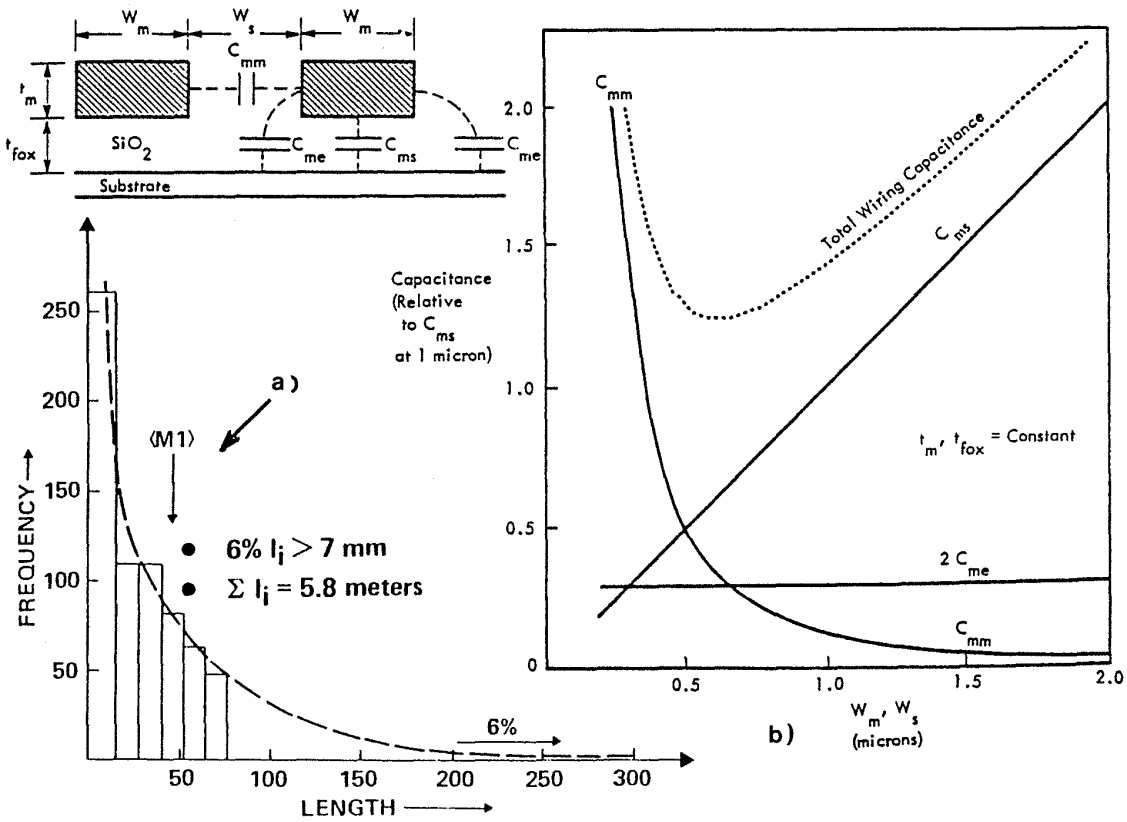

Fig. 4-5 (a) Example of lead length distribution of metal interconnects on an IC having a single level of metal.[4] Reprinted with permission of Electronics. (b) Variation of components of interconnect capacitance with design rules. The various components are defined in the adjacent figure.[5] (© 1982 IEEE).

the side-by-side capacitance increases with decreasing line pitch. The end result is an overall increase in the system cycle time. Again, the use of a multilevel-metal interconnect system, in which the wires run orthogonally in adjacent layers can reduce this problem.

Third, the layout should minimize cross-talk in order to reduce the level of inductance noise coming from the random switching of individual circuits. This goal can be accomplished through the use of a multilevel-interconnect structure in which all the wire tracks on one level run in one direction, while those on the adjacent level run in the perpendicular direction.

Finally, because the functional density of the chips can be increased, less chip-to-chip signal transmission is required. Since such off-chip driving is much slower than on-chip signal transmission, the overall system speed will be enhanced.

The above discussion implies that the lower levels of metal or polysilicon (which generally have a finer pitch, and therefore higher resistance and capacitance) should be reserved for interconnecting neighboring devices with short interconnection lines. The

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Table 4.1 Interconnection Delay in Silicon VLSI Chips[1]

Conductor Materials	Resistivity ($\mu\Omega$-cm)	Thickness (nm)	Sheet Resistance (Ω/square)	Delay (psec/mm^2)
Polysilicon	1,000	500	20	7,000
$TaSi_2$	46	100	4.6	1,587
Ti	42.7	100	4.3	1,484
PdSi	32	100	3.2	1,104
$MoSi_2$	22	100	2.2	759
$TiSi_2$	17	100	1.7	586
Ta	13.1	100	1.3	448
WSi_2	12.5	100	1.3	448
Pd	10.5	100	1.1	380
W	5.3	100	0.53	183
Mo	5.3	100	0.53	183
Al	2.6	100	0.26	90

upper interconnect levels, which are usually designed with a larger pitch and lower resistance, should be used to transmit signals across the entire chip.

4.2.1.3 Ease of Design and Gate Utilization for ASICs and Wafer-Scale Integration. In VLSI manufacturing, an interrelationship exists between the design and processing tasks, particularly when gate-array and standard-cell circuits are being produced. Such *application-specific ICs* (ASICs) are widely used because they allow new circuits to be quickly designed and rapidly fabricated. Gate-array wafers can be processed up to the metallization layers and then stockpiled. Users can implement their circuit designs by interconnecting the uncommitted logic gates through the use of custom metal masks. The design effort of interconnecting the uncommitted logic gates, however, must be minimal, and it should be possible to utilize a large fraction (if not all) of the gates in the uncommitted array.

Multilevel-interconnect technology allows both of these goals to be achieved much more easily. For example, a two- to fourfold decrease in design time was realized when a bipolar gate array was implemented with a three-level-metal process rather than with a two-level technology.[6] In another example, the ratio of the chip area required for power buses as a function of the number of gates in a gate array is plotted for two-level-metal and three-level-metal processes (Fig. 4-6).[7] The extra level of metal significantly decreases the area of the chip that must be used for the power buses. Hence, this area can be used to interconnect the devices – which reduces the difficulty of the design task.

Wafer-scale integration is a another concept in which a large number of chips from a single wafer are interconnected to create large digital systems without the chips being separated and mounted in separate packages. Since good die are interconnected after

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having been fabricated and tested, a multilevel-interconnection technology is essential for implementing this approach.

4.2.1.4 Cost. If multilevel-interconnect processes are used to fabricate integrated circuits, the die size should decrease. Thus, more die per wafer can be manufactured. If the manufacturing cost per wafer remains the same and the yield is not impacted by the implementation of a multilevel-interconnect process, the cost per chip will decrease. In fact, smaller die sizes should imply higher yields, and enhancing the benefit of chip-size reduction. In addition, improved device performance may allow the circuit to command a higher market price.

However, the implementation of a multilevel-interconnect system requires that at least two additional masking steps be used for each additional level of interconnect. The extra process steps add to the manufacturing cost of each wafer, and the number of defects/cm^2 is also generally proportional to the number of masking steps. In addition, the manufacturing yield and long-term reliability for a multilevel metal process are typically lower, since the process becomes more technically demanding. As a result, it must be determined whether the chip-size reduction and enhanced chip value will produce a margin of profit that is greater than the amount lost due to additional incurred process costs and yield and reliability loss.

4.2.2 Problems Associated with Multimetal-Interconnect Processes

As alluded to in the previous section, adding a multilevel interconnect process to a fabrication sequence introduces a new set of difficulties. In addition to added process

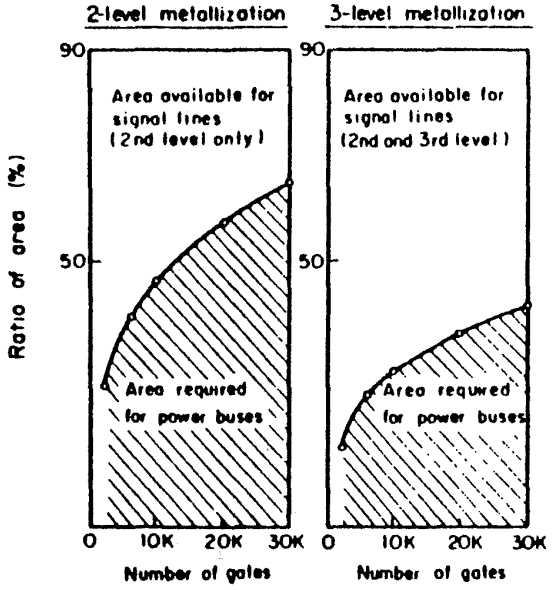

Fig. 4-6 Ratio of area required for power buses to the total chip area for ICs using two- and three-level-metal interconnect technologies.[7] (© 1983 IEEE).

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complexity and loss of topological planarity, there are several other concerns.

First, new materials must be used, which necessarily involves an extensive characterization of their properties to ensure that they are compatible with all other aspects of the process technology.

Second, new process-related manufacturing difficulties may be encountered that can adversely impact manufacturing yield (e.g., interlevel shorts due to pinholes; stringers due to incomplete etching over severe steps; failure to open vias due to difficulty in implementing reliable endpoint-detection techniques in the dry-etch process; film delamination due to poor adhesion or high stress; and difficulty in bonding to some metal alloys).

Third, new failure modes may be encountered – for example, electromigration, corrosion, and hillock formation – and these must also characterized to determine whether they will significantly compromise circuit reliability.

The problems related to multilevel interconnects is listed at this point in order to show that the benefits can be gained only by successfully pursuing a considerable technical-development effort. More specific details on these problems (and on how they can be overcome) will be provided throughout the chapter. Section 4.7 also gives an overview of the yield and reliability problems that occur when multilevel-interconnect technologies are implemented.

4.2.3 Terminology of Multilevel-Interconnect Structures

Figure 4-7 shows the terminology associated with a double-level-metal structure for MOS technologies. The MOS structure has a dielectric layer between the polysilicon gate/interconnect level and Metal 1, which we refer to as the *polysilicon/Metal 1*

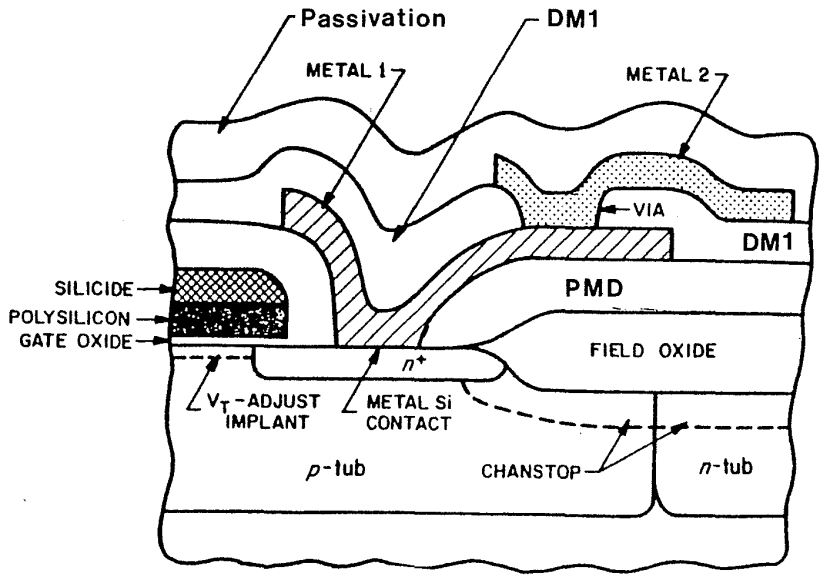

Fig. 4-7 Terminology of double-level-metal interconnects.

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dielectric (or PMD). The dielectric layers between metal levels are called *intermetal dielectrics*. The intermetal dielectric between Metal 1 and Metal 2 is designated as DM1, and dielectric layers between other levels of metal (e.g., Metals 2 and 3, or Metals 3 and 4) are DM2, DM3, etc. The openings in PMD are referred to as *contact holes*. Contact through them is established between Metal 1 and polysilicon, as well as between Metal 1 and the Si substrate. Openings in the intermetal dielectric layers are known as *vias:* these allow contact to be made between Metals 1 and 2, Metals 2 and 3, etc.

In bipolar technology, the dielectric layer between Metal 1 and the substrate is still referred to as PMD, despite the fact that it may not isolate Metal 1 from polysilicon. The openings in PMD are again called contact holes, although they are only used to allow contact to be established between Metal 1 and the substrate (i.e., not poly). The notation for the other metal and dielectric layers is otherwise identical to that used in MOS technologies.

A distinction exists between our use of the terms *multi-level* and *multilayer*. A *multilayer-interconnect structure* is a thin film consisting of more than one layer of material, but existing at just one level of the interconnect system. Hence, a multilayer film can serve as the conductor (or dielectric) at each level of a multilevel-interconnect system.

4.3 MATERIALS FOR MULTILEVEL INTERCONNECT TECHNOLOGIES

The two groups of materials employed in multilevel-interconnect technologies are *thin-film conductors* and *thin-film insulators*. In this section we will describe the properties of such materials that have been adopted for use in VLSI applications.

4.3.1 Conductor Materials for Multilevel Interconnects

4.3.1.1 Requirements of VLSI Conductor Materials. Before describing properties of the specific conductor materials that have been considered for VLSI interconnect technologies, it's useful to examine the general requirements needed by such conductors. The most important of these are listed in Table 4-2. The list is long and many of the requirements are quite stringent. Nevertheless, unless a conductor structure can satisfy virtually satisfy all of them, it is unlikely to find use in VLSI applications. As a result, the number of materials that have been found suitable for VLSI interconnects is rather small. Table 4-3 summarizes the important properties of this group. The resistivities given in the table are typical for polycrystalline films with thicknesses of 10 - 1000 nm. The lower-resistivity values are exhibited by films that are purer and thicker, and that are large-grained. Deviations from stoichiometry for alloy conductors usually also lead to increased resistivity. As a result, the resistivity of a given type of film may vary from one deposition run to another, unless all deposition parameters are controlled to yield identical films.

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Another of the key properties of VLSI thin-film conductors is their ability to adhere to Si and to SiO_2. In this respect, Al, Ti, Ti:W, and TiN films are the best. Al and Ti reduce SiO_2 to form interfacial metal-oxide bonds that promote adhesion and stability. WSi_2, $MoSi_2$, and $TiSi_2$ also adhere well to SiO_2, but not as well as Al and Ti. On the other hand, W and Mo do not reduce SiO_2, and therefore they exhibit poor adhesion to SiO_2 surfaces. As a result, W and Mo are not used as stand-alone conductor materials. Instead, a layer such as Ti, Ti:W, or TiN_x is required under W or Mo films to promote adequate adhesion to Si and SiO_2.

Table 4.2 Desired Properties of Conductor Structures for VLSI

a. Low resistivity (has to be < 4 $\mu\Omega$-cm).
b. Surface smoothness (and hillock resistant).
c. Resistance to electromigration failure effects.
d. Bondable (final level of a multilevel system).
e. Adhesion to underlying substrate materials must be excellent.
f. Stable - the mechanical and electrical properties, remain constant with time under the following conditions:
   1. throughout processing, including sintering, interlevel, and passivation dielectric deposition;
   2. in an oxidizing ambient;
   3. under normal operating conditions; and
   4. under ordinary storage (stress voids).
g. Corrosion resistant.
h. Should not contaminate devices, wafers, or processing equipment.
i. Depositable to controlled thickness and uniformity, and free of deposited particulates.
j. Anisotropically etchable with high selectivity with respect to substrate and mask material (see Vol. 1, chaps. 15 and 16).
k. Depositable over vertical walls with conformal coverage of steps ("good step coverage").
l. Film reflectance should be controllable to allow effective photolithographic processing.
m. If necessary, the metallization film should be depositable as a combination metal film (multilayer) (see Vol. 1, chap. 10).
n. Each required layer should be depositable in alloy form, with alloy composition tightly controllable (see Vol. 1, chap. 10).
o. Depositable pure -- i.e., without reaction with the gases present in the deposition chamber, and without incorporation of residual gases into the deposited films) (see Vol. 1, chap. 10).
p. Low film stresses.
q. Deposition and patterning processing i. should be economically viable, through:
   1. high throughput;
   2. reasonable processing-equipment purchase, maintenance, and operating costs;
   3. high reliability and up time of processing equipment;
   4. low enough in complexity that highly skilled operators not required.

4.3.1.2 Local-Interconnect Conductor Materials (Polysilicon, Metal Silicides, and Polycides). The *local-interconnection level* is defined in chapter 3, section 3.11.2; various schemes to implement local interconnects are also described there. Polysilicon and polycides (i.e., structures in which a refractory-metal layer is formed on top of a polysilicon layer) have been used as local interconnect

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structures in NMOS technologies. (More information on the properties, formation, and patterning of polysilicon and polycides can be found in Vol. 1, chaps. 6 and 11, respectively.)

Various conductors have been proposed as local interconnect materials in CMOS technologies, including: dual-doped polysilicon, $TiSi_2$, Ti:W, TiN, and CVD W. Information on the characteristics of CMOS local interconnect materials is presented in chapter 3, section 3.11.2, as well as elsewhere in this volume.

4.3.1.3 Aluminum Metallization. Patterned aluminum thin films have been the most widely used interconnect structures in the manufacture of silicon ICs. As described in detail in chapter 3 of this volume and in Volume 1, chapter 10, the main reasons for the pervasiveness of Al are its low resistivity (2.7 $\mu\Omega$-cm) and its good adhesion to SiO_2 and Si. In addition, Al is generally used as the top level of metal in multilevel-metal systems because wire-bonding technology to Al thin films is a well-characterized process.

The main limitations of Al are its low melting temperature (660°C) and its low eutectic temperature with Si (577°C). In addition, Al thin films begin to form hillocks at relatively low processing temperatures (i.e., above 300°C), and they offer relatively poor resistance to electromigration effects and corrosion. (The electromigration and hillock problems are described in more detail in section 4.7.) The problems that arise when Al contacts are made to Si (i.e., related to the eutectic temperature of Al and Si) are considered in chapter 3, section 3.4.3.

Attempts to alleviate the above problems have generally involved the addition of alloy materials to Al or the formation of multilayer-Al conductor structures. The addition of Si to Al was discussed in chapter 3, section 3.4.3 as a technique for preventing junction spiking in Al contacts to Si. Electromigration and hillock resistance have been improved through the addition of such elements as Cu, Ti, Pd and Si to Al to form alloys. Another approach to overcoming the latter problems has involved the fabrication of multilayer-metal structures consisting of Al and other metal layers, such as the following: (1) Ti, Cr, and Ta layers sandwiched between Al layers; (2) Ti:W layers deposited below or on top of the Al film; and (3) W selectively deposited over the top and sidewalls of patterned Al lines. Such multilayer structures are also described in section 4.7. The addition of other metals to form Al alloys, however, generally degrades one or more of the Al characteristics (e.g., resistivity, corrosion resistance, etchability, or bondability).

Thin films of Al for VLSI interconnects are commonly deposited by dc magnetron sputtering (see Vol. 1, chap. 10). Although evaporation of Al films was carried out in the early days of IC fabrication, the need for Al-alloy films with tightly controlled alloy composition was the primary reason for the displacement of evaporation by sputtering. Sputtering generally allows more control over the alloy composition than evaporation (see Vol. 1, chap. 10). Some recent advances in sputter deposition are reviewed in reference 8. Research is also being conducted on CVD Al, as described in section 4.5.5.2.

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4.3.1.4 Tungsten and Other Conductor Materials for VLSI Interconnects. Tungsten has been intensively investigated for a number of roles in multilevel-interconnect systems for the following reasons:

- It exhibits excellent resistance to electromigration effects, hillock formation, and humidity-induced corrosion.
- It can be deposited by means of CVD, and thus allows much better step coverage than can be obtained by sputter-deposited or evaporated films (e.g., Al films).
- The use of selective CVD allows W to fill contact holes and vias that have very high aspect ratios, and it also allows W to be selectively deposited onto patterned Al lines.
- Finally, CVD W allows unframed vias and contact holes to be implemented, thereby increasing circuit packing density.

The main disadvantages of CVD W compared to Al are its higher resistivity (6-15 $\mu\Omega$-cm), its rough surface after deposition, and the difficulties involved with etching it. The details of CVD-W deposition, which involves planarization of W conductor structures and the filling of contact holes and vias with W, will be described in section 4.5.4. The issues involved with W etching will be considered at this point.

The etching of CVD W presents several problems. First, the surfaces of most CVD W films are very rough (usually 25% or more of the film thickness in the hydrogen reduction process – but much improved via SiH_4 reduction). Second, W and SiO_2 both form volatile fluoride by-products. Thus, it is difficult to obtain high selectivity with respect to the underlying oxides if a fluorine-based chemistry is used for dry-etching W. Such selectivity is necessary during the overetch time that must be used to clear away any stringers of W that remain at steps on the wafer surface (see Vol. 1, chap. 15). On the other hand, when chlorine chemistries (which allow higher selectivity to the oxide, and are therefore most commonly used to etch W) are employed, the erosion rate of photoresist is very high. As a result, an inorganic mask or a composite resist/SiO_2 mask has usually been used when W is dry etched.[110, 111] Such approaches, however, represent an undesirable process complexity.

One approach that allows a resist mask to be utilized makes use of a two-step etch process.[113] In the first step, a high-power RIE mode is used to rapidly etch 0.8 μm of a 1.0-μm-thick W film. A gas mixture of SF_6, HBr, and CH_4 is employed for this step. A selectivity to the resist of 4:1 is obtained by using this gas mixture together with a thermal UV treatment of the resist mask prior to etching. The second step uses a low-power rf mode, coupled with a remote microwave plasma to etch the remaining W. A gas mixture of SF_6, HBr, and CCl_4 is used, and selectivity of 4:1 to the oxide is obtained.

Interconnect films using sputter-deposited Mo (together with an underlayer of Ti:W or Ti) have also been implemented as the Metal 1 layer of a multilevel-interconnect system.[114] The Mo offers the advantages of excellent electromigration and hillock resistance. More information on this conductor structure is found in chapter 3, section 3.6.3.

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Interconnect films using Au were used in some early-generation integrated circuit technologies. Au offers low resistivity (2.2 $\mu\Omega$-cm), resistance against corrosion, and good electromigration properties. However, it does not adhere well to SiO_2, and it is "poison" to devices (i.e., it causes deep-level traps in the forbidden gap, degrading the minority carrier lifetime). These drawbacks make the fabrication of Au metallization systems quite complex, and hence Au has not found much use in VLSI applications. However, reference 9 describes an example of a recent two-level gold metallization process that uses Ti:W as a diffusion barrier and adhesion layer under the Au, and in which the Au is deposited by electroless plating.

Copper thin films offer even lower resistivity (1.7 $\mu\Omega$-cm) than Au films, and they are also expected to show good electromigration resistance. They would thus appear to be attractive as VLSI conductor materials, especially as device dimensions approach deep-submicron sizes. A dry-etching process for Cu films has not been successfully developed (see Vol. 1, chap. 16), however, and this is one of the chief reasons that Cu has not been widely considered for such applications.

A low-temperature Cu-deposition process that exhibits good adhesion to SiO_2 is given in reference 10. Since the presence of Cu in the Si also poisons devices, it would be necessary to prevent Cu migration into the Si substrate through the use of diffusion barriers. Such barriers are described in reference 99. A recent report on using Cu interconnects for ICs with device dimensions smaller than 0.5 μm is given in reference 233. Possible approaches to overcoming the problems of deposition, etching, device contamination, and corrosion associated with Cu interconnects are discussed. The

Table 4.3 Properties of Various Thin-Film Conductors Used in VLSI Multilevel Interconnects

Metal or Alloy	ρ ($\mu\Omega$-cm)	Melting Point (°C)	Reaction with Si (°C)	Stable on Si up to (°C)
Al	2.7-3.0	660	~250	~250
Mo	6-15	2,620	400-700	~400
W	6-15	3,410	600-700	~600
$MoSi_2$	40-100	1,980	-	≤1,000
$TaSi_2$	38-50	~2,200	-	≤1,000
$TiSi_2$	13-16	1,540	-	≤ 900
WSi_2	30-70	2,165	-	≤1,000
$CoSi_2$	10-18	1,326	-	≤950
PtSi	28-35	1,229	-	≤750
Ti:W (10 wt% Ti)	75-200	-	600-700	~700
TiN	25-200	~2880		

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etching problem to be circumvented by selectively depositing the Cu; device contamination can be controlled by utilizing silicon nitride under the Cu lines; and corrosion can be stopped by selectively covering the Cu lines with a layer of nickel.

4.3.2 Dielectric Materials for Multilevel Interconnects

4.3.2.1 Requirements of Dielectric Layers in Multilevel Interconnects. Dielectric layers must be used to electrically isolate one level of conductor from another in multilevel-interconnect systems. The list of properties that must be possessed by such dielectric layers is given in Table 4-4. As is the case for conductor materials used in such applications, the list of requirements is long and stringent. When we describe the materials that have been developed for this role, Table 4-4 will serve as our point of reference.

It should also be mentioned that there can be a significant difference between the dielectric film referred to in Fig. 4-7 as PMD (used between polysilicon, or other local-interconnect level material, and Metal 1) and the dielectric films that are employed between the metal layers (*intermetal dielectrics* – e.g., DM1 in Fig. 4-7). PMD films can be deposited (and densified if necessary) at a higher temperature than is possible for the intermetal dielectric layers. Furthermore, PMD films can be *flowed* and *reflowed* at temperatures in excess of 800°C. On the other hand, when Al is present on the wafer surface, the maximum temperature of the intermetal dielectric layers is limited to ~450°C. We will therefore discuss these two dielectric types separately, even though some dielectric films can be used for both applications.

4.3.2.2 Poly-Metal Interlevel Dielectric (PMD) Materials. Doped CVD SiO_2 films have found the widest application as PMD layers in MOS ICs. Silicon-nitride films have generally not been used as stand-alone PMD layers because they possess a much higher dielectric constant than SiO_2 films and because they cannot be flowed or reflowed. High-temperature CVD-oxide films (deposited at 900°C by the reaction of dichlorosilane and nitrous oxide) were among the first materials used for this purpose. Such films provide excellent step coverage, as well as dielectric properties almost identical to those of thermally grown SiO_2 films (see Vol. 1, chap. 6). Unfortunately, these films cannot be doped because of the high temperature at which they are deposited; as a result, they cannot be flowed or reflowed at temperatures lower than 1100°C.

Undoped TEOS films (deposited by the decomposition of *tetraethyl orthosilicate*, [TEOS] at 600-650°C) were also used as PMD layers in some early IC processes because of their excellent step coverage. In order to allow such TEOS films to be reflowed, phosphorus- and boron-doped TEOS deposition processes were subsequently developed. Recent efforts with doped-TEOS processes have been aimed at replacing the relatively toxic phosphine and diborane dopant gases with less toxic liquid sources.[12] In addition, PECVD TEOS processes have recently been developed in which TEOS films can be deposited at lower temperatures (e.g., 375°C; see section 4.3.2.4).

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Table 4.4 Desired Properties of Interlevel Dielectrics for VLSI[11]

1. Low *dielectric constant* for frequencies up to ~20 MHz, in order to keep capacitance between metal lines low.
2. High breakdown field strength (>5 MV/cm).
3. Low leakage, even under electric fields close to the breakdown field strength. Bulk resistivity should exceed 10^{15} Ω-cm.
4. Low surface conductance. Surface resistivity should be $>10^{15}$.
5. No moisture absorption or permeability to moisture should occur.
6. The films should exhibit low stress, and the preferred stress is compressive (~$5x10^8$ dynes/cm^2), since dielectric films under tensile stress exhibit more of a tendency to crack.
7. Good adhesion to aluminum, and of aluminum to the dielectric. (Good adhesion is also needed to the other conductors used in VLSI, such as doped polysilicon and silicides). In cases of poor adhesion (such as with gold or CVD W), a glue layer (such as Ti or Ti:W) may need to be applied between the conductor and the dielectric.
8. Good adhesion to *dielectric layers* above or below. Such dielectric layers could be thermal oxides, doped-CVD oxides, nitrides, oxynitrides, polyimides, or spin-on glasses.
9. Stable up to temperatures of 500°C.
10. Easily etched (by wet or dry processing).
11. Permeable to hydrogen. This is important for IC processing, in which an anneal in a hydrogen containing ambient must be used to reduce the concentration of interface states between Si and the gate oxides of MOS devices (see Vol. 1, chap. 8).
12. No incorporated electrical charge or dipoles. Some polyimides in particular contain polar molecules that can orient themselves in an electric field and give rise to an electric field even when the externally applied field is removed.
13. Contains no metallic impurities.
14. Step coverage that does not produce reentrant angles.
15. Good thickness uniformity across the wafer, and from wafer to wafer.
16. In the case of doped oxides, good dopant uniformity across the wafer, and from wafer to wafer.
17. Low defect density (pinholes and particles).
18. Contains no residual constituents that outgas during later processing to the degree that they degrade the properties of other layers of the interconnect system (e.g., outgassing from some polyimide films, SOG films, or low-temperature TEOS films).

Silane-based phosphorus-doped SiO_2 films deposited at low temperatures (350-450°C) have also been used as PMD layers. The addition of phosphorus to the films allows reflow to be performed at ~1000°C in steam. However, the need for lower flow and reflow temperatures has made silane-based BPSG and boron/phosphorus-doped TEOS films more attractive.[13] Reflow temperatures of less than 850°C can be achieved with BPSG.

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Silane-based BPSG films (3-5 wt% each of B and P) are deposited at low temperatures (400-450°C) and are then immediately densified at ~800°C for one hour. The purpose of this step is to completely stabilize the BPSG films, which would otherwise be prone to blistering during subsequent processing. The higher the boron concentration in such films, the lower the flow temperature; however, BPSG films with high boron concentrations (i.e., greater than 5%) are not stable, and hence are not used.

A report has been made of a BPSG film with 4.8 wt% B and 4.6 wt% P that was flowed at 900°C for 30 minutes; this film exhibited a nearly planar surface over patterned polysilicon.[14] A two-layer film was actually used for the PMD – that is, a thin (120-nm-thick) silicon-nitride layer was deposited before the BPSG. The nitride prevents dopants from the BPSG from diffusing into the poly or substrate device regions during the flow and reflow thermal cycles. Note, however, that the temperature used to flow the film in this example may be too high for processes that employ shallow junctions or $TiSi_2$ self-aligned contact structures (as described in chap. 3, section 3.9.1.1).

The phosphorus content of the BPSG films can be measured easily and quickly by using energy-dispersive X-rays (see Vol. 1, chap. 17). The boron content is more difficult to measure, but two methods for doing this are *wavelength dispersive X-ray analysis* (see Vol. 1, chap. 17), and a wet-chemical technique known as *colorimetry* (see ref. 15).

4.3.2.3 CVD SiO_2 Films as Intermetal Dielectrics. Until recently, the materials most widely used for intermetal dielectrics have been doped, silane-based CVD SiO_2 films. There are two main reasons for the widespread adoption of such films for this application: first, CVD SiO_2 films with good electrical and physical properties can be deposited at temperatures compatible with the presence of Al on the wafer ($\leq$ 450°C); and second, when CVD SiO_2 is doped with phosphorus, it serves as an excellent gettering layer for sodium ions and other lifetime-killing metallic impurities.

Good-quality SiO_2 films for intermetal applications are characterized by the following measures:

- The P-etch rates are on the order of 30 nm/min (*P-etch* is a mixture of 300 parts H_2O, 10 parts HNO_3 [70%], and 15 parts HF [49%]).
- The index of refraction is 1.46 (this value increases with oxygen deficiency).
- The dielectric strength is 4×10^6 V/cm.
- There is an absence of nodular growths and pebble-like surface defects.
- The films are pinhole-free.
- Good edge coverage of underlying metal steps is provided.

Intermetal SiO_2 films can be deposited by means of a number of CVD processes, including *atmospheric CVD, low-pressure CVD, and plasma-enhanced CVD* (see Vol. 1, chap. 6). While the CVD SiO_2 films deposited by these methods can exhibit good

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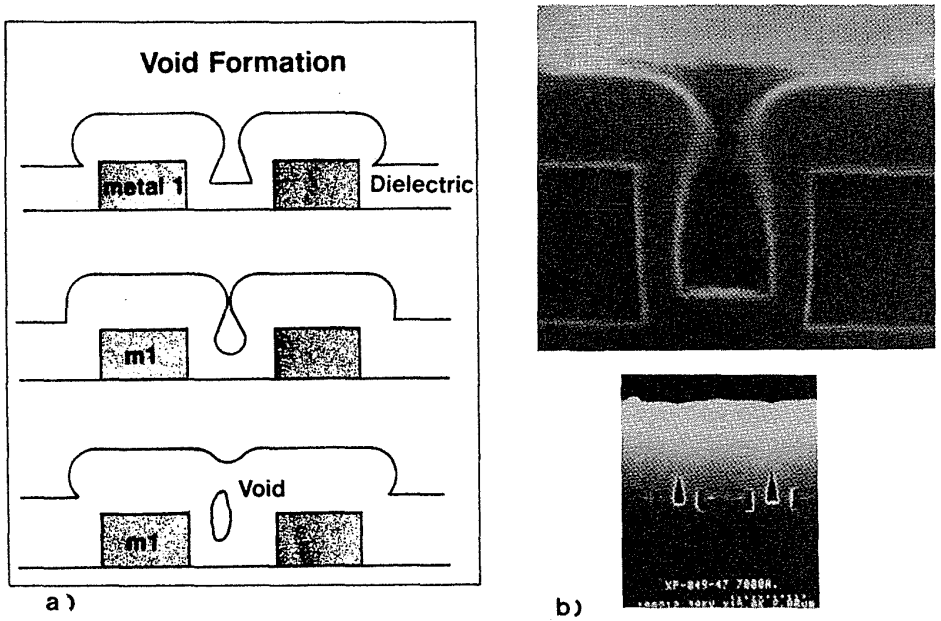

Fig. 4-8 (a) Diagram of void formation due to cusping of the dielectric. (b) SEM of voids left between 1.5-μm-spaced Metal 1 lines in a 3.0-μm-thick DM1 PECVD oxide.

electrical and physical properties, all silane-based CVD methods share a number of problems. First, coverage of these films over closely spaced steps is inadequate, primarily as a result of geometrical shadowing; as a result, the film thickness at the top of the step exceeds that on the bottom and sidewalls. In addition, the angle of the SiO_2 film at the base of the step can be *reentrant*, making step coverage and etching conditions more difficult. Related to this problem is the formation of voids when the thicker sidewalls of the oxide touch, leaving a void below (see Fig. 4-8).

The addition of phosphorus to silane-formed SiO_2 films (known as *phosphosilicate glass, PSG*, or *P glass*) helps to reduce stress in the SiO_2 films, makes them more resistant to moisture, and improves their gettering of sodium. However, it also increases the film etch rate. This can impact dielectric etchback planarization processes (see further sections 4.4.3 and 4.4.8). That is, if the incorporation of phosphorus is not uniform across the wafer (and from run to run), the etchback rate will not be uniform across the wafer. Such variations in etch rate can produce devices with very thin dielectric layers on some locations on a wafer.[16]

Phosphorus doping also degrades the step coverage of the CVD SiO_2 films by enhancing their cusping tendency. In addition, when PECVD SiO_2 is used to fill high-aspect-ratio spaces, a seam forms where the oxide sidewalls meet. This seam region may exhibit a much higher dry-etch rate than the bulk regions of the film. As a result, in an etchback planarization process, the faster-etching seam regions can cause the formation of deep grooves on the oxide surface.[16]

A third problem, gas-phase nucleation, is associated with silane-based plasma-enhanced CVD (PECVD) SiO_2 films. If the rf field becomes too strong, the dissociated

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gas molecules may react in the gas stream and form SiO_2 particles, which fall into the growing film.[17]

A PECVD borosilicate glass (BSG) has also been reported on as an intermetal dielectric material.[18] Its advantages include good-quality dielectric properties for deposition temperatures as low as 300°C, and a dry-etch rate higher than that of PSG, which makes it attractive for use in etchback SOG processes (see section 4.5.9). In addition, BSG provides excellent step coverage and can reportedly fill narrower spaces between metal lines than can silane-based PSG films.[11] Therefore, SiO_2 layers containing both B and P (to exploit the advantages that are obtained when each of these dopants is present in the film) should, in principle, produce intermetal-dielectric films with the best overall characteristics.

4.3.2.4 Low-Temperature-TEOS Films as Intermetal Dielectrics. Processes that allow both pyrolytic and plasma-enhanced deposition of SiO_2 from TEOS (PETEOS) at temperatures of 375°C (rather than from silane) have recently become commercially available.[16,19] Such low-temperature PETEOS oxides to some degree alleviate the problems of silane-based CVD SiO_2 films. First, the drawback of cusping is reduced in TEOS-based films, because when the oxide is deposited from organic silicon compounds, the adatoms have a higher surface mobility. The larger the mean free path for surface migration, the more local averaging of the local solid angle there is, improving step coverage and conformality. Second, this effect allows filling of spaces between adjacent lines with aspect ratios as high as 0.8, while silane-based PECVD SiO_2 films become ineffective when aspect ratios exceed 0.5. (PETEOS SiO_2 films showed no cusping, nor did etching in dilute HF delineate any seams when 0.8 aspect-ratio spaces were filled.) Third, the problem of non-uniform phosphorus incorporation (which might impact the etch rate) is alleviated, since the film does not include any phosphorus during deposition. Finally, the problem of gas-phase nucleation is eliminated, since TEOS is not *pyrophoric* (i.e., it will not spontaneously ignite in the presence of oxygen).

A report on the properties of boron-doped plasma CVD TEOS films for intermetal dielectric applications is given in reference 20. In another report, both the low-temperature pyrolytic TEOS film and the plasma-enhanced TEOS films were used, together with an etchback process, to produce a planar surface over topographies with steps ≤ 10 μm apart.[21]

Another PETEOS process that produces directional deposition (thus allowing void-free filling of high-aspect-ratio spaces) has recently been reported.[239] Step coverages with 80% bottom- to top-surface ratios and only 60% sidewall to top-surface ratios were observed on features with aspect ratios of ~1.0. Such directional deposition was observed in PETEOS films with low O_2:TEOS feed-gas ratios. The novel step coverage is attributed to the directionally impinging ions which induce anisotropic step coverage profiles and enhance the crosslinking in the formation of the silicate network.

An alternative source compound to TEOS or silane has also been investigated for low-temperature plasma-enhanced CVD SiO_2 film deposition. This compound is TMCTS (1,3,5,7-tetramethylcyclo-tetrasiloxane). It reportedly produces films of

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comparable quality to those of PECVD TEOS, but at a faster deposition rate. The addition of NF_3 to TEOS and TMCTS plasmas produces void-free filling of holes with aspect ratios as high as 1.0 (compared to void-free filling of holes with 0.7 aspect ratios when PECVD TEOS and TMCTS are used without NF_3).

4.3.2.5 Other Materials and Deposition Processes Used to Form Intermetal Dielectrics. In addition to doped CVD SiO_2 and low-temperature TEOS-based SiO_2 films, a variety of other materials have been implemented as intermetal dielectrics. These include PECVD silicon nitrides, bias-sputtered SiO_2, polyimides, and spin-on glasses. The PECVD nitrides have rarely been used as stand-alone inter-metal dielectric layers, because they posses a higher dielectric constant than CVD SiO_2 films. Instead, they are usually employed as one layer of a multilayer intermetal dielectric film; some examples will be given in later sections. The dielectric properties of bias-sputtered SiO_2 films, polyimide films, and SOG films will also be described in subsequent sections (4.4.5, 4.4.6, and 4.4.9, respectively). Research on other intermetal dielectric materials and alternative deposition processes for VLSI applications has also been reported, including photo-CVD,[22] laser activated CVD dielectric films,[23] CVD SiO_2 films deposited in a downstream afterglow reactor,[24] and evaporated Al_2O_3 layers.[25]

4.4 PLANARIZATION OF INTERLEVEL DIELECTRIC LAYERS

As pointed out in the introduction to this chapter, the planarization of interlevel dielectrics is one of the three critical issues that must be addressed when implementing a multilevel interconnect system for VLSI applications. We will now justify this assertion and describe the various approaches developed for dealing with this issue.

4.4.1 Terminology of Planarization in Multilevel Interconnects

As additional levels are added to multilevel-interconnection schemes and circuit features are scaled to submicron dimensions, the required degree of planarization is increased. Such planarization can be implemented in either the conductor or the dielectric layers. In this section we will consider processes developed to planarize dielectric layers; in later sections, techniques for planarizing conductor layers and vias will be considered.

The term *planarization* is employed quite frequently (and loosely) both here and in other technical literature. At this point, therefore, it is useful to define this term more carefully and completely, especially as it applies to the planarization of dielectric layers in multilevel-interconnect technology. The example case we will use for this discussion is that of a dielectric layer (DM1) that is deposited after Metal 1 is patterned. In the case where *no planarization exists* (Fig. 4-9a), the step heights on the DM1 surface closely approximate the step heights of the Metal 1 layer and the underlying topography.

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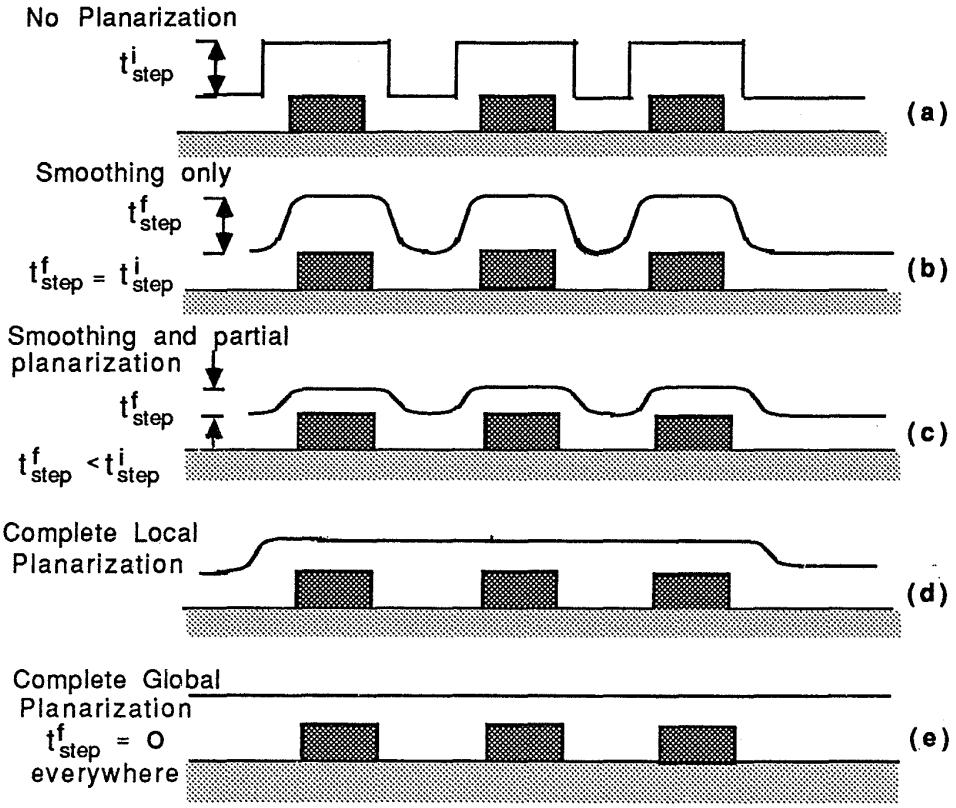

Fig. 4-9 Degrees of dielectric planarization

Furthermore, in this case the steps on the DM1 surface also have steep slopes (i.e., vertical, or even reentrant).

4.4.1.1 Degree of Planarization. The steps on the surface of DM1 can be made less severe through various planarization processes. The degree to which this can be successfully accomplished differs according to the planarization technique used. We classify the degree of planarization according to the following *qualitative planarization criteria*:

1. The first degree of planarization (*smoothing*) involves a lessening of the step slopes at the DM1 surface (Fig. 4-9b). The step heights in this case, however, are not significantly reduced in magnitude.
2. In the second degree of planarization (*partial* or *semi-planarization*) the step heights are reduced (but not eliminated), and the slopes of the steps are also smoothed (Fig. 4-9c).
3. In the third degree of planarization (*complete local planarization*), the steps at the surface of DM1 are completely eliminated wherever the spaces in the underlying topography are relatively close together (e.g., <10 μm apart), but the steps at isolated, wide features still exhibit a step (Fig. 4-9d).

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4. In the fourth degree of planarization (*complete global planarization*), the surface of DM1 is completely planarized over arbitrary topography (Fig. 4-9e).

A *quantitative measure* of the step-height reduction, referred to as the *planarization factor*, β, is given by[26]

$$\beta = 1 - (t^f_{step}/t^i_{step}) \qquad (4-7)$$

where t^i_{step} and t^f_{step} are the initial and final step heights, respectively. In complete-planarization cases, $\beta = 1$; if no planarization (or only smoothing) exists, then $\beta = 0$.

4.4.1.2 The Need for Dielectric Planarization. As the number of levels in an interconnect technology is increased, the stacking of additional layers on top of one another produces a more and more rugged topography. Let us consider, for example, a two-level metal, single-poly CMOS process. Assume that the step height of the semi-recessed field oxide is 0.3 μm, and the thicknesses of the poly and the first and second metals are 0.4, 0.5 and 1.0 μm, respectively. The maximum height of the steps on the wafer surface after each of these processes will correspondingly be 0.3, 0.7, 1.2, and 2.2 μm (Fig. 4-10). It is apparent that the surface of the wafer must be planarized

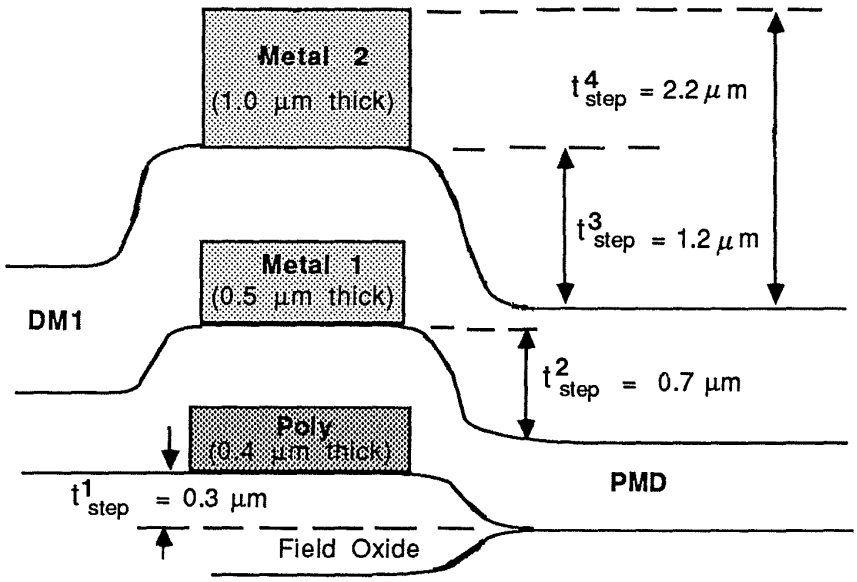

Fig. 4-10 As the number of levels in an interconnect technology is increased, the stacking of additional layers on top of one another produces steps of progressively greater heights.

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in some fashion to prevent the topography roughness from growing with each level. Without such planarization, the microscopic canyons that result on the wafer surface from stacking of device features can lead to topography conditions that would eventually reduce the yield of circuits to unacceptably small values.

A nonplanar wafer topography results in three conditions that prevent the fabrication of reliable electrical connections in multilevel interconnect systems. These conditions are as follows:

1. *Poor step coverage of the metal lines as they cross over the high and steep steps.* A measure of how well a film maintains its nominal thickness is expressed by the ratio of the minimum thickness of a film as it crosses a step, t_s, to the nominal thickness of the film on horizontal regions, t_n (Fig. 4-11a). This property is referred to as the *step coverage* of the film, and it is expressed as the percentage of the nominal thickness that occurs at the step:

$$\text{Step coverage (\%)} = (t_s/t_n) \times 100\% \qquad (4 - 8)$$

Step coverage of 100% is ideal for a conductor, but in general the height of the step and the aspect ratio of the features being covered impact the expected step coverage. (The *aspect ratio* is defined as the height-to-spacing ratio of two adjacent steps.) The greater the step height or the aspect ratio, the more difficult it is attain coverage of the step without a corresponding thinning of the film that overlies it (Fig. 4-11b shows an example of poor step coverage.). Hence, worse step coverage is expected under these conditions. In addition to the step height and aspect ratio, step coverage depends on two other topological factors: the *contour* and the *slope* of the step. In general, the smoother the steps contour and the less vertical its slope, the better will be the step coverage of any overlying films.

2. *Metal stringers remain behind at the foot or sides of a steep step when anisotropic etching is used.* This condition is shown in Fig. 4-11c (and see Vol. 1, chap. 15). In addition, the resist is typically eroded by the same gases that etch the metal. The resist must therefore be thick enough in all locations that it will not be completely removed before the etch process is completed. If the dielectric surface has steps, in certain locations (i.e., over the upper corners of the steps in the dielectric, see Fig. 4-11d) there may not be sufficient resist thickness to survive during the time of overetch that must be used for removal of the stringers. The resist-erosion rate during the overetch time is also generally enhanced: because most of the exposed metal has been etched away the reactant gases that were being consumed during etching of the metal are now present in greater concentrations. In cases where the resist is completely eroded at thin spots, the metal beneath the resist will be exposed to the etch gases and may be etched away to an unacceptable degree.

Even if the above two limitations could be overcome, the following obstacle would eventually force planarization to be implemented:

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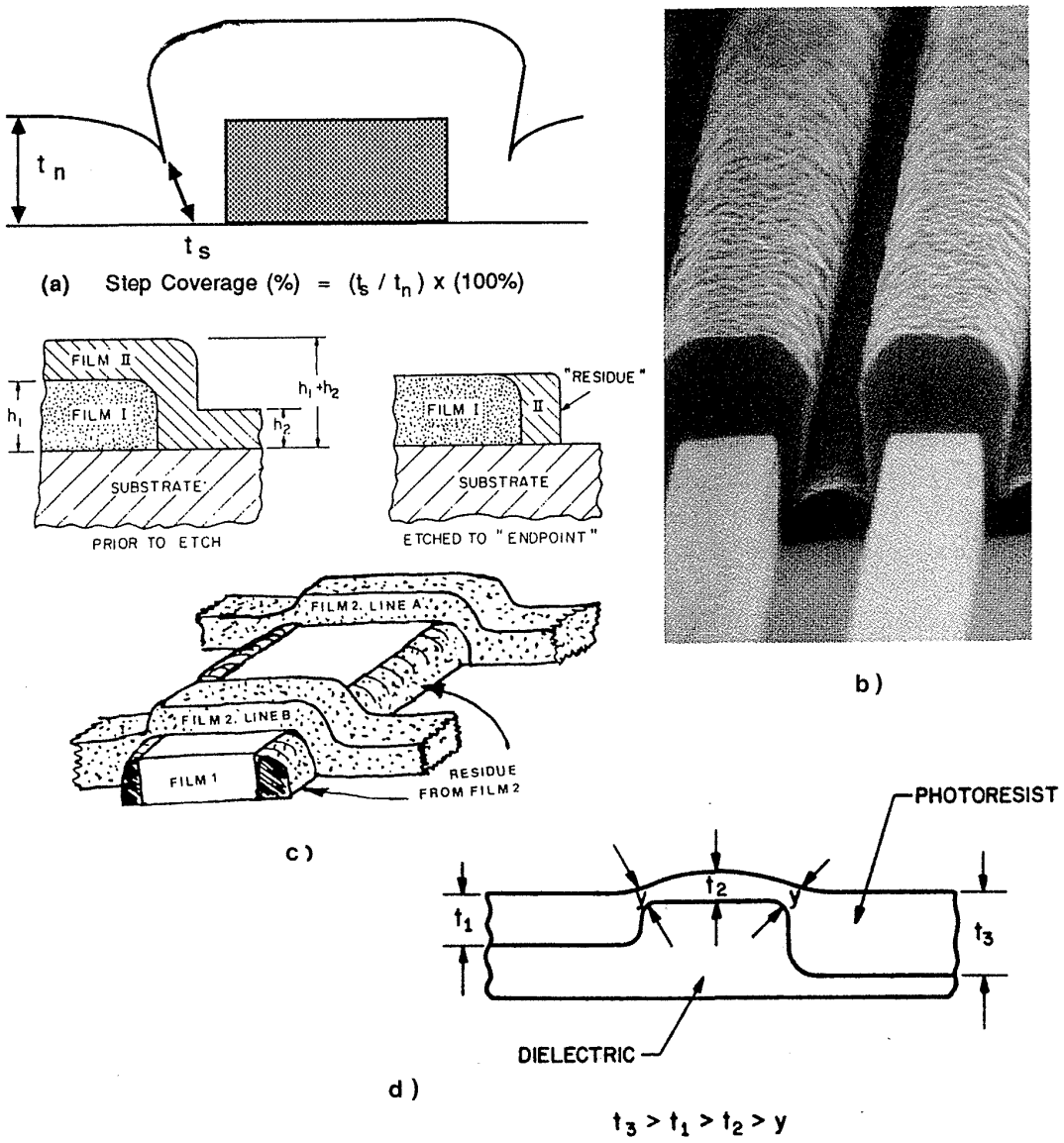

Fig. 4-11 (a) Definition of step coverage. (b) SEM micrograph showing poor step coverage. (c) Metal stringers remain behind at the foot or sides of a steep step when anisotropic etching is used. (d) Problem of resist thinning as film crosses underlying steps.

3. *The depth-of-field limitations of submicron optical-lithography tools will require surfaces to be planar within ±0.5 μm.* As a result, if steps larger than 0.5 μm exist on the surface of DM1 (or any other layer on the wafer), it will not be possible to pattern features in Metal 1 to the maximum resolution of the stepper. Thus, planarization will be mandatory if optical lithography is to be usable for fabricating ICs with submicron feature sizes. Note that this topic is discussed in more detail in chapter 2, section 2.9.2.

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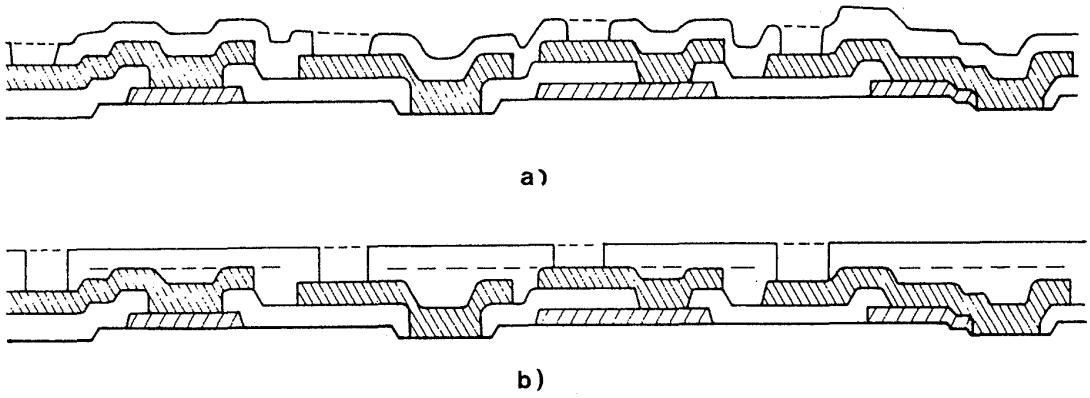

Fig. 4-12 (a) When no planarization is used, the via and contact holes between adjacent conductor levels all have approximately the same depth. (b) If planarization of the intermetal-dielectric layer, DM1, is achieved, the via depths can vary very widely in depth.

Planarization of the intermetal dielectric layers is one of the chief approaches that have been taken to alleviate the problem of rough surface topography.

4.4.1.3 The Price That Must Be Paid as the Degree of Dielectric Planarization Is Increased. In the sections that follow, we will describe a progression of planarization techniques, beginning with the smoothing of dielectric films, and going through complete global planarization. However, at least two significant penalties are encountered as the degree of planarization is increased, since the maximum variation in the thickness of the dielectric layer at different locations on the circuit will also increase. This is illustrated in Figs. 4-12a and b, in which the variations in the thickness of the dielectric in a nonplanarized topography are compared to the variations that occur in a fully planarized interconnect structure.

The first penalty associated with this effect is that the the dielectric layer may end up being too thin over some of the underlying conductors after the dielectric has been planarized (Fig. 4-12b). If this occurs, it may be necessary to deposit an additional dielectric layer to increase the thickness of DM1 before depositing Metal 2.

The second, and more serious, penalty involves the process of creating openings in the dielectric layers to allow selective contacting between conductors on different interconnect levels. As the degree of planarization is increased, such openings (referred to as *vias* when they are established in intermetal dielectric layers) will have different depths. For example, consider the two-level-metal structure shown in Fig. 4-13a. In this structure, the LOCOS field-oxide step is 200 nm, the polysilicon thickness is 400 nm, and the PMD layer thickness is 400 nm. It can be seen that if a completely planarized DM1 layer is used, via depths will vary from 0.3 to 1.3 μm. Such a large variation can lead to insurmountable via-filling problems.

If the technology for adequately covering vias with metal requires that the via sidewalls be sloped, an etch process for forming such sloped sidewalls will have to be

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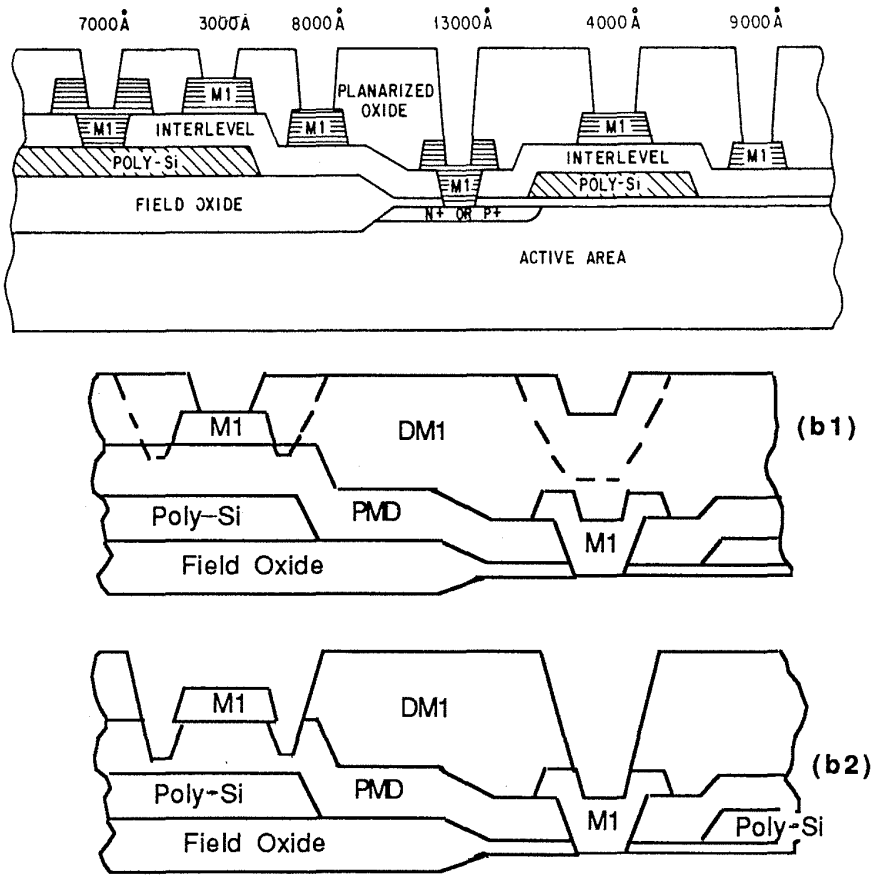

Fig. 4-13 (a) Example which shows how much the via depth can vary in a DLM process if full planarization is achieved.[259] (© 1986 IEEE). (b) If a sloped-sidewall etch is used to etch the vias shown in part (a), the dimensions of the shallow vias will continue to increase during the time needed to completely etch the deep vias. If the lateral dimensions of the shallow vias exceed the width of the Metal 1 pattern below these vias, the etch process will begin to erode the PMD layer (b2), even if a nested via is used.

used.* However, if the vias have significantly different depths, it may not be possible to implement a sloped-sidewall etch process. If a sloped-sidewall etch is used in the case shown in Fig. 4-12b, the dimensions of the shallow vias will continue to increase during the time needed to completely etch the deep vias. If the lateral dimensions of the

* Via sidewall sloping is usually needed when metal films are deposited by sputtering. In such cases, if the via sidewalls are too steep, metal step coverage becomes inadequate, and metal thinning (or even metal-film discontinuity) occurs. Therefore, it becomes necessary to slope the sidewalls as much as feasible.

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shallow vias exceed the width of the Metal 1 pattern below these vias, the etch process will begin to erode the PMD layer (Fig. 4-13b2), even if a nested via is used (see section 4.5).

In such cases, it may be necessary to avoid the use of a complete planarization process and to resort instead to a smoothing or semi-planarization procedure. With these methods it is possible to select a small enough maximum variation in via depths that a sloped-sidewall etch process can be successfully implemented.[27] In general, however, the smoothing and semi-planarization techniques lose their effectiveness when three or more levels of metal are required and when device dimensions are smaller than 1 μm. Here, the use of complete planarization processes becomes mandatory, and technologies must be employed that allow vertically sided contact holes and vias of varying depths to be completely filled. A variety of candidate approaches for satisfying this need are described in section 4.5.

4.4.1.4 Design Rules Related to Intermetal Dielectric-Formation and Planarization Processes. The type of intermetal dielectric material, its thickness, and the method of its deposition and planarization can all have an impact on the design rules that must be applied when laying out an integrated circuit with a particular multilevel-metal system. We will consider here a two-level-metal system with an underlying polysilicon level, and we'll assume that the topography beneath the polysilicon is completely planar. In this system, design rules dealing with the following conditions must be specified: (1) minimum polysilicon-to-Metal 1 spacing, assuming no metal overlap of the poly, (2) minimum distance between coincident edges when Metal 1 overlaps polysilicon, and (3) minimum spacing of Metal 1 to Metal 1.

If polysilicon and Metal 1 come too close together, a gap will exist between them that will lead either to void formation in the CVD oxide DM1 layer following deposition (Fig. 4-14a) or to the formation of a deep narrow crevice that cannot be covered by the next level of metal, even after some planarization procedures have been implemented (Fig. 4-14b).

In the second case, if polysilicon and metal edges are coincident, the total step height may be too high for adequate coverage by Metal 2 to be achieved (Fig. 4-14c). Figure 4-14d illustrates the case in which the problems of coincident edges and a narrow crevice are exacerbated by their simultaneous occurrence.

In the third case, the spacing between adjacent Metal 1 lines must be large enough to prevent void or crevice formation in the deposited dielectric film. The step that exists in the LOCOS field oxide must also be considered in real situations when such design rules are being formulated.

One possible way to prevent the formation of voids, crevices, and excessively high steps, is to allow the spacings between Metal 1 and underlying features to be sufficiently large that any possible combination of misalignment cannot lead to the problems listed. However, this alternative is impractical, because it increases chip size and causes excessive complexity in layout design.

The trend in advanced IC designs today is toward the elimination of all such restrictive dielectric-layer-related design rules, with the development focus on dielectric

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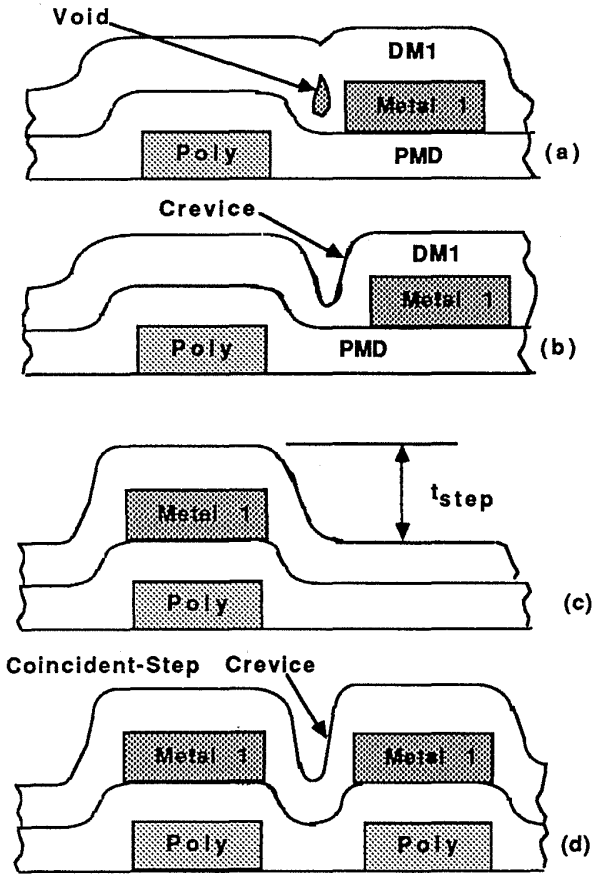

Fig. 4-14 Conditions associated with the relative spacing of polysilicon and Metal 1 that lead to layout design rules of these layers.

planarization processes that allow *all spaces between any adjacent or overlapping features (and all possible step heights), to be covered with a dielectric layer whose surface does not exhibit any voids, crevices, or excessively high steps.* Even though this is an actively pursued goal, it has not yet been attained in all processes and technologies. We will describe the various planarization approaches that have been developed along the path toward the condition in which no restrictive design rules need be invoked.

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4.4.2 Step-Height Reduction of Underlying Topography as a Technique to Alleviate the Need for Planarization

In two-level-metal processes, it may be possible to avoid having to perform *any* planarization procedures with respect to DM1 if the topography underlying DM1 is planarized by the process steps that precede DM1 deposition. Although this approach may appear to be obsolete for VLSI and ULSI circuits, several of the step-height reduction techniques also turn out to be useful for providing a planar surface under Metal 1. Such a condition will ultimately be required for three- and four-level-metal processes. We will therefore begin the survey of planarization techniques of dielectric layers by considering this approach.

4.4.2.1 Provide a Completely Planar Substrate Topography. The methods used to provide a completely planar substrate surface at the conclusion of isolation-structure formation in the substrate are described in chapter 2. In general, all of these methods rely on the formation of a fully-recessed field oxide layer in the substrate. The semirecessed LOCOS technology that has served MOS ICs for a number of generations, will ultimately have to be abandoned or modified in order for this goal to be achieved.

4.4.2.2 Provide a Planar Surface over Local-Interconnect Levels. Once a completely planar surface has been established following formation of the isolation structures, a polysilicon gate or emitter layer is fabricated. This layer can also serve as a *local-interconnect layer* (silicides and refractory metals have also been developed for this function). The oxide spacers that are formed at the edges of the polysilicon during the fabrication of lightly doped drain structures (see chap. 5, section 5.6.5) and salicides (see chap. 3, section 3.9.1) result in some smoothing of the steps in the dielectric layer between the poly and Metal 1.

In addition, since this local-interconnect level is made of materials that can normally tolerate relatively high temperatures (e.g., >800°C), the CVD glass that covers it can be flowed to smooth the steps at its surface. For example, as shown in Fig. 4-15, a 30-minute 900°C anneal in N_2 of a BPSG film (4.8 wt% B and 4.6 wt% P) over patterned polysilicon can result in an almost completely planar surface.[28] If a 900°C flow temperature is too high, a sacrificial etchback step can be used to planarize the surface of the glass layer to the same degree. In one report, a spin-on glass film is used as the sacrificial layer in such a process.[29]

Recent advancements in the glass-flow process have included the use of RTP (so that shallow junctions can be maintained)[30] and the design of a CVD-SiO_2 reactor in which simultaneous deposition and flow can be accomplished.[31] Mention of a reduced-temperature (<800°C), high-pressure reflow process has also been made, although not much information on its details has been published as of this writing.[32]

4.4.2.3. Minimize the Thickness of the Metal 1 Layer. The thinner the Metal 1 layer, the better will be the step coverage of Metal 2 as it crosses the steps

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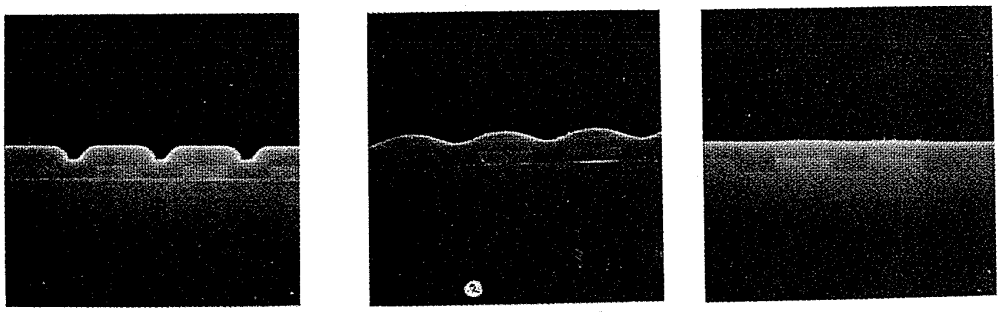

Fig. 4-15 Planarization of the PMD layer (BPSG) by thermal flow.[28] Reprinted with permission of Semiconductor International.

caused by Metal 1. A minimum thickness of ~500 nm has been proposed for Metal 1.[33] To ensure that such a thin Metal 1 layer will itself provide adequate thickness as it crosses over steps in the underlying topography, the planarization techniques described in the previous section will have to be employed. In addition, a useful approach in double-level-metal technologies is to utilize Metal 1 to interconnect the gates, while reserving Metal 2 for the power (V_{DD}) and ground (V_{SS}) buses. This also allows a relatively thin first-level metal to be used.

4.4.2.4 Achieve Smoothing of Steps in DM1 by Sloping the Sidewalls of Metal 1 Lines. As shown in Fig. 4-16, the reentrant angles of the steps in DM1 depend on the sidewall profile of Metal 1. If the sidewalls of Metal 1 are vertical (or even reentrant), the steps in atmospherically deposited CVD-SiO_2 DM1 layers will also be reentrant. This will reduce the step coverage of Metal 2 and will give rise to stringers if an anisotropic Metal 2 etch is used. If the sidewalls are sloped, as shown in Figs. 4-16c and 4-16d, the DM1 steps will be smoothed (the more slope, the better the smoothing). The most widely used technique for obtaining sloped sidewalls in metal lines with dry etching is to controllably erode the masking-resist layer during the metal etch. This is done by isotropically etching a sloped-resist mask edge at the same time that the metal is being etched. The slope in the resist sidewall is achieved either by flowing the resist at a high temperature or by reactively facet-etching the resist corner.[34]

As dimensions decrease, however, the latitude for sloping decreases. Another way to produce smoothing is to modify the metal-sidewall profile without sloping the sidewalls. One such approach involves cutting the sharp top corner of the metal line, as

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shown in Fig. 4-16e.[35] In this technique, a polymer is formed on the sidewalls of the Al lines following dry etching (but preceding removal of the resist). Next, a slight etch of the resist is performed so that the top corners of the Al lines are exposed. A wet etch of the Al is then used to cut the top corners. Finally, the resist is removed. Figure 4-16f shows an SEM photographs of an Al line with such cut top corners.

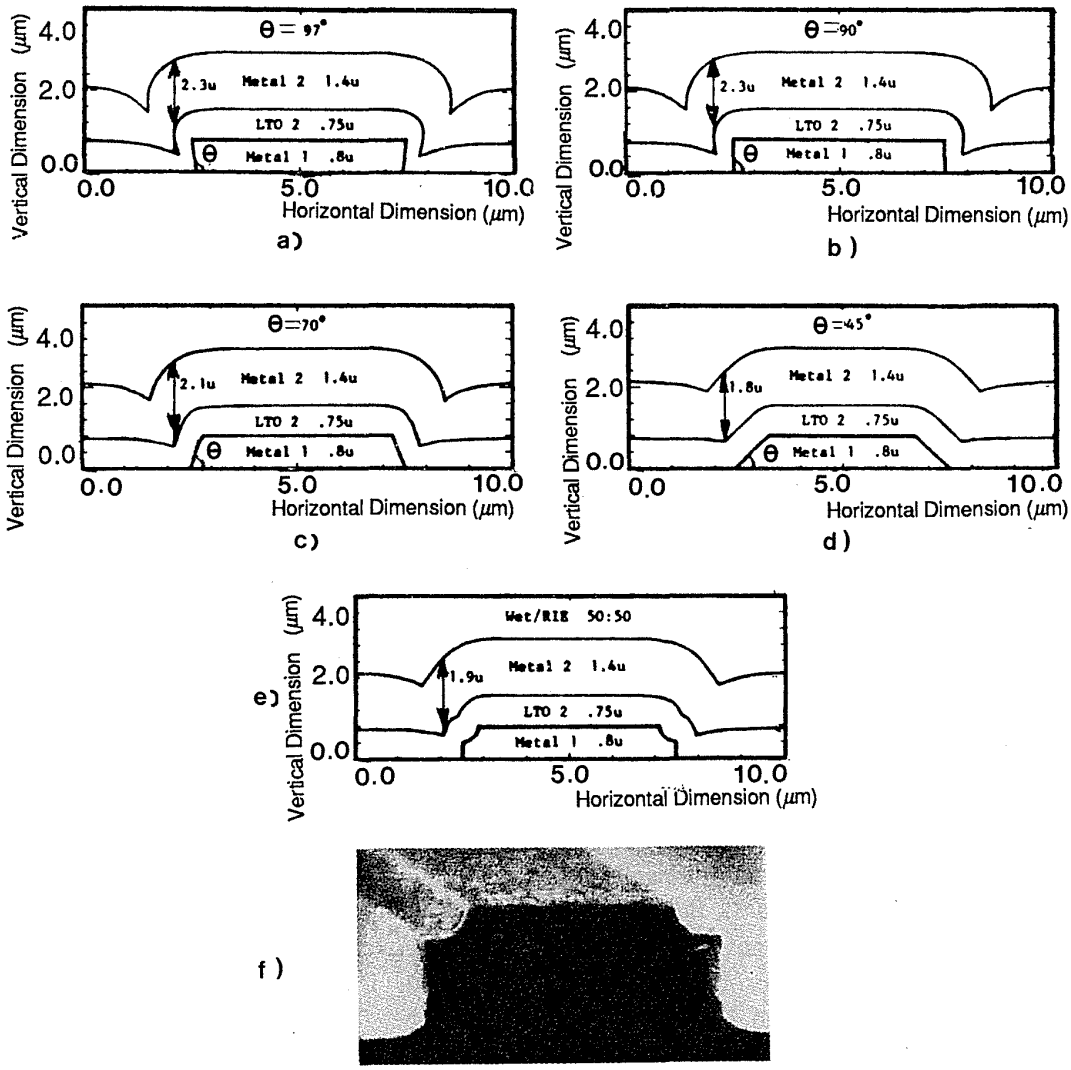

Fig. 4-16 Dependence of the angle of the DM1 sidewall on the profile of Metal 1. (a) Reentrant M1 sidewalls produce reentrant angles. (b) Vertical Metal 1 sidewalls still lead to DM1 reentrant angle sidewalls. (c) and (d) Sloped Metal 1 sidewalls produce DM1 sidewalls that are properly sloped and smooth, for ease of Metal 2 step coverage.[33] (© 1985 IEEE). (e) Etching away the top corner of the metal line also helps smooth the DM1 sidewall profile. (f) SEM micrograph of Metal 1 lines with the top corners cut off.[35] (© 1987 IEEE).

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4.4.3 Deposition of Thick CVD-SiO_2 Layers, and Etching Back without a Sacrificial Layer

As described in an earlier section, one of the simplest methods available for smoothing steps in DM1 is to deposit a CVD-glass layer that is significantly thicker than the step height it must cover. That is, it has been determined that in low-temperature CVD dielectric layers, the slope of the DM1 step decreases as the DM1 thickness increases. For example, it has been shown that if a PECVD oxide is deposited to 1.5X the underlying metal thickness, the steps of DM1 no longer exhibit reentrant angles.[36] From this effect, it would appear that the greater the ratio of the DM1 thickness to the underlying step height, the better the profile of DM1 would be (from the point of view of step coverage by an overlying metal film).

In practice, however, this is unrealistic, because increasing the thickness of DM1 also increases the via depth between Metal 1 and Metal 2. Furthermore, as the Metal 1 lines become more closely spaced, voids will form in the dielectric (see Fig. 4-8) if conventional atmospheric, low-pressure, or plasma enhanced low-temperature CVD-SiO_2 processes are used (ACVD, LPCVD or PECVD SiO_2, respectively). In order for void formation to be prevented, the thickness of DM1 must not be greater than half the minimum spacing between Metal 1 features. For example, for a 2-μm metal spacing, the maximum thickness of DM1 would have to be less than 1 μm. For a 1-μm space, no more than 0.5 μm of DM1 thickness could be deposited – and unfortunately, a film of this thickness (using the 1.5X guideline) would not prevent reentrant angles over 0.5-μm-thick metal lines.

A recently introduced process that utilizes a dielectric layer of plasma-enhanced low-temperature CVD TEOS together with a low-temperature thermal CVD TEOS (as described in section 4.3.2) allows narrow, high-aspect-ratio spaces between metal lines to be filled without the formation of voids. (As described earlier, plasma TEOS allows spaces with aspect ratios as high as 0.85 to be filled without void formation, whereas PECVD silane-based SiO_2 films exhibit voids when the aspect ratio of a space exceeds 0.5.)[37] This process will make the use of a nonsacrificial-etchback technique applicable to smaller-sized devices. However, it can be seen from Fig. 4-17a that this process does not provide global planarization.

If the spacing between metal lines is large enough to allow this technique to be employed (or if the low-temperature CVD TEOS process mentioned above is used), but the thickness of DM1 is too great after deposition, the DM1 can be etched back until a desired thickness is obtained. If an etch process that has a sputtering component is used, the etch will also round off the corners (see Vol. 1, chaps. 9 and 16), enhancing the smoothing effect (Fig. 4-17b).[38] One advantage of this type of process over a sacrificial-etchback process (see section 4.4.8) is that it is much simpler and does not cause contamination of the reactor walls by polymer deposition. A report detailing such a plasma TEOS nonsacrificial-layer etchback approach for a double-level-metal CMOS process is found in reference 37.

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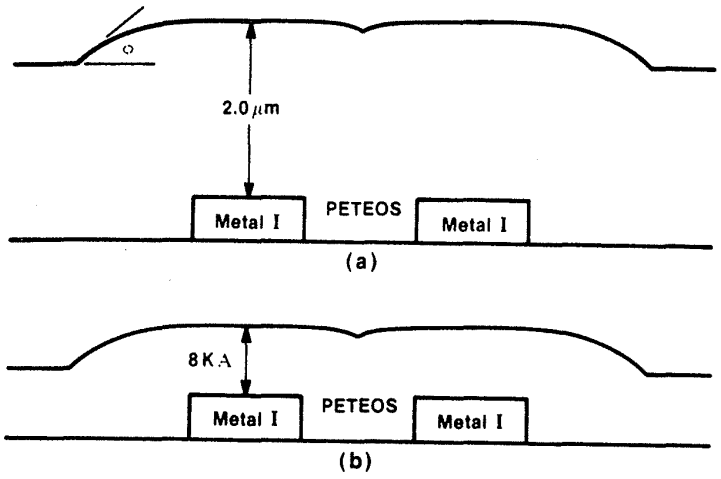

Fig. 4-17 (a) Thick PETEOS deposition (2.0 μm) over 0.5-μm Metal 1 creates a "smoothed" topography for Metal 2 at the edge of an isolated Metal 1 feature while planarizing closely spaced Metal 1 features. (b) An anisotropic etchback of the interlevel dielectric preserves the "smoothed" surface.[37] (© 1987 IEEE).

4.4.4 Oxide Spacers

We have seen that the step coverage of metal lines is dramatically improved if the steps have gentle slopes. Flowing of doped CVD glass layers is used to achieve such slopes when the PMD layer covers polysilicon. Unfortunately, when metal is deposited on the wafer, the high temperatures needed to cause glass flow cannot be tolerated, and hence this solution cannot be applied. Another method of producing such smoothing is to taper the sidewalls of the underlying metal lines. Techniques to achieve such tapering were described in an earlier section. Tapered metal lines, however, are difficult to form, and they require tight process control. In addition, as the line widths get narrower (without a corresponding decrease in line thickness), the latitude for sloping decreases. The use of oxide spacers at the sidewalls of the metal lines allows shallower-sloped steps to be created without tapering of the metal lines.[39,40,41]

The oxide-spacer approach begins with the deposition of a doped PECVD-SiO_2 layer over Metal 1. This layer exhibits conformal coverage over the Metal 1 lines and other steps (see Vol. 1, chap. 6). The PECVD SiO_2 layer is then anisotropically etched back until Metal 1 is exposed. Unetched portions of SiO_2 at the vertical sides of metal lines

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and other steps remain following this etch; such residual structures are known as *oxide spacers* (Fig. 4-18). The slope of the spacer sidewalls is less severe than the slope of the as-deposited conformal PECVD oxide. The smoothing occurs as a result of faceting during the anisotropic dry-etch step (see Vol. 1, chap 9). Following spacer formation, a second layer of CVD SiO_2 is again conformally deposited, and the gentler slopes of the spacers are thus replicated in the steps at the surface of the dielectric layer.

The oxide-spacer technology is seen to be a semi-planarization technique. As a result, it offers the following advantages:

- It is a simple approach for achieving adequate Metal 2 step coverage in that it requires no photolithography and only one extra SiO_2 deposition and its etchback.
- It is not sensitive to the oxide-thickness uniformity or to the degree of overetch used in the etchback step.

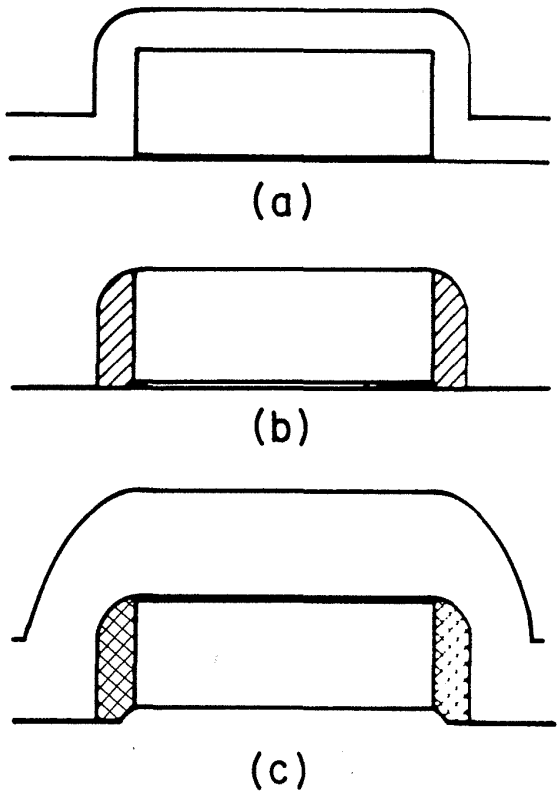

Fig. 4-18 Spacer formation: (a) CVD deposition over a polysilicon line; (b) spacer formation by RIE; (c) spacer structure covered with CVD oxide.

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- It avoids the deposition and etching of a sacrificial resist layer, steps that can cause contamination of the etch chamber through the deposition of polymer by-products arising from the resist etching.
- All of the via holes are of the same depth, since the final SiO_2 layer is equally thick in all places (making the etching of sloped via holes much easier).

Oxide spacers also have several important limitations, including the following:

- Since the step heights themselves are not reduced by this technique, as each layer of a multilevel structure is added the steps additively grow larger. This causes severe lithography problems for small depth-of-field steppers (see chap. 2, section 2.9.2); step-coverage problems would become severe for third and fourth levels of metal.
- If adjacent Metal 1 lines get too close (e.g., when the aspect ratio of the spaces between adjacent Metal 1 lines approaches 0.6), voids will form when the first PECVD-SiO_2 layer is deposited (Fig. 4-8). The narrow spacing leads to shadowing effects, and when combined with the lower surface mobility of reactive species at temperatures below 600°C, these effects can result in deposition rates that are higher on the upper surfaces than in the valleys between structures. Such voids may open up during the etchback step and subsequently trap moisture, photoresist, or metal from the next deposition.
- Long Metal 2 lines will have measurably larger resistances than those deposited on a completely planar surface (since the line must travel up and down the steps of the semiplanarized surface).

Because of these limitations, the oxide spacer approach is viewed as a stopgap solution, one that can be used only in two-level metal processes with Metal 1 spacings that are no closer than ~2 μm.

4.4.5 Polyimides as Intermetal Dielectrics

The use of polyimide films as interlevel dielectrics has been pursued as another technique for providing partial planarization of the dielectric surface. Polyimides offer the following attractive properties for such applications:

- They produce surfaces in which the step heights of underlying features are reduced, and step slopes are gentle and smooth.
- They are able to fill small, high-aspect-ratio openings without producing the voids that occur when low-temperature CVD-oxide films are deposited.
- The cured polyimide films can tolerate temperatures of up to 500°C without degradation of their dielectric film characteristics.

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- Polyimide films have a dielectric-breakdown strength that is only slightly lower than that of SiO_2;
- The dielectric constant of polyimides (3.2-3.4) is smaller than that of SiO_2 (3.5-4.0) and of silicon nitride (6.0-9.0);
- The films are free of pinholes and cracks;
- The process used to deposit and pattern the polyimide films is relatively simple, and it is significantly less expensive to carry out than are the non-spin-on inorganic planarized-dielectric alternatives. That is, polyimide film is spun on in the form of a liquid (polyamic-acid precursor), much as in the process used to deposit photoresist films. During a high-temperature-cure step (e.g., at 150°C for 30 min and 300°C for 60 min), the polyamic acid undergoes a chemical change (imidization) that causes it to become the solid polyimide film. Vias are normally dry etched in the cured film using oxygen- or fluorine-based plasmas.

The partial planarization produced by polyimide films occurs because the film is deposited as a liquid. Just as the surface of a lake is flat because of the surface tension of the liquid, the polyamic acid in liquid form fills the crevices on the wafer surface and produces a flat surface. During the bake step (in which the polyamic acid is imidized), the solvent in which the polyamic acid is dissolved is also driven off, along with OH as H_2O. Since only a relatively small percentage of the film consists of solids (typically, 15-30%), the final surface height of the polyimide in areas of the wafer over which the liquid depth is larger will be at a lower level than in areas over which the liquid depth is smaller (Fig. 4-19). In general, the larger the percentage of solids in the original liquid material, the higher the degree of planarization that is produced.

The planarization of actual polyimide films ranges from 49% to 69% if a single-coat application is used. Planarization can be further increased through the application of a second coat.[42] In many processes, a thin, so-called *hard-mask layer* has been used between the polyimide and the resist etch mask. This hard-mask layer is often needed because photoresist and polyimide both etch at about the same rate in the O_2 plasmas used to etch vias in the polyimide. Various films have reportedly been used for this purpose, including PECVD SiO_2, Al, Ti, and spin-on glass. After via etching is completed, the hard mask is removed.

Some impressive processes using polyimide as an interlevel dielectric have been reported, including a three-level-metal process for bipolar analog circuits from IBM (in which the polyimide acts as the interlevel dielectric between Metal 1 and Metal 2, and between Metal 2 and Metal 3, as well as the passivation layer);[43] a three-level-metal process for a bipolar gate array by Siemens;[44] and a multilevel-tungsten process from Hewlett-Packard.[45] Despite such successes, polyimide films have not gained widespread acceptance as interlevel dielectrics. The reasons for this have to do with the following manufacturing-compatibility and reliability concerns:

- Polyimide is hygroscopic (i.e., it readily absorbs water). When the polyimide films are rapidly heated (e.g., during a final sinter step or during the die-attach

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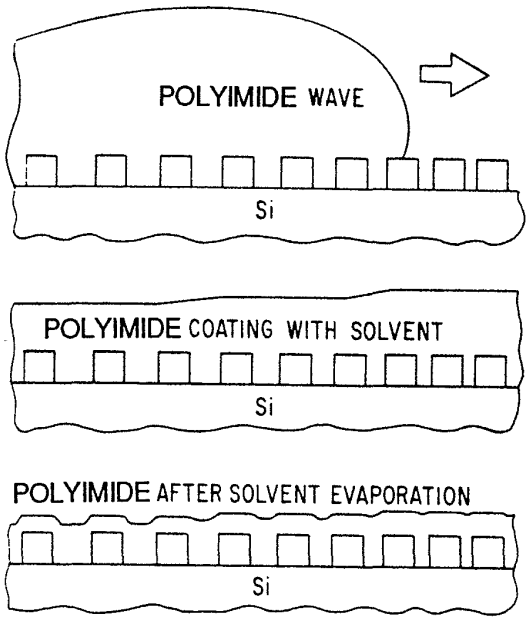

Fig. 4-19 Although the surface of polyimide film is planar when first spun on in liquid form (a) and (b), as the film is cured, solidified and shrunk, the steps on the surface reappear (c), especially at widely spaced features.

step), any absorbed water will be desorbed by the polyimide film. If a wide metal line covers a portion of the polyimide film, the moisture under the metal film will attempt to escape at the surface covered by the metal, which can lead to bubbling of the metal film. To prevent such occurrences, a slow, ramped dehydration bake must be used whenever the wafers with polyimide films are heated.[46] Some of these problems may be alleviated through the use of new polyimide materials that exhibit much less moisture absorption than those of earlier generations.[47]

• The absorbed moisture can potentially cause corrosion of underlying metal lines. Although a number of studies have indicated that this may not be a problem, preventive measures have been included in some polyimide processes to forestall such possibilities. For example, a coating of silicon nitride was added over each layer of polyimide in the processes of references 44 and 45. In the IBM process,[43] a silicon-nitride layer was deposited *under* the first polyimide intermetal-dielectric film to prevent moisture and ionic penetration to the devices.

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• Reliable adhesion of metal films to polyimide underlayers has also been a concern. Although an adhesion-promoting layer is deposited onto SiO_2 layers prior to the spinning on of the polyimide (which is quite effective in promoting good adhesion between the polyimide and the SiO_2), there is as yet no well-understood model that explains how to produce good adhesion between the overlying metal and the polyimide. The concern is magnified because the thermal-expansion coefficients of metals and polyimides are generally not equal, and residual stresses caused by such mismatches may lead to delamination failures. This problem, however, can be circumvented by coating the polyimide with a nitride film[44] or an oxide film.[47] A report dealing with adhesion of metal to polyimide is given in reference 48.

• Because polyimide films are easily etched in oxygen- and fluorine-based plasmas, a suitable etch process must be developed when metal films are patterned over polyimide layers. Since the underlying polyimide can be easily eroded during the overetch part of the metal-film-etching process, in some cases it may be necessary to provide a special etch-stop material under the main metal layer to prevent such polyimide erosion.

4.4.6 Planarization with Bias-Sputtered SiO_2

Deposition of SiO_2 films through rf sputtering of a silica-glass target is another technique used to achieve partially or completely planarized intermetal dielectric layers. Because the wafers themselves are also subjected to a negative rf bias during the sputter-deposition process, the process is termed *bias-sputtered SiO_2.**

The application of a bias to the wafers serves two key purposes in this process. First, if SiO_2 films are sputter deposited without bias, they are porous, they etch very rapidly in HF solutions, and they have a columnar structure with scattered nodular defects. A dielectric film with such a structure is obviously undesirable from the point of view of pinhole density, dielectric strength, and the ability to provide corrosion protection to underlying metal films. Ion bombardment during film growth (resulting from biasing of the wafers) can modify the microstructure of the film so that dense SiO_2 films with properties very similar to those of thermally grown SiO_2 can be obtained.

The second role of the applied bias is to establish deposition conditions that bring about planarization of the SiO_2 film. The planarization mechanism in bias-sputtered SiO_2 was analyzed in a paper by C. Y. Ting et al.[49] These researchers determined that planarization occurs due to the interaction of two factors: (1) the film buildup on the substrate resulting from sputtering at the target is independent of the geometry of the features of the substrate; and (2) resputtering at the substrate (which occurs as a result of the bias applied to the wafers) is a strong function of the geometry of the substrate features (i.e., sputtering yield is a function of the ion angle of incidence, and sloped

* The glass-sputtering target is commonly referred to as a *quartz target;* as a result, this process is also frequently called *bias-sputtered quartz,* or *BSQ.*

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surfaces on the substrate thus resputter faster than flat areas; Fig. 4-20a). In general, the sputtered SiO_2 process can proceed in one of three modes: (a) the nonplanarization mode; (b) the planarization mode; or (c) the erosive mode.

If the film is deposited without biasing of the wafer, the deposition will proceed in a *nonplanarization mode*. In such cases, the deposition rate will be greater than the resputtering rate, regardless of the slope of the substrate feature. Film growth as a function of time in this mode is shown in Fig. 4-20b; no planarization is seen to occur.

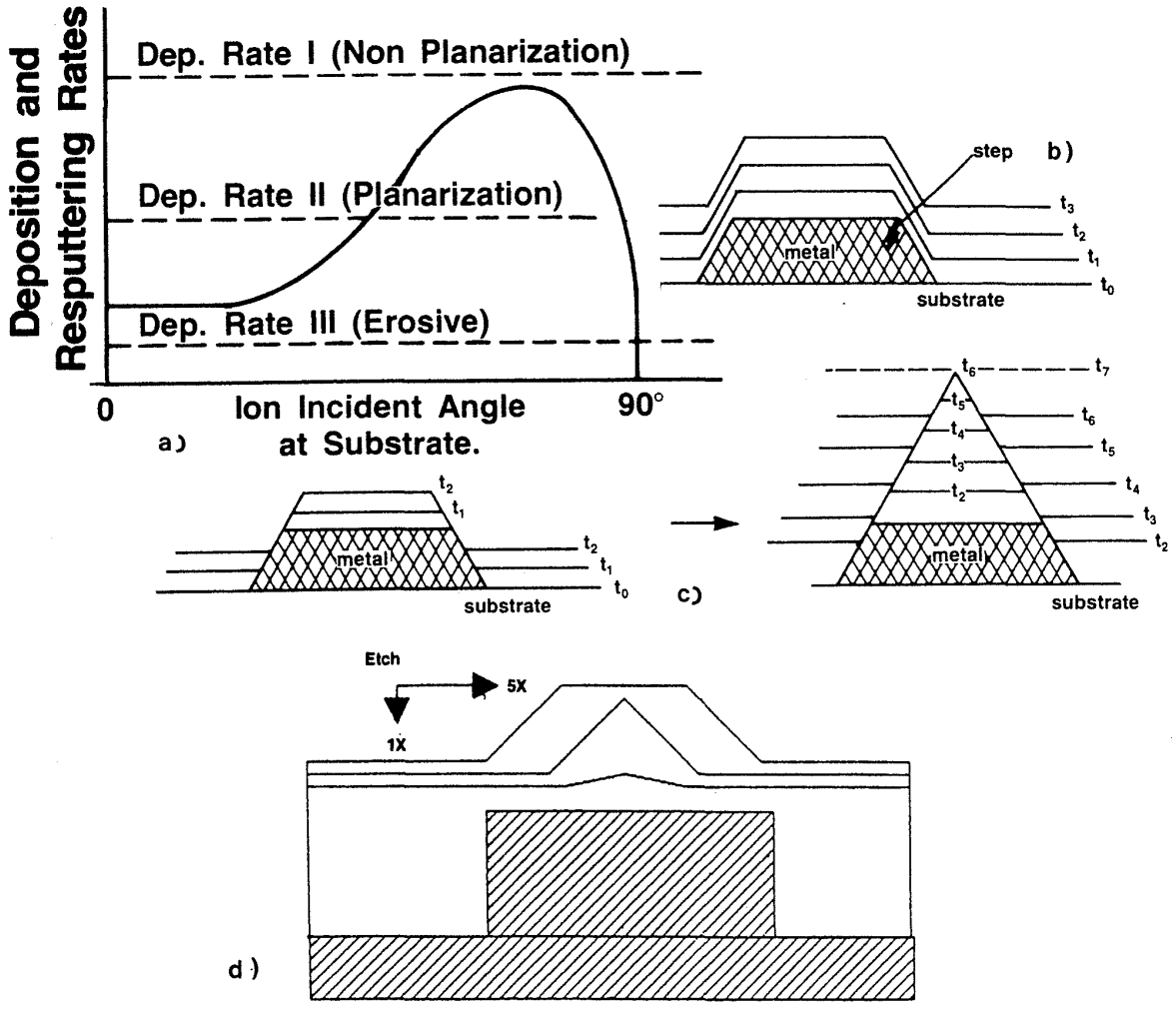

Fig. 4-20 (a) Sputtering (and hence also resputtering) yield is higher on surfaces whose angle toward the incident ions is less than 90°. (b) Nonplanarization mode - deposition rate is greater than resputtering rate (no bias is applied to the wafer). (c) Planarize mode - net deposition on the sloped areas is much lower than that on the flat areas. (d) Erosive mode - no net deposition anywhere, but material is sputtered away more rapidly on the sloped areas than on the flat areas. Although the pyramid structure on the surface eventually disappears first over narrow lines, it remains much longer over wider lines.

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If a bias is applied to the wafer, the deposition can be made to proceed in either a *planarized* mode or an *erosive* mode. In the *planarized mode,* the net deposition on the sloped areas is much lower than it is on the flat areas (Fig. 4-20c). In the *erosive mode*, there is no net deposition anywhere, but the sloped regions will be etched more rapidly than the flat regions. Under conditions of *planarized deposition,* as the SiO_2 film grows thicker, the surface of the SiO_2 over a narrow metal line will change, as shown in Fig. 4-20d. Eventually the pyramid structure on the surface will disappear, and complete planarization will be achieved.

For several reasons, the process is rarely allowed to proceed to this point in practical circumstances. First, the planarized SiO_2 film thickness would end up being much too thick for most applications. Second, complete planarization would have occurred only over the narrow lines – that is, over wide lines no reduction in the step height would have occurred, and over medium-width lines a pyramid would remain.

As a result of the second factor, in some bias-sputtered SiO_2 processes the maximum width of the metal lines to be covered is restricted, and the film is deposited to a thickness in which pyramids remain over these lines. The *erosive mode* is then used to sputter away the pyramids so that a planarized surface is achieved. This erosive step, however, causes some of the oxide in the flat areas to also be etched away. To end up with a sufficiently thick dielectric film in such processes, it might be necessary to carry out another dielectric deposition step.[229] If such multiple deposition/etch/deposition steps are performed, it may take several hours to produce an SiO_2 layer of adequate thickness and planarity. (In fact, to produce pyramid structures with less steep slopes, a greater resputtering rate during the planarization mode is needed, which further reduces the overall growth rate.) Thus, one limitation of the planarized, bias-sputtered SiO_2 process is low throughput due to low net-deposition rates. This limitation is emphasized by the high capital-equipment cost needed to implement the process.[50]

The bias-sputtered SiO_2 approach for planarizing films offers the advantages of being able to fill very narrow spaces and of doing so at relatively low temperatures (e.g., the deposition is typically carried out at <400°C). Nevertheless, even though IBM has reportedly used bias sputtered SiO_2 for many generations of IC products,[51] and other companies have also implemented it for some special applications,[217] this approach has not gained acceptance as a mainstream dielectric planarization technology in IC production. In addition to the low-throughput drawback already mentioned, there are a number of factors responsible for this. Among them are the following:

- The sputter-deposited SiO_2 films exhibit high compressive stresses (~100 MPa, compressive), which contribute to the problem of stress-induced cracks in the metal films underlying such dielectrics.

- The sputtered-SiO_2 material also deposits on the shields, shutters, and other surfaces of the sputter chamber. Since these films are also highly stressed, they have a strong tendency to flake off in the form of small particulates. As a result, particulate levels in the bias-sputtered SiO_2 process can be much higher than those observed in conventional CVD-oxide processes, and they can represent a serious yield limiter in manufacturing environments. Special rigorous cleaning procedures

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of the sputtering equipment must therefore be followed if bias-sputtered SiO_2 is to be successfully implemented.

- If the pyramid structures of Fig. 4-20d are not removed, they can cause cracking of metal lines deposited over them.
- Metallic contamination arising from resputtering of the sputter-chamber surfaces (e.g., iron contamination caused by resputtering of the stainless-steel fixtures inside the chamber) is another possible source of manufacturing yield loss.
- The purity of the SiO_2 targets has been a concern, and radiation damage associated with the sputter-deposition and etch phenomena has been reported to produce reliability degradation in MOS devices.

Progress has reportedly been made on several of the above problems. The pyramid structures on the SiO_2 surface have been eroded through the use of a photoresist sacrificial-etchback step (see section 4.4.8) after the SiO_2 film has been initially deposited by means of a planarization-mode deposition step.[52] In a more recent report, a double photoresist layer was used to increase the planarization over wide metal features.[53] In addition, the purity of the SiO_2 targets has been improved. Finally, a process has been described in which the radiation damage is reduced to an acceptable degree for practical use.[52] In this report, device damage that could not be annealed out by a 450°C step was identified as gate-oxide damage caused by bremsstrahlung X-rays (which are apparently produced when high-energy secondary electrons, originating from the sputter target, strike the wafer). The suggested way to decrease this damage was to prevent these high-energy electrons from reaching the wafers. This was achieved by placing a stainless-steel grid between the target and the wafers in the sputter chamber. The presence of the grid, which was biased to intercept the high-energy target electrons was reported to not measurably contaminate the devices. It did, however, result in an even lower deposition rate. A high-deposition-rate bias-sputtered SiO_2 process is described in reference 57.

4.4.7 CVD SiO_2 and Bias-Sputter Etchback

An alternative method similar to the bias-sputtered SiO_2 approach for forming partially planarized dielectrics is the *CVD/bias-sputter etchback* technique (CVD/Etch). In this process, the SiO_2 layer is formed through the use of plasma-enhanced CVD (PECVD) rather than through the sputtering of a glass target (Figs. 4-21a and b. The advantages are that the slow sputter-deposition process is replaced by a faster CVD process, and that the CVD process eliminates the problem of dielectric-film contamination due to impurities in the sputter target. In addition, the deposited films are not as highly stressed and particulates not as severe as with the bias-sputter approach. Finally, the high-energy electron damage caused by the sputter deposition is eliminated. The only bombardment of the wafer surface is by the argon ions. Since these penetrate no more than a few atomic layers, they affect only the interlayer dielectric, not the devices underneath.

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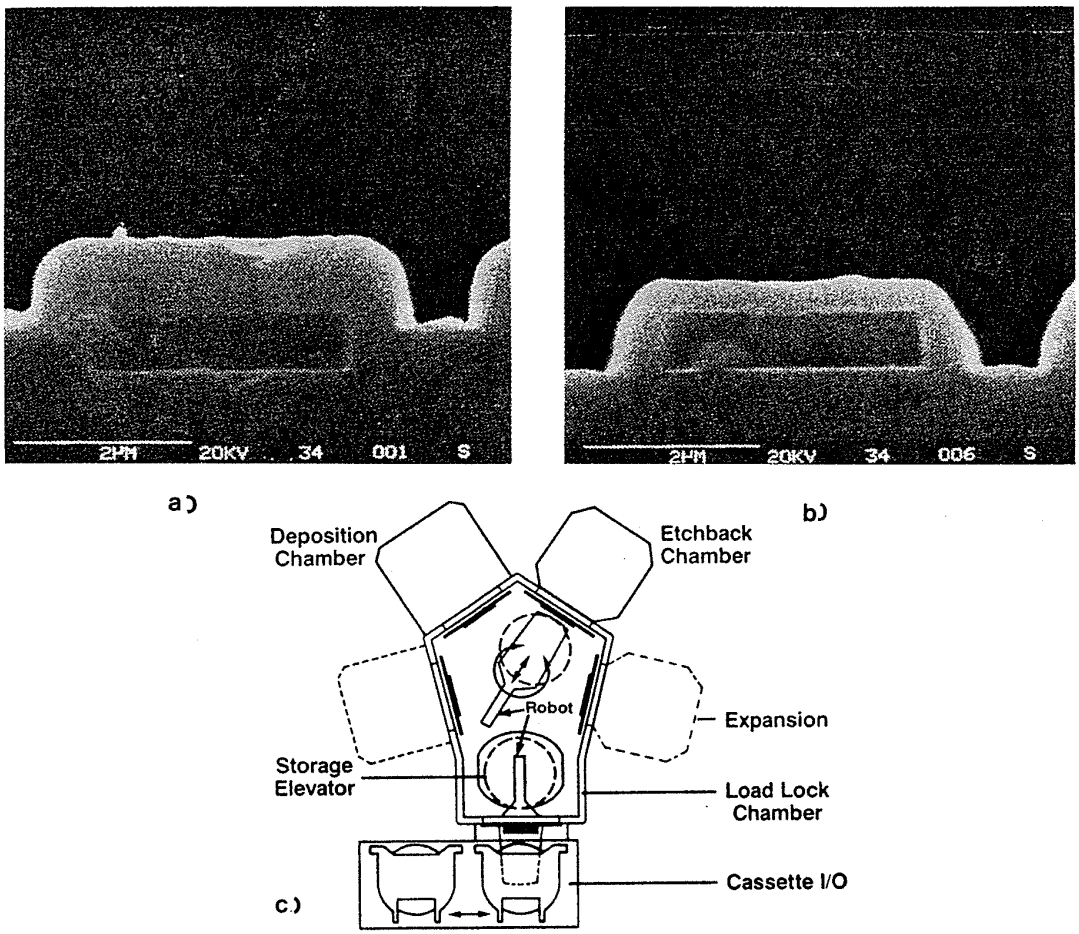

Fig. 4-21 CVD SiO_2 and in situ etchback. (a) Photograph of an as deposited PECVD oxide over vertical sidewalled Metal 1 lines. (b) Shape of PECVD oxide after reactive ion etching using energetic ion bombardment.[54] (© 1987 IEEE). (c) Example of a multi-chamber tool that can perform deposition in one chamber an etching in another. Courtesy of Applied Materials.

Early attempts to implement this technique involved deposition of the film in one machine, followed through sputter etching of the deposited layer in another. An enhancement of this technique involved reactive facet tapering of the oxide by the use of a reactive gas (CHF_3) in conjunction with Ar.[54,56] This produced steps on the surface of the oxide with slopes that were not as gentle as they would have been if the steps had been created by purely physical sputtering. However, the erosion rate was much faster, which significantly increased the throughput. Subsequent work integrated the process into a single reactor, first with a parallel-plate reactor,[55,243] and later with a multi-chamber tool that can perform deposition and etching without exposing the wafers to

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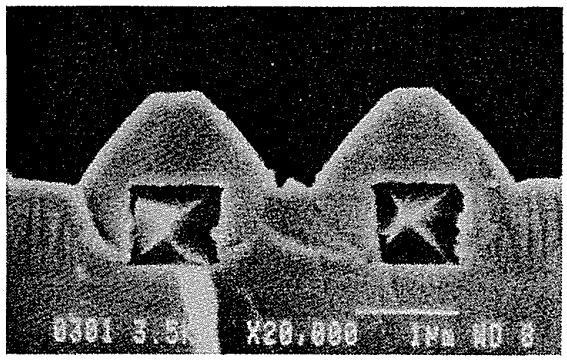

Fig. 4-22 At the conclusion of a CVD/Etch process, the surface topography over narrow lines will have a pyramid structure.[58] (© 1987 IEEE).

atmosphere between process steps (Fig. 4-21c).[58,244]

One disadvantage of the CVD/Etch method is that at low temperatures the CVD film does not fill high aspect ratio openings (e.g., a 0.5-μm space between 0.7-μm-thick metal lines) as effectively as does bias-sputtered SiO_2. Thus, for such high-aspect-ratio applications, the deposition and etchback procedure must be performed in several sequential deposition/etch sequences to prevent the formation of voids in such spaces.[58] First, an oxide layer is deposited that is not thick enough to cause seam closure in the opening. Sputter etching is then used to form sloped surfaces in the small openings. This keeps the small trenches open during deposition, allowing them to eventually be completely filled without the formation of keyholes (voids). This multistep approach also tends to stop the propagation of pinholes.

At the end of the multistep process, the surface topography will have pyramid structures over narrow lines, as shown in Fig. 4-22. To eradicate these pyramids, an erosive-mode step is carried out so that a planar surface is finally established. The pyramid structures can also be removed using a resist-etchback technique.[59] A report has been made of a two-level-metal wiring technology with metal pitches of 1.9 μm for Metal 1 and 2.4 μm for Metal 2 that uses this method to form the interlevel dielectric.[60]

There are two main drawbacks to this multiple CVD/Etch process: (1) the throughput is low, even in a batch reactor (e.g., eight wafers in a batch); and (2) complete planarization is not achieved over wide steps.

4.4.8 Planarization through Sacrificial-Layer Etchback

Planarization of CVD interlevel-dielectric films can also be achieved using the *sacrificial-layer etchback* technique. This method has gained the most widespread acceptance in two-level-metal processes down to ~1 μm device technologies (and even in some reported three-level-metal bipolar processes).[61] Using this approach, it is possible to achieve a high degree of planarization between steps that are ~2-10 μm apart. With more closely spaced features, the technique runs into problems, and for more

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widely spaced steps, planarization is less complete. The process is carried out by first depositing the CVD film that will serve as the interlevel dielectric. This layer is then coated with a film that will later be etched off (sacrificed). In most cases, such sacrificial layers are deposited as low-viscosity liquids. Upon being baked, these liquids become solid thin films that are thick enough to produce an essentially flat surface. A few other reports have described the use of conformally deposited silicon nitrides over CVD oxides or oxynitrides. These processes rely on controlling the difference in plasma etch rates between the two materials to obtain semi-planarization of the dielectric surface.

When sacrificial liquid layers are used, the material is spun on over the underlying dielectric film (which, at best, may exhibit conformal coverage of the wafer surface, but essentially no planarization). The sacrificial layer is relatively thick (typically, 1-3 μm) for improved surface planarity. The wafer is then baked until the spun-on film becomes a solid, and the surface (above features that are less than ~10 μm apart) becomes reasonably well planarized, as shown in Fig. 4-23a.

Photoresists have been the most widely used sacrificial liquid layers, although polyimide and spin-on-glass (SOG) layers have also been occasionally used for this role. Resists are popular primarily because of their purity, their well-characterized process history, and their lower cost.[62,63] High-temperature baking (>150°C) may be used to flow the resist to improve planarization even further. However, the effect of such high bake temperatures on the plasma-etch rate of the resist must be taken into account in order for good process control to be achieved. Figure 4-24 illustrates the degree of planarization that is obtained as a function of the width of an isolated feature for several photoresists (and the AZ protective-coating material).[64] As long as the feature size is smaller than 10 μm, the degree of planarization can exceed 70% with most photoresists.

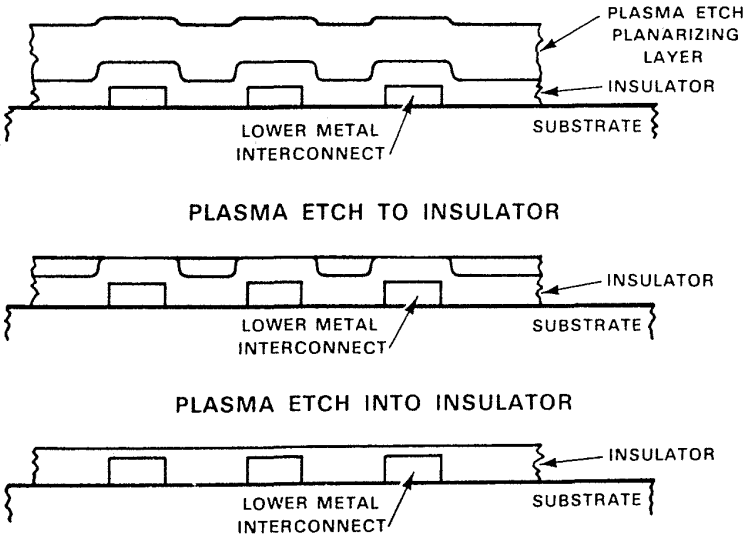

Fig. 4-23 Sequence of steps used in a sacrificial-layer-etchback process for planarization.

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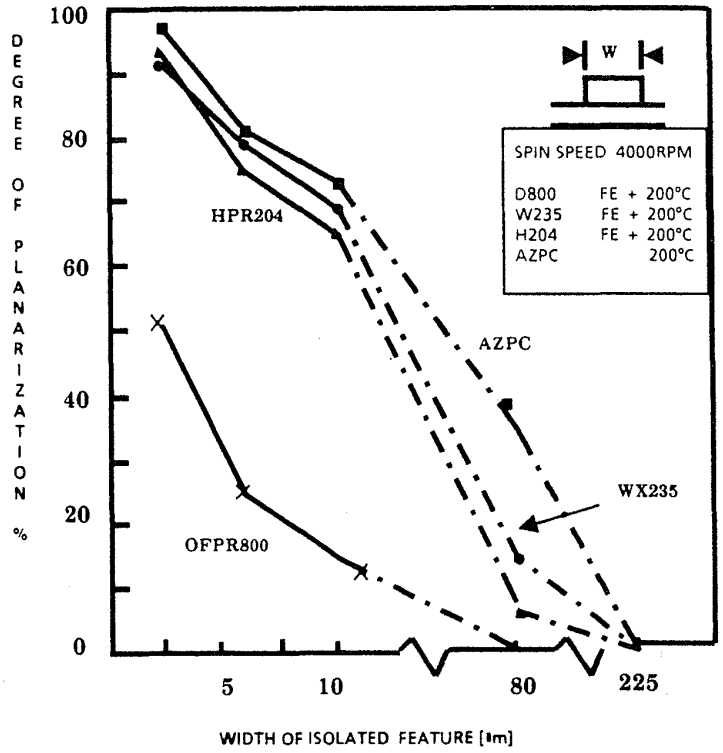

Fig. 4-24 Degree of planarization versus various feature sizes for different polymer films.[64] (© 1987 IEEE).

In the next step, the sacrificial layer is first rapidly etched back in a plasma (typically, O_2 or O_2 mixed with CF_4)[65] until the topmost regions of the dielectric layer are just exposed (Fig. 4-23b). The etch chemistry is then modified so that the sacrificial-layer material and the dielectric are etched at approximately the same rate. The etch is continued under these conditions until all of the sacrificial layer has been etched away. At this point, the surface of the dielectric film is highly planarized since the profile of the sacrificial layer is transferred to the dielectric layer by the etchback procedure. The thickness of the dielectric film over underlying features, such as metal lines, may be thinner than desired after the etchback is completed. In some processes, in fact, the etchback step is allowed to proceed until the Metal 1 lines are exposed. In any case, an additional layer of CVD dielectric is generally deposited in order to establish a minimum adequate thickness everywhere on the wafer surface.

4.4.8.1 Degree of Planarization Achieved by Sacrificial Etchback. The sacrificial-etchback process planarizes the final dielectric-layer surface by reducing the step height and smoothing the steep steps of the as-deposited dielectric layer. Although the step height can be reduced to zero (complete planarization) over closely spaced features, this may not always be the desired result. Such complete planarization will lead to widely varying via depths, which may be difficult to adequately fill with the

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next level of metal. As a result, a trade-off of β (defined by Eq. 4-7) against *maximum via depth variation* can be made. The final step height is related to the initial step height and the ratio of the etch rates of the resist, E_r, and the oxide-etch rate, E_o, by[66]

$$t^f_{step} = t^i_{step} - [(E_o / E_r)(t^i_{step} - t_r)] \qquad (4-9)$$

where t_r is the step height in the planarizing layer. Combining Eqs. 4-7 and 4-9 yields the following simple relation between the process parameters and β:[65]

$$\beta = (E_o / E_r)[1 - (t_r / t^i_{step})] \qquad (4-10)$$

The linear relationship between β and the etch rate ratio (E_o/E_r) indicates the need for maintaining precise control over both the deposition processes and the planarization etch.

The maximum degree of planarization, β_1, based on the maximum via depth variation and the minimum acceptable post-etchback thickness of oxide, t_{ox}, covering Metal 1 (or polysilicon), is given by

$$\beta_1 = (t_{ox}' - t_{ox}) / t'_{step} \qquad (4-11)$$

where t'_{step} is the step height of the underlying topography and t_{ox}' is the maximum depth of the vias following etchback. Thus, the appropriate degree of planarization is $\beta \leq \beta_1$. A model for predicting the planarization that will be produced by an etchback process is described in reference 68. The desired etch-rate ratio is typically obtained by varying the oxygen-flow rate in a CF_4/O_2, CHF_3/O_2, or C_2F_6/O_2 plasma, as illustrated in Fig. 4-25.

The above discussion is generally valid only for the planarization of topographies in which features are less than 10 μm apart. For wide, isolated features, the step height will not be reduced, since the resist thickness on top of such features will be the same as the thickness over adjacent substrate regions (Fig. 4-26a). If it is necessary for t_r to be zero everywhere on the wafer surface – regardless of the underlying feature widths, spacings and density – it is possible to use a dual photoresist process (which also involves an additional resist-patterning step, as well as a *planarization block mask* [PBM] to pattern the inverse of the undesired topography), as described in references 67 and 70 (Fig. 4-26b). In this procedure, the first organic film is spun on, and the PBM mask is used expose and develop this film. As a result, this layer remains in the wide "low" regions, which are thereby effectively filled. Consequently, the final planarizing-resist film only has to fill small crevices (Fig. 4-26b).

It has been pointed out, however, that creation of the PBM mask cannot be implemented by merely reversing the mask that produced the underlying topography. That is, this simple approach results in errors due to changes in the resist thickness caused by the underlying pattern, misalignment, and "overfilling", as the resist competes with (partial) planarization accomplished by the underlying deposited films (Fig.

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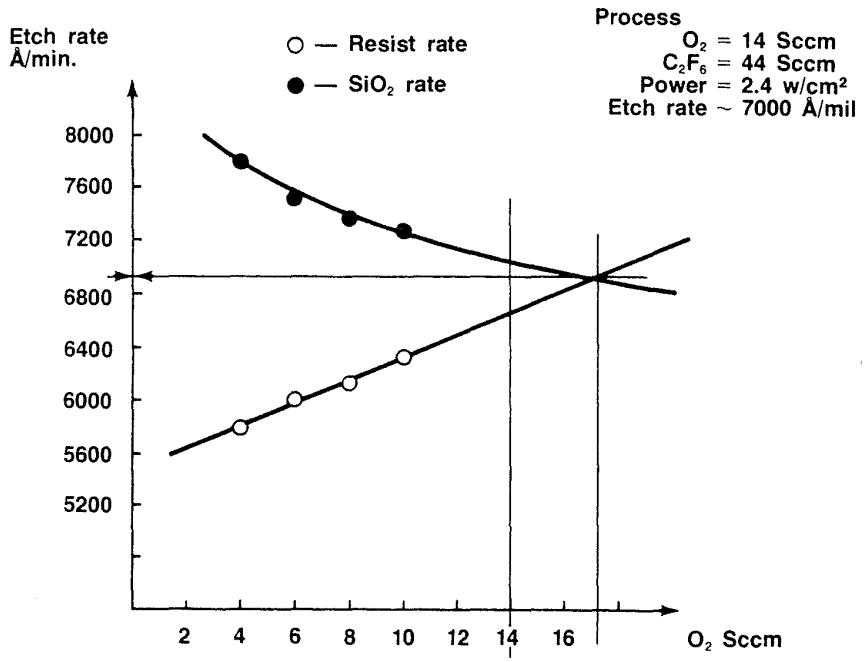

Fig. 4-25 Example of how the etch rates of resist and SiO_2 can be equalized by varying the gas mixture used in the plasma-etching process. Courtesy MRC, Inc.

4-26c).[228] The PBM mask must therefore be designed to compensate for these errors.

A novel thermal flow/thermal setting polymer (aromatic polyalkylenes) has recently been described that planarizes even the largest geometries, such as 100 μm bonding pads, after a reflow step at 200°C (Fig. 4-26d).[249] In this figure the results obtained using 1.2 μm of AZ1370 photoresist coating are also included. The new polymer provides a 60% planarization even at feature sizes of 250 μm.

Another etchback technique for obtaining complete global planarization that does not rely on dry etching is *chemical-mechanical lapping*.[69] This technique has been considered for removing the top layer of the Si substrate after a selective epitaxial process has been performed to remove facet indentations (see chap. 2), as well as for intermetal-dielectric planarization. The technique is still being investigated in a research mode, and is discussed further in section 4.4.11.

4.4.8.2 Advantages of the Sacrificial Etchback Process. In addition to being a low-temperature process, the sacrificial etchback method uses familiar processing technology, materials, and equipment (e.g. spinners, dry etchers, and CVD dielectric-deposition systems). It is also relatively straight-forward, and the final interlevel-dielectric film is a material (CVD SiO_2) for which there is already a long process history. Finally, most competing processes exhibit more severe drawbacks than this approach.

4.4.8.3 Sacrificial-Etchback Process Problems. To achieve the desired degree of planarity and final dielectric film thickness, tight process control is necessary

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for such parameters as the magnitude of the etch rate, the etch-rate uniformity across a wafer, end-point detection, and oxide-thickness uniformity under the resist layer. The resist etch rate is sensitive to the cure cycle (especially if a high-temperature bake step [>150°C] is used to improve surface planarity), to chamber preconditioning, and in batch processes, to the number of wafers present in the chamber. Using SOG as a sacrificial layer in lieu of resist has been suggested as a way to alleviate the problem of resist etch-rate variability, since the etch rate of SOG is found to be less variable with bake temperature and processing ambient conditions (e.g., humidity).[71]

The process requires a multitude of steps, which implies a lengthy process, and thus a low throughput. In general, etchback is a difficult process to successfully implement in a batch-etch mode, resulting in an even lower throughput.

While the thickness of the resist is a function of many variables, in general, it will be thickest over narrow spaces and thinnest over high, narrow, isolated steps. Thus, the dielectric film thickness may become unacceptably thin over the latter after etchback. In addition, the small amount of resist remaining between narrowly spaced features makes end-point detection difficult.

If an insufficient cure cycle is used, solvent remaining in the resist may bubble out

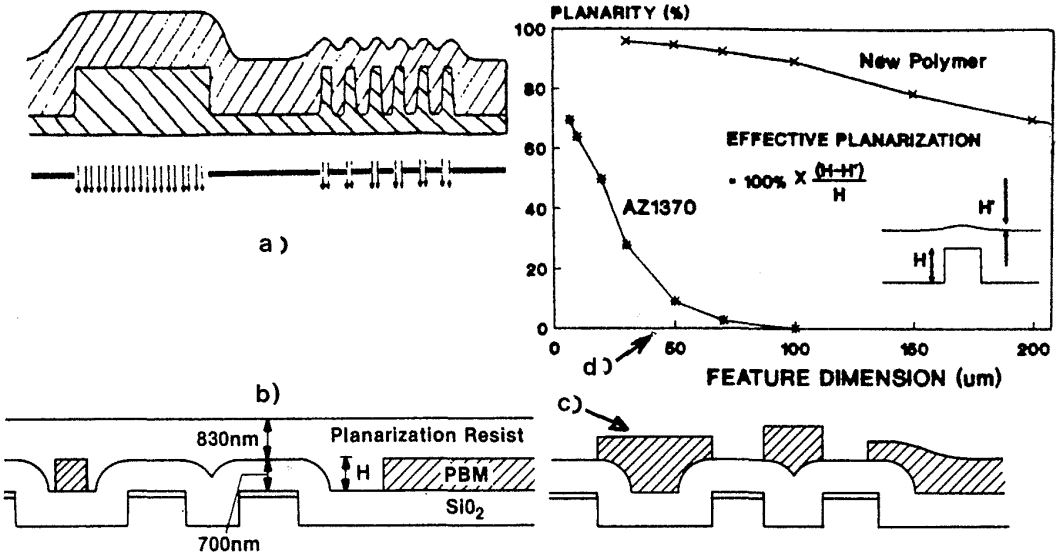

Fig. 4-26 (a) Step height at wide isolated features is not reduced by spinning on a photoresist because the resist thickness over the wide feature is the same as that over adjacent substrate areas. (b) A planarization block mask (PBM) together with an additional resist deposition have been used to overcome the problem of part (a).[67] (c) If the PBM mask is not properly compensated for underlying surface topography, a non-planarized final surface is still obtained.[228] This paper was originally presented at the Spring 1989 Meeting of The Electrochemical Society, Inc. held in Los Angeles, CA. (d) The effective planarization for the new polymer and AZ1370 versus width of the feature being covered.[249] This paper was originally presented at the Fall 1989 Meeting of The Electrochemical Society, Inc.

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during the etchback step, causing craters in the resist surface. These defects may be transferred to the dielectric surface by the etchback step, causing thin spots in the dielectric film.

When a heavy resist-erosion process is performed, the chamber may become contaminated with a polymer coating. As a result, the two-step process described earlier is typically used; in the first step, an oxygen plasma (which does not cause polymer formation) is used to erode the resist until the SiO_2 is exposed. Etch-gas mixtures that produce less polymerization are also employed to reduce this problem.

If the aspect ratio between adjacent Metal 1 lines with vertical sidewalls exceeds 0.4, voids will form when most CVD-SiO_2 layers are deposited. These voids cause resist and moisture trapping (and subsequent release when the voids are opened during the etchback process, as shown in Fig. 4-26b). Opened voids will also trap metal during the Metal 2 deposition step, which will remain in the form of metal stringers following Metal 2 patterning. Thus, this process is not feasible for Metal 1 spacings of less than ~1.25 μm unless a process is available for the deposition of SiO_2 layers at low temperatures without the formation of voids in high-aspect ratio spaces (e.g., ECR deposition of oxides, or PECVD TEOS films).

The plasma-etch chemistry must be adjusted during the etchback step, since the etch-rate ratio established from etch-rate measurements of unpatterned wafers will be different from that observed when oxide and resist are etched at the same time.[59] There are two reasons for the etch rate increase when oxide is simultaneously etched:[72] first, since less resist is exposed, the concentration of the reactive species (oxygen) is higher; second, once oxide etching has begun, the oxygen that is liberated as a byproduct ($SiO_2 + 4F \rightarrow SiF_4 + O_2$) may react with the resist, leading to enhanced resist etching. The magnitude of the increase, which can be up to threefold, depends on the percentage of oxide exposed surface. These effects are known as *global loading effects* (see Vol. 1, chap. 16). Typically, the etch chemistry is adjusted by reducing O_2 flow.

The etch-rate ratio is also sensitive to the pattern density on the wafer surface (this is known as a *local-loading*, or *micro-loading effect*). Etch-rate-ratio data should therefore be obtained from monitor wafers with a pattern density similar to that of product wafers. Reference 73 describes a multiple etchback process that takes the loading effects (both global and local) into account, thereby reducing planarity variations across the wafer.

4.4.8.4 Alternative Sacrificial Etchback Processes. Several alternative sacrificial-etchback processes have also been reported. One uses a spun-on AZ Novolac-resin protective coating (essentially positive photoresist without the photoactive compound) as a sacrificial layer, because it is less expensive and exhibits somewhat-better planarizing and dry-etching properties than do resists (Fig. 4-24). Such material is normally used to protect the wafer surface during back lapping and etching procedures.[64] A 200°C bake step after spin-on is recommended to improve the degree of planarization. Integration of a sacrificial-etchback process using such an AZ protective coating was reported for a 1.2-μm DLM-CMOS process.

Another method uses a dual CVD-oxynitride/nitride dielectric layer (deposited sequentially in a single chamber) plus resist.[74] Partial planarization is sought so that

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the via-depth variation is less than 0.25 μm. This is accomplished by selecting the appropriate oxynitride and nitride film thicknesses (0.55 μm and 0.85 μm, respectively) together with suitable etchback process conditions. The resist acts as a *complete* sacrificial layer, and the nitride as a *partial* sacrificial layer (which also fills the gaps between steps). Following the etchback process, all of the nitride is removed over the Metal-1 regions, but remains in the troughs between the steps. The oxynitride layer still remains over the Metal-1 steps following etchback, at essentially its originally deposited thickness.

The etchback step in this method is carried out in two parts, beginning with a gas mixture of $SF_6 + O_2$ that etches resist and nitride at the same rate. Only resist is removed initially, but eventually nitride over the narrow spaces is exposed. The second part of the etchback step is initiated once this occurs. The plasma chemistry is altered by deleting the O_2 from the feed gas because the only resist remaining on the wafer is in the narrow spaces between Metal-1 lines. It therefore etches more rapidly than when large regions of resist are being etched (microloading effect). By deleting O_2 from the plasma, the etch-rate ratio of resist to nitride is essentially returned to unity for this condition. The oxynitride layer is hardly etched by the etchback step, since the selectivity over nitride in SF_6 is ~5:1, allowing the nitride over Metal-1 regions to be removed without etching the CVD oxide. As a result, no redeposition after etchback is needed.

In the next example process, a CVD nitride/CVD oxide film with no covering resist layer is used as the sacrificial layer (Fig. 4-27a). A plasma-etch step which removes the nitride more rapidly than the SiO_2 and partially-planarizes the surface by leaving some unetched nitride in the grooves, is used. Once the oxide over the Metal-1 steps is exposed, the etch process is changed so that the nitride-to-oxide etch-ratio becomes unity (Fig. 4-27b). Etchback is continued until all the nitride is removed (Fig. 4-27c). Finally, an additional layer of CVD SiO_2 is deposited (Fig. 4-27d).[75]

In the last alternative method, the etchback process is integrated with a sloped-via-etch process, reducing the overall number of process steps.[76] A 2-μm CVD oxide is deposited, followed by resist deposition and via pattern exposure (Fig. 4-28a). The via pattern is anisotropically transferred into the SiO_2 by means of an RIE step (Fig. 4-28b) and an etchback planarization step is performed. The remainder of the via is etched during the etchback step, including tapering of its sidewalls.

4.4.9 Spin-On Glass (SOG)

Spin-on glass (SOG) is another interlevel-dielectric material that is applied in liquid form, and therefore exhibits planarization capabilities similar to those of polyimide films. SOG and polyimide films can both fill narrower spaces without causing voids than can CVD intermetal dielectric films. Even such crevices as those caused by closely spaced Metal-1 and polysilicon edges (Fig. 4-14b) can be planarized by SOG to a degree that allows for adequate metal step coverage. Other advantages of SOG films include: (a) simpler processing; (b) lower defect density; (c) higher throughput; (d) relatively low cost; and (e) no handling of hazardous gases.

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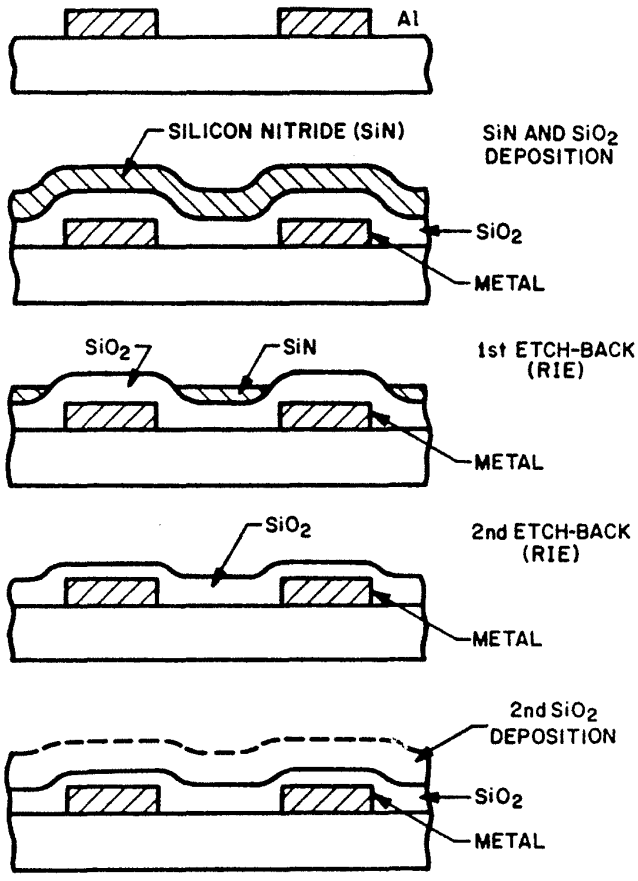

Fig. 4-27 Example of a sacrificial-etchback process that uses SiN as the sacrificial film.[75] (© 1983 IEEE).

SOG materials are *siloxanes* or *silicates* mixed in alcohol-based solvents, the primary difference between them being that a small percentage of Si-C bonds remains in the siloxane-based SOGs following the final cure cycle. Upon baking, the solvents are driven off and the remaining solid film exhibits properties similar to those of SiO_2 (as opposed to the organic film, in the case of polyimides). Silicate SOGs can also be doped with such compounds as P_2O_5 to improve the dielectric film properties. Case studies on the use of SOG materials can be found in references 77 and 78 (silicate based) and in references 79 and 80 (siloxane based).

Desirable properties of an SOG material are good consistency and shelf life, a simple cure cycle, excellent thermal stability, low stress and good crack resistance, spin-on uniformity, good adhesion, and an appropriate film-thickness range. Because the early SOG products, however, were proprietary mixes of organic monomers and attached organic groups mixed in solvents, it was difficult to predict their properties based on fundamental ideas of chemistry and materials science. The material properties of

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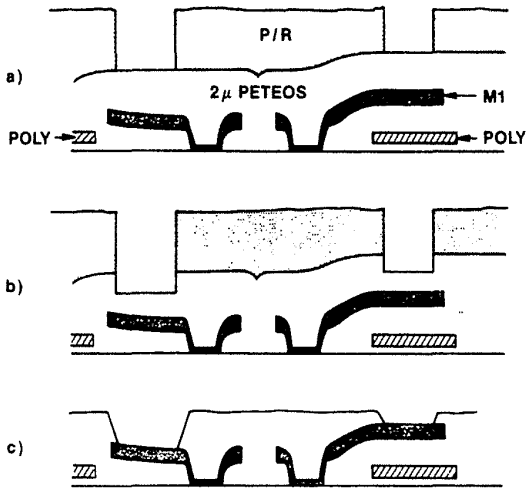

Fig. 4-28 Sequence showing how the etchback and via-sloping processes can be integrated to reduce the overall number of process steps.This paper was originally presented at the Spring 1988 Meeting of The Electrochemical Society, Inc. held in Atlanta, GA.

commercially available SOGs, however, have recently been described in more detail in references 81, 82, 83, 225, and 226 (siloxane based), and in references 84 and 225 (silicate based).

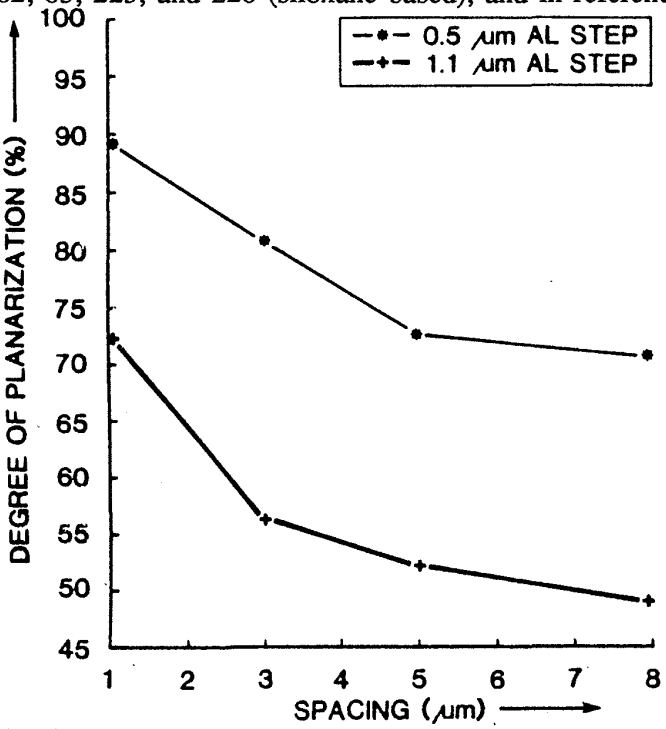

Fig. 4-29 Example of planarization by one type of SOG material as a function of spacing between steps. The underlying oxide step heights are 0. 5 and 1.0 μm.[77] (© 1988 IEEE).

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SOG films provide somewhat lower degrees of planarization than do photoresists. However, their smoothing effect on sharp, vertical edges is satisfactory; enabling good step coverage of Metal 2 lines without line width variation. Figure 4-29 shows the planarization capabilities of SOG films as a function of metal pitch. The planarization can be as high as 80% for very closely spaced features, while for larger spacings it drops to less than 50%.[85]

4.4.9.1 SOG Process Integration. SOG processing involves some special considerations. Since the solvents evaporate from the SOG very quickly after being dispensed, an optimum dispense/spin cycle must be developed so that adequate thickness uniformity can be obtained. The exhaust system is also very important for controlling film uniformity. In addition, the dispense nozzle must be cleaned frequently to prevent clogging, and the exhaust bowl must be rinsed so that any particles spun off the wafer will be washed away. Specially designed equipment is commercially available to meet these requirements (Fig. 4-30). A static dispense is recommended for coatings with thicknesses of 200-400 nm.

After being spun on, the SOG is baked first at a low temperature (e.g., 150-250°C for 1-15 min in air), and then at a higher temperature (e.g., 400-425°C for 30-60 min in air). The solvent is first driven off, and water is evolved from the film (due to polymerization of the silanol [SiOH] groups). The loss of considerable mass together with material shrinkage creates a tensile stress in the film. If too thick a layer is applied, the stress can lead to film cracking. Organic groups, such as methyl (CH_3) or phenyl (C_6H_5) have been added to siloxane films (from 1 to 12 wt% carbon) to improve

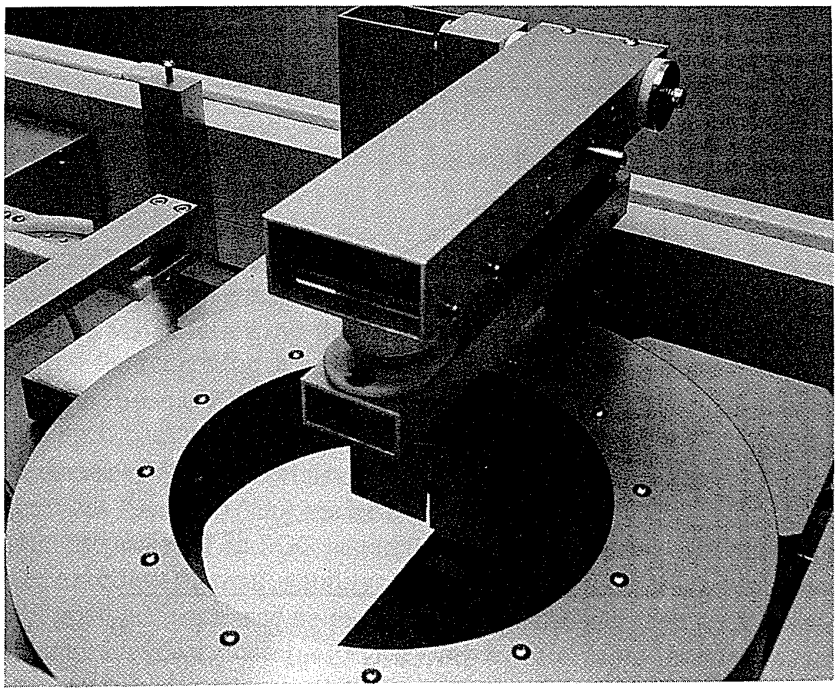

Fig. 4-30 Photograph of an SOG dispense nozzle. Courtesy of SEMIX, Inc.

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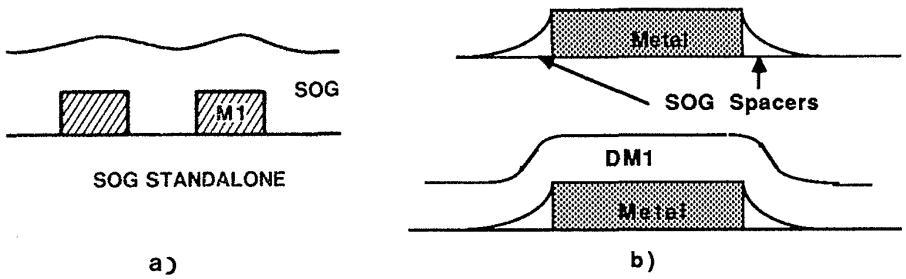

Fig. 4-31 (a) SOG standalone film. (b) Spin on SOG over underlying metal; etchback to leave SOG spacers; deposit DM1 oxide over this structure.

cracking resistance. (While a higher carbon content would be more effective for this purpose, it would also tends to degrade adhesion and steam resistance. Hence, a tradeoff is usually made in selecting an optimum carbon content.)[100] The simplest technique for integrating an SOG film into a multilevel interconnect process would be to use it as a stand-alone film (Fig. 4-31a). Unfortunately, when an SOG film is formed to the thickness required of an interlevel dielectric, it exhibits an intolerable degree of cracking. SOG can also be spun on over a CVD-oxide layer, or CVD SiO_2 can be applied over a thin spun-on layer of SOG; however, such approaches have also proved to be unworkable, since frequent adhesion failures are observed when SOG is in contact with metal or resist layers. In addition, resist stripping procedures may attack the SOG film and degrade its stability.[86] Still another technique involves deposition of an SOG film over a CVD oxide to smooth the surface. The SOG and oxide are then sacrificially etched back to leave gradually sloped CVD SiO_2 spacers, and a second CVD-SiO_2 layer is deposited over the metal/spacer structure (Fig. 4-31b).[87] This technique offers the benefits and drawbacks of the spacer semi-planarization method described in section 4.4.4.

The most widely reported implementations of SOG material involve *sandwich-type structures*, in which SOG is deposited over an initial CVD dielectric layer (*interlevel dielectric layer 1*, or ILD1), and a second CVD dielectric layer (ILD2) is then applied. There are two variations of this sandwich: *etchback SOG*, and *non-etchback SOG*. In the first technique, the SOG is partially etched back after being cured so that it remains only in the troughs between metal lines (Fig. 4-32a).[88,89,97,100] No SOG remains over locations at which vias will be etched. After the etchback step, ILD2 is deposited. In the *non-etchback SOG structures*, ILD2 is deposited over the SOG following curing. The SOG remains permanently as a continuous thin film between the two layers of CVD SiO_2 (Fig. 4-33).[90,91,92,93]

4.4.9.2 The Etchback SOG Process. Despite its greater complexity, the *etchback* approach has been more widely adopted, primarily because it avoids the so-called *poisoned-via problem* that can be encountered with the non-etchback method. The etchback method is normally implemented with the less crack-susceptible siloxane-based

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SOG films (the process sequence is illustrated in Fig. 4-32). Since sufficient planarization is normally not obtained with a single coating of SOG, two or more layers are often spun on before etchback is performed. A detailed description of an etchback SOG process is given in reference 255.

One drawback to the etchback process is that a thicker ILD1 film must be deposited than will ultimately remain, since some is removed during the etchback step. For a semi-recessed field-oxide thickness of 0.6 μm, a polysilicon layer 0.4 μm thick, and a 0.2-μm-thick SOG film, a 1.0-μm-thick ILD1 layer is needed. A minimum spacing of 1.2 μm is required between Metal-1 steps to prevent the formation of voids with a conventional-PECVD SiO_2 ILD1 layer. For smaller Metal-1 spacings, the etchback process becomes impractically complex with conventional PECVD ILD1 layers.

A plasma-TEOS/SOG process has been reported to allow spaces as small as 0.8 μm to be planarized by means of this etchback-SOG method,[94] with a 300-nm PECVD layer and a plasma-TEOS film used as a bilayer ILD1 film (fig. 4-32b). The plasma TEOS allows the small spacings to be filled without the formation of voids. The SOG is next applied to fill the "intermediate-width" gaps (i.e., near 2.5 μm) that are not sufficiently filled by the bilayer ILD1 film. Following an SOG etchback step, a thin ILD2 layer of PECVD SiO_2 is used to complete the sandwich structure. A second

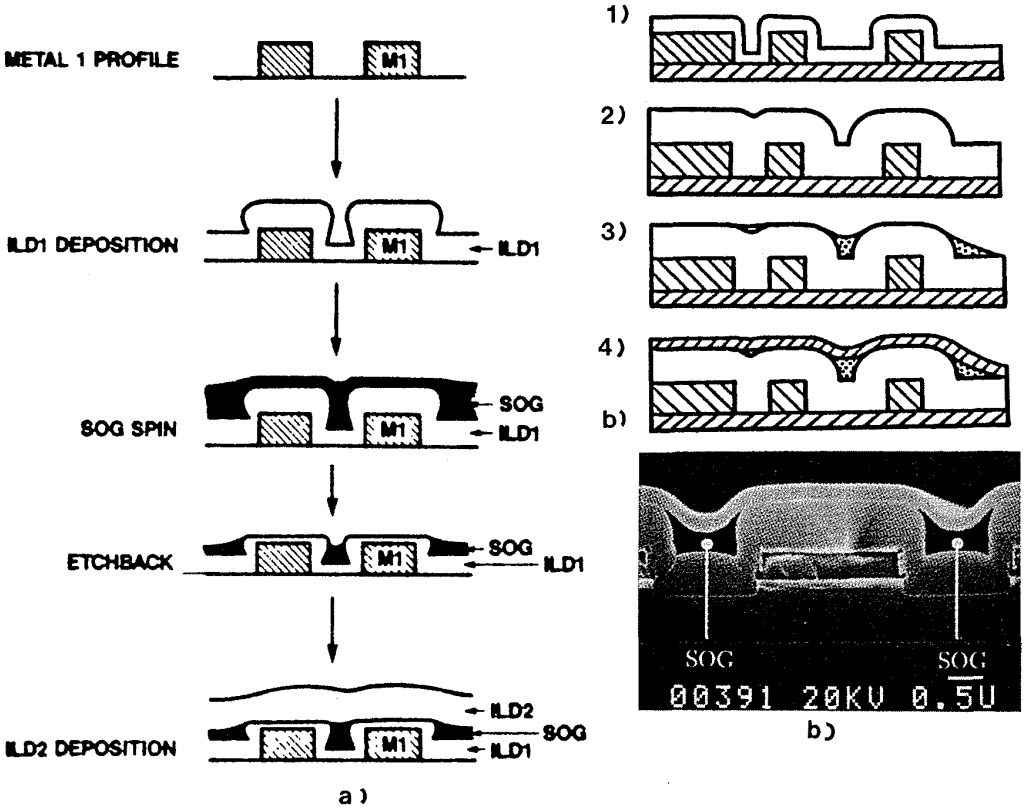

Fig. 4-32 (a) Sequence of steps used in the etchback SOG process. (b) Etchback SOG process which uses plasma TEOS as part of the CVD film that is first deposited. This allows smaller spaces between adjacent steps to be filled without void formation.[94] (© 1988 IEEE).

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method for increasing the step coverage of Metal 2 over these "intermediate gaps" is to cut the top edges of the Metal-1 Al lines, as described in section 4.4.2.4.[35]

Other problems of the etchback technique include:

- SOG-to-SOG adhesion problems are sometimes observed when more than one layer of SOG is used to improve the degree of planarization. The cause of SOG-to-SOG delamination is thought to be the slow out-gassing of the first SOG layer during the cure of the second layer, which pushes up the top layer.[95]
- Lifting of the SOG from small gaps, occurs due to stress caused by volume shrinkage of the SOG and poor adhesion to the ILD1 film.[95]
- Etch-rate differences exist between the SOG and the ILD1 layer (this problem is compounded by the added complication that the SOG etch rate is apparently also stress dependent);
- Microloading effects occur during the etchback step (similar to those described in the sacrificial etchback section).[96]
- The etchback process has a very small process margin for submicron technology. The CVD layer under the SOG must be thick enough to prevent Metal 1 from being exposed during the etchback step. The SOG thickness varies with topography and the amount of SOG to be removed has to include the thickest area where vias are allowed to be opened. A thick CVD layer will reduce the spacing between Metal 1 lines such that the SOG cannot flow in, or the CVD layer pinches off, leaving voids between the metal lines.

The use of polyimide instead of SOG in an etchback sandwich type structure has also been reported,[97] with good filling of small spaces (~1 μm) between Metal 1 lines observed. In this approach, an LPCVD oxide of 600-700-nm thickness is first deposited. At this thickness, the 1-μm spaces between metal lines are not yet pinched off by the deposited SiO_2 layer. Next, a 1.2-μm polyimide film is spun on and cured. This composite film is then etched back, using a process that compensates for the variation in oxide etch rate as the amount of oxide area is exposed.

A two-step etch process was developed for this application: (1) O_2 is used to etch the majority of the polyimide thickness (to reduce polymer-residue formation), and (2) simultaneous etchback of polyimide and SiO_2 is performed using a $C_2F_6 + O_2$ mixture. Following the etch process, a bakeout step is used to drive out any moisture from the polyimide remaining in the crevices. The bake step is followed immediately by the ILD2 deposition. Two and 3 levels of metal have been fabricated with this process.

4.4.9.3 The Nonetchback SOG Process. There are fewer steps with this process, and the difficult etchback step is eliminated. However, as noted, the non-etchback process suffers from the *poisoned-via* problem if siloxane-type SOG materials are used. During Metal 2 deposition, this type of SOG outgasses, causing higher contact resistance (e.g., 300-400 mΩ/via versus 60 mΩ/via for non-SOG controls) between

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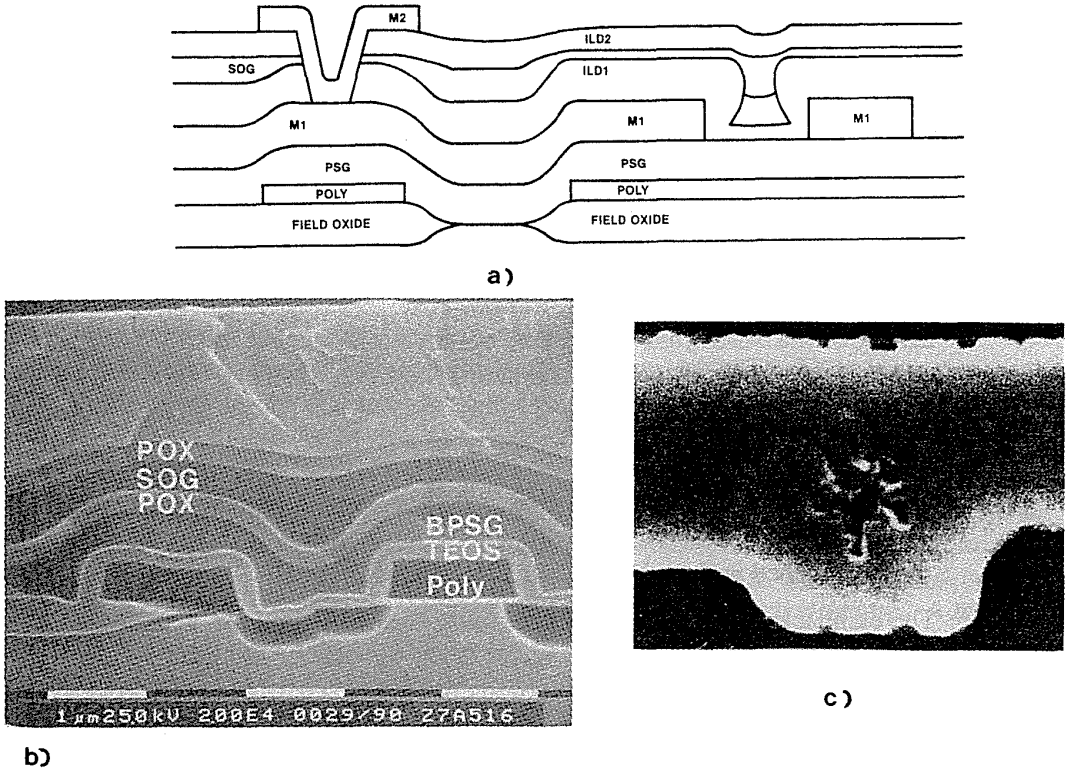

Fig. 4-33 (a) Drawing of a cross-section of structure formed using the non-etchback SOG process. (b) SEM micrograph of a structure formed with the non-etchback SOG process.[77] (© 1987 IEEE) (c) SEM micrograph of a cross section of a "poisoned via."[93] (© 1987 IEEE).

Metal 2 and Metal 1, or even an electrical "open" (Fig. 4-33c). The source of the gases has been found to be primarily moisture[253] that remains within the SOG (due to insufficient curing), or that has been reabsorbed during the wet process steps performed following spin-on and curing of the SOG film (e.g., during resist removal after the via etch or during pre-metal-deposition cleaning steps).

Although it has been suggested that the problem could be overcome through the use of an all-dry process sequence following SOG spin-on coupled with complete curing of the SOG film, most non-etchback approaches instead use a silicate-type SOG. Special crack-resistant silicate SOG materials (phosphorus doped to increase crack resistance) have been developed, since silicate SOG is inorganic. When such phosphosilicate glasses (containing ~9 wt% P_2O_5) are properly cured, the poisoned via effect is apparently eliminated.[91,92,93] Such nonetchback processes (with multiple coatings of SOG applied for adequate planarization) have been reported for Metal 1 spaces as small as 1 μm.[101] Two detailed reports of how a non-etchback phosphosilicate SOG process was integrated into a 1-μm CMOS processes for both polysilicon and first metal interconnect planarization is given in references 245 and 246.

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4.4.10 Electron-Cyclotron-Resonance Plasma CVD

Electron-cyclotron-resonance (ECR) plasma CVD SiO_2 and silicon-nitride films are being investigated as another method for planarizing intermetal-dielectric layers.[102,231] The most significant advantages of ECR-deposited dielectric films are their low deposition temperatures (i.e., room temperature to 150°C) and their apparent capability to fill higher aspect-ratio spaces than either PECVD or bias-sputtered CVD. This latter characteristic allows ECR oxides to fill spaces as small as 0.5 μm wide.* In addition, it has been observed that ECR oxide and nitride films contain lower concentrations of hydrogen and exhibit other promising physical properties.

ECR plasmas are capable of producing such films because they can operate at pressures an order of magnitude lower than conventional rf plasmas (i.e., at 1-2 mtorr pressure). The ECR plasma is generated at microwave frequencies of 2.45 GHz. For SiO_2 deposition a gas mixture of SiH_4, O_2, and Ar is metered into the reaction chamber (Fig. 4-34). Magnetic fields surrounding the microwave cavity produce a field gradient that directs the ions of the plasma to the surfaces of the wafers (which can either be maintained at room temperature or heated). The densities of the extracted ions are an order of magnitude higher than those observed in conventional tubular or parallel-plate PECVD reactors.

Bias is also applied to the wafers if a planarized dielectric layer is desired. Planarization is achieved during deposition through essentially the same mechanisms that are operative in bias-sputtered SiO_2 (i.e., CVD-SiO_2 deposition occurs simultaneously with sputter etching of the growing film by argon ions). This, combined with the low operating pressure of the plasma, allows small, high-aspect-ratio spaces to be filled. The high ion densities allow greater throughputs than are possible with bias-sputtered SiO_2 processes, but they are still rather low. Reports on the dielectric

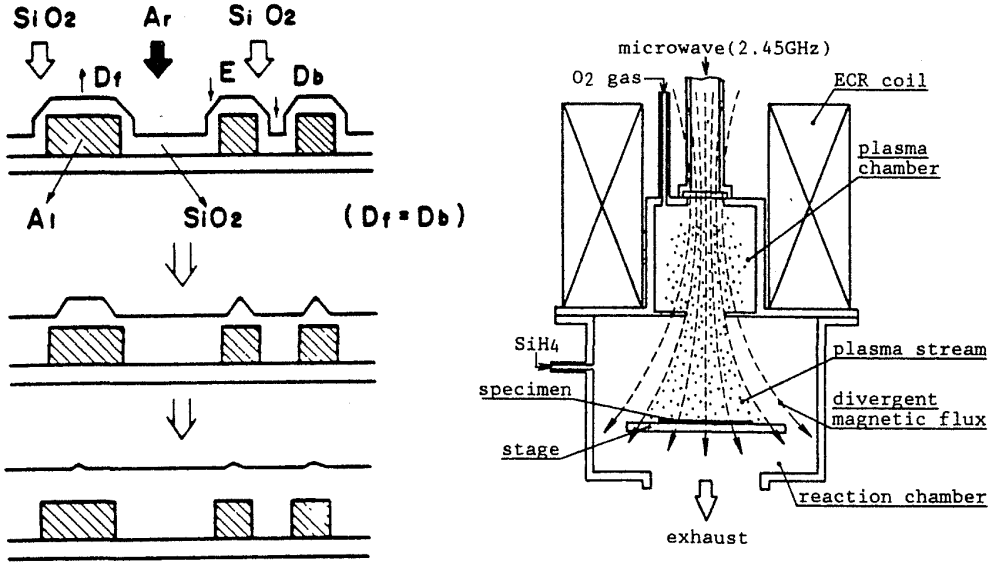

Fig. 4-34 (a) Principle of bias-ECR plasma CVD; (b) ECR plasma CVD apparatus.

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properties of ECR silicon-oxide and silicon-nitride films are given in references 103, 104, and 105.

It has been observed that the physical properties of the ECR films are better than those obtained with conventional PECVD processes. However, the step coverage can be very nonconformal, and the sidewall films can be quite porous if the film is deposited without rf bias.

Films deposited in conventional ECR machines exhibit non-uniform thickness, especially on large wafers (≥150 mm), due to the divergent magnetic field that extracts the ions from the microwave cavity. The modified magnetic coils of more recently designed machines make it possible to produce films with ±5% thickness uniformities across 150-mm wafers.[106]

A system that uses ECR to generate a plasma with oxygen gas (instead of Ar) has been reported for sputtering layers of SiO_2 by formed CVD in the same chamber.[261] The oxygen ions sputter the SiO_2 (formed earlier by reaction of SiH_4 and O_2) to achieve planarization. This can be achieved without applying a dc bias the substrate or by having self-bias develop between the wafer and the plasma. That is, an rf signal at 400 kHz is applied to the substrate. The impinging oxygen ions from the plasma can follow this electric field, and thus bombard the surface without having a self-bias build up on the substrate. Electrostatically-caused damage (due to the buildup of charge on the wafer surface as a result of self-bias) is thus prevented, while the sputtering needed to achieve planarization still occurs. High sputtering rates of SiO_2 films with low damage have been reported.

4.4.11 Chemical-Mechanical Polishing

The sacrificial-resist etchback process, even with a compensated-PBM resist layer, still has severe problems for multilevel metal applications. The deposition and etchback tolerances associated with large film thicknesses are cumulative, and any non-planarity of the resist is replicated in the final planarized oxide surface. Under RIE etchback conditions designed to reduce such non-planarities (i.e., the oxide/resist etchrate ratio is increased to more than 1.0), oxide spikes are caused (Fig. 4-35a). A chemical-mechanical polishing (CMP) process has recently been reported for removing such spikes.[265] The CMP process can rapidly remove such small elevated features without significantly thinning the oxide on the flat areas (Fig. 4-35b). It is pointed out that the CMP process alone is not viable for planarization because residual oxide will be left in the middle of large active areas or arrays after polishing (Fig. 4-35c). By using CMP and etchback planarization, however, an effective planarization method can be achieved.

Not many details about CMP technology have been published as of this writing, but references to silicon wafer-polishing techniques have been cited.[266] To prevent mechanical work damage from remaining on the polished film, the chemical component of the polishing should probably dominate. Since the wafers will likely be polished one at a time, the throughput is also likely to be low (e.g., on the order of 5-10 wafers per hour). Other predicted problems include the clean-up of the polishing-slurry particles from the wafer surface (slurry-particle size <0.1 μm), the question of how to make

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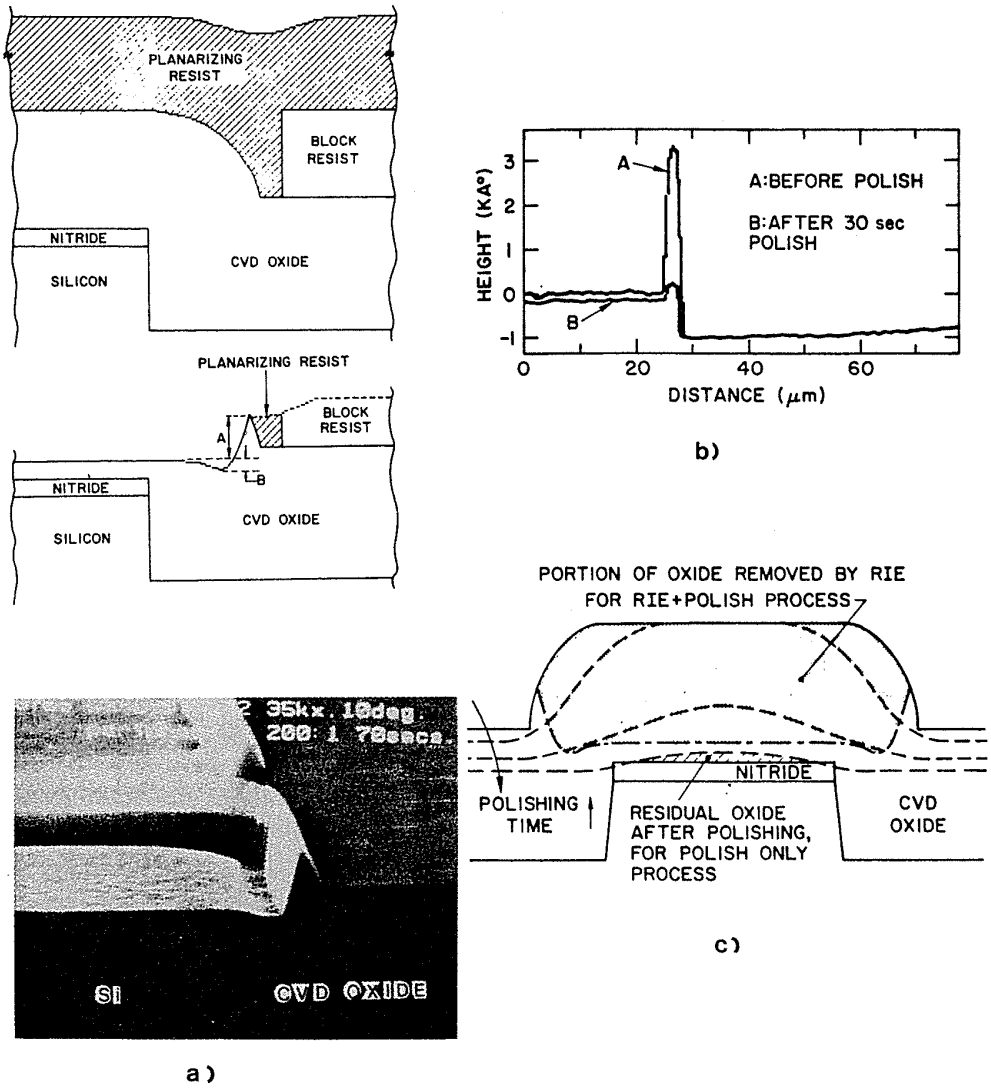

Fig. 4-35 (a) Cross section after selective RIE etchback, showing local oxide spikes that remain after the etchback when the oxide/resist etch-rate ratio > 1. (b) Measured oxide step heights before and after CMP, showing the fast removal rate of such spikes. (c) Schematic drawing showing the fundamental problem of "CMP-only" planarization.[264] (© 1989 IEEE).

such a dirty process compatible with the clean room environment (i.e., reducing the density of the 50,000 to 100,000 particles/ft^3 generated, to less than 50/ft^3), the lack of an end point detection method, and maintaining sufficient polishing-rate uniformity across the wafer, and from wafer to wafer. Commercially available equipment for performing this process is reportedly being developed.

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4.5. METAL DEPOSITION AND VIA FILLING

4.5.1 Conventional Approach to Via Fabrication and Formation of Metal-to-Metal Contacts through Vias

One aspect of minimum feature size that applies to via fabrication is the issue of the via sidewalls: for the same contact-opening sizes at the bottom of vias, straight sidewalled vias would require less area than would those with sloped sidewalls. Furthermore, when dry etching is used to open the vias, it is often easier to produce straight rather than sloped sidewalls.

Unfortunately, when physical vapor deposition is used to deposit metal over the vias, straight sidewalls result in worse step coverage by the metal than if the sidewalls were sloped. This has been shown both theoretically[117] and experimentally (Fig. 4-36a).[118] While adequate step coverage of the metal is critical, there is no single value of minimum step coverage that is considered adequate for all conditions. This is because the minimum value depends on many factors (including the current density passing through the metal, its absolute film thickness at the thinnest spot, the type of metal, etc.). In general, a range of 20-50% minimum step coverage is probably acceptable, depending on the application.

The step coverage of a sputtered metal film can be improved in a number of ways. The first is to optimize the deposition conditions by increasing the surface-migration ability of the atoms that have already arrived on the surface. These atoms will then

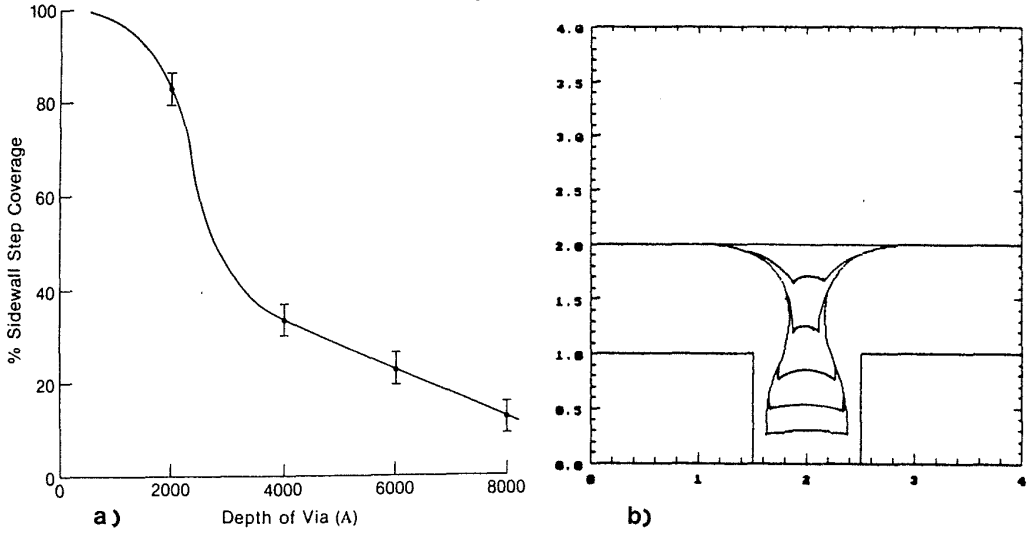

Fig. 4-36 (a) Percent sidewall step coverage of a standard dc sputtered aluminum film (0.8-μm thick) into vertically-sided 1.2-μm-diameter vias of different depths.[118] Copyright 1986. Reprinted with permission of the AIOP. (b) Simulation of a sputtered Al film into a via with an aspect ratio of 1.0, with the via being partially filled and unfilled. The profiles form the top represent the metal film deposited into a 100% filled, 80% filled, 60% filled, 40% filled, 20% filled and unfilled via.[249] This paper was originally presented at the Fall 1988 Meeting of The Electrochemical Society, Inc. held in Chicago, IL.

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rearrange themselves until the film has a uniform thickness over all topographical features. Surface mobility can be increased by raising the substrate temperature and by increasing ion bombardment (which also causes heating, since a large fraction of the incident energy flux is transferred to the film/substrate as heat). Sputtering processes that are capable of heating the wafers during deposition and causing them to be bombarded by ions (i.e., through bias sputtering; see Vol. 1, chap. 10) have been shown to produce improved step coverage. *Assuming that a sputtering process is developed that optimizes step coverage, however, the coverage will still depend on the sidewall slope and aspect ratio of the via.*

The aspect-ratio dependence of the step coverage into contact holes and vias is critical as feature sizes are scaled into the submicron regime. In order for the interlevel capacitance of the interconnections to the underlying and overlying metallization lines to be maintained (or even reduced), the thickness of the dielectric layers in which the contact holes and vias are formed may not be decreased at all. Thus, the aspect ratio will grow larger. For example, when an Al film is sputter deposited without bias and at <300°C, the step coverage into a vertically-sided via whose aspect ratio is 0.5 is typically ~20%. As the aspect ratio increases to 1.0 (so that the via depth equals the width), the step coverage decreases to less than 5%.

An example of a simulation of a sputtered Al film into a via with an aspect ratio of 1.0 is shown in Fig. 4-36b. (Another example of step coverage that has been reported as a function of aspect ratio is given in Fig. 3-27b.) As shown in Fig. 4-36, sputtered-Al depositions used in production processes in 1988 provide more than 50% step coverage into vertically sided vias only if the aspect ratio is smaller than 0.25 (e.g., for 1.2-μm-wide vias, the depth can be no more than 0.3 μm). Since the thicknesses of the PMD and DM1 layers generally exceed 0.5 μm each, adequate step coverage may not be achieved for small vertically-sided vias.

The conclusion to be drawn from the above discussion is that in *conventional via processing, sloped vias are necessary to ensure adequate step coverage in most applications when contact holes and vias are less than 1.5 μm wide.*

Two other important aspects of conventional via processing are the planarization of the intermetal-dielectric films and the decision of whether the design rules are to allow *stacked vias* (i.e., vias located on top of silicon and polysilicon contacts) or only *staggered vias* (Fig. 4-37a). As shown in Fig. 4-37b, if complete planarization of DM1 is achieved and if stacked vias are also permissible, via depths can vary by as much as 1 μm. Such large variations have two significant impacts on the via fabrication process. First, the deepest vias will have poor (and generally inadequate) step coverage unless sloped sidewalls are formed. Second, since a sloped-via process must be used, the Metal-1 patterns under the shallowest vias must be wide enough to prevent the etching of grooves along the pattern sidewalls when the deep vias are being opened (Fig. 4-38a). This increase in pattern size results in an area penalty that can significantly decrease packing density.

In general, in the earliest double-level-metal (DLM) processes for CMOS, conventional via processing was employed. The rules that had to be followed because of the difficulty in filling vertical vias included these:

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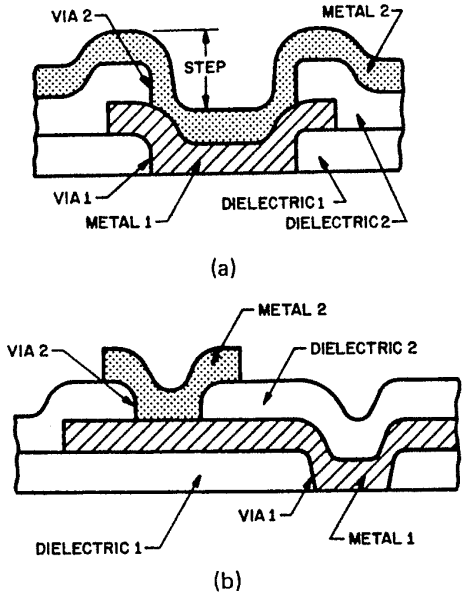

Fig. 4-37 Contact schemes: (a) stacked vias; and (b) staggered vias. From A. G. Sabnis, in G. S. Gildenblat and S. S. Cohen, Eds., *VLSI Electronics: Microstructure Science, Vol. 15, Metallization,* Chap. 7. Copyright 1987, Academic Press. Reprinted with permission.

- No step-height reduction planarization process could be used with respect to PMD and DM1 layers (i.e., only the first degree of planarization – *smoothing* –was employed), so that all vias could be maintained at the same depth.
- Only staggered vias were allowed.
- Contact to Metal 2 was allowed only through Metal 1.
- The vias had to be sloped to allow adequate step coverage by sputter-deposited metal.

However, vias with sloped sidewalls give rise to a set of design rules that must be followed when laying out patterns of the metal and via structures in a multilevel metal system.

4.5.1.1 Design Rules of Multilevel Metal Systems which are Impacted by Conventional Via-Processing Limitations. In the ideal case, metal pitch is determined by the minimum line and space dimensions that can be patterned using the most recent advances in lithographic techniques. In practice, metal pitch is also limited by the via size and the underlying metal pad size. The following design rules must thus be obeyed:

- The underlying metal pad must be larger than the via opening. This condition is referred to as a *framed* or *nested via*. If the via were larger than the metal pad, grooves would be etched alongside the pad during the via-etch step (Fig. 4-38a)

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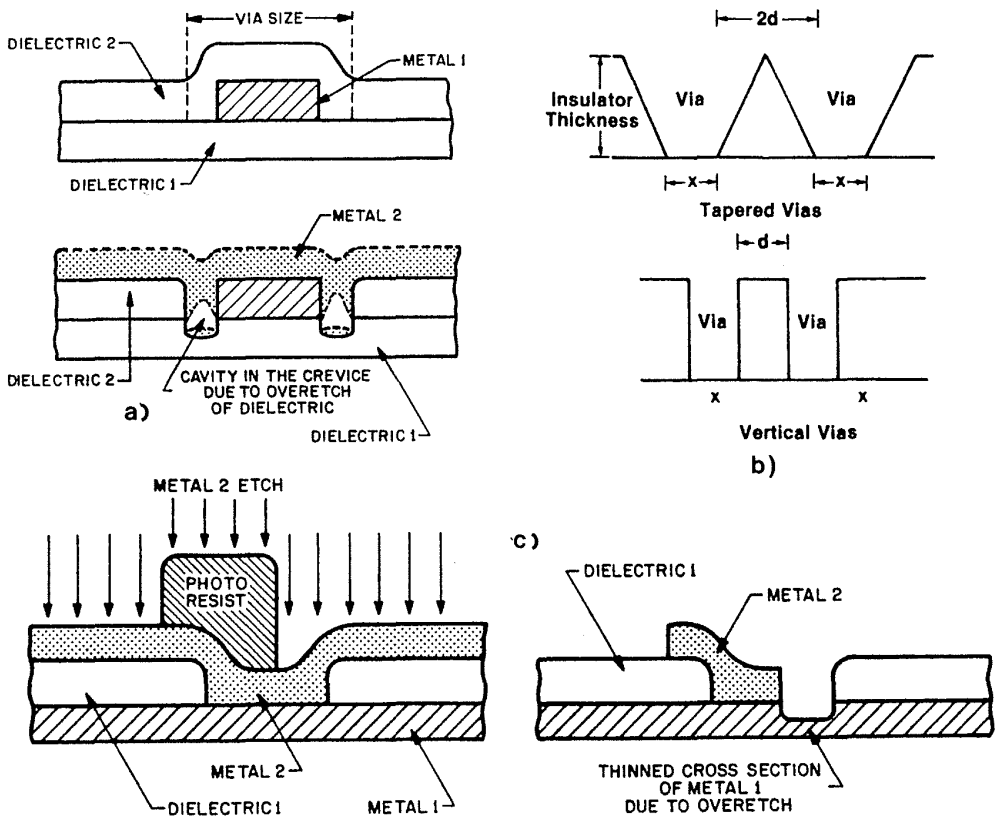

Fig. 4-38 (a) If the via dimension in the direction of the Metal-2 current flow is larger than the Metal-1 width, then crevices may be formed into the dielectric below Metal 1, and cavities can result in Metal 2. (b) If sloped vias are used, the minimum spacing between vias must be larger than if vertical vias are used. (c) If the via dimension in the direction of Metal 1 current is larger than the Metal-2 width, then Metal 1 can get overetched, thus the overlying metal must be larger than the top of the via opening. From A. G. Sabnis, in G. S. Gildenblat and S. S. Cohen, Eds., *VLSI Electronics: Microstructure Science, Vol. 15, Metallization,* Chap. 7. Copyright 1987, Academic Press. Reprinted with permission.

and could cause microcracking or thinning of Metal 2 when it is deposited over the via to contact Metal 1. The minimum dimension by which the metal pad must frame the via is dependent on the misalignment tolerances of the lithography step. If vias with varying depths must be etched, the enlargement that will occur when shallow-sloped vias continue to be etched during etching of the deep vias must also be taken into consideration.

• The slope of the vias must be taken into account when deciding on the minimum spacing between vias (Fig. 4-38b). A minimum space is needed between the tops of the etched via openings so that metal space on this horizontal surface can be reproducibly patterned.

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• The overlying metal pad must be larger than the top of the via opening to ensure full coverage of the via (Fig. 4-38c).

4.5.2 Advanced Via Processing (Vertical Vias and Complete Filling of Vias by Metal)

As long as an adequate sidewall taper of contact windows and vias can be implemented (and the aspect ratios do not become too great), sputter deposition can produce metal films with adequate step coverage into vias. However, design rules are rapidly evolving to a point at which sputtered metals will no longer be able to acceptably fill contact and via holes. In addition, in submicron technologies the extra area needed to accommodate sloped vias severely limits the maximum packing density (particularly since it is also difficult to tightly control the slope of the sidewalls in a production environment).

Finally, if sputter etching is used to clean the native oxide from the Al at the bottom of the vias prior to deposition of the next Al film, SiO_2 from the via sidewalls will be redeposited in the bottom, causing contact resistance problems. The problem is minimized through the use of vertically sided vias (or vias with a slight sidewall slope, e.g., 85°). Once the limits that mandate the use of such vertically-sided vias have been reached, *advanced via processing* (in which it is possible to completely fill vertical vias with metal) must be used.

4.5.2.1 Increases in Packing Density Resulting from Advanced Via Process Technology. Several space saving benefits are achieved through the use of this technology. First, the minimum distance between adjacent metal lines at the via is reduced, since the via has no slope (Fig. 4-38b). Second, the pad area of Metal 2 can be decreased, since the plug in the completely filled via provides ample overetch protection to underlying metal structures without mask coverage (Fig. 4-39a).

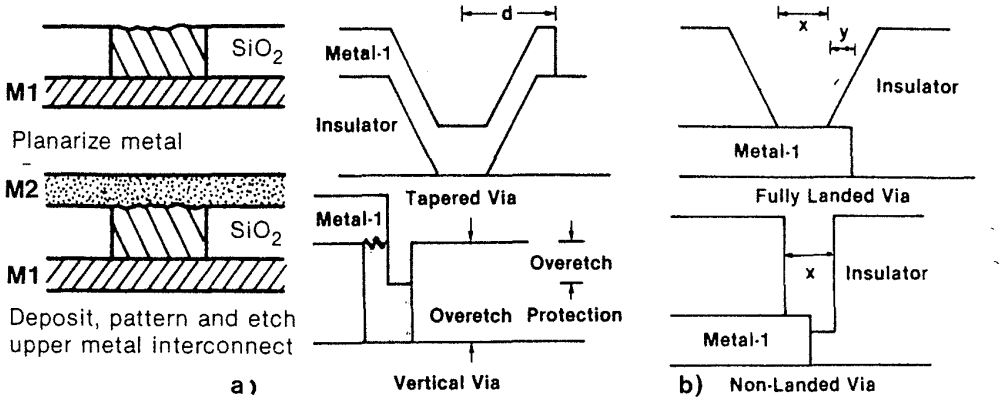

Fig. 4-39 Metal 1 and Metal 2 pad areas can be smaller when vertical vias and fully filled vias are used because: (a) such filled openings provide protection during any overetch that may occur during the etching of Metal 1 or Metal 2; (b) any grooves that may be created during the overetching that occurs when the via openings are etched are easily filled by the via-filling process.[128] (© 1987 IEEE).

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Third, the minimum size of the Metal 1 pad areas can be reduced, since any small grooves that might be etched alongside the pad during the via etch will be easily filled during the plug formation process (Fig. 4-39b). As a result, the pitches of both Metal 1 and Metal 2 can be reduced, allowing significantly increased packing density.

4.5.3 Processing Techniques that Allow for Vertical Vias

Two general fabrication approaches make the implementation of vertical vias possible:

1. *Filling of vias through deposition of metal into the opened via to form* a *plug in the opening.* In theory, this can be accomplished either independently of the metal-runner formation process, or through simultaneous fabrication of the plugs and metal runner. An example of the latter is the deposition and patterning of a blanket CVD W layer.

   On the other hand, when the plugs are formed separately, it is not necessary to replace the Al interconnect runners with those of a higher resistivity metal (W). Conversely, W contact plugs do not significantly increase the total resistance of interconnect lines because their length is so short (and because they maintain a large cross-sectional area): hence, they are appropriate for this use.

2. *Creation of a post, or pillar, which is then surrounded with a dielectric.*

Although the post approach offers several layout advantages, the plug approach is much easier to implement in a production-worthy process. Nevertheless, we will discuss both approaches.

4.5.3.1 Required Degree of Via Filling by Plugs. Although the plug structures described in the previous paragraphs will completely span the cross-sectional area of the contact holes or vias, they may not fill the openings up to the top. However, as noted earlier, adequate step coverage (e.g., >50%) by PVD metal into a vertically sided opening can still be achieved if the aspect ratio of the opening is less than 0.25. Step coverage by means of sputtered Al can thus be adequate under some circumstances, with more than 50% coverage possible in 1.2-μm wide, vertically sided, 600-nm-deep vias with 300-nm plugs. Figure 4-36b shows the step coverage of a 1.0 μm metal film into partially filled vias.[249]

4.5.4 CVD W Techniques for Filling Vertical Vias and Contact Holes

Two CVD W methods that have been developed for this application are *blanket CVD W and (etchback)* and *selective CVD W.*

4.5.4.1 General Information on the CVD Tungsten Process. The chemical vapor deposition (CVD) of tungsten is generally performed in either a hot-

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wall, low-pressure system or a cold-wall, low-temperature system. Although tungsten can be selectively deposited either from WF_6 or WCl_6, the former (tungsten hexafluoride) is better suited as the W source gas, since it is a liquid that boils at room temperature (while WCl_6 is a solid that melts at 275°C). WF_6 can also be reduced by silicon, hydrogen, or silane, as shown by the following equations:

Silicon reduction

$$2WF_6\ (\text{vapor}) + 3Si\ (\text{solid}) \rightarrow 2W\ (\text{solid}) + 3SiF_4\ (\text{vapor}) \qquad (4 - 12)$$

Hydrogen reduction

$$WF_6\ (\text{vapor}) + 3H_2\ (\text{vapor}) \rightarrow W\ (\text{solid}) + 6HF\ (\text{vapor}) \qquad (4 - 13)$$

Silane reduction

$$2WF_6\ (\text{vapor}) + 3SiH_4\ (\text{vapor}) \rightarrow 2W\ (\text{solid}) + 3SiF_4\ (\text{vapor}) + 6H_2\ (\text{vapor}) \qquad (4 - 14)$$

When the hydrogen reduction is used, the rate-limiting step is the dissociation of H_2 into atomic hydrogen on the reaction surface. Selectivity is therefore achieved through deposition at a temperature below which SiO_2 will not catalyze the H_2 dissociation (~500°C), but at which other surfaces (silicon, metal, and silicide) will do so. If the entire surface is covered with a material that forms a good nucleating surface, the W will be deposited everywhere even when temperatures are below 500°C (*blanket W deposition*). If the nucleating surface exists only in certain locations (e.g., at the bottom of contact holes or vias), W will be selectively deposited in those locations. Above these temperatures, however, W will deposit on the SiO_2 as well. If the silane reduction is used, selectivity can be reproducibly achieved if the temperature is kept below 325°C, but it will be lost if the SiH_4/WF_6 flow-rate ratio is greater than 1.6.

On a silicon surface, the deposition starts with the silicon-reduction reaction (Eq. 4-12) even when hydrogen is present, and it will occur exclusively if hydrogen is absent. This reaction is self-limiting, however, since once a W layer is deposited it serves as a diffusion barrier between the Si and WF_6; the silicon reduction essentially stops when the W film reaches a thickness of 10-15 nm. For every two atoms of W deposited, three atoms of Si are consumed and volatilized as SiF_4. Typically, 10 to 15 nm of Si are consumed. No deposit occurs on the SiO_2 during the reaction. The silicon reduction of WF_6 can be used to produce thin films of selectively deposited W, with excellent surfaces and with sheet resistances of 10-15 Ω/sq.

The *hydrogen reduction process* can be used to selectively deposit thicker CVD W films, as was first reported by Blewer and Wells.[120] Normally, the silicon reduction reaction deposits the initial thin layer on a Si surface, and the hydrogen reduction then reaction takes over. As a result, the carrier gas at the outset the of this type of deposition is normally Ar. After the Si reduces the WF_6, either H_2 or SiH_4 is added to the gas flow, and the Ar flow is stopped.

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When used to deposit W into contact and via holes through the blanket deposition method, hydrogen reduction gives excellent conformal coverage of the topography (which results in near-complete contact hole and via planarization). Broadbent and Ramiller studied the deposition kinetics of the hydrogen reduction of WF_6.[121] In this study, which spanned the temperature range of 250-500°C and the pressure range of 0.1-5 torr, an activation energy of 0.71 eV was obtained for all pressures. The growth rate was found to be independent of WF_6 partial pressure, but was observed to increase as the square root of the H_2 partial pressure. These dependencies suggest that *surface-adsorbed H_2 dissociation* is the rate-limiting reaction mechanism. The activation energy of 0.71 eV is in close agreement with the value of 0.69 eV for the H_2 surface diffusion of W. A more recent report of the kinetics of the hydrogen reaction is given in references 122 and 123.

The hydrogen reduction process, however, has several drawbacks. First, the deposition rate is relatively low (e.g., ~8 nm/min at 350°C), especially at the low deposition temperatures necessary when the CVD W process is used to fill via holes in which Al is the underlying metal layer. Second, the surface of such thicker deposited films is quite rough, with surface features 25% taller than the film thickness. (One report indicates that the surface roughness can be reduced through the use of a clean reactor, if a hot-wall furnace is used for the deposition process.)[110] Finally, the HF gas by-product of the reaction is believed to be responsible for the problems of encroachment under the oxide, as well as for wormholes which lead to junction leakage.

The *silane reduction process* was developed as a way to overcome the problems of the hydrogen reduction process.[124,125] High deposition rates can be achieved at low temperatures (up to 600 nm per minute at 250°C has been observed, with no loss of selectivity). In addition, the grain size of the deposited films is much smaller than that obtained with the hydrogen reduction process, resulting in much smoother W-film surfaces. Finally, since no HF gas is produced as the reaction by-product, the problems of encroachment and wormholes are also apparently eliminated. Note that the deposition temperature must be kept below 325°C so that selectivity can be maintained. The resistivity of silane W films produced by silane reduction is comparable to the 13 $\mu\Omega$-cm of W films produced by hydrogen reduction. Low and stable contact resistances to both *p* and *n* type silicon are also formed. A process for selective W CVD in a hot-wall reactor by silane reduction of WF_6 has recently been described.[254] The advantage of using a hot-wall reactor is that it can accommodate a larger number of wafers than can cold wall reactors.

4.5.4.2 Blanket CVD W and Etchback. Due to lateral encroachment and wormholes - problems that exist with selective CVD W deposited with the hydrogen reduction - blanket CVD W and etchback has been more widely adopted for contact hole and via filling (at the penalty of using a higher cost process).

The process is normally begun by depositing a 100-nm-thick adhesion layer on the wafer surface (e.g., Ti, Ti:W, TiN, WSi_x, or Ti/TiN).[126,127,128,129,243] Such adhesion layers are needed because of the extremely poor adhesion of CVD W on such insulators as BPSG, thermal oxide, and plasma-enhanced oxide and silicon nitride.

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Tungsten, however, will adhere well to these materials, and they in turn will adhere well to the insulators listed. Thus, a method which allows good adhesion of CVD W to the substrate is achieved.* Next, a layer of CVD W is blanket deposited. This can be accomplished using silane reduction. (A WSi_2 layer can be deposited as part of the silane-reduction deposition process. Since this is done in situ, the W can be deposited after the WSi_2 layer without the need to break vacuum.) As the deposition proceeds, the sidewalls of the vias are covered by the conformal CVD W film and they eventually become thick enough that they come into contact with one another. In the ideal case, the holes are thereby filled (Fig. 4-40a); in practice, however, the voids created when PVD processes are used to fill vias can still occur under some CVD W conditions (Fig. 4-40b). Process optimization of deposition temperature, pressure, and relative gas flows, however, can minimize or eliminate void formation.

The silane reduction process is more prone to void formation, probably because of its faster deposition rate. A combined hydrogen and silane reduction process has been reported as a means of eliminating void formation. The process has a deposition rate faster than that of the hydrogen reduction process alone, but still allows the establishment of a set of deposition conditions in which no voids form.[130] In another report, this combined process was used to fill vias through deposition of W at 400°C. This resulted in sufficiently high W deposition rates, and limited the growth of hillocks in the underlying Al films.[131]

Since a blanket W film is deposited everywhere, it must be etched back so that it remains only in the vias. The simplest way to do this is to etch back the W directly, without using a sacrificial resist layer. When vias of varying widths must be filled, however, the "dimples" that occur at the center of the W-filled vias (Fig. 4-40c) will be deeper in those that are wider and will also be replicated into the final film. In some cases, faster etching of W will occur along the seam. When a metal layer is deposited over these via plugs, poor step coverage may result.

Use of a planarizing resist layer has been suggested to overcome this limitation. If a 1:1 resist-to-W etch-rate ratio can be achieved – not an easy thing to do – such an etchback process could be used to planarize both wide and narrow vias. One study abandoned this approach in favor of the direct etchback process.[132] Another group reported success[119] by using an RIE etch-gas mixture of $CCl_2F_2 + O_2$ to obtain a 1:1 selectivity between W and resist (Fig. 4-41). Nevertheless, it was indicated that both high W film-thickness uniformity and high etch-rate uniformity are necessary for successful implementation of this process.

In another report, a polyimide film was used instead of resist as the sacrificial layer.[131] Still another group reported a two-step etchback process.[224] In the first step,

* TiN has been reported to have the best set of properties for this adhesion-layer application, including the lowest contact-resistance values – two orders of magnitude lower than when Ti is used – and the best resistance to the etch gases used to etch the CVD W.[130] In another report, WSi_x was found to yield poor W adhesion in submicron contacts, so Ti:W was used instead.[230] The Ti/TiN layer was used in a two-level metal process in which it also served as a contact to regions of silicon and polysilicon covered with $TiSi_2$.

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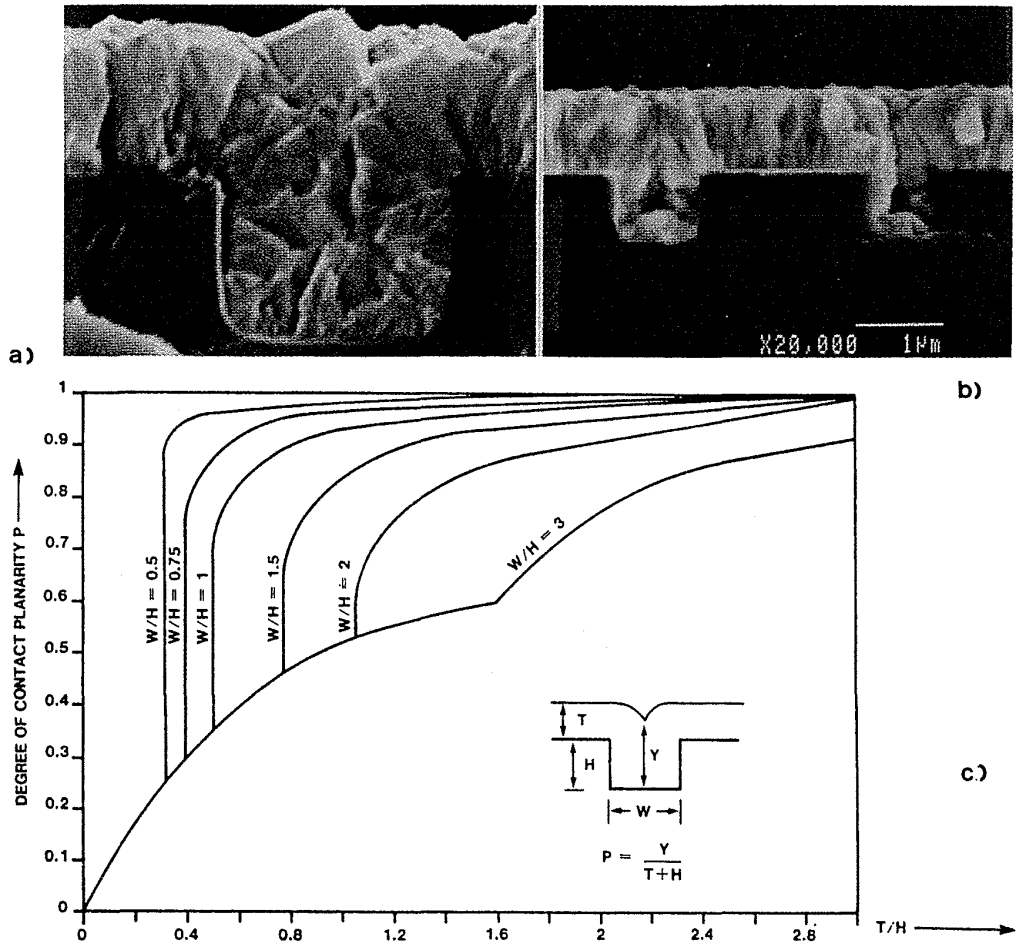

Fig. 4-40 (a) CVD W filling of contact hole without void formation. (b) SEM micrograph of voids that may form when CVD W is deposited into contact openings. (c) "Dimples" that are formed when CVD W is deposited into contact holes and etched back.[128] (© 1987 IEEE).

an SF_6 and C_2F_6 mixture was used to etch the W and the resist at similar rates (400 nm/min). The C_2F_6 acts to reduce the microloading effect in which the W etch rate increases as the amount of W exposed decreases during etching decreases. In the second step, residual W and the TiN adhesion layer are removed with a Cl_2-based plasma. The TiN is removed preferentially with respect to W and the underlying SiO_2. To eliminate metallic residue, an appreciable overetch is carried out, without excessive loss of W in the vias or of interlevel SiO_2.

In both types of etchback processes the dielectric surface must be highly planarized; otherwise, the overetch required to remove W stringers at steps will lower the height of the W plugs in the vias. The surface roughness of the CVD W film (Fig. 4-42a) worsens this problem, since a longer overetch is needed to clear all of the W residue from the field. In addition, the roughness of the tungsten surface can be transferred to the surface of the field oxide (which will produce other problems in further processing),

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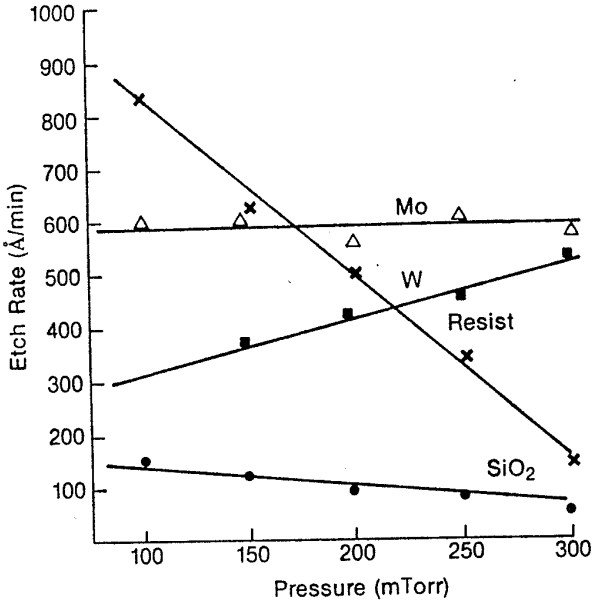

Fig. 4-41 Etch conditions used for W plug formation using photoresist planarization. Etch parameters are: flow – 60 sccm, 75% O_2 in CCl_2F_2/O_2; and power – 300 W (0.25 W cm^2); and a carbon cathode cover in the reactive ion etcher.[137] (© 1986 IEEE).

unless either an etchback process that planarizes the W surface, or a deposition process that produces smoother W films, is used. A technique to produce smoother films through the deposition of W in several layers (interspersed with a thin polysilicon layer between W layers) has been described (Fig. 4-42b).[127]

The erosion of W in the vias is also enhanced by a microloading effect that increases the etch rate when only a small area of the wafer contains W (i.e., when the only W exposed is in the vias or in the form of stringers). A three-step etchback step that minimizes this microloading effect has been reported.[133]

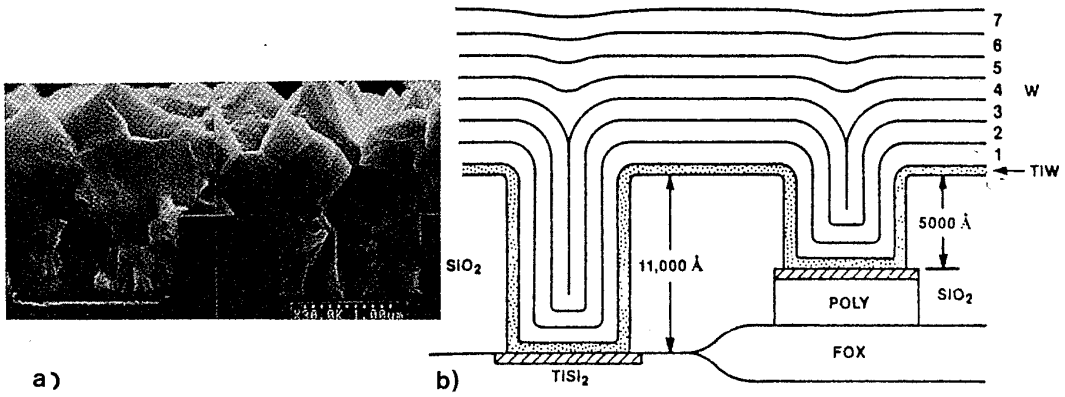

Fig. 4-42 (a) Surface roughness of conventional CVD-W films formed using the hydrogen-reduction process. (b) Smoother CVD-W films can be formed using a multi-layer-deposition technique in which a thin silicon layer is deposited between the W layers.[127] (© 1988 IEEE).

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Several other problems can be encountered with the blanket etchback process. First thick blanket-W films exhibit high stress, and such stressed films may cause wafer warpage. In addition, if W is deposited on the back of the wafer – where no adhesion layer may have been applied – the film will delaminate, producing unwanted particulates in the deposition chamber. Because W exhibits such good conformal coverage, backside deposition can occur unless the wafer is very well clamped to the plate on which it sits in the reaction chamber. Thus, the wafer clamping design is important. Furthermore, appropriate wafer clamping during the adhesion layer deposition is also important. That is, if the adhesion layer is not deposited on areas beneath the clips that hold the wafer, W can delaminate from these areas, again producing particles.[264]

In addition, The W deposited on the chamber walls can also build up until it spalls, producing particulates in the chamber. However, a recently designed single-wafer W-deposition chamber provides for in situ cleaning of the back of the wafer and the chamber (after each wafer is removed following film deposition).[252]

The second problem occurs during overetch, as a result of the etch gases attacking the adhesion layers. This can cause the formation of a groove between the W plug and the SiO_2 surrounding it, leading to step coverage problems for overlying Al films. TiN is reported to resist attack by the etch gases better than Ti, WSi_2, or Ti:W.[130]

A novel W etchback approach that uses a PECVD nitride sacrificial layer is described in reference 232. In this scheme, the problems of SiO_2 surface roughness and micro-loading effects during etchback are reported to be essentially eliminated. Overetching thus becomes less critical and can be used to compensate for nonuniformities in W deposition and etching. The elimination of loading effects allows coplanar W plugs to be easily achieved.

4.5.4.3 Selective CVD W. This method allows vias of varying widths to be filled without the problem of dimple occurrence in the wider vias. However, if deep vias are completely filled, then shallower ones will be overfilled (Fig. 4-43), necessitating an etchback step to planarize the surface. An alternative approach that does not require etchback is to partially fill the deeper vias and completely fill the shallower ones.

The main issues of importance for selective CVD W filling of vias are deposition selectivity, deposition rate, and the possibility of selectively depositing W on substrate materials other than silicon.[134] A review of the physical and electrical properties of selectively deposited W films produced in cold-wall systems through the hydrogen and silane reduction process is presented in reference 135.

The selectivity in deposition is dependent on various factors, including the type of insulator and the condition of the insulator surface. In general, selectivity tends to degrade as the W gets thicker. Ion bombardment or contamination of the insulator surface, however, causes the insulator surfaces to exhibit selectivity breakdown at an earlier stage in the deposition process. PSG demonstrates better selectivity than undoped SiO_2. Lowering of the WF_6 partial pressure, a decrease in the deposition temperature, and rapid scavenging the HF and SiF_4 reaction products will improve selectivity. A recent model for selectivity loss is described in reference 136.

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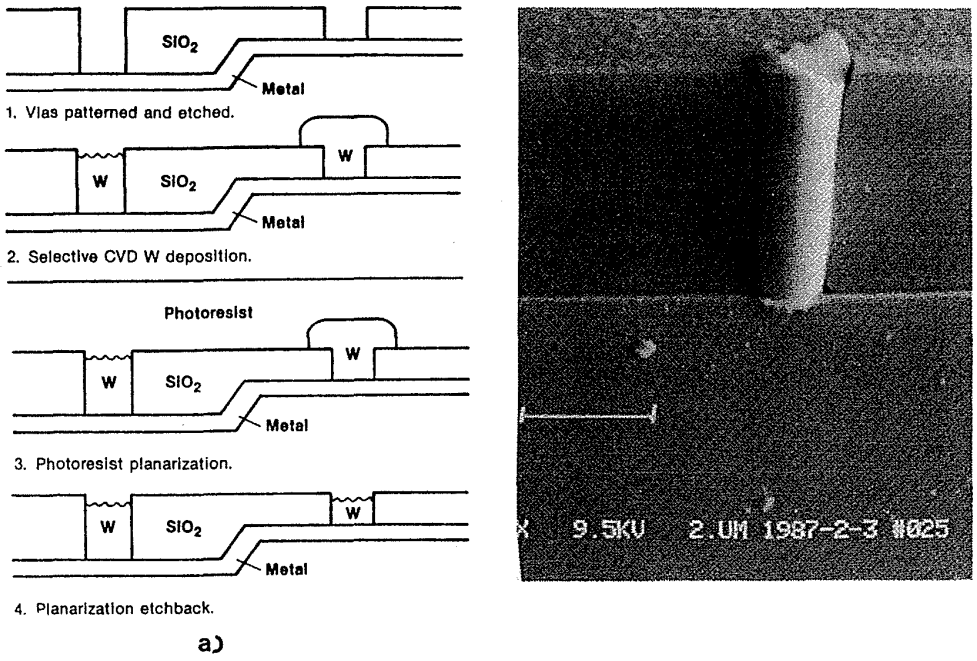

Fig. 4-43 Method of forming metal plugs using selective W deposition, resist planarization, and etchback. The shallow openings are overfilled and must be etched back to obtain a planar surface. (b) An SEM photo of a via plug 1.4 μm in diameter and 2.2 μm deep formed by selective-W deposition.[137] (© 1986 IEEE).

A *high deposition rate* is desirable from a manufacturing viewpoint. While the conditions that provide such high deposition rates in the hydrogen reduction process also degrade selectivity, the silane reduction process is able to provide high deposition rates (600-1000 nm/min) at lower temperatures (250-300°C, vs. 400-500°C for the hydrogen reduction process).

Since W will deposit selectively with either the hydrogen or the silane reduction of WF_6 as long as a good nucleating surface is exposed and the proper process conditions are met, the selective CVD W process can be used to deposit W into vias in which nucleating surface exists at the bottom. Vias with exposed Mo were used in one selective via-fill process (i.e., Metal 1 consisted of Ti:W overlaid with Mo).[137] In this process, a cold-wall reactor is used to deposit W at 50 - 500 nm/min. This process is compatible with the metal system used, since the contacts to Si using such a Metal 1 layer are stable to 650°C (see chap. 3, section 3.6.3). Other nucleating surfaces included $MoSi_2$,[138] and Al. The $MoSi_2$ was deposited over an Al film because a high contact resistance was observed when W was selectively deposited on Al. It was believed that this was due to nonvolatile reaction products (e.g., AlF_3) produced during the initial stages of W deposition. A later report indicated that this problem could be circumvented by a higher deposition temperature (>375°C) which would volatilize the AlF_3.[139]

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4.5.5 Other CVD Via-Filling Processes

4.5.5.1 Blanket CVD Polysilicon and Etchback for Contact Hole Filling. The use of a blanket-CVD polysilicon film together with etchback has been proposed as an alternative to the blanket-CVD-W filling of contact holes.[140,141] This approach circumvents the problems of film stress, backside deposition, deposition uniformity, and difficulty in etchback. In addition, the poly films can be deposited through the use of conventional hot-wall furnaces, rather than the special developmental CVD reactors needed for the deposition of W. Finally, because no adhesion layer is needed, a simple resistless etchback technique can be used.

An in situ heavily phosphorus-doped polysilicon film was used as the filling material in one report.[140] This procedure used an RTP anneal at 1050°C for 20 sec in an N_2 ambient following the poly deposition to produce films with the lowest sheet-resistance values (~9 Ω/sq). In another report,[141] the polysilicon plugs were doped with phosphorus following the etchback step. An undoped layer of SiO_2 on the BPSG prevented dopants from interacting with the diffusion ambient. Void formation in the center of the poly plug was eliminated through the use of a sloped-contact-hole etch procedure. In both reports, the polysilicon was also etched back without the use of a sacrificial resist layer, and a $Cl_2 + SF_6$ gas mixture was employed in the etchback step to give good selectivity to the underlying BPSG film and to ensure that no residue remained on the surface.

For 1.5 x 1.5 μm^2 contact holes, a contact resistance of 25±5 Ω per contact was measured for the in situ doped poly plugs (compared to 50 Ω per contact for Al:Si). Low junction breakdown-voltages were observed, however, and were determined to have been caused by junction punchthrough during the etchback process. In addition, it was noted that in order for this process to be used in CMOS, it would be necessary to use either two different types of poly doping, or a diffusion barrier (such as TiN) between the poly plugs and the Si substrate.

4.5.5.2 Selective Deposition of Poly. Contact-hole filling through selective deposition of polysilicon has also been reported.[221] In this approach, the native surface of the Si is purged by $SiCl_4$ and a carrier gas of hydrogen. This step deposits polysilicon seed crystals on the Si exposed at the bottoms of the contact openings in SiO_2. However, no polysilicon is deposited on the SiO_2 surfaces. Following the seeding, the gas mixture is switched to dichlorosilane, HCl, and H_2, and the process is continued as for selective epitaxial growth of Si (see chap. 2, section 2.7.5). Note that polysilicon rather than single-crystal silicon is chosen for selective deposition, since the grain boundaries of the poly enhance the diffusion of impurities. As a result, a lower-temperature process can be used to uniformly distribute dopants throughout the entire plug volume; ensuring fabrication of low-resistance plugs. However, the series resistance of such polysilicon plugs is relatively high.

4.5.5.3 Selectively Formed Silicide Contact Plugs. Intrinsic epitaxial Si is selectively deposited to approximately half the depth of contact holes in SiO_2,[222]

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and a film of Co or Ti is deposited to a thickness that will react the Si. A subsequent heating step is used to effect this reaction, and silicide plugs are thereby formed in the contact holes. The unreacted metal is then etched away with a selective metal etch. This technique has the advantage of not requiring a heavily doped SEG process for contact filling – a process that would be incompatible with CMOS technology.[223]

4.5.5.4 CVD Aluminum. While most of the work on CVD of metal films has involved tungsten, some research efforts have been directed at developing a CVD process for Al (although this technique is not yet sufficiently mature to be commercially available). The most successful CVD Al process involves the pyrolysis of triisobutyl aluminum (or TIBA).[142] Such films exhibit excellent conformal coverage, as well as resistivities of ~3.4 $\mu\Omega$-cm; in addition, they adhere well to Si and SiO_2. However, the surfaces of these blanket-deposited films are rough, which can cause lithography problems. Depositions are typically run at ~250°C and 100-200 torr, producing deposition rates of 10-20 nm/min. A review of this process and of the properties of CVD Al films is given by Levy and Green.[123]

It has recently been demonstrated that Al films can also be selectively deposited through the thermal decomposition of TIBA. Via holes as small as 0.4 μm have been successfully filled in this way.[144] In addition, whereas WF_6 can react extensively with Si during the selective CVD process, TIBA does not react with Si, and so leaves it undamaged. Finally, the surface-roughness drawback is apparently alleviated through this process.

Another recent paper described an LPCVD process for Al in a new batch-type, load-locked multichamber reactor, with smooth, highly-reflective Al films of high purity produced. Either blanket or selective Al deposition can be accomplished using this machine.[234]

There are two major problems associated with CVD Al. First, because TIBA is pyrophoric, explosive in contact with water, and toxic, it must be cold-trapped during processing rather than exhausted through the vacuum pump, and then disposed of after processing. In response to these difficulties, a process for forming CVD Al from a chloride source has also been studied.[145] The second problem exhibited is poor electromigration resistance. Although CVD Al has been shown to be as good as pure sputtered Al, it is not as good as Al:Cu, and a process for forming alloys must therefore be developed.

4.5.6 Alternatives to CVD for Filling of Vias

4.5.6.1 Bias Sputtering of Al for Complete Filling of Via Holes. If sufficient heat and bias are applied, complete filling of via holes can be achieved through sputter deposition of Al (Fig. 4-44).[107,108,115,116] Temperatures of between 400 and 500°C are necessary to sufficiently enhance the surface mobility is sufficiently enhanced so that complete filling is promoted as the film is deposited. However, such high temperatures, may cause unwanted effects in the film – for example, at 475°C and above, Cu in Al films tends to form large grains of Al-Cu intermetallics, which become

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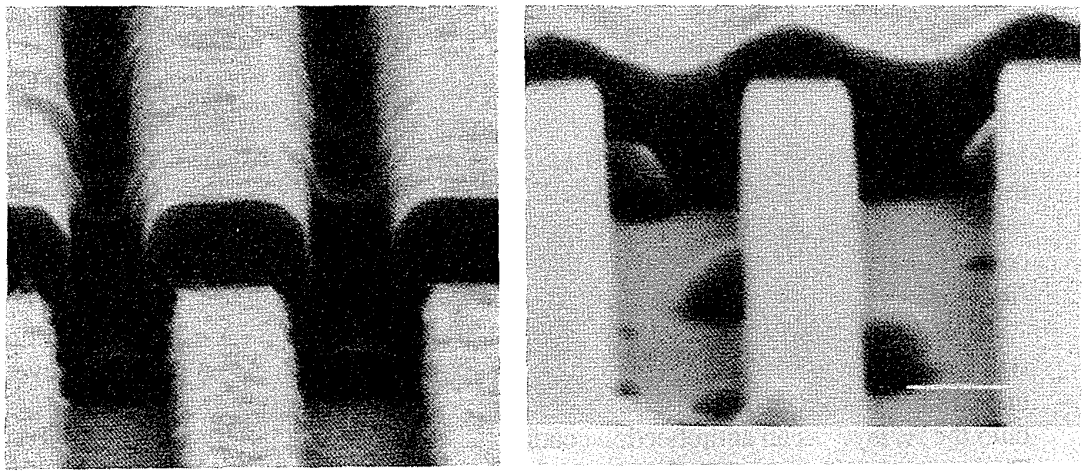

Fig. 4-44 Comparison of step coverage of: (a) conventionally sputter-deposited Al, and (b) high-temperature, high-bias sputterdeposition process that yields highly planarized Al films, even over high-aspect ratio contact openings with vertical sidewalls. Courtesy of MRC, Inc.

a serious problem for dry etching. At lower temperatures (200-350°C), Cu tends to segregate at the film/substrate interface. As a result, it has been reported that these films exhibit poor electromigration resistance, unless deposition temperatures in excess of 500°C are used.[262] It has also been reported that completely planarized Al causes heavy damage to the Si that cannot be fully annealed out. Work is being done to understand the nature of the damage, and to develop ways to minimize it.[109]

4.5.6.2 Laser Planarization of Al Films. Another technique for improving the step coverage of Al lines over vias involves melting the Al film through irradiation with a pulsed laser prior to patterning. The mass transport that occurs while the Al is molten arises from high surface tension (which is about 50 times that of water). Such flow can completely fill and planarize the surface over the vias (Fig. 4-45). All hillocks

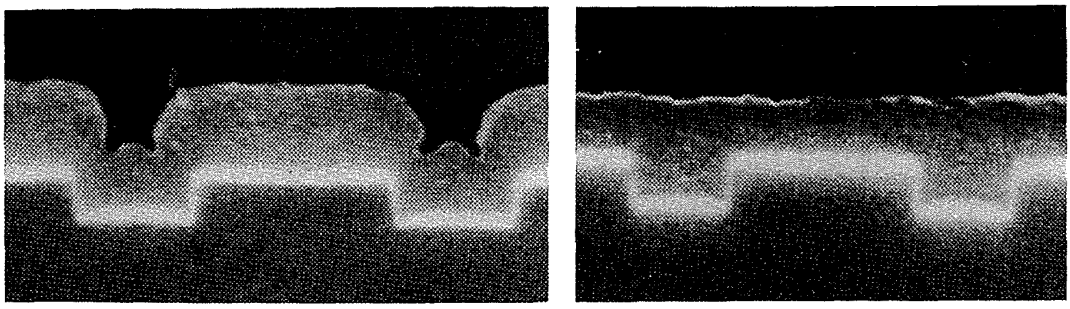

Fig. 4-45 SEM photos of an Al film before and after laser planarization.[210] Reprinted with permission of Solid State Technology.

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and surface irregularities are also removed. In addition, laser-planarized films show a reduced tendency to regrow hillocks.[146,220]

A dye laser (wavelength 504 nm) was used in the original report, and a laser pulse of ~1 μs duration was estimated to be adequate to allow the surface to reach a sufficient level of smoothness.[147] A thin (20 nm) layer of Si was in situ sputter deposited onto the Al film to passivate it against native aluminum-oxide formation (which would remain as a solid skin and impede planarization), and also to act as an antireflection coating (since ~92% of the light would otherwise be reflected from the uncovered Al film surface).

In later work, an excimer-laser process was developed, and the laser-pulse duration was reduced to 15-30 ns.[148,240] The shorter pulse and ultrarapid heating prevent undesirable metallurgical reactions. A thin Cu film (<100 nm) was sputter deposited onto the Al layer as an antireflection coating (since the reflectivity of Cu is only ~20%). The excimer laser can planarize the surface of a 150-mm wafer in about 40 sec, with either a step-and-repeat or a raster-scan motion employed. Data showed that no junction leakage was observed in Al:Si excimer-laser planarized films, and that contact resistance was comparable to that obtained with conventional furnace annealing. Contact openings 0.75 μm wide and 1.5 μm deep have reportedly been filled using this technique. The redistribution of alloy constituents in the film as a result of this procedure may play a role in the electromigration behavior of these films. Another report indicated that laser-planarized Al:Cu films exhibited no hillock growth following 450°C furnace annealing, and initial data also suggest that an improvement in electromigration resistance may be possible under specific process conditions.[241]

Recent work indicates that the method shows promising results in the research laboratory, but that it has a narrow process window of only 6-8% (e.g., the energy applied to the Al film must be carefully controlled to provide adequate melting without producing ablation).[242] The dominant variable is the laser energy which can vary by ±5%, but Al film thickness variations and substrate heating uniformity are other variables which can impact the local quantity of energy applied to the Al. Methods to widen this process window will need to be developed to make it a viable manufacturing option.

In one recent study an attempt was made to optimize the wafer temperature and laser power to provide the widest possible process window for the laser power. Good via filling and coverage of the Al over steps was achieved. The laser-flowed Al:Cu lines also showed electromigration resistance comparable to those of non-flowed Al:Cu lines.[263]

4.5.6.3 Contact-Hole and Via Filling with Selective Electroless Metal Deposition. Various metal films (including Ni, Cu, Au, and Pd) can be deposited through electroless deposition of metal films from aqueous solutions consisting of metal ions and reducing agents.[149] Reports on via filling have focused on Ni and Pd because of the abundant information processes, and because of the wide choice of reducing agents.

In one process, the Ni was able to fill the vias to the top, producing a uniform and planar surface (Fig. 4-46). Vias with several different diameters were filled simulta-

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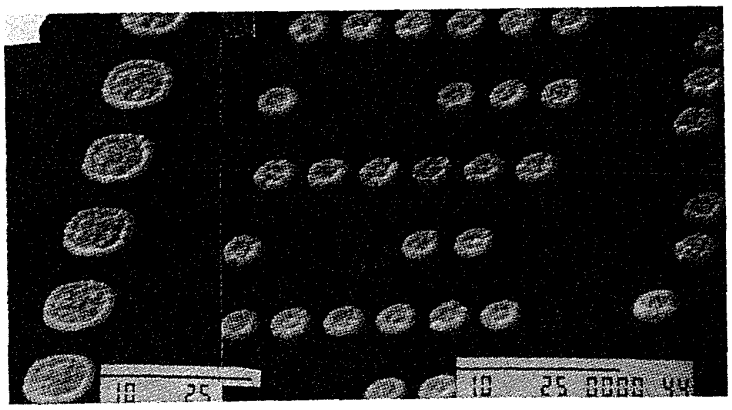

Fig. 4-46 SEM photos of 2.5-μm $TiSi_2$-based contacts filled with Ni.[149] Reprinted by permission of the publisher, The Electrochemical Society, Inc.

neously. An Al film was then deposited. Low contact resistance in the vias was exhibited following annealing. Unframed vias can be used, since the vias are filled with a different material than the main conductor, and since good selectivity can be obtained between the Al and the Ni during the Al etch process.

Three critical aspects of the Ni process must be controlled in order to successfully implement via filling with this technique.[150] First, the surface of the Al at the bottom of the via must be free of native oxide; this can be accomplished by performing a dilute HF dip. Second, the Al surface must be activated (e.g., by first depositing Pd), since Al is not catalytic for Ni deposition. This is achieved by using a displacement reaction ($3Pd^{+2} + 2Al \rightarrow 3Pd + 2Al^{+3}$) that deposits a high density of discrete Pd particles on the Al surface. The third critical aspect is the Ni deposition itself. A solution containing Ni ions and a reducing agent (e.g., hypophosphite, at a concentration of 0.1 mole/L, or dimethylamine borane) at ~70°C gives a deposition rate of ~3 μm/hr. Following the deposition, an anneal step of 400°C in N_2 is used to remove any traces of the solution in the vias and to improve the adhesion of Ni to the substrate.

In the selective electroless process for contact-hole filling, either Ni or Pd is deposited onto $CoSi_2$ or $TiSi_2$ at the bottom of contact holes in BPSG.[151] The conditions for Ni deposition are like those just described for via filling. Pd can be deposited without activation of the surface; however, it has been observed that both diodes and transistors fabricated with this process show degraded device characteristics following the metal deposition and anneal, due to interaction between the Ni/silicide or Pd/silicide and the underlying n^+ Si. A diffusion barrier will therefore be needed. For example, a 150-nm selective CVD W layer can be deposited onto the $TiSi_2$ layer in the contact holes. This has been observed to prevent the reaction between the Pd plugs and the underlying substrate for anneal temperatures < 450°C.[152]

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4.5.7 Pillar Formation as an Alternative to Contact-Hole and Via Filling

Pillars (also called *studs* or *posts*) may be formed prior to deposition of the dielectric. In contrast to conventional contact holes and vias, pillars allow the use of non-nested design rules, and device areas can thus be reduced. In addition, stacking of contact holes and vias is possible. Pillar-formation methods include:

- *Pillar formation by lift-off.* A lift-off technique (see Vol. 1, chap. 15) has been used as the method used to form pillars in a four-level metal interconnect system for bipolar gate arrays.[153,154]

- *Simultaneous deposition of the Metal-1 and pillar films, followed by two-mask patterning of pillars and Metal-1 lines.* This approach also includes a technique for self-aligning the pillars to the Metal-1 lines, even though two masking steps are used.[155] The Metal-1 patterns are etched, and then the pillars (Fig. 4-47).[251] To obtain a highly planar surface, a resist etchback technique is used that includes an additional masking step. This technique was designed for use with a metallization system having a 2.5-μm pitch.

- *Etching the pillars from a thin metal film using contrast-enhancement lithography.* In this approach, submicron-wide pillars are defined and etched using a contrast-enhancement lithography (CEL) technique.[156] The first pillar, which consists of a Ti/W/Al trilayer film, is deposited directly onto $TiSi_2$. The film is imaged using a CEL technique to form 1 x 1 μm pillars. The dielectric-

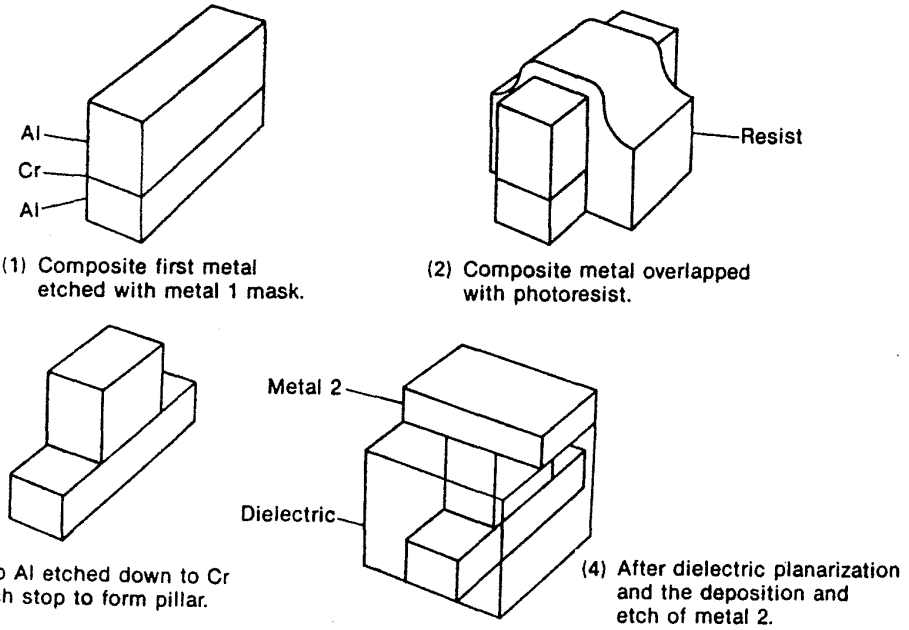

Fig. 4-47 Sequence used to produce Al/Cr/Al pillars using photoresist overlap method.[251] (© 1984 IEEE).

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layer formation is accomplished by etching back a CVD SiO_2 film. The tops of both high pillars (located on field-oxide and poly steps) and low pillars (located on substrate contact regions) must be exposed following the etchback procedure. Metal 1, which makes contact to the posts, is then deposited and patterned.

4.6 FILLED GROOVES IN A DIELECTRIC LAYER

Assume that a planarized dielectric surface exists between polysilicon and Metal 1 and that a process is available that can completely fill the contact holes etched in this layer. The fabrication of a multilevel interconnect system can now follow the process sequence that has been described, or an alternative process sequence can be carried out. In this sequence, part of the DM1 dielectric layer is deposited, and grooves are patterned in it. Metal 1 is then selectively formed in the grooves. Finally, the entire surface is covered with an additional dielectric layer.

This alternative filled groove approach has the important advantage of being able to produce a completely planarized dielectric surface *without the need of a planarizing procedure for DM1*. Because this approach is inherently planar and self-aligned, and also allows stacked vias, it can be used to fabricate three or more levels of metal. It also allows thicker metal layers to be deposited without the creation of topographical conditions that would make planarization even more difficult. This capability is necessary, for example, to produce W and Al lines of the same line resistance and equal widths. However, since the vertical elongation of the W lines increases the intra-level capacitance, this approach may not be suitable for all circuit designs and types.

The unique process step in this method is the deposition of metal in the dielectric grooves. Techniques to implement the process include the following:

- *Blanket CVD deposition and etchback of W.* This technique, dubbed the *filled-interconnect-groove* (or FIG) method, was described by Broadbent et al. (Fig. 4-48).[157] A thin Ti:W adhesion layer is first sputter deposited into the grooves. The CVD-W process is then carried out by means of hydrogen reduction of WF_6 so that a void-free filling of the grooves with W is achieved. This W film is then etched back until W remains only in the grooves of the SiO_2 film.

- *Selective CVD W deposition in the grooves.* This technique was presented by D. C. Thomas et al., who called it the *tungsten (W) interconnect technology,* WIT.[158] Si is implanted into the bottom of the grooves etched in the SiO_2 (with an implant dose of ~10^{17} cm^{-2}), where it serves to selectively initiate the deposition of W on the SiO_2 surface. A silicon-nitride layer prevents the Si from penetrating the nonetched SiO_2 surface and the sidewalls of the groove (Fig. 4-49). The nitride layer is removed by means of a hot phosphoric etch after the Si implant and before the W deposition.

- *Lift-off using edge-detection (LOPED).* This technique, illustrated in Fig. 4-50,[159] can be used to fill narrower spaces than would be possible with conventional lift-off methods (see Vol. 1, chap. 15).

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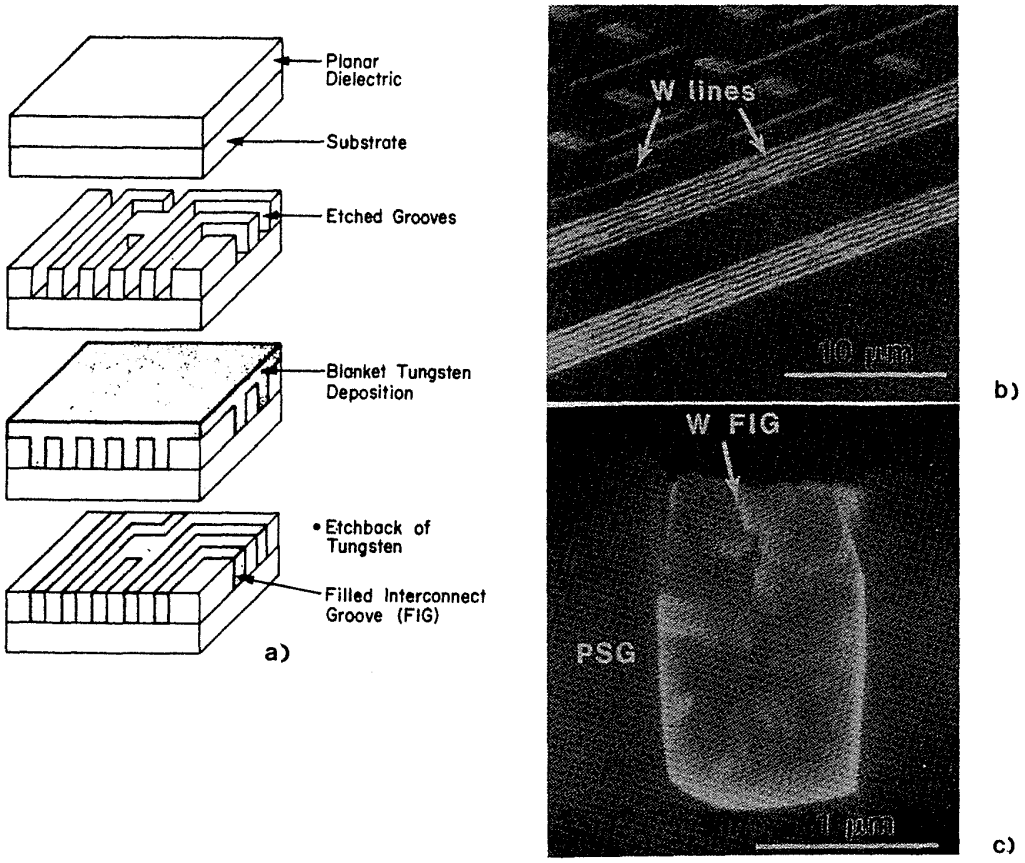

Fig. 4-48 (a) Representation of process sequence used to construct a level of filled interconnect groove (FIG) metallization. (b) Perspective top view of SEM micrograph of FIG metallization after etchback of the CVD W. (c) Cross section SEM micrograph of a FIG conductor (~1.1-μm wide) after CVD deposition and etchback.[157] (© 1988 IEEE).

• *Electroless selective deposition of metal.* Here the process technology employed to fill via holes is the same as that described in section 4.5.6.3, except that a thin Al layer is deposited into the grooves prior to the starting of the process sequence.[160]

4.7 MANUFACTURING YIELD AND RELIABILITY ISSUES OF VLSI INTERCONNECTS

Yield-limiting factors are flaws in the manufacturing process that result in the production of parts that fail to operate properly immediately following fabrication. Other flaws, known as *reliability factors* result in parts that operate correctly immediately following manufacture, but that fail later during normal operation (or even during storage). Defect-related random failures tend to follow yield trends, while wearout-related reliability failures may be totally independent of yield. (Information of a more detailed nature dealing with these issues will be presented in Vol. 3 of this text.)

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4.7.1 Factors That Impact Manufacturing Yield

Many of the yield-limiting factors associated with multilevel-interconnect fabrication are the same as those that afflict single-level interconnect processes:

- Junction spiking (see chap. 3, section 3.4.3),
- High contact resistance between Metal 1 and Si (see chap. 3, section 3.4.2.3),
- Gate-to-source shorts due to lateral silicidation over oxide spacer (see chap. 3, section 3.9.1.1),
- Contamination of Al interconnects by incorporation of residual gases present during sputter deposition.[161] For example, oxygen incorporation can cause an increase in the film resistance and hardness, which may lead to bonding problems. Nitrogen incorporation increases stress and thus the tendency to crack.[162]
- Misalignment of metal lines to contact holes (see Vol. 1, chap. 12).

4.7.2 Multilevel Interconnect-Related Yield Issues

Following are several of the factors that adversely impact yield when multilevel interconnects are used:

- *Pinholes and weakspots in the PMD and intermetal-dielectric layers*, which result in shorts or unacceptably low breakdown voltages between different conductor levels. These have several causes:

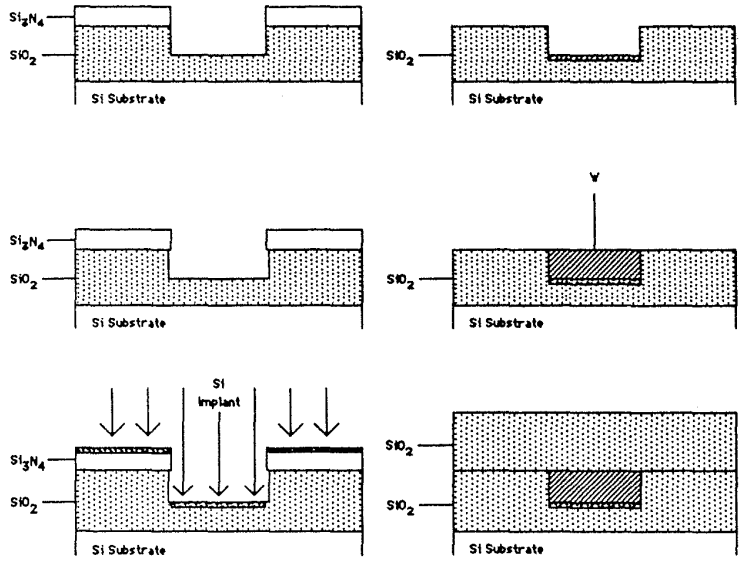

Fig. 4-49 Process flow for planar *W interconnect technology* (WIT).[158] (© 1988 IEEE).

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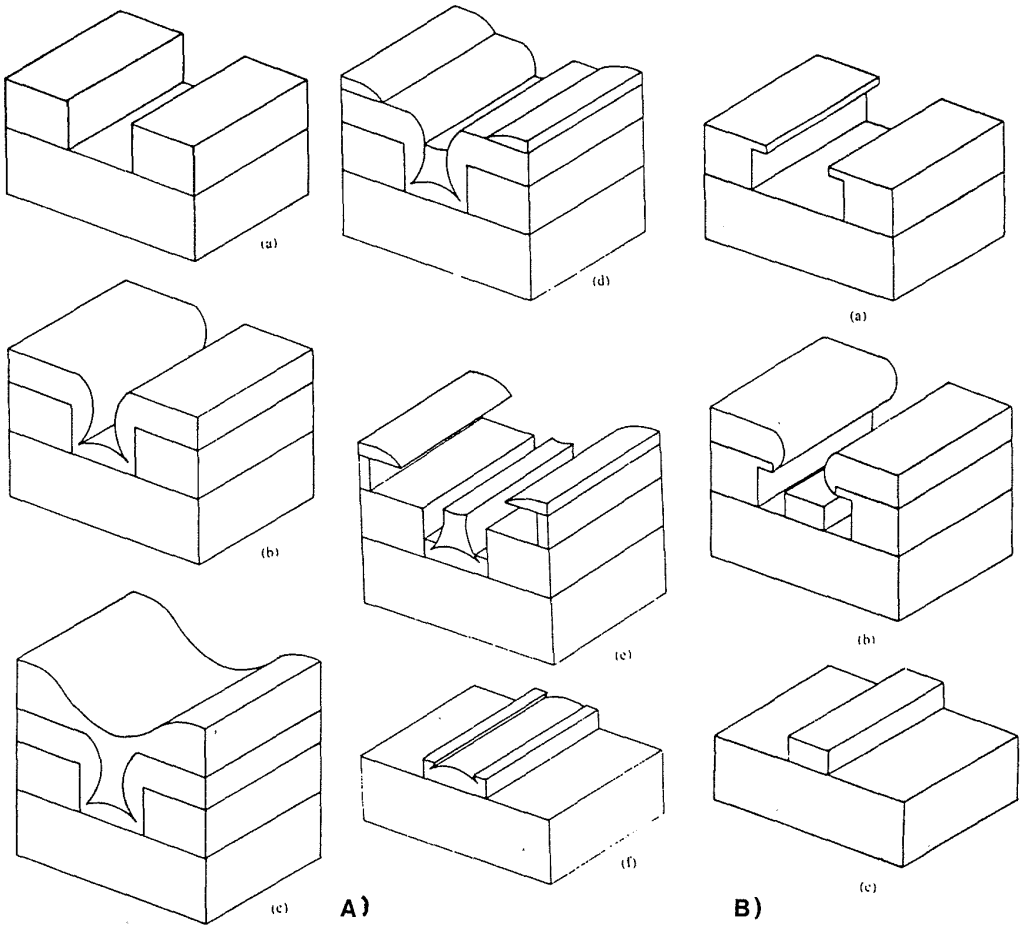

Fig. 4-50 (A) Outline of the LOPED process: (a) A layer of positive resist is patterned by a dark field mask and flood exposed after development; (b) The desired thin film is deposited with good step coverage; (c) A second resist layer is applied; (d) The second resist layer is etched; (e) The deposited film is etched; (f) The liftoff process is completed. **(B)** Process flow of direct liftoff: (a) A layer of photoresist is patterned by a dark-field mask and processed to form a reentrant angle; (b) The desired film is deposited with poor step coverage; (c) The liftoff step is completed by dissolving the lifting medium in a solvent. The excess film is removed at the same time.[159] (© 1989 IEEE).

- *Particulates.* These may be generated in three ways: (1) they may originate in the process environment; (2) they may be formed by gas-phase nucleation during CVD of the dielectric (see section 4.3.2.3); or (3) they may arise as a result of dielectric-film deposition on moving parts in the CVD chamber, later flaking off.
- *Hillock growth* in the underlying metal layer.
- *Thinning of the photoresist* over the corners of steep steps in the dielectric. This may may lead to complete resist erosion during via etching and subsequent attack of the dielectric (which can give rise to thin spots).

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• *Misalignment during via patterning process*, leading to open-circuit conditions.

• *Topography-related issues.* These include step-coverage problems that cause opens in interconnect lines or thinning of the metal lines to such a degree circuit performance becomes unacceptable; and stringers that short adjacent metal lines.

• *Open circuit or high contact resistance between conductor materials of different levels*, due to:

- Incomplete etching of all via holes (see section 4.6),
- Failure to remove the native oxide from the conductor (e.g., Al_2O_3 on Al) prior to the deposition of the next level of metal (see chap. 3, section 3.4.2.3),
- "Poisoned vias," which occur when the constituents of an SOG film outgas during the metal deposition, producing high via resistances (see section 4.4.9).
- High resistance between two conductor layers (e.g., high via resistance).

Since the very last effect listed above has not been discussed elsewhere, we will consider it here.

4.7.2.1 High Resistance between Two Conductor Layers. Generally speaking, the specific contact resistivity of metal to metal is very low, and does not represent a problem when contact between metal layers is made through a via. For example, the specific contact resistivity of Al-to-Al contacts is $<10^{-8}$ Ω-cm^2. However, relatively high contact resistance has been observed when W via plugs are used to make contact to underlying Al layers.[138] This is believed to be caused by fluorine (from the WF_6) reacting with the Al to form a nonvolatile AlF_3 layer at the Al-W interface.

Procedures for obtaining lower contact-resistance values between selective CVD W and Al have been reported. One report found that at temperature and deposition rates of ≥375°C and ≥20 nm/min, respectively, specific contact resistivities of ~10^{-8} Ω-cm^2 are obtained, (possibly because at such temperatures the AlF_3 is volatilized as soon as it forms).[139] In the second report, it was also observed that the contact resistance of selective-W-to-Al interfaces in submicron vias is deposition-temperature dependent, and that it continues to decrease up to temperatures of 550°C.[247] Another approach that produces low contact resistance between Al and CVD W plugs involves capping the Al film with a layer of sputtered Ti:W during the same pumpdown as the Al deposition. Following via patterning of the intermetal dielectric, CVD W is selectively deposited on the Ti:W. Since no Al is exposed, the possibility of forming AlF_3 is avoided.[257]

Relatively high contact resistance between selectively deposited W and $TiSi_2$ has also been observed.[163] This finding was confirmed by Ng and Merchant, who reported that the use of a higher deposition temperature could also reduce the contact resistance value.[164]

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4.7.3 General Reliability Issues Associated with IC Interconnects

4.7.3.1 Electromigration. Electromigration is the motion of the ions of a conductor (such as Al) in response to the passage of current through it. These ions are moved "downstream" by the force of the "electron wind." A positive divergence of the ionic flux leads to an accumulation of vacancies, forming a void in the metal. Such voids may ultimately grow to a size that results in an open-circuit failure of the conductor line. Electromigration is, therefore, a wearout mechanism.

In general, the failure rate is increased when the current density in the conductor line is increased, or the operating temperature is raised. Thinning of the conductor lines as they cross steep steps will also accelerate electromigration failure rates, because the current density at such locations along a line are increased. It has likewise been found that Si precipitates (or nodules) which occur in Al:Si films, can grow large enough to constrict Al cross-sections in narrow lines.

Techniques for increasing the resistance of an interconnect process to electromigration failure include the following:

- Adding Cu (0.5-4 %) to the Al film.
- Adding Ti (0.1-0.5 %) to the Al film.
- Using a layered Al film structure, with a highly electromigration resistant metal (such as Ti, W, or Mo) as the central layer of a trilayer film.
- Planarizing the intermetal dielectric, to eliminate thinning of the conductor lines as they cross steps.
- Selectively depositing a layer of CVD W over the Al lines.
- Avoiding the use of Al:Si when fabricating narrow, multilevel-metal structures.
- Replacing the Al metallization with a more electromigration-resistant metal, such as W or Mo.

4.7.3.2 Electromigration at the Contacts. Electromigration can also occur as a result of current flow through the contact interface. The "electron wind" drives the Si atoms along the grain boundaries of the Al film, causing the formation of voids in the Si. These voids result in either open circuit failures, or – if they are back-filled by Al - result in junction spiking failures. Such failures can be prevented through the use of a diffusion barrier material between the Si and the Al or of a metallization in which Si does not rapidly diffuse (e.g., W).

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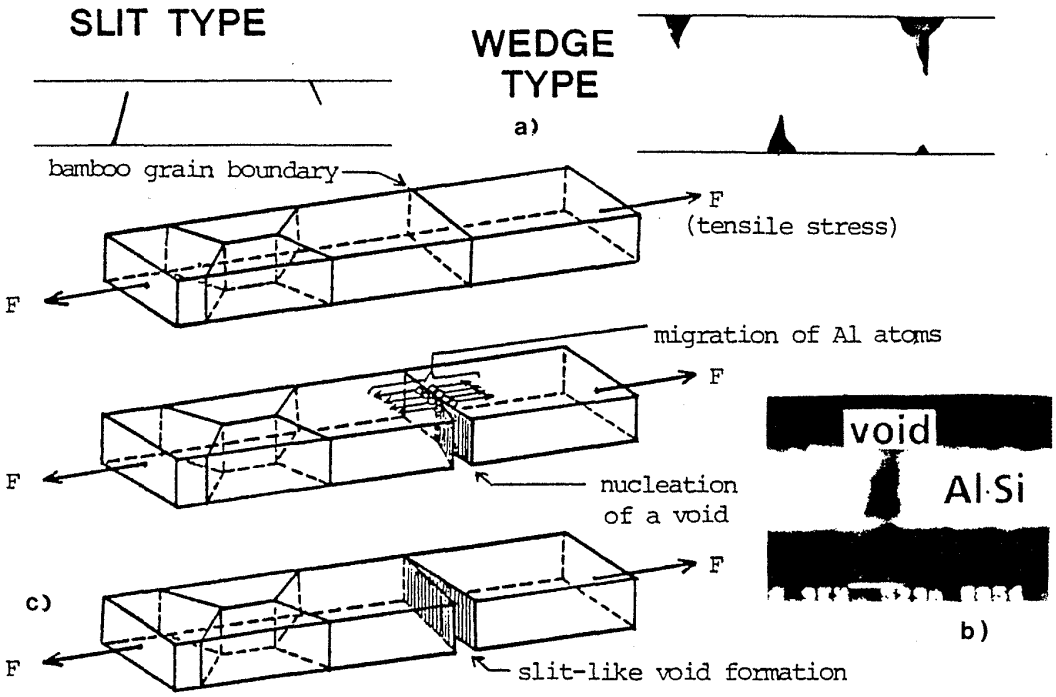

Fig. 4-51 (a) Schematic drawing of stress-induced voids in Al interconnect lines. (b) SEM photo of such a void. (c) Schematics of one proposed formation-mechanism of slit-like voids.[260] (© 1985 IEEE).

4.7.3.3 Stress-Induced Metal Cracks and Voids. Metal cracks and voids have been observed in Al interconnect lines (Fig. 4-51a and b) after the lines have been stored at elevated temperatures (even when no current has been passed through them).[165] Parts have also been found to fail after doing no more than sitting on a shelf for one or two years, even when they had passed earlier tests. In some cases the voids extend all the way across a line, causing an open-circuit failure. In others, the notches at the edges of the metal lines cause partial loss of a cross-sectional area, resulting in early electromigration failure. The problem is so severe that industry observers have claimed it contributed to putting at least one company out of business (Mostek).[166]

Two stress-related failure mechanisms have been identified: (1) high compressive stress in overlying dielectric films, which causes tensile stresses in the metal film; and (2) tensile stress in the Al films during heating, caused by the mismatch in the coefficients of thermal expansion of the Al lines and the silicon substrate (and the consequent inability of the Al lines to relieve this stress by differential movement, since it is then tightly bonded to the deposited dielectric). It is believed that the stress must be relieved by mass transport through the diffusion of Al atoms into the the grain boundaries from neighboring grains, with void formation resulting (Fig. 4-51c). In one report, the first mechanism is held primarily responsible for void formation in wide Al lines, while the second mechanism is thought to cause voids in narrow Al lines.[167]

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The problem is expected to become even more severe as devices shrink, for several reasons. First, the narrower the line width becomes, the greater the stress will be (Fig. 4-52a).[168] Second, the metal lines in lowest level of multimetal interconnect structures experience the greatest stress. Finally, the lines of the lowest-level metal are often the narrowest.

Several measures can be taken to reduce the severity of these effects in Al lines:

1. The stresses in the overlying films should be tensile or at least have a low compressive value. For example, the failure rate was far lower for silicon-oxynitride passivation layers that exhibited low compressive stress, than for highly compressively stressed PECVD nitride passivation layers.
2. Since the incorporation of N_2 into Al films makes the films very hard and

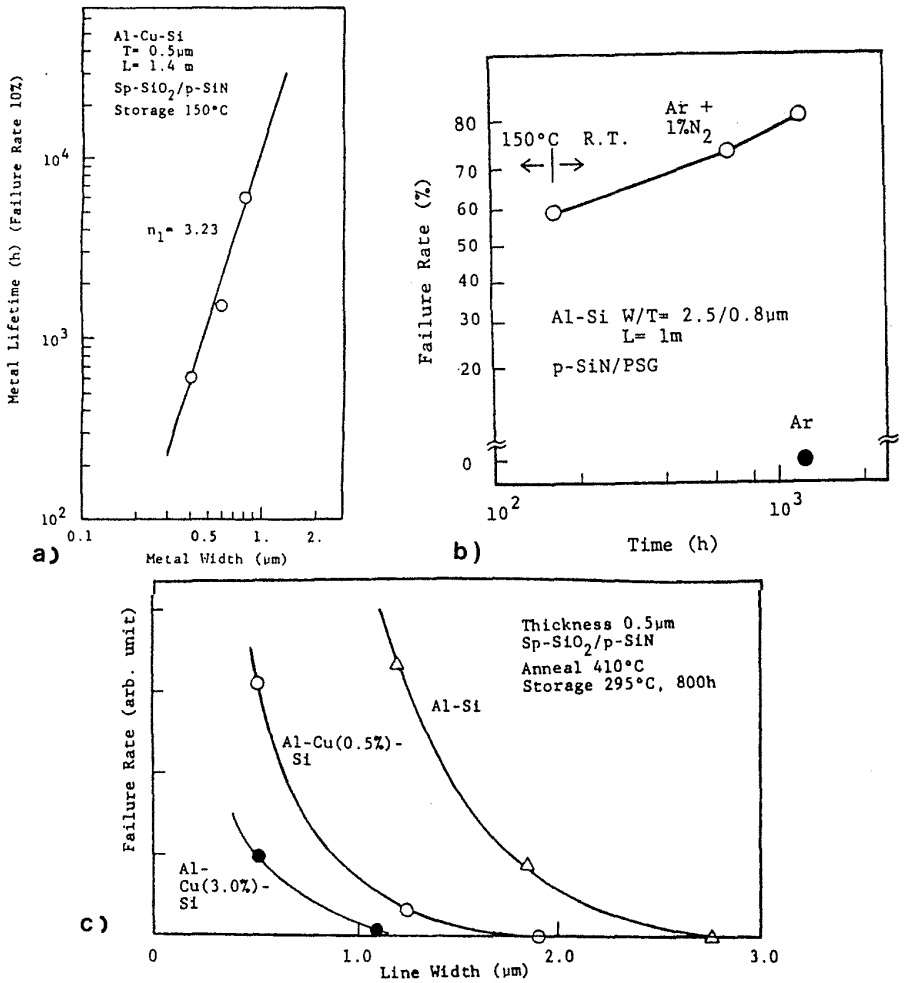

Fig. 4-52 (a) Line width dependence of stress-induced migration of Al:Si:Cu. (b) Stress-induced migration enhanced by N_2 contamination. (c) Dependence of stress-induced migration on the Cu content of the Al films.[168] This paper was originally presented at the Fall 1988 Meeting of The Electrochemical Society, Inc. held in Chicago, IL.

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and brittle, and thus dramatically increases the stress-induced void formation rate (Fig. 4-52b), care must be taken to prevent N_2 from being incorporated during sputter deposition.[162]

3. Adding Cu to the films reduces the failure rate (Fig. 4-52c). A recent report indicates that adding Pd to the Al films seems to be even more effective than adding Cu.[238]
4. A layered structure (with such materials as $MoSi_2$) produces lines with much longer life. These structures help prevent the formation of voids across the entire cross-sectional area of the interconnect line.
5. Because steep steps on the wafer surface enhance stress and increase failures, the interlevel dielectrics should be planarized.
6. A slow cooling time from 400°C to room temperature increases the failure rate, while rapid-quench cooling results in much lower failure rates.
7. Silicon nodules in the Al cause local stresses in the lines, which also increase the tendency for void formation.[169] See section 3.4.4, chap. 3 for a discussion on silicon-nodule formation in Al lines.

Other suggested approaches for alleviating the problem include the use of higher-melting-temperature metals, such as W (which exhibit lower diffusivities); the development of a more pliable passivation layer; the use of dielectric-film deposition processes that require lower temperatures; and intentional debonding of the interface between the metallization line and the dielectric layers that cover it.

4.7.3.4 Corrosion. Corrosion of the metal lines can be caused by the following:

- Transport of moisture and such contaminants as Cl through the passivation layer, and subsequent reaction of these with the metal lines (see section 4.8). The moisture and contaminants may either exist in the package material itself or may arrive through cracks in the package.

- Leaching of phosphorus from phosphorus-doped SiO_2 intermetal or passivation dielectric layers, followed by reaction of the phosphorus with absorbed moisture to form phosphoric acid (which then attacks the Al - see Vol. 1, chap. 10).

- Residual Cl (which remains on the wafer surface following a Cl-based dry-etch step of Al) reacts with moisture to form HCl, which then attacks the Al (see Vol. 1, chap. 10). The standard way of dealing with this problem has been to expose the wafer to a short, in situ CHF_3 or CF_4 etch step after the Al has been patterned and the resist has been dry etched. A recently reported alternative technique uses a reactor that contains an integrated spin-rinse system in the exit loadlock, which sequentially dispenses an organic solvent and water onto the wafer. This technique is believed to remove the carbonaceous chlorine-containing polymer that remains on the wafer following the etch process.[219]

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4.7.4 Reliability Issues Associated with Multilevel Interconnects

4.7.4.1 Hillock Formation and Prevention Measures. Hillocks are spike-like projections that erupt in response to a state of compressive stress in metal films and consequently protrude from the film's surface (4-53a). There are two reasons why hillocks are an especially severe problem in Al thin films (in which they may become twice as large as the film thickness), for two reasons. First, the thermal coefficient of expansion of Al (23.5×10^{-6}/°C) is almost ten times as large as that of Si (2.5×10^{-6}/°C). When a silicon wafer is heated, the thin Al film (which is tightly

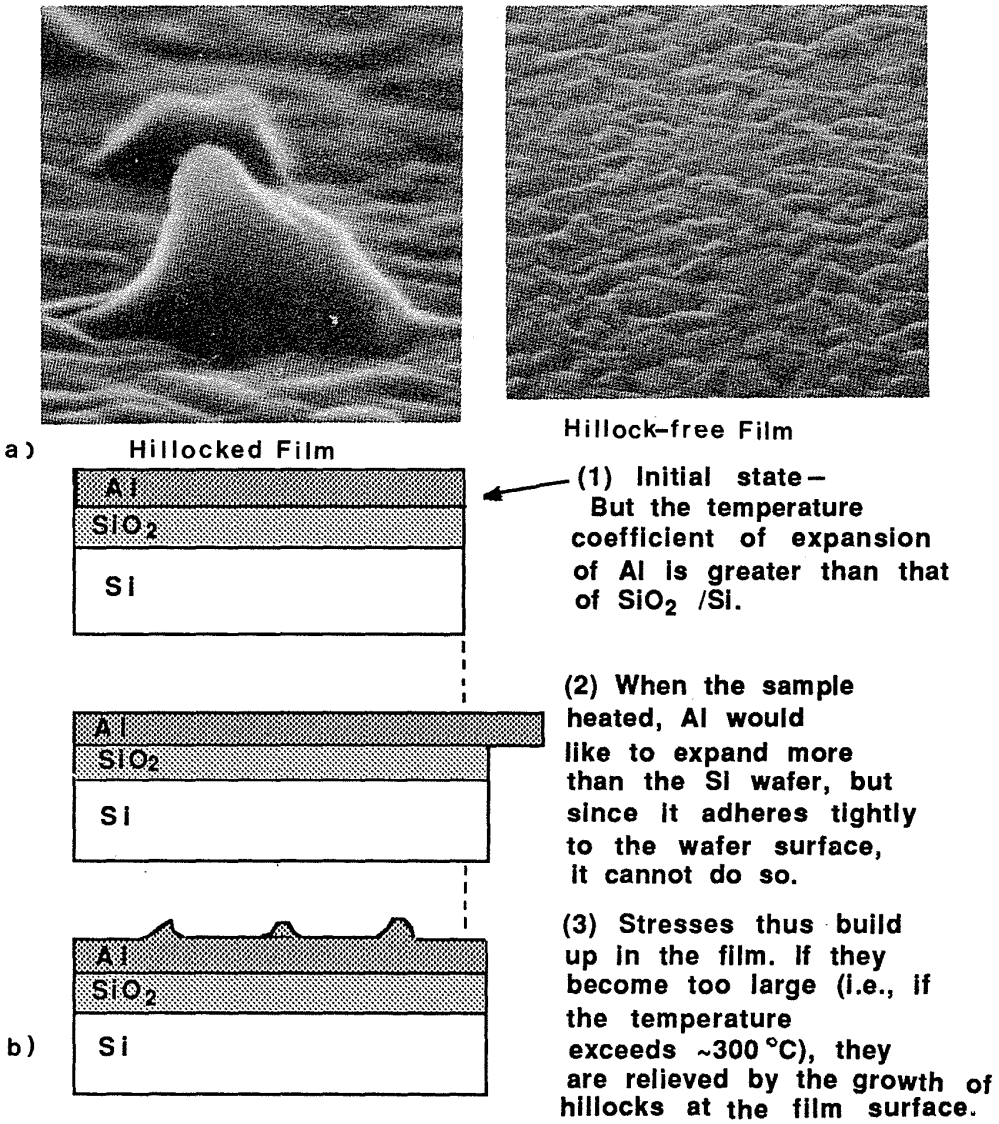

Fig. 4-53 (a) SEM photo of hillocked and hillock-free Al thin film. (b) Schematic drawing of how thermal stress causes hillock growth in Al thin films on a Si wafer.

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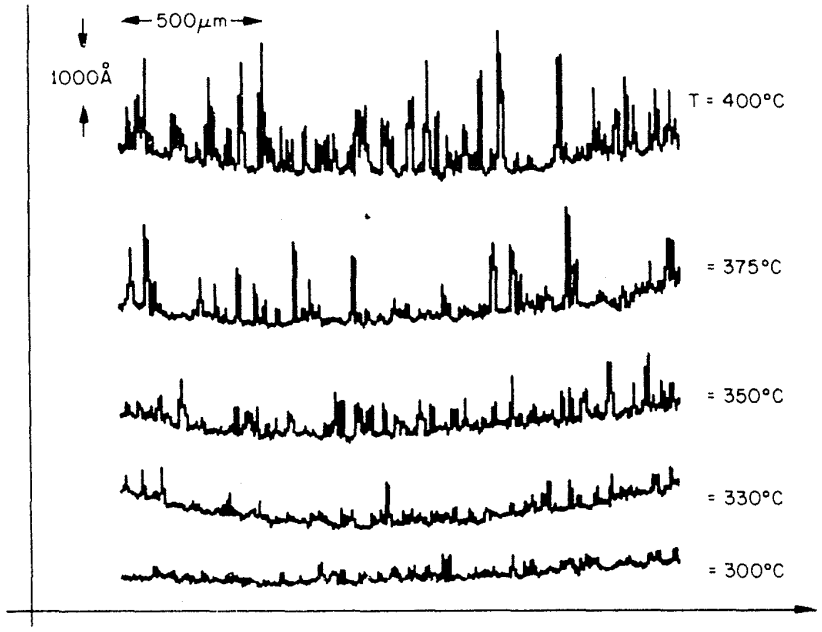

Fig. 4-53 (c) Hillock formation as a function of deposition temperature.[172] (© 1987 IEEE).

adherent to the much more massive wafer) "wants" to expand more than is allowed by the wafer expansion (Fig. 4-54b). The result is a compressive stress, σ, which increases at the following rate as a function of temperature:[170]

$$d\sigma/dT = -2 \times 10^7 \text{ dynes cm}^{-2} \text{ °C}^{-1} \qquad (4 - 15)$$

As a result, when the Al film is heated to temperatures in excess of 300°C, the compressive stresses in the film become very high.

The second factor involves the low melting point of Al (660°C), and the consequent high rate of vacancy diffusion in Al films. Hillock growth takes place as a result of a vacancy-diffusion mechanism.[171] Vacancy migration occurs as a result of the vacancy-concentration gradient arising from the stresses; in addition, the rate of diffusion increases very rapidly with increasing temperature. Hillock growth can thus be visualized as a mechanism that relieves the compressive stress in the Al film through the process of vacancy migration away from the hillock site, both through the Al grains and along grain boundaries. Figure 4-53c shows the sizes and the densities of hillocks on an Al:Si:Cu thin film on which a dielectric film was deposited at different temperatures (between 300° to 400°C).[172]

The most significant hillock-related problem in IC manufacturing occurs in multimetal-interconnect structures. In such structures, hillocks cause interlevel (as well as intralevel) shorting when they penetrate the dielectric layer that separates neighboring metal lines.

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Interlevel shorts can occur when a conformal-CVD dielectric is deposited over a hillocked metal film. When a photoresist is spun onto the dielectric layer, the resist will be thinner over the hillocks (Fig. 4-54a). During the via-etch process, the thin resist may be completely removed in these spots and the dielectric will then be exposed to the etching ambient. Under some circumstances the dielectric film may be completely etched away, allowing the exposed hillock to form a short to the next level of metal. Even if the dielectric is not completely removed, it may become so thin that low dielectric breakdown may occur between Metal 1 and Metal 2.

Intralevel shorts can occur if the hillocks protrude from the sides of the metal lines and cause overlying dielectric layers to delaminate (Fig. 4-54b). The hillocks can then continue to grow until they make contact with an adjacent-metal line. Such problems become more severe as the spacing between metal lines becomes narrower. The presence of hillocks also reduces film reflectivity, introducing alignment difficulties and making the microlithography process less controllable.

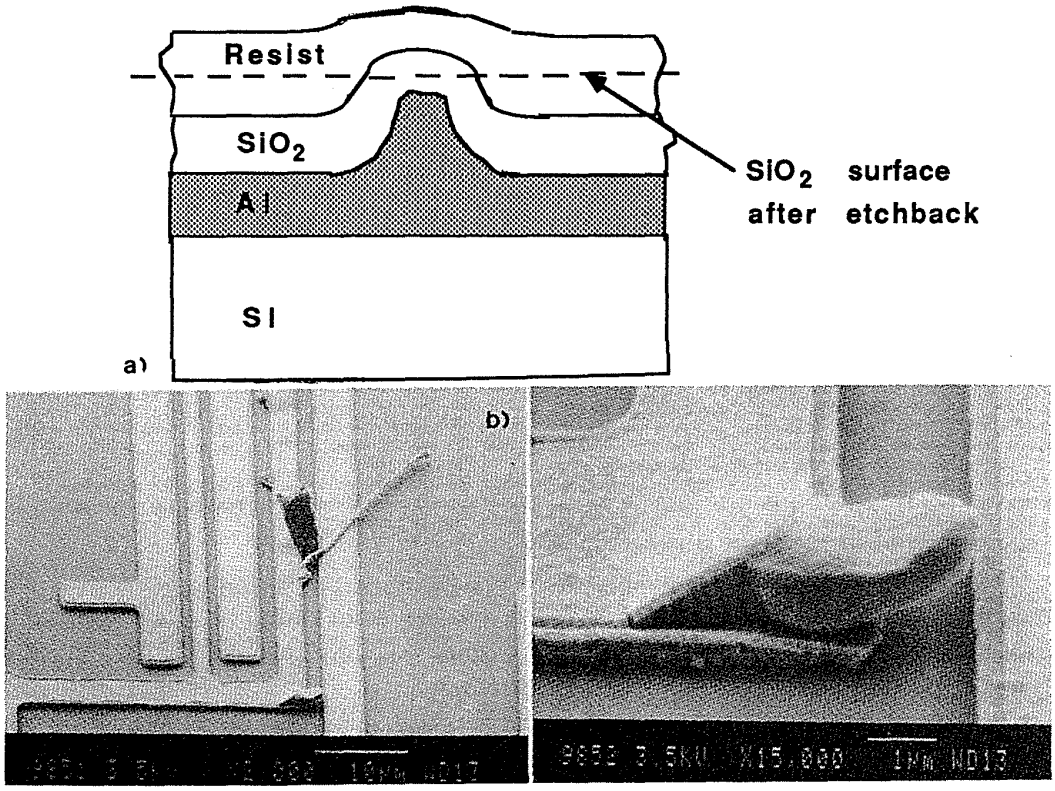

Fig. 4-54 (a) Schematic drawing of the thinning of photoresist over a hillock in the Al. During etching of the dielectric layer to open contacts the thinner resist may be completely eroded, causing the dielectric layer over the hillock to be etched. (b) Hillocks protruding from the sides of the metal lines, which may lead to intralevel shorts.[176] This paper was originally presented at the Fall 1988 Meeting of The Electrochemical Society, Inc. held in Chicago, IL.

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The following are several approaches that have been developed to alleviate the problem of hillock formation:

- *Adding elements that have a limited solubility in Al as alloys to the film.* The alloying element is added in excess of the solid solubility limit, causing precipitation in the grain boundaries. This can "plug" the grain boundaries, inhibiting vacancy migration and thereby inhibiting the rate of hillock growth. Copper has been found effective in this application. (Note that since electromigration is also a grain-boundary diffusion process, alloys that exhibit improved electromigration resistance also tend to be less prone to hillock growth.) In general, this approach reduces, but does not eliminate hillock formation.

- *Depositing a capping layer of W or Ti on top of the Al film.*[173,174,175] Note, however, that the cap layer may increase the propensity of the films to form sidewall hillocks, which can lead to more intralevel shorting. A Ti cap layer exhibited the fewest lateral hillock failures, according to one report.[176]

- *Layering Al films with one or more Ti layers* (Fig. 4-55a).[177] Apparently, the Al film must include some Si in order for hillock-free films to be produced. The resistivity of layered Al:Si/Ti films, however, is ~50% higher than the resistivities of Al:Cu or Al:Si films. In addition, unless a diffusion barrier is present between the layered Al film and the Si substrate, Si will be taken up from the substrate until the Ti layers are completely transformed to silicides.[178]

- *A W layer can be selectively deposited onto the patterned Al lines.* This can be accomplished because W preferentially nucleates on Al surfaces, allowing the layer to cover the sidewalls of the lines, as well as the top surface (Fig. 4-55b).[179,180] A thin (80 nm) W layer deposited onto a 150-nm-thick Al layer resulted in a Metal 1 film in which hillocks on vertical and lateral sidewalls were effectively suppressed and the electromigration resistance of the lines was greatly improved. A hydrogen-reduction process (carried out at 300°C to prevent hillocks from growing on the Al surfaces) was used to deposit the W at a rate of 2.5 nm/min. Another report indicated that such selectively W-clad Al films demonstrated dramatically improved reliability, even with 0.6-μm-wide lines.[181]

- *A low compressively stressed intermetal-dielectric layer of PECVD SiO_2 is deposited so rapidly that hillock formation is not initiated until sufficient SiO_2 material has been deposited to suppress the formation.*[182] In this process, hillocks still form – but if the start of the deposition can occur within 10 seconds of the wafer's being placed on the hot susceptor, and if the deposition rate can exceed 300 nm/min, very few hillocks > 0.5 μm in height will occur (Fig. 4-55c).

- *A dielectric deposition process can be used whose temperature of deposition is lower than the temperature at which hillocks form.* Examples of such processes include:

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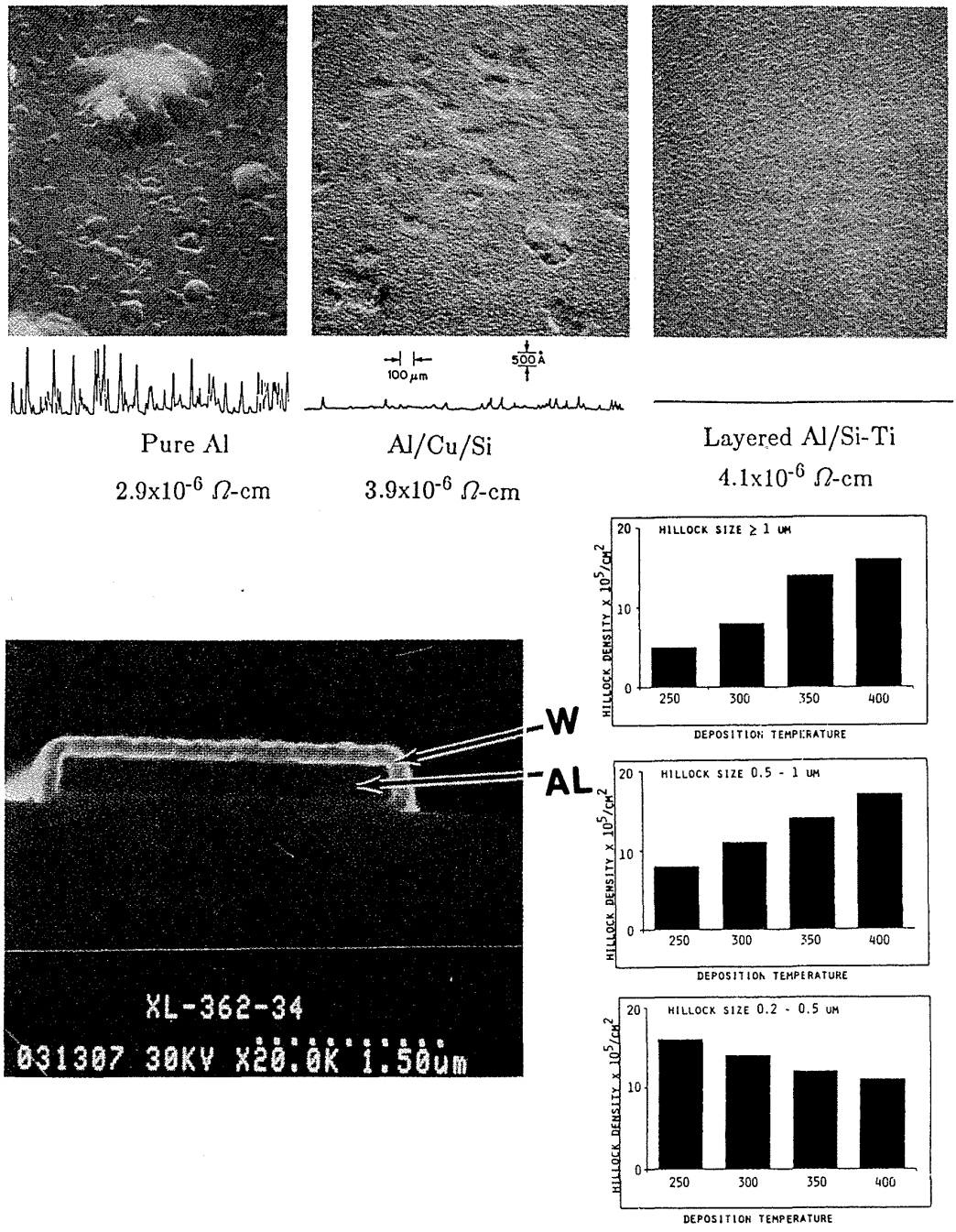

Fig. 4-55 (a) Comparison of hillocks formed in pure Al, Al/Cu/Si, and layered Al/Si:Ti films following an anneal at 450 °C for 30 min.[177] (© 1985 IEEE). (b) CVD W selectively deposited on an Al runner.[179] (© 1986 IEEE). (c) Hillock distribution on cold-sputtered Al after deposition of 0.9-μm SiO_2 at various temperatures. The time at temperature prior to deposition was held constant at one minute.[182] (© 1987 IEEE).

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- PECVD TEOS film, deposited at 330°C. (Figure 4-54c shows that the resulting hillock size and density are both small.)[172]
- ECR deposition (see section 4.4.10).
- Photo-CVD SiO_2.[183]
- Afterglow-CVD of SiO_2.[24]
- Anodized Al deposition.[184]

Once such dielectric films are in place, they suppress hillock growth during later thermal cycling.

• *Use of refractory metal films such as W or Mo (which exhibit much less propensity to form hillocks at 400°-500°C) in place of Al.*

• *Use of an ionized cluster beam deposition process to deposit smooth Al/CaF_2/Si films.* According to the report on this process, the films remained hillock free up to temperatures of 500°C.[185]

4.7.4.2 Dielectric Void Reliability Problems. If the voids are opened following an etchback step, they can trap moisture or photoresist residues that can cause long term reliability problems. In addition, metal may be deposited into the voids that can be very difficult to remove by etching, thus producing shorting between neighboring metal lines.

4.8 PASSIVATION LAYERS

Following patterning of the final metal layer, a *passivation layer* is deposited over the entire top surface of the wafers. This is an insulating, protective layer that prevents mechanical and chemical damage during assembly and packaging. The desired properties of the passivation materials are given in Table 4-5. In general, the thicker the passivation layer the better, since a thicker layer will provide better protection and improve the electromigration resistance of underlying Al lines. On the other hand, because thicker CVD films (especially silicon nitride films) have a higher tendency to crack, there is normally an upper limit to the thickness.

The final mask, called the *pad mask* or *bonding contact mask,* is used to define patterns corresponding to the regions in which electrical contact to the finished circuit will be made. These patterns in a resist layer allow openings in the passivation layer to be etched down to Al areas on the circuit called bonding pads (see chap. 5, Fig. 5-16). Either wet or dry etching can be used to etch the passivation layer. Since the dimensions of the pads are so large (i.e., normally 100 x 100 μm), wet etching is still frequently used to etch PSG films, while silicon nitride films are more easily etched by means of a dry etching process.

Phosphorus-doped, low-temperature CVD SiO_2 films were the first passivation layers to be used. The phosphorus is added to the SiO_2 to reduce the stresses in the film (and to thereby decrease the tendency of the film to crack), as well as to improve the gettering

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properties of the film (with respect to sodium ions and other fast-diffusing metallic contaminants). The higher the phosphorus concentration, the better these characteristics will be.

On the other hand, if more than 6 wt% phosphorus is added to the film, corrosion can become a serious problem, especially in the case of chips mounted in plastic, nonhermetic packages. Water vapor can rapidly penetrate the plastic packaging material, transporting with it contaminants from the surface of the package. If the PSG contains excess phosphorus, the moisture can react with it to form phosphoric acid (HPO_3), which will eventually penetrate the film. As noted earlier, electrochemical corrosion of the Al lines can lead to metallization failure. While the transport of contaminated moisture through the PSG is a relatively slow process, if cracks or defects (e.g., pinholes) exist in the film, the water vapor will be able to penetrate it much more rapidly.

Silicon nitride has also been used as a passivation-layer material because it provides an impermeable barrier to moisture and mobile impurities (e.g., sodium) and also forms a tough coat that protects the chips against scratching. Its high dielectric constant is not a disadvantage for this application, since the passivation layer is deposited on top of the last metal layer.

However, because the passivation layer must be deposited over Al films, only PECVD silicon nitride can be used for this application (since it is deposited at ~300°C). Unfortunately, PECVD nitride films normally exhibit a high mechanical stress (~6-8 x 10^8 Pa), which can cause cracks in the film during heating after deposition (especially at steps). The high compressive stresses in the films have also been shown to enhance void formation in Al interconnects (see section 4.7).

In addition, PECVD silicon nitride tends to be nonstoichiometric and contains substantial quantities of atomic hydrogen (10-30 at%). Large quantities of hydrogen have been found to accelerate hot-electron aging effects in MOS devices (see section 5.6.6). It has also been reported that the hydrogen from PECVD nitride is responsible for the formation of bubbles or cavities at the metal–plasma nitride interface when Al:Si alloys are used as the metallization. These appear after the 450°C anneal that is carried out following nitride deposition. It is supposed that the hydrogen reacts with the Si precipitates in the Al film to form gaseous compounds that produce the bubbles.[186,187] It has been recommended that a low-hydrogen-content passivation film be used, if nitride passivation is selected for MOS technologies with gate lengths of less than 1.5 μm (in which hot-electron degradation is significant).

Work has been done to develop processes for growing nitride films with low hydrogen concentration and stress, and more is now understood about the relationship of the film properties to such deposition conditions as rf frequency, power, and bias.[188] Lower H_2 concentrations in the nitride have been obtained when the film is formed with SiH_4-N_2 mixtures rather than with conventional SiH_4-NH_3 mixtures.[189] Fluorinated nitride (F-SiN) films have been developed that exhibit only 0.6% of hydrogen (in the form of Si-H).[190,191]

The use of PECVD silicon-oxynitride films (deposited with SiH_4, NH_3, N_2, and N_2O mixtures) as alternative passivation materials has also been investigated, since they exhibit nearly the same the moisture and sodium barrier characteristics of nitrides.

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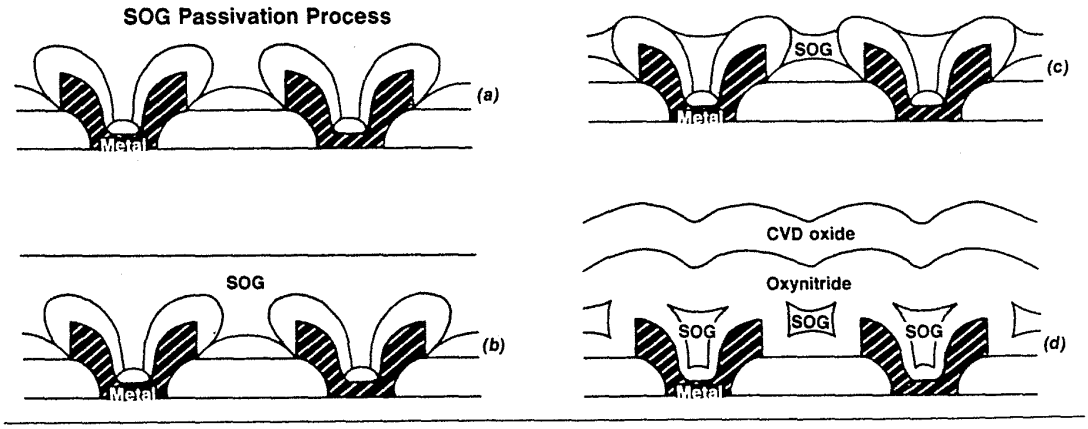

1. (a) Deposition of the first oxynitride layer, (b) SOG applied, (c) after SOG etch back, and (d) finished passivation process after second oxynitride and CVD oxide depositions.

Fig. 4-56 Using SOG film as a part of the passivation overcoat improves EPROM reliability.[256] Reprinted with permission of Semiconductor International.

While not quite as good as those of nitrides, the characteristics are better than those of oxides.[192] However, their stress is between that of APCVD oxide (tensile) and plasma nitride and oxide (compressive).[193] In addition, because the stress is a function of applied rf power, pressure, and bias, it is possible to optimize the stress by using bias. Ideally, a very low-stress dielectric oxynitride film can be formed that will still maintain good diffusion-barrier properties. (It is important to characterize the stress over the entire temperature range of operation to which the dielectric film will be subjected, since the stress can exhibit hysteresis effects. These may be due to structural changes in the film due to loss of material during heating.) Finally, it is reported that PECVD oxynitride films can be formed that contain considerably less H_2 (~one-half, in one report) than do PECVD nitrides.[194]

Another, more recently adopted approach to the formation of passivation layers involves multilayer passivation coating. An initial coating of PECVD oxide is deposited, followed by a PECVD nitride. The oxide layer reduces the mechanical stress (~40%) and the hydrogen content of the passivation layer, while the nitride protects the device against handling, humidity, and mobile ions. This inorganic bilayer may be followed by a polyimide layer that is several microns thick (especially useful in automated bump-bonding processes) and a thick layer of silicone gel, or similar material, for cushioning and for void elimination during die bonding.

In a second variation of this technique applied to EPROMs, a sandwich oxyntride-(etchedback) SOG-oxynitride layer is first formed. This film is then covered with a low phosphorus- content CVD-oxide layer to complete the composite passivation film (Fig. 4-56). Sandwiching the SOG film between the two oxynitride layers reduces the occurrence of voids and seams in the passivation layer. These voids and seams caused degraded passivation film coverage, which in turn correlated with increased EPROM array failures after steam stressing.[256]

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Table 4.5 Desired Properties of a Passivation-Layer Material

1. Provides good scratch protection to underlying circuit structures. In general, the thicker the passivation layer the better, subject to cracking and patterning restrictions.
2. Impermeable to moisture, as moisture is one of the main catalysts for corrosion.
3. Exhibits low stress, preferably compressive (~$5x10^8$ dynes/cm^2).
4. Conformal step coverage.
5. High thickness uniformity.
6. Impermeable to sodium atoms and other highly mobile impurities.
7. Easily patterned.
8. Good adhesion to conductors, as well as to the interlevel dielectric beneath the last level of metal.

4.9 SURVEY OF MULTILEVEL METAL SYSTEMS

As noted earlier, with NMOS IC technology it was possible to exploit the polysilicon layer as an extra level of interconnect, while in bipolar technology it was necessary to develop a two-level-metal system in order to obtain comparable flexibility of interconnect routing. As a result, the problems of two-level-metal systems (primarily, the implementation of low-temperature planarization techniques) first had to be tackled by bipolar IC manufacturers. When CMOS replaced NMOS as the dominant MOS VLSI technology, CMOS ICs also required a two-level-metal system, since the polysilicon could not perform the function of a local interconnect level as effectively as it had in NMOS (see chaps. 2 and 6). However, the polysilicon gate structures and the nonrecessed LOCOS field-oxide steps in CMOS created an even more difficult topography for two-level-metal CMOS systems than for bipolar systems.

4.9.1 Bipolar Double-Level-Metal Systems

The first example we present is that of a structure described in 1984 by Ghate et al. of Texas Instruments.[195] The Metal-1 pitch is 4 μm, and the Metal-2 pitch is 6 μm. Metal 1 is a 575-nm-thick bilayer film of Ti:W covered with Al:Cu, and the contact to silicon is made by self-aligned PtSi formed in the contact holes. Metal 2 is also a bilayer film of Ti:W and Al:Cu, 775 nm thick. The intermetal-dielectric layer is a 600-nm-thick PECVD oxide layer in which 1.1-μm vias are opened to allow contact between Metal 2 and Metal 1. No planarization of the intermetal dielectric was reported for this DLM process.

A second example, detailed by Bergeron et al. of IBM, uses a bilayer PECVD silicon-nitride/polyimide film as the intermetal dielectric. Smoothing of the underlying metal topography is achieved through use of the polyimide.[196] The Metal-1 pitch is 5 μm and the Metal-2 pitch is 7.0 μm. Metal 1 and Metal 2 are both Al:4%Cu films defined by lift-off, and Metal 2 is 2 μm thick. The bilayer intermetal-dielectric film is etched by

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means of two masking and etching steps. In the first, an oversized via opening in the polyimide is defined and etched through an isotropic dry-etch step. In the second, a smaller via in the nitride is defined and dry etched.

4.9.2 CMOS Double-Level-Metal Systems

The following DLM processes are listed according to the generation of CMOS technology for which they were reported to be designed, as specified by the minimum MOS device gate length.

4.9.2.1 Nonplanarized DLM (2.0-μm CMOS). An example of a two-level-metal CMOS interconnect structure that does not rely on any planarization methods was presented by Smith et al. of Intel (Fig. 4-57a).[197] The Metal-1 pitch is 5.0 μm, and the Metal-2 pitch is 6.0 μm. Metal 1 and Metal 2 are Al:Si films, and the intermetal dielectric is an oxynitride composite film. Metal 2 is used to strap the polysilicon lines in order to reduce the word line delay in SRAMs built with this technology. Via-hole sloping is achieved by implanting the top surface of the oxynitride. Note that contact between poly and the Si substrate is made with *butted contacts* (see chap. 3).

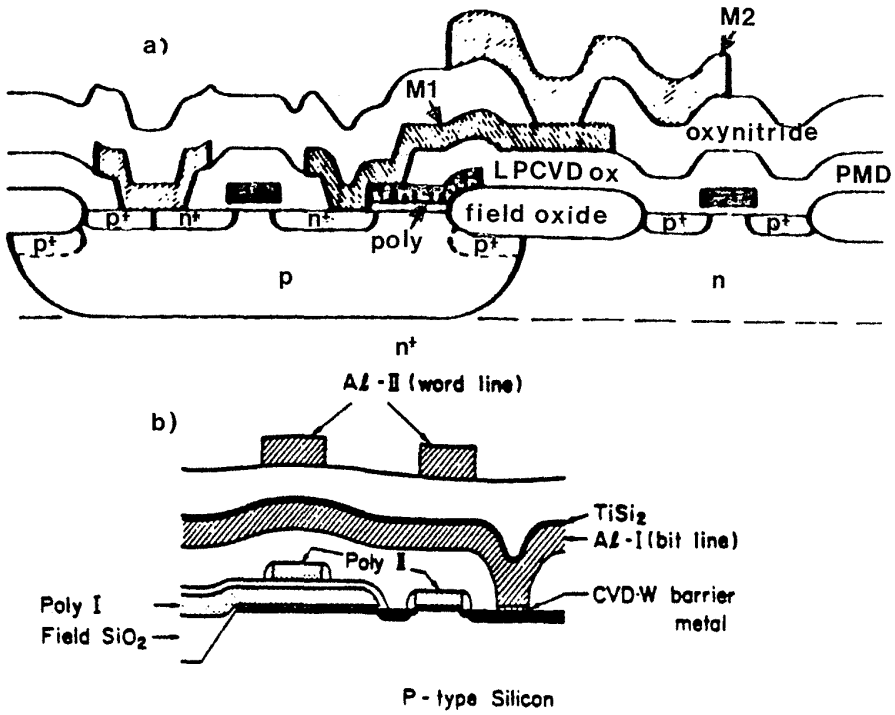

Fig. 4-57 (a) Example of a double-level-metal CMOS process with no planarization.[197] (© 1984 IEEE). (b) DLM process with a CVD W barrier metal and $TiSi_2$ hillock-suppression layer on top of the Metal-1 Al layer.[200] (© 1984 IEEE).

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4.9.2.2. Nonplanarized DLM: CVD W Metal (2.0-μm NMOS). A two-level-metal NMOS process that uses CVD W for both Metal 1 and Metal 2 was described by Mikkelson et al. of Hewlett-Packard.[198] The Metal-1 pitch is 3.0 μm; the Metal-2 pitch is 8 μm and the Metal-2 film thickness is 1.8 μm. The intermetal dielectric is CVD SiO_2. The tungsten is deposited by means of a blanket CVD process, and an underlying "glue layer" of CVD WSi_2 is used to provide good metal-layer adhesion to the SiO_2. No planarization was reported, possibly because of the good step coverage provided by the CVD W process.

4.9.2.3 Resist Etchback, Bias-Sputtered SiO_2, and SOG DLM for 1.5-μm CMOS. Four examples of two-level-metal processes for 1.5-1.25-μm CMOS are the following:

1. Barton and Maze of Hewlett-Packard described a DLM process that uses Al metallization and a sacrificial etchback dielectric planarization process.[199] The Metal-1 pitch is 4.0 μm, and the Metal-2 pitch is 4.0 μm. A bilayer of silicon oxynitride and silicon nitride is partially planarized through a resist etchback process (see section 4.8). The vias are 1.6 x 1.6 μm and can be placed anywhere except over contact holes.

2. Another two-level-metal, double-polysilicon process (for 1-Mbit DRAMs) was presented by Shibata et al. of Toshiba.[200] A low-resistivity polycide structure is used for Poly 1 (for bit lines); polysilicon is used for Poly 2, but was strapped with Metal 2 to reduce the delay of the word lines. A 50-nm-thick selective W film is used to make contact to the n^+ source and drain regions (and to serve as a diffusion barrier layer). A resist-etchback technique provides planarization of the PECVD SiO_2 intermetal dielectric. A layer of $TiSi_2$ is deposited onto Metal 1 lines to prevent hillock formation during processing (Fig. 4-57b).

3. Monk et al. of Westinghouse outlined a DLM process that employs bias-sputtered SiO_2 as the intermetal dielectric.[201] The first-level metal is a trilayer film of Ti:W, Al, and Ti. The Ti top layer is used to prevent hillock formation. Contact to the silicon is made by self-aligned PtSi formed in the contact holes. The Metal-1 pitch is 3.0 μm, and the Metal-2 pitch is 4.0 μm. The intermetal sputter-deposited SiO_2 serves to smooth the steps of the dielectric layer by forming steps with 45° angles over the metal edges. A two-step etch process is used to form tapered vias. Metal 2 consists of a bilayer of Al covered with Ti. The Ti serves as an antireflection coating during lithography, as well as an anti-hillock-forming layer. An overetch of Metal 2 is used to clear stringers that remain in the most severe lithography.

4. The final CMOS DLM example uses a nonetchback sandwich SOG process as the planarization method. It also uses PtSi contacts and Ti:W/Al:Cu/Ti:W trilayers for Metal 1 and Metal 2. The passivation film is a PECVD oxide/PECVD nitride bilayer. The intermetal dielectric consists of an underlayer of PECVD

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SiO_2 (200-nm thick), a layer of carbon-containing SOG, and a 500-nm top layer of PECVD SiO_2.[202]

4.9.2.4 Nonsacrificial Layer Etchback DLM (1.0-μm CMOS). A two-level-metal process that uses a nonsacrificial etchback step of a plasma-enhanced TEOS SiO_2 layer was outlined by Thoma et al.[172] and by Hills et al.,[203] all of of AT&T Bell Laboratories. It was designed for use in a twin-tub, 1.0-μm CMOS technology. The nonetchback planarization provides smoothing of the intermetal- dielectric layer, as was described in section 4.4.3. The Metal-1 pitch is 2.0 μm, and the Metal-2 pitch is 3.5 μm. Metal-1 thickness is 0.5 μm, and 1.5-μm-wide vias are used. (The dielectric etchback process was described in section 4.4.3.)

A more recent, and slightly more complex version of this process is presented in reference 235. Here, a resist-etchback step is used to planarize the PETEOS layer, and a proprietary technique is used to slope the sidewalls of the first Al layer. Vias are sloped with an isotropic/anisotropic etch, and the nominal via depth varies from 800 to 1400 nm. Adequate step coverage is achieved in even the deepest vias when a 400-nm-deep isotropic etch is used. This is an example of a relatively simple DLM process that can be extended to triple-level-metal structures.

4.9.2.5 Alternative CMOS DLM Process with Ti:W/Mo as Metal 1. DLM processes for most nonsubmicron CMOS technologies use Al alloys for Metal-1 and Metal-2 layers. Although CVD W has been extensively investigated as an alternative metallization material for overcoming the problems of Al conductor layers (especially for Metal 1), another, less widely used approach employs a bilayer of Ti:W/Mo. A report of a complete DLM process that uses such a bilayer has recently been presented by Hawley et al. of Xicor.[204] The Mo offers excellent electromigration and hillock resistance and alleviates the problem of junction spiking.

In this process, Ti:W makes contact to the Si. In order to establish low contact resistance to PMOS source and drain regions, it's necessary to perform a 625°-700°C sinter step following Metal 1 deposition. An etchback sandwich SOG dielectric layer is used as the intermetal dielectric film, and Al:Cu is used as the Metal-2 film. The Ti:W/Mo layer is dry etched in an SF_6 + Ar mixture. An in situ sputter-etch is performed before the Metal-2 Al:Cu film is sputter deposited, which yields a low contact resistance (1.25 $\mu\Omega$-cm^2) between Metal 1 to Metal 2.

4.9.2.6 DLM Processes for Submicron CMOS. The following is a survey of some DLM processes for submicron CMOS. These are more complex than the processes used for less advanced CMOS technologies.

- The first example of a DLM process that utilizes resist-etchback planarization for both the PMD and the intermetal-dielectric layers was described by Chapman et al. of Texas Instruments (Fig. 4-58).[205] This process was designed to be used in a 0.8-μm CMOS technology. The Metal-1 and Metal-2 pitches are both 2.6 μm, and the contact and via sizes are 0.8 μm. The PMD layer is bilayer of LPCVD TEOS and PECVD SiO_2.

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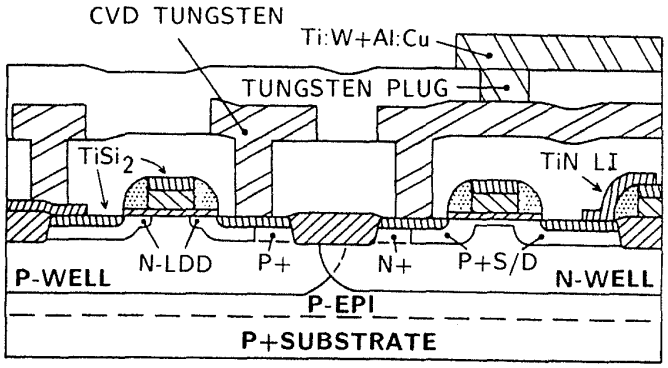

Fig. 4-58 Schematic cross section of a 0.8-μm CMOS DLM process.[205] (© 1987 IEEE).

The TEOS layer is deposited and then planarized by means of a resist-etchback technique prior to deposition of the phosphorus-doped PECVD SiO_2 layer. A blanket CVD W layer is deposited into the contact holes and also serves as the Metal-1 material. The CVD W makes contact to the self-aligned $TiSi_2$ contact structures. The intermetal dielectric is PECVD SiO_2, which is also planarized using a resist etchback technique. The vias are completely filled with selective CVD W.

The Metal-2 film consists of Ti:W covered with Al:Cu. The passivation layer is a plasma oxide/nitride bilayer film. Because no flow or reflow steps are used following $TiSi_2$ formation, low contact resistivity to the PMOS source/drain regions can be maintained by the $TiSi_2$.

• In the second process example, presented by Higelin et al. of Siemens,[206] planarization of both the PMD and the intermetal dielectric is performed. The PMD is LPCVD TEOS, which is planarized by using a resist-etchback process. A 200-nm-thick TEOS film is then deposited to ensure good isolation between poly and Metal 1. Blanket CVD W and etchback are used to fill the contact holes, with a Ti/TiN diffusion barrier under the W layer. Metal 1 consists of an Al:Si:Ti film. The intermetal-dielectric layer consists of a trilayer structure, with etched-back SOG or polyimide as the material in the middle. Blanket CVD W is used to fill the via, which is then etched back (using polyimide as the sacrificial layer). An Al:Cu:Si film is used as Metal 2.

• The third process was detailed by R. de Werdt et al.[207] and T. Doan et al,[208] both of Phillips Research Labs. It utilizes a single polysilicon layer with a $TiSi_2$ local interconnect structure to connect poly lines and diffused regions, selective CVD W as a contact-hole-filling material, and Al:2%Cu as both Metal 1 and Metal 2. Ti:W is used as a nucleation layer for the blanket CVD W and as an etchstop under the Al:Cu of Metals 1 and 2.

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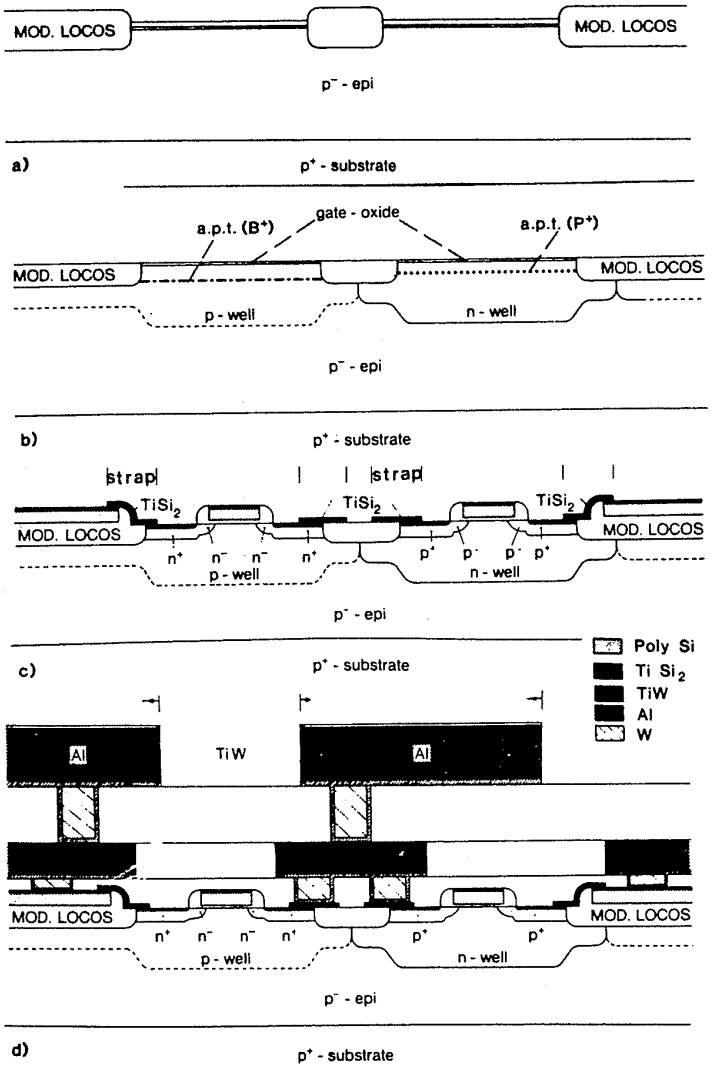

Fig. 4-59 Schematic cross section of submicron-CMOS DLM technology that uses: a fully planarized isolation structure; $TiSi_2$ over poly as a local interconnect; selective W as a contact hole plug; and Al:Cu for Metal 1 and Metal 2.[207] (© 1987 IEEE).

In this process, the substrate is completely planarized at the conclusion of the isolation formation procedure (Fig. 4-59). The PMD layer is likewise completely planarized, by means of a conformally deposited LPCVD TEOS process and a resist-etchback technique. Following the PMD resist etchback, a thin layer of BPSG is deposited for gettering and dielectric-layer integrity. An etchback SOG sandwich dielectric approach is used to planarize the intermetal dielectric. The vias are etched to give sidewalls with slopes of 80°, which allows adequate filling by the sputter-deposited Al:Cu Metal-2 film. The Ti:W etchstop layer under Metal 2 allows a 70% overetch step to be used with only 0.1-μm CD line loss in

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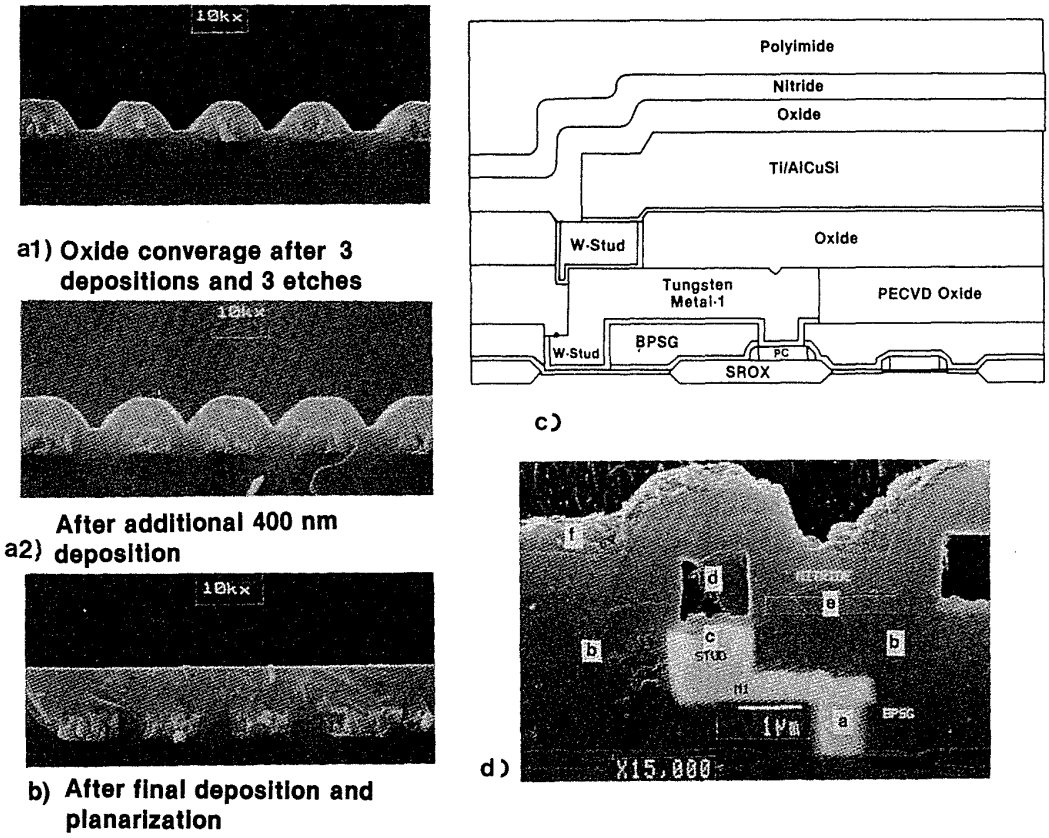

Fig. 4-60 Submicron-CMOS DLM process. (a) and (b) SEM photographs of CVD-oxide gap fill and planarization. (c) Cross section of the completed DLM structure. (d) SEM cross-sectional photograph of this structure.[128] (© 1987 IEEE).

Metal 2. A bilayer passivation film is used that consists of a 0.4-μm-thick PECVD oxide and a 0.3-μm-thick PECVD nitride.

The polysilicon width and spacing of this process are 0.7 μm and 0.9 μm, respectively. The Metal-1 and Metal-2 pitches are both 2 μm, and the minimum size for contact holes and vias is 0.9 μm.

• The fourth example was presented by C. Kaanta et al. of IBM.[209] Blanket CVD W is used to form studs in the contact holes and vias and also to form the Metal-1 layer. Void formation is avoided through optimization of the deposition temperature, pressure, and relative gas flows (Fig. 4-60). TiN serves as the adhesion layer under the CVD W.[130]

A special dry-etch process of W was developed to prevent attack down the sidewalls of the contact holes and vias during W overetch. A Cl_2/O_2 gas mixture gives good selectivity to BPSG or other deposited oxides. A silicon nitride film is also deposited over the CVD W to protect the W during overetch, since the resist-masking layer is rapidly eroded by the dry-etch conditions needed to successfully etch the W.

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A PECVD SiO_2 deposition/etchback process is used to fill the narrow spaces between adjacent metal lines (see section 4.4.7). As shown in Figs. 4-60a and b, a sequence of six thin CVD SiO_2 depositions – each followed by an etchback step – is needed to obtain filling of the narrow spaces. Another etchback technique (not specified in the paper) is used to completely planarize the surface. A final APCVD oxide is then deposited to provide a sufficiently thick dielectric film over the Metal-1 regions.

After the via holes have been opened and filled with CVD W (using an etchback step to planarize the W in the vias; Fig. 4-60c), the Ti/Al:Cu:Si Metal-2 film is deposited and patterned. A final passivation bilayer film of PECVD oxide and nitride is deposited and capped with a polyimide film.

The use of completely filled vertical contact holes and vias allows the use of unframed contact hole and via design rules, which significantly increases packing density.

• The fifth DLM process, proposed by H. Yamamoto et al. of Matsushita, is designed to be used in CMOS processes which require a 0.6-μm Metal-1 spacing and line width.[181] Al:Si Metal-1 and Metal-2 interconnects are clad by a 100-nm-thick layer of selective CVD W to improve electromigration and hillock resistance, as well as to increase the resistance of the lines to stress-induced voids. Selectively deposited W is also used to fill contact holes and vias (i.e., to completely fill the shallow ones and partially fill the deep ones). The intermetal dielectric is a photo-CVD and SOG multilayer film. The photo-CVD SiO_2 fills narrow spaces, and the SOG film fills the intermediate-dimension spaces.

4.9.3 Three-Level-Metal Systems

Most three-level-metal (TLM) systems have been designed for use in bipolar gate-array chips, probably for the same reasons that DLM processes were first developed in bipolar applications. Information on TLM processes for use with CMOS is also generally presented in less detail.

• An early TLM system for bipolar gate arrays was described in 1982 by Fried et al. from IBM (Fig. 4-61).[210] In this system, Metals 1, 2, and 3 were all Al:4%Cu films that were patterned by lift-off. The contact to silicon was made with PtSi and a Cr-Cr_xO_y diffusion barrier. The DM1 layer was bias-sputtered SiO_2, and DM2 and the passivation layers were PECVD SiO_2 that was etched back by bias sputtering.

• A second TLM system for a 10,000-gate ECL gate array was presented by Eggers et al. of Siemens in 1985.[211] This system utilizes a bilayer dielectric consisting of polyimide covered with PECVD nitride for DM1, DM2, and the passivation layer. The polyimide provides smoothing of the wafer topography. The nitride seals the polyimide, preventing it from absorbing moisture, and provides a surface to which Metals 2 and 3 can reliably adhere. The metallization for all three layers is an AlTiSi alloy, for good electromigration and hillock

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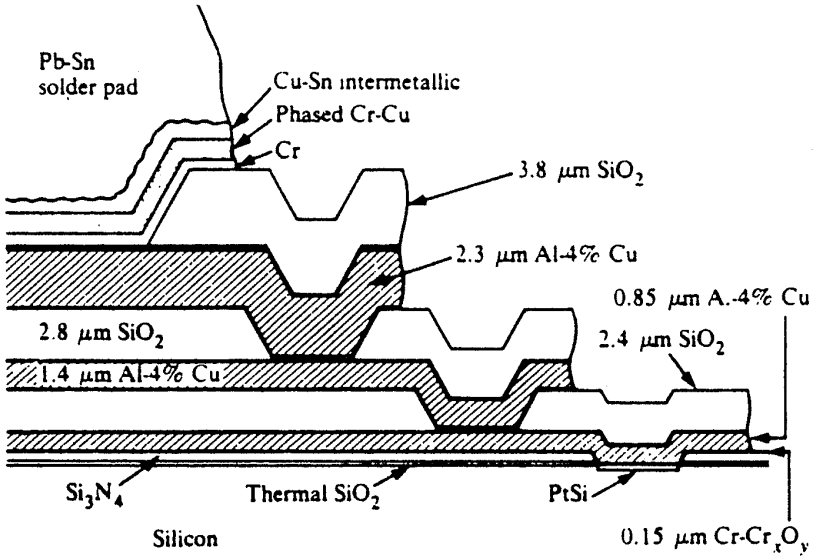

Fig. 4-61 Schematic of an early three-level-metal interconnect structure.[210] Copyright 1982 by International Business Machines Corporation. Reprinted with permission.

resistance. The pitches are 6 μm for Metal 1, 8 μm for Metal 2, and 10 μm for Metal 3. Reliability tests of circuits fabricated with this process and mounted in plastic packages showed excellent results.

• A third process was outlined in 1987 by Welch et al. of Texas Instruments.[212] Here, the premetallization dielectric topography is planarized by means of a resist-etchback technique, and a blanket CVD W process is then used to fill the contact holes. A planarizing resist is used to smooth the rough surface of the W film and the small dimples that remain over the contacts themselves. The etchback is stopped when 100-200 nm of W remain in the field regions. Ti:W is used as an adhesion layer for this W and for the W plugs in the contact holes. An Al alloy is used for the remainder of the Metal 1 layer. Blanket CVD W (including etchback) is also used to fill vias in DM1 and DM2.

• A fourth TLM process was presented by Moriya et al. of Toshiba in 1983.[213] In this structure, selective CVD W is used to fill the contact holes and make direct contact to Si, as well as to selectively fill vias in DM1 and DM2. A layer of $MoSi_2$ is deposited onto Metal 1 and Metal 2 to serve as a nucleating surface for the via-fill selective W process. Planarization of the CVD SiO_2 layers DM1 and DM2 is carried out by means of a resist-etchback technique.

• A fifth process uses CVD W for all metal layers, and polyimide capped with PECVD nitride as the intermetal dielectric layers.[214,216] Feasibility studies using this process produced working CMOS circuits.

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• A sixth TLM process, described by Manos et al. of Motorola, again used a blanket-deposited and etched W layer as the first-level-metal layer.[237] A combination-sputter deposited/CVD TiN layer was used as a contact diffusion-barrier film. Since W is the first metal material, the vias between Metal 1 and Metal 2 can be reflowed. However, great care must be taken during this reflow step to prevent the formation of tungsten oxide. Good via filling and low-contact-resistance vias can be achieved using this process.

4.9.4 Four-Level Metal Systems

Two four-level-metal processes have been described as of this writing. The first, reported by Bartush of IBM,[216] was used to fabricate 10,000-gate bipolar gate-array chips. Instead of patterning and filling vias in the intermetal-dielectric layers, studs are formed using a *lift-off* technique. Studs may be stacked to achieve interconnection between conductors that are more than one level away from each other (Fig. 4-62). Sacrificial etchback of resist layers is reported to be the technique used to planarize the intermetal-dielectric films. The first film is apparently deposited by means of a process that can fill the narrow spaces between studs/Metal 1 lines and that can provide partial planarization (e.g., a bias-sputtered SiO_2 film, a PECVD TEOS film, or an ECR-deposited SiO_2 film). The partially planarized topography is then completely planarized through resist etchback. The intermetal-dielectric films are composite nitride/oxide layers. The nitride is used to ensure that all of the studs are exposed prior to deposition

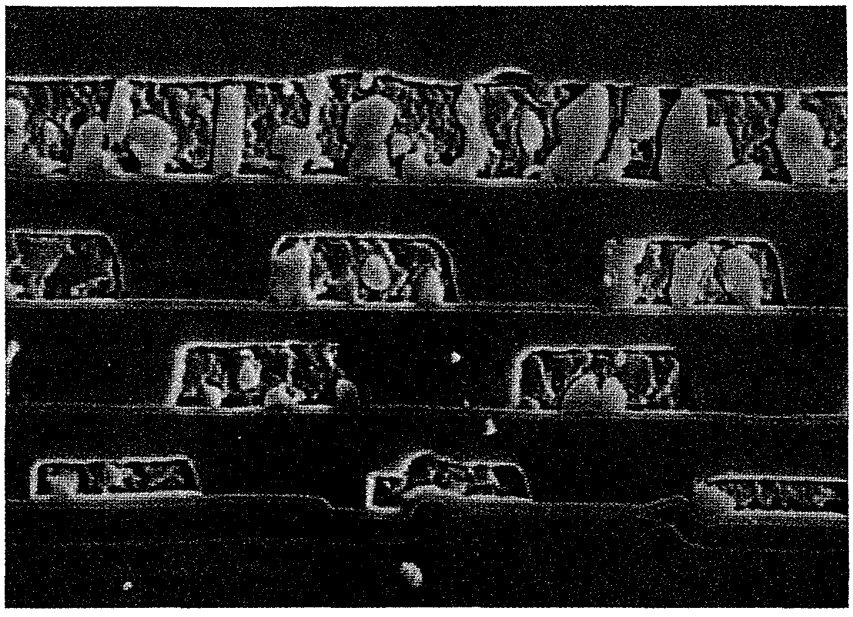

Fig. 4-62 SEM photograph of a cross section of a completed four-level-metal chip.[216] (© 1987 IEEE).

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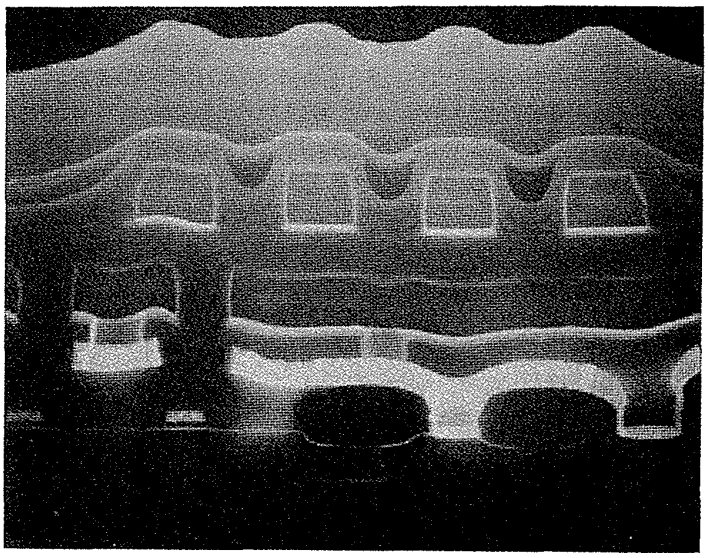

Fig. 4-63 SEM photograph of another completed four-level-metal interconnection structure.[236] (© 1988 IEEE).

of the next metal-level film, and it is left in place to become part of the bilayer film for subsequent intermetal dielectrics.

The second four-level-metal process was described by Nishida et al. of Hitachi (Fig. 4-63).[236] A minimum 0.6-μm feature size is employed. Sputtered W is used as the first level metal, and spin-on glass sandwich structures are used to planarize the intermetal-dielectric layers. Layered Al/TiN films were used for the other metal levels. A variety of circuits have been fabricated with this technology, including a 1-μm CMOS SRAM and a BiCMOS gate array with macro cells.

4.10 SUMMARY OF MULTILEVEL-INTERCONNECT-TECHNOLOGY REQUIREMENTS FOR VLSI

• *A planarized wafer topography at the end of the isolation-formation process* (see chap. 2 for discussion of various approaches that have been proposed to achieve this).

• *A planarized topography over the local-interconnect level* (e.g., over polysilicon or silicide). This can be accomplished through glass flow (probably by means of RTP, to maintain shallow junctions in devices) and etchback techniques.

• *Complete filling of contact holes and vias.* This will probably be achieved through the use of such processes as CVD of W or Al (blanket or selective), bias-sputtered planarized Al, laser-planarized Al, pillar formation, or selective electroless deposition.

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• *Processes that result in complete global planarization of interlevel-dielectric surfaces.* Such processes are described in sections 4.4 and 4.6.

• *Unframed and vertically-etched vias.*

• *Interconnect materials with low resistivity, hillock resistance, high electromigration-resistance, and compatibility.*

• *An appropriate passivation layer.*

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PROBLEMS

4.1 Why is the parasitic capacitance per unit area smaller for Metal 1 on field oxide, but much larger for the polysilicon lines on field oxide?

4.2 (a) Calculate the RC time constant of a 0.5-μm-thick Al line formed on 0.5 μm-thick thermally grown oxide. The length and width of the line are 1 cm and 1 μm, respectively. The resistivity of the line is 10^{-5} Ω-cm. (b) What will be the RC time constant for a polysilicon line ($R_{sh} = 30$ Ω/sq) of identical dimensions?

4.3 Metal lines of varying widths are fabricated. Before being patterned, the sheet resistance of the metal film is measured and is found to be 2.5 Ω/sq. Find the total resistance of 0.5, 1, 2, and 5 μm wide and 1 cm long lines. What other information is still needed before it can be determined what type of metal makes up these lines?

4.4 The design of a circuit requires that a maximum permissible current density of 2×10^5 A/cm^2 through a conductor 1 mm long, 1 μm wide, and nominally 0.5 μm thick. Assume that 10% of the conductor length passes over steps and at these locations is 50% of the nominal

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metal vim thickness. What maximum voltage may be used across the conductor if the sheet resistance is 5.6×10^{-2} Ω/sq?

4.5 Given a via that is 1 μm wide and 0.7 μm deep, estimate the step coverage of a conventionally sputtered film into the via if the via is: (a) unfilled, (b) 25% filled, and (c) 50% filled.

4.6 A metal film having a temperature coefficient of expansion of 27×10^{-6} per degree K is deposited on a Si wafer, which has a temperature coefficient of expansion of 9×10^{-6} per degree K. The wafer is then heated to 450 °C. Calculate the stress generated in the film when cooled to 25 °C.

4.7 What is the maximum current that can be allowed to flow in an Al conductor 1 μm thick and 4 μm wide if the current density is not to exceed 5×10^5 A/cm^2?

4.8 (a) What is the sheet resistance of a 1-μm-thick Al-Cu-Si line which has a resistivity of 3.2 μΩ-cm? (b) What is the capacitance of this line to the substrate if it is on a thermal oxide that is 600 nm thick? (c) What is the RC product associated with this 500-μm line?

4.9 Repeat problem 4.8 for a polysilicon line with a resistivity of 500 μΩ-cm.

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