UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner
v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No.: IPR2025-00119
U.S. Patent No. 10,879,254
Issue Date: December 29, 2020

Title: THREE - DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME

DECLARATION OF DR. JACK C. LEE IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 10,879,254

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I, Dr. Jack C. Lee, declare as follows:

I. INTRODUCTION

1. I have been retained by Micron Technology, Inc. ("Micron") as an independent expert consultant in this proceeding before the United States Patent and Trademark Office ("PTO"). I am not an employee of Micron or any affiliate or subsidiary of Micron.

2. I have been asked to consider whether certain references disclose or teach the features recited in claims 1-15, 17-18, and 20 of U.S. Patent No. 10,879,254, which I refer to herein as the '254 Patent.

3. My opinions and the bases for my opinions are set forth below.

4. I am being compensated at my standard consulting rate of $680 per hour for my time. My compensation is based solely on the amount of time that I devote to activity related to this case and is in no way contingent on the nature of my findings, the presentation of my findings in testimony, or the outcome of this or any other proceeding. I have no other financial interest in this proceeding.

II. BACKGROUND AND EXPERT QUALIFICATIONS

5. My *curriculum vitae* ("CV") is attached hereto as Ex. 1004 and provides an accurate identification of my background, experience, and qualifications as an expert in electronics and NAND memory technology.

6. I received a B.S. degree in Electrical Engineering, with highest honors, in 1980, and an M.S. degree in Electrical Engineering in 1981, both from University of California, Los Angeles. I received a Ph.D. degree in Electrical Engineering in 1988 from University of California, Berkeley ("UC Berkeley").

7. From 1979 to 1984, I was a Member of Technical Staff at the TRW Microelectronics Center, in the High-Speed Bipolar Device Program. I worked on bipolar device/circuit design, fabrication, and testing. I was promoted to Engineering Group Leader level in 1983.

8. I received several academic honors while at UC Berkeley. For example, I won the Best Paper Award from the Institute of Electrical and Electronics Engineers ("IEEE") International Reliability Physics Symposium in 1988. I was also awarded a Lectureship with my own teaching assistant from UC Berkeley.

9. After receiving my Ph.D. in August 1988, I joined the faculty at The University of Texas at Austin ("UT Austin"). As a faculty member, I have taught numerous courses in semiconductor device fabrication and design, at both the undergraduate and graduate levels. This includes classes relating to, among other things, 3D NAND technology. I have supervised over 40 students who received their doctoral degrees under my guidance. Since September 2000, I have held the Cullen Trust for Higher Education Endowed Professorship in Engineering in the

Department of Electrical and Computer Engineering at UT Austin. In September 2023, I was promoted to the Professor Emeritus level.

10. My current research and teaching interests include semiconductor devices, semiconductor memory applications (including non-volatile memory), fabrication processes, silicon-on-insulator technologies, electrical and material characterization, reliability and modeling, packaging technologies, dielectric and passivation processes, display technologies, photovoltaic and solar cell technologies, high-K gate dielectrics and electrode, and alternative channel materials. I routinely encounter and address topics relating to NAND flash memory, and more specifically 3D NAND flash memory, in my research. My research has been partially supported by grants from the National Science Foundation, the Texas Advanced Research Program, the Semiconductor Research Corporation (SRC), SEMATECH, Texas Emerging Technology Funds, and others.

11. I have authored over 600 journal publications and conference proceeding papers and have coauthored 8 books and book chapters on semiconductor technologies. Many of these relate to the structure and operation of memory devices, including non-volatile memory such as NAND flash memory and 3D NAND flash memory. I am a named inventor of 9 U.S. patents. I have also received numerous teaching and research awards, e.g., inventor recognition and best paper awards.

12. In 2002, I became an IEEE fellow for my "contributions to the understanding and development of ultra-thin dielectrics and their application to silicon devices." I was also an IEEE Electron Devices Society Distinguished Lecturer from 2004 to 2016.

13. I have served in various technology consulting and business advisor roles. For example, I have taught short courses on semiconductor device physics and technologies at various semiconductor companies and consortiums (e.g., SEMATECH). I have also organized several international conferences and have given lectures at numerous conferences and symposia, including the International Symposium on VLSI Technologies, the IEEE Symposia on VLSI Technology, and the IEEE International Electron Devices Meeting. These conferences are some of the most prestigious in the field.

III. ASSIGNMENT AND MATERIALS CONSIDERED

14. I have been asked to provide analysis and explain the subject matter of the '254 Patent, including the state of the art when the application underlying the '254 Patent was filed. I have also been asked to consider, analyze, and explain certain prior art to the '254 Patent including how that art relates to claims 1-15, 17-18, and 20 (which I refer to as the "challenged claims") of the '254 Patent and to provide my opinions regarding whether that art invalidates the challenged claims.

15. The opinions expressed in this declaration are not exhaustive of opinions I may offer in the future regarding the unpatentability of the challenged claims of the '254 Patent. Therefore, the fact that I do not address a particular point should not be understood to indicate an agreement on my part that any claim complies with the requirements of any other applicable rule.

16. I reserve the right to amend and supplement this declaration in light of additional evidence, arguments, or testimony presented during this IPR or related proceedings on the '254 Patent.

17. In forming the opinions set forth in this declaration, I have considered and relied upon my education, knowledge of the relevant field, knowledge of scientific and engineering principles, and my experience. I have also reviewed and considered the '254 Patent (Ex. 1001), its prosecution history (Ex. 1002), and the following additional materials:

EXHIBIT NO.	DESCRIPTION
1005	U.S. Patent No. 10,777,501 to Nakajima et al. ("Nakajima")
1006	U.S. Patent Publ. No. 2019/0198524 to Fujiki et al. ("Fujiki")
1007	U.S. Patent No. 10,658,378 to Tao et al.
1008	Micheloni, "3D Flash Memories" (2016)
1009	U.S. Patent Publ. No. 2017/0179026 A1 to Toyama et al.

EXHIBIT NO.	DESCRIPTION
1010	U.S. Patent No. 10,354,980 to Mushiga et al. ("Mushiga")
1011	U.S. Patent Publ. No. 2019/0229125 to Zhou et al.
1012	PCT Publication No. WO 2019/042103 A1 to Dai et al.
1013	U.S. Patent No. 10,679,721 to Kim et al.
1014	Aritome, "NAND Flash Memory Technologies" ("Aritome")
1015	U.S. Patent No. 10,290,643 to Kai et al. ("Kai")
1016	U.S. Patent No. 9,859,297 to Park et al. ("Park")
1017	U.S. Patent Publ. No. 2018/0308559 to Kim et al. ("Kim")
1018	U.S. Patent No. 8,945,996 to Tang et al.
1019	U.S. Patent No. 10,115,632 to Masamori et al.
1020	U.S. Patent No. 5,945,717 to Chevallier
1021	U.S. Patent No. 10,347,487 to Lee et al.
1022	Ronse, "Optical lithography—a historical perspective," C. R. Physique 7 (2006) ("Ronse")
1023	U.S. Patent Publ. No. 2019/0081061 A1 to Tessariol et al. ("Tessariol")
1024	U.S. Patent No. 9,620,514 to Kai et al.
1025	Hwang, "Atomic Layer Deposition for Semiconductors," Springer (2014) ("Hwang")
1026	U.S. Patent No. 10,515,799 to Wang et al.
1027	U.S. Patent No. 9,570,460 to Kanakamedala et al.
1028	U.S. Patent No. 9,728,546 to Serov et al.

EXHIBIT NO.	DESCRIPTION
1029	Excerpt from YMTC's Exemplary Infringement Claim Chart for U.S. Patent No. 10,879,254 (Ex. A-2 to Disclosure of YMTC II Asserted Claims and Infringement Contentions, dated October 2, 2024) ("Ex. A-2, YMTC's Contentions") [PROTECTIVE ORDER MATERIAL – FILED UNDER SEAL]
1030	U.S. Patent No. 11,075,084 to Shen et al.
1031	U.S. Patent No. 10,304,852 to Cui et al. ("Cui")
1032	U.S. Patent No. 9,793,139 to Sharangpani et al.
1037	Weste, "Principles of CMOS VLSI Design," Addison-Wesley (1993) ("Weste")
1038	U.S. Patent No. 10,388,666 to Kai et al. ("Kai II")
1039	Japanese Patent Appl. No. JP 2017-247987 to Fujiki et al.
1040	Certified Translation of Japanese Patent Appl. No. JP 2017-247987 to Fujiki et al.
1041	File History of U.S. Patent No. 10,756,104 (U.S. Patent Publ. No. 2019/0198524) ("the Fujiki FH")
1042	Wolf, "Silicon Processing for the VLSI Era, Volume 1-Process Technology," Lattice Press (1986) ("Wolf Vol. 1")
1043	Wolf, "Silicon Processing for the VLSI Era, Volume 1-Process Integration," Lattice Press (1990) ("Wolf Vol. 2")
1044	U.S. Patent No. 10,714,341 to Cohen et al.

IV. UNDERSTANDING OF THE LAW

18. I am not an attorney, but have been instructed in and applied the law as described in this section.

19. I understand that the first step in comparing a challenged claim to the prior art is for the claim to be properly construed. I address how a person of ordinary skill in the art (POSITA) would have understood the challenged claims of the alleged invention in Sections VIII (no claim terms require express construction) and IX (where I discuss certain claim terms).

20. I have been further instructed and understand that a patent claim is unpatentable and invalid as obvious if the subject matter of the claim as a whole would have been obvious to a POSITA of the claimed subject matter as of the time of the invention at issue. I understand that when assessing the obviousness of claimed subject matter, the following factors are evaluated: (1) the scope and content of the prior art; (2) the difference or differences between each claim of the patent and the prior art; and (3) the level of ordinary skill in the art at the time the patent was filed.

21. I understand that claimed subject matter may be obvious in view of more than one item of prior art. I understand, however, that it is not enough to show simply that all the limitations of the claimed subject matter are spread throughout the prior art. Instead, for claimed subject matter to be obvious over multiple

references, there must be some reason or motivation for a POSITA to combine the prior art references to arrive at the claimed subject matter.

22. I have been informed that, in seeking to determine whether an invention that is a combination of known elements would have been obvious to a POSITA at the time of the invention, one must consider the references in their entirety to ascertain whether the disclosures in those references render the combination obvious to such a person.

23. I have been informed and understand that, while not required, the prior art references themselves may provide a teaching, suggestion, motivation, or reason to combine. The motivation linking two or more prior art references can also come from other sources, including, for instance, economic or market demand or the common sense of a POSITA at the time of the invention.

24. I understand that a particular combination may be proven obvious by showing that it was obvious to try the combination. I have been informed that, if a technique has been used to improve one device, and a POSITA would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.

25. I further understand that an obviousness analysis recognizes that market demand, rather than scientific literature, often drives innovation, and that a motivation to combine references also may be supplied by the direction of the

marketplace. For example, when there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a POSITA has good reason to pursue the known options within his or her technical grasp because the result is likely the product not of innovation but of ordinary skill and common sense.

26. I have been informed that the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. Thus, where all the elements of a claim are used in substantially the same manner, in devices in the same field of endeavor, the claim is likely obvious.

27. Additionally, I understand that a patent is likely to be invalid for obviousness if a POSITA can implement a predictable variation or if there existed at the time of the invention a known problem for which there was an obvious solution encompassed by the patent's claims. Therefore, when a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one.

28. I further understand that combining embodiments related to each other in a single prior art reference would not ordinarily require a leap of inventiveness.

29. I also understand that a POSITA must have had a reasonable expectation of success when combining references for claimed subject matter to be obvious.

30. I have been informed and I understand that factors referred to as "objective indicia of non-obviousness" or "secondary considerations" are also to be considered when assessing obviousness when such evidence is available. I understand that these factors can include: (1) commercial success; (2) long-felt but unresolved needs; (3) copying of the invention by others in the field; (4) initial expressions of disbelief by experts in the field; (5) failure of others to solve the problem the claimed subject matter solved; and (6) unexpected results.

31. I also understand that evidence of objective indicia of non-obviousness must be commensurate in scope with the claimed subject matter. I further understand that there must be a relationship, sometimes referred to as a "nexus," between any such secondary indicia and the claimed invention.

32. Finally, I have been informed that one cannot use hindsight to determine that an invention was obvious.

33. I provide my opinions in this declaration based on the guidelines set forth above.

V. LEVEL OF SKILL IN THE ART

34. I have been informed and understand that the level of ordinary skill in the relevant art at the time of the invention is relevant to inquiries such as the meaning of claim terms, the meaning of disclosures found in the prior art, and the reasons a POSITA may have for combining references.

35. I have been informed and understand that factors that may be considered in determining the level of ordinary skill include: (1) the education of the inventor; (2) the type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology; and (6) education level of active workers in the relevant field. I have been further informed and understand that a person of ordinary skill in the art (POSITA) is also a person of ordinary creativity.

36. In my opinion, a POSITA in the field of the '254 Patent would have had a bachelor of science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (e.g., researching, designing, or teaching) NAND flash memory devices, or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience).

37. In my opinion, this POSITA would also have been aware of and generally knowledgeable about semiconductor manufacturing and 3D NAND's structure, its component parts, how it operates, and how it is controlled.

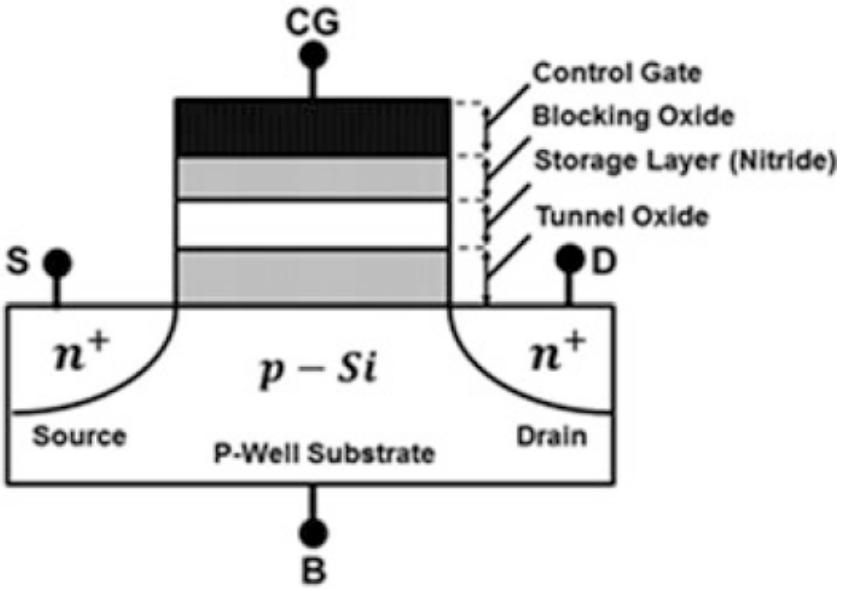
38. In view of my educational background and decades of experience working with semiconductor memory—including non-volatile 3D NAND flash memory—I was a person of more than the ordinary level of skill in the art as of August 2018. In forming my opinion, I have drawn on my academic background and professional experiences. My opinions herein, however, were formed taking into account the perspective of an ordinarily skilled artisan.

VI. TECHNOLOGY BACKGROUND AND STATE OF THE ART

39. I have been asked to provide a brief overview of the technology relevant to the '254 Patent and the state of the art when the '254 priority application was filed.

40. The '254 Patent (and the prior art I discuss herein) relate to three-dimensional (3D) NAND flash memory. "Flash memory" has been known for many decades and is a type of memory that stores information even when power is removed (*viz.*, when the device is turned off).

41. At the heart of flash memory lies the "memory cell," which stores information as electrical charge. An example memory cell is below:



Ex. 1008, 41. In a memory cell, current flows from the "drain" of the device to the "source" of the device, which is typically connected to a low voltage, such as ground. *Id.*, 150 ("[T]he Source Line … plays the role of the 'local ground' for each memory cell.").

42. The acronym "NAND" refers to a "not-AND" logic gate, and NAND flash memory is a particular type of flash memory where the memory cells form a structure similar to that of a NAND gate. Ex. 1008, 14. The other most common type of flash memory is NOR flash, but NAND offers a higher integration density and occupies a larger market than NOR flash.

43. A NAND flash memory device, like most flash memory devices, has an associated memory controller that controls the read, write, and erase operations

on a memory cell by applying a voltage to that cell's "control gate," labeled as "CG" in the above figures. Ex. 1008, 41.

44. For many years, a NAND flash memory was "planar," that is, two-dimensional (2D). In 2D NAND flash memory, all memory cells lie on a 2D plane (*i.e.*, the x-y plane) on the surface of a memory chip as shown below:

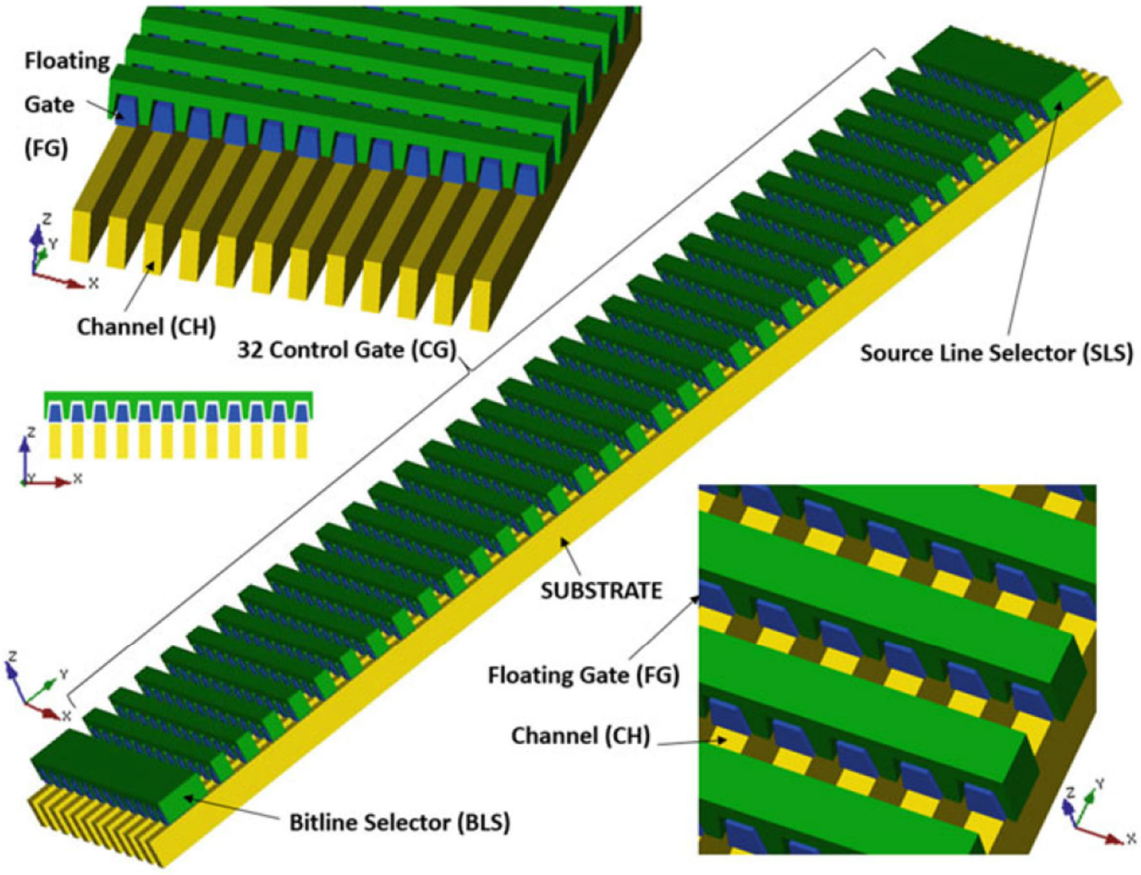


Fig. 3.9 Bird's-eye view of a planar NAND string

Ex. 1008, 86.

45. To boost data storage densities and reduce cost per gigabit, the art developed so-called "three-dimensional (3D) NAND flash cells" starting in about

2006. Ex. 1014, 292. Unlike planar 2D NAND flash memory, in 3D NAND flash memory the memory cells are arranged in vertical, cylindrical NAND flash columns, often referred to as "memory strings." Conceptually, a modern 3D NAND structure could be conceived by starting from the 2D NAND string building block and turning the 2D NAND string on its side, resulting in a 3D structure with a vertical channel. The following image provides an example:

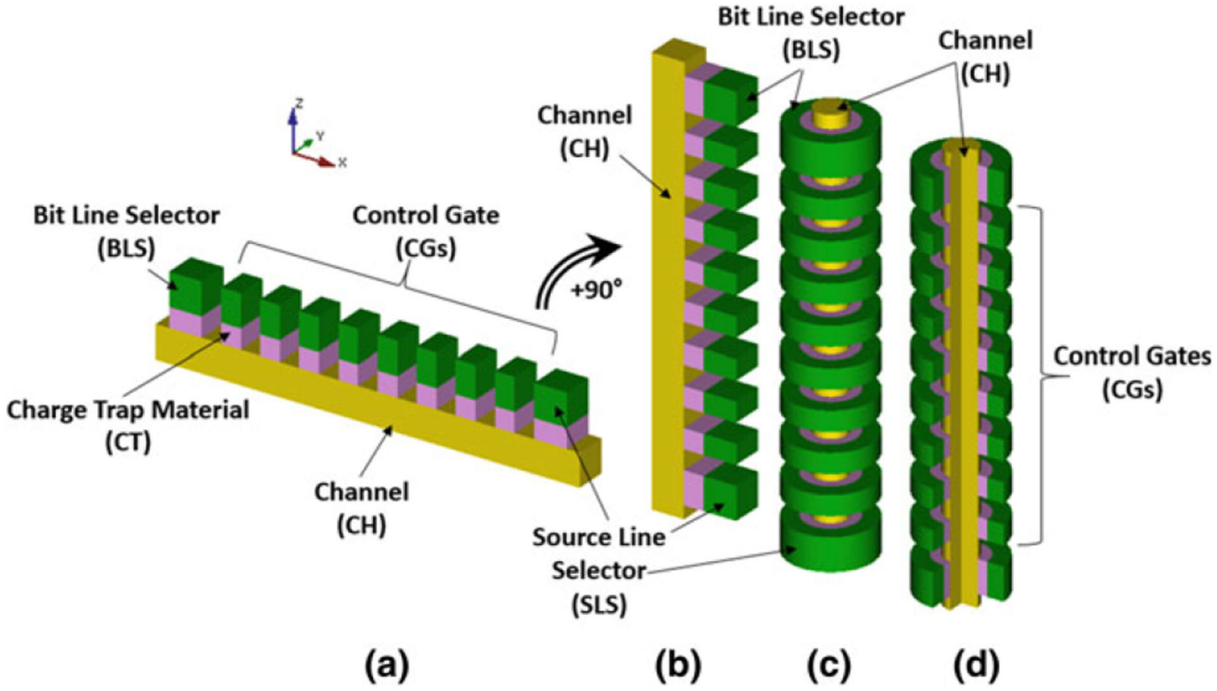


Fig. 4.1 NAND Flash string with horizontal gate and vertical channel: **a** planar, **b** planar rotated by 90°, **c** vertical channel with cylindrical shape and **d** its cross section

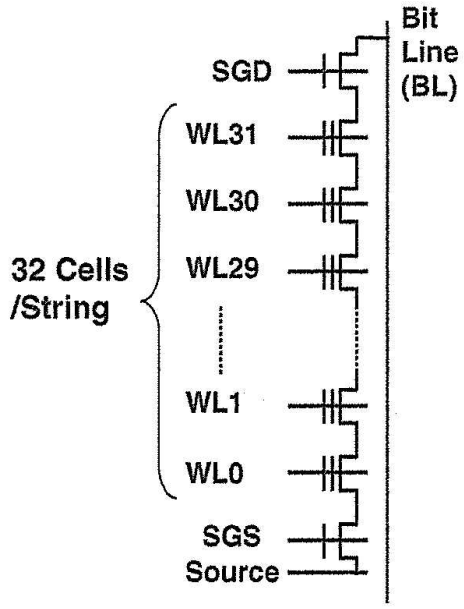
Ex. 1008, 102. As labeled in Figure 4.1, above, each NAND string includes a "cylindrical channel." *Id.*, 58. The concept of a "channel" was well-known in semiconductor devices and refers to a thin and layer of charge that is formed between the source and drain of a transistor when a voltage is applied to the gate. The

"channel" is highly conductive and allows current to easily flow between the source and drain. The "cylindrical channel" in 3D NAND devices also provides the means for current to flow in a memory string.

46. Multiple of such vertical channels are then repeated in a three-dimensional array. Ex. 1014, 296.

47. As can be seen above, the NAND flash memory "strings" each contain multiple cells "connected in series." Ex. 1014, 38. The source of one cell is connected to the drain of the next one. Depending on the technology, typically a string consists of 32 to 128 NAND cells.

48. Each end of a string is terminated with a "select transistor." One is often called the "SGD" (drain-end select gate transistor) and the other one is often called "SGS" (source-end select gate transistor). The "SGD connects" at the string's drain side "to isolate it from a bit line (BL)." Ex. 1014, 38. Hence, the SGD is also known as the "bit line select transistor" or the "upper select gate." The SGS connects at the string's source side "to isolate it from a source line (SL)." *Id*. Since the source line is commonly connected to the ground terminal, SGS is also known as the "ground select transistor" or the "lower select gate." Word lines are connected to each memory cell control gate. *Id.*, 38-39. A schematic representation of a memory string is shown below:



Ex. 1014, 39.

49. Various architectures for constructing 3D NAND flash memory were known in the art. One such example is the well-known BiCS (Bit Cost Scalable) architecture, where various "contacts" (electrical connections) are formed on top of the memory array. Below are two illustrations of the BiCS architecture show top and bottom perspective views.

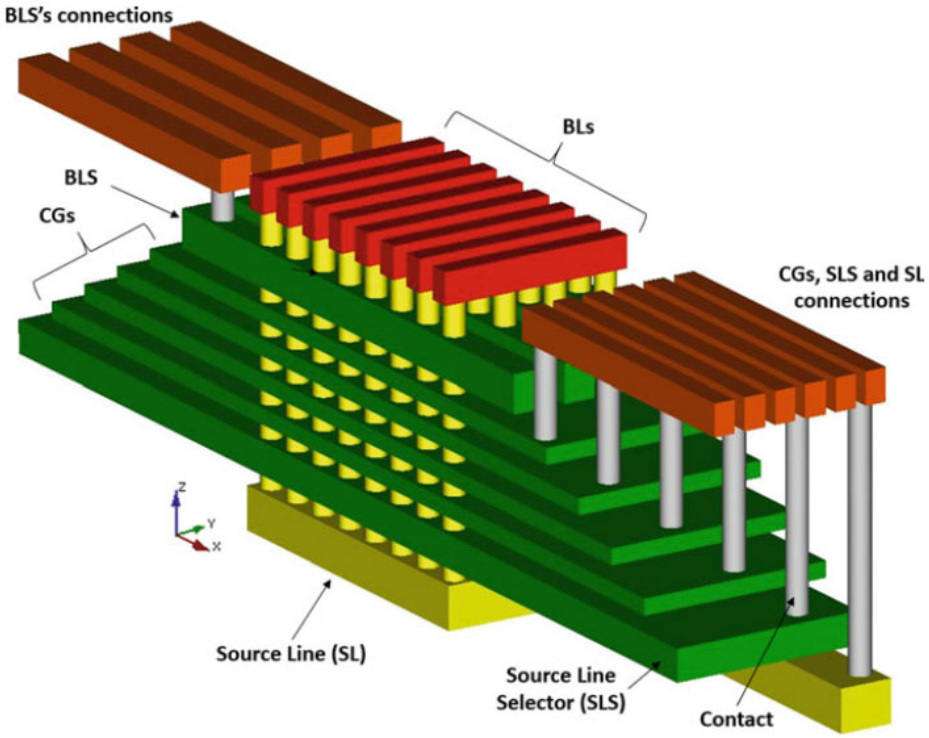


Fig. 4.13 Top bird's eye view of BiCS with gate connections

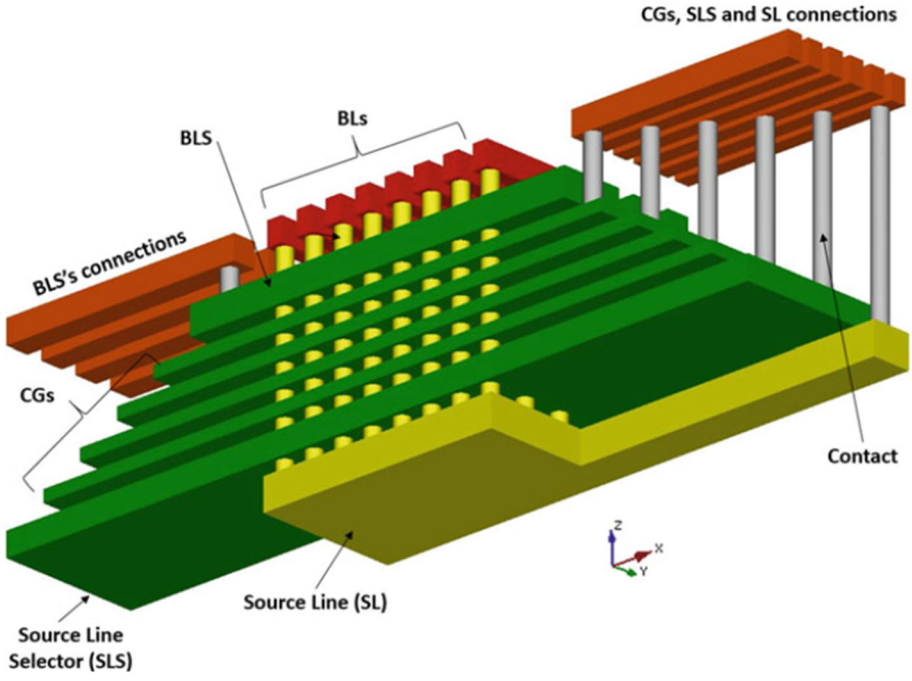


Fig. 4.14 Bottom bird's-eye view of BiCS with gate connections

Ex. 1008, 109-110. As is traditional in MOSFET transistors, the "source" terminal connects to a low voltage, such as ground. The same holds true in 3D NAND design, and the BiCS architecture includes source line contacts for providing a low voltage (e.g., ground) connection to the memory strings. This is shown in yellow in the figures above.

50. As can be seen above, the source line contact does not travel directly through the memory stack. It was well known, however, to form contact directly through the memory stack by forming a hole in the stack, an insulating line in the hole, and filling the hole with a conductive material. I provide a several examples below:

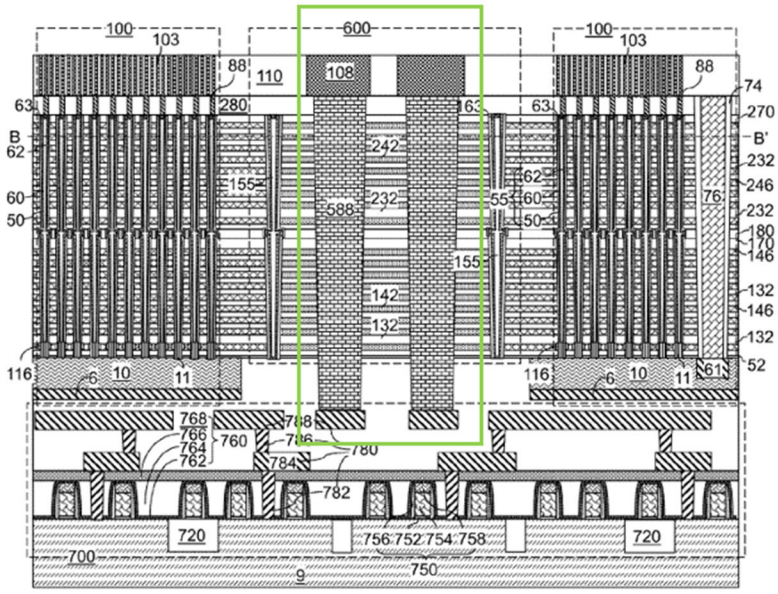


FIG. 69A

Ex. 1009 (Toyama), Title ("Through-Memory-Level Via Structures"), [0367], Fig. 69A (588) (annotated) [1].

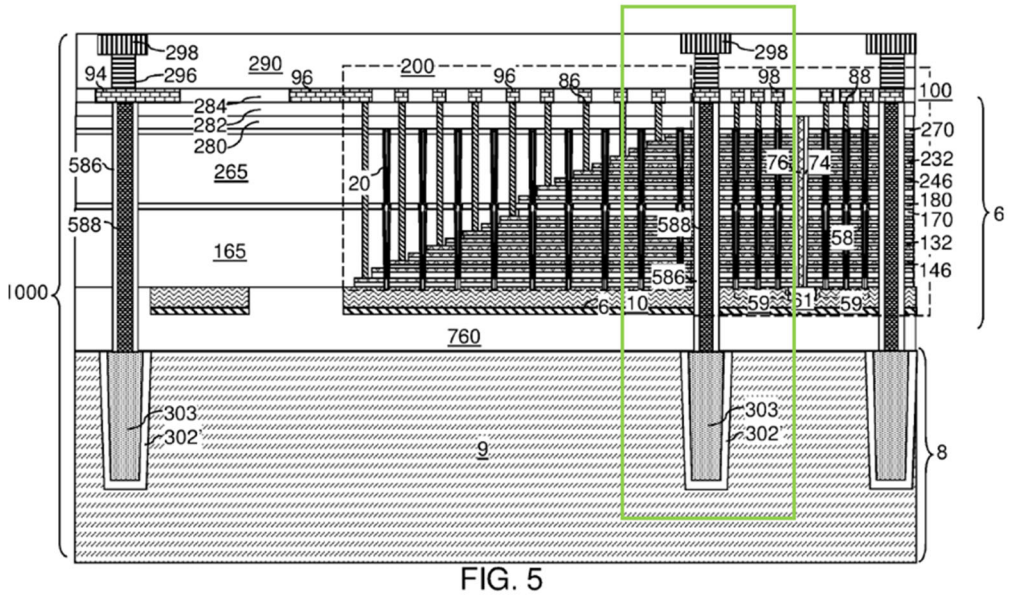


FIG. 5

Ex. 1010 (Mushiga), 10:31-58, Fig. 5 (588).

[1] Annotations added throughout unless noted.

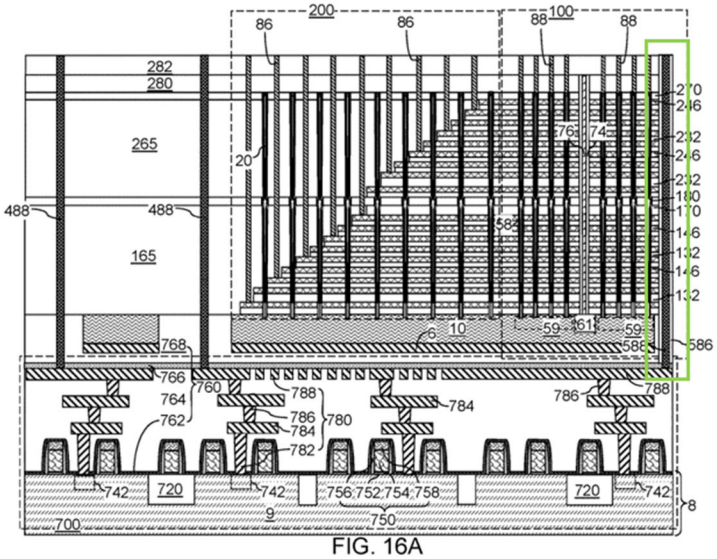


FIG. 16A

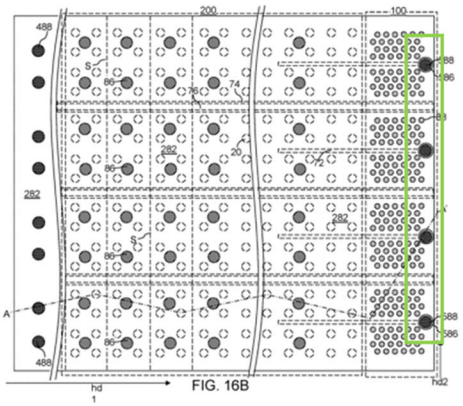


FIG. 16B

Ex. 1011 (U.S. Pat. Pub. 2019/0229125), [0189], Figs. 16A, 16B (588). Indeed, in other prior art patents, the assignee of the '254 Patent discloses forming through-array contacts through the array. *E.g.*, Ex. 1012 (WO 2019042103) (Fig. 2, 248) and Ex. 1013 (U.S. Pat. 10,679,721), Fig. 1 (110), Abstract ("TAC").

51. The individual memory cells in a memory string are accessed by word lines that typically extend horizontally and connect to a control gate for a given cell on each memory string. On the periphery of the 3D NAND device, the word lines form a staircase structure, where each subsequent word line protrudes a short distance beyond the word line above it, like a staircase, as shown below in green.

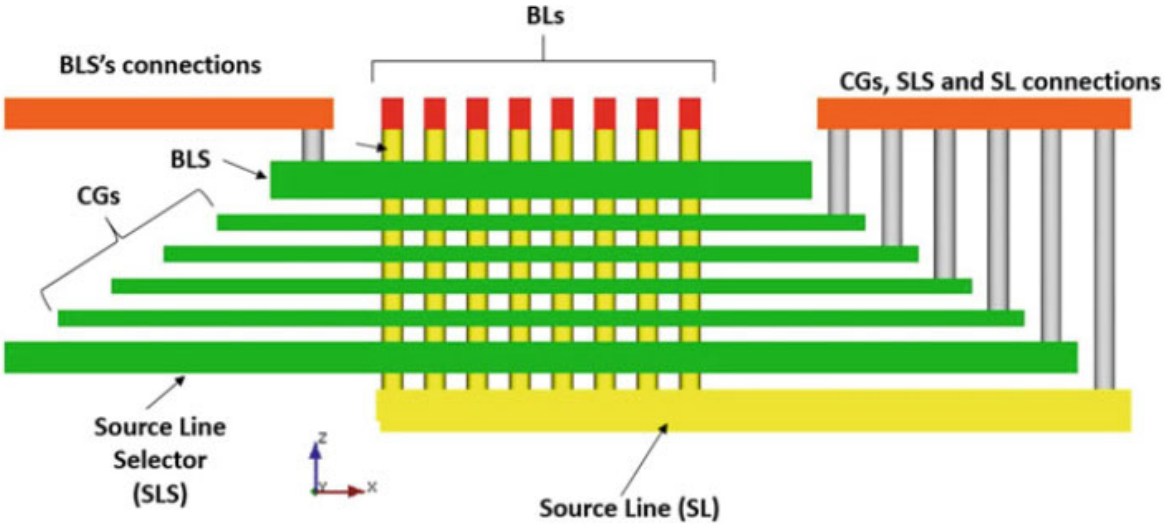


Fig. 4.12 Vertical cross section of BiCS with gate connections

Ex. 1008, 109 (green control gates forming a staircase). As noted, each word line delivers a control signal to a number of memory cells at the same horizontal level in the 3D NAND memory device.

52. The collection of memory cells controlled by a common signal together constitute a "word," and the control gate is a "word line." *Id.*; Ex. 1014, 38-40. The grey columns in the figure above, often referred to as "local contacts," show how the word lines can be controlled by signals on the top surface of the 3D NAND device. In the context of 3D NAND chips, "local contacts" refer to the electrical connections made within the memory device to link various components such as the word lines and source lines. In facts, local contacts are also often referred to as "vias," which have been widely known and used in all sorts of semiconductor devices for many decades. These vias create vertical electrical connections between the different

layers within the 3D NAND stack. They are integral to the architecture of semiconductor devices generally, including 3D NAND technology where they enable the functional linkage of stacked memory cells across multiple layers. Note that these local contacts can be of various lengths – some long and some very short. For example, the local contacts (the grey columns in the figure above) that connect to the word lines located near the top of the memory stack are very short while the grey column that connect to the source line is much longer. Where local contacts are connecting an existing vertical structure, such as a memory string or slit, the local contacts tend to be relative short.

53. A variety of modifications to the BiCS architecture were known, including the use of slit structures to serve as source line contacts for the NAND strings. Exemplary slit structures are shown in purple below. These particular slit structures function as contacts for connecting to the source (which may be shared by some, or all, memory strings) located on the bottom of the 3D NAND device. Because slits have an insulating liner, they can separate the array into blocks, which are units of the array.

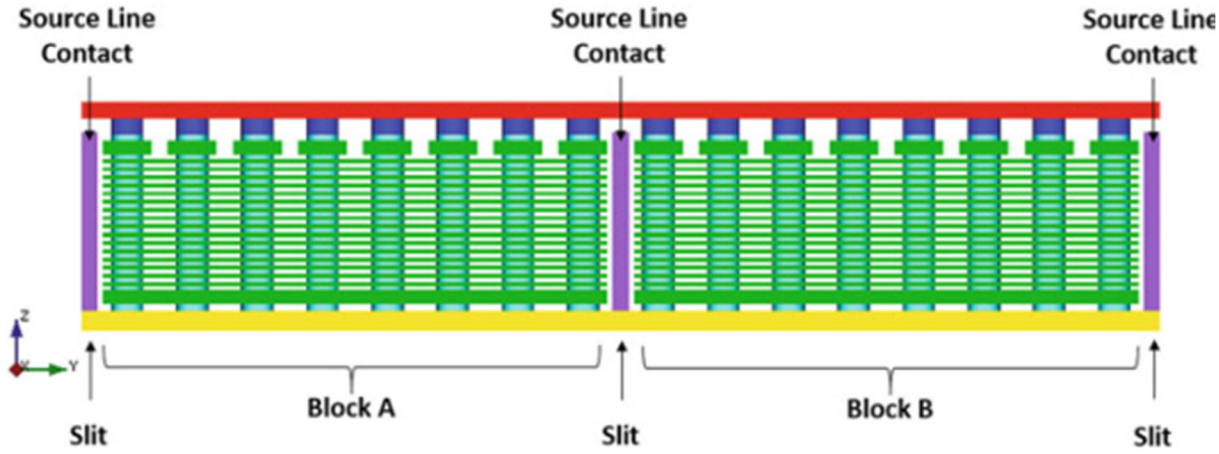


Fig. 6.8 Side view of Fig. 6.7

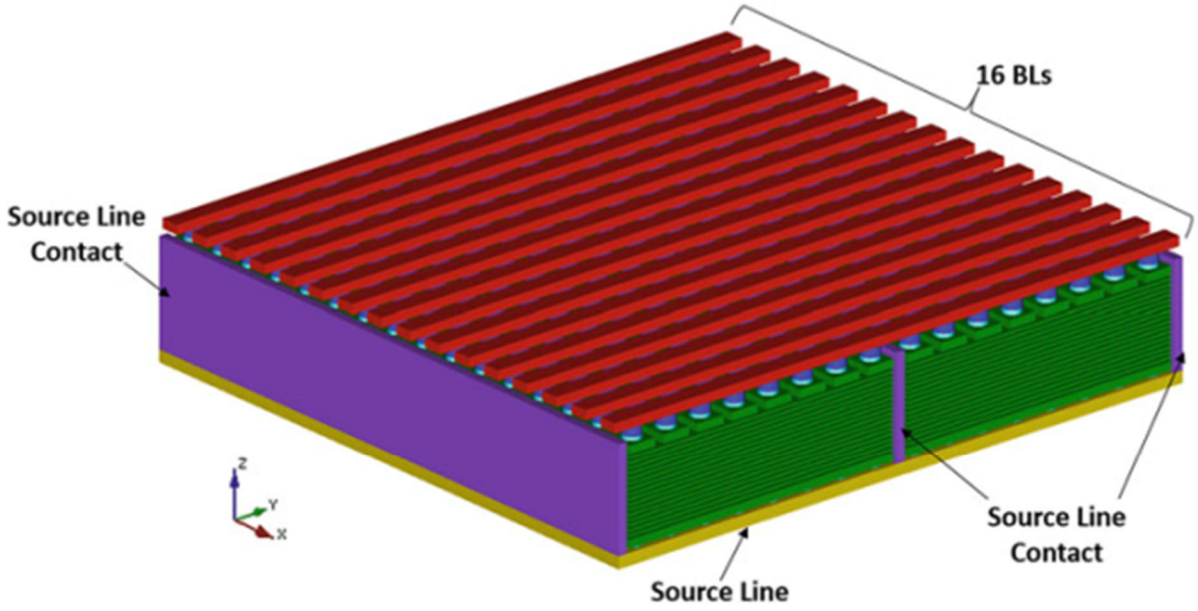


Fig. 6.7 Array slits

Ex. 1008, 185.

54. In both figures above, gaps are shown between the various structures. In actual 3D NAND memory devices, these "gaps" are not empty space; rather, they are filled with insulating material (known as "dielectric" material). Among other

things, dielectrics serve to isolate electrical signals and prevent one conductive structure from interfering with another other. Another function performed by the dielectric is mechanical support to prevent the other structures from collapsing.

55. Well before the effective filing date of the '254 Patent, companies (including Micron) had developed various techniques for manufacturing 3D NAND flash memory, many of which leveraged fabrication principles and materials that had been in use generally in the semiconductor manufacturing industry for decades.

56. The fabrication of 3D NAND memory chips involves etching techniques to construct vertical, high-density storage architectures. These etching processes, fundamental to semiconductor manufacturing, have been well established prior to 2018 but have been adapted for 3D NAND. Here are just a few examples of etching processes used for 3D NAND. Channel hole etching which typically makes use of a dry etching process, e.g., deep reactive ion etching (DRIE) to create vertical channels through the NAND stack. DRIE was developed in the mid-1990s, allows for etching with high aspect ratios, essential for the vertical structures in 3D NAND. Staircase etching involves sequential etching steps to create a staircase-like structure for accessing word lines across each memory layer. This process leverages standard lithographic and etching techniques known long before 2018, adapted to create the precise, repetitive structures needed for multi-layer access. Hard-mask etching process, well-known long before 2018, involves depositing a durable

material like nitrides which is then patterned using photolithography to serve as a mask. The hard mask protects underlying layers during subsequent etching. Selective etching is used to remove specific materials without damaging others by using different chemistries in plasma to target certain layers of materials, again was well-known long before 2018. Spacer etching which involves depositing and then partially removing the material developed to define narrow, uniform spacers (gaps) for cell isolation. Spacer etching processes was developed for lightly-doped drain (LDD) MOSFETs back in the 1980's and adapted for 3D NAND manufacturing process. Each of these processes originates from fundamental techniques known in semiconductor manufacturing well before 2018, adapted for the advanced architecture of 3D NAND.

57. Stacking multiple chips, also known as 3D integration, was just one of many advancements in semiconductor technology that have happened over the years. The concept of 3D integration should not be confused with 3D NAND. Although 3D integration has application to 3D NAND chips, the concept of vertically stacking multiple dies/chips predates 3D NAND by many years and has been used extensively in a variety of chip technologies. This method significantly enhances device performance and functionality while conserving space, addressing the limitations faced by traditional planar scaling methods. Naturally, when stacking multiple dies on top of one another, via structures (also called through-silicon vias

(TSVs) or through-array contacts (TACs)) were implemented to provide connections between different chips in the stack. I discuss and provide examples of TACs above.

58. In summary, techniques for manufacturing 3D NAND memory devices, including TACs and slits, were well-known in the art before the '254 Patent's effective filing date.

VII. THE '254 PATENT

A. Effective Filing Date

59. Based on my review of the '254 Patent, I note that it also references a PCT application on its face, which was filed August 21, 2018.

60. For purposes of this declaration, I have been asked to assume that August 21, 2018 is the effective filing date of the '254 Patent. My opinions in this declaration were formed from the perspective of a POSITA as of August 21, 2018, including both the knowledge of a POSITA at that time as well as how a POSITA would have understood the '254 Patent and the prior art.

B. Overview

61. The '254 Patent's title specifically highlights TACs: "Three-dimensional memory devices having through array contacts and methods for forming the same." As I describe in Section VI, and as the '254 Patent describes, TACs extend through the memory stack. Ex. 1001, 8:28-60. The '254 Patent alleges there are issues with forming TACs through a "barrier structure." *Id.*, 4:55-5:20.

While the ’254 Patent does not depict a barrier structure, it appears that the ’254 Patent is referring to, for example, a rectangular block of oxide through which conductive contacts extend. For example, after etching out a rectangular area of the stack and filling that void with oxide forms such a barrier structure. This provides an insulating structure so that pure conductive core TACs can extend through the structure. Below is such a structure from another YMTC patent (the assignee of the ’254 Patent):

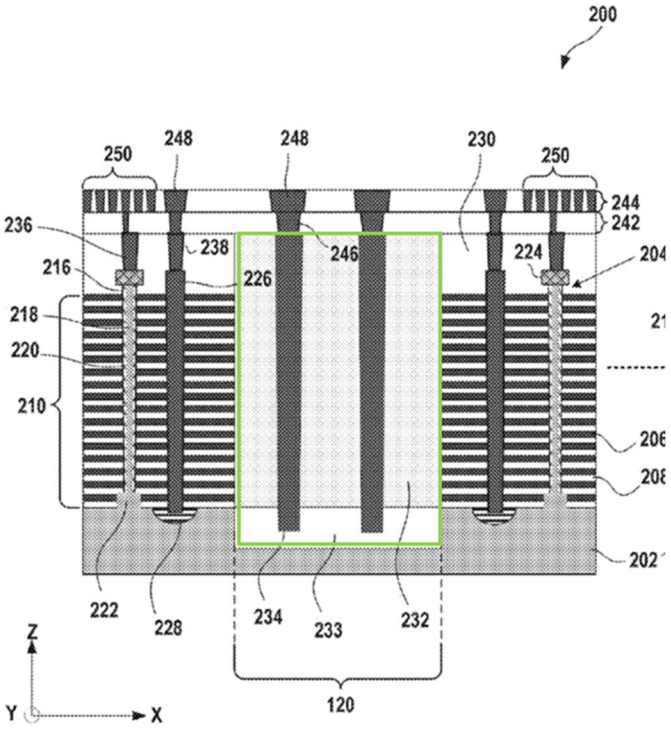


FIG. 2

Ex. 1007 (U.S. Pat. 10,658,378), Fig. 2 (120).

62. Rather than relying on a barrier structure, the '254 Patent teaches the use of a thin spacer (138) for each TAC, which also serves an insulating function.

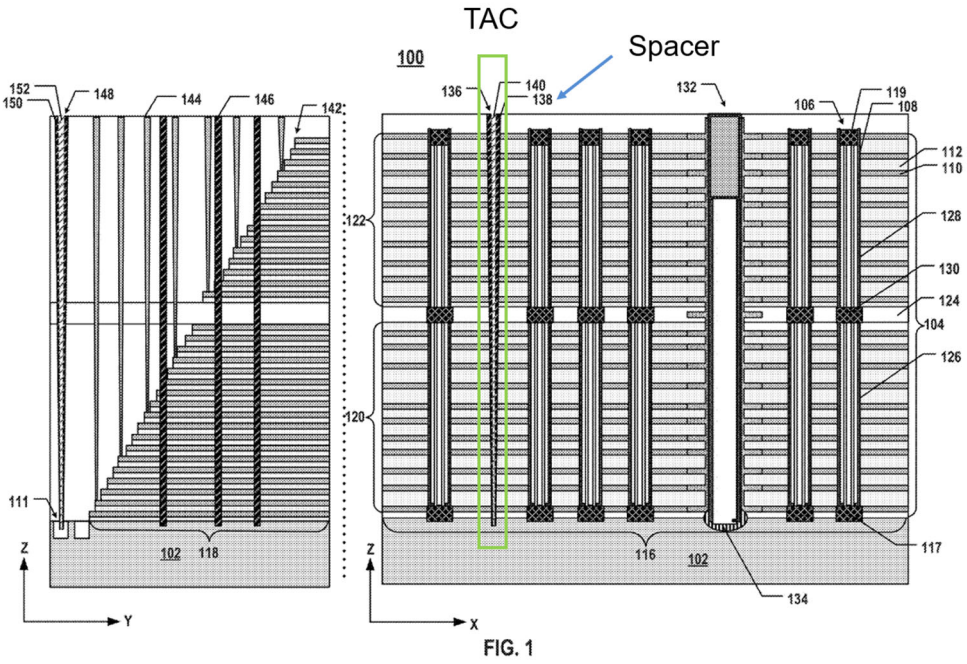


FIG. 1

Ex. 1001, Abstract, 4:55-5:20.

63. As shown above, the TACs include a dielectric, e.g., silicon oxide, spacer (138) to insulate the TAC from the memory stack (e.g., the conductive gate layers) and a conductive core (140). Ex. 1001, 8:45-60. Recall that gate layers are conductive, and thus an insulator liner is necessary to prevent short circuiting the gate layers. The conductive core enables the TAC to connect devices above and below the array, i.e., provide an electrical coupling between such devices. *Id.*, 4:55-59.

64. I summarize the file history below. The file history suggests that the Examiner may have found forming a slit after the TACs to be the alleged point of novelty. Ex. 1001, Abstract. The Abstract highlights this timing requirement, and this timing requirement is a requirement of each independent claim.

65. As I describe in Section VI, slits were well known and textbook material. Shown below in red, the slit structure (which fills the open slit) can include a conductor core and dielectric spacer, and thereby interconnect a source voltage (above the array) to a common source in the substrate (below the array). Ex. 1001, 8:1-27. The slit can extend laterally (in the Y-direction, into the page) and therefore segment the array into blocks. *Id.* The slit (while a void) can be used in the gate replacement process to replace the sacrificial gates with conductive gates. *Id.*, 14:44-62. That is, this void allows for the etching of the sacrificial gate and then the deposition of the conductive gates, e.g., forming tungsten conductive gates.

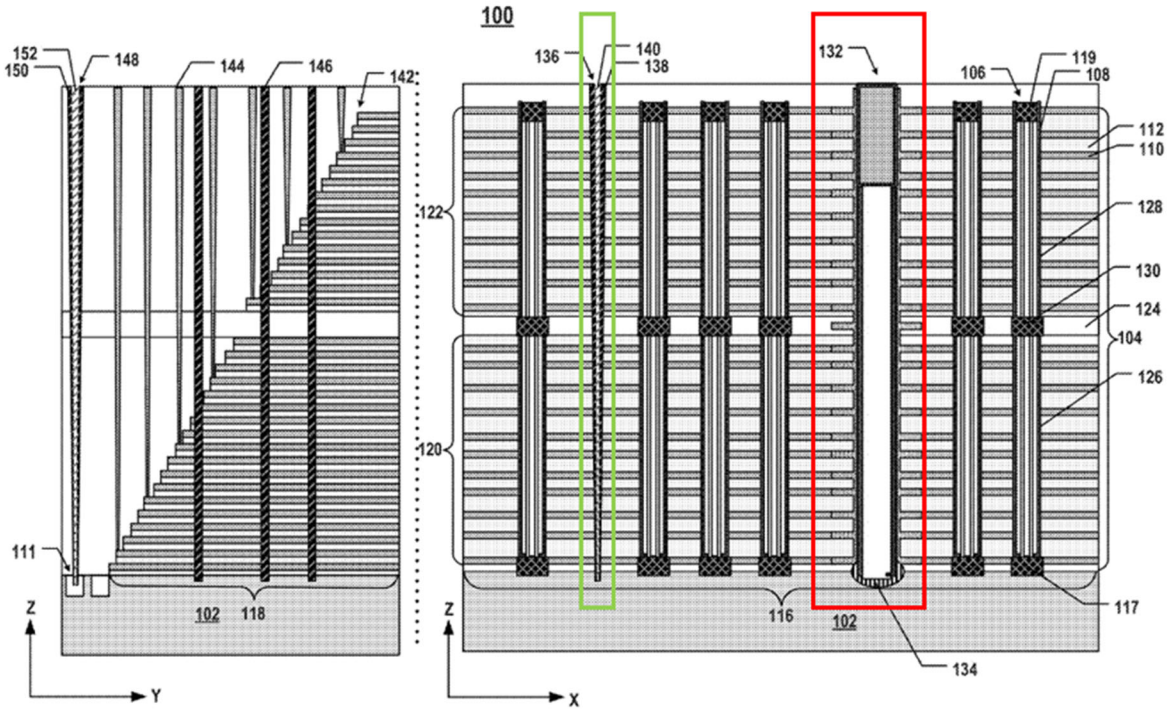


FIG. 1

Id., Fig. 1.

66. The ’254 Patent’s Figure 6 depicts a process flow and the process steps in order. As can be seen, the ’254 Patent describes forming the slits after forming the TACs:

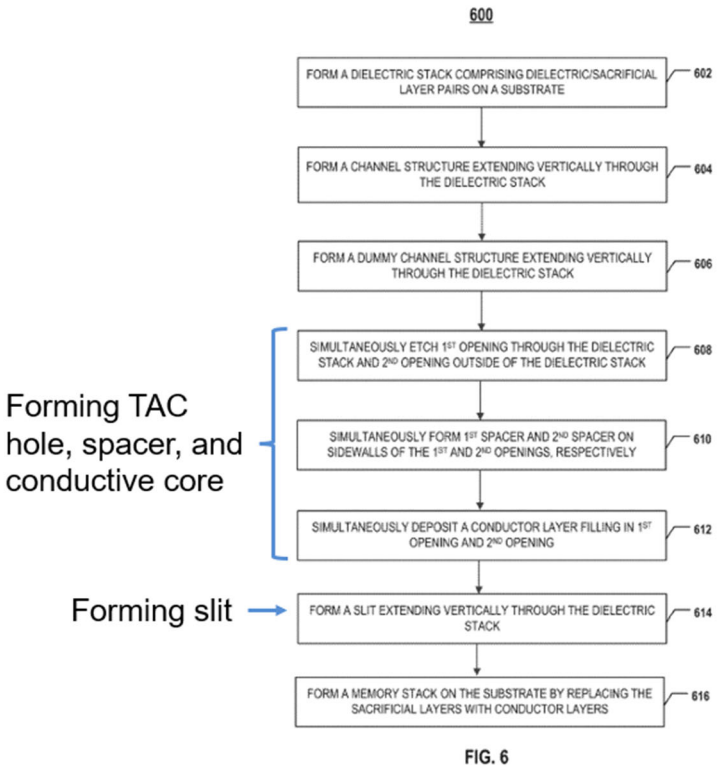


FIG. 6

Ex. 1001, Fig. 6; *see also id.*, Fig. 3B, 12:24-63 (forming TACs holes), Fig. 3C-E, 12:64-14:19 (various ways to form spacer), Fig. 3F, 14:20-43 (forming conductive core for TAC), Fig. 5A, 14:44-15:12 (forming slit), Fig. 5A, 15:12-24 (filling slit).

C. Prosecution History

67. As noted above, I have reviewed the '254 Patent's file history. The file history is quite short with no rejections over the prior art. On October 26, 2020, the claims were allowed, and the Notice of Allowance highlights forming the TAC and then after forming the TAC, forming the slit: "forming a spacer on a sidewall of the first opening; forming a through array contact (TAC) extending vertically through the stack by depositing a conductor layer over the spacer in the first opening; and

after forming the TAC, forming a slit extending vertically through the stack." Ex. 1002, 133-34. This strongly suggests that the timing requirement is the alleged point of novelty, because as I describe in Section VI, both of these structures were well known in the art.

VIII. CLAIM CONSTRUCTION

68. I am not a legal expert or an attorney and offer no opinions on the law. I understand that claim construction is a matter of law. However, I have been informed by counsel of the legal standards that apply to claim construction in an *inter partes* review, and I have applied them in forming my opinions. I understand that during an inter partes review, the same claim construction standard used in federal district court is applied when addressing the meaning of claim terms.

69. I have been informed that the words of a claim are generally given their plain and ordinary meaning that the term or phrase would have to POSITA at the time of the invention in view of the surrounding claim language, the specification and the file history (collectively, the "intrinsic evidence" or "intrinsic record").

70. I also understand that courts may consider extrinsic evidence, such as expert and inventor testimony, dictionaries, and learned treatises (collectively, the "extrinsic evidence" or the "extrinsic record"), but that such extrinsic evidence should be given less weight than the intrinsic evidence.

71. In my opinion, the challenged claims do not require further construction and can be afforded their plain and ordinary meaning for purposes of the analysis of the prior art that I am conducting in this declaration.

IX. UNPATENTABILITY ANALYSIS

72. For the reasons I explain in greater detail below, it is my opinion that as of the effective filing date of the '254 Patent, claims 1-15, 17-18, and 20 of the '254 Patent are unpatentable as obvious over the prior art discussed in this declaration.

A. Overview of the Prior Art

73. The following paragraphs provide an overview of the primary reference that I discuss throughout this declaration.

1. Fujiki

74. Fujiki relates to a conventional 3D memory that includes TACs.

75. Specifically, Fujiki discloses forming a TAC: "a through-via hole 94 is formed to pierce the stacked body 50, the insulating film 45, and the upper portions of the insulating film 32 and reach a portion of the interconnect 36. Then, the insulating film 79 is formed on the inner surface of the through-via hole 94; and the through-via 78 is formed on the inner surface of the insulating film 79. The through-via 78 is connected to the interconnect 36." Fujiki, [0053]. Note that "via" is a

common semiconductor term that typically refers to a vertical conductive element that connects upper- and lower-level elements.

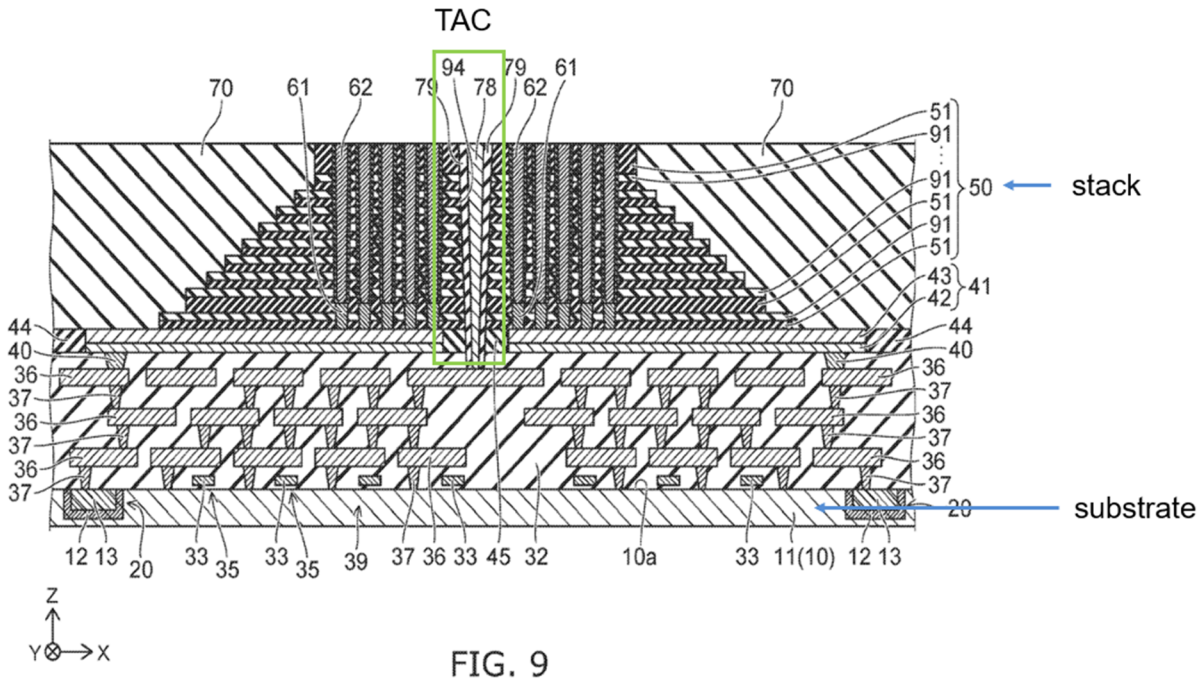


FIG. 9

Id., Fig. 9.

76. After forming the TAC, Fujiki discloses "[c]ontinuing as shown in FIG. 10 and FIG. 3, slits 95 are formed to pierce the insulating film 70 and the source electrode film 41; and ***slits 96 are formed to pierce the stacked body 50***." Fujiki, [0054]. I describe slits in Section VI. Slits are long lateral trenches that typically divide the memory stack into smaller units, e.g., memory blocks.

77. As shown below, Fujiki also discloses peripheral contacts 82 and 83, which do not traverse the memory stack:

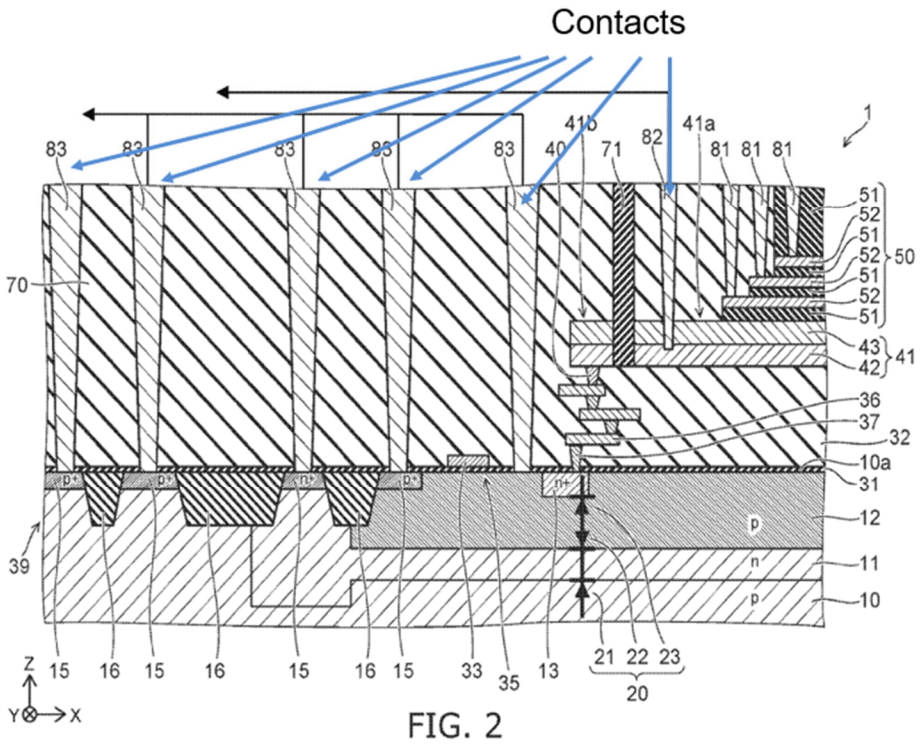


FIG. 2

Fujiki, Fig. 2.

2. Fujiki (the US Appl.) Was Effectively Filed on December 25, 2017

78. I was asked to review a translation of Fujiki's JP 2017 application (original Ex. 1039 and translation Ex. 1040) and determine whether it describes all of the disclosures in the Fujiki 2019 US Application (Ex. 1006). In short, the Fujiki 2019 US Application appears to largely be a translation of the Fujiki JP 2017, and the Fujiki JP 2017 describes all the disclosures of the Fujiki 2019 US Application. The US Application does include an additional figure, namely, figure 13. Figure 13, however, is only a top-down view of the third-embodiment. A top-down view refers

to a view as if one were looking (from over the device) down onto the device. In other words, it merely provides a particular viewpoint for that embodiment. Both the Fujiki JP application and the US Application, however, also includes a cross-sectional view of the third embodiment and a description thereof. Thus, both describe the same third embodiment.

79. I was asked to review the below table and confirm that a POSITA would have found the below description of how the translation and US Application correlate to be accurate, and I agree the below table provides an accurate correlation.

Fujiki US 2019/0198524 and corresponding support in JP 2017-247987 (*see* Ex. 1039 (JP App.) and Ex. 1040 (10/21/24 certified translation))

US 2019/0198524 (Ex. 1006)	JP 2017-247987 (Exs. 1039-40)	Comment
Foreign Application Priority data (30) (Cover)	Date of Application (Certificate of Availability page); Application Number (Certificate of Availability page); Submission date (Cover)	Same
Title (54) (Cover)	Name of invention (Cover)	Substantively the same[2]

[2] Generally, throughout Ex. 1006 (Fujiki US App.) and 1040 (translation), the Fujiki US App. uses "memory device" and the translation uses "storage device."

US 2019/0198524 (Ex. 1006)	JP 2017-247987 (Exs. 1039-40)	Comment
Abstract (Cover)	Methods of solving the problems [0005]	Substantively the same[3]
Drawings/Figures	Drawings/Figures	The US includes an additional figure upon which the Petition does not rely, namely, fig. 13. Figure 13, however, is only a top-down view of the third-embodiment, in which the translation describes the same without the additional top-down view. Thus, the Fujiki JP Appl. does support figure 13. Otherwise, the figures are the same. Aligning US figures to JP: • Figures 1-12 are the same. • Fujiki US App. figure 14 corresponds to translation's figure 13. • Fujiki US App. figure 15

[3] Generally, throughout Ex. 1006 (Fujiki US App.) and Ex. 1040 (translation), the Fujiki US App. uses "stacked" and the translation uses "laminated."

US 2019/0198524 (Ex. 1006)	JP 2017-247987 (Exs. 1039-40)	Comment
		corresponds to translation's figure 14.
Field [0002]	Technical Field [0001]	Substantively the same
Background [0003]	Background Art [0002]	Substantively the same
Brief Description of the Drawings [0004] – [0018]	Brief Description of the Drawings [0007]	The US includes an additional figure (Fig. 13 [0016]). Otherwise, the figures and descriptions are the same.
Detailed Description [0019]	Methods of solving the problems [0006]	Substantively the same
First embodiment [0020] – [0059]	First embodiment [0008] – [0040]	Substantively the same
Second embodiment [0060] – [0066]	Second embodiment [0041] – [0045]	Substantively the same
Third embodiment [0067] – [0068]	Third embodiment [0046]	Substantively the same
Third embodiment cont. [0069] – [0070]	Third embodiment cont. [0047]	Substantively the same[4] The Fujiki US App. also references the top-

[4] From this point forward, recall that the Fujiki US App. figure 14 corresponds to translation's Figure 13 and Fujiki US App. figure 15 corresponds to translation's Figure 14.

US 2019/0198524 (Ex. 1006)	JP 2017-247987 (Exs. 1039-40)	Comment
		down view of fig. 13. Again, figure 13 is simply the top-down view of figure 12.
Third embodiment cont. [0071] – [0072]	Third embodiment cont. [0048]	Substantively the same
Third embodiment cont. [0073]	Third embodiment cont. [0049]	The Fujiki US App. also describes contacts 82 and 84. These contacts, however, are shown in Figures 2 and 3 of the first embodiment (source and peripheral contacts). *See* Ex. 1040, Figs 2-3, [0026]. Thus, the Fujiki JP App. fully supports this paragraph.
Third embodiment cont. [0074] – [0082]	Third embodiment cont. [0050] – [0057]	Substantively the same
Third embodiment cont. [0083]	Third embodiment cont. [0058]	Substantively the same. Note that the Fujiki US App. references the top-down view of Figure 13.
Third embodiment cont. [0084] – [0085]	Third embodiment cont. [0059]	Substantively the same
Third embodiment cont. [0086]	Third embodiment cont. [0060]	Substantively the same. Note that the Fujiki US App. references the

US 2019/0198524 (Ex. 1006)	JP 2017-247987 (Exs. 1039-40)	Comment
		top-down view of Figure 13.
Third embodiment cont. [0087] – [0090]	Third embodiment cont. [0061] – [0063]	Substantively the same
Claim 1	Claim 1	Substantively the same
Claim 4	Claim 2	Substantively the same
Claim 10	Claim 3	Fujiki JP App. lists additional elements.
Claim 16	Claim 4	Substantively the same.
Claim 19	Claim 5	Substantively the same (while Fujiki US App. lists all the elements, Fujiki JP App. incorporates claim 4).

3. Summary of Grounds for Invalidity: Fujiki in View of a POSITA's Knowledge

80. Fujiki, combined with the knowledge of a POSITA, renders Claims 1-15, 17-18, and 20 of the '254 Patent obvious. Specifically, Fujiki's teachings and the knowledge of POSITA would motivate a POSITA to apply known techniques to yield a predictable result, achieving the claimed invention with a reasonable expectation of success. The methods outlined herein leverage predictable, routine practices and widely adopted techniques in semiconductor fabrication, particularly for high-aspect-ratio structures. A POSITA would recognize these implementations

as industry-standard approaches, derived directly from well-documented methods and widely recognized for their reliability and effectiveness in achieving the claimed outcomes.

B. Ground 1: Fujiki in View of the Knowledge of a POSITA Render Obvious Claims 1-15, 17-18, and 20

1. Claim 1:

[1.PRE] "A method for forming a three-dimensional (3D) memory device, comprising:"

81. While not offering an opinion on whether the preamble is limiting, Fujiki discloses it. Fujiki, [0025] ("stacked NAND flash memory"), [0046] ("method for manufacturing"). Fujiki's "stacked NAND flash memory" is a conventional 3D NAND.

[1.A] "forming a stack comprising a plurality of dielectric/sacrificial layer pairs on a substrate;"

82. As I describe in detail below, Fujiki discloses forming a stack (50) comprising a plurality of dielectric/sacrificial layer pairs (51/91) on a substrate (10 or 43).

83. The '254 Patent provides certain definitions of terms in the specification. This includes "on" and "substrate." Ex. 1001, 3:52-4:15.

84. The '254 Patent defines substrate: "As used herein, the term 'substrate' refers to a material onto which subsequent material layers are added. The substrate itself can be patterned. Materials added on top of the substrate can be patterned or

can remain unpatterned. Furthermore, the substrate can include a wide array of semiconductor materials, such as silicon, germanium, gallium arsenide, indium phosphide, etc. Alternatively, the substrate can be made from an electrically non-conductive material, such as a glass, a plastic, or a sapphire wafer." Ex. 1001, 4:6-15. This definition means that the "substrate" need not be the base substrate, e.g., the most bottom layer.

85. The '254 Patent defines "on": "It should be readily understood that the meaning of 'on,' 'above,' and 'over' in the present disclosure should be interpreted in the broadest manner such that 'on' not only means 'directly on' something but also includes the meaning of 'on' something with an intermediate feature or a layer therebetween." Ex. 1001, 3:52-61. This definition means that X can be "on" Y even if X is over, but not physically contacting, Y.

86. Fujiki discloses "substrate 10." Fujiki, [0028], [0033]. I note that substrate 10 is the base substrate layer. Given the '254 Patent's definition of substrate, the upper-level substrate, e.g., which has a common source for the channel structures, could also be the "substrate" of claim 1.

87. Fujiki forms "stacked body 50 … by alternately depositing the insulating films 51 made of silicon oxide and insulative sacrificial films 91 made of silicon nitride (SiN)" on substrate 10 (again, the '254 Patent does not use "on" to mean directly on such that it physically contacts). Fujiki, [0050].

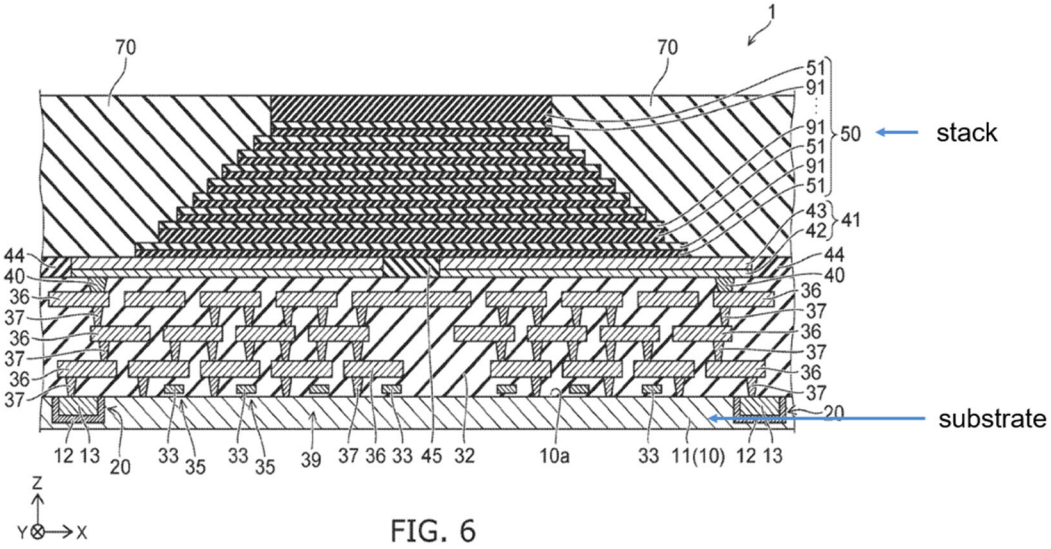


FIG. 6

Id., Fig. 6.

[1.B] "forming a channel structure extending vertically through the stack;"

88. As I describe below, Fujiki discloses forming a channel structure (61, 62, 64-67) extending vertically through the stack (50).

89. Fujiki discloses "memory cell[s] … at each crossing portion between the electrode films 52 and the silicon pillars 62." Fujiki, [0044]. This portion of Fujiki is referring to the fact that in 3D NAND, the channel structures are vertical columns, each column being a string of memory cells. The memory cells are at the intersection of the gate layers and channel structures.

90. Fujiki's FIG. 5 illustrates "a cross-sectional view showing a memory cell." Fujiki, [0008]; *see also id.*, [0044] ("channel"). This view is from the perspective of cutting a channel structure, e.g., at the mid-point height of the channel

structure, and view down to see the layers of the channel structure (these layers extend through the stack and are circular).

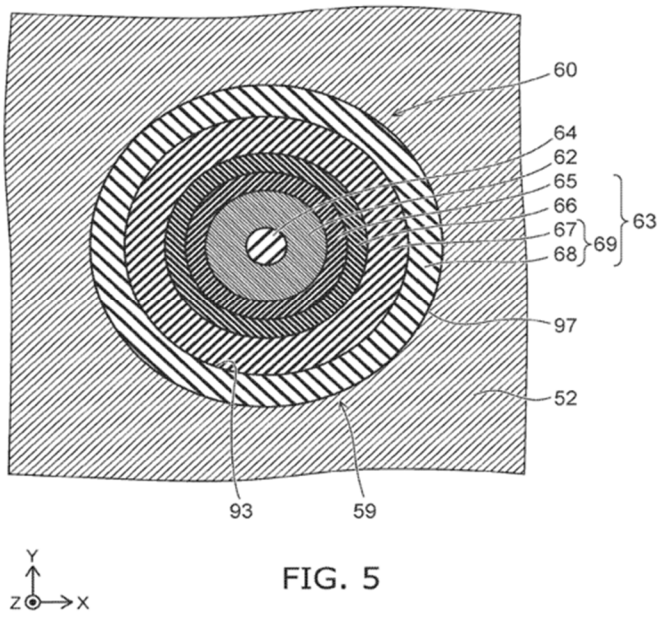


FIG. 5

Id., Fig. 5.

91. As is conventional, Fujiki forms memory holes through the stack that extends to layer 41. Fujiki, [0051-52]. Namely, Fujiki etches through the stack to create the openings for the memory structures. *Id.* Next, Fujiki creates the memory structures by depositing the different memory cell layers into the holes. *Id.*, [0053].

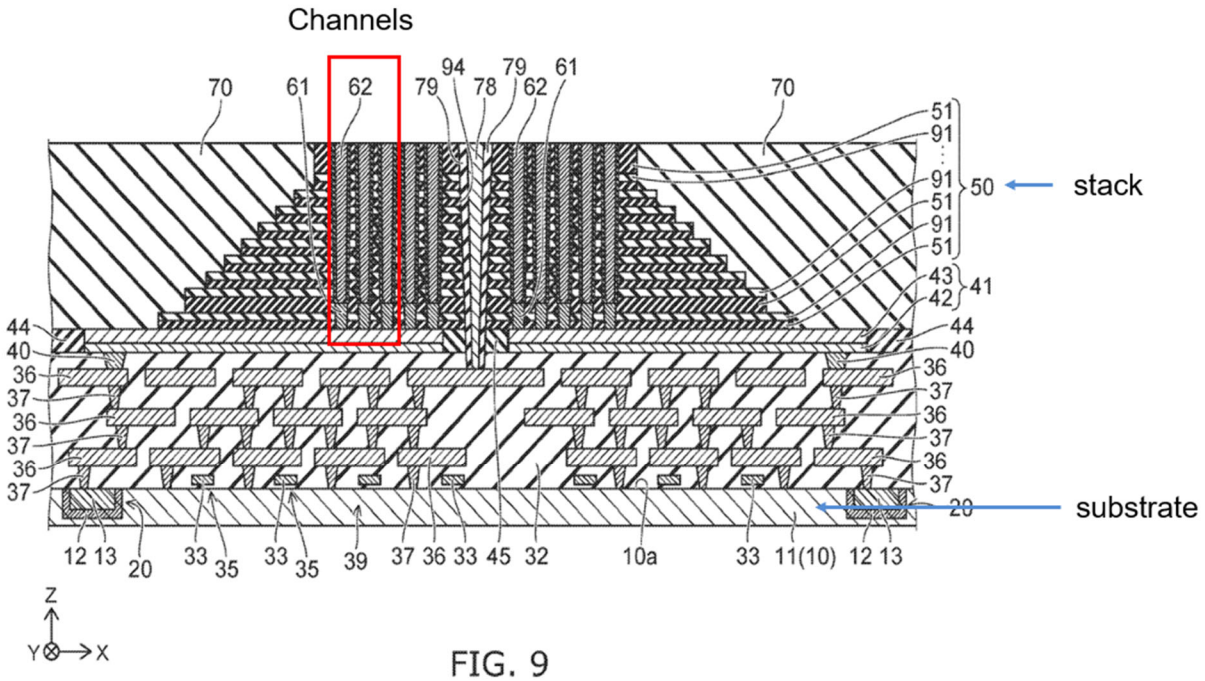


FIG. 9

Id., Fig. 9.

[1.C] "forming a first opening extending vertically through the stack;"

92. As I describe below, Fujiki discloses forming a first opening (94) extending vertically through the stack (50). Note that this limitation and the next two, are the limitations relating to forming the through-array contact (TAC).

93. The first step of forming the TAC is forming "a through-via hole 94 is formed to pierce the stacked body 50, the insulating film 45, and the upper portions of the insulating film 32 and reach a portion of the interconnect 36." Fujiki, [0053]. Like the channels, this involves an etch through the memory stack.

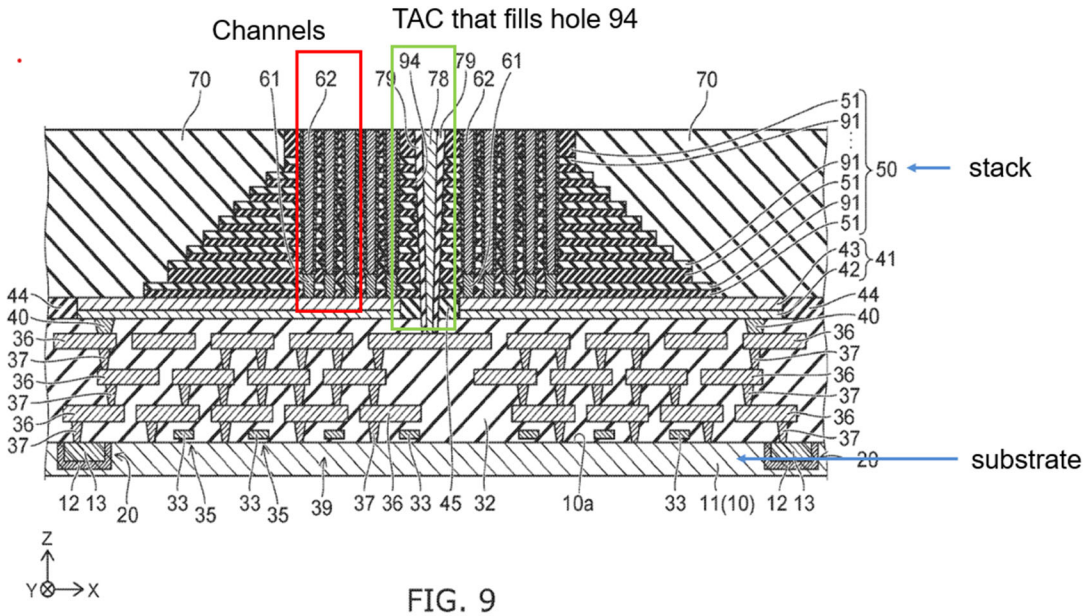


FIG. 9

Id., Fig. 9.

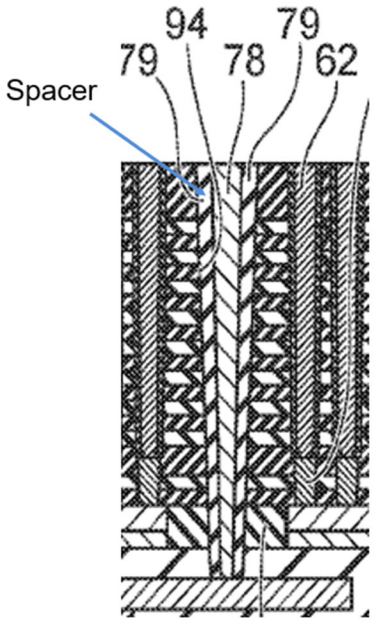
[1.D] "forming a spacer on a sidewall of the first opening;"

94. As I describe below, Fujiki discloses forming a spacer (79) on a sidewall of the first opening (94). This is the second step of forming the TAC.

95. Fujiki discloses "the insulating film 79 is formed on the inner surface of the through-via hole 94." Fujiki, [0053]. As the name implies, the insulating film 79 insulates the conductive through-via (*see* claim [1.E]) from the conductive gate layers and source electrode film. *Id.*, [0042]. The insulating film has various names in the semiconductor industry. For example, another common name for this structure is a liner. In any event, the insulating film (or liner) is a film, typically silicon oxide, that covers the sidewalls of the hole. Recall that the etch to create the first opening etches through the memory stack. Ultimately, that stack comprises

conductive gate layers (after gate replacement if the memory is a gate replacement memory). Thus, if there was not an insulating spacer, the conductive core of a TAC would inadvertently electrically couple to the gate layers.

96. The '254 Patent uses the term "spacer." The '254 Patent describes "spacer" simply as an insulating film (like Fujiki) (again, such a structure was also known as a liner). Namely, these structures insulate (or isolate) the conductive core of the contact from other conductive members along the sidewalls of the TAC. Ex. 1001, 8:52-54.

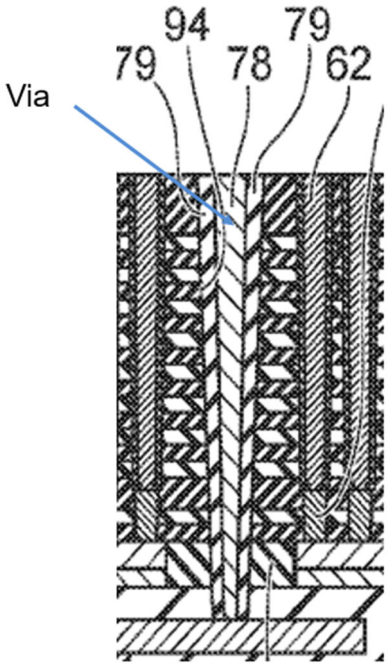


Fujiki, Fig. 9 (partial).

[1.E] "forming a through array contact (TAC) extending vertically through the stack by depositing a conductor layer over the spacer in the first opening; and"

97. As I describe below, Fujiki discloses, or at least renders obvious, forming a through array contact (TAC) (78/79) extending vertically through the stack (50) by depositing a conductor layer (78) over the spacer (79) in the first opening (94).

98. Fujiki discloses "the through-via 78 is formed on the inner surface of the insulating film 79. The through-via 78 is connected to the interconnect 36." Fujiki, [0053].



Id., Fig. 9 (partial).

99. It would have been understood that "through-via 78" is a conductor layer for several reasons.

100. First, Fujiki discloses that "[t]he through-via 78 is insulated from the electrode films 52 and the source electrode film 41 by the insulating film 79." Fujiki, [0042]. The presence of an insulating film surrounding the through-via indicates its conductivity, which aligns with the TAC function in the claimed invention. Also, the "electrode films 52" are the conductive gate layers. The "source electrode film" is the source region of a substrate material in which the bottom of the channel structure extend. *Id*., Fig. 6. The gate electrodes are conductive, and the source region is semiconductive (or conductive depending on the doping level). Thus, when Fujiki references the insulating film "insulat[ing]" the through-via 78 from these elements, Fujiki is referring to the fact that the through-via 78 and these other two elements are conductive, and there is a need to insulate (or isolate) the through-via 78 from these elements.

101. Second, as I describe above, "via" is a well-known term. It refers to a contact between levels that connects upper- and lower-level components. Ex. 1037 (Weste), 157. Of course, to do this, it must be conductive.

102. Third, Fujiki provides a "control circuit" under the array. Fujiki, [0032]. 3D NAND, like other memories, require on-die supporting circuitry (often known as peripheral circuitry or under-array circuitry). Fujiki is referring to such circuitry. Fujiki's through-via connects this circuit to upper-level devices via lower interconnect 36, plug 77, and upper layer interconnect 80. *Id.*, [0042], Fig. 1. Thus,

the via must be conductive to accomplish the connection, i.e., to electrically couple these elements. Were the through-vias not conductive, the electrically coupling would not occur, and the circuit would not operate.

103. It would be routine to fill a contact hole with a conductive material, e.g., tungsten, to form the conductive core. Various depositions techniques are available. Typically, there is a masking, deposition step, and CMP polishing after the deposition.

[1.F] "after forming the TAC, forming a slit extending vertically through the stack."

104. As I explain below, Fujiki discloses, or at least renders obvious, after forming the TAC (78/79), forming a slit (96) extending vertically through the stack (50).

105. The TAC is shown in Figure 9. After this, Fujiki describes "[c]ontinuing as shown in FIG. 10 and FIG. 3, slits 95 are formed to pierce the insulating film 70 and the source electrode film 41; and ***slits 96 are formed to pierce the stacked body 50***. … Then, the sacrificial films 91 (referring to FIG. 9) are removed by performing wet etching via the slits 96. As a result, spaces 97 are formed where the sacrificial films 91 are removed." Fujiki, [0054]. The process sequence in Fujiki of creating the TAC first, followed by forming the slit, aligns directly with this limitation, and the method's explicit steps mirror the TAC and slit formation required by claim 1.

106. The slits 96 are not shown in Figure 10. However, it is clear the slits extend through the stack for several reasons. As an initial matter, Fujiki's use of "pierce the stacked body 50" is instructive. Fujiki uses "pierce" to refer to the slit extending through a particular component, e.g., Fujiki describes that slits 95 "pierce" through "electrode film 41," i.e., extend though the electrode film 41.

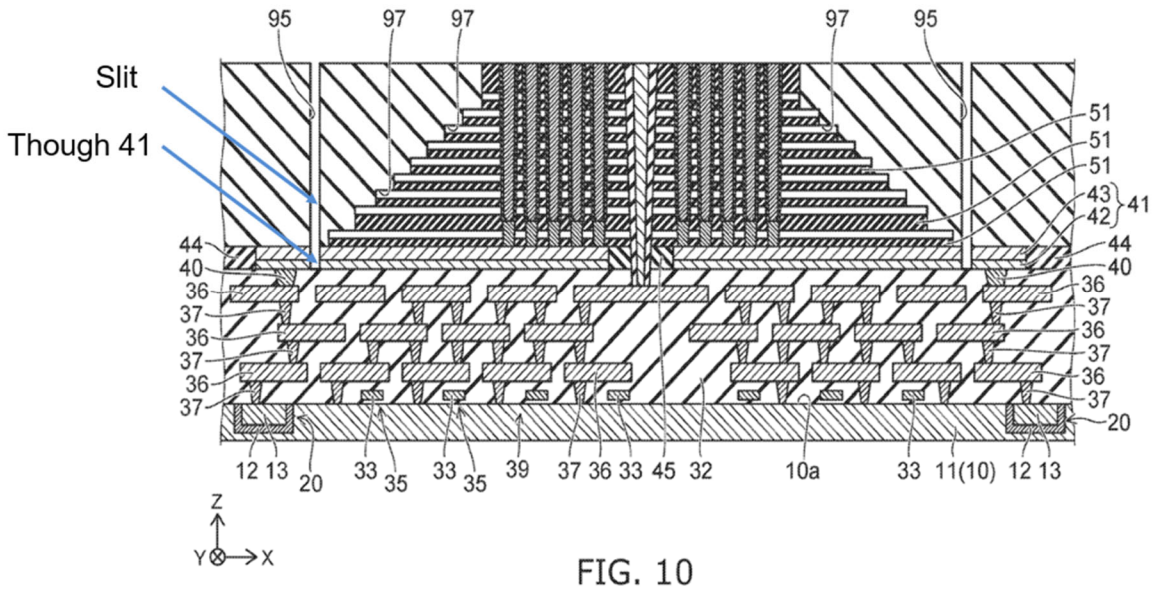


FIG. 10

Fujiki, Fig. 10.

107. Similarly, because Fujiki states "slits 96 are formed to pierce the stacked body 50," this means that the slits 96 extend through the stack. Fujiki, [0054].

108. Note that slits 96 serve as voids for the gate replacement process and ultimately become insulative slit structures 72. Fujiki, [0055]. As I describe below,

this further illustrates that slits 96 pierce the stack. The slits 96 and slit structures 72 are shown in in Figure 3:

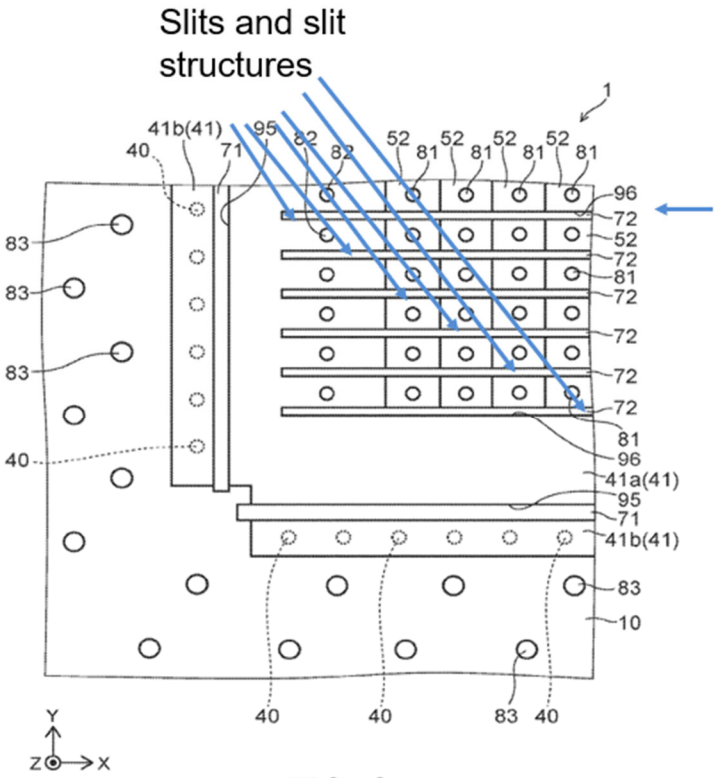


FIG. 3

Id., Fig. 3.

109. I also note that the third embodiment provides more detail on slits 96. The third embodiment additionally provides films 54-55 and plugs 56 to connect the slits structures (71 and 72) that fill slits 95 and 96. The additional film 54 under the stack is shown below:

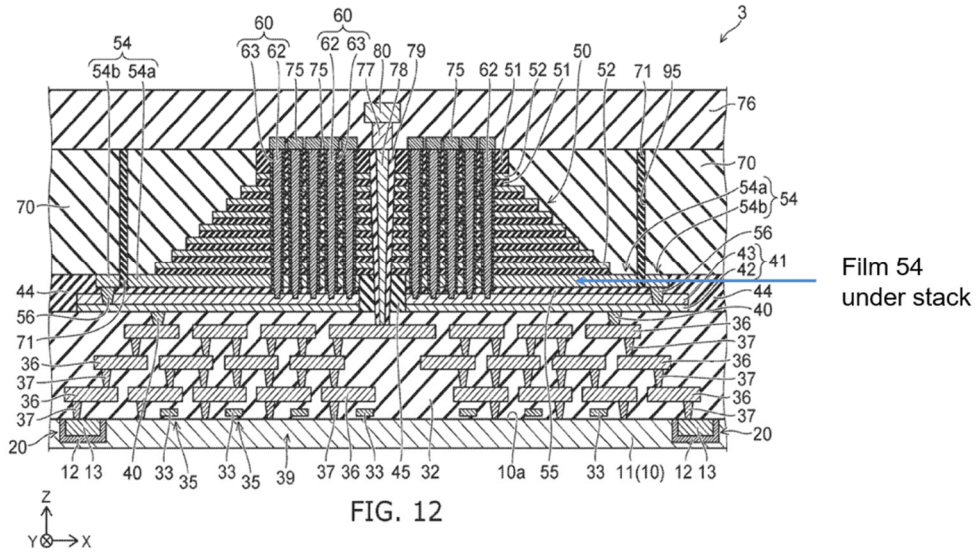


FIG. 12

Fujiki, Fig. 12. In this embodiment, Fujiki describes that the slits "pierce the silicon film 54" to make the connection between slits 95 and 96. Here, the slits extend further, into the silicon film to form the connections. Fujiki consistently uses "pierce" to refer to extending through.

110. It also would have been obvious that the slits extend through the stack even without the above context for several reasons.

111. First, as I describe above, Fujiki employs a gate line replacement process using the slits (to etch out the sacrificial gates and deposit the replacement gates). Fujiki, [0055]. Performing this process via slits that extend through the stack was conventional and, as I describe below, necessary. Ex. 1005 ("Nakajima"), 8:12-15, Fig. 11.

112. Second, a typical etch for creating the slits is, for example, an RIE etch. *Id.* It is important that etch extends through the stack. This is because the sacrificial layers ultimately become the conductive gates, e.g., tungsten gates. Typically, the bottom gate layers may be select gates (e.g., source-side select gates). If the replacement process fails to replace the bottom gates, the device will effectively be non-functional, because, for example, the bottom gates will remain sacrificial material, e.g., silicon nitride, and the bottom memory cells will not turn on. Reading a middle memory cell, for example, requires turning on the above and below memory cells (e.g., with a pass voltage). Thus, the etch step for creating the slits must ensure to reach through the stack, and that there is a natural buffer below the stack (the layer underlying the memory stack).

113. In short, while Fujiki discloses a slit that extends through the stack, even without that context, a POSITA would have had the obvious motivation to do so to ensure fabricating a functional device. Such etches, similar to TAC or channel etches, were textbook material and involve masking and etch, e.g., RIE.

2. Claim 2:

[2] "The method of claim 1, further comprising prior to forming the first opening, forming a dummy channel structure extending vertically through the stack."

114. As I describe below, Fujiki in view of the knowledge of a POSITA renders this limitation obvious.

115. As to the temporal requirement, Fujiki discloses forming channel structures before the TAC (which involves "forming the first opening"). Fujiki discloses forming the channels and states "[t]hen, a through-via hole 94 is formed …." Fujiki, [0053].

116. Concerning dummy channels, a POSITA would have been motivated, with a high expectation of success, to also form dummy channels for several reasons.

117. First, it has been well known for decades that elements, such as channel structures, at the end of an array are subject to process variations. Ex. 1020 (U.S. Pat. 5,945,717), 8:47-53 ("In a typical flash cell array, cells located at the edge of the array are much more subject to processing variations than the cells not located at the edge. Because of this, it is common to refrain from using the cells at the array edge. Such cells, which extend around the perimeter of the array, are sometimes referred to as dummy cells."). For modern processes, this has become even a greater issue. Ex. 1021 (U.S. Pat. 10,347,487), 2:20-43 ("Edge of array issues may typically occur at the boundary between a chop mask and pitch double patterning. An abnormality at the edge of an array pattern can cause blowout or shorting issues, depending on the integration process. Conventionally, an abnormal edge pattern at the edge of array may be controlled by adding a dummy pattern region, which is later sacrificed in processing."). Thus, one normally employs dummy channel

structures at the edge of the array. Otherwise, these channel structures may be defective, and not properly store data.

118. Second, adding dummy channels such that the overall pattern is more consistent was well known for decades, too. Ex. 1022 (Ronse), 11 ("As a result, this technique is particularly useful in regular patterns like memories, and much less in random logic designs where features can be completely irregular."). Semiconductor fabrication involves patterning, and patterning periodic structures is much more difficult than a consistent pattern due to, for example, pattern distortion. Thus, again, the use of dummy structures was the norm to reduce fabrication issues.

119. Third, dummy channels provide structure support, which is important during the gate line replacement process. As I describe above, Fujiki uses a gate replacement process. Fujiki, [0055]. This process etches out the sacrificial gates and leaves voids where those sacrificial gates were in the stack. As a result, "support pillars" are necessary to support the stack during this process. Ex. 1018 (U.S. Pat. 8,945,996), 5:64-6:2, 7:19-23. A common support structure was a dummy channel. Ex. 1019 (U.S. Pat. 10,115,632), 30:14-27; *see also id.*, 15:3-22 (structures 20 are dummy channel structures). I note that it was well known to include dummy support members that extend through the entire stack or partially through the stack. Ex. 1015 (Kai), Fig. 6A (support members 20), 16:28-38. For example, the dummy channels may be on the edge of the array or in the staircase region.

120. Prior art references such as Kai confirm that adding active and dummy channels for structural support was a recognized technique, as dummy channels provide reinforcement without requiring upper-level connections, a key feature for achieving structural integrity in high-aspect-ratio stacks. Ex. 1015 (Kai), 10:20-27. A POSITA would apply this approach as a routine measure to bolster stack stability, particularly during gate replacement processes. This predictable implementation leverages standard support techniques recognized as necessary for maintaining high-aspect-ratio structures. *E.g.*, *id.*, 9:23-26 (defining "support opening" as "a structure in which a support structure (such as a support pillar structure) that mechanically supports other elements is subsequently formed"), 9:45-48 ("support openings 19" extend through stack), 10:20-27 (forming channels in support openings).

121. By way of example, Kai refers to the dummy channels as "support pillar structure 20" and active channels as "memory stack structures." Ex. 1015 (Kai), 16:28-38; Fig. 15A, 25:58-63 (dummy support channels (20) have no connection to the upper level, whereas the active channel structures (55) include contacts (88)). By way of another example, Park discloses forming active and dummy, supporting channels. Ex. 1016 (Park), 6:19-26, 7:45-51. Kim provides another similar example of forming active and dummy, supporting channels. Note that dummy channel structures can be made at the same time as active channels, and if the dummy channels have all the same materials as the active channels, this saves processing

time. Ex. 1017 (U.S. Pat. Pub. 2018/0308559) [0047] ("The stack structure ST may be penetrated with a plurality of dummy holes DH on the connection region CTR," "DS may physically support," and listing same materials as channels), [0071] ("The channel holes CH and the dummy holes DH may be formed at the same time."), [0072] (same time), Fig. 13 (DH through stack on edge).

122. Fourth, as I note above, dummy channels can be made by the same process and at the same time as the active channels. Ex. 1015 (Kai), 10:20-27. The dummy channels, however, typically will not include interconnects to upper-elements, because the structures do not store data. Thus, dummy channels do not consume space above the structures, but still function as support members (and have the processing benefits that I describe above).

123. Finally, employing dummy structures would have been routine and a POSITA would have had a high expectation of success in doing so. First, Fujiki already discloses forming channel structures. Simply not connecting a channel structure to upper-level interconnects, such that it is an active channel, forms a dummy channel. The materials in the active and the dummy channels can be exactly the same. Also, I describe above that the addition of dummy channel structures actually reduces processing issues, such as defective bits and simplifies patterning. And again, these were commonplace and textbook material for decades.

3. Claim 3:

[3] "The method of claim 1, wherein forming the first opening comprises simultaneously etching the first opening through the stack and a second opening outside of the stack."

124. As I describe below, Fujiki discloses, or at least renders obvious, this limitation.

125. In addition to the through-vias in the middle of the stack, Fujiki discloses forming "contacts 81 to 83" outside of the stack. Fujiki, [0043]. These include contacts 82 and 83 that extend through insulating layer 70. Either is in a "a second opening":

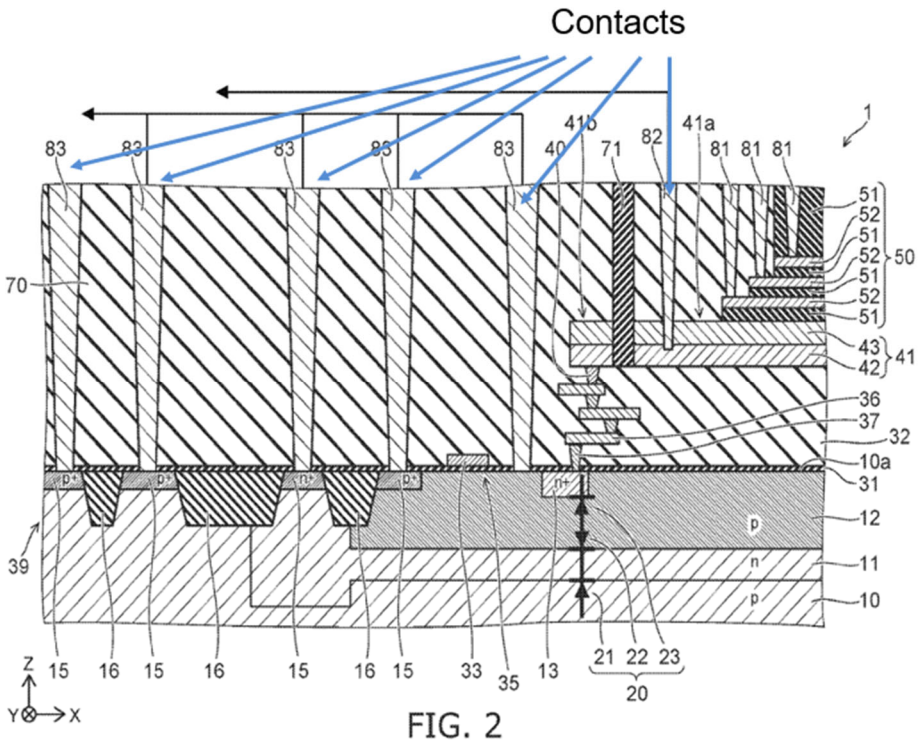


FIG. 2

Id., Fig. 2.

126. Fujiki only describes forming one through-via in his description. Fujiki, [0050]. It would have been understood, or at least obvious, that Fujiki discloses forming multiple through-vias at the same time, and also forming the contact holes for 82 and 83 at the same time, thus streamlining the manufacturing process and minimizing processing steps. As an initial matter, Fujiki states that the shown components are "fewer than the actual components." *Id.*, [0024]. It would be atypical for there to a be single through-via in Fujiki, and Fujiki would not have been understood to disclose a single through-via. The conventional 3D NAND configuration with TACs includes multiple TACs. *E.g.*, Ex. 1010 (Mushiga), Fig. 5, 10:31-58; Nakajima, Figs. 1, 2 (multiple TACs, i.e., C4s), 7:26-8:11. And it was typical to describe a process for creating a single contact even though that process actually forms multiple contacts simultaneously, because the focus is on the steps to create that contact (and that process just scales with masking to create additional instances). *E.g.*, Nakajima, Figs. 1, 2 (multiple TACs, i.e., C4s), 7:26-8:11.

127. Next, the first issue when considering whether one would etch holes simultaneously in different areas of the memory is whether those areas are in a state in which such simultaneously etching is possible. As can be seen above, insulating film 70 surrounds the stacked body and the contacts. Fujiki, [0040]. This is a deposition of, e.g., silicon oxide, to insulate the various portions of the chip and create a planar upper level (for additional layers, e.g., local contacts). Because

insulating film 70 has been deposited by the time the through-vias are etched, the holes for 82 and 83 can also be etched at the same time. *Id.*, Figs. 8-10. Simultaneous etching of openings for TACs and peripheral contacts was well known for reducing processing time and improving efficiency. This approach is routinely documented in prior art references such as Mushiga, where contacts within and outside the array are formed concurrently. Ex. 1010 (Mushiga), 10:31-58.

128. A POSITA would have been highly motivated to simultaneously etch the through-vias and contacts 82 and 83.

129. Importantly, this approach would significantly reduce processing time. Even the basic process of etching the holes involves multiple steps, e.g., forming a mask, etching the hole, etching out the bottom, potential clean steps, etc. Repeating this entire sequence for separate holes, when unnecessary, would be inefficient. Therefore, avoiding redundant processing steps was widely recognized as efficient practice, even when creating holes for both active and dummy elements. Ex. 1023 (U.S. Pat. Pub. 2019/0081061, Tessariol), [0037] ("dummy-structure openings 56 and via openings 54 are formed at the same time (i.e., simultaneously)"), Fig. 9. This efficiency advantage led to the development of etching chemistries, dating back many decades before the filing of the '254 Patent, that are able to even etch different hole sizes at the same time. *E.g.*, Ex. 1043 (Wolf Vol. 2), 47

130. Simultaneous formation would have been routine and highly predictable. Such techniques were well known in the art. For example, Mushiga demonstrates forming holes for through-array contacts (588) (as well as insulating spacers and conductive cores) at the same time in various portions of the memory device was routine and well understood:

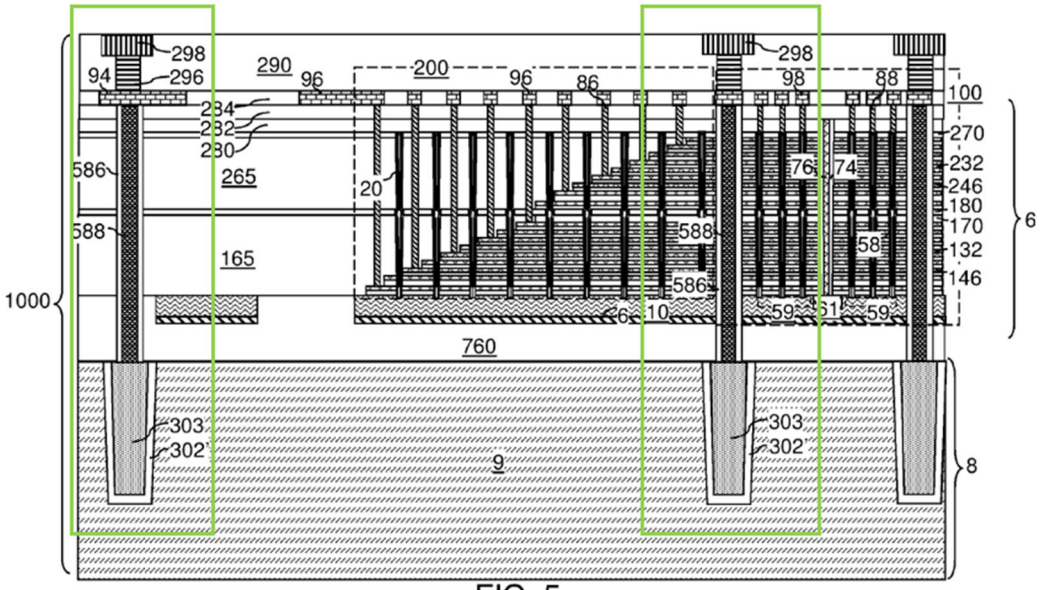


FIG. 5

Ex. 1010 (Mushiga), Fig. 5, 10:31-58.

131. Similarly, Masamori discloses forming holes for multiple contacts (as well as the conductive fill) at the same time, and even forms support structures and multiple contacts at that same time:

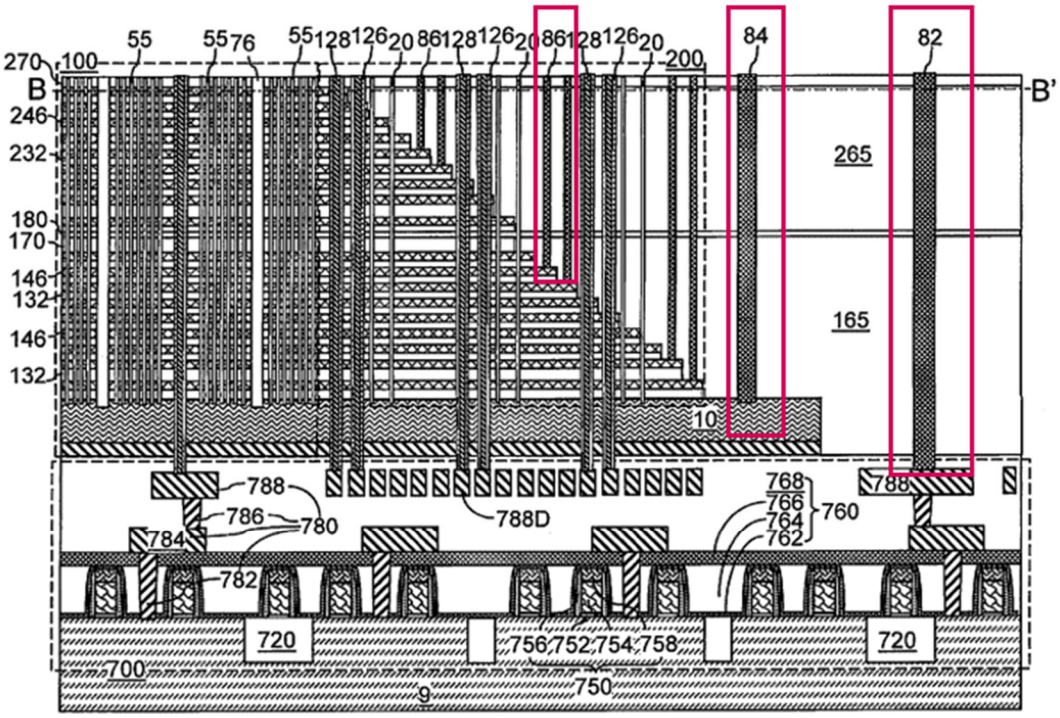


FIG. 13A

Ex. 1019 (U.S. Pat. 10,115,632), Fig. 13A, 24:22-29 ("Alternatively, two or more types of contact via structures (82, 84, 86) may be formed employing a common set of patterning processes and fill processes provided that the anisotropic etch process therein can control vertical extent of cavities at target height levels for each type of cavities that are simultaneously formed.").

132. As shown above, the contact holes extend down to target depths that interface with a different type of material: conductive gate layer (86), the substrate (84), and a metal interconnect (82). Masamori describes using a timed anisotropic etch to control the target heights. *Id.* A timed anisotropic etch is a directional etch

in which the duration controls the depth. These etches, and other more complex etches, e.g., including a punch through step at the end as the etch progresses to a different material, were well known well before the '254 Patent's priority date.

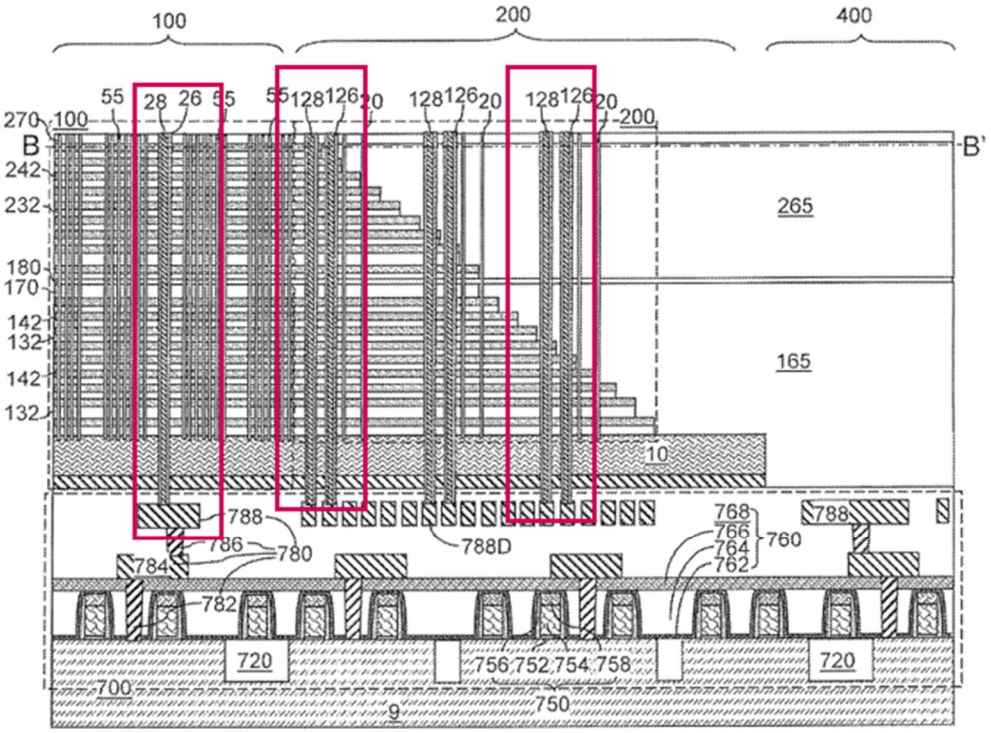


FIG. 8A

Ex. 1019, Fig. 8A, 17:51-54 ("In one embodiment, the laterally-insulated support structures (126, 128) can be formed concurrently with the laterally-insulated conductive via structures (26, 28) and can have the same structure.").

133. Kai II also discloses forming openings for various contacts and memory structure openings in a single step:

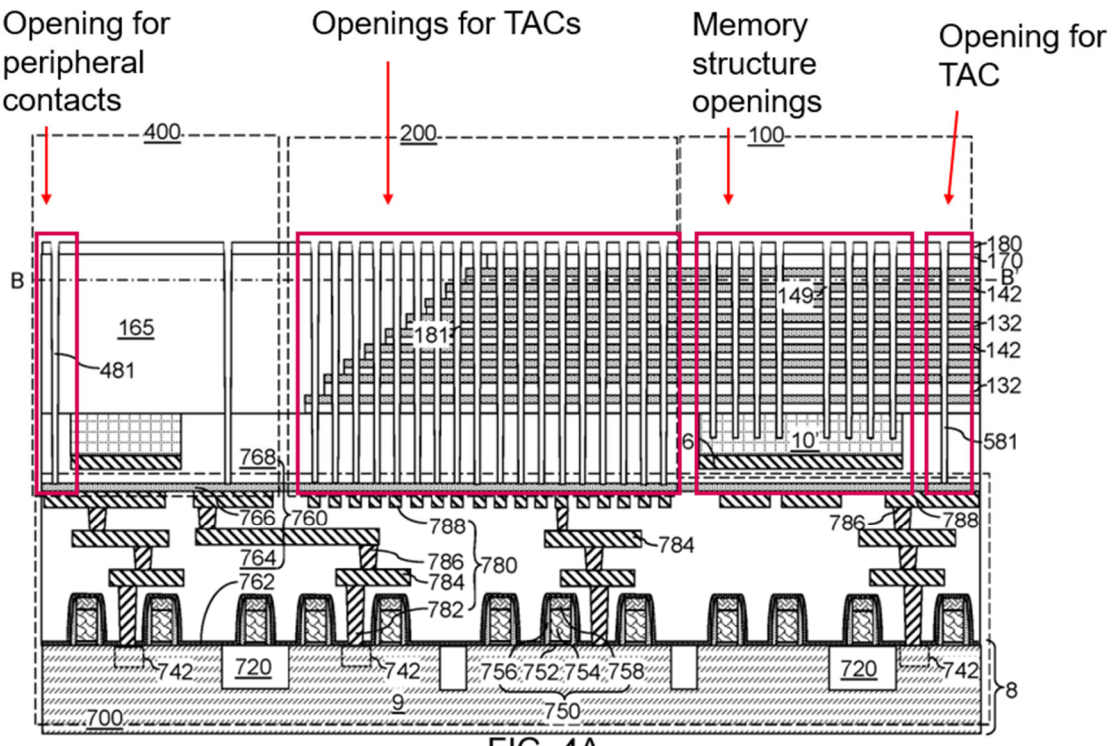


FIG. 4A

Ex. 1038 (U.S. Pat. 10,388,666, Kai II), Fig. 4A, 17:30-44 ("The pattern of openings in the photoresist layer can be transferred through the inter-tier dielectric layer 180 and the first-tier structure (132, 142, 170, 165) and into the in-process source-level material layers 10′ and the at least one second dielectric layer 768 by a first anisotropic etch process to form the various first-tier openings (149, 181, 481, 581) concurrently, i.e., during the first anisotropic etch process. The various first-tier openings (149, 181, 481, 581) can include first-tier memory openings 149, first-tier staircase-region openings 181, first-tier array-region openings 581, and first-tier peripheral-region openings 481.").

134. Like Masamori, Kai II's contact holes extend to different target depths that interface to different materials: the memory structure openings (149) extend into the substrate (as shown above) and other openings extend down to the metal interconnects. *E.g.*, Ex. 1038, 17:48-58, 18:9-21 (181 and 581 openings extending to interconnect). Again, Kai II employs an anisotropic etch. *Id.*, Fig. 4A, 17:30-44. A timed-anisotropic etch can control the target depth, but again, other etch techniques were also well known.

135. As I describe above, Fujiki would have been understood to simultaneously etch multiple contact holes, and thus it would have been obvious to extend this to different types of contact holes.

136. A POSITA would have had a high expectation of success to simultaneously etch the through-via holes and 82 and 83 contact holes. First, as I describe above, the memory device is in a state (with the insulating fill) to enable the etch. Second, etch chemistries and types (e.g., anisotropic) that simultaneously etch holes, including despite some of the holes extending through all of the stack and other holes extending through only a portion (or none) of the stack, were well known and routine to implement. *E.g.*, Nakajima, 7:37-43 (forming holes for C4 contacts), Fig. 2 (TACs, C4, through in various locations); Ex. 1023 (Tessariol), [0037] ("dummy-structure openings 56 and via openings 54 are formed at the same time (i.e., simultaneously)"), Fig. 9 (extending through different number of stack layers).

As I describe above, controlling the timing of, for example, an anisotropic etch along with masking techniques that define the hole pattern, i.e., define the location of the contact holes, enables the simultaneous etching. These were well known techniques well before the '254 Patent's priority date. Of course, more exotic deposition techniques were also known before the '254 Patent that can fine tune the etch depths, including etch chemistries. *E.g.*, Ex. 1043 (Wolf Vol. 2), 47.

4. Claim 4:

[4] "The method of claim 3, wherein forming the TAC comprises depositing the conductor layer in the first opening to form the TAC and in the second opening to form a peripheral contact."

137. My analysis under claim [1.E] demonstrates that Fujiki deposits the conductor layer in the first opening. The '254 Patent uses "peripheral contact" to refer to contacts outside of the memory stack, and contacts 82 and 83 are outside of the memory stack. Ex. 1001, 10:2 (peripheral contact 148), Fig. 1. Contacts 82 and 83 are outside of the array (see claim [3] analysis). Fujiki deposits a conductor layer in the second opening to form contacts 82 and 83, as those are contacts, and would have been understood to include, e.g., tungsten. Fujiki, [0043].

138. The claim language does not recite a simultaneous requirement with respect to depositing the conductive layer. As I describe below, however, Fujiki discloses, or at least renders obvious, simultaneously depositing conductive layers in the first and second holes by describing multiple conductive vias that could be

deposited in a single step for both the TAC and peripheral contacts. The deposition process for filling the TAC is equally applicable to peripheral contacts, allowing a single conductive deposition step for both types of contacts, thus meeting the limitation of forming a conductor layer in both openings.

139. The convenience and predictability of using a single deposition step for both types of contacts are further supported by Mushiga, which documents simultaneous deposition for TACs and peripheral contacts. Ex. 1010 (Mushiga), Fig. 5, 10:31-58.

140. As I explain in my claim 3 analysis, it would have been understood, or at least obvious, to form the through-via and contact 82 and 83 holes at the same time. For the same reasons, it would have been understood, or at least obvious, to form the conductive layers at the same time. Just like Fujiki describes forming a single through-via hole, Fujiki describes forming a single through-via core. Fujiki, [0052]. But as I describe for claim 3, Fujiki would have been understood to disclose multiple through-vias at the same time, that is, form multiple insulating layers. The conductor core for such contacts is typically the same material, e.g., tungsten. Thus, Fujiki would simply employ the same deposition of the same material to fill through-via holes and contact holes 82 and 83. Again, this would save significant processing time. Lastly, the deposition of a metal core was highly routine and predictable, as the examples in claim 3 demonstrate.

5. Claim 5:

[5.PRE] "The method of claim 1, wherein forming the spacer on the sidewall of the first opening comprises:" [5.A] "depositing a dielectric layer on the sidewall and a bottom surface of the first opening; and"

141. As I describe below, Fujiki renders this limitation obvious in view of the knowledge of a POSITA.

142. Fujiki discloses forming a spacer on the sidewall of the first opening by depositing a dielectric layer on the inner surface. This technique is a predictable and routine implementation in the field, commonly used in fabricating high-aspect-ratio structures, as noted in Ex. 1025 (Hwang). A POSITA would readily recognize the use of this layer deposition method as a standard, textbook approach, ensuring uniform insulating coverage within the opening.

143. Fujiki does not detail the process for forming the insulating film on the through-via hole. While the final insulating film will not be on the bottom of the through-via hole (as the through-via conductive core must electrically couple to an underlying element), the initial deposition of the liner typically will deposit onto the bottom surface. This is a result of the deposition, namely, the deposition chemistry will simply deposit the dielectric material, e.g., silicon oxide on the exposed surfaces of the holes. *E.g.*, Ex. 1028 (U.S. Pat. 9,728,546), 34:62-35:3 ("The dielectric liners 141 can be formed, for example, by formation of a dielectric material layer including a first dielectric material, and by a subsequent anisotropic etch (such as a reactive

ion etch) that removes horizontal portions of the dielectric material layer to form dielectric spacers 141"), 17:41-46 ("Each first semiconductor channel portion 601 can be formed on inner sidewalls of each memory film 50 by deposition of a semiconductor material layer and a subsequent anisotropic etch of the semiconductor material layer.").

144. This can be seen in Nakajima which describes and depicts this effect of the deposition process: "silicon oxide layer 81 is conformally formed along the bottom and the side surface of the hole H1." Nakajima, 7:44-49.

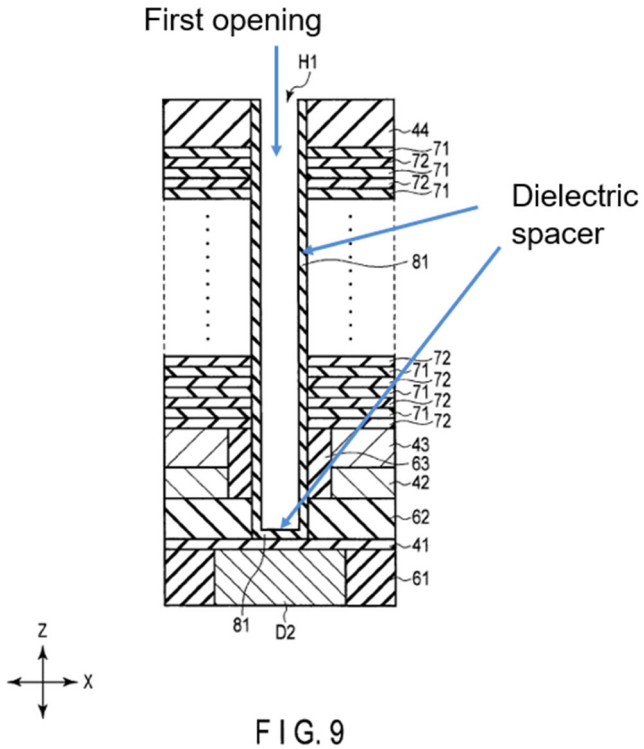


FIG. 9

Id., Fig. 9.

145. I note that depositing a conformal liner typically results in this bottom coverage. *E.g.*, Nakajima, 7:44-49 ("silicon oxide layer 81 is conformally formed along the bottom and the side surface of the hole H1"). Attempting to conformally deposit, for example, silicon oxide without resulting bottom coverage would be difficult if not impractical. Put another way, simply creating the conformal liner and then removing the bottom portion is more straightforward than creating a process that avoid bottom coverage.

146. Conformal liners are important. Dimensions have shrunk a great deal in semiconductor devices. An aspect ratio of such through vias is already high. Thus, a thin conformal layer to properly insulate the entire sidewall area, yet leave room for the conductive cord, was important. This need drove the popularity of ALD processes for this and other purposes. Ex. 1025 (Hwang), 12 ("better conformality over three-dimensional (3D) structures"), 13 ("unprecedented conformality over the 3D structures").

147. Conformal deposition techniques that cover the bottom portion, while also providing beneficial thin, conformal layers, were highly predictable. Indeed, ALD was textbook material well before the '254 Patent. The exact process of forming a liner (and then removing the bottom portion) was well understood, and involves, for example, basic depositions (e.g., ALD) and etches (e.g., anisotropic etch). *E.g.*, Nakajima, 7:44-61 (deposition and etch to form spacer); Ex. 1028 (U.S.

Pat. 9,728,546), 17:41-46, 34:62-35:3 (same); Ex. 1009 (Toyama), [0226], [0313] (ALD for spacers); Ex. 1023 (Tessariol), [0038], [0063] (recognizing multiple suitable deposition and etch types for spacers).

[5.B] "removing part of the dielectric layer that is deposited on the bottom surface of the first opening."

148. As I describe below, Fujiki renders this limitation obvious in view of the knowledge of a POSITA.

149. As I demonstrate in my analysis of claim [5.A], it would have been understood, or certainly obvious, to form Fujiki's liner with a conformal deposition that results in initial dielectric on the bottom portion of the hole. Of course, as I explain there, it then become necessary to remove it. Fujiki's through-vias connect to lower interconnects 36. Fujiki, [0042], Fig. 1. Were this bottom oxide present, the through-vias would be unable to electrically couple to the lower interconnects. The techniques to remove this bottom oxide were well known, as Nakajima demonstrates: "Next, as shown in FIG. 10, a portion of the silicon oxide layer 81 that is located at the bottom of the hole H1 is removed by, for example, RIE using a mask layer not shown in the drawing, so that the silicon nitride layer 41 is exposed." Nakajima, 7:50-53.

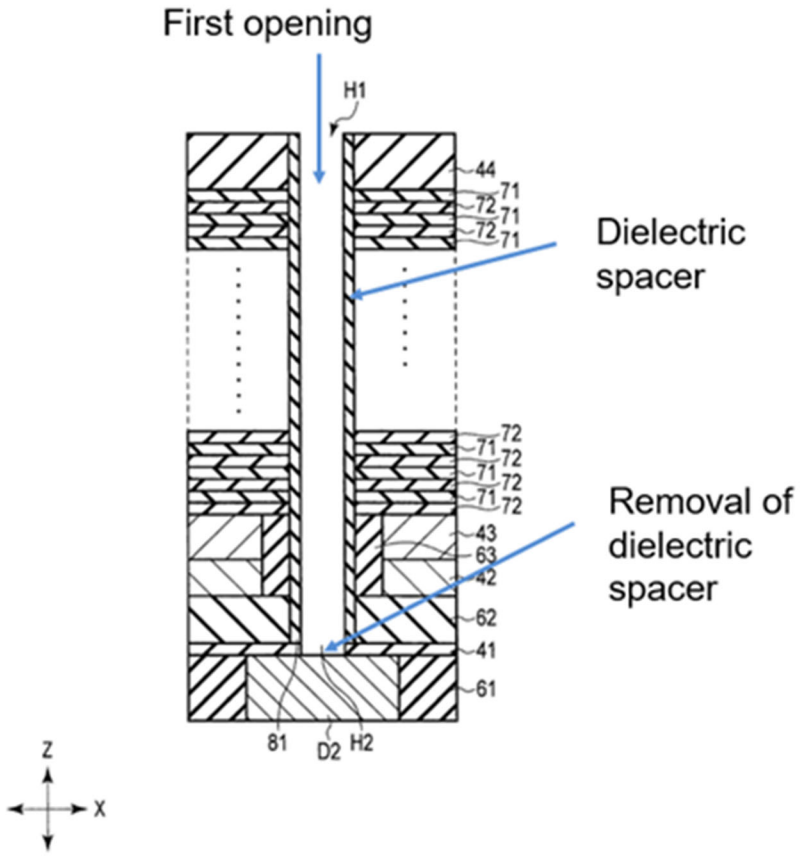


FIG. 10

Nakajima, Fig. 10; *see also* Ex. 1028 (U.S. Pat. 9,728,546), 17:41-46, 34:62-35:3 (same).

150. Again, as with the conformal depositions to deposit the liner, the etch techniques, e.g., RIE, to remove the bottom oxide were likewise textbook material.

6. Claim 6:

[6] "The method of claim 5, wherein the deposition of the dielectric layer comprises atomic layer deposition (ALD), and the removal of the part of the dielectric layer comprises anisotropic etching on the bottom surface of the first opening."

151. As I explain below, Fujiki renders this limitation obvious in view of the knowledge of a POSITA.

ALD

152. Fujiki does not detail the processing steps to form insulating film 79 (spacer) for the through-via (TAC). Fujiki, [0053]; *see also* claim [1.D] analysis. My analysis under claim 5 demonstrates that it was obvious to form a conformal spacer.

153. ALD was a standard technique to deposit a conformal dielectric spacer, e.g., a silicon oxide spacer, in a hole or trench (e.g., hole through a memory stack using). Ex. 1009 (Toyama), [0226] (backside trench 79), [0313] (moat trenches 579); Ex. 1024 (U.S. Pat. 9,620,514), 35:51-61 (forming "dielectric spacer" by first forming "silicon oxide layer" via "ALD"); Ex. 1023 (Tessariol), [0063] (ALD), [0038] (conductive vias 58).

154. A POSITA would have been motivated to employ ALD for Fujiki's liner for several reasons.

155. First, conformal spacers ensure uniform insulating material to insulate the conductive core, and ALD is ideal to deposit thin dielectric layers (which an insulating spacer is). The liner obviously must be relatively thin given the high aspect ratio and relatively small dimensions of TACs in the array. ALD grew in popularity for its ability to deposit material conformally for 3D structures. Ex. 1025 (Hwang), 12 ("better conformality over three-dimensional (3D) structures") 13 ("unprecedented conformality over the 3D structures").for several reasons.

Conformal deposition has always been a key benefit of ALD. Ex. 1025 (Hwang), 12 ("better conformality over three-dimensional (3D) structures") 13 ("unprecedented conformality over the 3D structures").

156. Second, ALD was textbook material well before the '254 Patent's priority date, including for this exact application. The specific process steps for such spacers were readily available.

157. Third, ALD was highly predictable and understood for this application, as it was textbook material. *Id.*; Ex. 1042 (Wolf Vol. 1), 32-36 (decade old textbook describing anisotropic etches); Ex. 1009 (Toyama), [0226], [0313]; Ex. 1023 (Tessariol), [0063], [0038].

Anisotropic Etching

158. My analysis for claim 5 demonstrate that it would have been obvious to form the conformal liner and remove the bottom portion. One obvious technique to remove the bottom portion is anisotropic etching.

159. For example, Nakajima discloses "[n]ext, as shown in FIG. 10, a portion of the silicon oxide layer 81 that is located at the bottom of the hole H1 is removed by, for example, RIE using a mask layer not shown in the drawing, so that the silicon nitride layer 41 is exposed." Ex. 1005, 7:50-53. The resulting sidewalls are vertical. Such RIE etches that are anisotropic were well known. Ex. 1026 (U.S. Pat. 10,515,799), 6:63-65 ("For example, channel hole 120 can be formed by

anisotropic reactive ion etching (RIE)."); Ex. 1027 (U.S. Pat. 9,570,460), 11:55-58 ("The at least one memory film 7, 9, 11 and cover layer 410 may be etched using RIE or another suitable anisotropic wet or dry etching method to form the opening 417."). Anisotropic etching aims to remove material in a specific direction and that is precisely what Nakajima's RIE etch does.

160. I also note that it was well known that to form a material, including a dielectric liner, on only the sidewall of a hole, the typical approach involves a deposition and then an etch—such as an anisotropic etch—to remove the deposition on the bottom portion. Ex. 1028 (U.S. Pat. 9,728,546), 34:62-35:3 ("The dielectric liners 141 can be formed, for example, by formation of a dielectric material layer including a first dielectric material, and by a subsequent anisotropic etch (such as a reactive ion etch) that removes horizontal portions of the dielectric material layer to form dielectric spacers 141"), 17:41-46 ("Each first semiconductor channel portion 601 can be formed on inner sidewalls of each memory film 50 by deposition of a semiconductor material layer and a subsequent anisotropic etch of the semiconductor material layer.").

161. An advantage of anisotropic etch, which provides a motivation to employ this technique, is that an anisotropic etch is directional. Thus, in a high-aspect ratio hole, the directional etch can target the bottom of a hole with a small diameter. Nakajima, 7:50-53 (employing anisotropic etch to remove bottom

dielectric portion in high aspect ratio hole). Another benefit is that because the etch is directional, the directional nature of the etch mitigates the risk of etching through the sidewall dielectric. Were an etch to remove too much of the sidewall, there would be no insulator liner on that portion, causing an inadvertent electrical coupling between the TAC and, e.g., a conductive gate layer.

162. Anisotropic etches were textbook material well before the '254 Patent and well understood. *E.g.*, Ex. 1026 (U.S. Pat. 10,515,799), 6:63-65 ("anisotropic reactive ion etching (RIE)"); Ex. 1027 (U.S. Pat. 9,570,460), 11:55-58 ("RIE or another suitable anisotropic wet or dry etching method"). Such etches were readily available for this purpose and the above illustrates.

7. Claim 7:

[7.PRE] "The method of claim 1, wherein forming the spacer on the sidewall of the first opening comprises:" [7.A] "forming a plurality of shallow recesses by removing parts of the sacrificial layers abutting the sidewall of the first opening;"

163. As I explain below, Fujiki renders this limitation obvious both under PO's incorrect interpretation and under the correct interpretation. I address this limitation under what appears to be PO's incorrect interpretation of the limitation and the correct interpretation.

164. The '254 Patent discloses an etch that intentionally forms recesses in the sacrificial layers. Ex. 1001, 13:47-61, Fig. 3D. It appears in alleging infringement in the district court case, however, PO interprets this claim to include

largely undetectable and unintentional alleged recesses. Ex. 1029 (Ex. A-2, YMTC's Contentions), 30. In typical etches through a stack with silicon oxide and silicon nitride layers (usually the composition of the sacrificial gates), the result will be recesses in either the silicon oxide or silicon nitride layers due to what is known as etch selectivity. In simple terms, an etch involves using a chemical, which may in a wet or dry form, to remove material. That chemical, however, can favor a particular type of material, and more aggressively remove that material. For a stack of silicon oxide and silicon nitride layers, prior art etches would typically favor one of these material types. Ex. 1030 (U.S. Pat. 11,075,084), 2:59-67 (In "3D NAND memory, it is important to have an etching gas which can etch both SiO_2 and SiN layers (or both SiO_2 and p-Si layers) without selectivity. In another words, it is a challenge to find an etch gas that has similar high etch rates of SiO_2 and SiN in terms of getting a smooth sidewall of high aspect ratio holes in 3D NAND memory."). Thus, prior art etches would naturally create very small lateral recesses, which may be in the silicon nitride sacrificial layers depending on the etch type. *Id*., 2:59-67.

PO's Incorrect Claim Interpretation

165. Recall that Fujiki discloses etching through a silicon nitride and silicon oxide stack (*see* claim [1.A], [1.C]). And recall that typical prior art etches that effectively create a hole through that stack result in very small lateral recesses in either the dielectric spacers or sacrificial layers. Ex. 1030 (U.S. Pat. 11,075,084),

2:59-67. Thus, it would have been obvious that small unintentional recesses would naturally result, because this was known as a natural result of these prior art etches.

The Correct Claim Interpretation

166. Creating intentional lateral recesses in a hole for a contact, however, was also known. For example, Cui (U.S. Pat. 10,304,852) discloses contacts 183 that travel through the staircase and through the entire array. Ex. 1031 (Cui), Fig. 14A, 25:51-53 (e.g., 183 contact on right of region 200); *see also* Ex. 1015 (Kai), 11:9-34 ("laterally recessed"). Cui discloses two types of these holes. First, Cui depicts an embodiment in which the sidewalls of this contact are straight ("cylindrical via cavity"). Ex. 1031 (Cui), Fig. 15A, 25:63-26:22. Second, Cui depicts an alternative embodiment with large recesses in the conductor layers ("ribbed via cavity"). *Id.*, Fig. 16A, 26:23-32. In other words, both alternative options were known.

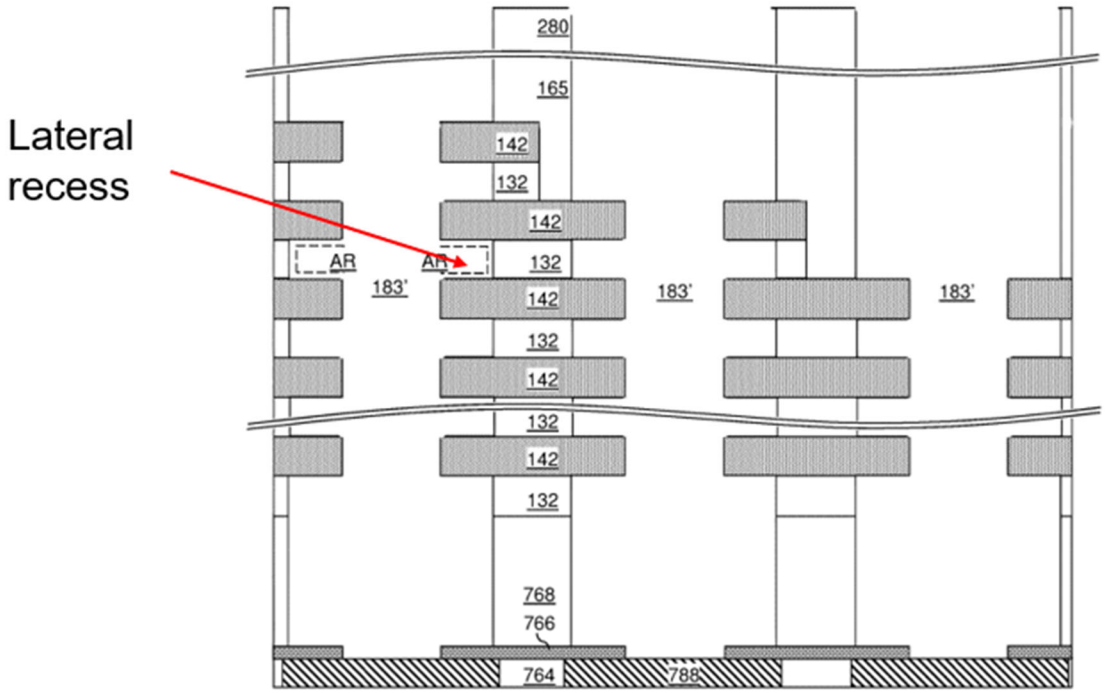


FIG. 16A

Id., Fig. 16A.

167. The ribbed via cavity in Cui creates additional space. In effect, the spacer, or liner, is longer now, because it travels into and out of the lateral recesses. The '254 Patent describes this same purpose of the lateral recesses. Ex. 1001, 13:48-61. Cui refers to these additional regions as "rib regions." Ex. 1031 (Cui), 26:23-32. The dielectric material, i.e., the spacer, will additionally fill these rib regions.

168. Implementing the rib regions provide two fundamental options. First, the rib regions can be made in the sacrificial or conductive gates. Second, the rib regions can be made in the dielectric layers. Both result in the same additional space.

It is only a matter of selecting one of two options. Etching these regions in each layer type was known. Ex. 1031 (Cui), Fig. 16A, 26:23-32 (recesses in dielectric layers); Ex. 1015 (Kai), 11:9-34 (recesses in sacrificial gates).

169. A POSITA would have had a high expectation of success in forming the rib regions. Again, etch chemistries that naturally create small lateral recesses were known. Further, isotropic and selective etches were well known, and selecting an etch chemistry to a certain selectivity was well known. *E.g.*, Ex. 1031 (Cui), 26:33-45; Ex. 1015 (Kai), 11:9-34 (recesses in sacrificial gates).

[7.B] "depositing a dielectric layer filling in the shallow recesses and on the sidewall and a bottom surface of the first opening; and"

170. As I explain under my analysis of claim 5, Fujiki would have been understood to deposit, or at least renders obvious, forming a conformal liner. Thus, the conformal liner would fill the lateral, shallow recesses for the same reasons.

[7.C] "removing part of the dielectric layer that is deposited on the bottom surface of the first opening."

171. For the same reasons that I discuss in claim 5, it would have been obvious to remove the bottom portion, as that is necessary for the TAC to connect to the underlying interconnect.

8. Claim 8:

[8] "The method of claim 7, wherein the removal of the part of the dielectric layer comprises isotropic etching on the sidewall and the bottom surface of the first opening."

172. As I explain below, Fujiki renders this limitation obvious in view of the knowledge of a POSITA.

173. As an initial matter, the '254 Patent recognizes the known conditions when an isotropic etch would be suitable to remove the bottom oxide. Specifically, the '254 patent describes using an isotropic etch because the dielectric material on the bottom will be thinner[5] than on the sidewalls, thereby allowing for a non-directional etch. Ex. 1001, 14:1-19. An isotropic etch is non-directional. Thus, of course, an isotropic etch would only be suitable if there was less oxide on the bottom. Otherwise, the isotropic etch would etch through the sidewall dielectric while removing the bottom portion, and there would not be liner properly insulating the TAC from the conductive gate layers. The conditions for which an isotropic etch is appropriate for removing a target material were well known. That is, when attempting to remove a material from an area (here, oxide on the bottom), there must

[5] I note that in my first declaration addressing this claim there were typographic mistakes in this claim analysis that made "thinner" say "thicker." Because of that, I am discussing different references to illustrate the conditions for which an isotropic etch is appropriate.

be less material on that area relative to the other areas in which the etch chemical will contact (again, an isotropic etch is non-directional, so for a hole, the etch will remove materials on the sidewalls and bottom portion). Thus, when considering whether an isotropic etch is appropriate, the relative thickness of all areas on which the etchant will contact are taken into account. *E.g.*, Ex. 1044 (U.S. Pat. 10,714,341), 1:48-62 ("Furthermore, since the sacrificial material is removed using an isotropic etch process, the use of a thick sacrificial material, which is needed to form a thick metal film on the substrate, will require the formation of a large lateral overhang, since the vertical etch rate of the sacrificial material is the same as lateral etch rate of the sacrificial material."). The appropriate relative thickness, e.g., the bottom dielectric being much thinner than the sidewalls, is what will make the non-directional isotropic etch suitable.

174. The benefits and tradeoffs between isotropic (non-directional) and anisotropic (directional) were textbook material many decades before the filing of the '254 Patent. *E.g.*, Ex. 1042 (Wolf Vol. 1), 32-36 (isotropic and anisotropic etching). For example, isotropic etch does not pose the same potential damage issues as anisotropic etches. *Id.* Of course, an anisotropic etch is directional. Thus, for a conformal liner in which the liner's thickness is substantially uniform, only an anisotropic etch is appropriate.

175. In my analysis of claims [5.PRE-B] and [6], I describe various deposition techniques, e.g., to conformally create a dielectric liner, and in my analysis of claim 3, I describe that timing and etch chemistries can enable forming multiple holes, even of different sizes, at the same time. These basic techniques were all textbook material well before the filing of the '254 Patent. For example, depositing conformal liners was well known. Of course, a deposition may leave less oxide on the bottom. In that case, for the reasons above, it would be obvious to use an isotropic etch.

A POSITA would have had a high expectation of success in employing isotropic etches because these etches were textbook material for many decades before the filing of the '254 Patent. *E.g.*, Ex. 1042 (Wolf Vol. 1), 32-33 (isotropic etching).

9. Claim 9:

[9.PRE] "The method of claim 1, wherein forming the first opening comprises:" [9.A] "simultaneously etching the first opening through the stack, a second opening outside of the stack, and a third opening through the stack,"

176. As I describe below, Fujiki renders these limitations obvious in view of the knowledge of a POSITA.

177. First, my analysis under claim [3] demonstrates that Fujiki would be understood to disclose, or renders obvious, simultaneously etching the hole for the

through-via ("a first opening") and the holes for 82 or 83 contacts (either "a second opening") at the same time.

178. Second, my analysis under claim [2] demonstrates that it would have been obvious to etch dummy holes, including dummy channel holes. My analysis here identifies a dummy hole as a "third hole."

179. Third, for the reasons that I discuss in claim 3, it would have been obvious to etch all these holes at the same time. Again, I explain at length there that simultaneous etching saves considerable processing time. Fabrication time is important in the semiconductor industry. Fabrication facilities (fabs) are highly costly and are typically operated continuously to maximize production. Increasing wafer throughput, and thus die output, is crucial for the commercial success of products, especially for commodity memory chips.

180. For these reasons, it was known to etch many different types of holes at the same time. This includes memory openings (which typically are for both active and dummy channel structures) and contact openings. Kai II, for example, demonstrates this simultaneously etching:

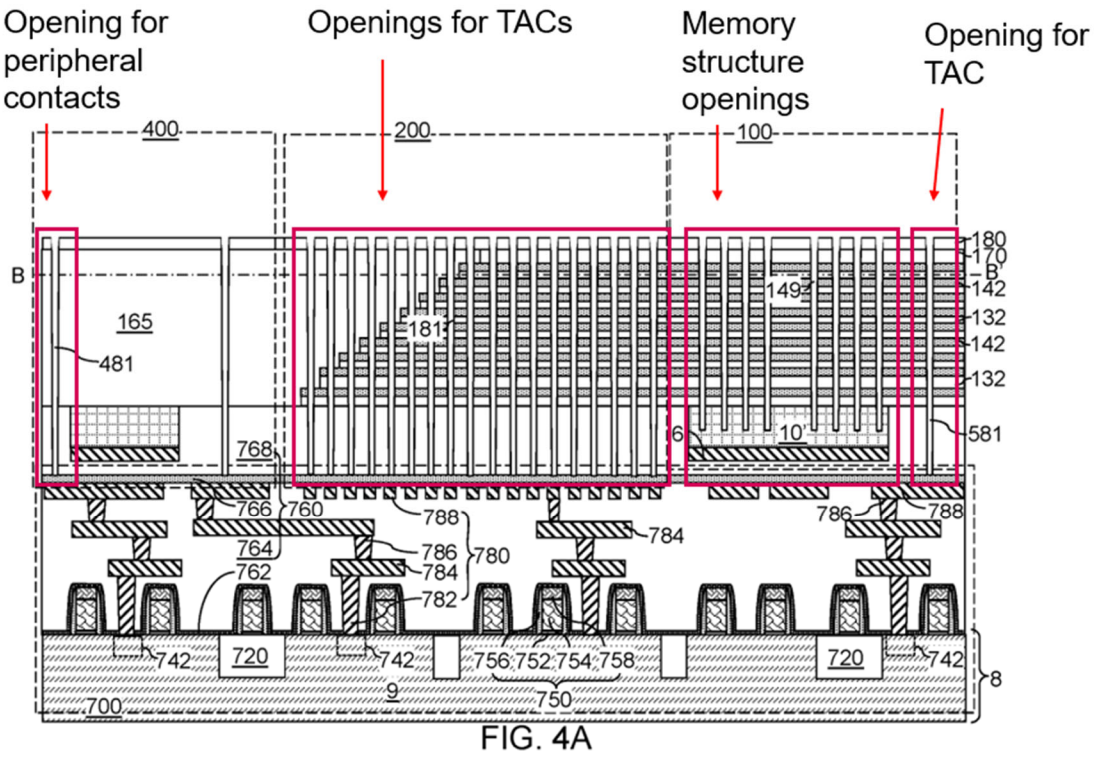


FIG. 4A

Ex. 1038 (Kai II), Fig. 4A, 17:30-44 ("The pattern of openings in the photoresist layer can be transferred through the inter-tier dielectric layer 180 and the first-tier structure (132, 142, 170, 165) and into the in-process source-level material layers 10′ and the at least one second dielectric layer 768 by a first anisotropic etch process to form the various first-tier openings (149, 181, 481, 581) concurrently, i.e., during the first anisotropic etch process. The various first-tier openings (149, 181, 481, 581) can include first-tier memory openings 149, first-tier staircase-region openings 181, first-tier array-region openings 581, and first-tier peripheral-region openings 481.").

181. My analysis under claim 2 demonstrates that it was well known to form both active channel and dummy channel openings at the same time. *E.g.*, Ex. 1015 (Kai), 9:23-26 (defining "support opening" as "a structure in which a support structure (such as a support pillar structure) that mechanically supports other elements is subsequently formed"), 9:45-48 ("support openings 19" extend through stack), 10:20-27 (forming channels in support openings); Ex. 1016 (Park), 6:19-26, 7:45-51 (same); Ex. 1017 (Kim), [0047], [0071], [0072] (same). Thus, Kai II is disclosing forming contacts, memory openings, and dummy memory openings at the same time.

[9.B] "wherein a lateral dimension of the third opening is smaller than lateral dimensions of the first and second openings."

182. As I explain below, Fujiki renders this limitation obvious in view of the knowledge of a POSITA.

183. In general, the lateral dimensions of via structures typically get smaller towards the array. The array contains millions or billions of channel structures and is the densest area. The peripheral is less dense, and the processing does not have to be as precise. And it was well known that larger contacts may exists in the peripheral, providing for example, a lower resistance. In the array portion, given the density, more issues persist, such as creating inadvertent short circuits, support issues, etc. Fujiki conceptually demonstrates this below:

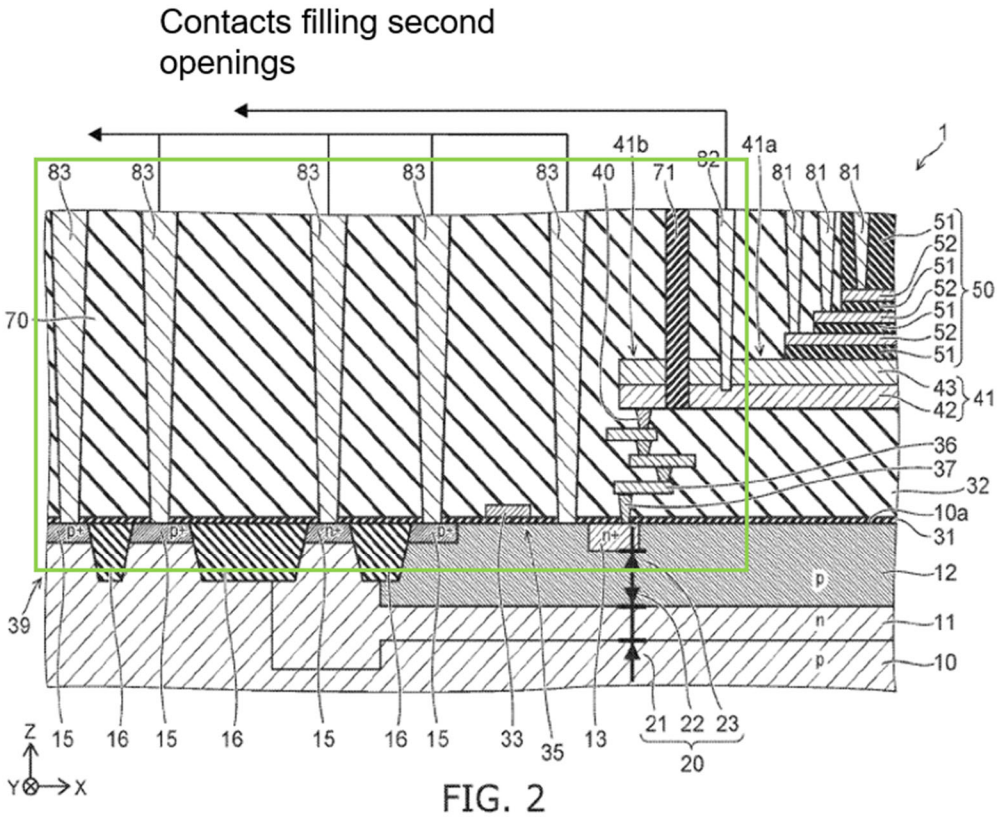


FIG. 2

Ex. 1006 (Fujiki), Fig. 2. Thus, it would have been obvious that the second hole, which is outside of the array in the peripheral, may have the largest lateral dimension, consistent with Fujiki's Figure 2. That said, it was also common to make contacts the same size. Ex. 1043 (Wolf Vol. 2), 47.

184. As to the third hole, however, it would have been obvious that the third hole will have the smallest lateral dimensions. As I explain in my claim [9.A] analysis, the third hole is a dummy hole, e.g., a dummy channel hole. As I describe in my claim [2] analysis, such structures provide a support function. Channel holes

are miniscule in size relative to contacts. For example, below is a top-down view showing channel structures in region 100 versus various contacts:

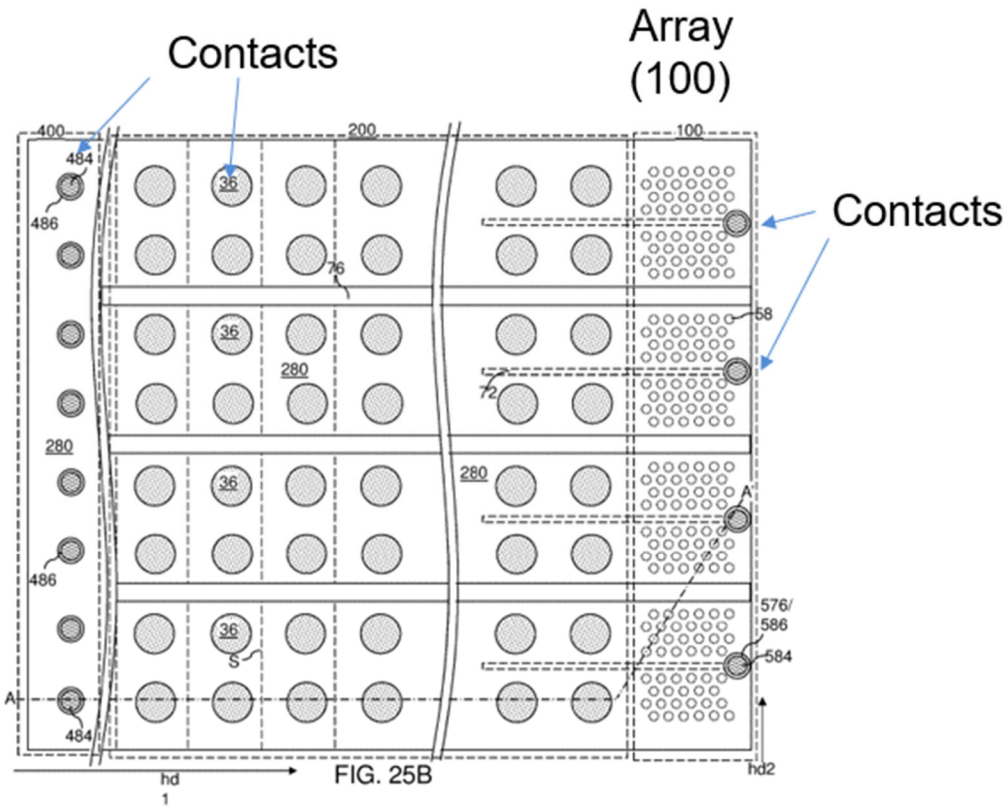


FIG. 25B

Ex. 1031 (Cui), Fig. 25B. Also note the height difference in Figure 2 above. The contacts 83 are longer, and as a natural result of etches that taper (as shown in Figure 2), the lateral width of the top is naturally wider. Note while obviously not to scale, the difference in size of these elements, namely, the channel holes (and channels) and various contact would have been understood to represent the well-known difference in relative size of the many small channels versus the fewer and larger contacts.

10. Claim 10:

[10.PRE] "The method of claim 9, wherein forming the spacer on the sidewall of the first opening comprises:" [10.A] "depositing a dielectric layer (i) fully filling in the third opening to form a dummy channel structure and (ii) partially filling in the first opening and the second opening; and"

185. As I explain below, Fujiki renders this limitation obvious in view of the knowledge of a POSITA.

186. First, my analysis under claim [1.D] demonstrates that Fujiki discloses depositing a dielectric liner in the first opening. As I have also explained, that liner would be understood to be a conformal liner.

187. Second, it would have been obvious to include a liner on Fujiki's peripheral contacts. This was standard for even peripheral contacts. Regardless of location, this enables using the same process, as shown below:

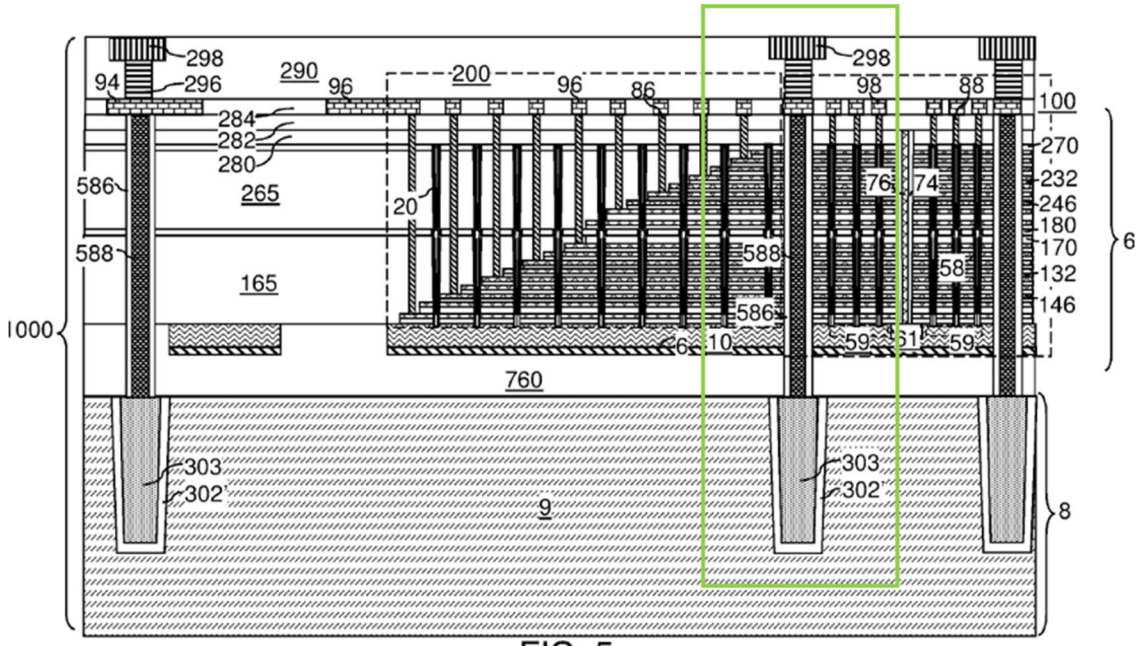


FIG. 5

Ex. 1010 (Mushiga), 10:31-58, Fig. 5 (588). Specifically, the deposition of the liner would extend into these holes because the process would not mask these holes before the deposition of the liner.

188. In addition, Fujiki would not have been understood to depict every element of its 3D NAND. In typical 3D NANDs, contacts, including those outside the memory stack, may need to travel through conductive elements before reaching the target depth, e.g., a local interconnect. For example, as shown below, contacts extend through the substrate to underlying interconnects. Often, the substrate (10) will extend past the stack, as shown below. In these cases, a dielectric liner is necessary, because otherwise after creating the TAC with the conductive core, that

core would physically contact other conductive elements, leading to inadvertent electrical coupling of the TAC and other elements.

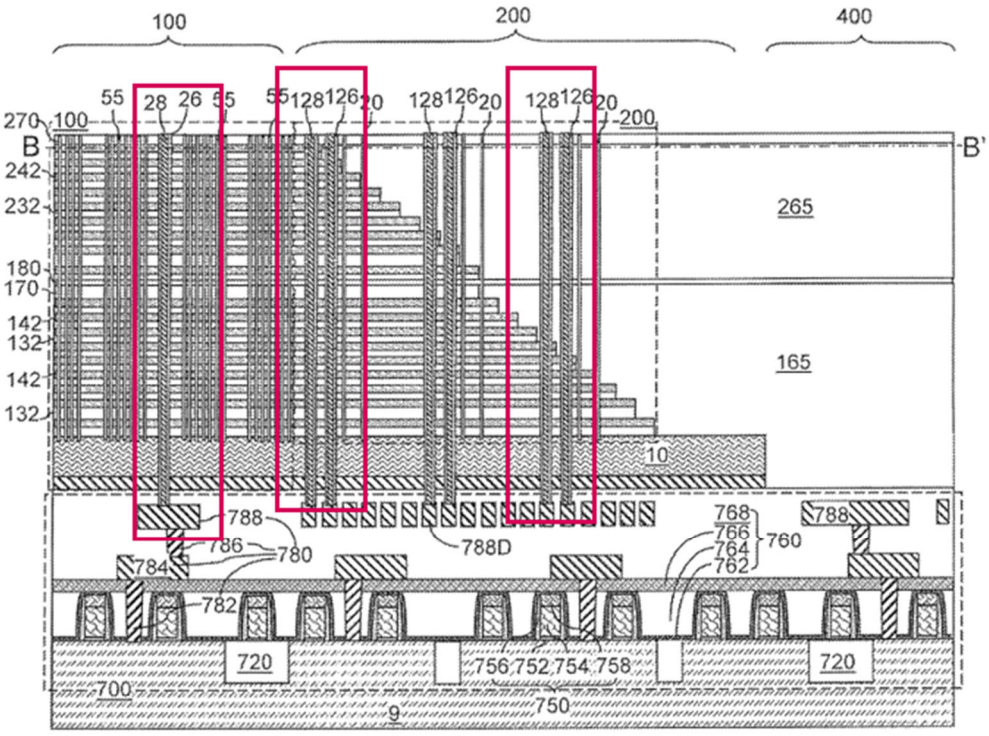


FIG. 8A

Ex. 1019 (U.S. Pat. 10,115,632), Fig. 8A, 17:51-54.

189. Third, I explain why it would be obvious to form dummy holes in my claim [2] analysis, including for a support structure. A common support pillar was a solid dielectric, e.g., oxide, pillar. Ex. 1032 (U.S. Pat. 9,793,139), 15:21-36 ("dielectric support pillar 7P"). The solid, dielectric memory provides additional support during the gate line replacement process. *Id.*

[10.B] "removing parts of the dielectric layer that are deposited on a bottom surface of the first opening and on a bottom surface of the second opening."

190. My analysis in claim [5.B] demonstrates that it would have been obvious to remove the bottom portion of the dielectric liners to create the TACs. This removal enables the TAC to electrically connect to an underlying local interconnect (or other conductive element), as the bottom oxide would otherwise obstruct that connection.

11. Claim 11:

[11.PRE] "A method for forming a three-dimensional (3D) memory device, comprising:"

191. This limitation is identical to claim [1.PRE] and Fujiki discloses it for the same reasons.

[11.A] "forming a stack comprising a plurality of dielectric/sacrificial layer pairs on a substrate;"

192. This limitation is identical to claim [1.A] and Fujiki discloses it for the same reasons.

[11.B] "forming a channel structure extending vertically through the stack;"

193. This limitation is identical to claim [1.B] and Fujiki discloses it for the same reasons.

[11.C] "forming a dummy channel structure extending vertically through the stack;"

194. Fujiki renders obvious forming a dummy channel structure that extends vertically through the stack for the reasons set forth in claim [2].

[11.D] "simultaneously etching a first opening through the stack and a second opening outside of the stack;"

195. This limitation is present in claim [3], and Fujiki discloses it, or renders it obvious, for the same reasons.

[11.E] "simultaneously forming a first spacer on a sidewall of the first opening and a second spacer on a sidewall of the second opening;"

196. My analysis of claims [3]-[4] demonstrates that Fujiki discloses, or renders obvious, forming the through-vias and 82 or 83 contacts at the same time, and thus forming the spacers in the first hole (for the through-via) and second hole (either for contact 82 or 83) at the same time.

197. The analysis under claim [10.PRE-A] demonstrates that it would be obvious to form spacers on both the through-via holes and peripheral contacts 82 or 83 as well. Again, as I explain there, it would be obvious to form the peripheral contacts with spacers because it uses the same process and peripheral contacts often must travel through conductive members to arrive at the local interconnects.

[11.F] "depositing a conductor layer (i) filling in the first opening to form a through array contact (TAC) and (ii) filling in the second opening to form a peripheral contact; and"

198. This limitation is substantively the same as claim [4] (but recites "depositing" instead of "filling," which is an inconsequential difference), and Fujiki discloses it, or renders it obvious, for the same reasons (as shown it completely fills the hole).

199. I also note that Fujiki would have been understood to completely fill the contact hole. Dating back decades, techniques were developed for this very purpose, because a conductive contact should include a solid core that fills the contact hole. In simple terms, this reduces the effective resistance, resulting in better electrical characteristics. Specific techniques, e.g., CVD depositions, are able to achieve this, e.g., with tungsten. *E.g.*, Ex. 1043 (Wolf Vol. 2), 52, 135.

[11.G] "after forming the TAC and peripheral contact, forming a slit extending vertically through the stack."

200. This limitation is substantively the same as claim [1.F] (the above demonstrates it would have been obvious to form all TACs at the same time), and Fujiki discloses it for the same reasons.

12. Claim 12:

[12.PRE] "The method of claim 11, wherein forming the first spacer on the sidewall of the first opening comprises:"

[12.A] "depositing a dielectric layer on the sidewall and a bottom surface of the first opening; and"

[12.B] "removing part of the dielectric layer that is deposited on the bottom surface of the first opening."

201. These limitations are substantively the same as claim [5.PRE-B] ("first spacer" here refers to the TAC through the array of claim 5), and Fujiki discloses them for the same reasons.

13. Claim 13:

[13] "The method of claim 12, wherein the deposition of the dielectric layer comprises atomic layer deposition (ALD), and the removal of the part of the dielectric layer comprises anisotropic etching on the bottom surface of the first opening."

202. This limitation is identical to claim [6], and Fujiki renders it obvious for the same reasons.

14. Claim 14:

[14.PRE]-[14.C]

203. These limitations are effectively identical to claim [7.PRE-7C], and Fujiki renders them obvious for the same reasons. These limitations recite "first" to require that the steps apply to the TAC. Claim 7's steps are on the TAC.

15. Claim 15:

[15] "The method of claim 14, wherein the removal of the part of the dielectric layer comprises isotropic etching on the sidewall and the bottom surface of the first opening."

204. This limitation is identical to claim [8], and Fujiki renders it obvious for the same reasons.

16. Claim 17:

[17] "The method of claim 11, wherein the dielectric layers in the dielectric/sacrificial layer pairs comprise silicon oxide, the sacrificial layers in the dielectric/sacrificial layer pairs comprise silicon nitride, and the first and second spacers comprise silicon oxide."

205. As I explain below, Fujiki renders this limitation obvious in view of the knowledge of a POSITA.

206. Fujiki discloses forming "stacked body 50 … by alternately depositing the insulating films 51 made of silicon oxide and insulative sacrificial films 91 made of silicon nitride (SiN)." Fujiki, [0050].

207. Fujiki also discloses that "[a]n insulating film 79 that is made of, for example, silicon oxide is provided at the periphery of the through-via 78." Fujiki, [0042].

208. My analysis of claims [3]-[4], [10-PRE] demonstrates that Fujiki discloses, or renders obvious, forming the through-vias and 82 or 83 contacts at the same time. Thus, these spacers, like the insulating film 79, would be made of silicon oxide.

17. Claim 18:

[18.PRE] "A method for forming a three-dimensional (3D) memory device, comprising:"

209. This limitation is identical to claim [1.PRE], and Fujiki discloses it for the same reasons.

[18.A] "forming a stack comprising a plurality of dielectric/sacrificial layer pairs on a substrate;"

210. This limitation is identical to claim [1.A], and Fujiki renders it obvious for the same reasons.

[18.B] "forming a channel structure extending vertically through the stack;"

211. This limitation is identical to claim [1.B], and Fujiki renders it obvious for the same reasons.

[18.C] "simultaneously etching a first opening through the stack, a second opening outside of the stack, and a third opening through the stack, wherein a lateral dimension of the third opening is smaller than lateral dimensions of the first and second openings;"

212. This limitation is identical to claim [9.A-B], and Fujiki renders it obvious for the same reasons. Technically, these limitations refer to "a first opening" instead of "the first opening," but refer to the same element.

[18.D] "depositing a dielectric layer (i) fully filling in the third opening to form a dummy channel structure and (ii) partially filling in the first opening and the second opening;"

213. This limitation is identical to claim [10.A], and Fujiki renders it obvious for the same reasons.

[18.E] "removing parts of the dielectric layer that are deposited on a bottom surface of the first opening and on a bottom surface of the second opening;"

This limitation is identical to claim [10.B], and Fujiki renders it obvious for the same reasons.

[18.F] "depositing a conductor layer (i) filling in the first opening to form a through array contact (TAC) and (ii) filling in the second opening to form a peripheral contact; and"

214. This limitation is virtually identical to claim [4], and Fujiki discloses it, or renders it obvious, for the same reasons (again, this claim recites "a conductor layer" instead of "the conductive layer" and recites "filling") (as shown Fujiki completely fills the hole).

[18.G] "after forming the TAC and peripheral contact, forming a slit extending vertically through the stack."

215. This limitation is substantively the same as claim [1.F] but also recites forming the slit after the peripheral contact. As the above illustrates, Fujiki renders obvious forming these contacts at the same time, and thus the claim [1.F] analysis demonstrates that Fujiki discloses it is obvious for the same reasons, because Fujiki discloses forming the slit after the through-via contacts.

18. Claim 20:

[20] "The method of claim 18, further comprising prior to etching the first, second, and third openings, forming a staircase structure at one side of the stack."

216. As I explain below, Fujiki discloses this limitation.

Fujiki discloses forming the staircase before forming the contacts. Fujiki, [0050].

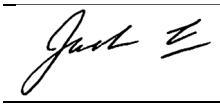
C. Secondary Considerations of Non-Obviousness

217. Based on my review of the '254 Patent's file history, I note that no secondary considerations of non-obviousness were identified in connection with the patent's claims. Nor am I otherwise aware of any evidence of commercial success, skepticism, failure of others, industry praise, unexpected results, or the like relating to the '254 Patent. Instead, as discussed above, it is my opinion that the subject matter embraced by the challenged claims was known in and obvious over the prior art.

218. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willfully false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1101 of Title 18 of the United States Code.

Date: November 7, 2024

Location: Austin TX

Signature: 

DR. JACK C. LEE