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The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is	JP2017 - 247987
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[Document name] Statement
[Name of invention] Semiconductor storage device and manufacturing method thereof
[Technical field]
【0001】
The embodiments relate to a semiconductor storage device and the manufacturing method thereof.
[Background art]
【0002】
In recent years, there have been proposals for stacked semiconductor storage devices that integrate memory cells in three dimensions. In such laminated semiconductor storage devices, in order to make the size even more compact, the furnishing of a thick insulating film between the semiconductor substrate and the memory cell, and the formation of a control circuit within the upper layer portion of the semiconductor substrate and the insulating film have been examined. In this case, a conductive film is furnished on the insulating film and is used as the source line.
[Prior art literature]
[Patent literature]
【0003】
[Patent literature 1] JP 2010-165794
[Patent literature 2] Specification of U.S. Patent Application Publication No. 2011/0073866
[Overview of the invention]
[Problems to be resolved by the invention]
【0004】
The objective of the embodiment is to provide a semiconductor storage device the can be miniaturized and a manufacturing method for this
[Methods of solving the problems]
【0005】
Semiconductor storage device comprises a semiconductor substrate having a diode formed in the upper layer portion thereof, a first insulating film provided on the semiconductor substrate, a first conductive film provided on the aforementioned first insulating film and connected to the aforementioned diode, a laminate provided on the aforementioned first conductive film and in which insulating film and electrode film are alternately stacked, a semiconductor member penetrating the aforementioned stack and connected to the aforementioned conductive film, and a charge storage member provided between the electrode film and the semiconductor member.
【0006】
A manufacturing method for the semiconductor storage device according to the embodiment comprising a step in which a diode is formed in the top layer portion of the semiconductor substrate, a step in which a first insulating film is formed on the semiconductor substrate, a step in which a first conductive film connected to the aforementioned diode is formed on the aforementioned first film, a step in which a laminate is formed by alternatingly forming a first insulating material film and a second insulating material film on the aforementioned first conductive film, a step in which a hole that extends to the aforementioned first conductive film on the aforementioned laminate is formed through reactive ion etching, a step in which a charge storage member is formed on the inner surface of the aforementioned hole, a step in which a semiconductor member connected to the aforementioned first conductive film is formed within the aforementioned hole, and a step in which the aforementioned second insulating material film is replaced with an electrode film after the aforementioned semiconductor member has been formed.
[Brief description of the drawings]
【0007】
[FIG. 1] A cross-sectional view showing a semiconductor storage device according to the first embodiment.
[FIG. 2] A cross-sectional view showing a semiconductor storage device according to the first embodiment.
[FIG. 3] A top view showing a semiconductor storage device according to the first embodiment.
[FIG. 4] A cross-sectional view showing the periphery of a memory cell transistor of a semiconductor storage device according to the first embodiment.
[FIG. 5] A cross-sectional view showing the periphery of a memory cell transistor of a semiconductor storage device according to the first embodiment.
[FIG. 6] A cross-sectional view showing the manufacturing method for a semiconductor storage device according to the first embodiment.
[FIG. 7] A cross-sectional view showing the manufacturing method for a semiconductor storage device according to the first embodiment.

[FIG. 8] A cross-sectional view showing the manufacturing method for a semiconductor storage device according to the first embodiment.

[FIG. 9] A cross-sectional view showing the manufacturing method for a semiconductor storage device according to the first embodiment.

[FIG. 10] A cross-sectional view showing the manufacturing method for a semiconductor storage device according to the first embodiment.

[FIG. 11] A cross-sectional view showing a semiconductor storage device according to the second embodiment.

[FIG. 12] A cross-sectional view showing a semiconductor storage device according to the third embodiment.

[FIG. 13] A cross-sectional view showing the manufacturing method for a semiconductor storage device according to the third embodiment.

[FIG. 14] A cross-sectional view showing the manufacturing method for a semiconductor storage device according to the third embodiment.

[Mode for carrying out the invention]

【0008】

(First embodiment)

The first embodiment is explained below.

FIG. 1 and FIG. 2 are cross-sectional views showing a semiconductor storage device according to this embodiment.

FIG. 3 is a top view showing a semiconductor storage device according to the this embodiment;

FIG. 4 and FIG. 5 are cross-sectional views showing the periphery of a memory cell transistor of a semiconductor storage device according to the first embodiment.

It should be noted that each figure is schematic and has been drawn with exaggerations and omissions as appropriate. For example, each component is depicted smaller and larger than it actually is. In addition, the number of components and dimensional ratios, etc., do not necessarily conform between the figures.

The semiconductor storage device according to this embodiment is a laminated NAND flash memory.

【0009】

As shown in FIG. 1, a silicon substrate 10 is furnished in the semiconductor storage device 1 according to this embodiment. The silicon substrate 10 is formed, for example, by a single crystal silicon (Si).

【0010】

As shown in FIG. 2, for example, the conductive shape of the body portion of the silicon substrate 10 is a p-shape. Then, a portion of the top layer portion of the silicon substrate 10 is formed with an n-shaped well 11. A portion of the upper layer portion of the n-shaped well 11 forms a p-shaped well 12. A portion of the upper layer portion of the p-shaped well 12 forms an n+-shaped diffusion layer 13. The donor concentration of the n+ diffusion layer 13 is higher than the donor concentration of the n-well 11.

【0011】

Diode 21 is formed at the interface between silicon substrate 10 and n-shaped well 11, diode 22 is formed at the interface between p-shaped well 12 and n-shaped well 11, and diode 23 is formed at the interface between p-shaped well 12 and n+-shaped diffusion layer 13. The diode 21, diode 22 and diode 23 are connected in series to form bidirectional diode 20. A portion of the top layer portion of the silicon substrate 10 is formed with one or a plurality of bidirectional diodes 20.

【0012】

A diffusion layer 15 and a Shallow Trench Isolation (STI) 16 are formed in the upper layer portion of the silicon substrate 10. In addition, in the top layer portion of the silicon substrate 10, for example, a source drain layer (not shown) of a metal-oxide-semiconductor field-effect transistor (MOSFET), etc., are also formed.

【0013】

As shown in FIG. 1 and FIG. 2, a gate insulating layer 31 is formed on the silicon substrate 10, and an insulating film 32 is formed thereon. The gate insulating layer 31 and insulating film 32 are formed, for example, by silicon oxide (SiO). The gate insulating layer 31 is formed, for example, by the thermal oxidation of the silicon substrate 10, and the insulating film 32 is formed, for example, by a chemical vapor deposition (CVD) method with TEOS (Tetraethyl orthosilicate: Si(OC2H5)4) used as the main material.

【0014】

Hereinafter in this specification, for convenience of description, an XYZ orthogonal coordinate system is used. The two directions parallel to and orthogonal to the top surface 10a of the silicon substrate 10 are named “X direction” and “Y direction” and the direction perpendicular to the top surface 10a of the silicon substrate 10 is named “Z direction”. In addition, of the Z direction, the direction from the silicon substrate 10 towards the insulating film 32 is also referred to as “up” and the opposite direction is referred to as “down”; this expression is also convenient and is not related to the direction of gravity.

【0015】

A gate electrode 33 is furnished on the gate insulating layer 31 and within the insulating film 32. The source drain layer (not shown), gate insulating layer 31 and gate electrode 33 form a MOSFET 35. Wiring 36 and plug 37 are formed within the insulating film 32. A portion of plug 37 connects the wires 36 to each other, while other parts of plug 37 connects the wires 36 to the diffuser layer 15 of the silicon substrate 10. MOSFET 35, some wiring 36 and some plugs 37 form the control circuitry 39. It should be noted that the control circuitry 39 may include other elements. A plug 40 is furnished on the top row wiring 36 within the insulation film 32.

【0016】

A source electrode film 41 is furnished on the insulating film 32. The shape of the source electrode film 41 is generally flat-plate-shaped, extending along the XY plane and patterned to the predetermined form, as described below. The source electrode film 41 is furnished with a metal layer 42, made of, for example, from tungsten (W), and a silicon layer 43, made of, for example, polycrystalline silicon (Si), is furnished on the metal layer 42. The perimeter of the source electrode film 41 is furnished with an insulating film 44. In addition, the area surrounded by the source electrode film 41 is furnished with an insulating film 45 that passes through the source electrode film 41 in the Z direction.

【0017】

A portion of the lower surface of the source electrode membrane 41 is in contact with the plug 40. Through this, a portion of the source electrode membrane 41 is connected to the top of the plug 40. The bottom of the plug 40 is connected to a portion of the top row wiring 36. This wire 36 is connected to the lower level wire 36 via the plug 37, and a portion of the lower level wire 36 is connected to the upper surface of the n+-shaped diffusion layer 13 via the plug 37. Through this, a portion of the source electrode membrane 41 is connected to one end of the bi-directional diode 20 via the plug 40, a plurality of wires 36, and a plurality of plugs 37. The current path from the source electrode film 41 to the bidirectional diode 20 is isolated from the control circuit 39.

【0018】

A laminate 50 is furnished on the source electrode film 41. In laminate 50, insulating film 51 and electrode film 52 are alternately laminated along the Z direction. The insulating film 51 is made of, for example, silicon oxide, and the electrode film 52 is made of, for example, tungsten. In addition, the shape of the end of the laminate 50 is a stepped shape in which a terrace is formed at each electrode film 52. It should be noted that an air gap may also be formed as an alternative insulator to the insulating film 51.

【0019】

A column 60 is furnished within the laminate 50. The shape of the column 60 is a cylindrical shape in which the center axis extends in the Z direction. A silicon member 61 is furnished at the bottom of the column 60 and a silicon pillar 62 is furnished on the silicon member 61. A memory film 63 is furnished on the periphery of the silicon pillar 62. The silicon pillar 62 is connected to the silicon member 61, and the silicon member 61 is connected to the source electrode film 41.

【0020】

As shown in FIG. 4 and FIG. 5, a core member 64 made from silicon oxide is furnished within the silicon pillar 62. In memory film 63, tunnel insulating film 65, charge storage film 66, and silicon oxide layer 67 are furnished in this order from the inside, that is, from the silicon pillar 62 side to the outside. On the other hand, an aluminum oxide layer 68 is furnished on the upper surface and the lower surface of the electrode film 52, as well as on the side opposite the silicon pillar 62. The silicon oxide layer 67 and the aluminum oxide layer 68 comprise a block insulating film 69.

【0021】

Tunnel insulating film 65 is normally insulating, but allows tunnel current to flow when the predetermined voltage within the driving voltage range of semiconductor storage device 1 is applied, and is, for example, a single layer of silicon oxide film, or an ONO film in which a silicon oxide layer, a silicon nitride layer, and a silicon oxide layer are laminated in this order. The charge storage film 66 is a film capable of storing charge, and is made of a material that includes an electron trap site, such as silicon nitride, for example. The block insulating film 69 is a film that does not substantially allow current to flow even when a voltage is applied within the range of the driving voltage of the semiconductor storage device 1.

【0022】

The tunnel insulation film 65, charge storage film 66, and block insulation film 69 form the memory film 63. Memory film 63 is disposed between silicon pillar 62 and electrode film 52. Silicon member 61, silicon pillar 62, memory film 63, and core member 64 form column 60. The silicon pillar 62 is insulated from the electrode film 52 by memory film 63. The silicon member 61 is also insulated from the electrode film 52 by an insulating film (not shown).

【0023】

As shown in FIG. 1 to FIG. 3, an insulating film 70, made from, for example, silicon oxide, is furnished around the laminate 50 on the source electrode film 41 and insulating film 44. An insulating plate 71 is furnished to circumscribe the laminate 50 within insulating film 70. The insulating plate 71 is spaced apart from the laminate 50. The insulating plate 71 penetrates the source electrode film 41 and extends to the insulating film 32. In addition, a plurality of insulating plates 72 extending in the X direction are furnished within the laminate 50. The insulating plate 72 penetrates the insulating film 51 and electrode film 52 in the laminate 50 and extends to the source electrode film 41. Each of the laminates 50 space apart in the Y direction by the insulating plate 72 form a block that is, for example, the smallest unit of data erasure. The insulating plates 71 and 72 are formed, for example, from silicon oxide. It should be noted that the insulating plate 71 and the insulating plate 72 may be connected to each other. In addition, the shape of the insulating plate 71 may be framed such that it surrounds the laminate 50 looking from the Z direction. However, in this case as well, the insulating plate 71 is spaced apart from the laminate 50.

【0024】

By the insulating plate 71, the source electrode film 41 is divided into a central portion 41a disposed inside the insulating plate 71 and a peripheral portion 41b disposed outside the insulating plate 71. The central portion 41a and the peripheral portion 41b are insulated from each other by insulating plate 71. In other words, the lower portion of the insulating plate 71 is disposed between the central portion 41a and the peripheral portion 41b. The central portion 41a is connected to the silicon pillar 62 via the silicon member 61. The peripheral portion 41b is connected to the bi-directional diode 20 via plug 40, wiring 36 and plug 37.

【0025】

A bit line 75 extending in the Y direction is furnished on the laminate 50 and on insulating film 70. Bit line 75 is connected to the top of silicon pillar 62. An insulating film 76 is furnished on the laminate 50 and on insulating film 70 so that it covers bit line 75. A plug 77 is furnished within the insulating film 76. Between the wiring 36 and the plug 77 of the control circuit 39, a piercing via 78 extending in the Z direction is furnished so as to penetrate the insulating film 45 surrounded by laminate 50 and source electrode film 41. The periphery of the piercing via 78 is furnished with an insulating film 79, made from, for example, silicon oxide. The piercing via 78 is insulated from the electrode film 52 and source electrode film 41 by insulating film 79. A top layer wire 80 is furnished on plug 77, and is connected to the plug 77.

【0026】

As shown in FIG. 2 and FIG. 3, contacts 81-83 are furnished within the insulating film 70. The bottom of the contact 81 is connected to the electrode film 52, and the top is connected to a portion of the upper layer wiring (not shown). The bottom of the contact 82 is connected to the source electrode membrane 41, and the top is connected to another portion of the upper layer wiring (not shown). The bottom of the contact 83 is connected to the diffusion layer 15, etc., of the silicon substrate 10, and the top is connected to another portion of the upper layer wiring (not shown).

【0027】

In the semiconductor storage device 1 according to this embodiment, a memory cell 59 is formed for each intersection between electrode film 52 and silicon pillar 62. The channel of the memory cell 59 is a silicon pillar 62, the gate insulating film is a tunnel insulating film 65 and a block insulating film 69, the gate is an electrode film 52, and the charge storage member is a charge storage film 66. Then, the control circuit 39 controls the potentials of the source electrode film 41, the bit line 75, and each electrode film 52 to inject charge from the silicon pillar 62 into the charge storage film 66 or to discharge charge from the charge storage film 66 to the silicon pillar 62. Through this, the threshold voltage of the memory cell 59 is changed and the data is stored.

【0028】

Next, an explanation is given on the method of manufacturing a semiconductor storage device according to this embodiment.

FIG. 6 to FIG. 10 are cross-sectional views illustrating a method of manufacturing a semiconductor storage device according to this embodiment.

【0029】

First, as shown in FIG. 6 and FIG. 2, an n-shaped well 11, a p-shaped well 12, an n+-shaped diffusion layer 13, a diffusion layer 15, and an STI 16, etc., are formed in the upper layer portion of the silicon substrate 10. Through this, a bi-directional diode 20 is formed in a portion of the top layer portion of the silicon substrate 10.

【0030】

Next, the thermal oxidation treatment forms a gate insulating layer 31 on the top surface 10a of the silicon substrate 10. The CVD method, made from TEOS, for example, is then repeated to form an insulating film 32 while forming gate electrode 33, plug 37, wire 36 and plug 40. Through this, control circuit 39 is formed in the top layer portion of the silicon substrate 10 and the insulating film 32. At this time, the plug 40 is connected to the n+-shaped diffusion layer 13 via some plugs 37 and some wiring 36.

【0031】

Next, the metal layer 42 is formed on the insulating film 32 and the silicon layer 43 is deposited thereon to form the source electrode film 41. Next, the source electrode film 41 is patterned to form an insulating film 44 around the source electrode film 41 and to form an insulating film 45 in the area surrounded by the source electrode film 41.

【0032】

Next, the insulative sacrificial layer 91 made from silicon oxide and silicon nitride (SiN) is then alternately deposited on the source electrode film 41, insulating film 44 and insulating film 45, to form laminate 50. It should be noted that the material of the sacrificial layer 91 is not limited to silicon nitride, and may be any insulative material that has an etch selectivity ratio with respect to insulating film 51. Next, the ends of the laminate 50 are then processed in a stepwise manner in which a terrace is formed for each sacrificial layer 91. Next, the deposition of silicon oxide results in insulating film 70 being formed around the laminate 50.

【0033】

Next, the mask pattern 92 is formed on the laminate 50 and on the insulating film 70, as shown in FIG. 7. The mask pattern 92 is then used as a mask to perform Reactive Ion Etching (RIE). Specifically, the etching gas is turned to plasma in order to convert the etch species into positive ions, an electric field is applied to accelerate the positive ions, and which are then made to selectively collide with the laminate 50 via the mask pattern 92. Through this, a memory hole 93 is formed in the laminate 50. At this time, the laminate 50 is formed from an insulative material, in other words, silicon oxide and silicon nitride, so that the positive charge derived from the positive ions of the etch species is accumulated within the memory hole 93. On the other hand, a negative charge is accumulated on the outer surface of the intermediate structure at this stage. It should be noted that in FIG. 7, the positive charge is represented by a symbol circled with "+", and the negative charge is represented by a symbol circled with "-".

【0034】

Then, as shown in FIG. 8, when the memory hole 93 reaches the source electrode film 41, the positive charge accumulated within the memory hole 93 moves to the source electrode film 41 and further flows into the n+ -shaped diffusion layer 13 via the plug 40, wiring 36, plug 37, as shown in FIG. 8 as path E. Through this, the diodes 23 and 21 of the bi-directional diode 20 are caused to yield, and a positive charge flows into the silicon substrate 10 via the bi-directional diode 20 and is discharged externally via the silicon substrate 10. As a result of this, arching in the insulating film 32 can be prevented.

【0035】

Next, as shown in FIG. 9, FIG. 4, and FIG. 5, within the lower portion of the memory hole 93, the silicon member 61 is formed through the epitaxial growth of silicon from the silicon layer 43. Next, the silicon oxide layer 67, charge storage film 66, tunnel insulating film 65, silicon pillar 62, and core member 64 are then formed on the inner surface of memory hole 93 on silicon member 61. The silicon pillar 62 is connected to the source electrode film 41 via the silicon member 61. Next, the piercing via hole 94 is formed so as to penetrate the top of the laminate 50, insulating film 45, and insulating film 32, reaching a portion of the wiring 36. Next, the insulating film 79 is formed on the inner surface of the piercing via hole 94, and the piercing via 78 is formed on the inner surface of the insulating film 79. The piercing via 78 is connected to the wiring 36.

【0036】

Next, as shown in FIG. 10 and FIG. 3, slit 95 is formed so as to penetrate insulating film 70 and source electrode film 41, and slit 96 is formed so as to penetrate laminate 50. The slit 95 divides the source electrode membrane 41 into a central portion 41a and a peripheral portion 41b. As the plug 40 is connected only to the peripheral portion 41b, this split isolates the central portion 41a from the silicon substrate 10. Next, wet etching is performed via slit 96 to remove sacrificial layer 91 (refer to FIG. 9). As a result of this, a space 97 is formed after the sacrificial layer 91 has been removed.

【0037】

Next, the aluminum oxide layer 68 is formed on the inner surface of the space 97 via slit 96, as shown in FIG. 1, FIG. 4 and FIG. 5. Aluminum oxide layer 68 comes into contact with silicon oxide layer 67 and forms block insulating film 69 together with silicon oxide layer 67. The tunnel insulation film 65, charge storage film 66, and block insulation film 69 form the memory film 63. Next, a barrier metal layer (not shown) is formed on the inner surface of space 97 via slit 96, after which a conductive material such as tungsten is embedded in space 97 to form the electrode film 52. Next, the performance of etching removes the portion of the electrode film 52 and aluminum oxide layer 68 formed in slit 95 and slit 96. Next, by embedding silicon oxide in slit 95 and slit 96, an insulating plate 71 is formed within slit 95, and an insulating plate 72 (refer to FIG. 3) is formed within slit 96.

【0038】

Next, as shown in FIG. 1, a bit line 75 extending in the Y direction is formed on the laminate 50 and on the insulating film 70, and is connected to the silicon pillar 62. In addition, an insulating film 76 is formed on the laminate 50 and on the insulating film 70, and a plug 77 and upper layer wiring 80 are formed within the insulating film 76. The upper layer wiring 80 connects to the piercing via 78 via plug 77. Semiconductor storage device 1 according to this embodiment is manufactured in this way.

【0039】

Next, the effects of this embodiment will be explained.

In this embodiment, as shown in FIG. 6, a bi-directional diode 20 is formed in the upper layer portion of the silicon substrate 10. In addition, when the source electrode film 41 is formed on the insulating film 32, the source electrode film 41 is connected to the bi-directional diode 20 via the plug 40, wiring 36, and plug 37. Through this, the bi-directional diode 20 is caused to yield due to the positive charge accumulated in the memory hole 93 when the memory hole 93 reaches the source electrode film 41, as shown in FIG. 8, which flows to the silicon substrate 10 via the source electrode film 41, plug 40, wiring 36, plug 37, n+-shaped diffusion layer 13, p-shaped well 12 and n-shaped well 11, and is discharged externally. Through this, arcing in the insulating film 32 is prevented, and the breaking of insulating film 32 can be avoided.

【0040】

In addition, as shown in FIG. 10, through the formation of slit 95, the source electrode membrane 41 is divided into the central portion 41a and the peripheral portion 41b. As a result of this, in the completed semiconductor storage device 1 shown in FIG. 1, the central portion 41a of the source electrode film 41 to which the silicon pillar 62 is connected can be reliably insulated from the silicon substrate 10, while at the same time, the stray capacity of the source electrode film 41 is reduced. As a result of this, the operation of the semiconductor storage device 1 is stabilized and accelerated.

【0041】

(Second embodiment)

Next, an explanation is given on the second embodiment.

FIG. 11 is a cross-sectional view showing a semiconductor storage device according to this embodiment.

【0042】

As shown in FIG. 11, the semiconductor storage device 2 according to this embodiment differs from the semiconductor storage device 1 according to the first embodiment described above (refer to FIG. 1 to FIG. 5) in that the insulating plate 71 is not provided. It should be noted that an insulating plate 72 (refer to Fig. 3) is also furnished in the semiconductor storage device 2.

【0043】

The semiconductor storage device 2 can be manufactured by forming only slits 96 (refer to FIG. 3) and not slit 95 in the steps shown in FIG. 10.

【0044】

In the same manner as the first embodiment described above, this embodiment also results in the positive charge accumulated in the memory hole 93 (refer to FIG. 7) flowing to the bi-directional diode 20 via the source electrode membrane 41, plug 40, wiring 36 and plug 37, causing the bi-directional diode 20 to yield and discharge externally via the silicon substrate 10. As a result of this, the destruction of insulating film 32 can be avoided.

【0045】

In addition, in the semiconductor storage device 2 according to this embodiment, the source electrode film 41 is not split by the insulating plate 71 (refer to FIG. 1 and FIG. 3), however, as a bi-directional diode 20 is interposed between the source electrode film 41 and the silicon substrate 10, the source electrode film 41 can be driven electrically independent from the silicon substrate 10 within the predetermined potential difference.

The other configurations, manufacturing methods and effects in this embodiment are similar to those of the first embodiment described above.

【0046】

(Third embodiment)

Next, an explanation is given on the third embodiment.

FIG. 12 is a cross-sectional view showing a semiconductor storage device according to this embodiment.

【0047】

As shown in FIG. 12, in the semiconductor storage device 3 according to this embodiment, in addition to the configuration of the semiconductor storage device 1 according to the first embodiment described above (refer to FIG. 1 to FIG. 5), a silicon film 54, an insulating film 55, and a plug 56 made of conductive polysilicon are furnished. In addition, the source electrode film 41 is not split by the insulating plate 71, but the silicon film 54 is split. Furthermore, there is no silicon member 61 (refer to FIG. 1), and the silicon pillar 62 is directly connected to the source electrode film 41.

【0048】

A detailed explanation is provided below.

The silicon film 54 is disposed between the source electrode film 41 and the laminate 50, the shape of which is generally a flat plate-shape that extends along the XY plane. The insulating film 55 is disposed between the source electrode film 41 and the silicon film 54. The plug 56 extends through the insulating film 55 and the silicon layer 43 of the source electrode film 41, the bottom of which is in contact with the metal layer 42 of the source electrode film 41, and the top of which is in contact with the silicon film 54. Through this, a portion of the silicon film 54 is connected to the source electrode film 41 via the plug 56. Similarly to the first embodiment, the source electrode membrane 41 is connected to the bi-directional diode 20 via the plug 40. Accordingly, a portion of the silicon film 54 is connected to the bi-directional diode 20 formed in a portion of the top layer portion of the silicon substrate 10. The current path from the silicon film 54 to the bi-directional diode 20 is isolated from the control circuit 39. The insulating film 44 is furnished around a laminate made from source electrode film 41, insulating film 55, and silicon film 54. Insulation

film 45 penetrates this laminate in the Z direction.

【0049】

In addition, the insulating plate 71 and the insulating plate 72 (refer to FIG. 3) penetrate the silicon film 54 in the Z direction, but the source electrode film 41 does not penetrate. Therefore, the insulating plate 71 splits the silicon film 54 into the central portion 54a and the peripheral portion 54b, but does not split the source electrode film 41. The plug 56 is connected to the peripheral portion 54b of the silicon film 54. In addition, similarly to the first embodiment described above, the insulating plate 72 which splits the laminate 50 into a plurality of blocks in the Y direction is interconnected with the insulating plate 71, which together penetrates the silicon film 54, for example, so as to separate the central portion 54a of the silicon film 54 located below the laminate 50 between the plurality of blocks aligned in the Y direction.

【0050】

In the column 60, the silicon member 61 is not furnished, and the bottom of the silicon pillar 62 is in contact with the source electrode membrane 41. The silicon pillar 62 runs through the central portion 54a of the silicon film 54 and is insulated from the silicon film 54 by the memory film 63, excluding the aluminum oxide layer 68. The central portion 54a of the silicon film 54 serves as a selection gate for switching the continuity/non-continuity of the lowest stage gate electrode, for example, the silicon pillar 62, for each block relative to the silicon pillar 62.

【0051】

Next, an explanation is given on the method of manufacturing a semiconductor storage device according to this embodiment.

FIG. 13 and FIG. 14 are cross-sectional views illustrating a method of manufacturing a semiconductor storage device according to this embodiment.

【0052】

First, as shown in FIG. 13, a structure is created for the portion from the silicon substrate 10 to the source electrode membrane 41 by a method similar to the first embodiment described above.

【0053】

Next, the insulating film 55 is formed on the source electrode film 41, and the plug 56 is formed within the insulating film 55 and silicon layer 43 of the source electrode film 41 to form a silicon film 54 thereon. Next, the silicon film 54 and the insulating film 55 are patterned to form the insulating film 44 around the laminate consisting of source electrode film 41, silicon film 54 and insulating film 55, and to form the insulating film 45 in the area that is surrounded by the laminate.

【0054】

Next, the sacrificial layer 91 consisting of a silicon oxide and a silicon nitride is then alternately deposited on the silicon film 54 to form laminate 50. Next, the insulating film 70 is formed around the laminate 50. Next, the mask pattern 92 is formed on the laminate 50 and on the insulating film 70. Next, RIE is performed in which the mask pattern 92 is used as a mask, and the silicon film 54 is used as an etch stopper to form a memory hole 93 in the laminate 50. The conditions of the RIE shall be such that the silicon oxide and silicon nitride are etched efficiently. At this time, similarly to the first embodiment, the positive charge is stored within the memory hole 93.

【0055】

Then, when the memory hole 93 reaches the silicon film 54, the etch rate is decreased. This brings it into alignment with the bottom of the memory hole 93. At this time, the positive charge accumulated in the memory hole 93 is moved to the silicon film 54. Then, as shown in path E, it is moved to source electrode membrane 41 via plug 56, then moved to n+-shaped diffusion layer 13 via plug 40, wiring 36 and plug 37, causing bi-directional diode 20 to yield and movement to silicon substrate 10. It is then discharged externally via the silicon substrate 10. Through this, arcing in insulating film 55 and insulating film 32 can be prevented.

【0056】

Next, as shown in FIG. 14, the RIE is continued by changing the conditions of the RIE to such that the silicon is etched efficiently. Through this, the memory hole 93 is caused to reach the insulating film 55. Next, the RIE conditions are changed to such that the silicon oxide is etched efficiently, and the RIE is continued. This causes the memory hole 93 to reach the silicon layer 43 of the source electrode membrane 41. The RIE ends here.

【0057】

Next, silicon oxide layer 67, charge storage film 66, tunnel insulating film 65, silicon pillar 62, and core member 64 are formed on the inner surface of memory hole 93, as shown in FIG. 12, FIG. 4, and FIG. 5. The silicon pillar 62 is connected to the silicon layer 43. The insulating film 79 and piercing via 78 are then formed.

【0058】

Next, as shown in FIG. 12 and FIG. 3, the insulating film 70, the laminate 50 and the below these are etched to form slits 95 and 96 at a generally even depth while the silicon film 54 is used as an etch stopper. Slits 95 and 96 can be formed simultaneously by, for example, etching one mask pattern with a mask. At this time, slits 95 and 96 penetrate silicon film 54 but do not penetrate source electrode film 41. This causes the silicon film 54 to be split into a central portion 54a and a peripheral portion 54b by slit 95. As the silicon pillar 62 is surrounded by the central portion 54a and the plug 56 is connected only to the peripheral portion 54b, the central portion 54a of the silicon film 54 that serves as the lowest gate electrode can be isolated from the source electrode film 41 by splitting the silicon film 54. The following manufacturing method is similar to the first embodiment described above.

【0059】

Next, the effects of this embodiment will be explained.

In this embodiment as well, similarly to the first embodiment described above, a bidirectional diode 20 is formed in the upper layer portion of the silicon substrate 10 and the source electrode membrane 41 is connected to the bidirectional diode 20 via plug 40, wiring 36 and plug 37. In addition, the silicon film 54 is connected to the source electrode film 41 via plug 56. Through this, as shown in FIG. 13, the bi-directional diode 20 is caused to yield when the memory hole 93 reaches the silicon film 54, and the positive charge accumulated within the memory hole 93 is caused to flow to and out of the silicon substrate 10 via the silicon film 54, plug 56, source electrode film 41, plug 40, wiring 36, plug 37, n+-shaped diffusion layer 13, p-shaped well 12 and n-shaped well 11. Through this, arcing in the insulating film 55 and in the insulating film 32 is prevented, and the destruction of the insulating film 55 and the insulating film 32 can be avoided.

【0060】

In addition, as shown in FIG. 12, through the formation of slit 95, the silicon film 54 is divided into the central portion 54a and the peripheral portion 54b. As a result of this, in the completed semiconductor storage device 3, the central portion 54a that functions as the lowest gate electrode relative to the silicon pillar 62 can be reliably insulated from the source electrode film 41. This allows for the central portion 54a and the source electrode membrane 41 to be driven electrically and independently. In addition, the stray capacity of the central portion 54a is reduced.

【0061】

Furthermore, as the bidirectional diode 20 is interposed between source electrode film 41 and silicon substrate 10, source electrode film 41 can be driven electrically and independent of silicon substrate 10 within the predetermined potential difference.

The other configurations, manufacturing methods and effects in this embodiment are similar to those of the first embodiment described above.

【0062】

According to the embodiments explained above, a semiconductor storage device capable of being made more compact and a method of manufacturing such a device can be realized.

【0063】

While a few of the embodiments of the invention have been described above, these embodiments are presented by way of example and are not intended to limit the scope of the invention. These novel embodiments can be implemented in various other forms and may be omitted, replaced, or modified in various ways to the extent that they there is no deviation from the summary of the invention. These embodiments and variations thereof are included in the scope and abstract of the invention, as well as in the scope of the inventions and equivalents thereof stated in the claims.

[Description of reference symbols]

【0064】

1, 2 and 3: Semiconductor storage device
10：Silicon substrate
10a：Top surface
11：n-shaped well
12：p-shaped well
13：n^+-shaped diffusion layer
15：Diffusion layer
16：STI
20：Bidirectional Diode
21, 22 and 23: Diodes
31：Gate insulating layer
32：Insulation film
33：Gate electrode
36：Wiring
37：Plug
39：Control circuit
40：Plug
41：Source electrode film
41a：Central portion
41b：Surrounding portion
42：Metal layer
43：Silicone layer
44 and 45: Insulation film
50：Laminate
51：Insulation film
52：Electrode film
54：Silicon film
54a：Central portion
54b：Surrounding portion
55：Insulation film
56：Plug
59：Memory cell
60：Column
61：Silicon member
62：Silicon pillar
63：Memory film
64：Core member
65：Tunnel insulation film
66：Charge storage film

67 : Silicon oxide layer
68 : Aluminum oxide layer
69 : Block insulating film
70 : Insulation film
71, 72: Insulating plates
75 : Bit line
76 : Insulation film
77 : Plug
78 : Pierce via
79 : Insulation film
80 : Upper layer wiring
81, 82 and 83: Contacts
91 : Sacrificial layer
92 : Mask pattern
93 : Memory hole
94 : Pierce via hole
95, 96: Slits
97 : Space
E : Path

[Document name] Scope of claims

[Claim 1]

A semiconductor storage device comprising a semiconductor substrate having a diode formed in the top layer;

a first insulating film provided on the aforementioned semiconductor substrate;

a first conductive film disposed on the aforementioned first insulating film and connected to the aforementioned diode;

a laminate provided on the aforementioned first conductive film, with the laminate being formed by alternately laminating insulators and electrode films;

a semiconductor member that penetrates the aforementioned laminate and which is connected to the aforementioned first conductive film;

a charge storage member disposed between the aforementioned electrode film and the aforementioned semiconductor member.

[Claim 2]

The semiconductor storage device described in Claim 1 further comprising a first plug connected between the aforementioned diode and the aforementioned first conductive film;

the aforementioned first conductive film

having a first portion connected to the aforementioned semiconductor member;

a second portion connected to the aforementioned second plug and insulated

from the aforementioned first portion.

[Claim 3]

The semiconductor storage device described in Claim 1 further comprising a second conductive film disposed between the aforementioned first conductive film and the aforementioned laminate;

a second insulating film disposed between the aforementioned first conductive film and the aforementioned second conductive film;

a first plug connected between the aforementioned diode and the aforementioned first conductive film;

a second plug connected between the aforementioned first conductive film and the aforementioned second conductive film;

the aforementioned second conductive film

having a first portion surrounding the aforementioned semiconductor member;

a second portion connected to the aforementioned second plug and insulated

from the aforementioned first portion.

[Claim 4]

A manufacturing method for a semiconductor storage device comprising a step in which a diode is formed in the top layer of a semiconductor substrate;

a process in which a first insulating film is formed on the aforementioned semiconductor substrate;

a process in which a first conductive film connected to the aforementioned diode is formed on the first insulating film;

a process in which a laminate is formed by alternately forming a first insulating material film and a second insulating material film on the aforementioned first conductive film;

a process in which a hole that extends to the aforementioned first conductive film in the aforementioned laminate is formed through reactive ion etching;

a process in which a charge storage member is formed on the inner surface of the aforementioned hole;

a process in which a semiconductor member connected to the aforementioned first conductive film is formed within the aforementioned hole in which the aforementioned charge storage member is formed;

and a process in which the aforementioned second insulating material film is replaced with an electrode film after the aforementioned semiconductor member has been formed.

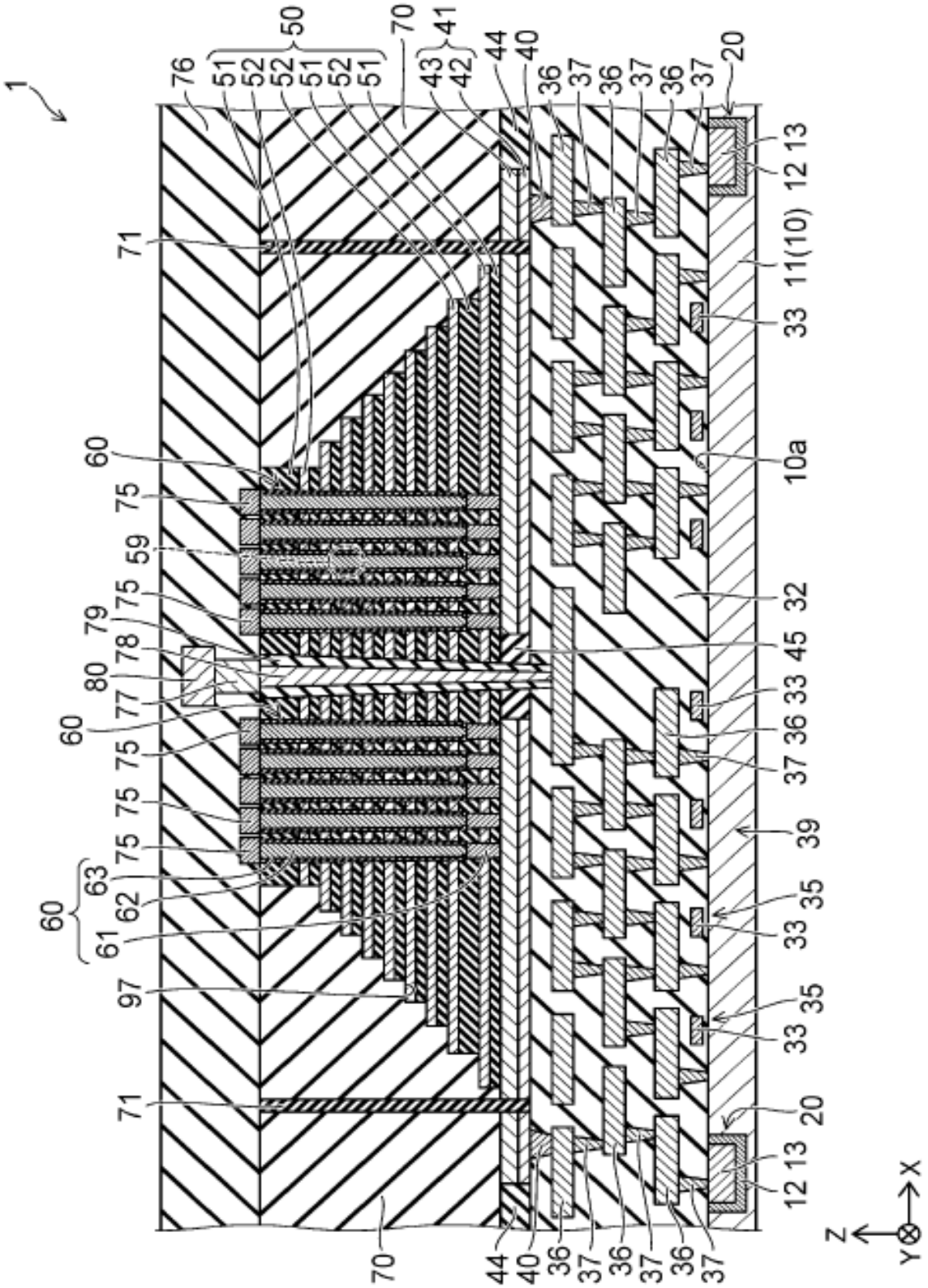
[Claim 5]

A manufacturing method for the semiconductor storage device described in Claim 4, wherein the step in which the aforementioned first insulating film is formed comprises a step in which a plug connected between the aforementioned diode and the aforementioned first conductive film is formed within the aforementioned first insulating film;

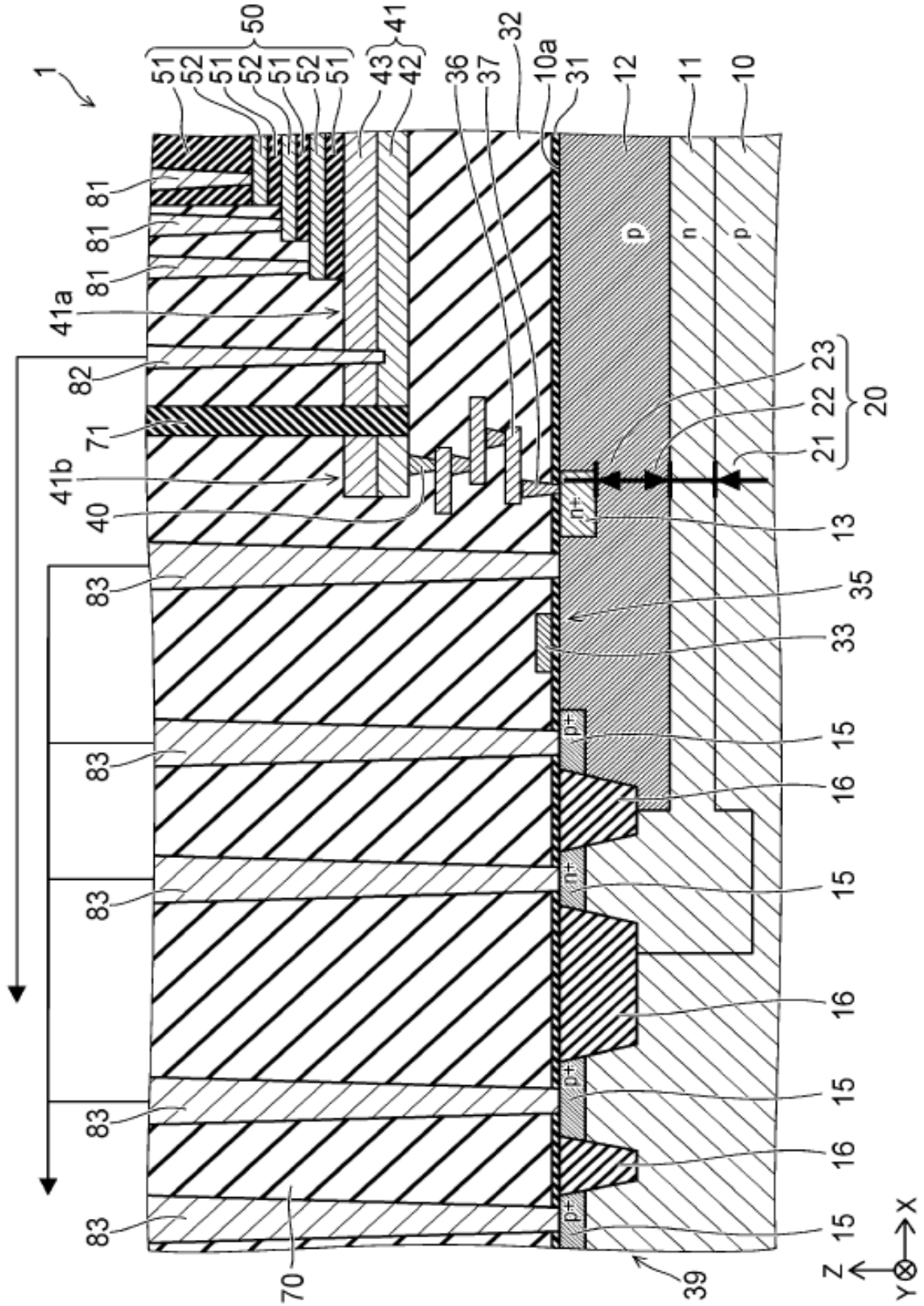
a step of dividing the aforementioned first conductive film into a first portion connected to the aforementioned semiconductor member and a second portion connected to the aforementioned plug after the aforementioned hole has been formed.

[Document name] Summary
[Summary]
[Problem] To provide a semiconductor storage device that can be miniaturized and a manufacturing method for this.
[Means of Solving the Problem] Semiconductor storage device 1 comprises a semiconductor substrate 10 having a diode 20 formed in the upper layer portion thereof, a first insulating film 32 provided on the semiconductor substrate 10, a conductive film 41 provided on the aforementioned first insulating film 32 and connected to the aforementioned diode 20, a stack 50 provided on the aforementioned conductive film 41 and in which insulating film 51 and electrode film 52 are alternately stacked, a semiconductor member 62 penetrating the aforementioned stack 50 and connected to the aforementioned conductive film 41, and a charge storage member 66 provided between the electrode film 52 and the semiconductor member 62.
[Selected drawing] FIG. 2

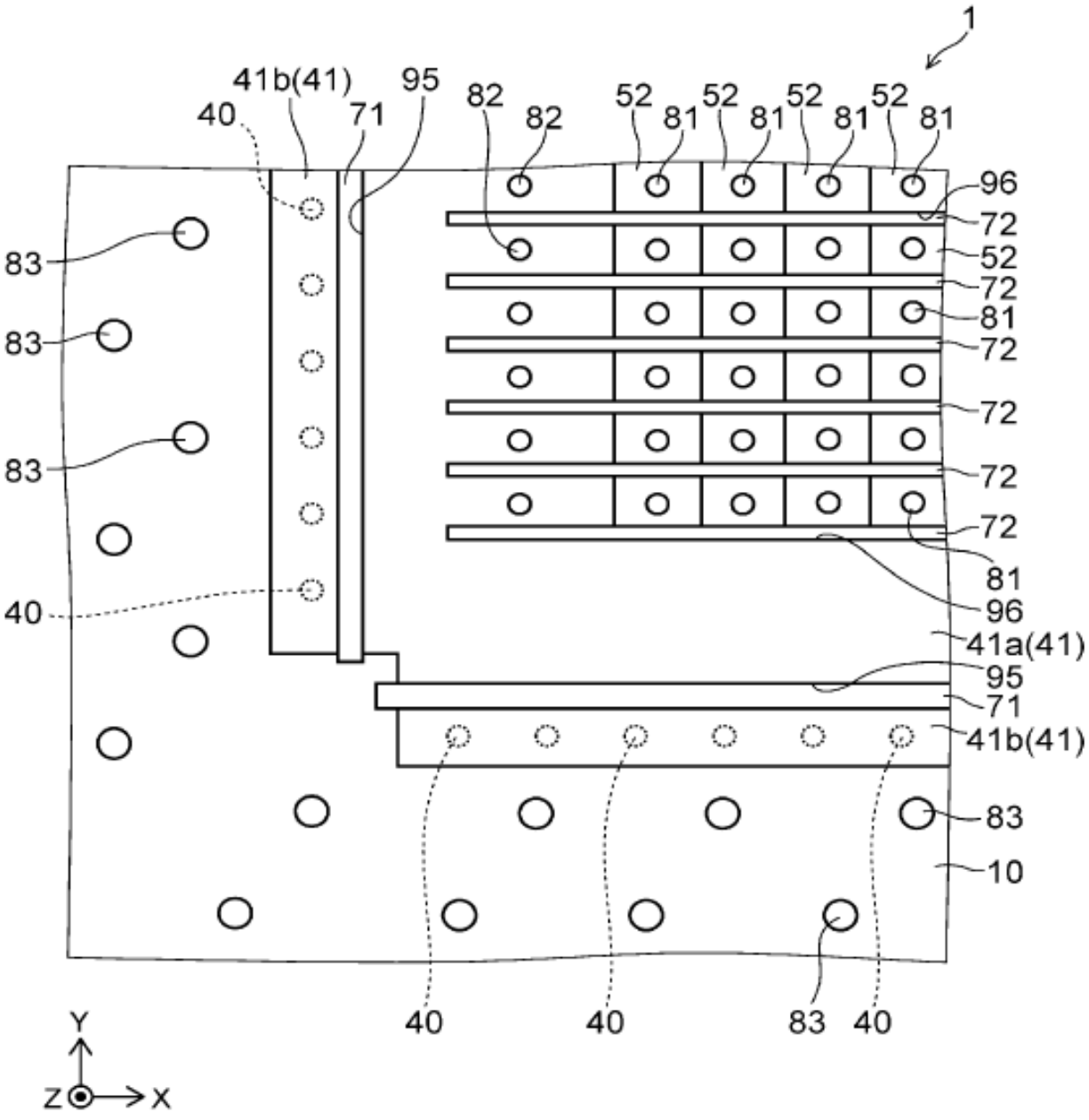
[Document name] Drawings
[FIG. 1]



[FIG. 2]



[FIG. 3]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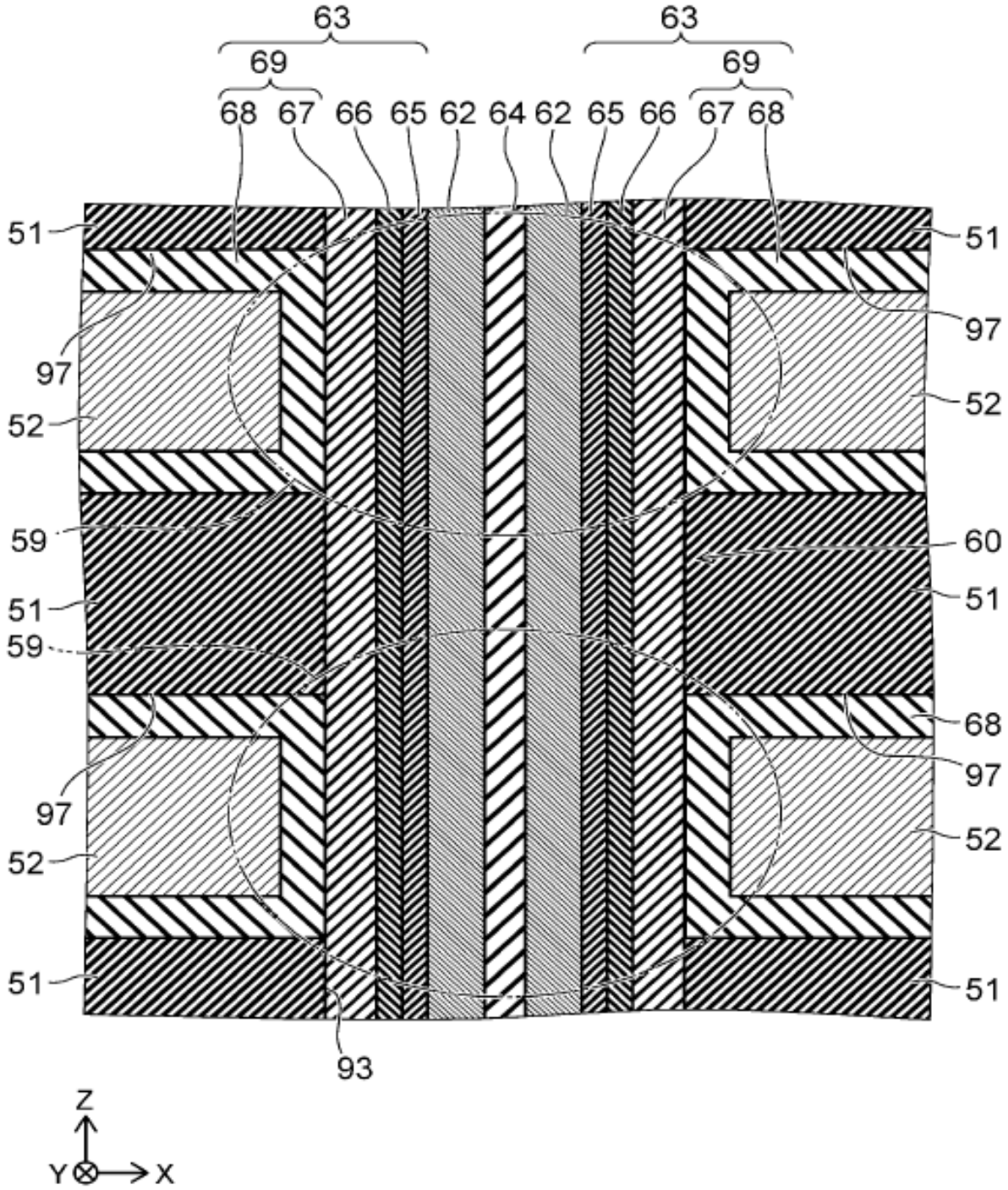
[FIG. 4]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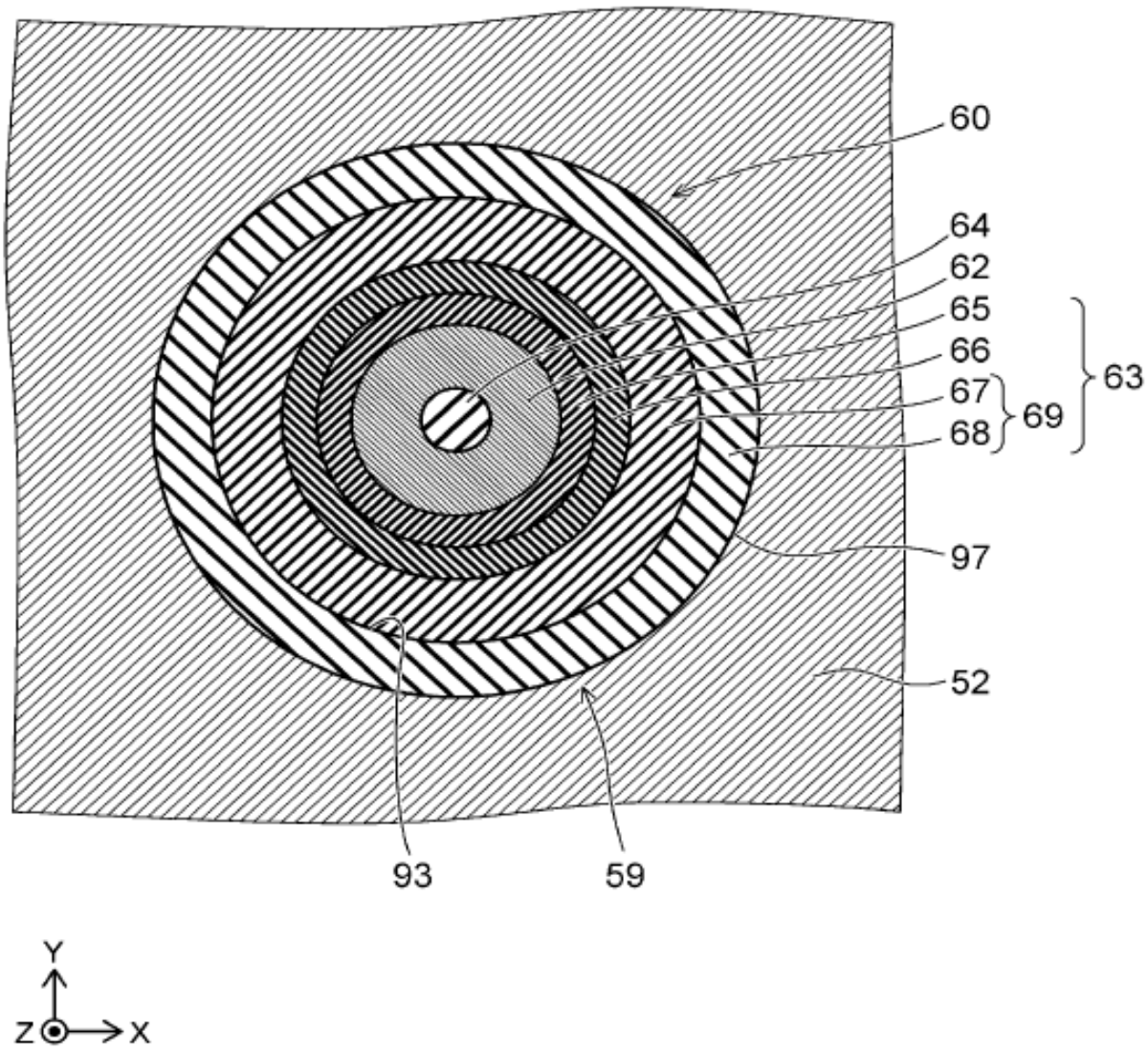
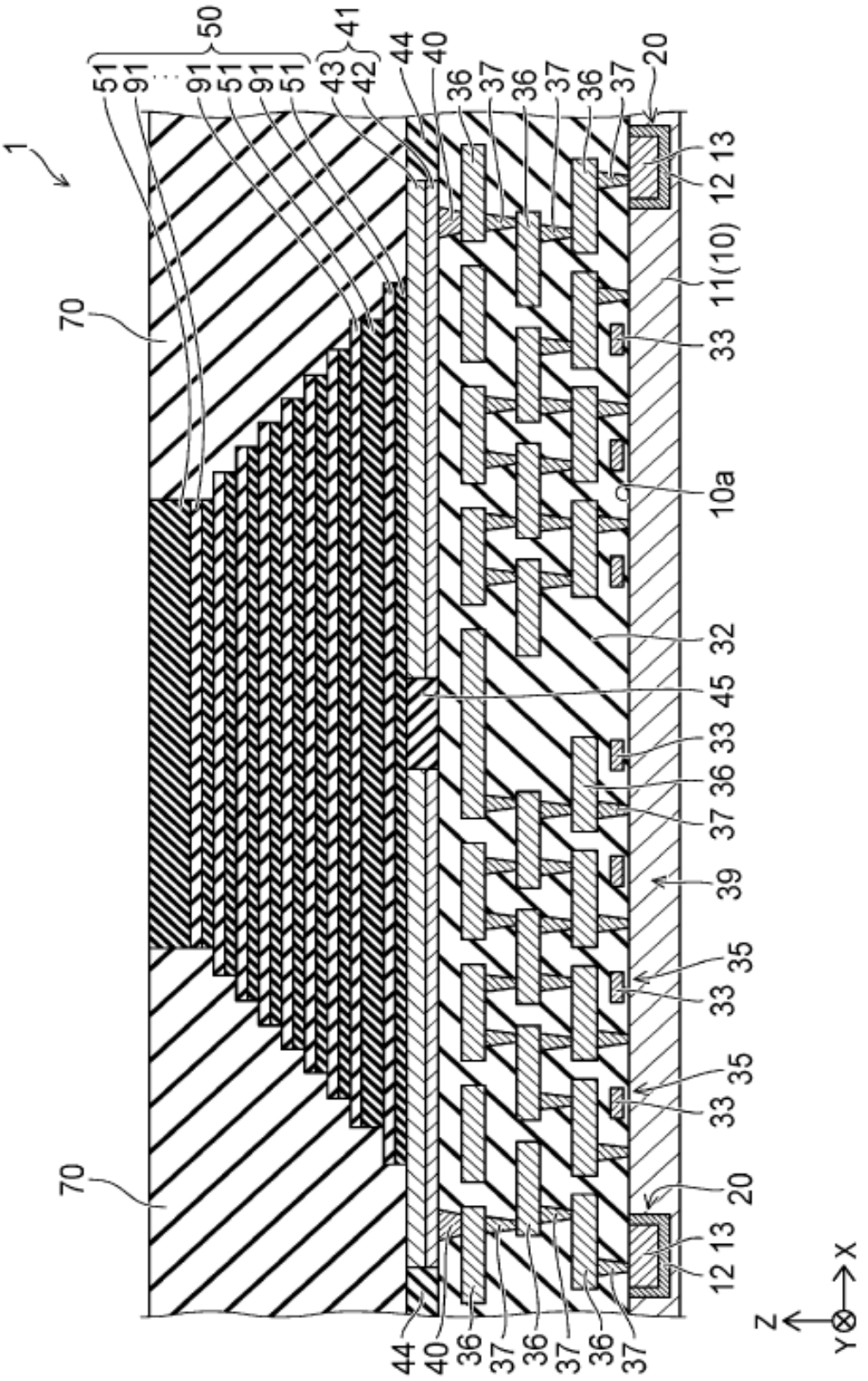
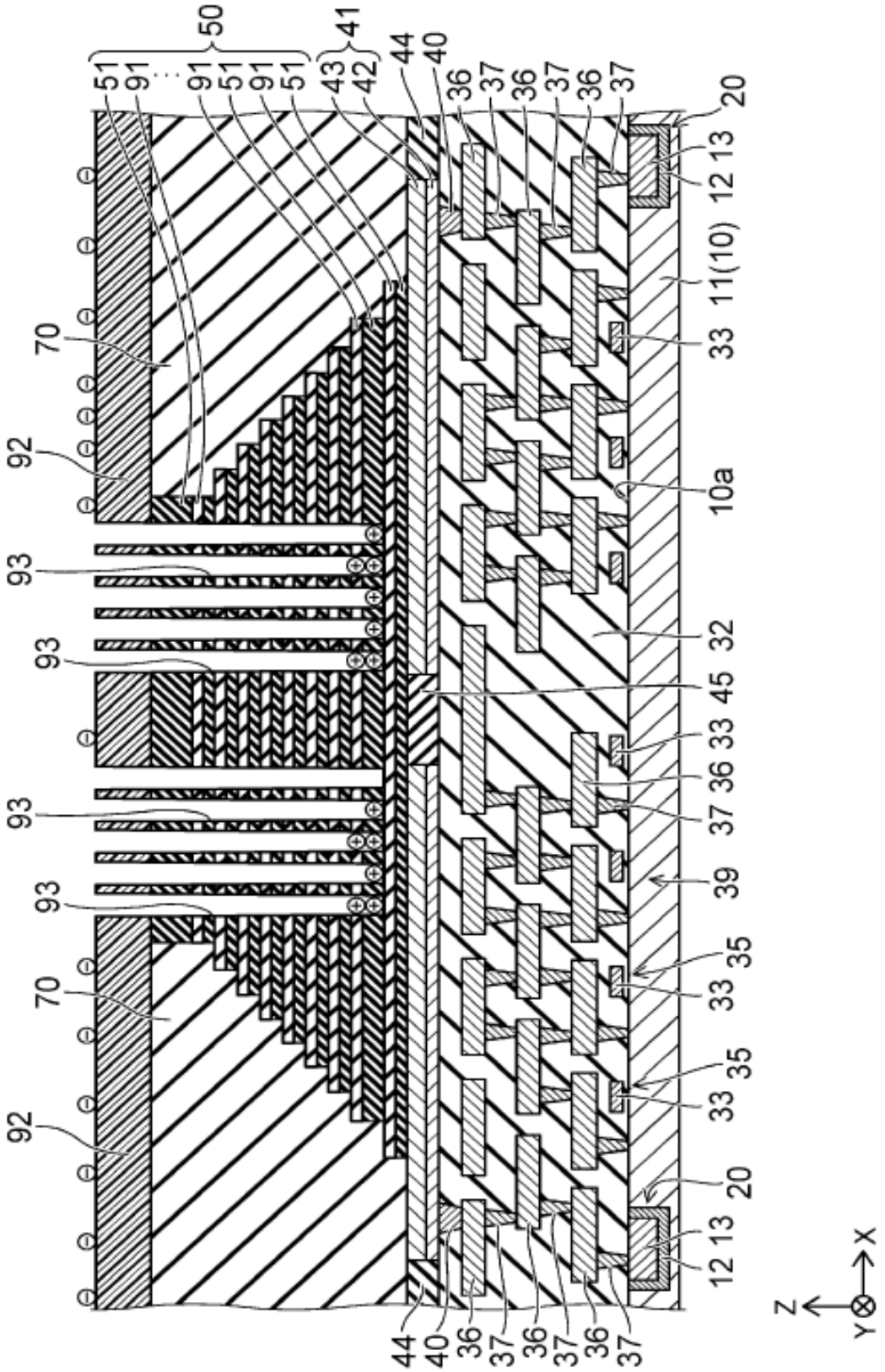
[FIG. 5]



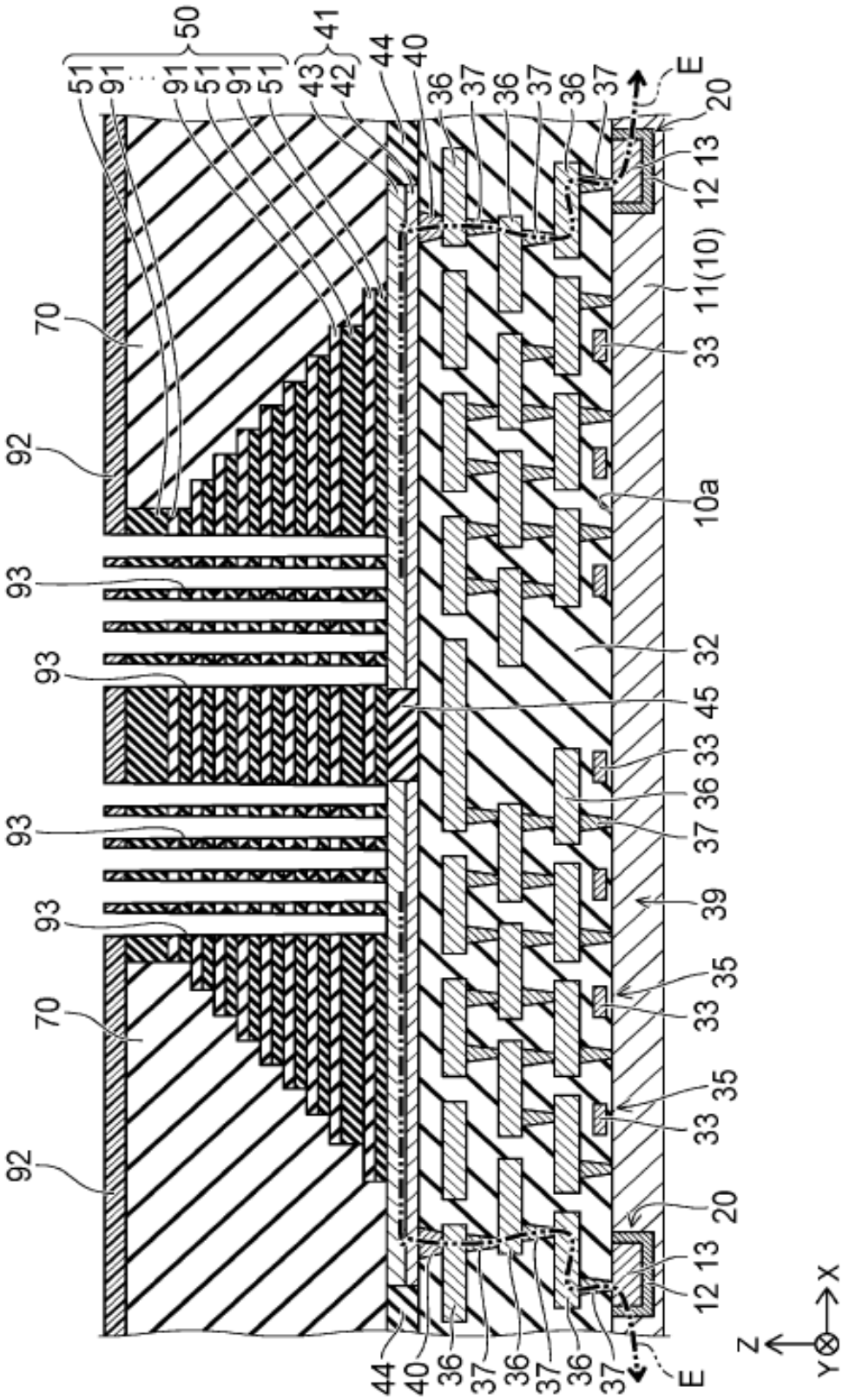
[FIG. 6]



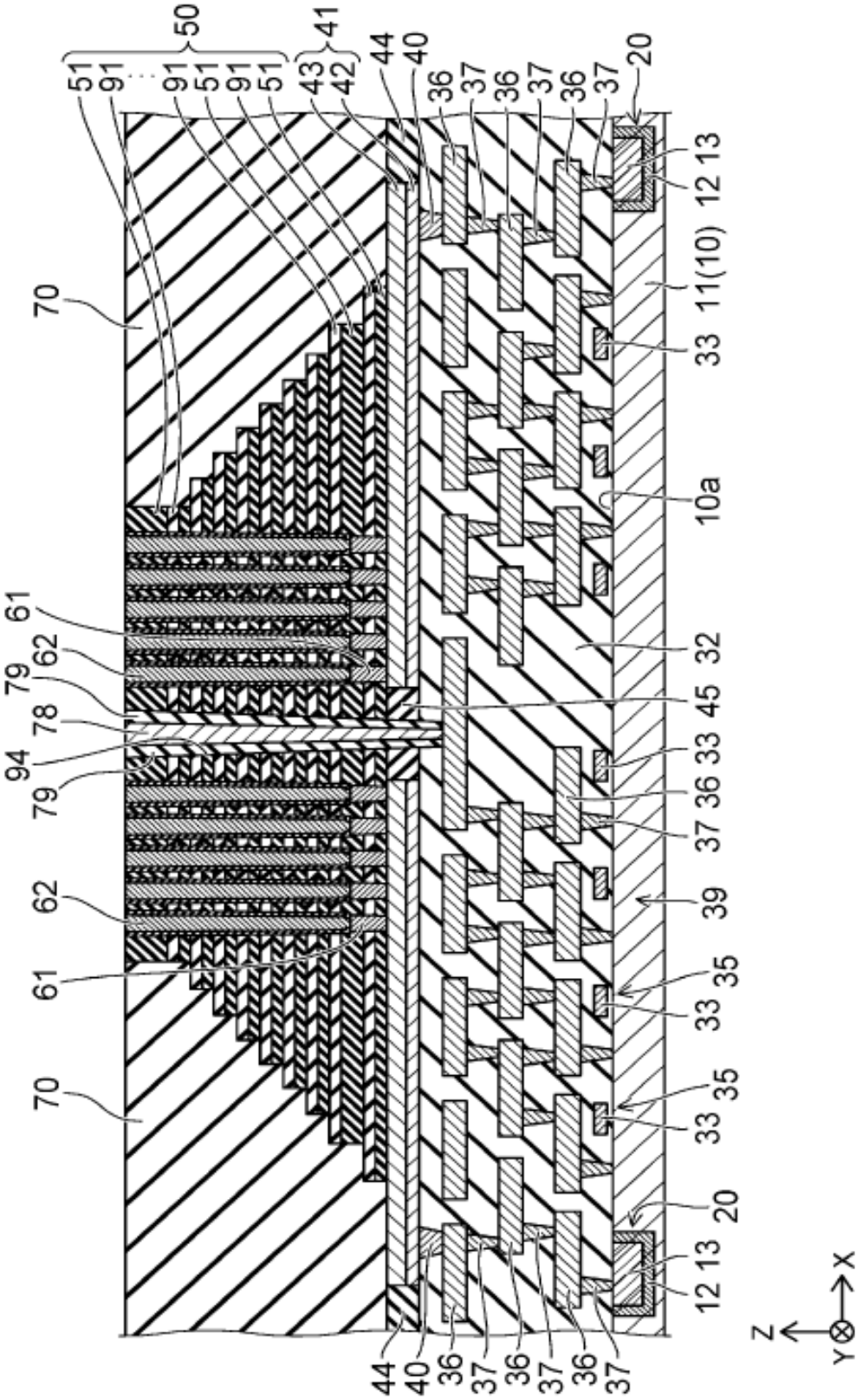
[FIG. 7]



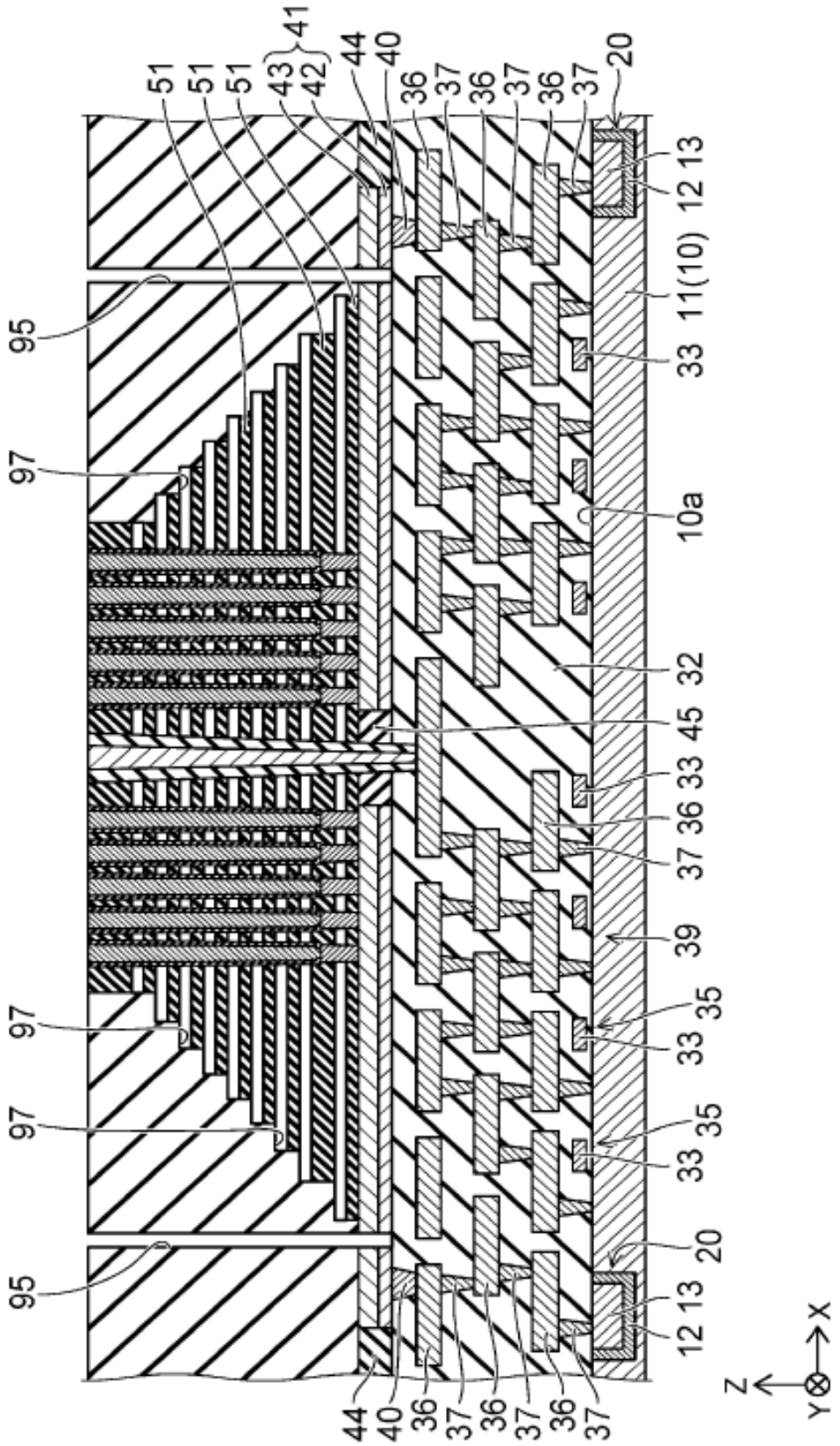
[FIG. 8]



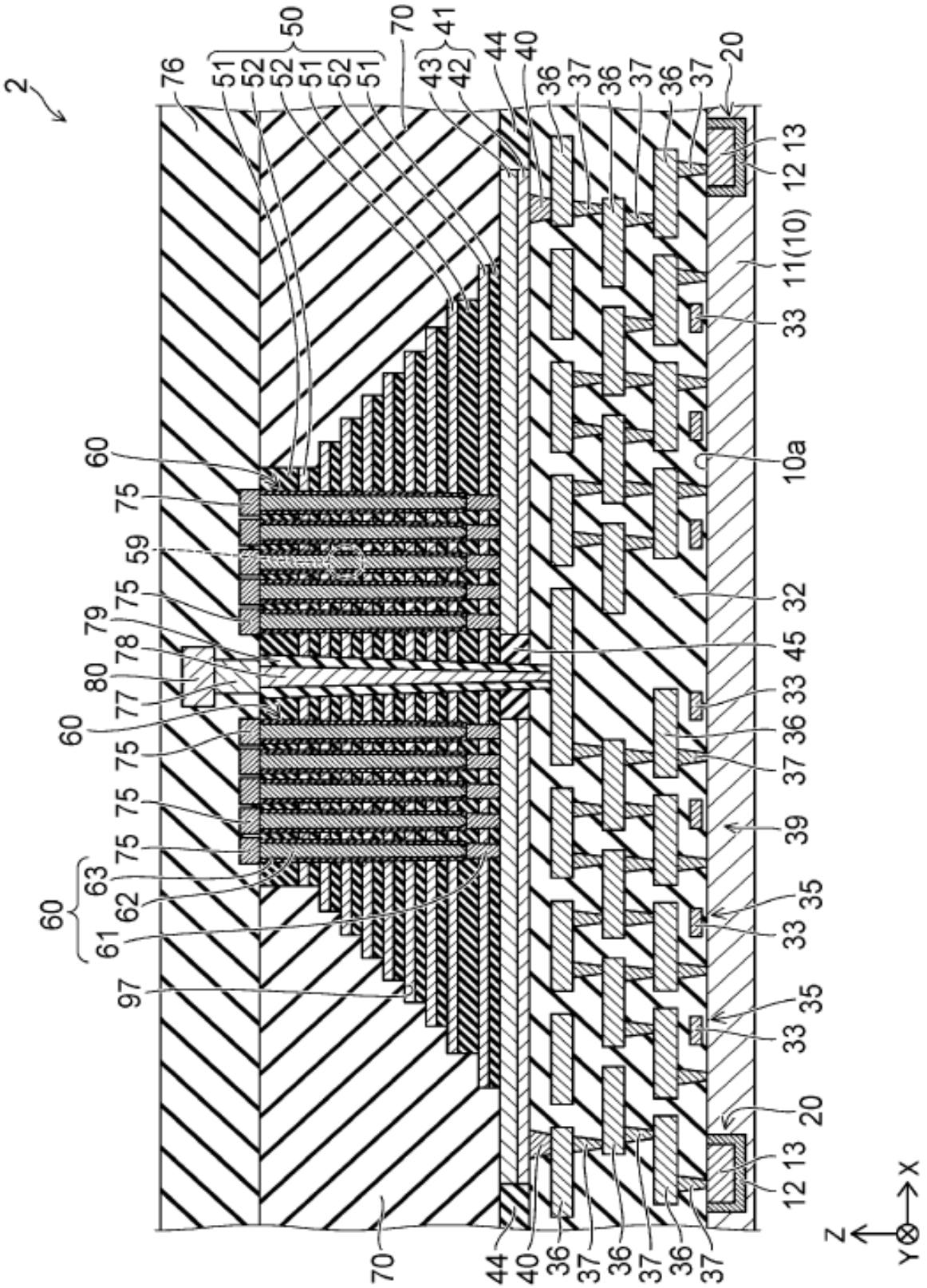
[FIG. 9]



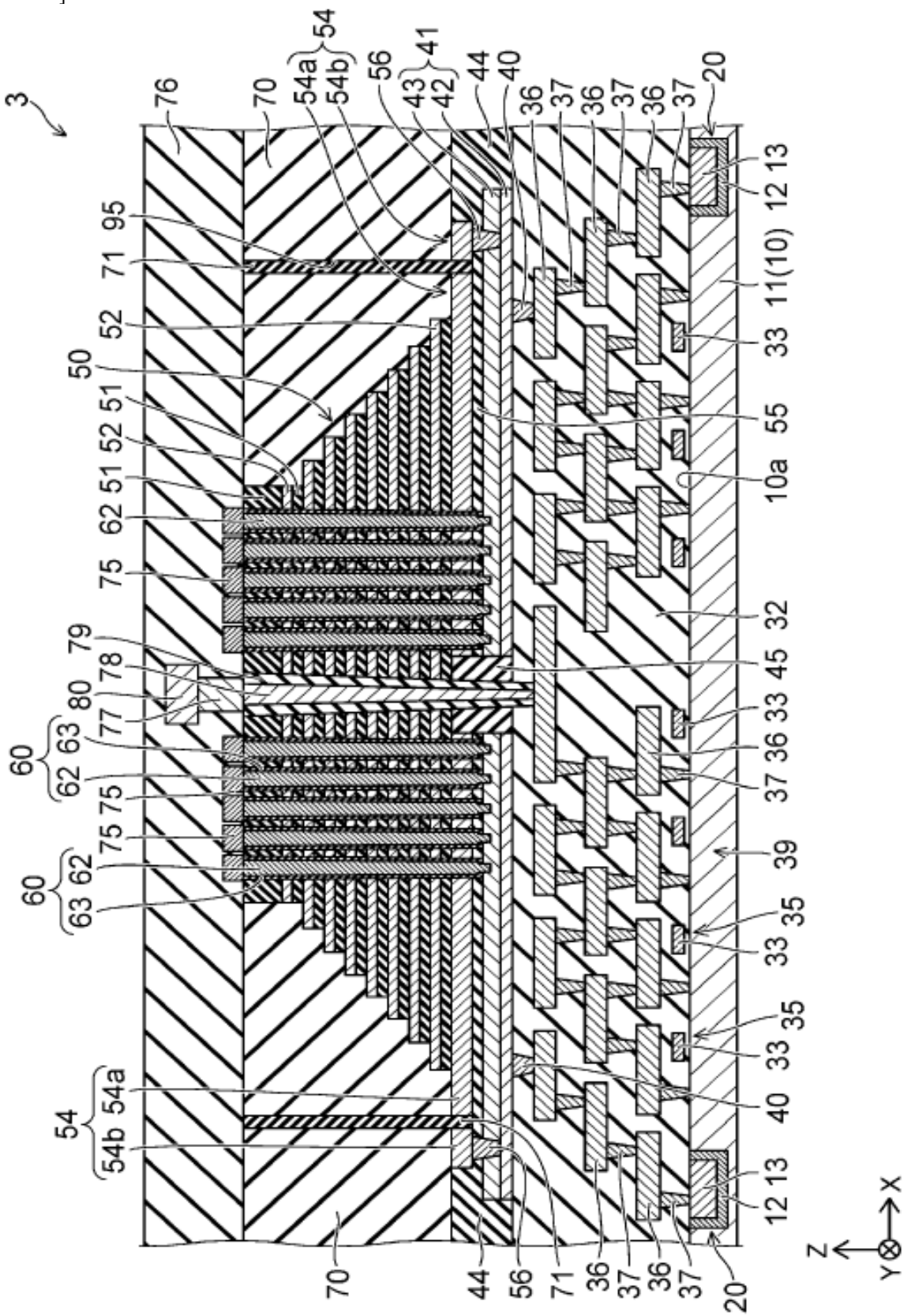
[FIG. 10]



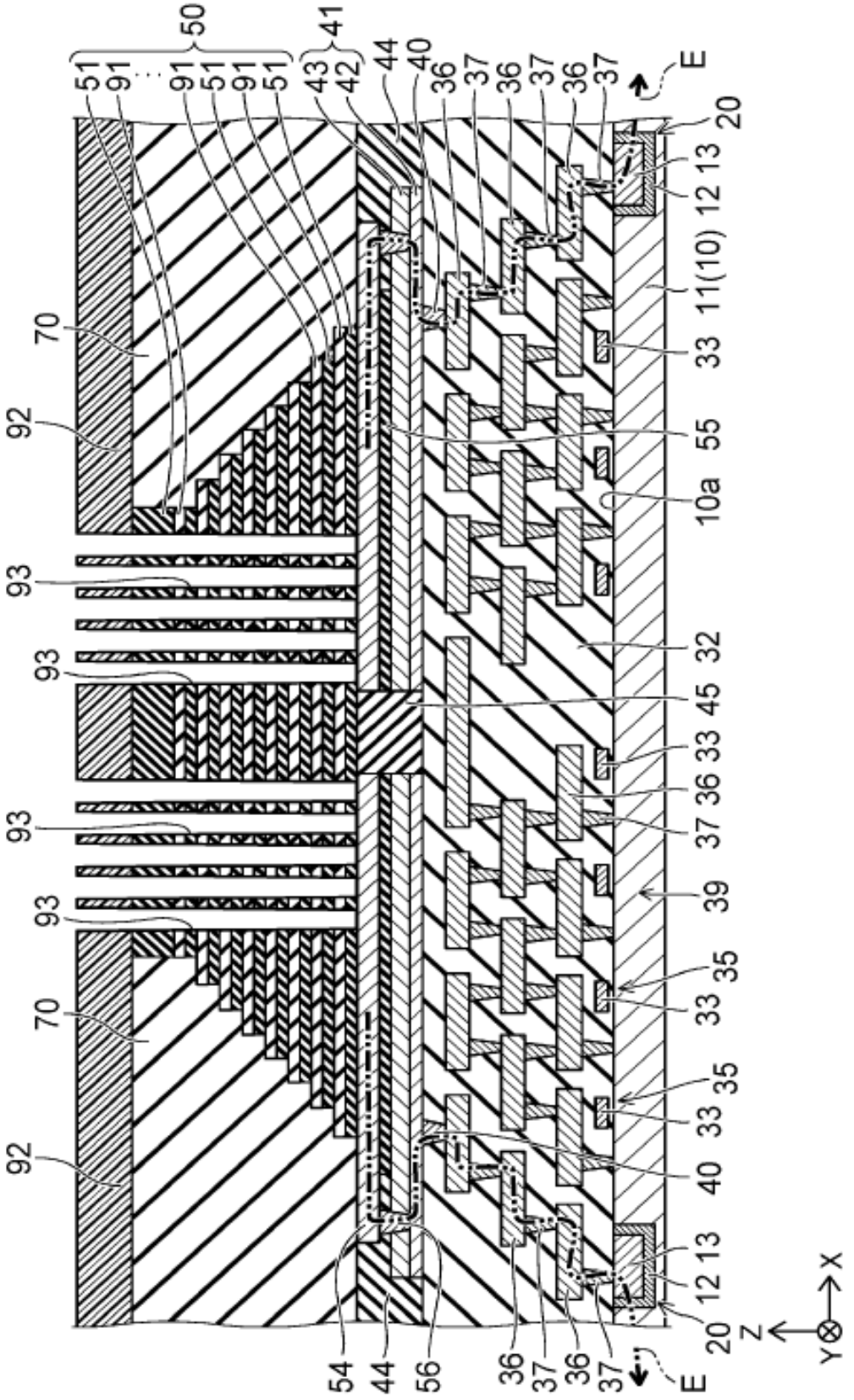
[FIG. 11]



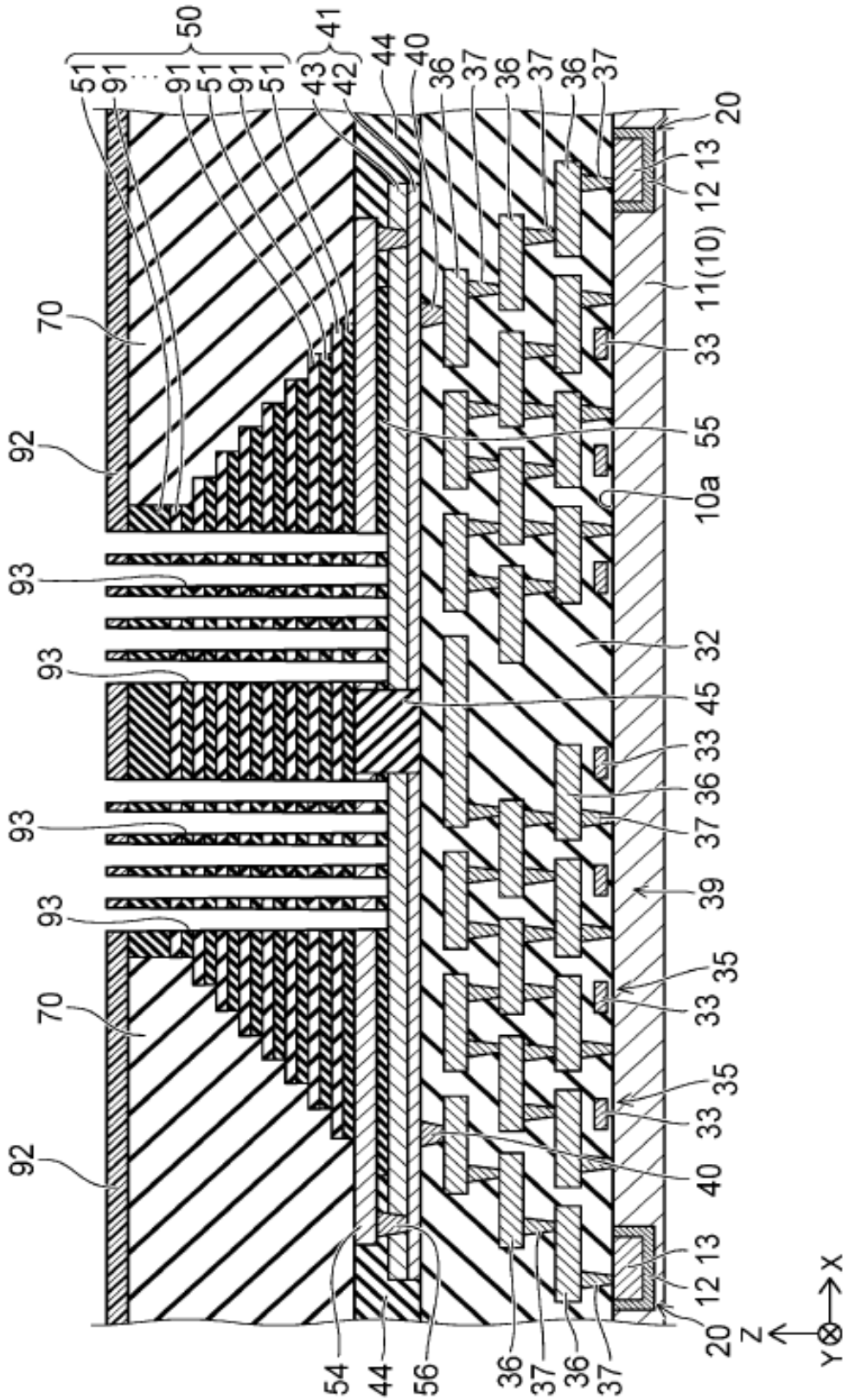
[FIG. 12]



[FIG. 13]



[FIG. 14]



[Document name]	Notification of Change of Name (General Succession)
[Submission date]	September 5, 2018
[Address]	Attn. Commissioner, Japan Patent Office
[Case identification]	
[Application number]	Japanese Patent Application 2017-247987
[Successor]	
[Identification number]	318010018
[Name or title]	Toshiba Memory Co., Ltd.
[Successor's agent]	
[Identification number]	100108062
[Attorney]	
[Name or title]	Masahiko Hyugaji
[Inventory of submitted properties]	
[Name of property]	Certificate of all historical matters 1
[Indication of claim]	We make reference to the Notification of Change of Applicant's Name (General Succession) relating to Japanese Patent Application No. 2014-201807 submitted on the same date, and omit this here accordingly.
[Name of property]	Power of Attorney 1
[Indication of claim]	We make reference to the Notification of Change of Applicant's Name (General Succession) relating to Japanese Patent Application No. 2014-201807 submitted on the same date, and omit this here accordingly.

Applicant history

317006041
20170411
New registration

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Toshiba Memory Co., Ltd.
318010018
20180705
New registration

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Pangea Inc.
318010018
20180801
Name change Address change

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Toshiba Memory Co., Ltd.

Certification of personally signed document

I, the undersigned, Timothy Prellwitz, appointed Notary Public with international notary ID 20191219, hereby certify that: **Simon Edmunds**

have been identified through governmental issued ID and that I have acknowledged and verified the original signature on the attached document.

If there are any questions or concerns, please contact me through the details below.

The foregoing document was acknowledged before me on 2024-10-21

Timothy Prellwitz – Notary Public
Document ID 389-24

NOTARIUS PUBLICUS * TIMOTHY PRELLWITZ *

OFFICIAL SEAL NOTARY PUBLIC

TRANSPERFECT

October 21, 2024

Certification

Translator's Declaration:

I, Simon Edmunds, hereby declare:
That I possess advanced knowledge of the Japanese and English languages.

My qualifications are as follows: BA Hons in Japanese, certificate in advanced Japanese, certificate in patent translation.

The attached Japanese into English translation has been translated by me and to the best of my knowledge and belief, it is a true and accurate translation of:

JP2017247987

I understand that willful false statement and link are punishable by fine or imprisonment, or both (18 U.S.C. 1001) and may jeopardize the validity of the application or any patent issuing thereon. I declare under the penalty of the perjury that all statements made herein of my own knowledge are true and all statements made on information and belief are believed to be true.

Simon Edmunds

Sworn to before me this
21st of October 2024

Signature, Notary Public

Stamp, Notary Public