Docket No. 516693US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

INVENTOR(S) Jun FUJIKI, et al.

SERIAL NO: New Application ART UNIT:

FILING DATE: Herewith EXAMINER:

FOR: SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR MANUFACTURING SAME

FEE TRANSMITTAL

☐ No additional fee is required

☐ Small entity status of this application under 37 C.F.R. §1.9 and §1.27 is claimed.

☐ Track 1 Prioritized Examination

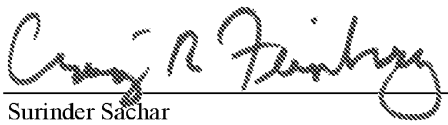
The Fee has been calculated as shown below:

FOR	NUMBER FILED	NUMBER EXTRA	RATE	CALCULATIONS
TOTAL CLAIMS	20 - 20 =	0	x $100 =	$ 0.00
INDEPENDENT CLAIMS	3 - 3 =	0	x $460 =	$ 0.00
UTILITY APPLICATION SIZE FEE	32* - 100 = (* 42 x .75)	0 (each addtl. 50 sheets over 100)	x $400 =	$0.00
☐ MULTIPLE DEPENDENT CLAIMS (If applicable)			+ $820 =	$0.00
■ LATE FILING OF DECLARATION			+ $160 =	$160.00
☐ NON-ELECTRONIC FILING FEE			+ $400 =	$0.00
■ FILING FEE ($300.00) ■ SEARCH FEE ($660.00) ■ EXAMINATION FEE ($760.00)			BASIC FEES	$1,720.00
			TOTAL OF ABOVE CALCULATIONS	$1,880.00
☐ REDUCTION BY 50% FOR FILING BY SMALL ENTITY				$0.00
☐ FILING FEE REDUCED IF E-FILED – SMALL ENTITY			+ $-75 =	$0.00
☐ FILING IN NON-ENGLISH LANGUAGE			+ $140 =	$0.00
			TOTAL	$1,880.00

☐ Please charge Deposit Account No. **15-0030** in the amount of **$0.00**

■ Credit card payment is being made online (if electronically filed), or is attached hereto (if paper filed), in the amount of **$1,880.00**.

■ The Director is hereby authorized to charge any additional fees which may be required for the papers being filed herewith and for which no payment is enclosed herewith, or credit any overpayment to Deposit Account No. **15-0030**, with the **EXCEPTION** of deficiencies in fees for multiple dependent claims in new applications.

Submitted by: 

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	516693US
	Application Number	New Application
Title of Invention	SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR MANUFACTURING SAME	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	516693US
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Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

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Application Information:

Title of the Invention	SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR MANUFACTURING SAME		
Attorney Docket Number	516693US	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	15	Suggested Figure for Publication (if any)	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	516693US
	Application Number	New Application
Title of Invention	SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR MANUFACTURING SAME	

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	■ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)
Customer Number	22850		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the application number blank.

Prior Application Status			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Application Number	Country	Filing Date (YYYY-MM-DD)	Access Code (if applicable)
2017-247987	Japan	2017-12-25	6D0B

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

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Title of Invention	SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR MANUFACTURING SAME		

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78 this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant must opt-out of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	516693US
	Application Number	New Application
Title of Invention	SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR MANUFACTURING SAME	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

■ Assignee	☐ Legal Representative under 35 U.S.C. 117	☐ Joint Inventor
☐ Person to whom the inventor is obligated to assign.	☐ Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor :	

If the Applicant is an Organization check here. ■

Organization Name	TOSHIBA MEMORY CORPORATION

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Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

If the Assignee or Non-Applicant Assignee is an Organization check here. ■

Organization Name	TOSHIBA MEMORY CORPORATION

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	516693US
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Title of Invention	SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR MANUFACTURING SAME	

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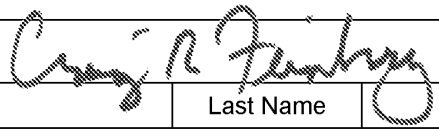
Country Japan		Postal Code	
Phone Number		Fax Number	
Email Address			

Signature:

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature				Date (YYYY-MM-DD)	2018-09-12
First Name		Last Name		Registration Number	

Craig R. Feinberg
Registration No.: 62,116

SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR MANUFACTURING SAME

CROSS-REFERENCE TO RELATED APPLICATION

This application is based upon and claims the benefit of priority from Japanese Patent Application No. 2017-247987, filed on December 25, 2017; the entire contents of which are incorporated herein by reference.

FIELD

Embodiments described herein relate generally to a semiconductor memory device and a method for manufacturing same.

BACKGROUND

In recent years, a stacked semiconductor memory device has been proposed in which memory cells are integrated three-dimensionally. For such a stacked semiconductor memory device, investigations are being performed to realize even more downsizing by providing a thick insulating film between the semiconductor substrate and the memory cells and by forming a control circuit inside the insulating film and the upper layer portion of the semiconductor substrate. In such a case, a conductive film is provided on the insulating film and used as a source line.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cross-sectional view showing a semiconductor memory device according to a first embodiment;

FIG. 2 is a cross-sectional view showing the semiconductor memory device according to the first embodiment;

FIG. 3 is a top view showing the semiconductor memory device according to the first embodiment;

FIG. 4 is a cross-sectional view showing a memory cell transistor of the semiconductor memory device according to the

first embodiment;

FIG. 5 is a cross-sectional view showing a memory cell transistor of the semiconductor memory device according to the first embodiment;

FIG. 6 is a cross-sectional view showing a method for manufacturing the semiconductor memory device according to the first embodiment;

FIG. 7 is a cross-sectional view showing a method for manufacturing the semiconductor memory device according to the first embodiment;

FIG. 8 is a cross-sectional view showing a method for manufacturing the semiconductor memory device according to the first embodiment;

FIG. 9 is a cross-sectional view showing a method for manufacturing the semiconductor memory device according to the first embodiment;

FIG. 10 is a cross-sectional view showing a method for manufacturing the semiconductor memory device according to the first embodiment;

FIG. 11 is a cross-sectional view showing a semiconductor memory device according to a second embodiment;

FIG. 12 is a cross-sectional view showing a semiconductor memory device according to a third embodiment;

FIG. 13 is a top view showing the semiconductor memory device according to the third embodiment;

FIG. 14 is a cross-sectional view showing a method for manufacturing the semiconductor memory device according to the third embodiment; and

FIG. 15 is a cross-sectional view showing a method for manufacturing the semiconductor memory device according to the third embodiment.

DETAILED DESCRIPTION

According to one embodiment, a semiconductor memory

device includes a semiconductor substrate including a diode formed in an upper layer portion of the semiconductor substrate, a first insulating film provided above the semiconductor substrate, a first conductive film provided above the first insulating film and coupled to the diode, a stacked body provided above the first conductive film, an insulator and an electrode film being stacked alternately in the stacked body, a semiconductor member piercing the stacked body and being connected to the first conductive film, and a charge storage member provided between the electrode film and the semiconductor member.

First embodiment

A first embodiment will now be described.

FIG. 1 and FIG. 2 are cross-sectional views showing a semiconductor memory device according to the embodiment.

FIG. 3 is a top view showing the semiconductor memory device according to the embodiment.

FIG. 4 and FIG. 5 are cross-sectional views showing the memory cell transistor of the semiconductor memory device according to the embodiment.

The drawings are schematic and are drawn with appropriate exaggerations or omissions. For example, the components are drawn to be larger and fewer than the actual components. Also, the numbers, dimensional ratios, etc., of the components do not always match between the drawings.

The semiconductor memory device according to the embodiment is stacked NAND flash memory.

As shown in FIG. 1, a silicon substrate 10 is provided in the semiconductor memory device 1 according to the embodiment. For example, the silicon substrate 10 is formed of single-crystal silicon (Si).

As shown in FIG. 2, for example, the conductivity type of the main body portion of the silicon substrate 10 is a p-type. An n-type well 11 is formed in a portion of the upper layer portion of the silicon substrate 10. A p-type well 12 is formed

in a portion of the upper layer portion of the n-type well 11. An n^+-type diffusion layer 13 is formed in a portion of the upper layer portion of the p-type well 12. The donor concentration of the n^+-type diffusion layer 13 is higher than the donor concentration of the n-type well 11.

A diode 21 is formed at the interface between the silicon substrate 10 and the n-type well 11; a diode 22 is formed at the interface between the p-type well 12 and the n-type well 11; and a diode 23 is formed at the interface between the p-type well 12 and the n^+-type diffusion layer 13. A bidirectional diode 20 is formed by connecting the diode 21, the diode 22, and the diode 23 in series. One or multiple bidirectional diodes 20 are formed in a portion of the upper layer portion of the silicon substrate 10.

A diffusion layer 15 and STI (Shallow Trench Isolation (an element-separating insulating film)) 16 are formed in the upper layer portion of the silicon substrate 10. Also, for example, the source/drain layers of MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors) (not illustrated), etc., are formed in the upper layer portion of the silicon substrate 10.

As shown in FIG. 1 and FIG. 2, a gate insulating layer 31 is formed on the silicon substrate 10; and an insulating film 32 is formed on the gate insulating layer 31. For example, the gate insulating layer 31 and the insulating film 32 are formed of silicon oxide (SiO). For example, the gate insulating layer 31 is formed by thermal oxidation of the silicon substrate 10; and, for example, the insulating film 32 is formed by CVD (Chemical Vapor Deposition) using TEOS (Tetraethyl orthosilicate ($Si(OC_2H_5)_4$)) as a source material.

In the specification hereinbelow, an XYZ orthogonal coordinate system is employed for convenience of description. Two mutually-orthogonal directions parallel to an upper surface 10a of the silicon substrate 10 are taken as an "X-direction" and a "Y-direction;" and a direction perpendicular to the upper surface 10a of the silicon substrate 10 is taken as a "Z-direction." Although a direction that is in the Z-direction

from the silicon substrate 10 toward the insulating film 32 also is called "up" and the reverse direction also is called "down," these expressions are for convenience and are independent of the direction of gravity.

A gate electrode 33 is provided inside the insulating film 32 on the gate insulating layer 31. A MOSFET 35 is formed of source/drain layers (not illustrated), the gate insulating layer 31, and the gate electrode 33. Interconnects 36 and plugs 37 are formed inside the insulating film 32. A portion of the plugs 37 connects the interconnects 36 to each other; and another portion of the plugs 37 connects the interconnect 36 to the diffusion layer 15 of the silicon substrate 10. A control circuit 39 includes the MOSFET 35, a portion of the interconnects 36, and a portion of the plugs 37. Other components may be included in the control circuit 39. A plug 40 is provided on the interconnect 36 of the uppermost level inside the insulating film 32.

A source electrode film 41 is provided on the insulating film 32. The configuration of the source electrode film 41 is a substantially flat plate configuration spreading along the XY plane and is patterned into a prescribed configuration as described below. In the source electrode film 41, for example, a metal layer 42 that is made of tungsten (W) is provided; and, for example, a silicon layer 43 that is made of polycrystalline silicon (Si) is provided on the metal layer 42. An insulating film 44 is provided at the periphery of the source electrode film 41. An insulating film 45 that pierces the source electrode film 41 in the Z-direction is provided in a region surrounded with the source electrode film 41.

A portion of the lower surface of the source electrode film 41 contacts the plug 40. Thereby, the portion of the source electrode film 41 is connected to the upper end of the plug 40. The lower end of the plug 40 is connected to a portion of the interconnect 36 of the uppermost level. The interconnect 36 is connected to the interconnects 36 of lower levels by the plugs 37; and a portion of the interconnect 36 of the lowermost level

is connected to the upper surface of the n^+-type diffusion layer 13 via the plug 37. Thereby, a portion of the source electrode film 41 is connected to one end of the bidirectional diode 20 via the plug 40, the multiple interconnects 36, and the multiple plugs 37. The current path from the source electrode film 41 to the bidirectional diode 20 is insulated from the control circuit 39.

A stacked body 50 is provided on the source electrode film 41. In the stacked body 50, insulating films 51 and electrode films 52 are stacked alternately along the Z-direction. The insulating films 51 are made of, for example, silicon oxide; and the electrode films 52 are made of, for example, tungsten. The configuration of the end portion of the stacked body 50 is a staircase configuration in which terraces are formed every electrode film 52. Air gaps may be formed as the insulators instead of the insulating films 51.

A columnar portion 60 is provided inside the stacked body 50. The configuration of the columnar portion 60 is a circular column having a central axis extending in the Z-direction. A silicon member 61 is provided at the lower portion of the columnar portion 60; and a silicon pillar 62 is provided on the silicon member 61. A memory film 63 is provided at the periphery of the silicon pillar 62. The silicon pillar 62 is connected to the silicon member 61; and the silicon member 61 is connected to the source electrode film 41.

As shown in FIG. 4 and FIG. 5, a core member 64 that is made of silicon oxide is provided inside the silicon pillar 62. A tunneling insulating film 65, a charge storage film 66, and a silicon oxide layer 67 are provided in this order from the inner side, i.e., the silicon pillar 62 side, toward the outer side in the memory film 63. On the other hand, an aluminum oxide layer 68 is provided on the upper surface of the electrode film 52, on the lower surface of the electrode film 52, and on the side surface of the electrode film 52 opposing the silicon pillar 62. A blocking insulating film 69 includes the silicon oxide layer 67 and the aluminum oxide layer 68.

Although the tunneling insulating film 65 normally is insulative, the tunneling insulating film 65 is a film in which a tunneling current flows when a prescribed voltage within the range of the drive voltage of the semiconductor memory device 1 is applied and is, for example, a single-layer silicon oxide film or an ONO film in which a silicon oxide layer, a silicon nitride layer, and a silicon oxide layer are stacked in this order. The charge storage film 66 is a film that can store charge, is made from, for example, a material having trap sites of electrons, and is made of, for example, silicon nitride. The blocking insulating film 69 is a film in which a current substantially does not flow even when a voltage within the range of the drive voltage of the semiconductor memory device 1 is applied.

The memory film 63 is formed of the tunneling insulating film 65, the charge storage film 66, and the blocking insulating film 69. The memory film 63 is disposed between the silicon pillar 62 and the electrode film 52. The columnar portion 60 includes the silicon member 61, the silicon pillar 62, the memory film 63, and the core member 64. The silicon pillar 62 is insulated from the electrode films 52 by the memory film 63. The silicon member 61 also is insulated from the electrode films 52 by an insulating film (not illustrated).

As shown in FIG. 1 to FIG. 3, an insulating film 70 that is made of, for example, silicon oxide is provided at the periphery of the stacked body 50 on the source electrode film 41 and on the insulating film 44. An insulating plate 71 is provided inside the insulating film 70 to substantially surround the stacked body 50. The insulating plate 71 is separated from the stacked body 50. The insulating plate 71 pierces the source electrode film 41 and reaches the insulating film 32. Also, multiple insulating plates 72 that extend in the X-direction are provided inside the stacked body 50. The insulating plates 72 pierce the insulating films 51 and the electrode films 52 of the stacked body 50 and reach the source electrode film 41. For example, a block that is used as the minimum unit of the data erase is formed of each of the stacked bodies 50 divided in the

Y-direction by the insulating plates 72. For example, the insulating plates 71 and 72 are formed of silicon oxide. The insulating plate 71 and the insulating plates 72 may be linked to each other. Also, the configuration of the insulating plate 71 may be a frame-like configuration surrounding the stacked body 50 when viewed from the Z-direction. However, even in such a case, the insulating plate 71 is separated from the stacked body 50.

The source electrode film 41 is divided by the insulating plate 71 into a central portion 41a disposed on the inner side of the insulating plate 71 and a peripheral portion 41b disposed on the outer side of the insulating plate 71. The central portion 41a and the peripheral portion 41b are insulated from each other by the insulating plate 71. In other words, the lower portion of the insulating plate 71 is disposed between the central portion 41a and the peripheral portion 41b. The central portion 41a is connected to the silicon pillars 62 via the silicon members 61. The peripheral portion 41b is connected to the bidirectional diode 20 via the plug 40, the interconnects 36, and the plugs 37.

Bit lines 75 that extend in the Y-direction are provided on the stacked body 50 and on the insulating film 70. The bit lines 75 are connected to the upper ends of the silicon pillars 62. An insulating film 76 is provided on the stacked body 50 and on the insulating film 70 to cover the bit lines 75. A plug 77 is provided inside the insulating film 76. A through-via 78 that extends in the Z-direction to pierce the stacked body 50 and the insulating film 45 surrounded with the source electrode film 41 is provided between the plug 77 and the interconnect 36 of the control circuit 39. An insulating film 79 that is made of, for example, silicon oxide is provided at the periphery of the through-via 78. The through-via 78 is insulated from the electrode films 52 and the source electrode film 41 by the insulating film 79. An upper layer interconnect 80 is provided on the plug 77 and is connected to the plug 77.

As shown in FIG. 2 and FIG. 3, contacts 81 to 83 are

provided inside the insulating film 70. The lower ends of the contacts 81 are connected to the electrode films 52; and the upper ends of the contacts 81 are connected to a portion of the upper layer interconnects (not illustrated). The lower ends of the contacts 82 are connected to the source electrode film 41; and the upper ends of the contacts 82 are connected to another portion of the upper layer interconnects (not illustrated). The lower ends of the contacts 83 are connected to the diffusion layers 15 of the silicon substrate 10, etc.; and the upper ends of the contacts 83 are connected to yet another portion of the upper layer interconnects (not illustrated).

In the semiconductor memory device 1 according to the embodiment, a memory cell 59 is formed at each crossing portion between the electrode films 52 and the silicon pillars 62. The channel of the memory cell 59 is the silicon pillar 62; the gate insulating film is the tunneling insulating film 65 and the blocking insulating film 69; the gate is the electrode film 52; and the charge storage member is the charge storage film 66. The control circuit 39 injects charge from the silicon pillar 62 into the charge storage film 66 and discharges the charge from the charge storage film 66 into the silicon pillar 62 by controlling the potentials of the source electrode film 41, the bit lines 75, and the electrode films 52. Thereby, the threshold voltages of the memory cells 59 are changed; and data is stored.

A method for manufacturing the semiconductor memory device according to the embodiment will now be described.

FIG. 6 to FIG. 10 are cross-sectional views showing the method for manufacturing the semiconductor memory device according to the embodiment.

First, as shown in FIG. 6 and FIG. 2, the n-type well 11, the p-type well 12, the n^+-type diffusion layer 13, the diffusion layer 15, the STI 16, etc., are formed in the upper layer portion of the silicon substrate 10. Thereby, the bidirectional diode 20 is formed in a portion of the upper layer portion of the silicon substrate 10.

Continuing, the gate insulating layer 31 is formed in the upper surface 10a of the silicon substrate 10 by performing thermal oxidation treatment. Then, for example, the gate electrode 33, the plugs 37, the interconnects 36, and the plug 40 are formed while forming the insulating film 32 by repeating CVD using TEOS as a source material. Thereby, the control circuit 39 is formed inside the insulating film 32 and the upper layer portion of the silicon substrate 10. At this time, the plug 40 is connected to the n^+-type diffusion layer 13 via a portion of the plugs 37 and a portion of the interconnects 36.

Continuing, the source electrode film 41 is formed by forming the metal layer 42 on the insulating film 32 and by depositing the silicon layer 43 on the metal layer 42. Then, the source electrode film 41 is patterned; the insulating film 44 is formed at the periphery of the source electrode film 41; and the insulating film 45 is formed in a region surrounded with the source electrode film 41.

Continuing, the stacked body 50 is formed on the source electrode film 41, the insulating film 44, and the insulating film 45 by alternately depositing the insulating films 51 made of silicon oxide and insulative sacrificial films 91 made of silicon nitride (SiN). The material of the sacrificial films 91 is not limited to silicon nitride as long as the material is insulative and has etching selectivity with respect to the insulating films 51. Then, the end portion of the stacked body 50 is patterned into a staircase configuration in which a terrace is formed every sacrificial film 91. Then, the insulating film 70 is formed at the periphery of the stacked body 50 by depositing silicon oxide.

Continuing as shown in FIG. 7, a mask pattern 92 is formed on the stacked body 50 and on the insulating film 70. Then, reactive ion etching (RIE) is performed using the mask pattern 92 as a mask. Specifically, positive ions of the etching species are generated by plasmatizing an etching gas; and the positive ions are accelerated by applying an electric field and caused to collide selectively with the stacked body 50 via the mask pattern 92. Thereby, memory holes 93 are formed in the

stacked body 50. At this time, the stacked body 50 is formed from insulating materials, i.e., silicon oxide and silicon nitride; therefore, a positive charge that originates in the positive ions of the etching species accumulates inside the memory holes 93. On the other hand, at this stage, a negative charge accumulates on the outer surface of the intermediate structure body. In FIG. 7, the positive charge is illustrated by the symbols of "+" surrounded with a circle; and the negative charge is illustrated by the symbols of "-" surrounded with a circle.

Continuing as shown in FIG. 8, when the memory holes 93 reach the source electrode film 41, the positive charge that has accumulated inside the memory holes 93 moves into the source electrode film 41 and further flows into the n^+-type diffusion layer 13 via the plug 40, the interconnects 36, and the plugs 37 as shown by a path E in FIG. 8. Thereby, the diode 23 and the diode 21 of the bidirectional diode 20 breakdown; and the positive charge flows into the silicon substrate 10 via the bidirectional diode 20 and is discharged to the outside via the silicon substrate 10. As a result, arcing inside the insulating film 32 can be prevented.

Continuing as shown in FIG. 9, FIG. 4, and FIG. 5, the silicon members 61 are formed by epitaxial growth of the silicon inside the lower portions of the memory holes 93 by using the silicon layer 43 as a starting point. Then, the silicon oxide layer 67, the charge storage film 66, the tunneling insulating film 65, the silicon pillar 62, and the core member 64 are formed on the inner surfaces of the memory holes 93 on the silicon members 61. The silicon pillars 62 are connected to the source electrode film 41 via the silicon members 61. Then, a through-via hole 94 is formed to pierce the stacked body 50, the insulating film 45, and the upper portions of the insulating film 32 and reach a portion of the interconnect 36. Then, the insulating film 79 is formed on the inner surface of the through-via hole 94; and the through-via 78 is formed on the inner surface of the insulating film 79. The through-via 78 is connected to the interconnect 36.

Continuing as shown in FIG. 10 and FIG. 3, slits 95 are formed to pierce the insulating film 70 and the source electrode film 41; and slits 96 are formed to pierce the stacked body 50. The source electrode film 41 is divided into the central portion 41a and the peripheral portion 41b by the slits 95. This dividing causes the central portion 41a to be insulated from the silicon substrate 10 because the plug 40 is connected to only the peripheral portion 41b. Then, the sacrificial films 91 (referring to FIG. 9) are removed by performing wet etching via the slits 96. As a result, spaces 97 are formed where the sacrificial films 91 are removed.

Continuing as shown in FIG. 1, FIG. 4, and FIG. 5, the aluminum oxide layer 68 is formed on the inner surfaces of the spaces 97 via the slits 96. The aluminum oxide layer 68 contacts the silicon oxide layer 67; and the blocking insulating film 69 is formed of the aluminum oxide layer 68 and the silicon oxide layer 67. The memory film 63 is formed of the tunneling insulating film 65, the charge storage film 66, and the blocking insulating film 69. Then, a barrier metal layer (not illustrated) is formed on the inner surfaces of the spaces 97 via the slits 96; subsequently, the electrode film 52 is formed by filling a conductive material such as tungsten, etc., into the spaces 97. Then, the portions of the electrode film 52 and the aluminum oxide layer 68 formed inside the slits 95 and inside the slits 96 are removed by etching. Then, by filling silicon oxide into the slits 95 and into the slits 96, the insulating plates 71 are formed inside the slits 95; and the insulating plates 72 are formed inside the slits 96 (referring to FIG. 3).

Continuing as shown in FIG. 1, the bit lines 75 that extend in the Y-direction are formed on the stacked body 50 and on the insulating film 70 and connected to the silicon pillars 62. The insulating film 76 is formed on the stacked body 50 and on the insulating film 70; and the plug 77 and the upper layer interconnect 80 are formed inside the insulating film 76. The upper layer interconnect 80 is connected to the through-via 78 via the plug 77. Thus, the semiconductor memory device 1

according to the embodiment is manufactured.

Effects of the embodiment will now be described.

In the embodiment as shown in FIG. 6, the bidirectional diode 20 is formed in the upper layer portion of the silicon substrate 10. Also, the source electrode film 41 is connected to the bidirectional diode 20 via the plug 40, the interconnects 36, and the plugs 37 when forming the source electrode film 41 on the insulating film 32. Thereby, when the memory holes 93 reach the source electrode film 41 as shown in FIG. 8, the bidirectional diode 20 breaks down due to the positive charge accumulated inside the memory holes 93; and the positive charge flows in the silicon substrate 10 via the source electrode film 41, the plug 40, the interconnects 36, the plugs 37, the n^+-type diffusion layer 13, the p-type well 12, and the n-type well 11 and is emitted to the outside. Thereby, the arcing inside the insulating film 32 can be prevented; and the breakdown of the insulating film 32 can be avoided.

As shown in FIG. 10, the source electrode film 41 is divided into the central portion 41a and the peripheral portion 41b by forming the slits 95. As a result, in the semiconductor memory device 1 after completion shown in FIG. 1, the central portion 41a of the source electrode film 41 to which the silicon pillars 62 are connected can be insulated reliably from the silicon substrate 10; and the parasitic capacitance of the source electrode film 41 decreases. As a result, the operations of the semiconductor memory device 1 are more stable and faster.

Second embodiment

A second embodiment will now be described.

FIG. 11 is a cross-sectional view showing a semiconductor memory device according to the embodiment.

As shown in FIG. 11, the semiconductor memory device 2 according to the embodiment differs from the semiconductor memory device 1 according to the first embodiment described above (referring to FIG. 1 to FIG. 5) in that the insulating plate 71 is not provided. The insulating plates 72 (referring to FIG.

3) are provided in the semiconductor memory device 2 as well.

The semiconductor memory device 2 can be manufactured by forming only the slits 96 (referring to FIG. 3) and by not forming the slits 95 in the process shown in FIG. 10.

According to the embodiment as well, similarly to the first embodiment described above, the positive charge that accumulates inside the memory holes 93 (referring to FIG. 7) flows in the bidirectional diode 20 via the source electrode film 41, the plug 40, the interconnects 36, and the plugs 37, causes the bidirectional diode 20 to breakdown, and is discharged to the outside via the silicon substrate 10. As a result, the breakdown of the insulating film 32 can be avoided.

In the semiconductor memory device 2 according to the embodiment, although the source electrode film 41 is not divided by the insulating plate 71 (referring to FIG. 1 and FIG. 3), the bidirectional diode 20 is interposed between the source electrode film 41 and the silicon substrate 10; therefore, the source electrode film 41 can be driven electrically independently from the silicon substrate 10 within the range of the prescribed potential difference.

Otherwise, the configuration, the manufacturing method, and the effects of the embodiment are similar to those of the first embodiment described above.

Third embodiment

A third embodiment will now be described.

FIG. 12 is a cross-sectional view showing a semiconductor memory device according to the embodiment.

FIG. 13 is a top view showing the semiconductor memory device according to the embodiment.

In the semiconductor memory device 3 according to the embodiment as shown in FIG. 12 and FIG. 13, a silicon film 54 that is made of conductive polysilicon, an insulating film 55, and a plug 56 are provided in addition to the configuration of the semiconductor memory device 1 according to the first embodiment described above (referring to FIG. 1 to FIG. 5).

The insulating plates 71 and the insulating plates 72 are linked to each other. The source electrode film 41 is not divided by the insulating plates 71 and 72; but the silicon film 54 is divided by the insulating plates 71 and 72. The silicon members 61 (referring to FIG. 1) are not provided; and the silicon pillars 62 are directly connected to the source electrode film 41.

Details will now be described.

The silicon film 54 is disposed between the source electrode film 41 and the stacked body 50; and the configuration of the silicon film 54 is a substantially flat plate configuration spreading along the XY plane. The insulating film 55 is disposed between the source electrode film 41 and the silicon film 54. The plug 56 pierces the insulating film 55 and the silicon layer 43 of the source electrode film 41; the lower end of the plug 56 contacts the metal layer 42 of the source electrode film 41; and the upper end of the plug 56 contacts the silicon film 54. Thereby, a portion of the silicon film 54 is connected to the source electrode film 41 via the plug 56. Similarly to the first embodiment, the source electrode film 41 is connected to the bidirectional diode 20 via the plug 40. Accordingly, a portion of the silicon film 54 is connected to the bidirectional diode 20 formed in a portion of the upper layer portion of the silicon substrate 10. The current path that reaches the bidirectional diode 20 from the silicon film 54 is insulated from the control circuit 39. The insulating film 44 is provided at the periphery of a stacked structure made of the source electrode film 41, the insulating film 55, and the silicon film 54. The insulating film 45 pierces the stacked structure in the Z-direction.

Although the insulating plates 71 and the insulating plates 72 pierce the silicon film 54 in the Z-direction, the insulating plates 71 and the insulating plates 72 do not pierce the source electrode film 41. Therefore, the silicon film 54 is divided into a central portion 54a and a peripheral portion 54b by the insulating plates 71; but the source electrode film 41 is

not divided by the insulating plates 71. The plug 56 is connected to the peripheral portion 54b of the silicon film 54. The position of the plug 40 is not limited to the outside of the insulating plate 71. The central portion 54a is divided into a plurality of portions for each block by the insulating plate 72. As described above, the insulating plate 72 divides the stacked body 50 into a plurality of blocks in the Y direction. A contact 84 is provided for each block in the insulating film 70. The lower end of the contact 84 is connected to the central portion 54a of the silicon film 54. As a result, different potentials can be applied to the central portion 54a of the silicon film 54 for each block. On the other hand, the contact 82 connected to the source electrode film 41 is disposed at a position separated from the silicon film 54.

In the columnar portions 60, the silicon members 61 are not provided; and the lower ends of the silicon pillars 62 contact the source electrode film 41. The silicon pillars 62 pierce the central portion 54a of the silicon film 54 and are insulated from the silicon film 54 by the memory film 63 except for the aluminum oxide layer 68. The central portion 54a of the silicon film 54 functions as the gate electrode of the lowermost level for the silicon pillars 62, e.g., a select gate that switches the conduction/non-conduction of the silicon pillars 62 for each block.

A method for manufacturing the semiconductor memory device according to the embodiment will now be described.

FIG. 14 and FIG. 15 are cross-sectional views showing the method for manufacturing the semiconductor memory device according to the embodiment.

First, as shown in FIG. 14, the structure body from the silicon substrate 10 to the source electrode film 41 is made by a method similar to that of the first embodiment described above.

Continuing, the insulating film 55 is formed on the source electrode film 41; the plug 56 is formed inside the insulating film 55 and the silicon layer 43 of the source electrode film 41; and the silicon film 54 is formed on the plug 56. Then, the

silicon film 54 and the insulating film 55 are patterned; the insulating film 44 is formed at the periphery of a stacked structure made of the source electrode film 41, the silicon film 54, and the insulating film 55; and the insulating film 45 is formed in a region surrounded with the stacked structure.

Continuing, the stacked body 50 is formed on the silicon film 54 by alternately depositing the insulating films 51 made of silicon oxide and the sacrificial films 91 made of silicon nitride. Then, the insulating film 70 is formed at the periphery of the stacked body 50. Then, the mask pattern 92 is formed on the stacked body 50 and on the insulating film 70. Then, the memory holes 93 are formed in the stacked body 50 by performing RIE by using the mask pattern 92 as a mask and by using the silicon film 54 as an etching stopper. The conditions of the RIE are set to conditions such that silicon oxide and silicon nitride are etched efficiently. At this time, similarly to the first embodiment, positive charge accumulates inside the memory holes 93.

Continuing, when the memory holes 93 reach the silicon film 54, the etching rate decreases. Thereby, the positions of the lower ends of the memory holes 93 are aligned. At this time, the positive charge that accumulates inside the memory holes 93 moves into the silicon film 54. Then, as shown by the path E, the positive charge moves into the source electrode film 41 via the plug 56, moves into the n^+-type diffusion layer 13 via the plug 40, the interconnects 36, and the plugs 37, causes breakdown of the bidirectional diode 20, and moves into the silicon substrate 10. Then, the positive charge is discharged to the outside via the silicon substrate 10. Thereby, the arcing at the insulating film 55 and the insulating film 32 can be prevented.

Continuing as shown in FIG. 15, the conditions of the RIE are modified to conditions such that silicon is etched efficiently; and the RIE is continued. Thereby, the memory holes 93 reach the insulating film 55. Then, the conditions of the RIE are modified to conditions such that silicon oxide is etched

efficiently; and the RIE is continued. Thereby, the memory holes 93 reach the silicon layer 43 of the source electrode film 41. Here, the RIE is ended.

Continuing as shown in FIG. 12, FIG. 4, and FIG. 5, the silicon oxide layers 67, the charge storage films 66, the tunneling insulating films 65, the silicon pillars 62, and the core members 64 are formed on the inner surfaces of the memory holes 93. The silicon pillars 62 are connected to the silicon layer 43. Then, the insulating film 79 and the through-via 78 are formed.

Continuing as shown in FIG. 12, FIG. 13 and FIG. 3, the silicon film 54 is utilized once as an etching stopper; the insulating film 70, the stacked body 50, and the region below the insulating film 70 and the stacked body 50 are etched; and the slits 95 and 96 are formed to substantially uniform depths. For example, the slits 95 and 96 can be formed simultaneously by etching using one mask pattern as a mask. Although the slits 95 and 96 pierce the silicon film 54 at this time, the slits 95 and 96 do not pierce the source electrode film 41. Thereby, the silicon film 54 is divided into the central portion 54a and the peripheral portion 54b by the slit 95. The silicon pillars 62 are surrounded with the central portion 54a; and the plug 56 is connected to only the peripheral portion 54b; therefore, by dividing the silicon film 54, the central portion 54a of the silicon film 54 that functions as the gate electrode of the lowermost level can be insulated from the source electrode film 41. The subsequent manufacturing method is similar to that of the first embodiment described above.

Effects of the embodiment will now be described.

In the embodiment as well, similarly to the first embodiment described above, the bidirectional diode 20 is formed in the upper layer portion of the silicon substrate 10; and the source electrode film 41 is connected to the bidirectional diode 20 via the plug 40, the interconnects 36, and the plugs 37. The silicon film 54 is connected to the source electrode film 41 via the plug 56. Thereby, when the memory

holes 93 reach the silicon film 54 as shown in FIG. 14, breakdown of the bidirectional diode 20 occurs; and the positive charge that accumulates inside the memory holes 93 flows in the silicon substrate 10 via the silicon film 54, the plug 56, the source electrode film 41, the plug 40, the interconnects 36, the plugs 37, the n^+-type diffusion layer 13, the p-type well 12, and the n-type well 11 and is emitted to the outside. Thereby, the arcing inside the insulating film 55 and inside the insulating film 32 can be prevented; and the breakdown of the insulating film 55 and the insulating film 32 can be avoided.

By forming the slits 95 as shown in FIG. 12 and FIG. 13, the silicon film 54 is divided into the central portion 54a and the peripheral portion 54b. As a result, in the semiconductor memory device 3 after completion, the central portion 54a that functions as the gate electrode of the lowermost level for the silicon pillars 62 can be insulated reliably from the source electrode film 41. Thereby, the central portion 54a and the source electrode film 41 can be driven electrically independently. Also, the parasitic capacitance of the central portion 54a decreases.

Because the bidirectional diode 20 is interposed between the source electrode film 41 and the silicon substrate 10, the source electrode film 41 can be driven electrically independently from the silicon substrate 10 within the range of the prescribed potential difference.

Otherwise, the configuration, the manufacturing method, and the effects of the embodiment are similar to those of the first embodiment described above.

According to the embodiments described above, a semiconductor memory device and a method for manufacturing the semiconductor memory device can be realized in which downsizing is possible.

While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the inventions. Indeed,

the novel embodiments described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the embodiments described herein may be made without departing from the spirit of the inventions. The accompanying claims and their equivalents are intended to cover such forms or modification as would fall within the scope and spirit of the inventions.

What is claimed is:

1. A semiconductor memory device, comprising:

a semiconductor substrate including a diode formed in an upper layer portion of the semiconductor substrate;

a first insulating film provided above the semiconductor substrate;

a first conductive film provided above the first insulating film and coupled to the diode;

a stacked body provided above the first conductive film, an insulator and an electrode film being stacked alternately in the stacked body;

a semiconductor member piercing the stacked body and being connected to the first conductive film; and

a charge storage member provided between the electrode film and the semiconductor member.

2. The device according to claim 1, wherein

the semiconductor substrate includes:

a first semiconductor layer of a first conductivity type;

a second semiconductor layer formed in a portion of an upper layer portion of the first semiconductor layer, the second semiconductor layer being of a second conductivity type; and

a third semiconductor layer formed in a portion of an upper layer portion of the second semiconductor layer, the third semiconductor layer being of the first conductivity type, and

the first conductive film is coupled to the third semiconductor layer.

3. The device according to claim 2, wherein

the semiconductor substrate is of the second conductivity type, and

the first semiconductor layer is formed in a portion of the

upper layer portion of the semiconductor substrate.

4. The device according to claim 1, further comprising a first plug coupled between the diode and the first conductive film,

the first conductive film including

a first portion connected to the semiconductor member, and

a second portion connected to the first plug and insulated from the first portion.

5. The device according to claim 4, wherein

the second portion is provided at a periphery of the first portion.

6. The device according to claim 4, further comprising:

a second insulating film provided at a periphery of the stacked body; and

an insulating plate provided inside the second insulating film and between the first portion and the second portion.

7. The device according to claim 4, further comprising:

a first interconnect provided in the first insulating film and coupled between the first plug and the diode.

8. The device according to claim 7, further comprising:

a second interconnect provided in the first insulating film and coupled to a transistor formed on the semiconductor substrate, the first interconnect being insulated from the second interconnect.

9. The device according to claim 8, further comprising:

a through-via piercing the stacked body and the first conductive film, and coupled to the second interconnect.

10. The device according to claim 1, further comprising:

a second conductive film provided between the first conductive film and the stacked body;

an intermediate insulating film provided between the first conductive film and the second conductive film;

a first plug coupled between the diode and the first conductive film; and

a second plug coupled between the first conductive film and the second conductive film.

11. The device according to claim 10, wherein

the second conductive film includes a first portion surrounding the semiconductor member, and a second portion connected to the second plug and insulated from the first portion.

12. The device according to claim 11, wherein

the second portion is provided at a periphery of the first portion.

13. The device according to claim 11, further comprising:

a second insulating film provided at a periphery of the stacked body; and

an insulating plate provided inside the second insulating film and between the first portion and the second portion.

14. The device according to claim 10, further comprising:

a first interconnect provided in the first insulating film and coupled between the first plug and the diode.

15. The device according to claim 14, further comprising:

a second interconnect provided in the first insulating film and coupled to a transistor formed on the semiconductor substrate; and

a through-via piercing the stacked body and the first and second conductive films, and coupled to the second interconnect.

16. A method for manufacturing a semiconductor memory device, comprising:

forming a diode in an upper layer portion of a semiconductor substrate;

forming a first insulating film above the semiconductor substrate;

forming a first conductive film above the first insulating film, the first conductive film being coupled to the diode;

forming a stacked body above the first conductive film by alternately forming a first insulating material film and a second insulating material film;

forming a hole in the stacked body to reach the first conductive film by performing reactive ion etching;

forming a charge storage member inside the hole;

forming a semiconductor member inside the hole where the charge storage member is formed, the semiconductor member being connected to the first conductive film; and

replacing the second insulating material film with an electrode film after the forming of the semiconductor member.

17. The method according to claim 16, wherein

the forming of the first insulating film includes forming a plug inside the first insulating film, the plug being coupled between the diode and the first conductive film, and

the method further comprises subdividing the first conductive film into a first portion and a second portion after the forming of the hole, the first portion being connected to the semiconductor member, the second portion being connected to the plug.

18. The method according to claim 16, wherein

the forming of the diode includes

forming a first semiconductor layer of a first conductivity type in a portion of the upper layer portion of the semiconductor substrate,

forming a second semiconductor layer of a second conductivity type in a portion of an upper layer portion of the first semiconductor layer, and

forming a third semiconductor layer of the first conductivity type in a portion of an upper layer portion of the second semiconductor layer, the first conductive film being coupled to the third semiconductor layer.

19. A method for manufacturing a semiconductor memory device, comprising:

forming a diode in an upper layer portion of a semiconductor substrate;

forming a first insulating film above the semiconductor substrate;

forming a first conductive film above the first insulating film, the first conductive film being coupled to the diode;

forming an intermediate insulating film above the first conductive film;

forming a plug piercing the intermediate insulating film;

forming a second conductive film above the intermediate insulating film, the second conductive film being coupled to the first conductive film via the plug;

forming a stacked body above the second conductive film by alternately forming a first insulating material film and a second insulating material film;

forming a hole in the stacked body, the second conductive film, and the second insulating film to reach the first conductive film by performing reactive ion etching;

forming a charge storage member inside the hole;

forming a semiconductor member inside the hole where the charge storage member is formed, the semiconductor member being connected to the first conductive film;

subdividing the second conductive film into a first portion and a second portion after the forming of the hole, the first portion surrounding the semiconductor member, the second portion being connected to the plug; and

replacing the second insulating material film with an electrode film after the forming of the semiconductor member.

20. The method according to claim 19, wherein

the forming of the diode includes

forming a first semiconductor layer of a first conductivity type in a portion of the upper layer portion of the semiconductor substrate,

forming a second semiconductor layer of a second conductivity type in a portion of an upper layer portion of the first semiconductor layer, and

forming a third semiconductor layer of the first conductivity type in a portion of an upper layer portion of the second semiconductor layer, the first conductive film being coupled to the third semiconductor layer.

ABSTRACT

A semiconductor memory device includes a semiconductor substrate including a diode formed in an upper layer portion of the semiconductor substrate, a first insulating film provided above the semiconductor substrate, a first conductive film provided above the first insulating film and coupled to the diode, a stacked body provided above the first conductive film, an insulator and an electrode film being stacked alternately in the stacked body, a semiconductor member piercing the stacked body and being connected to the first conductive film, and a charge storage member provided between the electrode film and the semiconductor member.

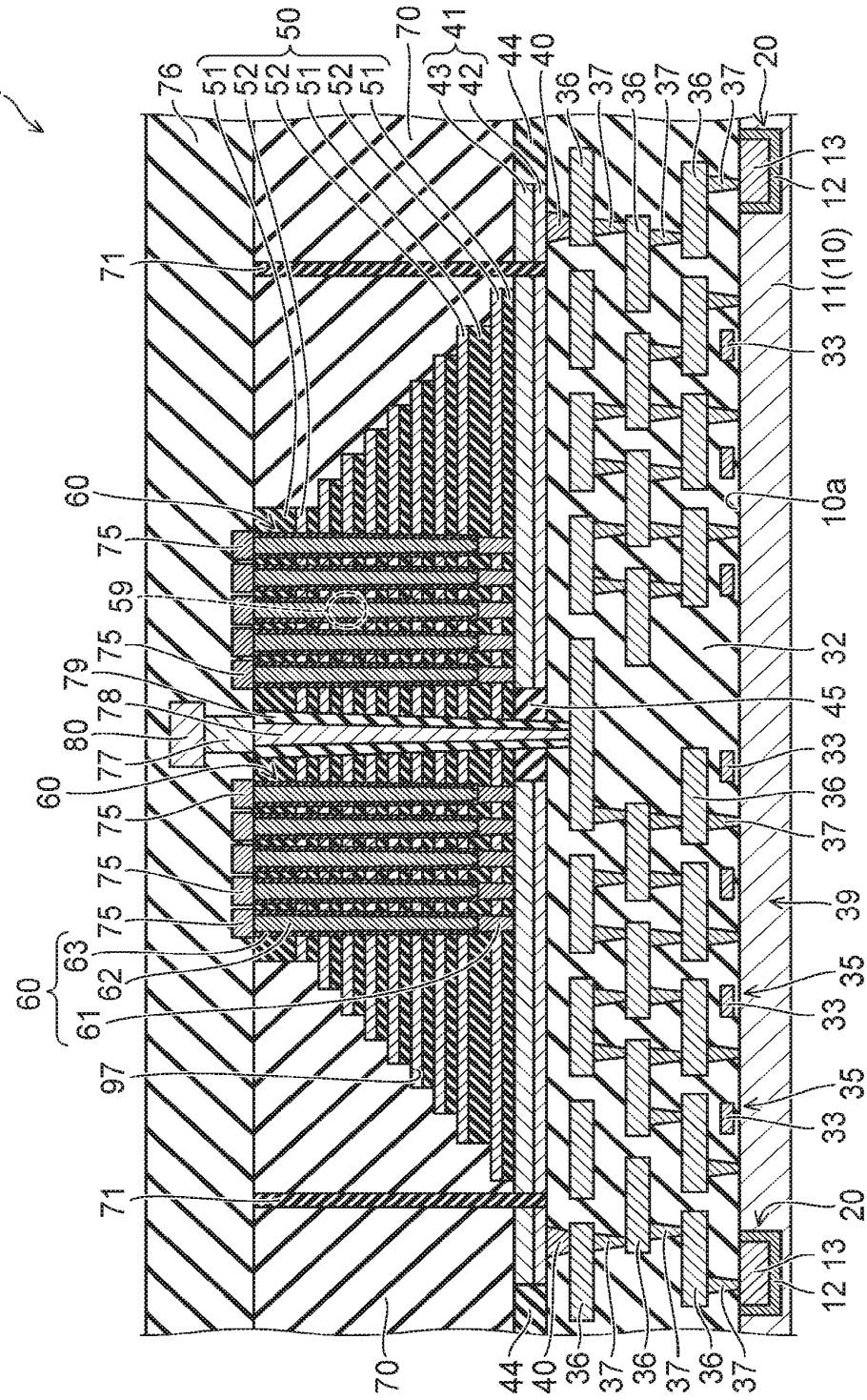


FIG. 1

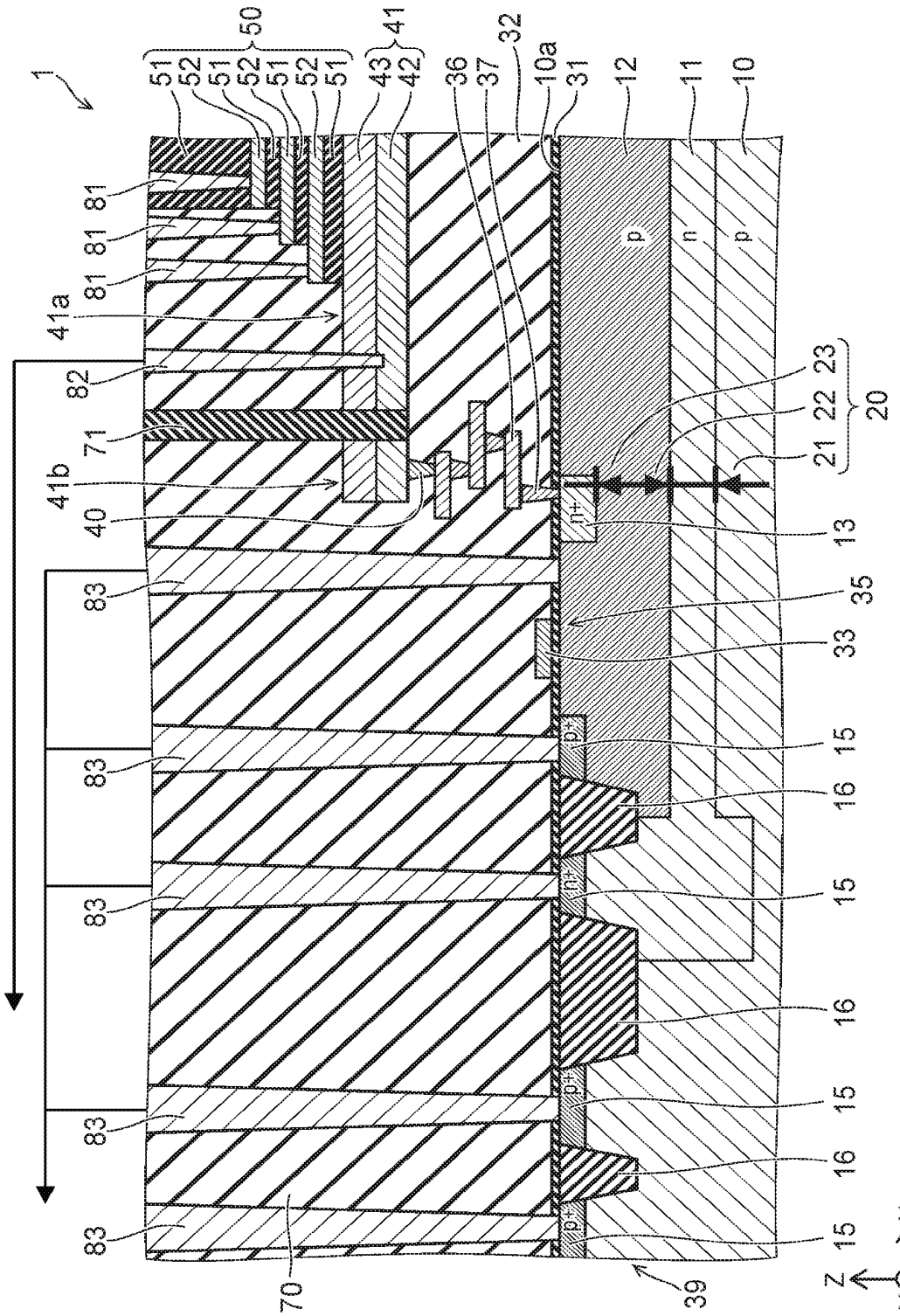

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FIG. 2

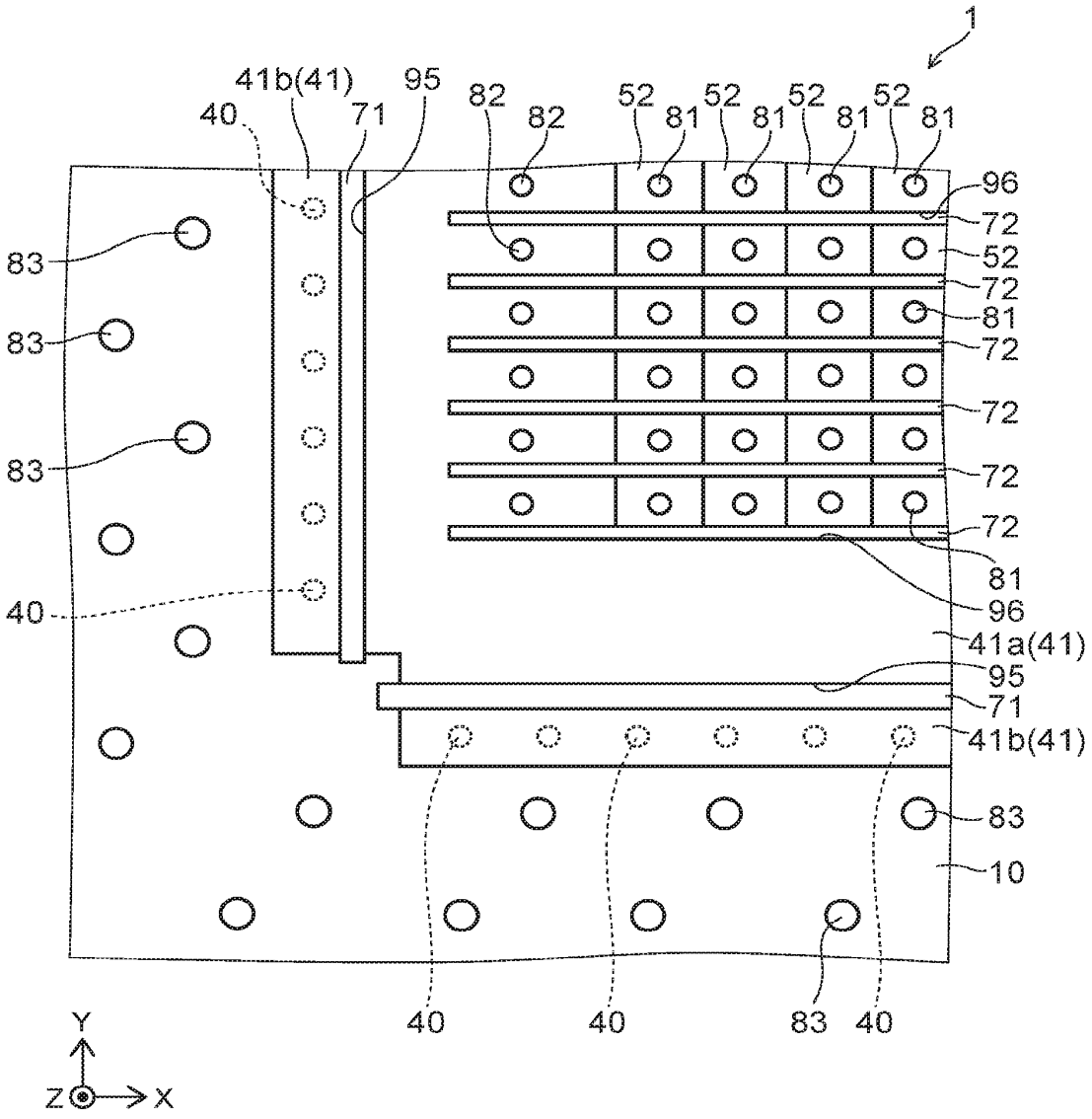
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FIG. 3

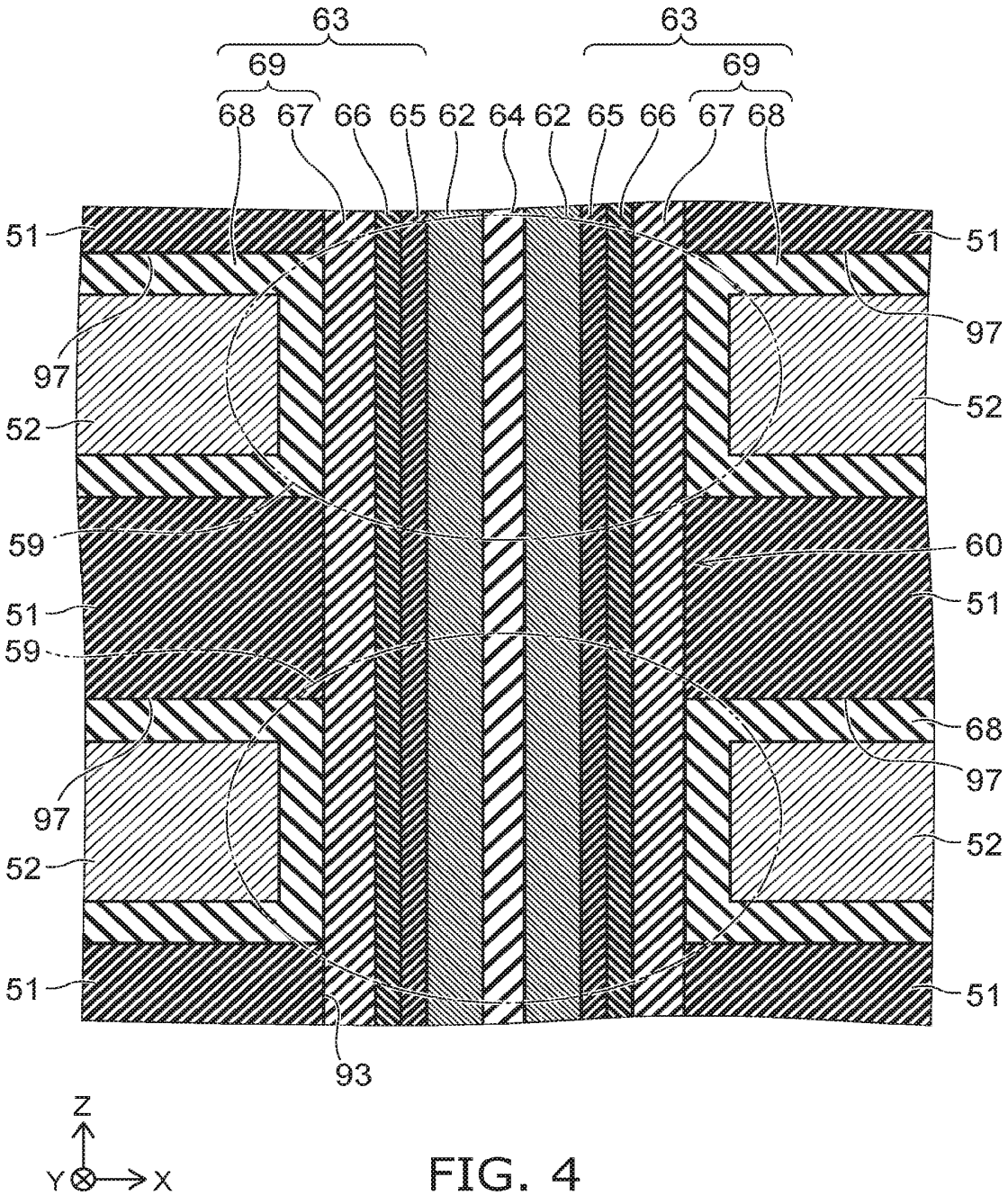
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FIG. 4

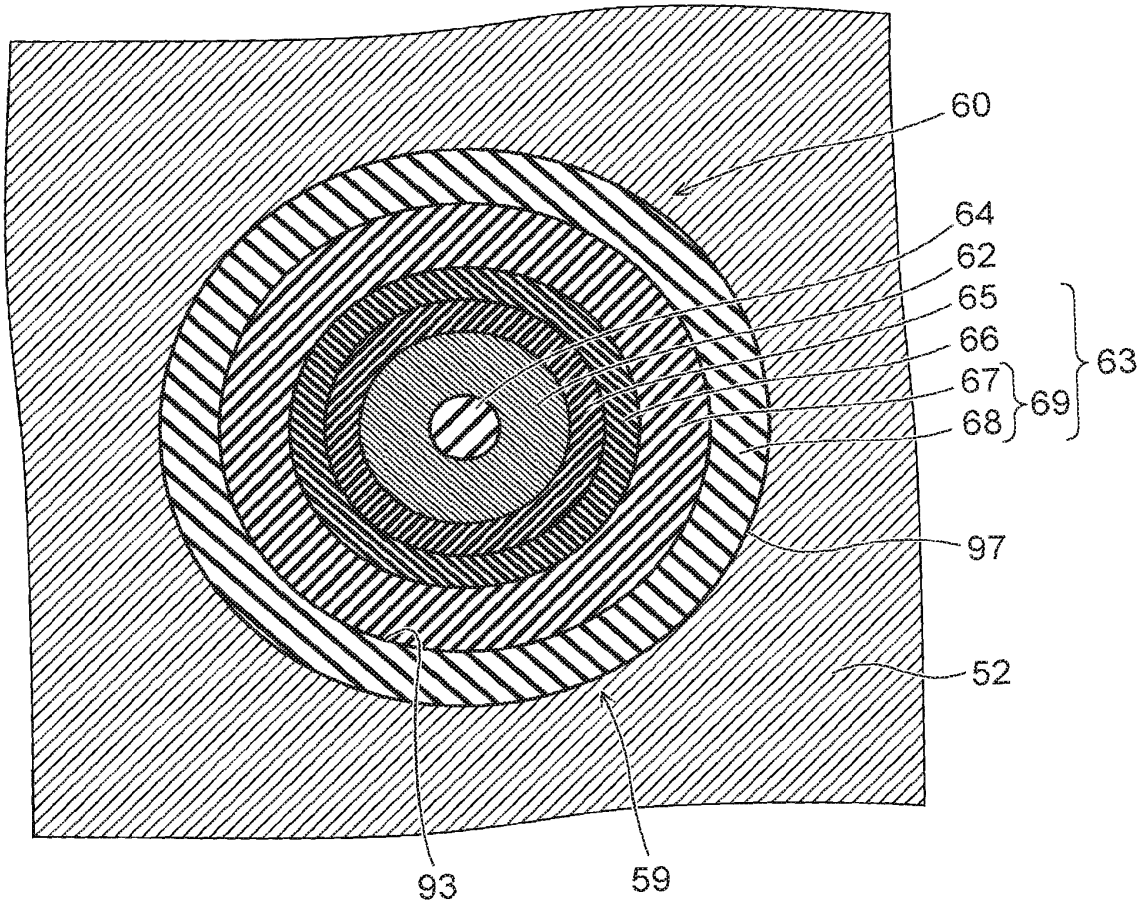
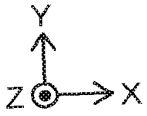


FIG. 5



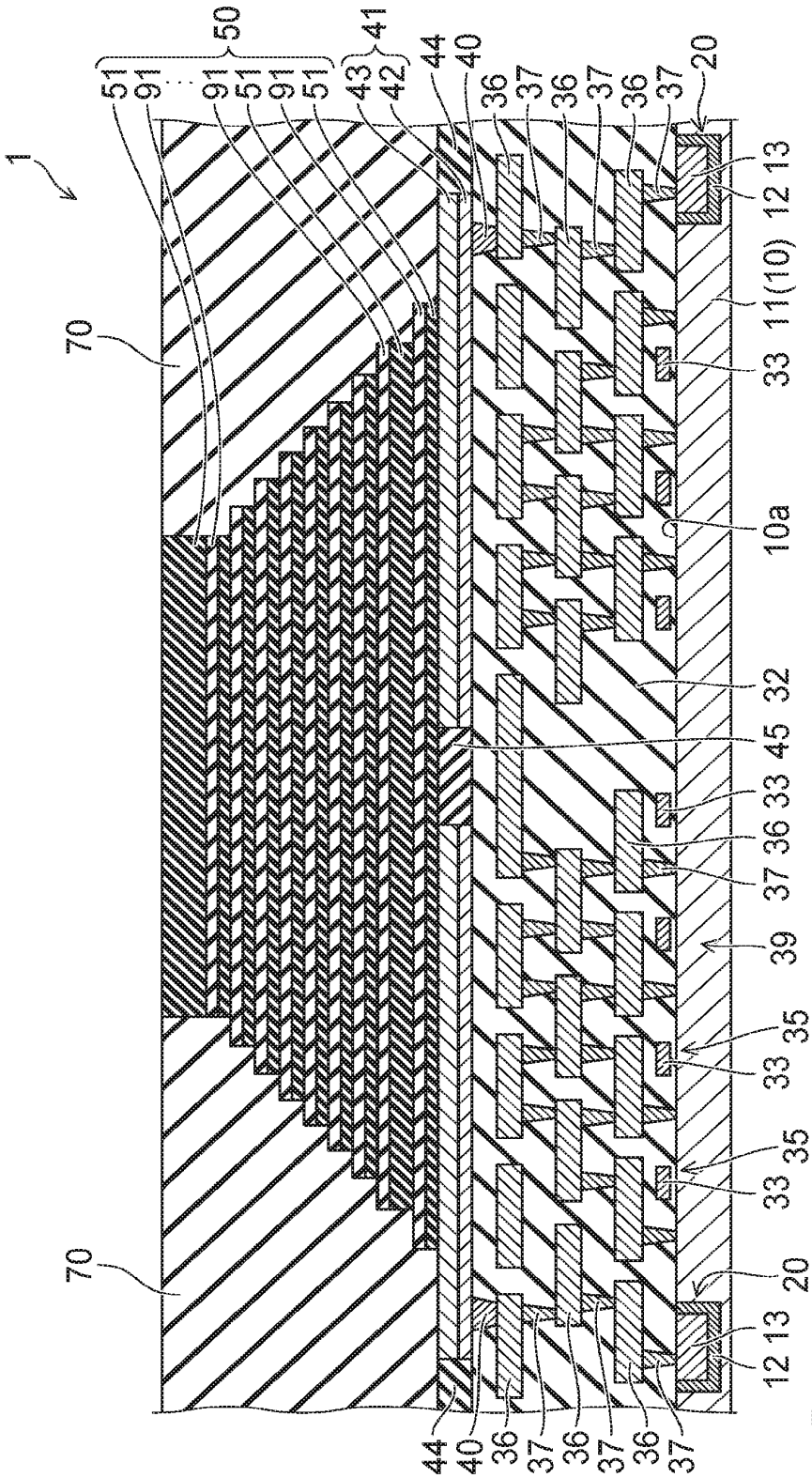


FIG. 6

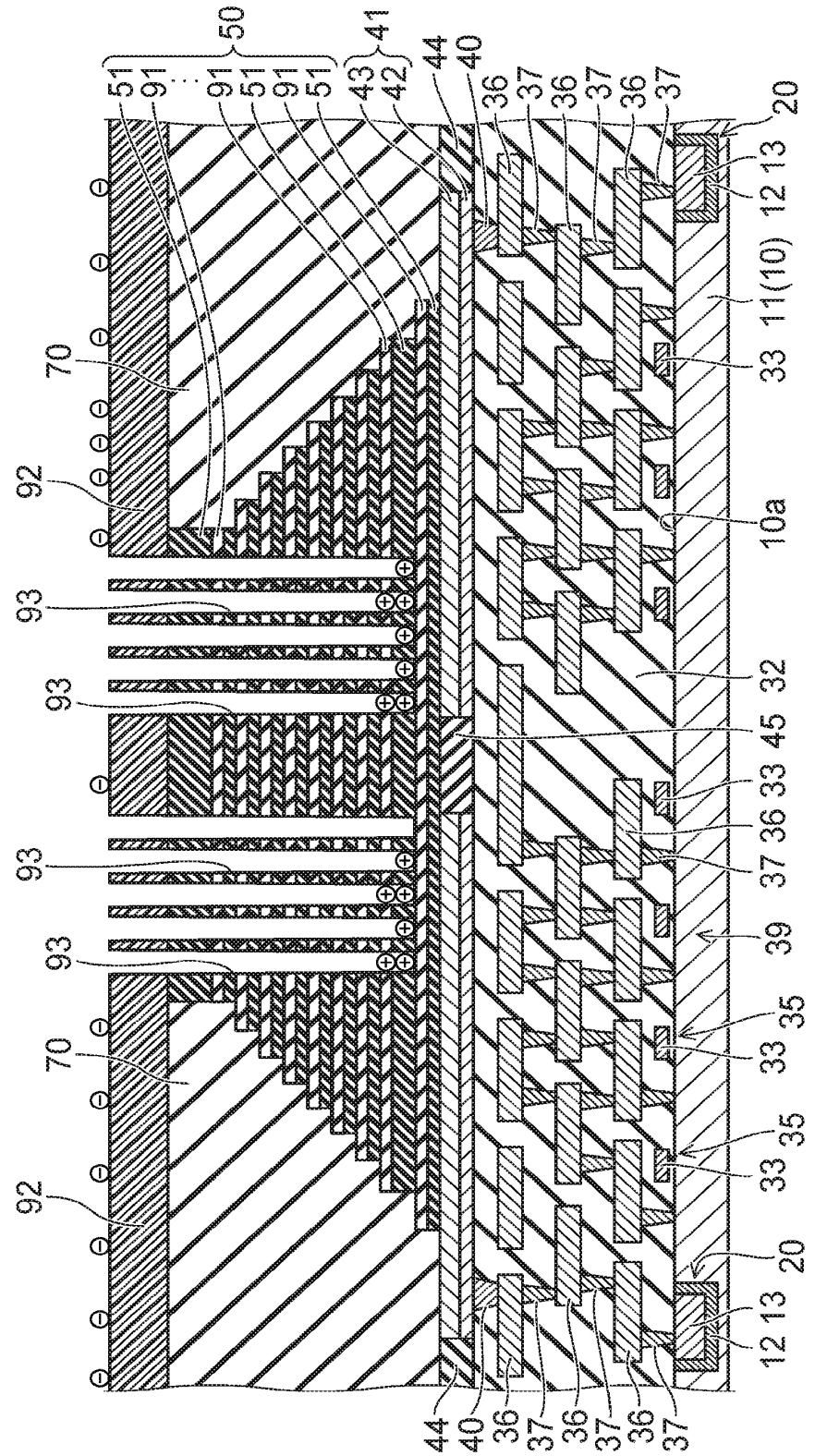
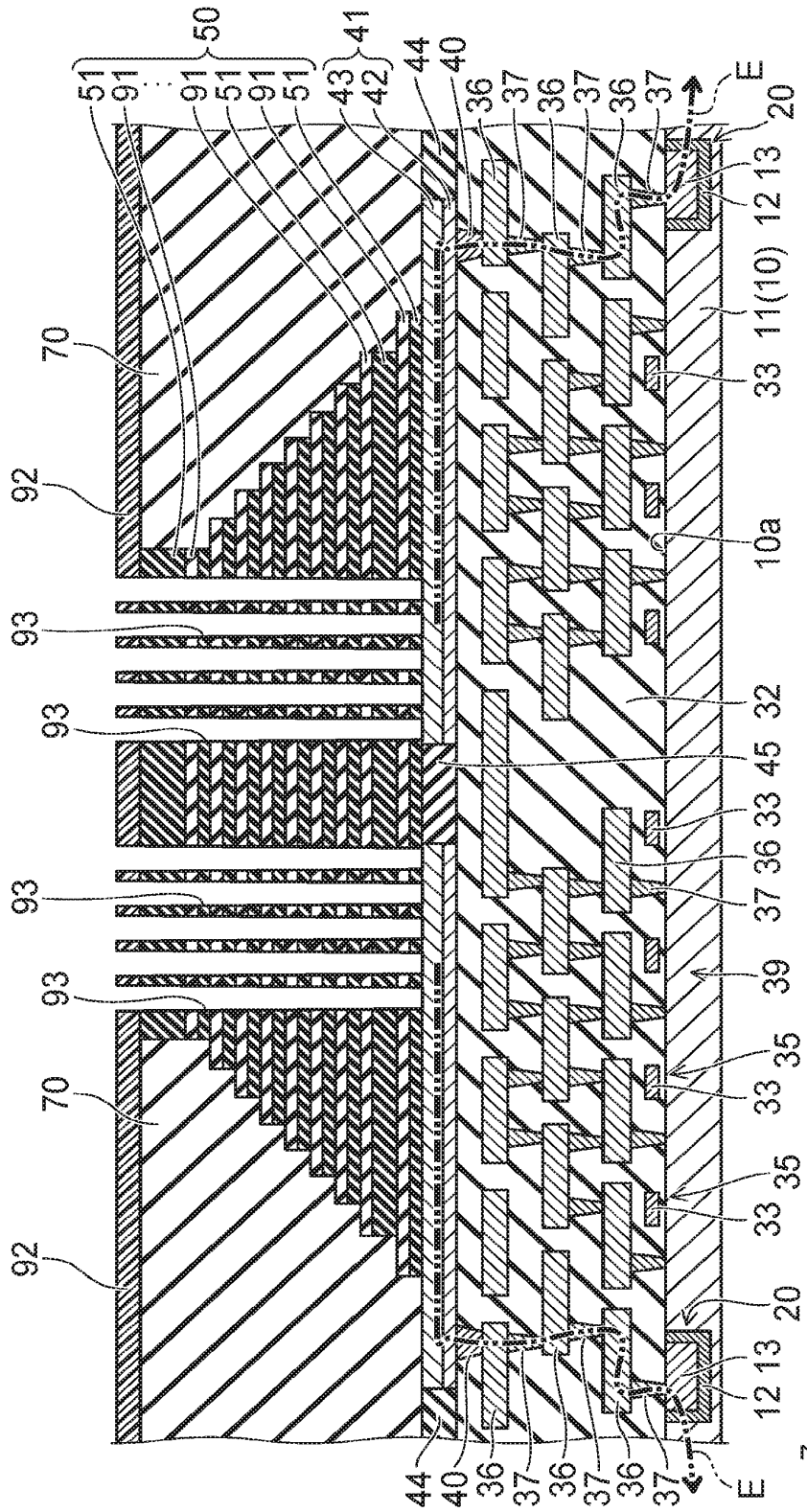


FIG. 7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51
91
43
42
44
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36
37
E
20
13
12
11(10)
33
70
92
10a
93
32
45
39
35
Z
X
Y

FIG. 8

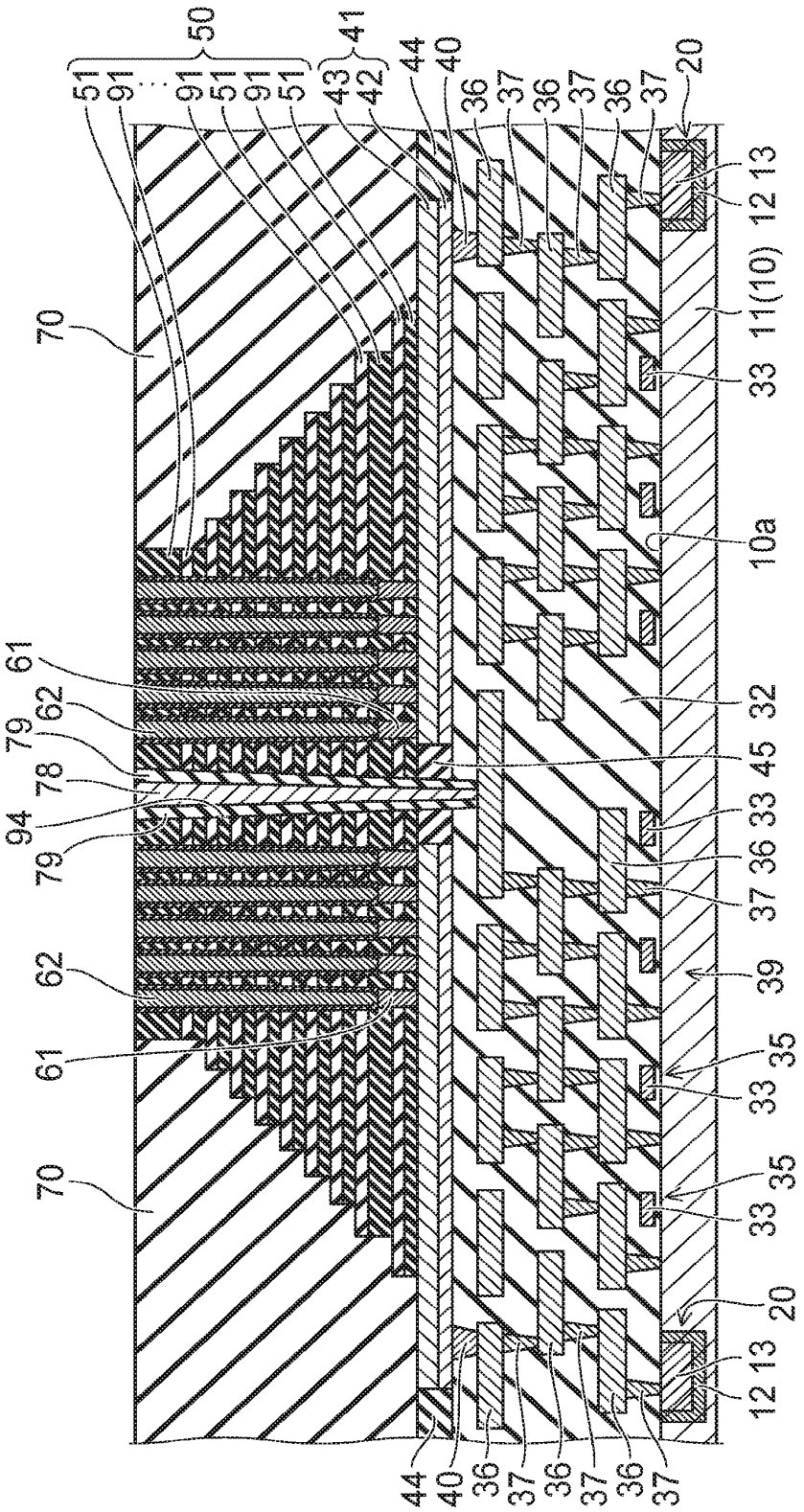


FIG. 9

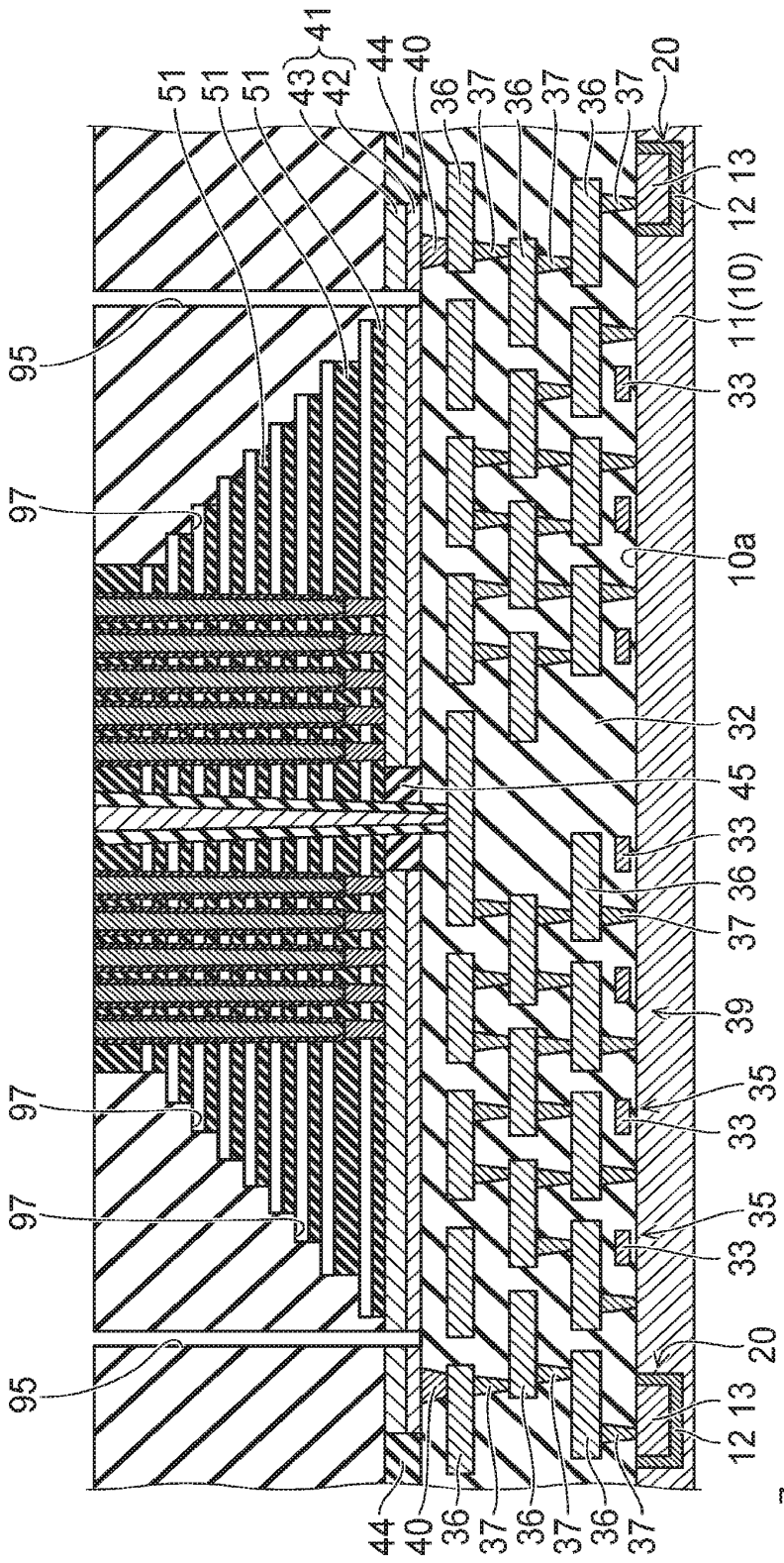


FIG. 10

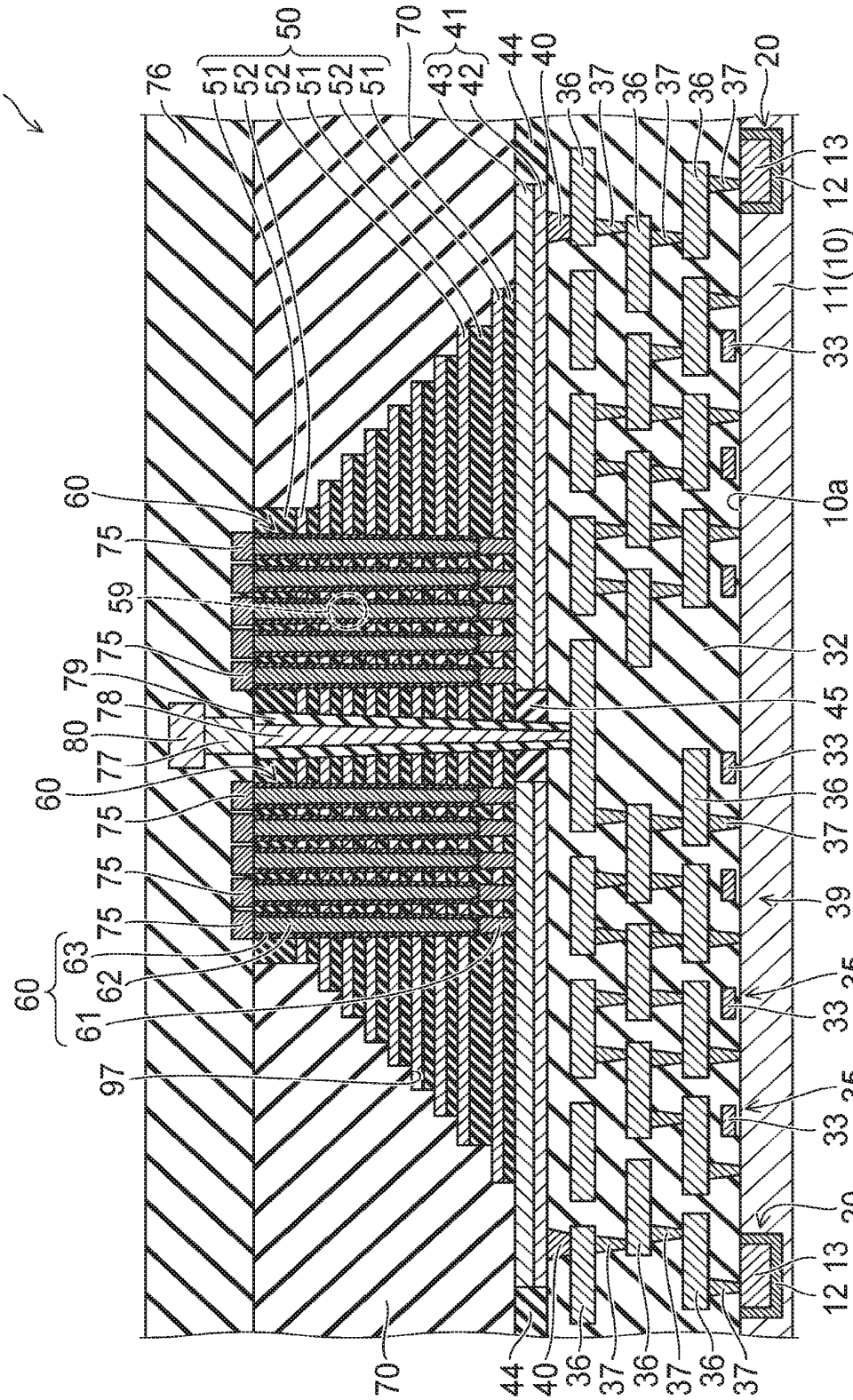


FIG. 11

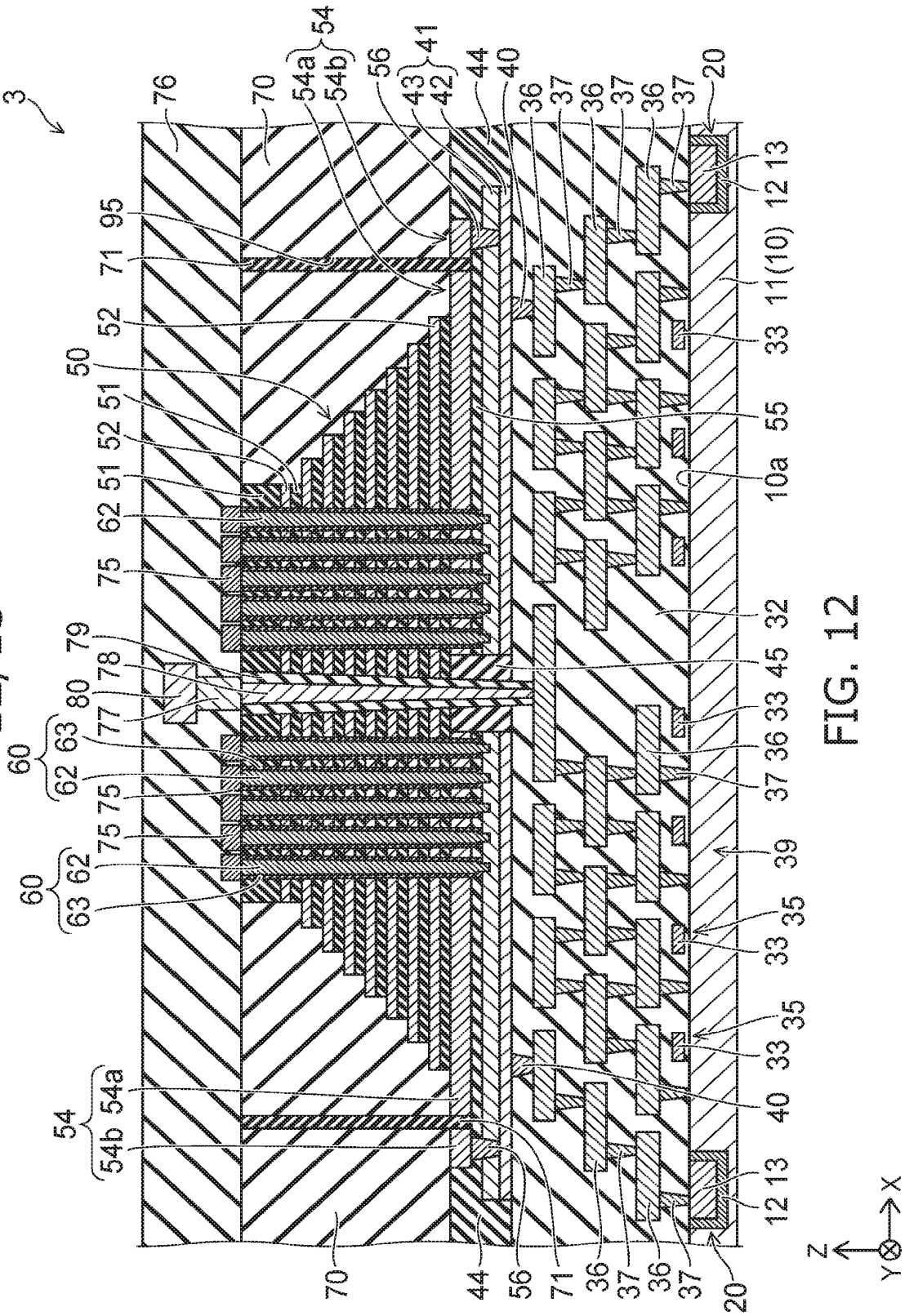
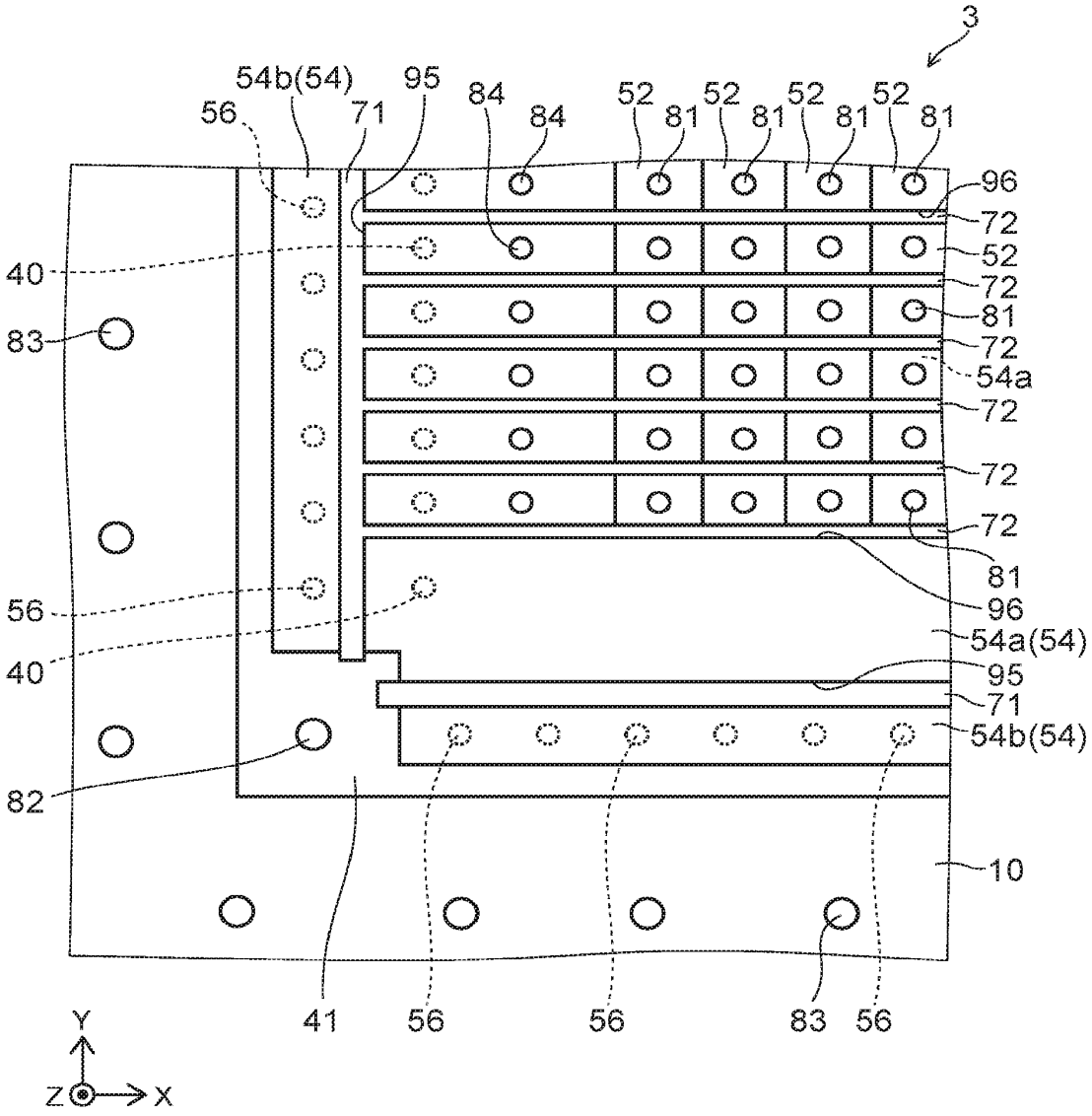


FIG. 12


3
54b(54)
95
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71
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72
54a
72
72
72
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96
54a(54)
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54b(54)
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82
10
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Z
X

FIG. 13

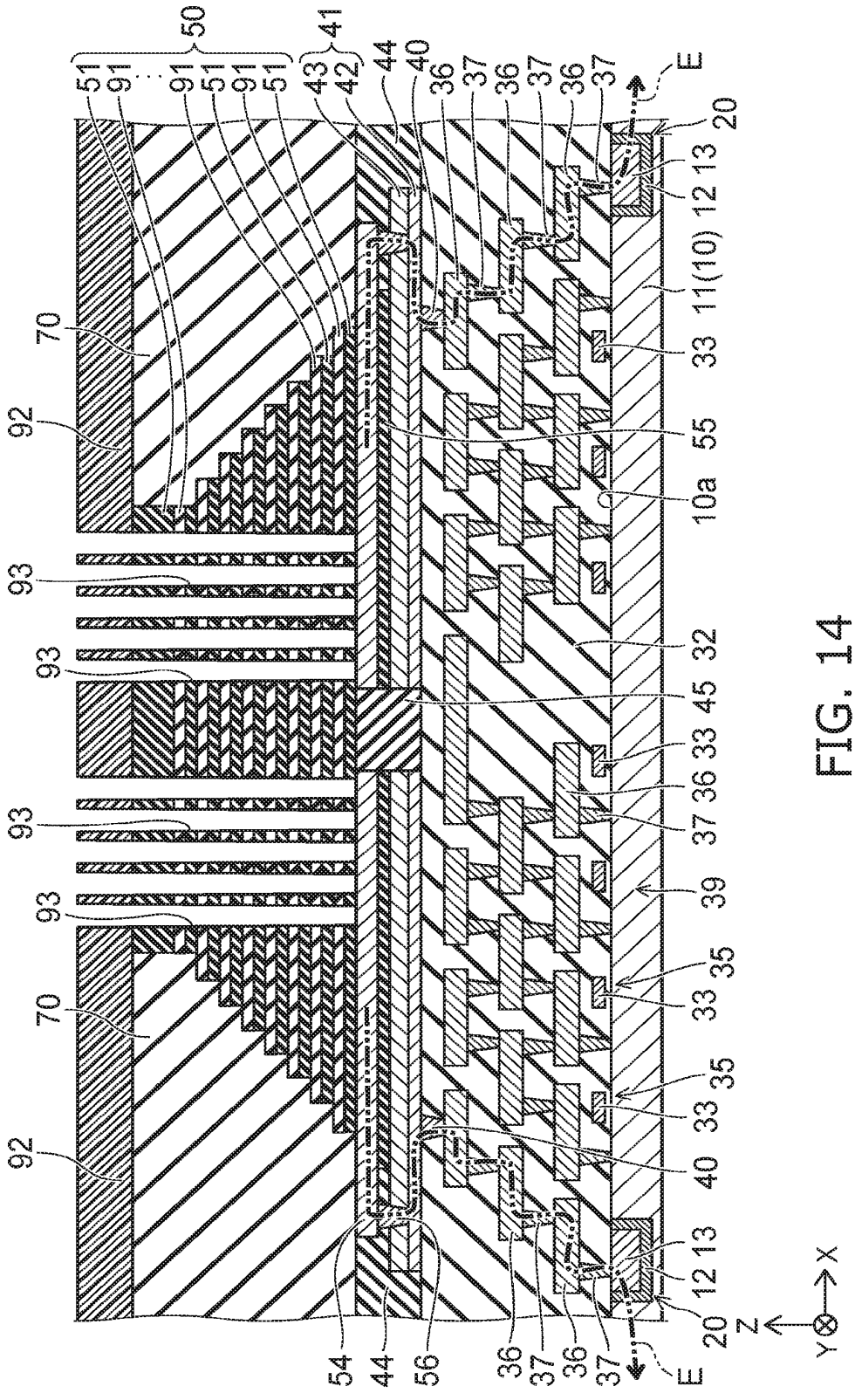


FIG. 14

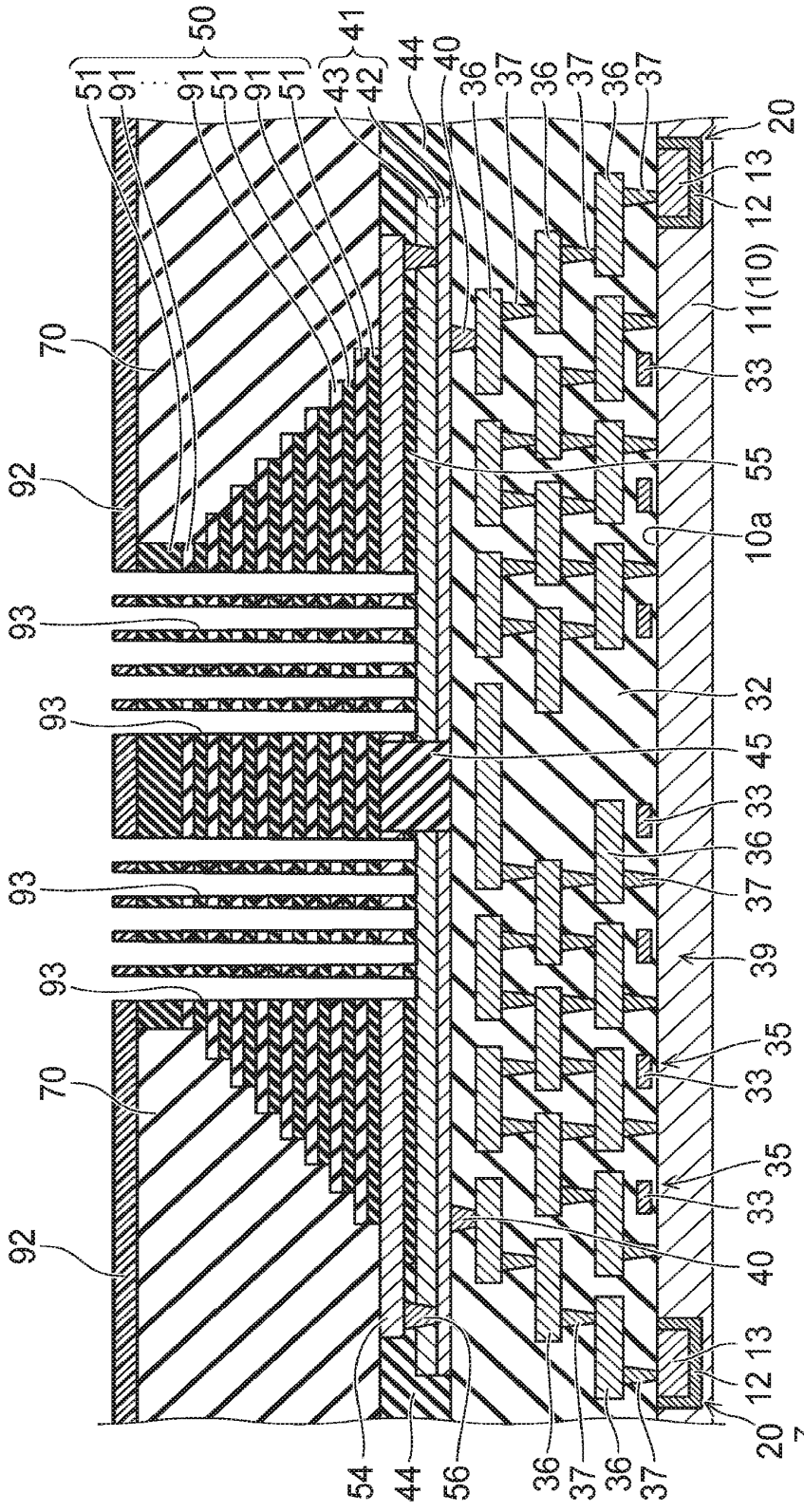


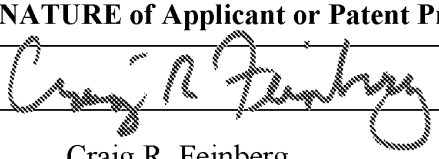
FIG. 15

TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5. If the Power of Attorney by Applicant form is not accompanied by this transmittal form or an equivalent, the Power of Attorney will not be recognized in the application.

Application Number	New Application
Patent Number	
Filing Date	Herewith
Issue Date	
First Named Inventor	Jun FUJIKI
Title	SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR MANUFACTURING SAME
Art Unit	
Examiner Name	
Attorney Docket Number	516693US

SIGNATURE of Applicant or Patent Practitioner

Signature		Date	9/12/2018
Name	Craig R. Feinberg	Telephone	703-413-3000
Registration Number	Registration No.: 62,116		

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications.

■ *Total of 1 forms are submitted.

POWER OF ATTORNEY BY APPLICANT

(ASSIGNEE, LEGAL REPRESENTATIVE OR PERSON WHO OTHERWISE SHOWS SUFFICIENT PROPRIETARY INTEREST)

I hereby revoke all previous powers of attorney given in the application identified in the attached Transmittal for Power of Attorney form.

■ I hereby appoint Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter:

22850

Please recognize or change the correspondence address for the above-identified patent to:

■ The address associated with the above-mentioned Customer Number.

I am the Applicant:

■ Assignee or Person to Whom the Inventor is Under an Obligation to Assign and am authorized to act on behalf of all assignees

☐ Person Who Otherwise Shows Sufficient *Proprietary* Interest (*e.g.*, a petition under 37 CFR 1.46 (b)(2) was granted in the application or is concurrently being filed with this document)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature		Date	July 6, 2017
Name	Michihito HATSUMI	Telephone	
Title	General Manager, Intellectual Property Division		
Company	Toshiba Memory Corporation		

NOTE: Signature - This form must be signed by the applicant. See 37 CFR 1.4 for signature requirements and certifications. Submit multiple forms for more than one signature, see below*.

■ *Total of 1 forms are submitted.

TMC

DR

Docket No. 516693US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF:	Jun FUJIKI, et al.	
SERIAL NO:	New Application	GAU:
FILED:	Herewith	EXAMINER:
FOR:	SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR MANUFACTURING SAME	

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

Commissioner:
Applicant(s) wish to disclose the following information.

REFERENCES

■ The applicant(s) wish to make of record the reference(s) listed on the attached form PTO-1449 and/or accompanying documents from a corresponding foreign application. Copies of the listed reference(s) are attached, where required, as are either statements of relevancy or any readily available partial or full English translations of pertinent portions of any non-English language reference(s). English abstract(s) and/or machine translation(s) may also be included for the cited foreign reference(s). Moreover, the machine translation process for such reference(s) may have included Optical Character Recognition (OCR) processing. Portions not captured by machine translation or OCR and remaining non-English words may have been manually translated. M.P.E.P. 609.04(III) states that there is no requirement "for translations to be verified." Accordingly, Applicant has not verified the accuracy of any such abstract, machine translation, and/or OCR processing. In lieu of a concise explanation of relevance of the cited foreign-language document, an English machine translation of the body of the document may be enclosed.

☐ Credit card payment is being made online (if electronically filed), or is attached hereto (if paper filed), in the amount required under 37 CFR §1.17(p).

CERTIFICATION

☐ Each item of information contained in this information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement.

☐ No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to the knowledge of the undersigned, having made reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this statement.

DEPOSIT ACCOUNT

■ Please charge any additional fees for the papers being filed herewith and for which no payment is enclosed herewith, or credit any overpayment to deposit account number **15-0030**.

Respectfully submitted,

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Form PTO 1449 (Modified)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY DOCKET NO. 516693US	SERIAL NO. New Application
LIST OF REFERENCES CITED BY APPLICANT		INVENTOR(S) Jun FUJIKI, et al.	
		FILING DATE Herewith	GROUP

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	AA	2011/0073866 A1	3/31/2011	KIM, Y. et al.			
	AB	2014/0085979 A1	3/27/2014	KONO, F.			
	AC	8,389,990 B2	3/5/2013	MIKAWA, T. et al.			
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						
	AM						
	AN						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION YES	TRANSLATION NO
	AO	2010-165794	7/29/2010	Japan (with English Abstract and Machine Generated English Translation)	X	
	AP					
	AQ					
	AR					
	AS					
	AT					
	AU					
	AV					

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)

	AW	
	AX	
	AY	
	AZ	☐ Additional References sheet(s) attached
Examiner		Date considered

*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Espacenet

Bibliographic data: JP2010165794 (A) — 2010-07-29

SEMICONDUCTOR MEMORY DEVICE

Inventor(s): ENDO MASATO; ARAI FUMITAKA ± (ENDO MASATO, ; ARAI FUMITAKA)

Applicant(s): TOSHIBA CORP ± (TOSHIBA CORP)

Classification: **- international:** ***H01L21/8247; H01L27/10; H01L27/115; H01L29/788; H01L29/792***

- cooperative:

Application number: JP20090005933 20090114 Global Dossier

Priority number(s): JP20090005933 20090114

Abstract of JP2010165794 (A)

PROBLEM TO BE SOLVED: To provide a semiconductor memory device capable of suppressing an influence of potentials of electrode layers, functioning as a control gate of a memory cell, on other regions. ;SOLUTION: The semiconductor memory device includes a laminate provided over a memory cell region and a peripheral circuit region on a semiconductor substrate 11 and formed by alternately laminating a plurality of electrode layers WL1 to WL5 and a plurality of insulating layers 24, a semiconductor layer 21 provided in a hole formed penetrating the laminate in the memory cell region and extending in the laminating direction of the laminate, a charge storage layer 17 provided between the semiconductor layer 21 and the electrode layers WL1 to WL5, a transfer transistor provided below the laminate in the peripheral circuit region and transferring a potential to the electrode layers WL1 to WL5, and a lower shield wiring layer SL1 provided between the transfer transistor and the bottom electrode layer WL1 and applied with a shield potential corresponding to the potential of a diffusion layer of the transfer transistor. ;COPYRIGHT: (C)2010,JPO&INPIT

Notice

CLAIMS JP2010165794

1.
A semiconductor substrate having a memory cell region and a peripheral circuit region; a stacked body provided over the memory cell region and the peripheral circuit region on the semiconductor substrate and having a plurality of electrode layers and a plurality of insulating layers alternately stacked A semiconductor layer provided in a hole formed through the laminate in the memory cell region and extending in a stacking direction of the electrode layer and the insulating layer; A transfer transistor provided under the stacked body in the peripheral circuit region and transferring a potential to the electrode layer; a transfer transistor provided between the transfer transistor and the lowermost layer of the electrode layer; And a lower shield wiring layer provided with a shield potential corresponding to the potential of the diffusion layer of the transfer transistor.

2.
A semiconductor substrate having a memory cell region and a peripheral circuit region; a stacked body provided over the memory cell region and the peripheral circuit region on the semiconductor substrate and having a plurality of electrode layers and a plurality of insulating layers alternately stacked A semiconductor layer provided in a hole formed through the laminate in the memory cell region and extending in a stacking direction of the electrode layer and the insulating layer; A transfer transistor provided under the stacked body in the peripheral circuit region and transferring a potential to the electrode layer; a transfer transistor provided between the transfer transistor and the lowermost layer of the electrode layer; A lower shield interconnection layer which is provided with a first shield potential corresponding to a potential of a diffusion layer of the transfer transistor, a second shield interconnection layer provided on the uppermost electrode layer, The semiconductor memory device characterized by a second

shield potential corresponding to the potential of the serial electrode layers and an upper shield wiring layers provided.

3.

3. The semiconductor memory device according to claim 1, wherein the lower shield interconnection layer is provided with the same potential as a potential of a diffusion layer of the transfer transistor located below the lower shield interconnection layer.

4.

An intermediate potential between the potential of the diffusion layer of the transfer transistor located under the lower shield interconnection layer and the potential of the electrode layer of the lowermost layer is applied to the lower shield interconnection layer Wherein said first and second memory cells are connected to each other.

5.

A semiconductor substrate having a memory cell region and a peripheral circuit region; a stacked body provided over the memory cell region and the peripheral circuit region on the semiconductor substrate and having a plurality of electrode layers and a plurality of insulating layers alternately stacked A semiconductor layer provided in a hole formed through the laminate in the memory cell region and extending in a stacking direction of the electrode layer and the insulating layer; And a top shield wiring layer provided on the uppermost electrode layer and provided with a shield potential corresponding to the potential of the electrode layer. Storage device.

Notice

DESCRIPTION JP2010165794

Kind Code: A1 A semiconductor memory device capable of suppressing the influence of a potential of an electrode layer functioning as a control gate of a memory cell on another region. SOLUTION: The semiconductor memory device of the present invention comprises a laminate in which a plurality of electrode layers WL1 to WL5 and a plurality of insulating layers 24 are provided alternately stacked over a memory cell region and a peripheral circuit region on a semiconductor substrate 11 , A semiconductor layer 21 provided in a hole formed through the stacked body in the memory cell region and extending in the stacking direction of the stacked body, and a charge accumulation provided between the semiconductor layer 21 and the electrode layers WL 1 to WL 5 A transfer transistor provided under the stacked body in the peripheral circuit region and transferring a potential to the electrode layers WL 1 to WL 5, a transfer transistor provided between the transfer transistor and the lowermost electrode layer WL 1, And a lower shield interconnection layer SL 1 to which a shield potential corresponding to the potential of the layer is applied. (FIG

Semiconductor memory device

[0001]

The present invention relates to a semiconductor memory device.

[0002]

In a MONOS (Metal-Oxide-Nitride-Oxide-Semiconductor) type nonvolatile semiconductor memory device using a silicon nitride film as a data storage layer (charge storage layer), it is possible to stack memory cells on a substrate Has been done.

For example, Patent Document 1 discloses a technique related to a nonvolatile semiconductor memory device having a structure in which a columnar semiconductor is provided in a direction perpendicular to a substrate main surface and a plurality of memory cells are connected in series in that direction. When the electrode layer functioning as the control gate of the memory cell is provided extending to the peripheral circuit region, depending on the potential of the electrode layer, the resistance of the diffusion layer of the transistor formed in the peripheral circuit region is increased, There is concern about the problem that it can not be done.

[0003]

Japanese Unexamined Patent Application Publication No. 2007-180389

[0004]

The present invention provides a semiconductor memory device capable of suppressing the influence of the potential of an electrode layer functioning as a control gate of a memory cell on other regions.

[0005]

According to an aspect of the present invention, there is provided a semiconductor device comprising: a semiconductor substrate having a memory cell region and a peripheral circuit region; a semiconductor substrate provided over a region of the memory cell region and the peripheral circuit region on the semiconductor substrate, A semiconductor layer provided in a hole formed through the laminate in the memory cell region and extending in a stacking direction of the electrode layer and the insulating layer; A charge storage layer provided between the semiconductor layer and the electrode layer; a transfer transistor provided below the stacked body in the peripheral circuit region to transfer a potential to the electrode layer; And a lower shield interconnection layer which is provided between the lower shield interconnection layer and the lower layer and to which a shield potential corresponding to the potential of the diffusion layer of the transfer transistor is applied That the semiconductor memory device is provided.

According to another aspect of the present invention, there is provided a semiconductor device comprising: a semiconductor substrate having a memory cell region and a peripheral circuit region; a semiconductor substrate provided over the memory cell region and the peripheral circuit region on the semiconductor substrate, A laminated body in which a plurality of insulating layers are alternately laminated; a laminated body which is provided in a hole formed through the laminated body in the memory cell region and extends in a laminating direction of the electrode layer and the insulating layer A charge storage layer provided between the semiconductor layer and the electrode layer; a transfer transistor provided below the stacked body in the peripheral circuit region to transfer a potential to the electrode layer; A lower shield interconnection layer which is provided between the transfer transistor and the electrode layer of the lowermost layer and to which a first shield potential corresponding to the potential of the diffusion layer of the transfer transistor is applied, Provided on the electrode layer, and the upper shield wiring layer a second shield potential corresponding to the potential of the electrode layer is provided, a semiconductor memory device characterized by comprising a are provided.

According to still another aspect of the present invention, there is provided a semiconductor device comprising: a semiconductor substrate having a memory cell region and a peripheral circuit region; a semiconductor substrate provided over the memory cell region and the peripheral circuit region on the semiconductor substrate, And a plurality of insulating layers are alternately stacked in a stacking direction of the stacked body and a stacked body which is provided in a hole formed through the stacked body in the memory cell region and which is provided in a stacking direction of the electrode layer and the insulating layer A charge accumulation layer provided between the semiconductor layer and the electrode layer; a charge storage layer provided on the electrode layer of the uppermost layer and provided on an upper portion to which a shield potential corresponding to the potential of the electrode layer is applied And a shield interconnection layer formed on the semiconductor substrate.

[0006]

According to the present invention, there is provided a semiconductor memory device which can suppress the influence of the potential of the electrode layer functioning as the control gate of the memory cell on other regions.

[0007]

FIG. 3 is a schematic diagram showing a planar positional relationship of main elements in a semiconductor memory device according to an embodiment of the present invention.

FIG. 2 is a schematic view corresponding to a cross section A - A in FIG. 1. FIG. 4 is a schematic view corresponding to a cross section taken along line B - B of FIG. 1; FIG. 2 is a schematic view corresponding to a cross section taken along the line C - C of FIG. 1. FIG. 4 is a schematic view corresponding to the D - D cross section in FIG. 1. FIG. 4 is a schematic diagram corresponding to the E - E cross section of FIG. 1; FIG. 4 is a schematic view corresponding to a cross section taken along line F - F in FIG. 1; FIG. 7 is a cross-sectional view similar to FIG. 2 in another embodiment. 7 is a cross-sectional view similar to FIG. 7 in the other embodiment. FIG. 7 is a cross-sectional view similar to FIG. 7 in yet another embodiment. FIG.

[0008]

Hereinafter, embodiments of the present invention will be described with reference to the drawings. Elements in common in each drawing are denoted by the same reference numerals. FIG. 1 is a schematic diagram showing a planar positional relationship of main elements in a semiconductor memory device according to an embodiment of the present invention. FIG. 2 is a view corresponding to a cross section A - A in FIG. 1. FIG. 3 is a view corresponding to the B - B cross section in FIG. 1. FIG. 4 is a view corresponding to a cross section taken along the line C - C in FIG. 1. FIG. 5 is a view corresponding to the D - D cross section in FIG. 1. FIG. 6 is a view corresponding to the E - E cross section in FIG. 1. FIG. 7 is a view corresponding to the section F - F in FIG. 1.

[0009]

In this specification, for convenience of description, an XYZ orthogonal coordinate system is introduced. In this coordinate system, two directions parallel to the upper surface (main surface) of the semiconductor substrate and orthogonal to each other are defined as X direction and Y direction, and a direction perpendicular to the main surface of the semiconductor substrate is defined as Z Direction.

[0010]

The semiconductor memory device according to the present embodiment includes a memory cell array 10 in which a plurality of memory cells are three-dimensionally arranged, a peripheral circuit 50 for writing data in the memory cell, an operation for reading out data stored in the memory cell, and the like On the same semiconductor substrate. FIG. 1 shows a row decoder for selecting an electrode layer which functions particularly as a control gate of a memory cell among peripheral circuits 50.

[0011]

First, memory cells will be described with reference to FIG. 2.

[0012]

For example, on the surface of a p-type silicon substrate (or p-type well layer) 11, n <-> type diffusion layers 12, 13 and n <+> type diffusion layer 14 are selectively formed.

The diffusion layer 14 is connected to the cell source CS. On the surface of the substrate 11 between the diffusion layer 12 and the diffusion layer 13, a source side selection gate SGS is provided via an insulating film 15. The source side selection gate SGS is made of, for example, amorphous or polycrystalline silicon. The diffusion layers 12 to 14, the insulating film 15, and the source side selection gate SGS constitute a source side selection transistor.

[0013]

On the diffusion layer 12, a memory string MS configured by connecting a plurality of memory cells MC in series in the Z direction is provided. By controlling the gate voltage applied to the source side selection gate SGS, it is possible to turn on and off between the memory string MS and the cell source CS.

[0014]

An interlayer insulating layer 19 is provided on the substrate 11, and a lower shield interconnection layer SL 1 (hereinafter also simply referred to as a shield interconnection layer) is provided on the interlayer insulating layer 19. On the shield interconnection layer SL 1, a multilayer body in which a plurality of insulating layers 24 and a plurality of electrode layers WL 1 to WL 5 are alternately laminated is provided. The number of layers of the electrode layers WL <b> 1 to WL <b> 5 is arbitrary, but in the present embodiment, for example, a case of five layers is exemplified.

[0015]

The shield wiring layer SL 1 and the electrode layers WL 1 to WL 5 are made of amorphous or polycrystalline silicon, for example. Alternatively, the shield wiring layer SL 1 may be made of metal silicide or metal having lower resistance.

[0016]

A drain side selection gate SGD is provided on the uppermost insulating layer 24 on the laminate, and insulating layers 25, 26 are provided thereon. The drain side selection gate SGD is made of amorphous or polycrystalline silicon, for example. In addition, the upper surface of the insulating layer 26 is covered with the insulating film 18.

[0017]

A through hole that extends in the Z direction and reaches the diffusion layer 12 is formed in the laminate, and the insulating film 16, the charge storage layer 17, the insulating film 18, and the semiconductor layer 21 are provided on the side wall of the through hole .

[0018]

For example, the insulating film 16 is a silicon oxide film, the charge storage layer 17 is a silicon nitride film, and the insulating layer 18 is a silicon oxide film, which constitute a so-called ONO (Oxide-Nitride-Oxide) film.

The semiconductor layer 21 is, for example, n <-> -type silicon. The semiconductor layer 21 is in contact with the diffusion layer 12 at the bottom of the through hole.

[0019]

A portion where the semiconductor layer 21 and each of the electrode layers WL 1 to WL 5 are opposed to each other with the ONO film interposed therebetween forms a memory cell MC, the semiconductor layer 21 functions as a channel in the memory cell MC, each of the electrode layers WL 1 to WL 5 is a control gate , And the charge accumulation layer 17 functions as a data storage layer that accumulates charges injected from the semiconductor layer 21.

[0020]

The memory cell MC is a memory cell having a charge trap structure, and the charge storage layer 17 has many traps for trapping charges (electrons), and is made of, for example, a silicon nitride film.

The insulating film 18 between the charge storage layer 17 and the semiconductor layer 21 is formed such that when charges are injected from the semiconductor layer 21 into the charge storage layer 17 or charges accumulated in the charge storage layer 17 diffuse into the semiconductor layer 21 In this case, it becomes a potential barrier. The insulating film 16 between the charge storage layer 17 and each of the electrode layers WL <b> 1 to WL <b> 5 prevents the charge accumulated in the charge storage layer 17 from diffusing into the electrode layers WL <b> 1 to WL <b> 5. A plurality of memory cells MC corresponding to the number of electrode layers WL 1 to WL 5 are connected in series in the Z direction to constitute a memory string MS.

[0021]

On the top of the semiconductor layer 21, a p <-> type semiconductor layer 22 and an n <+> type semiconductor layer 23 are provided by ion implantation, respectively. The drain side selection gate SGD faces the semiconductor layer 22 with the

insulating film 18 interposed therebetween, and thereby constitutes a drain side selection transistor.

[0022]

A portion provided on the upper surface of the insulating film 18 in the semiconductor layer 23 is metal silicided, and this portion is connected to the bit line BL. On / off control between the memory string MS and the bit line BL can be controlled by controlling the gate voltage applied to the drain side selection gate SGD.

[0023]

An insulating layer 28 is buried inside the semiconductor layers 21 to 23, and an interlayer insulating layer 27 is also provided thereon and around the cell source CS. Further, the end of the shield wiring layer SL 1, the electrode layers WL 1 to WL 5, and the drain side selection gate SGD on the side opposite to the memory string MS is metal-silicided to reduce the resistance.

[0024]

The laminated body including the shield wiring layer SL 1, the insulating layer 24, and the electrode layers WL 1 to WL 5 described above extends to the peripheral circuit region. These stacked bodies are shown as word lines WL in the plan view of FIG.

[0025]

In the peripheral circuit region, a transfer transistor for transferring a potential to each of the electrode layers WL <b> 1 to WL <b> 5 and the shield wiring layer SL <b> 1 is provided. For example, FIG. 1 shows a region where a transfer transistor 20 for transferring a potential to the electrode layer WL 2, a transfer transistor 30 for transferring a potential to the electrode layer WL 1, and a transfer transistor 40 for transferring a potential to the shield interconnection layer SL 1 are formed Respectively.

[0026]

FIG. 5 corresponding to the D - D cross section in FIG. 1 shows the sectional structure of the portion where the transfer transistor 20 is formed.

[0027]

Transfer transistor 20 includes n <-> type diffusion layers 33 a, 33 b selectively formed on the surface of substrate 11, n <+> type diffusion layers 34 a, 34 b, diffusion layer 33 a and diffusion layer 33 b A gate insulating film 32 provided on the surface of the substrate 11 between the gate insulating film 32 and the gate electrode 31 provided thereon.

The region in which they are formed is shown as the active region 60 of the transfer transistor 20 in FIG. The diffusion layer formed on the surface of the substrate 11 is separated from the diffusion layers of other transistors and elements by an insulating layer 35 having a STI (Shallow Trench Isolation) structure, for example.

[0028]

A wiring 39 is provided on the stacked body with an insulating layer 29 interposed therebetween, and the diffusion layer 34 a of the transfer transistor 20 is connected to the wiring 39 via the contact portion 36. The diffusion layer 34 b is connected to the electrode layer WL 2 via the contact portions 38 and 41.

[0029]

As shown in FIG. 4 corresponding to the C - C cross section in FIG. 1, the electrode layers WL 1 to WL 5 and the shield wiring layer SL 1 are formed stepwise in the peripheral circuit region. Each of the electrode layers WL 1 to WL 5 and the shield wiring layer SL 1 is formed in a stepwise shape and is connected to a corresponding transfer transistor via a contact portion.

[0030]

For example, the electrode layer WL 2 is connected to the diffusion layer 34 b of the transfer transistor 20 via the contact portion 41 and the contact portion 38 shown in FIG. 5. The electrode layer WL 1 is connected to the diffusion layer 34 b of the transfer transistor 30 via the contact portion 42 and the contact portion 38 shown in FIG. 6. The shield wiring layer SL 1 is connected to the diffusion layer 34 b of the transfer transistor 40 via the contact portion 43 and the contact portion 38 shown in FIG. 7.

[0031]

The stepped portion connected to the transfer transistor in each of the electrode layers WL 1 to WL 5 and the shield interconnection layer SL 1 is metal silicided and has low resistance.

[0032]

In the transfer transistor 20 shown in FIG. 5, when a predetermined gate voltage is applied to the gate electrode 31 via the gate wiring 37, the diffusion layers 34 a and 34 b are conducted to each other, and are applied to the diffusion layer 34 a via the wiring 39 and the contact portion 36 Is transferred to the diffusion layer 34 b.

The potential of the diffusion layer 34 b is transferred to the electrode layer WL 2 through the contact portions 38 and 41.

[0033]

FIG. 6 corresponding to the EE section in FIG. 1 shows a cross-sectional structure of the portion where the transfer transistor 30 is formed.

[0034]

Similarly for this transfer transistor 30, n <-> type diffusion layers 33a, 33b selectively formed on the surface of the substrate 11, n <+> type diffusion layers 34a, 34b, diffusion layer 33a and diffusion A gate insulating film 32 provided on the surface of the substrate 11 between the gate electrode 31 and the gate electrode 31, and a gate electrode 31 provided on the gate insulating film 32.

The region in which they are formed is shown as the active region 60 of the transfer transistor 30 in FIG.

[0035]

In the transfer transistor 30, when a predetermined gate voltage is applied to the gate electrode 31 through the gate wiring 37, the diffusion layers 34 a and 34 b are conducted, and the potential applied to the diffusion layer 34 a via the wiring 39 and the contact portion 36 Is transferred to the diffusion layer 34 b. The potential of the diffusion layer 34 b is transferred to the electrode layer WL 1 through the contact portions 38 and 42.

[0036]

FIG. 7 corresponding to the F - F cross section in FIG. 1 shows a cross sectional structure of a portion where the transfer transistor 40 is formed.

[0037]

Similarly for this transfer transistor 40, n <-> type diffusion layers 33 a, 33 b selectively formed on the surface of the substrate 11, n <+> type diffusion layers 34 a, 34 b, diffusion layer 33 a and diffusion A gate insulating film 32 provided on the surface of the substrate 11 between the gate electrode 31 and the gate electrode 31, and a gate electrode 31 provided on the gate insulating film 32.

The region in which they are formed is shown as the active region 60 of the transfer transistor 40 in FIG.

[0038]

In the transfer transistor 40, when a predetermined gate voltage is applied to the gate electrode 31 via the gate wiring 37, the diffusion layers 34 a and 34 b are conducted, and the potential applied to the diffusion layer 34 a via the wiring 39 and the contact portion 36 Is transferred to the diffusion layer 34 b. The potential of the diffusion layer 34 b is transferred to the shield wiring layer SL 1 via the contact portions 38 and 43.

[0039]

The semiconductor memory device according to the present embodiment is a nonvolatile semiconductor memory device that can electrically erase and write data electrically and can hold stored contents even when the power supply is turned off.

[0040]

Here, a memory cell (cell to be written) having a control gate of any electrode layer (here, for example, the electrode layer WL 2) in the block (selected block) surrounded by the dotted line in FIGS. 1, in which electrons are injected into the charge storage layer to write data.

[0041]

0 V is applied to the selected bit line BL connected to the writing target cell (including the memory string including the same), and Vdd (for example, about several volts) is applied to the other unselected bit lines BL.

The drain side selection transistor connected to the write target cell is turned on and the source side selection transistor connected to the write target cell is turned off.

Vdd is given to the cell source. 0 V is applied to the substrate 11 or the p-type well layer. Vpgm (eg, about 20 V) is applied to the electrode layer WL 2 which is the control gate of the cell to be programmed, and Vpass (about 10 V, for example) is applied to

the other electrode layers. That is, to the electrode layer WL 2 of the selected block, the write potential Vpgm given to the wiring 39 is transferred and applied by the transfer transistor 20 shown in FIG. 5.

[0042]

As a result, 0 V of the selected bit line BL propagates to the channel (semiconductor layer 21) of the cell to be written, and the intensity of the electric field applied to the ONO film between the channel and the electrode layer WL 2 of the cell to be written becomes stronger , Electrons are injected into the charge storage layer 17 of the cell to be written, and data writing is performed.

[0043]

A desired shielding potential according to the potentials of the diffusion layers 34a and 34b of the transfer transistor below the shield interconnection layer SL1 and the potential of the lowermost electrode layer WL1 is applied to the shield interconnection layer SL1.

Table 1 shows an example of the potentials of the electrode layers WL <b> 1 to WL <b> 5 and the potential of the shield wiring layer SL <b> 1.

[0044]

[0045]

Vpgm is a voltage sufficient to perform data writing (electron injection) in the cell to be written, and is, for example, about 20 V.

Vpass is a voltage which prevents writing to the non-writing object cell and Vpgm at the unselected bit line is set to the channel region of the cell such that writing is not performed on the memory cell having the electrode layer as the control gate , And it is, for example, about 10 V.

[0046]

In the semiconductor memory device according to the present embodiment, in order to effectively utilize the substrate area, a transfer transistor is provided under a portion extending to the peripheral circuit region in the electrode layers WL 1 to WL 5. That is, as shown in FIG. 1, the word line WL including the electrode layers WL 1 to WL 5 extends so as to cross over the active region 60 of the transfer transistor.

[0047]

In such a structure, depending on the potential of the electrode layer existing above the active region 60, the n <-> type diffusion layers 33a, 33b of the transfer transistor therebelow has high resistance, and in some cases, the reverse conductivity type inversion A layer may be formed and it may be impossible to transfer charges.

[0048]

In contrast, in the present embodiment, the shield interconnection layer SL 1 is provided between the lowermost electrode layer WL 1 and the transfer transistor, and a desired shield potential is applied to the shield interconnection layer SL 1.

As a result, the influence of the electrode layer potential on the n <-> type diffusion layers 33a and 33b of the transfer transistor is blocked, and the resistance rise of the n <-> type diffusion layers 33a and 33b can be suppressed.

[0049]

Table 1 shows potential examples of the electrode layers WL1 to WL5 and the shield wiring layer SL1 above the transfer transistor when the transfer transistor transfers, for example, Vpgm to an arbitrary electrode layer.

[0050]

When Vpgm is transferred to the electrode layer WL1 of the lowermost layer by the transfer transistor, for example, the same Vpgm is given to the shield wiring layer SL1.

This makes it possible to suppress the electron density reduction or the formation of the inversion layer particularly on the surface side of the n <-> type diffusion layers 33 a and 33 b of the transfer transistor, and to suppress the resistance rise of the diffusion layers 33 a and 33 b.

[0051]

Vpgm is transferred to, for example, the electrode layer WL 2 by the transfer transistor, and when the potential applied to the lowermost layer WL 1 is Vpass, in order to suppress the resistance of the diffusion layers 33 a and 33 b from increasing, similarly to the above, in the shield wiring layer SL 1 Gives Vpgm. Alternatively, Vpg mL lower than Vpgm is shielded to such an

extent that the resistance in the diffusion layers 33a, 33b does not cause a problem in order to ensure the withstand voltage of the insulating layer between the lowest electrode layer WL1 to which Vpass is given and the shield wiring layer SL1 May be provided to the wiring layer SL 1.

[0052]

For example, Vpgm is transferred to the electrode layer WL 3 by the transfer transistor, and when the potential applied to the lowermost electrode layer WL 1 is 0 V, in order to suppress the resistance of the diffusion layers 33 a and 33 b from increasing, similarly to the above case, the shield wiring layer Give Vpgm to SL1. Also in this case, in order to ensure the withstand voltage of the insulating layer between the lowest layer electrode layer WL 1 to which 0 V is applied and the shield wiring layer SL 1, the resistance of the diffusion layers 33 a and 33 b is set to be higher than Vpgm The lowered Vpg mL may be applied to the shield wiring layer SL 1.

[0053]

Since the shield interconnection layer SL 1 does not function as a control gate of the memory cell, it is possible to design with only the low resistance without considering the transistor characteristics such as a threshold value. From such a viewpoint, the shield wiring layer SL 1 is not limited to a semiconductor, and may be formed of a compound of a metal and a semiconductor, or a metal.

[0054]

Next, another embodiment of the present invention will be described with reference to FIGS. FIG. 8 is a cross-sectional view of the memory cell array portion corresponding to FIG. 2 of the embodiment described above, and FIG. 9 is a cross-sectional view of the row decoder portion corresponding to FIG.

[0055]

In the present embodiment, an upper shield interconnection layer SL 2 (hereinafter also simply referred to as a shield interconnection layer) is provided between the uppermost electrode layer WL 5 and the drain side selection gate SGD. In the shield wiring layer SL 2, the desired shield potential applied to the wiring 39 is transferred via the contact portions 36, 38, 44 by the transfer transistor 70 shown in FIG. 9.

[0056]

For example, when high voltage Vpgm is applied to the uppermost electrode layer WL 5 to perform writing, the selected bit line connected to the memory string including the cell to be written is set at 0 V, and 0 V is applied to the channel of the cell to be written, is performed.

[0057]

In the unselected memory string not including the cell to be written, the connection to the bit line is cut off by turning off the drain side selection gate, the channel potential is raised by the boost ratio, and the voltage is applied to the electrode layer WL 5 to which Vpgm is applied An electric field in which electron injection is performed does not act so that writing to nonselected cells is not performed.

At this time, a high voltage is applied between the source and the drain of the drain side selection gate in the unselected memory string, and there is a concern that erroneous writing to unselected cells occurs due to GIDL (Gate Induced Drain Leakage) phenomenon.

[0058]

On the other hand, in this embodiment, the shield interconnection layer SL 2 is provided between the electrode layer WL 5 of the uppermost layer and the drain side selection gate SGD, the shield interconnection layer SL 2 is provided with the shield interconnection layer SL 2 corresponding to the potential of the uppermost layer electrode layer WL 5 By providing a desired potential, the potential difference between the source and the drain of the drain side selection gate SGD can be relaxed, and erroneous writing by GIDL can be suppressed.

[0059]

Table 2 shows potential examples of the electrode layers WL 1 to WL 5 and the upper shield wiring layer SL 2 in the unselected memory string.

[0060]

[0061]

When the potential of the uppermost electrode layer WL 5 is 0 V, since no high voltage is applied between the source and the drain of the drain side selection gate SGD, GIDL does not occur and the potential applied to the shield wiring layer SL 2 is sufficiently 0 V .

[0062]

In the case where Vpass (for example, about 10 V) is applied to the electrode layer WL 5, in order to reduce the electric field between the source and the drain of the drain side selection gate SGD and suppress the occurrence of GIDL, several V to VpassL lower than Vpass are applied to the shield wiring layer SL2.

At this time, the potential applied to the shield interconnection layer SL 2 can be lowered to such an extent that the electrode layer WL 5 is not deteriorated by GIDL.

[0063]

In the case where Vpgm (eg, about 20 V) is applied to the electrode layer WL 5, in order to reduce the electric field between the source and the drain of the drain side selection gate SGD and suppress the generation of GIDL, similarly to the above case, Vpg mL to the shield wiring layer SL 2.

In this case, since GIDL is more likely to occur than when the electrode layer WL 5 is Vpass, it is desirable to give a higher potential to the shield wiring layer SL 2 than when the electrode layer WL 5 is Vpass.

However, if the potential of the shield interconnection layer SL 2 is too high, GIDL occurs in the vicinity of the shield interconnection layer SL 2 and deterioration in characteristics due to it can not be ignored, so the upper limit of the shield potential needs to be appropriately set.

[0064]

Since the shield interconnection layer SL 2 does not function as a control gate of the memory cell, it is possible to design with only the low resistance without considering the transistor characteristics such as the threshold value.

From such a viewpoint, the shield wiring layer SL 2 is not limited to a semiconductor, and may be formed of a compound of a metal and a semiconductor, or a metal.

[0065]

Besides, as shown in FIG. 10 which is a sectional view of a row decoder portion similar to FIG. 7, both the shield interconnection layer SL 1 and the shield interconnection layer SL 2 described above may be provided.

[0066]

In other words, by providing the lower shield interconnection layer SL 1 between the lowermost electrode layer WL 1 and the transfer transistor and giving a desired first shield potential, it is possible to suppress the increase in resistance of the diffusion layer of the transfer transistor. By providing the upper shield interconnection layer SL 2 between the electrode layer (the electrode layer WL 4 in the case of FIG. 10) and the drain side selection gate SGD and giving a desired second shield potential, erroneous writing to the unselected cell can be suppressed .

[0067]

The embodiments of the present invention have been described with reference to specific examples.

However, the present invention is not limited thereto, and various modifications are possible based on the technical idea of the present invention.

[0068]

In the above-described embodiment, the write potential Vpgm is transferred by the transfer transistor. However, the transfer transistor transfers its potential, for example, Vpass or 0 V according to the potential applied to the corresponding electrode layer.

For example, when the transfer transistor transfers Vpass, Vpass may be applied to the shield interconnection layer SL 1 thereon. However, even in that case, it is preferable to give the shield interconnection layer SL 1 a potential as high as possible as long as it is possible to secure a breakdown voltage between the shield interconnection layer SL 1 and the lowermost electrode layer WL 1 as described above, It is advantageous for suppression of rise.

[0069]

In the above-described embodiment, silicon is exemplified as a semiconductor, but a semiconductor other than silicon may be used. Further, the film structure including the charge storage layer 17 between each of the electrode layers WL 1 to WL 5 and the semiconductor layer 21 is not limited to the ONO (Oxide-Nitride-Oxide) structure. For example, the charge storage layer and the gate insulating film It may have a layered structure.

[0070]

10: memory cell array, 17: charge storage layer, 20, 30, 40 transfer transistor, 21 semiconductor layer, 50 peripheral circuit, CS ... cell source, SGS ... source side selection transistor, SGD ... drain side selection transistor, MC ... memory cell, MS ... memory string, WL1 to WL5 ... electrode layer, SL1 ... lower shield wiring layer, SL2 ... top shield wiring layer

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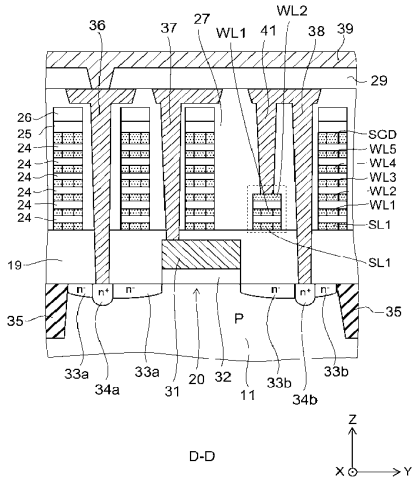
最終頁に続く

(54)【発明の名称】半導体記憶装置

(57)【要約】
【課題】メモリセルのコントロールゲートとして機能する電極層の電位が他領域に影響するのを抑制することができる半導体記憶装置を提供する。
【解決手段】本発明の半導体記憶装置は、半導体基板１１上におけるメモリセル領域及び周辺回路領域にわたって設けられ複数の電極層ＷＬ１～ＷＬ５と複数の絶縁層２４とが交互に積層された積層体と、メモリセル領域における積層体を貫通して形成されたホールの内部に設けられ積層体の積層方向に延びる半導体層２１と、半導体層２１と電極層ＷＬ１～ＷＬ５との間に設けられた電荷蓄積層１７と、周辺回路領域における積層体の下に設けられ、電極層ＷＬ１～ＷＬ５に電位を転送する転送トランジスタと、転送トランジスタと最下層の電極層ＷＬ１との間に設けられ、転送トランジスタの拡散層の電位に応じたシールド電位が与えられる下部シールド配線層ＳＬ１とを備えている。
【選択図】図５



【特許請求の範囲】
【請求項１】
メモリセル領域と周辺回路領域とを有する半導体基板と、
前記半導体基板上における前記メモリセル領域及び前記周辺回路領域にわたって設けられ、複数の電極層と複数の絶縁層とが交互に積層された積層体と、
前記メモリセル領域における前記積層体を貫通して形成されたホールの内部に設けられ、前記電極層と前記絶縁層との積層方向に延びる半導体層と、
前記半導体層と前記電極層との間に設けられた電荷蓄積層と、
前記周辺回路領域における前記積層体の下に設けられ、前記電極層に電位を転送する転送トランジスタと、
前記転送トランジスタと最下層の前記電極層との間に設けられ、前記転送トランジスタの拡散層の電位に応じたシールド電位が与えられる下部シールド配線層と、
を備えたことを特徴とする半導体記憶装置。
【請求項２】
メモリセル領域と周辺回路領域とを有する半導体基板と、
前記半導体基板上における前記メモリセル領域及び前記周辺回路領域にわたって設けられ、複数の電極層と複数の絶縁層とが交互に積層された積層体と、
前記メモリセル領域における前記積層体を貫通して形成されたホールの内部に設けられ、前記電極層と前記絶縁層との積層方向に延びる半導体層と、
前記半導体層と前記電極層との間に設けられた電荷蓄積層と、
前記周辺回路領域における前記積層体の下に設けられ、前記電極層に電位を転送する転送トランジスタと、
前記転送トランジスタと最下層の前記電極層との間に設けられ、前記転送トランジスタの拡散層の電位に応じた第１のシールド電位が与えられる下部シールド配線層と、
最上層の前記電極層の上に設けられ、前記電極層の電位に応じた第２のシールド電位が与えられる上部シールド配線層と、
を備えたことを特徴とする半導体記憶装置。
【請求項３】
前記下部シールド配線層には、この下部シールド配線層の下に位置する前記転送トランジスタの拡散層の電位と同電位が与えられることを特徴とする請求項１または２に記載の半導体記憶装置。
【請求項４】
前記下部シールド配線層には、この下部シールド配線層の下に位置する前記転送トランジスタの拡散層の電位と、最下層の前記電極層の電位との間の中間電位が与えられることを特徴とする請求項１または２に記載の半導体記憶装置。
【請求項５】
メモリセル領域と周辺回路領域とを有する半導体基板と、
前記半導体基板上における前記メモリセル領域及び前記周辺回路領域にわたって設けられ、複数の電極層と複数の絶縁層とが交互に積層された積層体と、
前記メモリセル領域における前記積層体を貫通して形成されたホールの内部に設けられ、前記電極層と前記絶縁層との積層方向に延びる半導体層と、
前記半導体層と前記電極層との間に設けられた電荷蓄積層と、
最上層の前記電極層の上に設けられ、前記電極層の電位に応じたシールド電位が与えられる上部シールド配線層と、
を備えたことを特徴とする半導体記憶装置。
【発明の詳細な説明】
【技術分野】
【０００１】
本発明は、半導体記憶装置に関する。
【背景技術】

【０００２】
データ記憶層（電荷蓄積層）としてシリコン窒化膜を用いるＭＯＮＯＳ（Metal-Oxide-Nitride-Oxide-Semiconductor)型不揮発性半導体記憶装置において、記憶密度を高めるためにメモリセルを基板上に積層することが行われている。例えば特許文献１には、柱状半導体を基板主面に対して垂直な方向に設け、その方向に複数のメモリセルが直列に接続された構造の不揮発性半導体記憶装置に関する技術が開示されている。
メモリセルのコントロールゲートとして機能する電極層を周辺回路領域まで延在させて設けた場合、その電極層の電位によっては、周辺回路領域に形成されたトランジスタの拡散層が高抵抗化し所望の動作を行えなくなる問題が懸念される。
【先行技術文献】
【特許文献】
【０００３】
【特許文献１】特開２００７－１８０３８９号公報
【発明の概要】
【発明が解決しようとする課題】
【０００４】
本発明は、メモリセルのコントロールゲートとして機能する電極層の電位が他領域に影響するのを抑制することができる半導体記憶装置を提供する。
【課題を解決するための手段】
【０００５】
本発明の一態様によれば、メモリセル領域と周辺回路領域とを有する半導体基板と、前記半導体基板上における前記メモリセル領域及び前記周辺回路領域にわたって設けられ、複数の電極層と複数の絶縁層とが交互に積層された積層体と、前記メモリセル領域における前記積層体を貫通して形成されたホールの内部に設けられ、前記電極層と前記絶縁層との積層方向に延びる半導体層と、前記半導体層と前記電極層との間に設けられた電荷蓄積層と、前記周辺回路領域における前記積層体の下に設けられ、前記電極層に電位を転送する転送トランジスタと、前記転送トランジスタと最下層の前記電極層との間に設けられ、前記転送トランジスタの拡散層の電位に応じたシールド電位が与えられる下部シールド配線層と、を備えたことを特徴とする半導体記憶装置が提供される。
また、本発明の他の一態様によれば、メモリセル領域と周辺回路領域とを有する半導体基板と、前記半導体基板上における前記メモリセル領域及び前記周辺回路領域にわたって設けられ、複数の電極層と複数の絶縁層とが交互に積層された積層体と、前記メモリセル領域における前記積層体を貫通して形成されたホールの内部に設けられ、前記電極層と前記絶縁層との積層方向に延びる半導体層と、前記半導体層と前記電極層との間に設けられた電荷蓄積層と、前記周辺回路領域における前記積層体の下に設けられ、前記電極層に電位を転送する転送トランジスタと、前記転送トランジスタと最下層の前記電極層との間に設けられ、前記転送トランジスタの拡散層の電位に応じた第１のシールド電位が与えられる下部シールド配線層と、最上層の前記電極層の上に設けられ、前記電極層の電位に応じた第２のシールド電位が与えられる上部シールド配線層と、を備えたことを特徴とする半導体記憶装置が提供される。
また、本発明のさらに他の一態様によれば、メモリセル領域と周辺回路領域とを有する半導体基板と、前記半導体基板上における前記メモリセル領域及び前記周辺回路領域にわたって設けられ、複数の電極層と複数の絶縁層とが交互に積層された積層体と、前記メモリセル領域における前記積層体を貫通して形成されたホールの内部に設けられ、前記電極層と前記絶縁層との積層方向に延びる半導体層と、前記半導体層と前記電極層との間に設けられた電荷蓄積層と、最上層の前記電極層の上に設けられ、前記電極層の電位に応じたシールド電位が与えられる上部シールド配線層と、を備えたことを特徴とする半導体記憶装置が提供される。
【発明の効果】
【０００６】

本発明によれば、メモリセルのコントロールゲートとして機能する電極層の電位が他領域に影響するのを抑制することができる半導体記憶装置が提供される。

【図面の簡単な説明】

【０００７】

【図１】本発明の実施形態に係る半導体記憶装置における主要要素の平面位置関係を示す模式図。

【図２】図１のＡ－Ａ断面に対応する模式図。

【図３】図１のＢ－Ｂ断面に対応する模式図。

【図４】図１のＣ－Ｃ断面に対応する模式図。

【図５】図１のＤ－Ｄ断面に対応する模式図。

【図６】図１のＥ　Ｅ断面に対応する模式図。

【図７】図１のＦ－Ｆ断面に対応する模式図。

【図８】他の実施形態における図２と同様な断面図。

【図９】同他の実施形態における図７と同様な断面図。

【図１０】さらに他の実施形態における図７と同様な断面図。

【発明を実施するための形態】

【０００８】

以下、図面を参照し、本発明の実施形態について説明する。各図面中共通する要素については同じ符号を付している。

図１は、本発明の実施形態に係る半導体記憶装置における主要要素の平面位置関係を示す模式図である。

図２は、図１におけるＡ－Ａ断面に対応する図である。

図３は、図１におけるＢ－Ｂ断面に対応する図である。

図４は、図１におけるＣ－Ｃ断面に対応する図である。

図５は、図１におけるＤ－Ｄ断面に対応する図である。

図６は、図１におけるＥ　Ｅ断面に対応する図である。

図７は、図１におけるＦ－Ｆ断面に対応する図である。

【０００９】

本明細書においては、説明の便宜上、ＸＹＺ直交座標系を導入する。この座標系においては、半導体基板の上面（主面）に対して平行な方向であって相互に直交する２方向をＸ方向及びＹ方向とし、半導体基板の主面に対して垂直な方向をＺ方向とする。

【００１０】

本実施形態に係る半導体記憶装置は、複数のメモリセルが３次元配列されたメモリセルアレイ１０と、メモリセルにデータを書き込む、メモリセルに記憶されたデータを読み出すなどの動作を行う周辺回路５０とを同じ半導体基板上に有する。図１には、周辺回路５０の中でも特にメモリセルのコントロールゲートとして機能する電極層を選択するロウデコーダを示す。

【００１１】

まず、図２を参照して、メモリセルについて説明する。

【００１２】

例えばｐ型のシリコン基板（またはｐ型ウェル層）１１の表面に、ｎ$^{+}$型の拡散層１２、１３とｎ$^{+}$型の拡散層１４が選択的に形成されている。拡散層１４はセルソースＣＳに接続されている。拡散層１２と拡散層１３との間の基板１１表面上には絶縁膜１５を介してソース側選択ゲートＳＧＳが設けられている。ソース側選択ゲートＳＧＳは、例えば非晶質または多結晶シリコンからなる。拡散層１２～１４、絶縁膜１５、ソース側選択ゲートＳＧＳは、ソース側選択トランジスタを構成する。

【００１３】

拡散層１２上には、複数のメモリセルＭＣがＺ方向に直列接続されて構成されるメモリストリングＭＳが設けられている。ソース側選択ゲートＳＧＳに与えるゲート電圧を制御することで、メモリストリングＭＳとセルソースＣＳとの間をオンオフすることができる

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【００１４】

基板１１上には層間絶縁層１９が設けられ、その層間絶縁層１９上には下部シールド配線層ＳＬ１（以下、単にシールド配線層ともいう）が設けられている。そのシールド配線層ＳＬ１上には、複数の絶縁層２４と複数の電極層ＷＬ１～ＷＬ５とが交互に積層された積層体が設けられている。電極層ＷＬ１～ＷＬ５の層数は任意であるが、本実施形態においては例えば５層の場合を例示する。

【００１５】

シールド配線層ＳＬ１および電極層ＷＬ１～ＷＬ５は、例えば非晶質または多結晶シリコンからなる。あるいは、シールド配線層ＳＬ１は、より低抵抗な金属シリサイドや金属から構成してもよい。

【００１６】

上記積層体上における最上層の絶縁層２４上にはドレイン側選択ゲートＳＧＤが設けられ、その上には絶縁層２５、２６が設けられている。ドレイン側選択ゲートＳＧＤは、例えば非晶質または多結晶シリコンからなる。また、絶縁層２６上面は絶縁膜１８で覆われている。

【００１７】

上記積層体には、Ｚ方向に延び拡散層１２にまで達する貫通ホールが形成され、その貫通ホールの側壁に、絶縁膜１６、電荷蓄積層１７、絶縁膜１８および半導体層２１が設けられている。

【００１８】

例えば、絶縁膜１６はシリコン酸化膜、電荷蓄積層１７はシリコン窒化膜、絶縁層１８はシリコン酸化膜であり、これらはいわゆるＯＮＯ（0xide-Nitride-0xide）膜を構成する。半導体層２１は例えばn^-型のシリコンである。半導体層２１は貫通ホールの底部で拡散層１２に接している。

【００１９】

ＯＮＯ膜を挟んで半導体層２１と各電極層ＷＬ１～ＷＬ５とが対向した部分はメモリセルＭＣを構成し、半導体層２１はメモリセルＭＣにおけるチャネルとして機能し、各電極層ＷＬ１～ＷＬ５はコントロールゲートとして機能し、電荷蓄積層１７は半導体層２１から注入される電荷を蓄積するデータ記憶層として機能する。

【００２０】

このメモリセルＭＣはチャージトラップ構造のメモリセルであり、電荷蓄積層１７は電荷（電子）を閉じこめるトラップを多数有し、例えばシリコン窒化膜からなる。電荷蓄積層１７と半導体層２１との間の絶縁膜１８は、電荷蓄積層１７に半導体層２１から電荷が注入される際、または電荷蓄積層１７に蓄積された電荷が半導体層２１へ拡散する際に電位障壁となる。電荷蓄積層１７と各電極層ＷＬ１～ＷＬ５との間の絶縁膜１６は、電荷蓄積層１７に蓄積された電荷が電極層ＷＬ１～ＷＬ５へ拡散するのを防止する。電極層ＷＬ１～ＷＩ５の層数に対応した複数のメモリセルＭＣがＺ方向に直列接続され、メモリストリングＭＳが構成される。

【００２１】

半導体層２１の上部には、それぞれイオン注入法によって、p^-型の半導体層２２とn^+型の半導体層２３が設けられている。ドレイン側選択ゲートＳＧＤは、絶縁膜１８を介して半導体層２２に対向し、これらによってドレイン側選択トランジスタが構成される。

【００２２】

半導体層２３における絶縁膜１８上面上に設けられた部分は金属シリサイド化され、その部分はビット線ＢＬに接続されている。ドレイン側選択ゲートＳＧＤに与えるゲート電圧を制御することによって、メモリストリングＭＳとビット線ＢＬとの間のオンオフを制御できる。

【００２３】

半導体層２１～２３の内側には絶縁層２８が埋め込まれ、さらにその上およびセルソー

スＣＳの周囲にも層間絶縁層２７が設けられている。また、シールド配線層ＳＬ１、電極層ＷＬ１～ＷＬ５およびドレイン側選択ゲートＳＧＤにおける、メモリストリングＭＳの反対側の端部は金属シリサイド化され低抵抗化されている。

【００２４】

以上説明したシールド配線層ＳＬ１、絶縁層２４および電極層ＷＬ１～ＷＬ５を含む積層体は、周辺回路領域にまで延在している。それら積層体を、図１の平面図ではワード線ＷＬとして示す。

【００２５】

周辺回路領域には、各電極層ＷＬ１～ＷＬ５、シールド配線層ＳＬ１に電位を転送する転送トランジスタが設けられている。例えば、図１には、電極層ＷＬ２に電位を転送する転送トランジスタ２０と、電極層ＷＬ１に電位を転送する転送トランジスタ３０と、シールド配線層ＳＬ１に電位を転送する転送トランジスタ４０が形成された領域を示している。

【００２６】

図１におけるＤ－Ｄ断面に対応する図５は、転送トランジスタ２０が形成された部分の断面構造を示す。

【００２７】

転送トランジスタ２０は、基板１１表面に選択的に形成されたｎ$^-$型の拡散層３３ａ、３３ｂと、ｎ$^+$型の拡散層３４ａ、３４ｂと、拡散層３３ａと拡散層３３ｂとの間の基板１１表面上に設けられたゲート絶縁膜３２と、この上に設けられたゲート電極３１とを有する。それらが形成された領域を、図１において転送トランジスタ２０のアクティブ領域６０として示している。基板１１表面に形成された前述の拡散層は、例えばＳＴＩ（Shallow Trench Isolation）構造の絶縁層３５によって、他のトランジスタや素子の拡散層と分離されている。

【００２８】

上記積層体の上には絶縁層２９を介して配線３９が設けられ、転送トランジスタ２０の拡散層３４ａはコンタクト部３６を介して配線３９に接続されている。拡散層３４ｂはコンタクト部３８、４１を介して電極層ＷＬ２に接続されている。

【００２９】

図１におけるＣ－Ｃ断面に対応する図４に示すように、各電極層ＷＬ１～ＷＬ５及びシールド配線層ＳＬ１は周辺回路領域で階段状に形成されている。各電極層ＷＬ１～ＷＬ５及びシールド配線層ＳＬ１は、階段状に形成された部分で、コンタクト部を介して、対応する転送トランジスタに接続されている。

【００３０】

例えば、電極層ＷＬ２は、コンタクト部４１及び図５に示すコンタクト部３８を介して転送トランジスタ２０の拡散層３４ｂに接続されている。電極層ＷＬ１は、コンタクト部４２及び図６に示すコンタクト部３８を介して転送トランジスタ３０の拡散層３４ｂに接続されている。シールド配線層ＳＬ１は、コンタクト部４３及び図７に示すコンタクト部３８を介して転送トランジスタ４０の拡散層３４ｂに接続されている。

【００３１】

各電極層ＷＬ１～ＷＬ５及びシールド配線層ＳＬ１において転送トランジスタと接続される階段状部分は金属シリサイド化され、低抵抗化されている。

【００３２】

図５に示す転送トランジスタ２０において、ゲート配線３７を介してゲート電極３１に所定のゲート電圧を印加すると拡散層３４ａ、３４ｂ間が導通し、配線３９及びコンタクト部３６を介して拡散層３４ａに与えられた電位が拡散層３４ｂに転送される。そして、その拡散層３４ｂの電位はコンタクト部３８、４１を介して電極層ＷＬ２に転送される。

【００３３】

図１におけるＥ－Ｅ断面に対応する図６は、転送トランジスタ３０が形成された部分の断面構造を示す。

【００３４】
この転送トランジスタ３０についても同様に、基板１１表面に選択的に形成されたｎ$^-$型の拡散層３３ａ、３３ｂと、ｎ$^+$型の拡散層３４ａ、３４ｂと、拡散層３３ａと拡散層３３ｂとの間の基板１１表面上に設けられたゲート絶縁膜３２と、この上に設けられたゲート電極３１とを有する。それらが形成された領域を、図１において転送トランジスタ３０のアクティブ領域６０として示している。
【００３５】
この転送トランジスタ３０において、ゲート配線３７を介してゲート電極３１に所定のゲート電圧を印加すると拡散層３４ａ、３４ｂ間が導通し、配線３９及びコンタクト部３６を介して拡散層３４ａに与えられた電位が拡散層３４ｂに転送される。そして、その拡散層３４ｂの電位はコンタクト部３８、４２を介して電極層ＷＬ１に転送される。
【００３６】
図１におけるＦ－Ｆ断面に対応する図７は、転送トランジスタ４０が形成された部分の断面構造を示す。
【００３７】
この転送トランジスタ４０についても同様に、基板１１表面に選択的に形成されたｎ$^-$型の拡散層３３ａ、３３ｂと、ｎ$^+$型の拡散層３４ａ、３４ｂと、拡散層３３ａと拡散層３３ｂとの間の基板１１表面上に設けられたゲート絶縁膜３２と、この上に設けられたゲート電極３１とを有する。それらが形成された領域を、図１において転送トランジスタ４０のアクティブ領域６０として示している。
【００３８】
この転送トランジスタ４０において、ゲート配線３７を介してゲート電極３１に所定のゲート電圧を印加すると拡散層３４ａ、３４ｂ間が導通し、配線３９及びコンタクト部３６を介して拡散層３４ａに与えられた電位が拡散層３４ｂに転送される。そして、その拡散層３４ｂの電位はコンタクト部３８、４３を介してシールド配線層ＳＬ１に転送される。
【００３９】
本実施形態に係る半導体記憶装置は、データの消去・書き込みを電気的に自由に行うことができ、電源を切っても記憶内容を保持することができる不揮発性半導体記憶装置である。
【００４０】
ここで、図１、２、５～７において点線で囲んで示すブロック（選択ブロック）におけるいずれかの電極層（ここでは例えば電極層ＷＬ２とする）をコントロールゲートとするメモリセル（書き込み対象セル）の電荷蓄積層に電子を注入してデータを書き込む場合について説明する。
【００４１】
書き込み対象セル（を含むメモリストリング）に接続されている選択ビット線ＢＬに０Ｖ、それ以外の非選択ビット線ＢＬにＶｄｄ（例えば数ボルト程度）が与えられる。書き込み対象セルに接続されているドレイン側選択トランジスタはオンにされ、書き込み対象セルに接続されているソース側選択トランジスタはオフにされる。セルソースにはＶｄｄが与えられる。基板１１またはｐ型ウェル層には０Ｖが与えられる。書き込み対象セルのコントロールゲートである電極層ＷＬ２にはＶpgm（例えば２０Ｖ程度）が与えられ、それ以外の電極層にはＶpass（例えば１０Ｖ程度）が与えられる。すなわち、選択ブロックの電極層ＷＬ２には、図５に示す転送トランジスタ２０によって、配線３９に与えられた書き込み電位Ｖpgmが転送され印加される。
【００４２】
これにより、選択ビット線ＢＬの０Ｖが書き込み対象セルのチャネル（半導体層２１）に伝播し、そのチャネルと、書き込み対象セルの電極層ＷＬ２との間のＯＮＯ膜に印加される電界強度が強くなり、書き込み対象セルの電荷蓄積層１７に電子が注入されデータ書き込みが行われる。

【００４３】
シールド配線層ＳＬ１には、そのシールド配線層ＳＬ１の下方の転送トランジスタの拡散層３４ａ、３４ｂの電位と、最下層の電極層ＷＬ１の電位に応じた、所望のシールド電位が与えられる。電極層ＷＬ１～ＷＬ５の電位及びシールド配線層ＳＬ１の電位の一例を表１に示す。
【００４４】
【表１】

	WL1＝Vpgm	WL1＝Vpass	WL1＝0V
WL5	Vpass	Vpass	Vpass
WL4	Vpass	Vpass	Vpass
WL3	Vpass	Vpass	Vpgm
WL2	Vpass	Vpgm	Vpass
WL1	Vpgm	Vpass	0V
下部シールド配線層	Vpgm	Vpgm or VpgmL	Vpgm or VpgmL

【００４５】
Ｖpgmは書き込み対象セルにデータ書き込み（電子注入）を行うのに十分な電圧であり、例えば２０Ｖ程度である。Ｖpassは非書き込み対象セルに書き込みが行われないようにする電圧であり、かつ非選択ビット線におけるＶpgmがかかる電極層をコントロールゲートとするメモリセルに書き込みが行われないようにそのセルのチャネル領域をブーストするのに十分な電圧であり、例えば１０Ｖ程度である。
【００４６】
本実施形態に係る半導体記憶装置では、基板面積の有効利用のため、電極層ＷＬ１～ＷＬ５における周辺回路領域まで延在している部分の下に、転送トランジスタを設けている。すなわち、図１に示すように転送トランジスタのアクティブ領域６０の上方を、電極層ＷＬ１～ＷＬ５を含むワード線ＷＬが横切るように延在している。
【００４７】
このような構造の場合、アクティブ領域６０上方に存在する電極層の電位によっては、その下の転送トランジスタのｎ⁻型拡散層３３ａ、３３ｂが高抵抗化し、場合によっては逆導電型の反転層が形成され、電荷の転送ができなくなってしまうことが起こり得る。
【００４８】
これに対して本実施形態では、最下層の電極層ＷＬ１と転送トランジスタとの間に、シールド配線層ＳＬ１を設け、そのシールド配線層ＳＬ１に所望のシールド電位を与える。これにより、転送トランジスタのｎ⁻型拡散層３３ａ、３３ｂに対する電極層電位の影響を遮断し、ｎ⁻型拡散層３３ａ、３３ｂの抵抗上昇を抑制することができる。
【００４９】
前述した表１は、転送トランジスタが任意の電極層に例えばＶpgmを転送しているときにおけるその転送トランジスタ上方の各電極層ＷＬ１～ＷＬ５およびシールド配線層ＳＬ１の電位例を示す。
【００５０】
転送トランジスタによって例えば最下層の電極層ＷＬ１にＶpgmを転送する場合、シールド配線層ＳＬ１には同じＶpgmが与えられる。これにより、転送トランジスタのｎ⁻型の拡散層３３ａ、３３ｂの特に表面側における電子密度の低減もしくは反転層の形成を抑制し、拡散層３３ａ、３３ｂの抵抗上昇を抑制できる。
【００５１】
転送トランジスタによって例えば電極層ＷＬ２にＶpgmを転送し、最下層のＷＬ１に与えられる電位がＶpassの場合、上記と同様に、拡散層３３ａ、３３ｂの高抵抗化抑制のために、シールド配線層ＳＬ１にはＶpgmを与える。あるいは、Ｖpassが与えられる最下層電極層ＷＬ１と、シールド配線層ＳＬ１との間の絶縁層の耐圧確保のため、拡散層３３ａ

、３３ｂにおける抵抗が問題とならない程度までＶpgmよりも低くしたＶpgmLをシールド配線層ＳＬ１に与えてもよい。

【００５２】

転送トランジスタによって例えば電極層ＷＬ３にＶpgmを転送し、最下層の電極層ＷＬ１に与えられる電位が０Ｖの場合、上記と同様に、拡散層３３ａ、３３ｂの高抵抗化抑制のために、シールド配線層ＳＬ１にはＶpgmを与える。そして、この場合にも、０Ｖが与えられる最下層電極層ＷＬ１と、シールド配線層ＳＬ１との間の絶縁層の耐圧確保のため、拡散層３３ａ、３３ｂにおける抵抗が問題とならない程度までＶpgmよりも低くしたＶpgmLをシールド配線層ＳＬ１に与えてもよい。

【００５３】

シールド配線層ＳＬ１は、メモリセルのコントロールゲートとしては機能しないため、しきい値等のトランジスタ特性のことを考慮に入れずに、低抵抗化だけを目的とした設計を行える。そのような観点から、シールド配線層ＳＬ１は、半導体に限らず、金属と半導体との化合物、金属から構成してもよい。

【００５４】

次に、図８、９を参照して本発明の他の実施形態について説明する。

図８は前述した実施形態の図２に対応するメモリセルアレイ部分の断面図であり、図９は図７に対応するロウデコーダ部分の断面図である。

【００５５】

本実施形態では、最上層の電極層ＷＬ５とドレイン側選択ゲートＳＧＤとの間に、上部シールド配線層ＳＬ２（以下、単にシールド配線層ともいう）を設けている。このシールド配線層ＳＬ２には、図９に示す転送トランジスタ７０によって、配線３９に与えられた所望のシールド電位がコンタクト部３６、３８、４４を介して転送される。

【００５６】

例えば最上層の電極層ＷＬ５に高電圧Ｖpgmを印加し書き込みを行う場合、書き込み対象セルを含むメモリストリングと接続された選択ビット線は０Ｖにされ、その０Ｖが書き込み対象セルのチャネルに印加され書き込みが行われる。

【００５７】

書き込み対象セルを含まない非選択メモリストリングにおいては、ドレイン側選択ゲートのオフによりビット線との接続がカットされ、ブースト比によりチャネル電位が持ち上げられ、Ｖpgmが印加される電極層ＷＬ５との間で電子注入が行われるような電界が作用せず、非選択セルへの書き込みが行われないようにする。このとき、非選択メモリストリングにおけるドレイン側選択ゲートのソース・ドレイン間には高電圧がかかり、ＧＩＤＬ（Gate Induced Drain Leakage）現象による非選択セルへの誤書き込みが起こってしまう問題が懸念される。

【００５８】

これに対して本実施形態では、最上層の電極層ＷＬ５とドレイン側選択ゲートＳＧＤとの間に、シールド配線層ＳＬ２を設け、そのシールド配線層ＳＬ２に、最上層電極層ＷＬ５の電位に応じた所望の電位を与えることによって、ドレイン側選択ゲートＳＧＤのソース・ドレイン間の電位差を緩和し、ＧＩＤＬによる誤書き込みを抑制することができる。

【００５９】

表２は、非選択メモリストリングにおける電極層ＷＬ１～ＷＬ５および上部シールド配線層ＳＬ２の電位例を示す。

【００６０】

【表２】

	WL5＝0V	WL5＝Vpass	WL5＝Vpgm
上部シールド配線層	0V	数V～VpassL	数V～VpgmL
WL5	0V	Vpass	Vpgm
WL4	Vpass	Vpgm	Vpass
WL3	Vpgm	Vpass	0V
WL2	Vpass	0V	Vpass
WL1	0V	Vpass	Vpass

【００６１】

最上層の電極層ＷＬ５の電位が０Ｖの場合、ドレイン側選択ゲートＳＧＤのソース・ドレイン間には高電圧がかからないため、ＧＩＤＬが発生せず、シールド配線層ＳＬ２に与える電位は０Ｖで十分である。

【００６２】

電極層ＷＬ５にＶpass（例えば１０Ｖ程度）が与えられる場合、ドレイン側選択ゲートＳＧＤのソース・ドレイン間の電界を緩和してＧＩＤＬの発生を抑えるべく、Ｖpassよりも低い数Ｖ～ＶpassLをシールド配線層ＳＬ２に与える。このときにシールド配線層ＳＬ２に与えられる電位は、電極層ＷＬ５がＧＩＤＬによって劣化しない程度まで低電圧化することが可能である。

【００６３】

電極層ＷＬ５にＶpgm（例えば２０Ｖ程度）が与えられる場合、上記と同様に、ドレイン側選択ゲートＳＧＤのソース・ドレイン間の電界を緩和してＧＩＤＬの発生を抑えるべく、Ｖpgmよりも低い数Ｖ～ＶpgmLをシールド配線層ＳＬ２に与える。この場合、電極層ＷＬ５がＶpassのときよりもＧＩＤＬがより発生しやすいため、電極層ＷＬ５がＶpassのときよりも高めの電位をシールド配線層ＳＬ２に与えることが望ましい。ただし、シールド配線層ＳＬ２の電位があまり高過ぎるとこのシールド配線層ＳＬ２近傍でＧＩＤＬが発生し、それによる特性劣化が無視できなくなるので、シールド電位の上限は適切に設定する必要がある。

【００６４】

シールド配線層ＳＬ２は、メモリセルのコントロールゲートとしては機能しないため、しきい値等のトランジスタ特性のことを考慮に入れずに、低抵抗化だけを目的とした設計を行える。そのような観点から、シールド配線層ＳＬ２は、半導体に限らず、金属と半導体との化合物、金属から構成してもよい。

【００６５】

また、図７と同様なロウデコーダ部分の断面図である図１０に示すように、前述したシールド配線層ＳＬ１とシールド配線層ＳＬ２の両方を設けてもよい。

【００６６】

すなわち、最下層の電極層ＷＬ１と転送トランジスタとの間に下部シールド配線層ＳＬ１を設け所望の第１のシールド電位を与えることで転送トランジスタの拡散層の高抵抗化を抑制でき、なおかつ最上層の電極層（図１０の場合電極層ＷＬ４）とドレイン側選択ゲートＳＧＤとの間に上部シールド配線層ＳＬ２を設け所望の第２のシールド電位を与えることで、非選択セルへの誤書き込みを抑制できる。

【００６７】

以上、具体例を参照しつつ本発明の実施形態について説明した。しかし、本発明は、それらに限定されるものではなく、本発明の技術的思想に基づいて種々の変形が可能である。

【００６８】

前述した実施形態では転送トランジスタで書き込み電位Ｖpgmを転送する例を挙げたが、対応する電極層に与える電位に応じて転送トランジスタはその電位、例えばＶpassや０Ｖも転送する。例えば、転送トランジスタがＶpassを転送している場合、その上のシール

ド配線層ＳＬ１にはＶpassを与えるようにしてもよい。ただし、その場合でも、前述したようにシールド配線層ＳＬ１と最下層の電極層ＷＬ１との間の耐圧が確保可能な限り高い電位をシールド配線層ＳＬ１に与えることが、転送トランジスタの拡散層の抵抗上昇抑制に有利である。

【００６９】

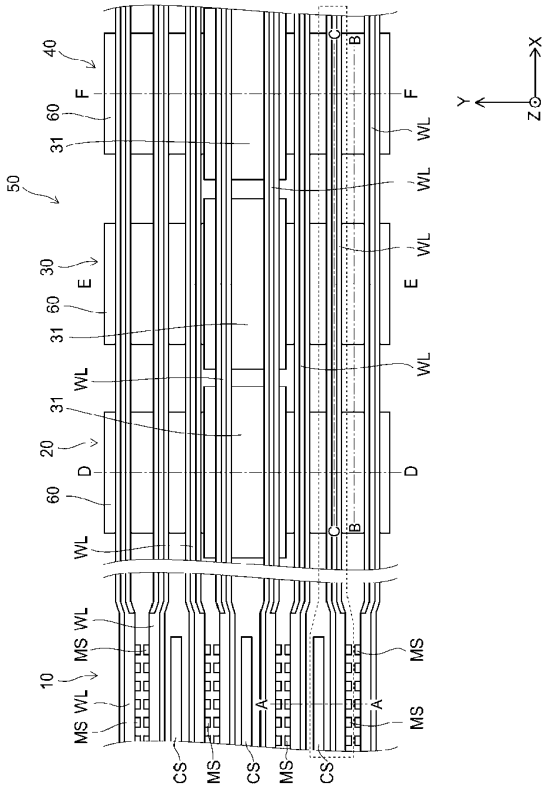
また、前述した実施形態では、半導体としてシリコンを例示したが、シリコン以外の他の半導体を用いてもよい。また、各電極層ＷＬ１～ＷＬ５と半導体層２１との間の電荷蓄積層１７を含む膜構造は、ＯＮＯ（0xide-Nitride-0xide）構造に限らず、例えば電荷蓄積層とゲート絶縁膜との２層構造であってもよい。

【符号の説明】

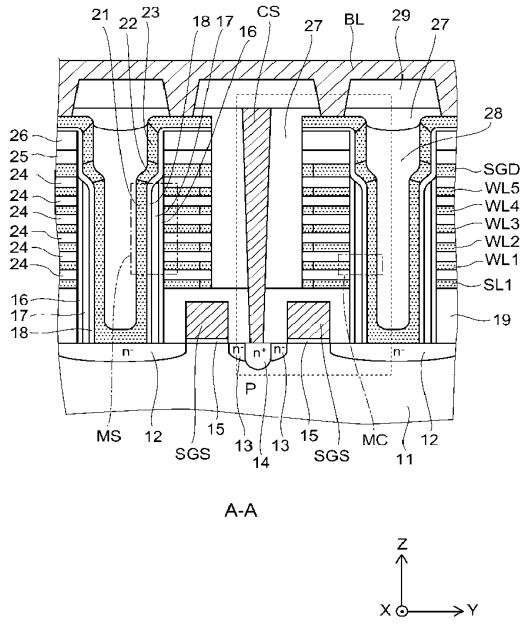
【００７０】

１０…メモリセルアレイ、１７…電荷蓄積層、２０，３０，４０…転送トランジスタ、２１…半導体層、５０…周辺回路、ＣＳ…セルソース、ＳＧＳ…ソース側選択トランジスタ、ＳＧＤ…ドレイン側選択トランジスタ、ＭＣ…メモリセル、ＭＳ…メモリストリング、ＷＬ１～ＷＬ５…電極層、ＳＬ１…下部シールド配線層、ＳＬ２…上部シールド配線層

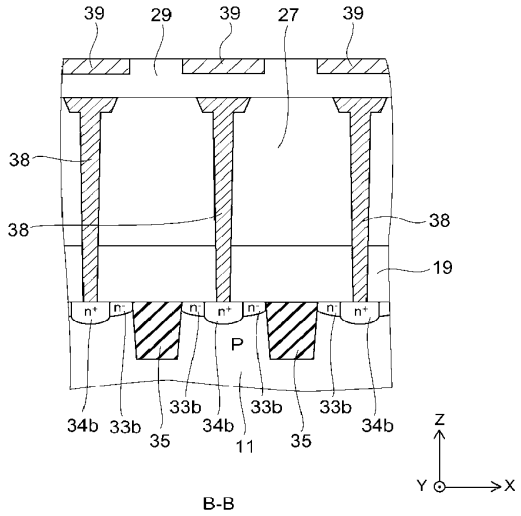
【図１】



【図２】

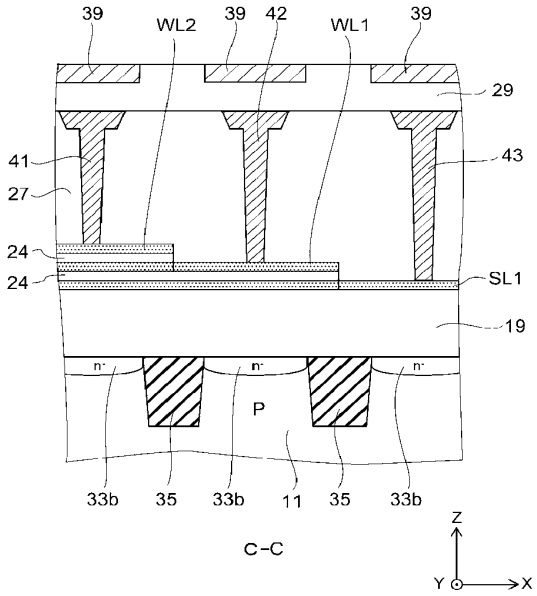


【図３】



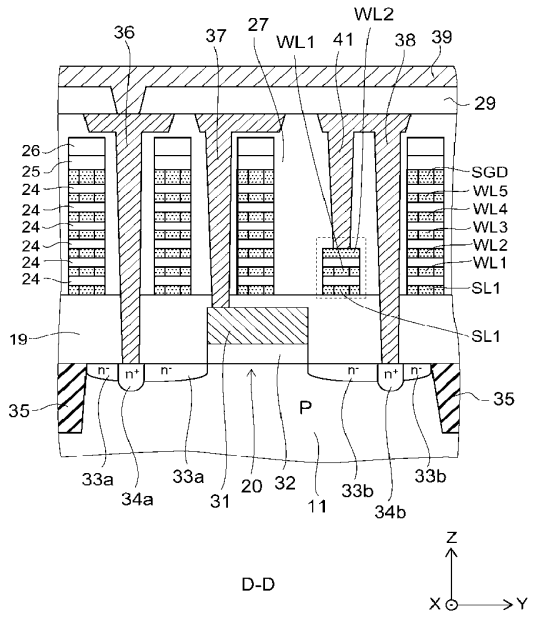
B-B

【図４】



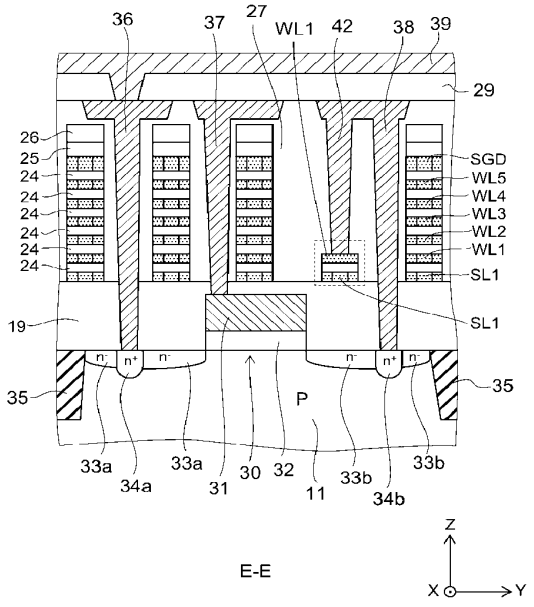
C-C

【図５】



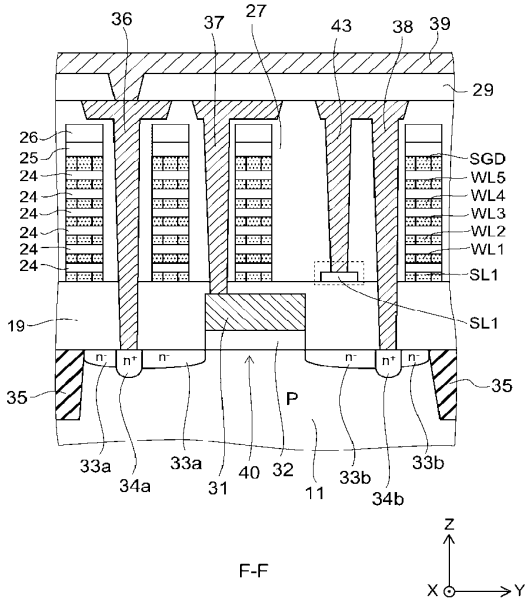
D-D

【図６】

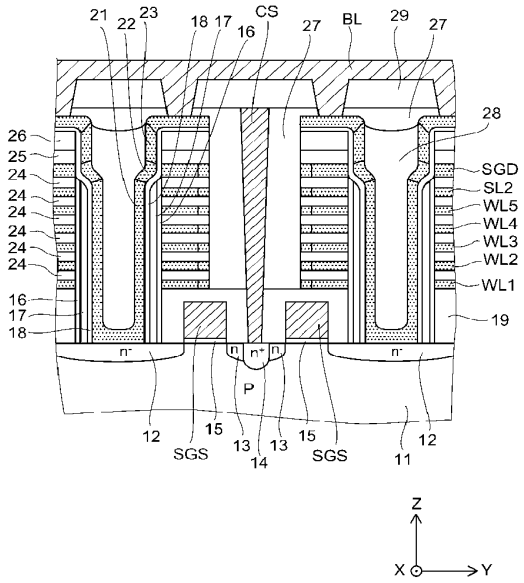


E-E

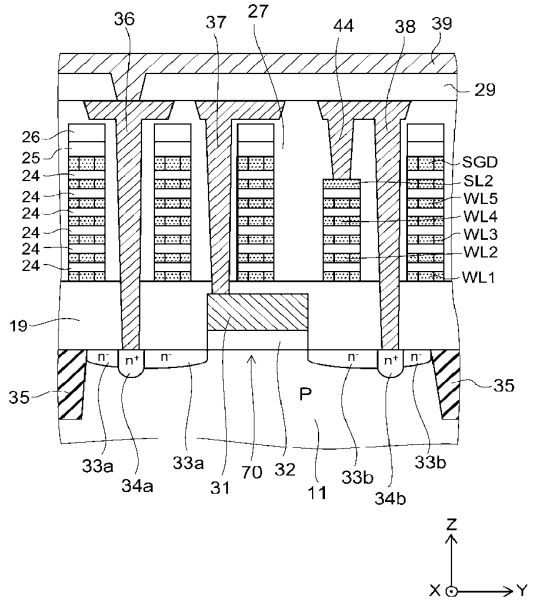
【図７】



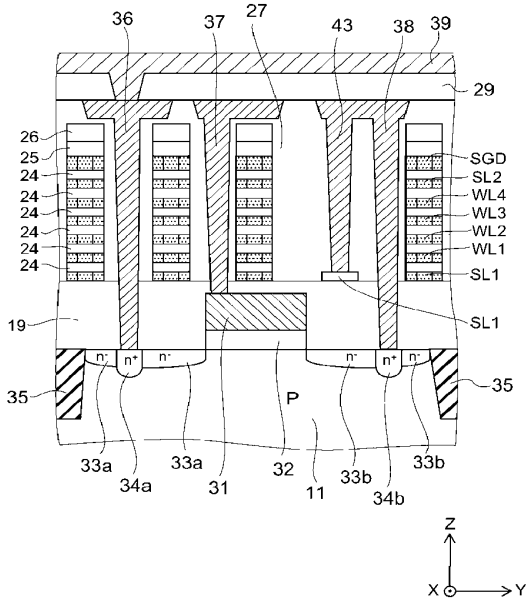
【図８】



【図９】



【図１０】



フロントページの続き

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GA15 JA04 JA35 JA53 KA01 KA17 LA16 MA06 MA16 MA19
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Filing Date:	
Title of Invention:	SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR MANUFACTURING SAME
First Named Inventor/Applicant Name:	Jun FUJIKI
Filer:	Philippe Jean-Claude Signore/Brandon Botchway
Attorney Docket Number:	516693US

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	300	300
UTILITY SEARCH FEE	1111	1	660	660
UTILITY EXAMINATION FEE	1311	1	760	760
Pages:				
Claims:				
Miscellaneous-Filing:				
LATE FILING FEE FOR OATH OR DECLARATION	1051	1	160	160
Petition:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
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1		516693USNewApplication.pdf	9390281 f45db96463adc39a99887c42125a47c6a9ae4d22	yes	79

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2	Fee Worksheet (SB06)	fee-info.pdf	36810 06e7d49954fcd573e411348a7e0b22ba9ce50a45	no	2

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CONFIRMATION NO. 1059

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1940 DUKE STREET
ALEXANDRIA, VA 22314

INFORMAL NOTICE

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Date Mailed: 10/03/2018

INFORMATIONAL NOTICE TO APPLICANT

Applicant is notified that the above-identified application contains the deficiencies noted below. No period for reply is set forth in this notice for correction of these deficiencies. However, if a deficiency relates to the inventor's oath or declaration, the applicant must file an oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each actual inventor no later than the expiration of the time period set in the "Notice of Allowability" to avoid abandonment. See 37 CFR 1.53(f).

The item(s) indicated below are also required and should be submitted with any reply to this notice to avoid further processing delays.

- A properly executed inventor's oath or declaration has not been received for the following inventor(s):
  Jun FUJIKI
  Shinya ARAI
  Kotaro FUJII

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
16/129,082	09/12/2018	2811	1880	516693US	20	3

CONFIRMATION NO. 1059

22850
OBLON, MCCLELLAND, MAIER & NEUSTADT, L.L.P.
1940 DUKE STREET
ALEXANDRIA, VA 22314

FILING RECEIPT

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Date Mailed: 10/03/2018

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

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Assignment For Published Patent Application

TOSHIBA MEMORY CORPORATION, Minato-ku, JAPAN

Power of Attorney: The patent practitioners associated with Customer Number 22850

Domestic Applications for which benefit is claimed - None.
A proper domestic benefit claim must be provided in an Application Data Sheet in order to constitute a claim for domestic benefit. See 37 CFR 1.76 and 1.78.

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.)
JAPAN 2017-247987 12/25/2017 Access Code Provided

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

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If Required, Foreign Filing License Granted: 10/01/2018

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 16/129,082**

Projected Publication Date: 06/27/2019

Non-Publication Request: No

Early Publication Request: No

Title

SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR MANUFACTURING SAME

Preliminary Class

257

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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Title 37, Code of Federal Regulations, 5.11 & 5.15

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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 16/129,082

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	300
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	660
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	760
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =	*			OR	x 100 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*				x 460 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1720

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

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This is to certify that the annexed is a true copy of the following application as filed with this Office.

出願年月日 Date of Application:	２０１７年１２月２５日
出願番号 Application Number:	特願２０１７－２４７９８７
パリ条約による外国への出願に用いる優先権の主張の基礎となる出願の国コードと出願番号 The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is	ＪＰ２０１７－２４７９８７
出願人 Applicant(s):	東芝メモリ株式会社

２０１８年１０月２３日

特許庁長官
Commissioner,
Japan Patent Office　宗像直

【書類名】　特許願
【整理番号】　11722301
【提出日】　平成29年12月25日
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【手数料の表示】
　【振替番号】　00038575
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【提出物件の目録】
　【物件名】　明細書　1
　【物件名】　特許請求の範囲　1
　【物件名】　要約書　1
　【物件名】　図面　1

【書類名】明細書
【発明の名称】半導体記憶装置及びその製造方法
【技術分野】
【０００１】
実施形態は、半導体記憶装置及びその製造方法に関する。
【背景技術】
【０００２】
近年、メモリセルを３次元的に集積させた積層型の半導体記憶装置が提案されている。このような積層型の半導体記憶装置においては、より一層の小型化を図るために、半導体基板とメモリセルとの間に厚い絶縁膜を設け、半導体基板の上層部分及び絶縁膜内に制御回路を形成することが検討されている。この場合は、絶縁膜上に導電膜を設け、ソース線として使用する。
【先行技術文献】
【特許文献】
【０００３】
【特許文献１】特開２０１０―１６５７９４号公報
【特許文献２】米国特許出願公開第２０１１／００７３８６６号明細書
【発明の概要】
【発明が解決しようとする課題】
【０００４】
実施形態の目的は、小型化が可能な半導体記憶装置及びその製造方法を提供することである。
【課題を解決するための手段】
【０００５】
実施形態に係る半導体記憶装置は、上層部分にダイオードが形成された半導体基板と、前記半導体基板上に設けられた第１絶縁膜と、前記第１絶縁膜上に設けられ、前記ダイオードに接続された第１導電膜と、前記第１導電膜上に設けられ、絶縁体及び電極膜が交互に積層された積層体と、前記積層体を貫通し、前記第１導電膜に接続された半導体部材と、前記電極膜と前記半導体部材との間に設けられた電荷蓄積部材と、を備える。
【０００６】
実施形態に係る半導体記憶装置の製造方法は、半導体基板の上層部分にダイオードを形成する工程と、前記半導体基板上に第１絶縁膜を形成する工程と、前記第１絶縁膜上に前記ダイオードに接続される第１導電膜を形成する工程と、前記第１導電膜上に、第１絶縁材料膜及び第２絶縁材料膜を交互に形成することにより、積層体を形成する工程と、反応性イオンエッチングを施すことにより、前記積層体に前記第１導電膜まで到達するホールを形成する工程と、前記ホールの内面上に電荷蓄積部材を形成する工程と、前記電荷蓄積部材が形成された前記ホール内に、前記第１導電膜に接続される半導体部材を形成する工程と、前記半導体部材を形成した後、前記第２絶縁材料膜を電極膜に置換する工程と、を備える。
【図面の簡単な説明】
【０００７】
【図１】第１の実施形態に係る半導体記憶装置を示す断面図である。
【図２】第１の実施形態に係る半導体記憶装置を示す断面図である。
【図３】第１の実施形態に係る半導体記憶装置を示す上面図である。
【図４】第１の実施形態に係る半導体記憶装置のメモリセルトランジスタ周辺を示す断面図である。
【図５】第１の実施形態に係る半導体記憶装置のメモリセルトランジスタ周辺を示す断面図である。
【図６】第１の実施形態に係る半導体記憶装置の製造方法を示す断面図である。
【図７】第１の実施形態に係る半導体記憶装置の製造方法を示す断面図である。

【図８】第１の実施形態に係る半導体記憶装置の製造方法を示す断面図である。
【図９】第１の実施形態に係る半導体記憶装置の製造方法を示す断面図である。
【図１０】第１の実施形態に係る半導体記憶装置の製造方法を示す断面図である。
【図１１】第２の実施形態に係る半導体記憶装置を示す断面図である。
【図１２】第３の実施形態に係る半導体記憶装置を示す断面図である。
【図１３】第３の実施形態に係る半導体記憶装置の製造方法を示す断面図である。
【図１４】第３の実施形態に係る半導体記憶装置の製造方法を示す断面図である。

【発明を実施するための形態】

【０００８】

（第１の実施形態）

以下、第１の実施形態について説明する。

図１及び図２は、本実施形態に係る半導体記憶装置を示す断面図である。

図３は、本実施形態に係る半導体記憶装置を示す上面図である。

図４及び図５は、本実施形態に係る半導体記憶装置のメモリセルトランジスタ周辺を示す断面図である。

なお、各図は模式的なものであり、適宜誇張及び省略して描かれている。例えば、各構成要素は実際よりも少なく且つ大きく描かれている。また、図間において、構成要素の数及び寸法比等は、必ずしも一致していない。

本実施形態に係る半導体記憶装置は、積層型のＮＡＮＤフラッシュメモリである。

【０００９】

図１に示すように、本実施形態に係る半導体記憶装置１においては、シリコン基板１０が設けられている。シリコン基板１０は、例えば、単結晶のシリコン（Ｓｉ）により形成されている。

【００１０】

図２に示すように、例えば、シリコン基板１０の本体部分の導電形はｐ形である。そして、シリコン基板１０の上層部分の一部には、ｎ形ウェル１１が形成されている。ｎ形ウェル１１の上層部分の一部には、ｐ形ウェル１２が形成されている。ｐ形ウェル１２の上層部分の一部には、n^+形拡散層１３が形成されている。n^+形拡散層１３のドナー濃度はｎ形ウェル１１のドナー濃度よりも高い。

【００１１】

シリコン基板１０とｎ形ウェル１１との界面にはダイオード２１が形成され、ｐ形ウェル１２とｎ形ウェル１１との界面にはダイオード２２が形成され、ｐ形ウェル１２とn^+形拡散層１３との界面にはダイオード２３が形成される。ダイオード２１、ダイオード２２及びダイオード２３が直列に接続されることにより、双方向ダイオード２０が形成される。シリコン基板１０の上層部分の一部には、１つ又は複数の双方向ダイオード２０が形成されている。

【００１２】

シリコン基板１０の上層部分には、拡散層１５及びＳＴＩ（Shallow Trench Isolation：素子分離絶縁膜）１６が形成されている。また、シリコン基板１０の上層部分には、例えば、ＭＯＳＦＥＴ（Metal-Oxide-Semiconductor Field-Effect Transistor：金属酸化物半導体電界効果トランジスタ）のソース・ドレイン層（図示せず）等も形成されている。

【００１３】

図１及び図２に示すように、シリコン基板１０上には、ゲート絶縁層３１が形成されており、その上には、絶縁膜３２が形成されている。ゲート絶縁層３１及び絶縁膜３２は、例えば、シリコン酸化物（ＳｉＯ）により形成されている。ゲート絶縁層３１は、例えば、シリコン基板１０を熱酸化することにより形成され、絶縁膜３２は、例えば、ＴＥＯＳ（Tetraethyl orthosilicate：$Si(OC_2H_5)_4$）を原料としたＣＶＤ（Chemical Vapor Deposition：化学気相成長）法により形成されている。

【００１４】

以下、本明細書においては、説明の便宜上、ＸＹＺ直交座標系を採用する。シリコン基板１０の上面１０ａに対して平行で、且つ、相互に直交する２方向を「Ｘ方向」及び「Ｙ方向」とし、シリコン基板１０の上面１０ａに対して垂直な方向を「Ｚ方向」とする。また、Ｚ方向のうち、シリコン基板１０から絶縁膜３２に向かう方向を「上」ともいい、その逆方向を「下」ともいうが、この表現も便宜的なものであり、重力の方向とは無関係である。

【００１５】

ゲート絶縁層３１上であって絶縁膜３２内には、ゲート電極３３が設けられている。ソース・ドレイン層（図示せず）、ゲート絶縁層３１及びゲート電極３３により、ＭＯＳＦＥＴ３５が形成される。絶縁膜３２内には、配線３６及びプラグ３７が形成されている。プラグ３７の一部は配線３６同士を接続し、プラグ３７の他の一部は、配線３６をシリコン基板１０の拡散層１５に接続する。ＭＯＳＦＥＴ３５、一部の配線３６及び一部のプラグ３７は、制御回路３９を構成する。なお、制御回路３９には、他の要素が含まれていてもよい。絶縁膜３２内における最上段の配線３６上には、プラグ４０が設けられている。

【００１６】

絶縁膜３２上には、ソース電極膜４１が設けられている。ソース電極膜４１の形状は、ＸＹ平面に沿って拡がる略平板状であり、後述するように、所定の形状にパターニングされている。ソース電極膜４１においては、例えばタングステン（Ｗ）からなる金属層４２が設けられており、金属層４２上には、例えば多結晶のシリコン（Ｓｉ）からなるシリコン層４３が設けられている。ソース電極膜４１の周囲には、絶縁膜４４が設けられている。また、ソース電極膜４１によって囲まれた領域には、Ｚ方向においてソース電極膜４１を貫く絶縁膜４５が設けられている。

【００１７】

ソース電極膜４１の下面の一部は、プラグ４０に接している。これにより、ソース電極膜４１の一部はプラグ４０の上端に接続されている。プラグ４０の下端は、最上段の配線３６の一部に接続されている。この配線３６は、プラグ３７を介してより下段の配線３６に接続されており、最下段の配線３６の一部は、プラグ３７を介してｎ＋形拡散層１３の上面に接続されている。これにより、ソース電極膜４１の一部は、プラグ４０、複数の配線３６及び複数のプラグ３７を介して、双方向ダイオード２０の一端に接続されている。ソース電極膜４１から双方向ダイオード２０に至る電流経路は、制御回路３９から絶縁されている。

【００１８】

ソース電極膜４１上には、積層体５０が設けられている。積層体５０においては、絶縁膜５１及び電極膜５２がＺ方向に沿って交互に積層されている。絶縁膜５１は例えばシリコン酸化物からなり、電極膜５２は例えばタングステンからなる。また、積層体５０の端部の形状は、電極膜５２毎にテラスが形成された階段状である。なお、絶縁膜５１に代わる絶縁体として、エアギャップが形成されていてもよい。

【００１９】

積層体５０内には、柱状部６０が設けられている。柱状部６０の形状は、中心軸がＺ方向に延びる円柱形である。柱状部６０の下部には、シリコン部材６１が設けられており、シリコン部材６１上には、シリコンピラー６２が設けられている。シリコンピラー６２の周囲には、メモリ膜６３が設けられている。シリコンピラー６２はシリコン部材６１に接続されており、シリコン部材６１はソース電極膜４１に接続されている。

【００２０】

図４及び図５に示すように、シリコンピラー６２内には、シリコン酸化物からなるコア部材６４が設けられている。メモリ膜６３においては、内側、すなわち、シリコンピラー６２側から外側に向かって、トンネル絶縁膜６５、電荷蓄積膜６６及びシリコン酸化層６７がこの順に設けられている。一方、電極膜５２の上面上、下面上及びシリコンピラー６２に対向する側面上には、アルミニウム酸化層６８が設けられている。シリコン酸化層６７及びアルミニウム酸化層６８により、ブロック絶縁膜６９が構成されている。

【００２１】
トンネル絶縁膜６５は、通常は絶縁性であるが、半導体記憶装置１の駆動電圧の範囲内にある所定の電圧が印加されるとトンネル電流を流す膜であり、例えば、単層のシリコン酸化膜、又は、シリコン酸化層、シリコン窒化層及びシリコン酸化層がこの順に積層されたＯＮＯ膜である。電荷蓄積膜６６は電荷を蓄積する能力がある膜であり、例えば電子のトラップサイトを含む材料からなり、例えば、シリコン窒化物からなる。ブロック絶縁膜６９は、半導体記憶装置１の駆動電圧の範囲内で電圧が印加されても実質的に電流を流さない膜である。
【００２２】
トンネル絶縁膜６５、電荷蓄積膜６６及びブロック絶縁膜６９により、メモリ膜６３が形成されている。メモリ膜６３は、シリコンピラー６２と電極膜５２との間に配置されている。シリコン部材６１、シリコンピラー６２、メモリ膜６３及びコア部材６４により、柱状部６０が構成されている。シリコンピラー６２は、メモリ膜６３によって、電極膜５２から絶縁されている。シリコン部材６１も、絶縁膜（図示せず）によって、電極膜５２から絶縁されている。
【００２３】
図１～図３に示すように、ソース電極膜４１上及び絶縁膜４４上における積層体５０の周囲には、例えばシリコン酸化物からなる絶縁膜７０が設けられている。絶縁膜７０内には、積層体５０を略囲むように、絶縁板７１が設けられている。絶縁板７１は積層体５０から離隔している。絶縁板７１は、ソース電極膜４１を貫通し、絶縁膜３２に到達している。また、積層体５０内には、Ｘ方向に延びる複数枚の絶縁板７２が設けられている。絶縁板７２は、積層体５０における絶縁膜５１及び電極膜５２を貫通し、ソース電極膜４１に到達している。絶縁板７２によりＹ方向に分離された積層体５０のそれぞれは、例えばデータ消去の最小単位となるブロックを形成する。絶縁板７１及び７２は、例えば、シリコン酸化物により形成されている。なお、絶縁板７１と絶縁板７２は、相互に連結していてもよい。また、絶縁板７１の形状は、Ｚ方向から見て積層体５０を囲むような枠状であってもよい。但し、この場合も、絶縁板７１は積層体５０から離隔している。
【００２４】
絶縁板７１により、ソース電極膜４１は、絶縁板７１の内側に配置された中央部分４１ａと、絶縁板７１の外側に配置された周辺部分４１ｂとに分断されている。中央部分４１ａと周辺部分４１ｂとは絶縁板７１によって相互に絶縁されている。換言すれば、絶縁板７１の下部は、中央部分４１ａと周辺部分４１ｂの間に配置されている。中央部分４１ａは、シリコン部材６１を介してシリコンピラー６２に接続されている。周辺部分４１ｂは、プラグ４０、配線３６及びプラグ３７を介して双方向ダイオード２０に接続されている。
【００２５】
積層体５０上及び絶縁膜７０上には、Ｙ方向に延びるビット線７５が設けられている。ビット線７５はシリコンピラー６２の上端に接続されている。積層体５０上及び絶縁膜７０上には、ビット線７５を覆うように、絶縁膜７６が設けられている。絶縁膜７６内には、プラグ７７が設けられている。制御回路３９の配線３６とプラグ７７との間には、積層体５０及びソース電極膜４１によって囲まれた絶縁膜４５を貫通するようにＺ方向に延びる貫通ビア７８が設けられている。貫通ビア７８の周囲には、例えばシリコン酸化物からなる絶縁膜７９が設けられている。貫通ビア７８は絶縁膜７９によって、電極膜５２及びソース電極膜４１から絶縁されている。プラグ７７上には、上層配線８０が設けられており、プラグ７７に接続されている。
【００２６】
図２及び図３に示すように、絶縁膜７０内には、コンタクト８１～８３が設けられている。コンタクト８１の下端は電極膜５２に接続されており、上端は上層配線の一部（図示せず）に接続されている。コンタクト８２の下端はソース電極膜４１に接続されており、上端は上層配線の他の一部（図示せず）に接続されている。コンタクト８３の下端はシリ

コン基板１０の拡散層１５等に接続されており、上端は上層配線の更に他の一部（図示せず）に接続されている。

【００２７】

本実施形態に係る半導体記憶装置１においては、電極膜５２とシリコンピラー６２との交差部分毎に、メモリセル５９が形成される。メモリセル５９のチャネルはシリコンピラー６２であり、ゲート絶縁膜はトンネル絶縁膜６５及びブロック絶縁膜６９であり、ゲートは電極膜５２であり、電荷蓄積部材は電荷蓄積膜６６である。そして、制御回路３９が、ソース電極膜４１、ビット線７５及び各電極膜５２の電位を制御することにより、シリコンピラー６２から電荷蓄積膜６６に電荷を注入したり、電荷蓄積膜６６からシリコンピラー６２に電荷を排出したりする。これにより、メモリセル５９の閾値電圧を変化させ、データを記憶する。

【００２８】

次に、本実施形態に係る半導体記憶装置の製造方法について説明する。

図６～図１０は、本実施形態に係る半導体記憶装置の製造方法を示す断面図である。

【００２９】

先ず、図６及び図２に示すように、シリコン基板１０の上層部分に、ｎ形ウェル１１、ｐ形ウェル１２、ｎ＋形拡散層１３、拡散層１５及びＳＴＩ１６等を形成する。これにより、シリコン基板１０の上層部分の一部に、双方向ダイオード２０が形成される。

【００３０】

次に、熱酸化処理を施すことにより、シリコン基板１０の上面１０ａにゲート絶縁層３１を形成する。次に、例えばＴＥＯＳを原料としたＣＶＤ法を繰り返して絶縁膜３２を形成しつつ、ゲート電極３３、プラグ３７、配線３６及びプラグ４０を形成する。これにより、シリコン基板１０の上層部分及び絶縁膜３２内に、制御回路３９が形成される。このとき、プラグ４０は、一部のプラグ３７及び一部の配線３６を介して、ｎ＋形拡散層１３に接続される。

【００３１】

次に、絶縁膜３２上に金属層４２を形成し、その上にシリコン層４３を堆積することにより、ソース電極膜４１を形成する。次に、ソース電極膜４１をパターニングして、ソース電極膜４１の周囲に絶縁膜４４を形成すると共に、ソース電極膜４１によって囲まれた領域に絶縁膜４５を形成する。

【００３２】

次に、ソース電極膜４１、絶縁膜４４及び絶縁膜４５上に、シリコン酸化物からなる絶縁膜５１とシリコン窒化物（ＳｉＮ）からなる絶縁性の犠牲膜９１を交互に堆積させて、積層体５０を形成する。なお、犠牲膜９１の材料はシリコン窒化物には限定されないが、絶縁性であって絶縁膜５１との間でエッチング選択比がとれる材料とする。次に、積層体５０の端部を、犠牲膜９１毎にテラスが形成された階段状に加工する。次に、シリコン酸化物を堆積させることにより、積層体５０の周囲に絶縁膜７０を形成する。

【００３３】

次に、図７に示すように、積層体５０上及び絶縁膜７０上にマスクパターン９２を形成する。次に、マスクパターン９２をマスクとして、反応性イオンエッチング（Reactive Ion Etching：ＲＩＥ）を施す。具体的には、エッチングガスをプラズマ化することにより、エッチング種を陽イオンとし、電界を印加して陽イオンを加速し、マスクパターン９２を介して積層体５０に選択的に衝突させる。これにより、積層体５０にメモリホール９３が形成される。このとき、積層体５０は、絶縁性材料、すなわち、シリコン酸化物及びシリコン窒化物から形成されているため、メモリホール９３内には、エッチング種の陽イオンに由来する正の電荷が蓄積される。一方、この段階の中間構造体の外表面上には、負電荷が蓄積される。なお、図７においては、正電荷を「＋」を円で囲んだ記号で表し、負電荷を「―」を円で囲んだ記号で表している。

【００３４】

そして、図８に示すように、メモリホール９３がソース電極膜４１に到達すると、メモ

リホール９３内に蓄積されていた正電荷はソース電極膜４１に移動し、更に、図８に経路Ｅとして示すように、プラグ４０、配線３６、プラグ３７を経由して、ｎ＋形拡散層１３に流入する。これにより、双方向ダイオード２０のダイオード２３及びダイオード２１が降伏し、正電荷は双方向ダイオード２０を介してシリコン基板１０内に流入し、シリコン基板１０を介して外部に排出される。この結果、絶縁膜３２内におけるアーキングを防止することができる。

【００３５】

次に、図９、図４及び図５に示すように、メモリホール９３の下部内において、シリコン層４３を起点としてシリコンをエピタキシャル成長させることにより、シリコン部材６１を形成する。次に、シリコン部材６１上において、メモリホール９３の内面上にシリコン酸化層６７、電荷蓄積膜６６、トンネル絶縁膜６５、シリコンピラー６２及びコア部材６４を形成する。シリコンピラー６２は、シリコン部材６１を介して、ソース電極膜４１に接続される。次に、積層体５０、絶縁膜４５、絶縁膜３２の上部を貫通し、配線３６の一部に到達するように、貫通ビアホール９４を形成する。次に、貫通ビアホール９４の内面上に絶縁膜７９を形成し、絶縁膜７９の内面上に貫通ビア７８を形成する。貫通ビア７８は配線３６に接続される。

【００３６】

次に、図１０及び図３に示すように、絶縁膜７０及びソース電極膜４１を貫くように、スリット９５を形成すると共に、積層体５０を貫くように、スリット９６を形成する。スリット９５により、ソース電極膜４１が、中央部分４１ａと周辺部分４１ｂとに分断される。プラグ４０は周辺部分４１ｂのみに接続されているため、この分断により、中央部分４１ａがシリコン基板１０から絶縁される。次に、スリット９６を介してウェットエッチングを施し、犠牲膜９１（図９参照）を除去する。この結果、犠牲膜９１を除去したあとにスペース９７が形成される。

【００３７】

次に、図１、図４及び図５に示すように、スペース９７の内面上に、スリット９６を介してアルミニウム酸化層６８を形成する。アルミニウム酸化層６８はシリコン酸化層６７に接触し、シリコン酸化層６７と共にブロック絶縁膜６９を形成する。トンネル絶縁膜６５、電荷蓄積膜６６及びブロック絶縁膜６９により、メモリ膜６３が形成される。次に、スリット９６を介して、スペース９７の内面上にバリアメタル層（図示せず）を形成し、その後、スペース９７内にタングステン等の導電材料を埋め込んで、電極膜５２を形成する。次に、エッチングを施すことにより、電極膜５２及びアルミニウム酸化層６８のうち、スリット９５内及びスリット９６内に形成された部分を除去する。次に、スリット９５内及びスリット９６内にシリコン酸化物を埋め込むことにより、スリット９５内に絶縁板７１を形成すると共に、スリット９６内に絶縁板７２（図３参照）を形成する。

【００３８】

次に、図１に示すように、積層体５０上及び絶縁膜７０上に、Ｙ方向に延びるビット線７５を形成し、シリコンピラー６２に接続する。また、積層体５０上及び絶縁膜７０上に絶縁膜７６を形成すると共に、絶縁膜７６内にプラグ７７及び上層配線８０を形成する。上層配線８０はプラグ７７を介して貫通ビア７８に接続する。このようにして、本実施形態に係る半導体記憶装置１が製造される。

【００３９】

次に、本実施形態の効果について説明する。

本実施形態においては、図６に示すように、シリコン基板１０の上層部分に双方向ダイオード２０を形成する。また、絶縁膜３２上にソース電極膜４１を形成したときに、ソース電極膜４１が、プラグ４０、配線３６及びプラグ３７を介して、双方向ダイオード２０に接続されるようにする。これにより、図８に示すように、メモリホール９３がソース電極膜４１に到達したときに、メモリホール９３内に蓄積された正電荷によって双方向ダイオード２０が降伏し、この正電荷が、ソース電極膜４１、プラグ４０、配線３６、プラグ３７、ｎ＋形拡散層１３、ｐ形ウェル１２及びｎ形ウェル１１を介してシリコン基板１０

に流れ、外部に放出される。これにより、絶縁膜３２内におけるアーキングを防止し、絶縁膜３２が破壊されることを回避できる。

【００４０】

また、図１０に示すように、スリット９５を形成することにより、ソース電極膜４１を中央部分４１ａと周辺部分４１ｂとに分断する。この結果、図１に示す完成後の半導体記憶装置１において、シリコンピラー６２が接続されるソース電極膜４１の中央部分４１ａを、シリコン基板１０から確実に絶縁することができると共に、ソース電極膜４１の寄生容量が減少する。この結果、半導体記憶装置１の動作が安定化且つ高速化する。

【００４１】

（第２の実施形態）

次に、第２の実施形態について説明する。

図１１は、本実施形態に係る半導体記憶装置を示す断面図である。

【００４２】

図１１に示すように、本実施形態に係る半導体記憶装置２は、前述の第１の実施形態に係る半導体記憶装置１（図１～図５参照）と比較して、絶縁板７１が設けられていない点が異なっている。なお、半導体記憶装置２においても、絶縁板７２（図３参照）は設けられている。

【００４３】

半導体記憶装置２は、図１０に示す工程において、スリット９６（図３参照）のみを形成し、スリット９５を形成しないことにより、製造することができる。

【００４４】

本実施形態によっても、前述の第１の実施形態と同様に、メモリホール９３（図７参照）内に蓄積された正電荷が、ソース電極膜４１、プラグ４０、配線３６及びプラグ３７を介して双方向ダイオード２０に流れ、双方向ダイオード２０を降伏させて、シリコン基板１０を介して外部に排出される。この結果、絶縁膜３２が破壊されることを回避できる。

【００４５】

また、本実施形態に係る半導体記憶装置２においては、ソース電極膜４１は絶縁板７１（図１及び図３参照）によって分断されていないが、ソース電極膜４１とシリコン基板１０との間には双方向ダイオード２０が介在しているため、所定の電位差の範囲内で、ソース電極膜４１をシリコン基板１０から電気的に独立に駆動することができる。

本実施形態における上記以外の構成、製造方法及び効果は、前述の第１の実施形態と同様である。

【００４６】

（第３の実施形態）

次に、第３の実施形態について説明する。

図１２は、本実施形態に係る半導体記憶装置を示す断面図である。

【００４７】

図１２に示すように、本実施形態に係る半導体記憶装置３においては、前述の第１の実施形態に係る半導体記憶装置１（図１～図５参照）の構成に加えて、導電性のポリシリコンからなるシリコン膜５４、絶縁膜５５及びプラグ５６が設けられている。また、絶縁板７１によってソース電極膜４１は分断されておらず、シリコン膜５４が分断されている。更に、シリコン部材６１（図１参照）は設けられておらず、シリコンピラー６２はソース電極膜４１に直接接続されている。

【００４８】

以下、詳細に説明する。

シリコン膜５４は、ソース電極膜４１と積層体５０との間に配置されており、その形状は、ＸＹ平面に沿って拡がる略平板状である。絶縁膜５５は、ソース電極膜４１とシリコン膜５４との間に配置されている。プラグ５６は、絶縁膜５５及びソース電極膜４１のシリコン層４３を貫通し、その下端はソース電極膜４１の金属層４２に接し、その上端はシリコン膜５４に接している。これにより、シリコン膜５４の一部は、プラグ５６を介して

ソース電極膜４１に接続されている。第１の実施形態と同様に、ソース電極膜４１はプラグ４０を介して双方向ダイオード２０に接続されている。従って、シリコン膜５４の一部はシリコン基板１０の上層部分の一部に形成された双方向ダイオード２０に接続されている。シリコン膜５４から双方向ダイオード２０に至る電流経路は、制御回路３９から絶縁されている。絶縁膜４４は、ソース電極膜４１、絶縁膜５５及びシリコン膜５４からなる積層体の周囲に設けられている。絶縁膜４５は、この積層体をＺ方向に貫いている。

【００４９】

また、絶縁板７１及び絶縁板７２（図３参照）は、Ｚ方向においてシリコン膜５４を貫通しているが、ソース電極膜４１は貫通していない。このため、絶縁板７１によって、シリコン膜５４は中央部分５４ａと周辺部分５４ｂに分断されているが、ソース電極膜４１は分断されていない。プラグ５６は、シリコン膜５４の周辺部分５４ｂに接続されている。また、前述の第１の実施形態と同様に、積層体５０をＹ方向に複数のブロックに分離する絶縁板７２は、例えば、ともにシリコン膜５４を貫通する絶縁板７１と相互に連結されて、積層体５０の下方に位置するシリコン膜５４の中央部分５４ａを、Ｙ方向に並ぶ複数のブロック間で分離させる。

【００５０】

柱状部６０において、シリコン部材６１は設けられておらず、シリコンピラー６２の下端がソース電極膜４１に接している。シリコンピラー６２はシリコン膜５４の中央部分５４ａを貫いており、アルミニウム酸化層６８を除くメモリ膜６３によって、シリコン膜５４から絶縁されている。シリコン膜５４の中央部分５４ａは、シリコンピラー６２に対して、最下段のゲート電極、例えば、シリコンピラー６２の導通／非導通をブロック毎に切り替えるセレクトゲートとして機能する。

【００５１】

次に、本実施形態に係る半導体記憶装置の製造方法について説明する。

図１３及び図１４は、本実施形態に係る半導体記憶装置の製造方法を示す断面図である。

【００５２】

先ず、図１３に示すように、前述の第１の実施形態と同様な方法により、シリコン基板１０からソース電極膜４１までの構造体を作製する。

【００５３】

次に、ソース電極膜４１上に絶縁膜５５を形成すると共に、絶縁膜５５及びソース電極膜４１のシリコン層４３内にプラグ５６を形成し、その上にシリコン膜５４を形成する。次に、シリコン膜５４及び絶縁膜５５をパターニングし、ソース電極膜４１、シリコン膜５４及び絶縁膜５５からなる積層体の周囲に絶縁膜４４を形成すると共に、この積層体によって囲まれた領域に絶縁膜４５を形成する。

【００５４】

次に、シリコン膜５４上に、シリコン酸化物からなる絶縁膜５１及びシリコン窒化物からなる犠牲膜９１を交互に堆積させて、積層体５０を形成する。次に、積層体５０の周囲に絶縁膜７０を形成する。次に、積層体５０上及び絶縁膜７０上にマスクパターン９２を形成する。次に、マスクパターン９２をマスクとし、シリコン膜５４をエッチングストッパとしてＲＩＥを施し、積層体５０にメモリホール９３を形成する。ＲＩＥの条件は、シリコン酸化物及びシリコン窒化物が効率よくエッチングされるような条件とする。このとき、第１の実施形態と同様に、メモリホール９３内に正電荷が蓄積される。

【００５５】

そして、メモリホール９３がシリコン膜５４に到達すると、エッチング速度が低下する。これにより、メモリホール９３の下端の位置が揃う。このとき、メモリホール９３内に蓄積された正電荷がシリコン膜５４に移動する。そして、経路Ｅで示すように、プラグ５６を介してソース電極膜４１に移動し、プラグ４０、配線３６及びプラグ３７を介してｎ＋形拡散層１３に移動し、双方向ダイオード２０を降伏させて、シリコン基板１０に移動する。そして、シリコン基板１０を介して外部に排出される。これにより、絶縁膜５５及

び絶縁膜３２におけるアーキングを防止できる。
【００５６】
次に、図１４に示すように、ＲＩＥの条件をシリコンが効率よくエッチングされるような条件に変更して、ＲＩＥを継続する。これにより、メモリホール９３が絶縁膜５５に到達する。次に、ＲＩＥの条件をシリコン酸化物が効率よくエッチングされるような条件に変更して、ＲＩＥを継続する。これにより、メモリホール９３がソース電極膜４１のシリコン層４３に到達する。ここで、ＲＩＥを終了する。
【００５７】
次に、図１２、図４及び図５に示すように、メモリホール９３の内面上にシリコン酸化層６７、電荷蓄積膜６６、トンネル絶縁膜６５、シリコンピラー６２及びコア部材６４を形成する。シリコンピラー６２はシリコン層４３に接続される。次に、絶縁膜７９及び貫通ビア７８を形成する。
【００５８】
次に、図１２及び図３に示すように、シリコン膜５４を一旦エッチングストッパとして利用しつつ、絶縁膜７０と積層体５０及びこれらの下方をエッチングして、スリット９５及び９６を略均等な深さで形成する。スリット９５及び９６は、例えば、１つのマスクパターンをマスクとしたエッチングによって同時に形成することができる。このとき、スリット９５及び９６には、シリコン膜５４を貫通させるが、ソース電極膜４１は貫通させない。これにより、シリコン膜５４は、スリット９５により、中央部分５４ａと周辺部分５４ｂとに分断される。シリコンピラー６２は中央部分５４ａによって囲まれており、プラグ５６は周辺部分５４ｂのみに接続されているため、シリコン膜５４を分断することにより、最下段のゲート電極として機能するシリコン膜５４の中央部分５４ａを、ソース電極膜４１から絶縁することができる。以後の製造方法は、前述の第１の実施形態と同様である。
【００５９】
次に、本実施形態の効果について説明する。
本実施形態においても、前述の第１の実施形態と同様に、シリコン基板１０の上層部分に双方向ダイオード２０を形成し、ソース電極膜４１をプラグ４０、配線３６及びプラグ３７を介して、双方向ダイオード２０に接続している。また、シリコン膜５４をプラグ５６を介してソース電極膜４１に接続している。これにより、図１３に示すように、メモリホール９３がシリコン膜５４に到達したときに、双方向ダイオード２０が降伏し、メモリホール９３内に蓄積された正電荷が、シリコン膜５４、プラグ５６、ソース電極膜４１、プラグ４０、配線３６、プラグ３７、ｎ＋形拡散層１３、ｐ形ウェル１２及びｎ形ウェル１１を介してシリコン基板１０に流れ、外部に放出される。これにより、絶縁膜５５内及び絶縁膜３２内におけるアーキングを防止し、絶縁膜５５及び絶縁膜３２が破壊されることを回避できる。
【００６０】
また、図１２に示すように、スリット９５を形成することにより、シリコン膜５４を中央部分５４ａと周辺部分５４ｂとに分断する。この結果、完成後の半導体記憶装置３において、シリコンピラー６２に対して最下段のゲート電極として機能する中央部分５４ａを、ソース電極膜４１から確実に絶縁することができる。これにより、中央部分５４ａとソース電極膜４１を電気的に独立して駆動することができる。また、中央部分５４ａの寄生容量が減少する。
【００６１】
更に、ソース電極膜４１とシリコン基板１０との間には双方向ダイオード２０が介在しているため、所定の電位差の範囲内で、ソース電極膜４１をシリコン基板１０から電気的に独立して駆動することができる。
本実施形態における上記以外の構成、製造方法及び効果は、前述の第１の実施形態と同様である。
【００６２】

以上説明した実施形態によれば、小型化が可能な半導体記憶装置及びその製造方法を実現することができる。

【００６３】

以上、本発明のいくつかの実施形態を説明したが、これらの実施形態は、例として提示したものであり、発明の範囲を限定することは意図していない。これら新規な実施形態は、その他の様々な形態で実施されることが可能であり、発明の要旨を逸脱しない範囲で、種々の省略、置き換え、変更を行うことができる。これら実施形態やその変形は、発明の範囲や要旨に含まれるとともに、特許請求の範囲に記載された発明及びその等価物の範囲に含まれる。

【符号の説明】

【００６４】

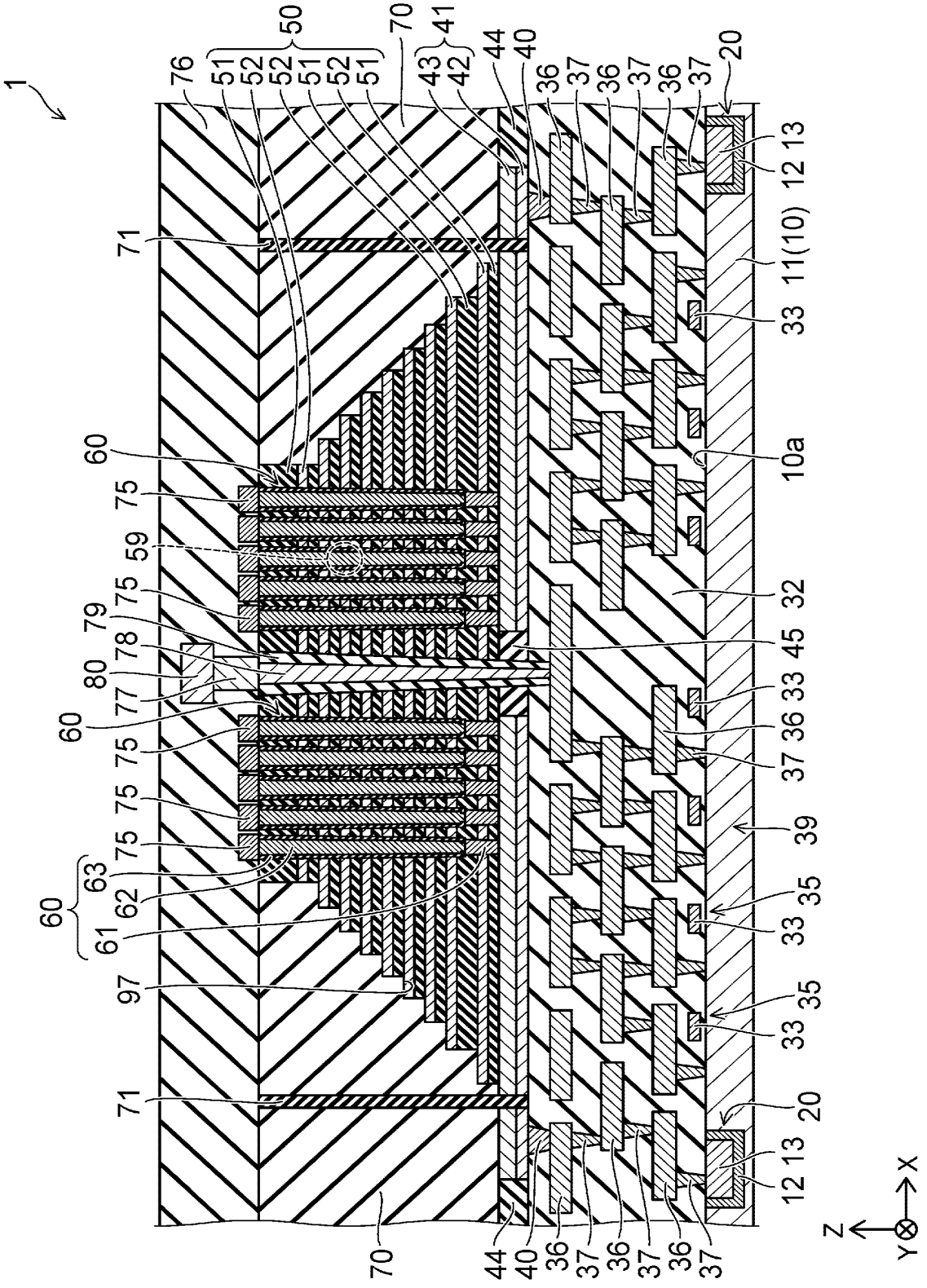
１、２、３：半導体記憶装置
１０：シリコン基板
１０ａ：上面
１１：ｎ形ウェル
１２：ｐ形ウェル
１３：n^+形拡散層
１５：拡散層
１６：ＳＴＩ
２０：双方向ダイオード
２１、２２、２３：ダイオード
３１：ゲート絶縁層
３２：絶縁膜
３３：ゲート電極
３６：配線
３７：プラグ
３９：制御回路
４０：プラグ
４１：ソース電極膜
４１ａ：中央部分
４１ｂ：周辺部分
４２：金属層
４３：シリコン層
４４、４５：絶縁膜
５０：積層体
５１：絶縁膜
５２：電極膜
５４：シリコン膜
５４ａ：中央部分
５４ｂ：周辺部分
５５：絶縁膜
５６：プラグ
５９：メモリセル
６０：柱状部
６１：シリコン部材
６２：シリコンピラー
６３：メモリ膜
６４：コア部材
６５：トンネル絶縁膜
６６：電荷蓄積膜

６７：シリコン酸化層
６８：アルミニウム酸化層
６９：ブロック絶縁膜
７０：絶縁膜
７１、７２：絶縁板
７５：ビット線
７６：絶縁膜
７７：プラグ
７８：貫通ビア
７９：絶縁膜
８０：上層配線
８１、８２、８３：コンタクト
９１：犠牲膜
９２：マスクパターン
９３：メモリホール
９４：貫通ビアホール
９５、９６：スリット
９７：スペース
Ｅ：経路

【書類名】特許請求の範囲
【請求項１】
上層部分にダイオードが形成された半導体基板と、
前記半導体基板上に設けられた第１絶縁膜と、
前記第１絶縁膜上に設けられ、前記ダイオードに接続された第１導電膜と、
前記第１導電膜上に設けられ、絶縁体及び電極膜が交互に積層された積層体と、
前記積層体を貫通し、前記第１導電膜に接続された半導体部材と、
前記電極膜と前記半導体部材との間に設けられた電荷蓄積部材と、
を備えた半導体記憶装置。
【請求項２】
前記ダイオードと前記第１導電膜との間に接続された第１プラグをさらに備え、
前記第１導電膜は、
前記半導体部材に接続された第１部分と、
前記第１プラグに接続され、前記第１部分から絶縁された第２部分と、
を有する請求項１記載の半導体記憶装置。
【請求項３】
前記第１導電膜と前記積層体との間に設けられた第２導電膜と、
前記第１導電膜と前記第２導電膜との間に設けられた第２絶縁膜と、
前記ダイオードと前記第１導電膜との間に接続された第１プラグと、
前記第１導電膜と前記第２導電膜との間に接続された第２プラグと、
をさらに備え、
前記第２導電膜は、
前記半導体部材を囲む第１部分と、
前記第２プラグに接続され、前記第１部分から絶縁された第２部分と、
を有する請求項１記載の半導体記憶装置。
【請求項４】
半導体基板の上層部分にダイオードを形成する工程と、
前記半導体基板上に第１絶縁膜を形成する工程と、
前記第１絶縁膜上に前記ダイオードに接続される第１導電膜を形成する工程と、
前記第１導電膜上に、第１絶縁材料膜及び第２絶縁材料膜を交互に形成することにより、積層体を形成する工程と、
反応性イオンエッチングを施すことにより、前記積層体に前記第１導電膜まで到達するホールを形成する工程と、
前記ホールの内面上に電荷蓄積部材を形成する工程と、
前記電荷蓄積部材が形成された前記ホール内に、前記第１導電膜に接続される半導体部材を形成する工程と、
前記半導体部材を形成した後、前記第２絶縁材料膜を電極膜に置換する工程と、
を備えた半導体記憶装置の製造方法。
【請求項５】
前記第１絶縁膜を形成する工程は、前記第１絶縁膜内に、前記ダイオードと前記第１導電膜との間に接続されるプラグを形成する工程を有し、
前記ホールを形成した後、前記第１導電膜を、前記半導体部材に接続された第１部分と前記プラグに接続された第２部分とに分割する工程をさらに備えた請求項４記載の半導体記憶装置の製造方法。

【書類名】要約書
【要約】
【課題】小型化が可能な半導体記憶装置及びその製造方法を提供する。
【解決手段】半導体記憶装置１は、上層部分にダイオード２０が形成された半導体基板１０と、前記半導体基板１０上に設けられた第１絶縁膜３２と、前記第１絶縁膜３２上に設けられ、前記ダイオード２０に接続された導電膜４１と、前記導電膜４１上に設けられ、絶縁膜５１及び電極膜５２が交互に積層された積層体５０と、前記積層体５０を貫通し、前記導電膜４１に接続された半導体部材６２と、前記電極膜５２と前記半導体部材６２との間に設けられた電荷蓄積部材６６と、を備える。
【選択図】図２

【書類名】図面
【図１】



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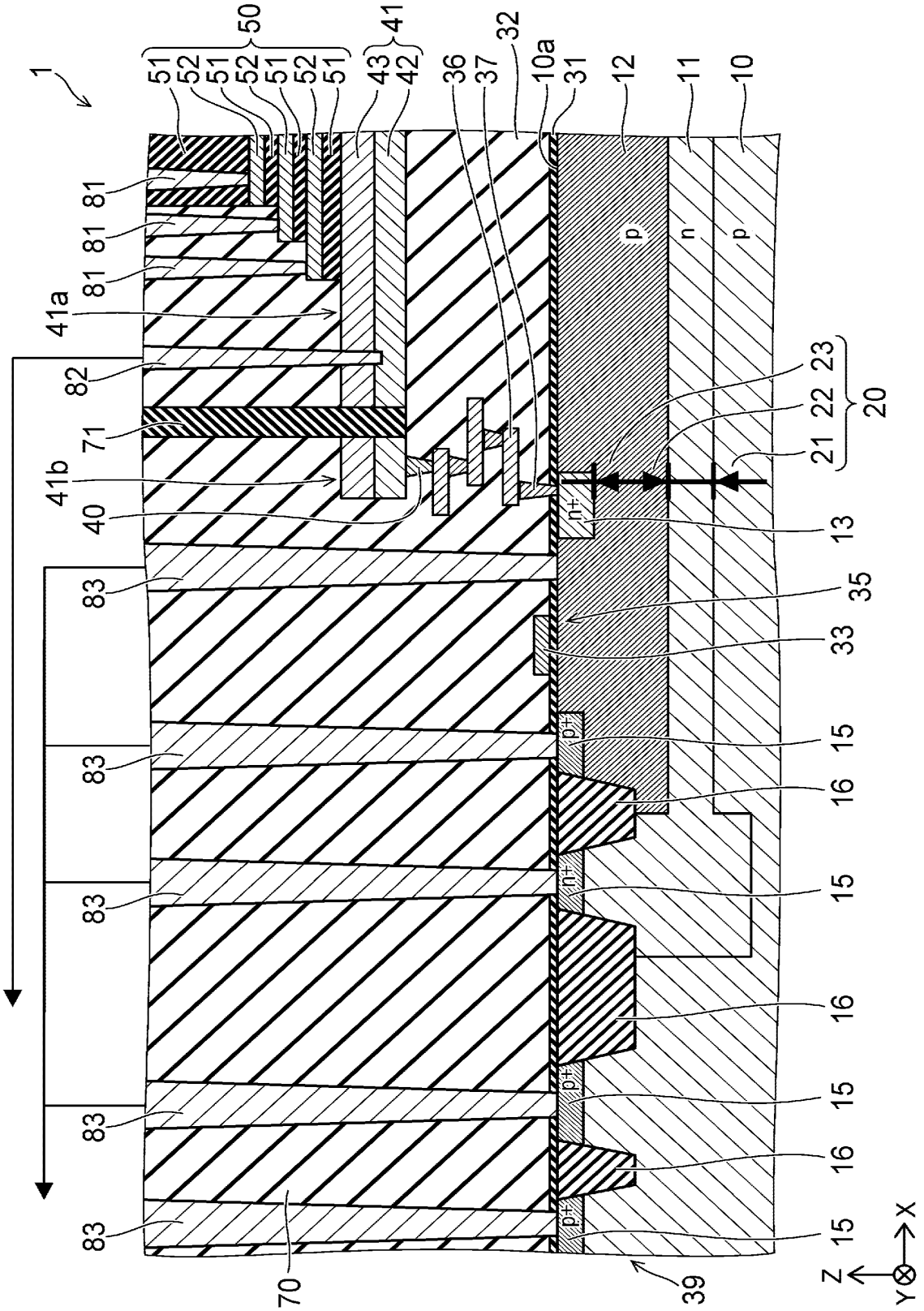

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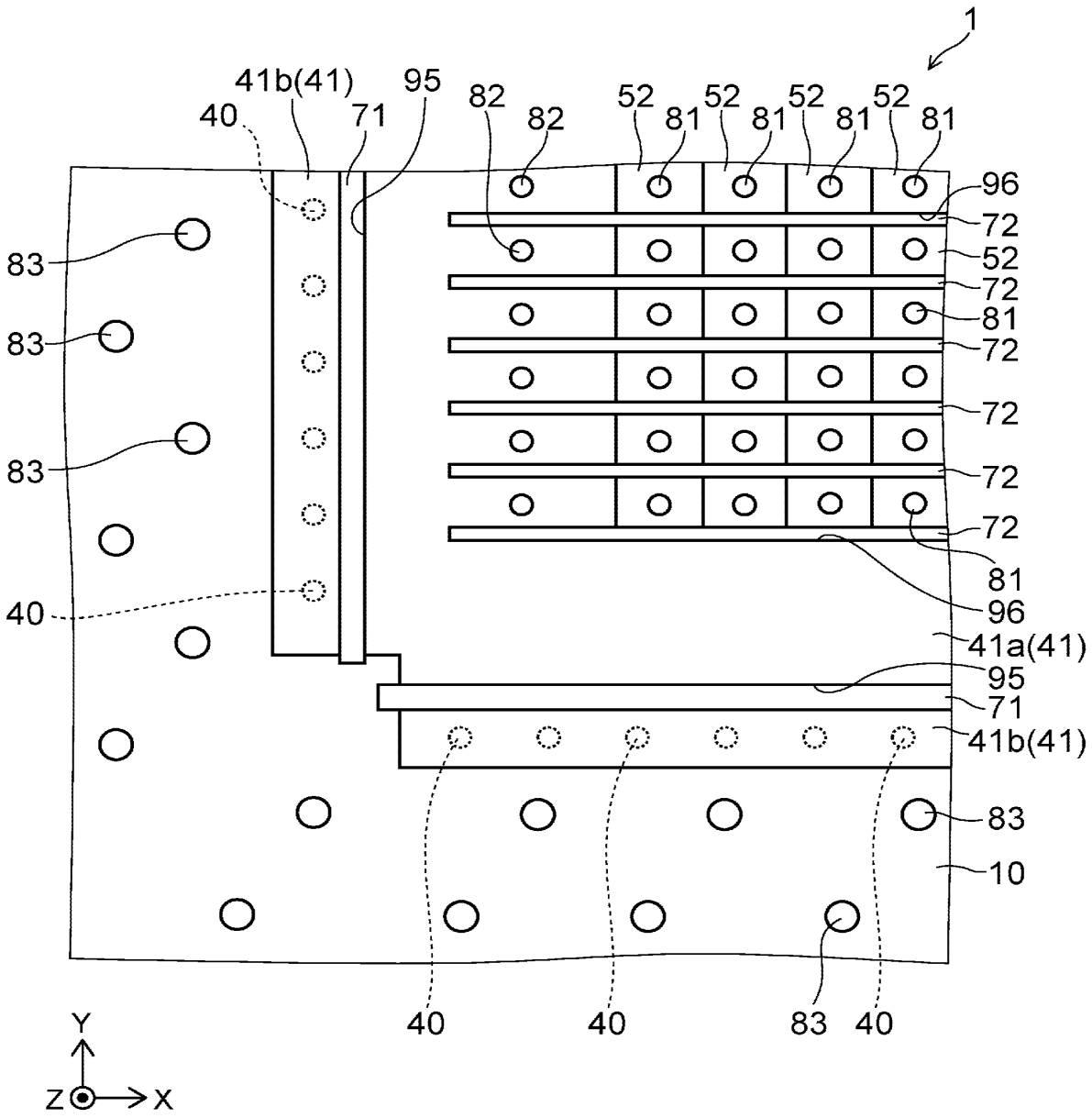
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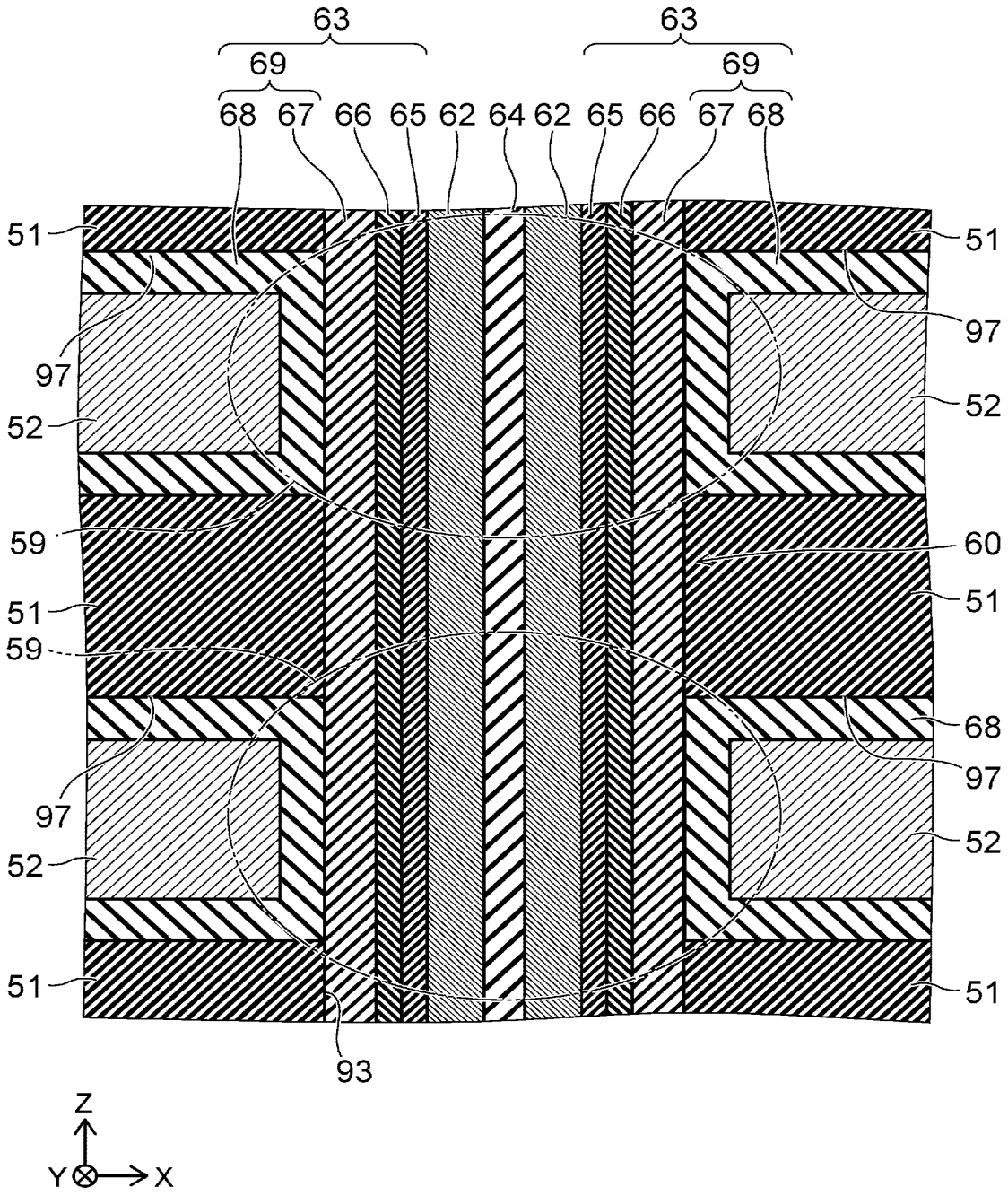
X

【図４】



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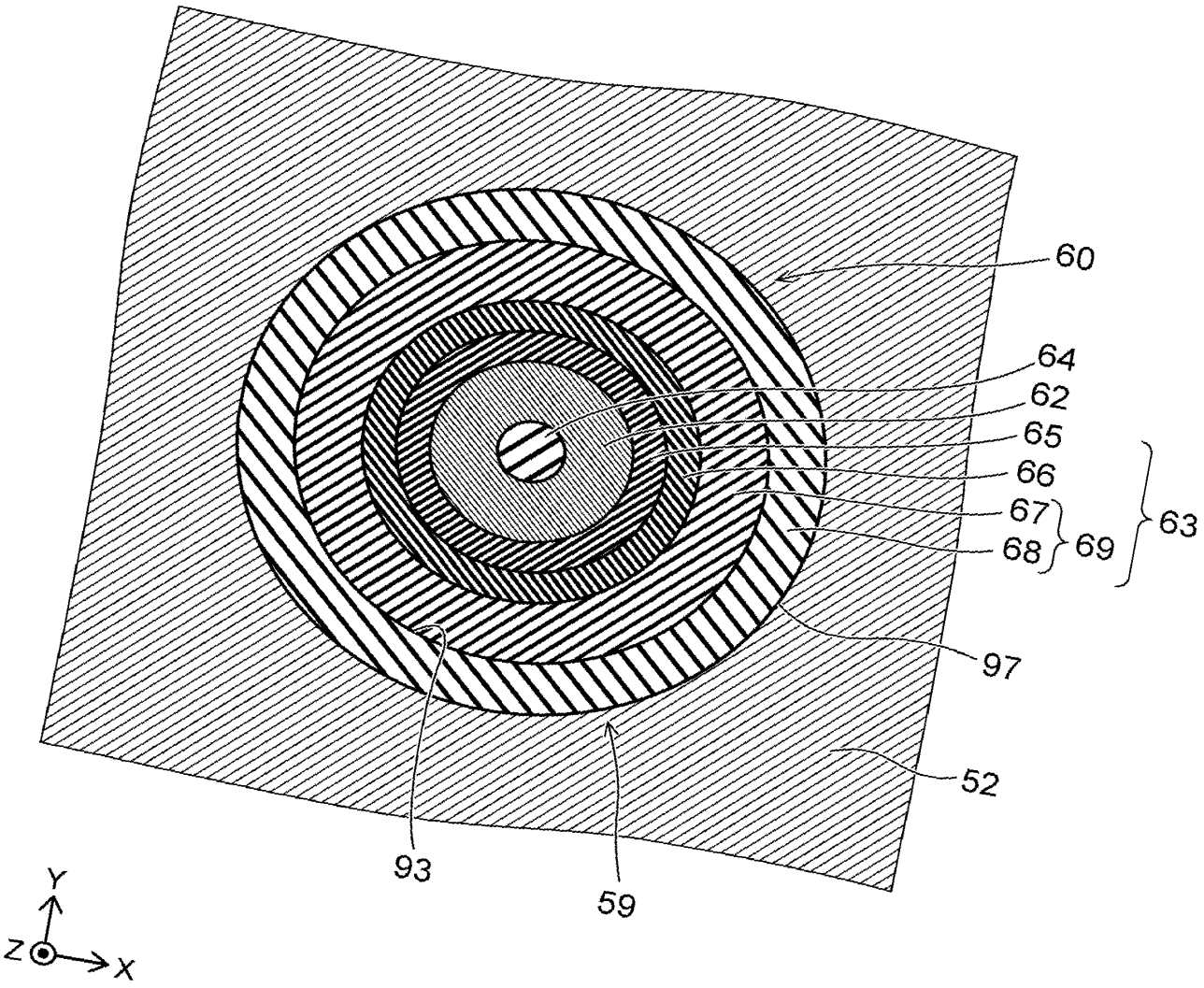

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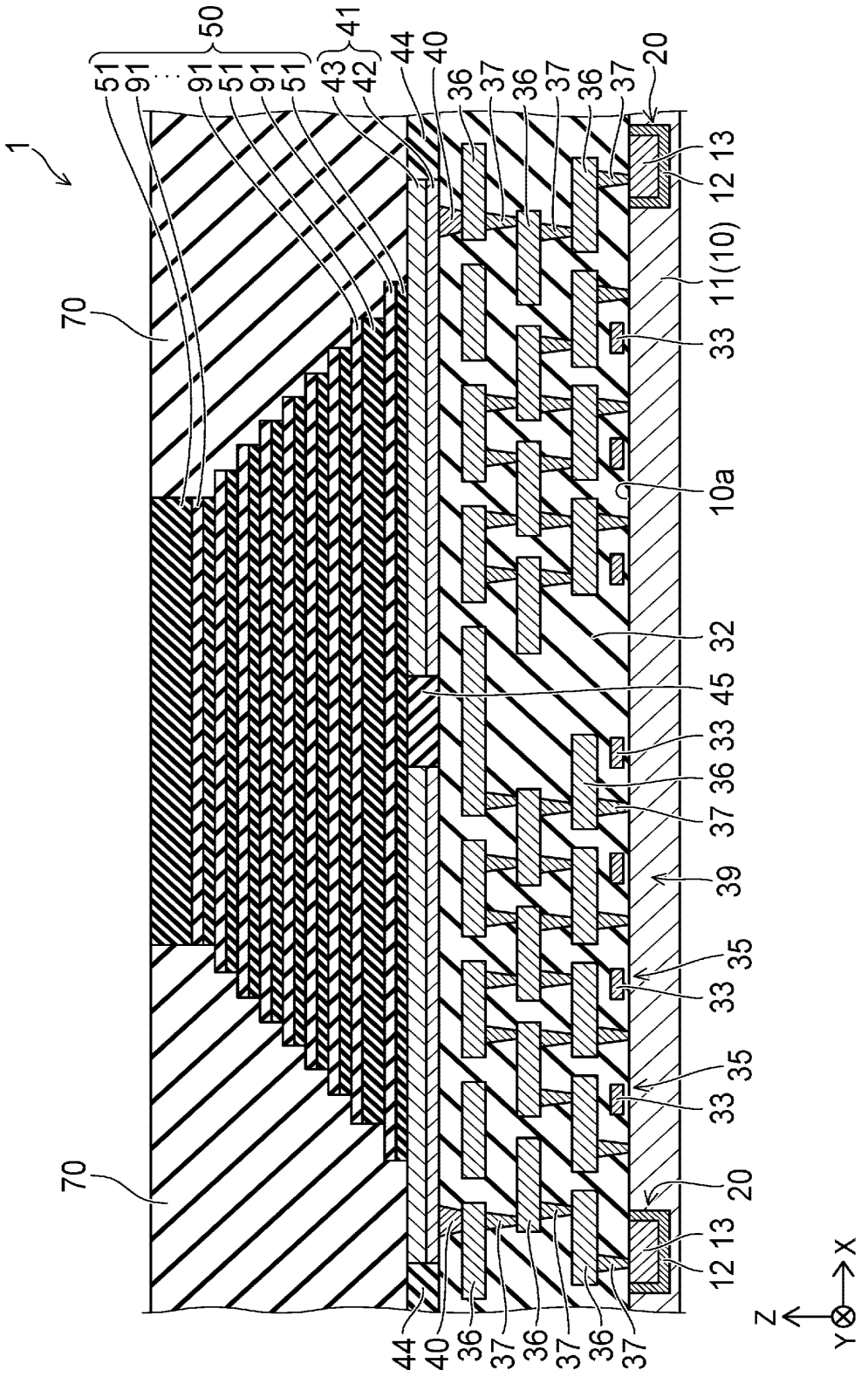

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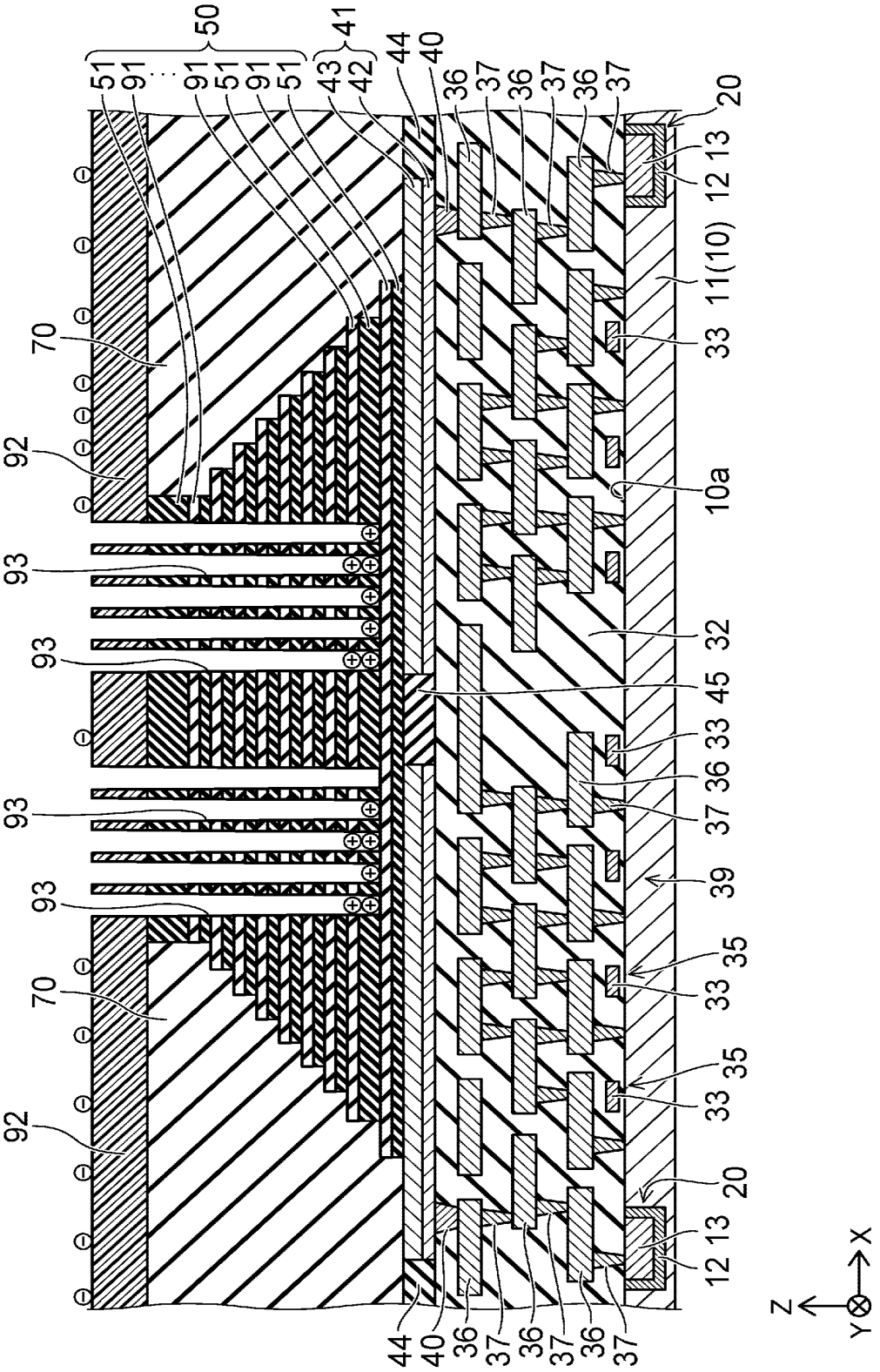

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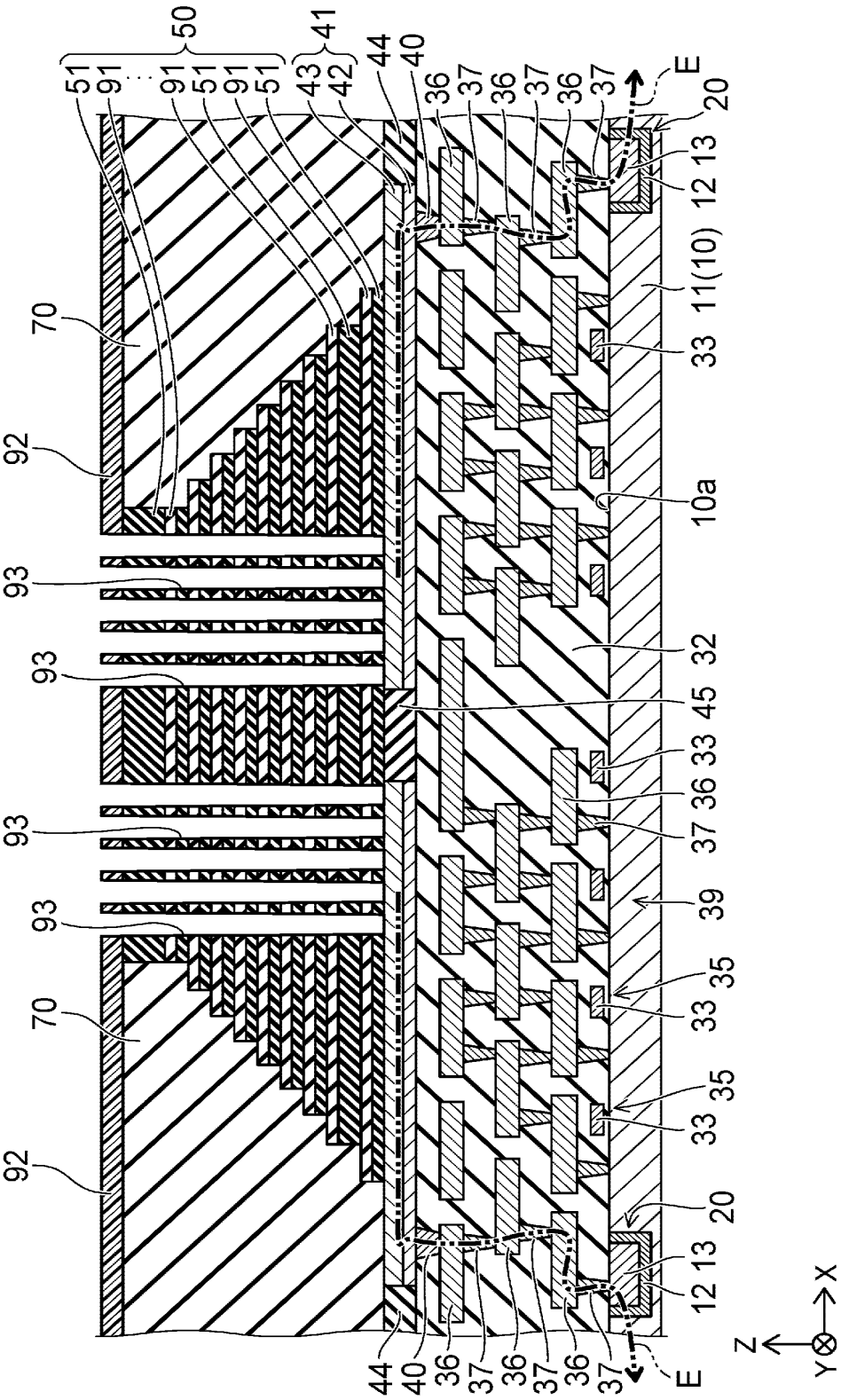

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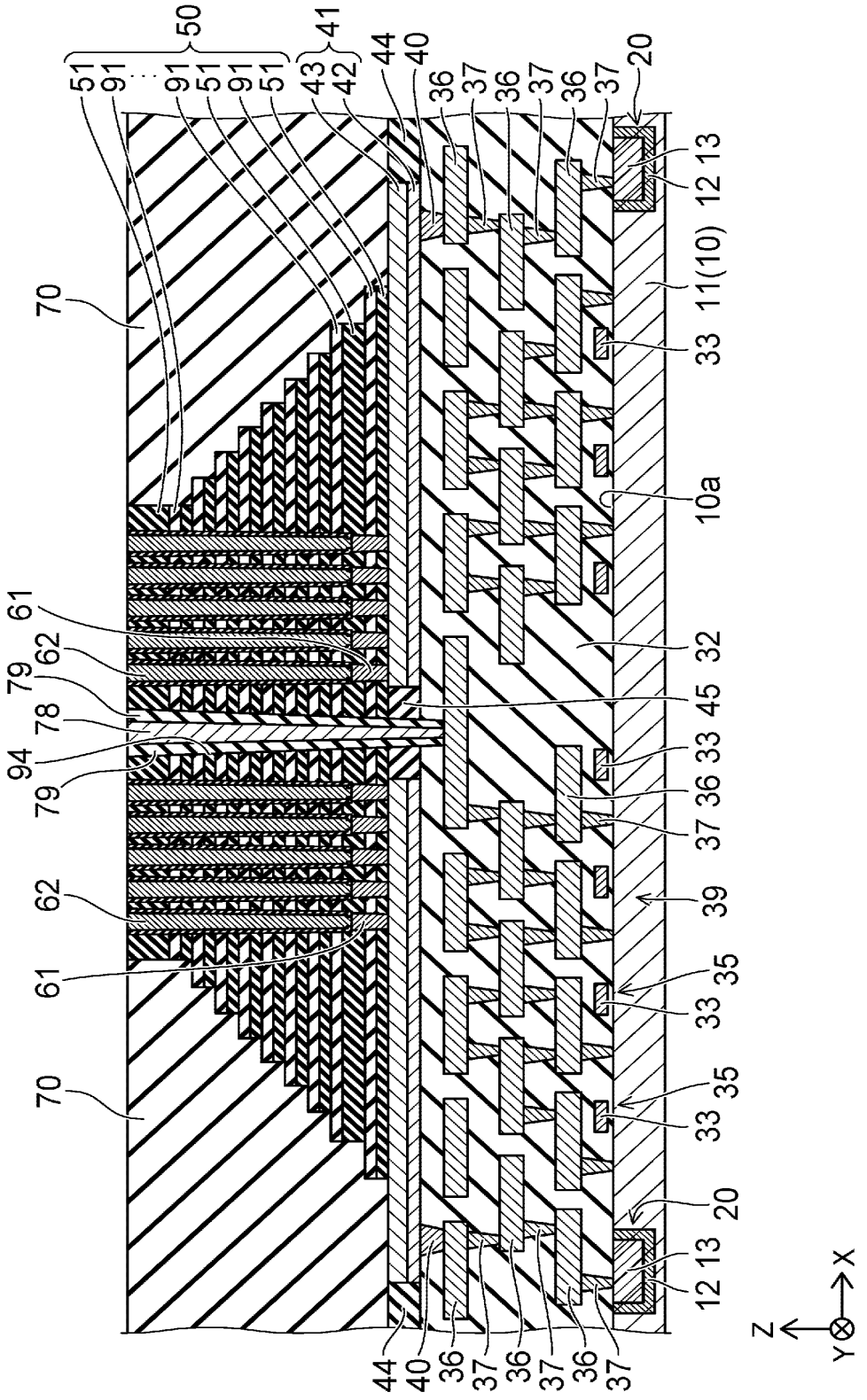

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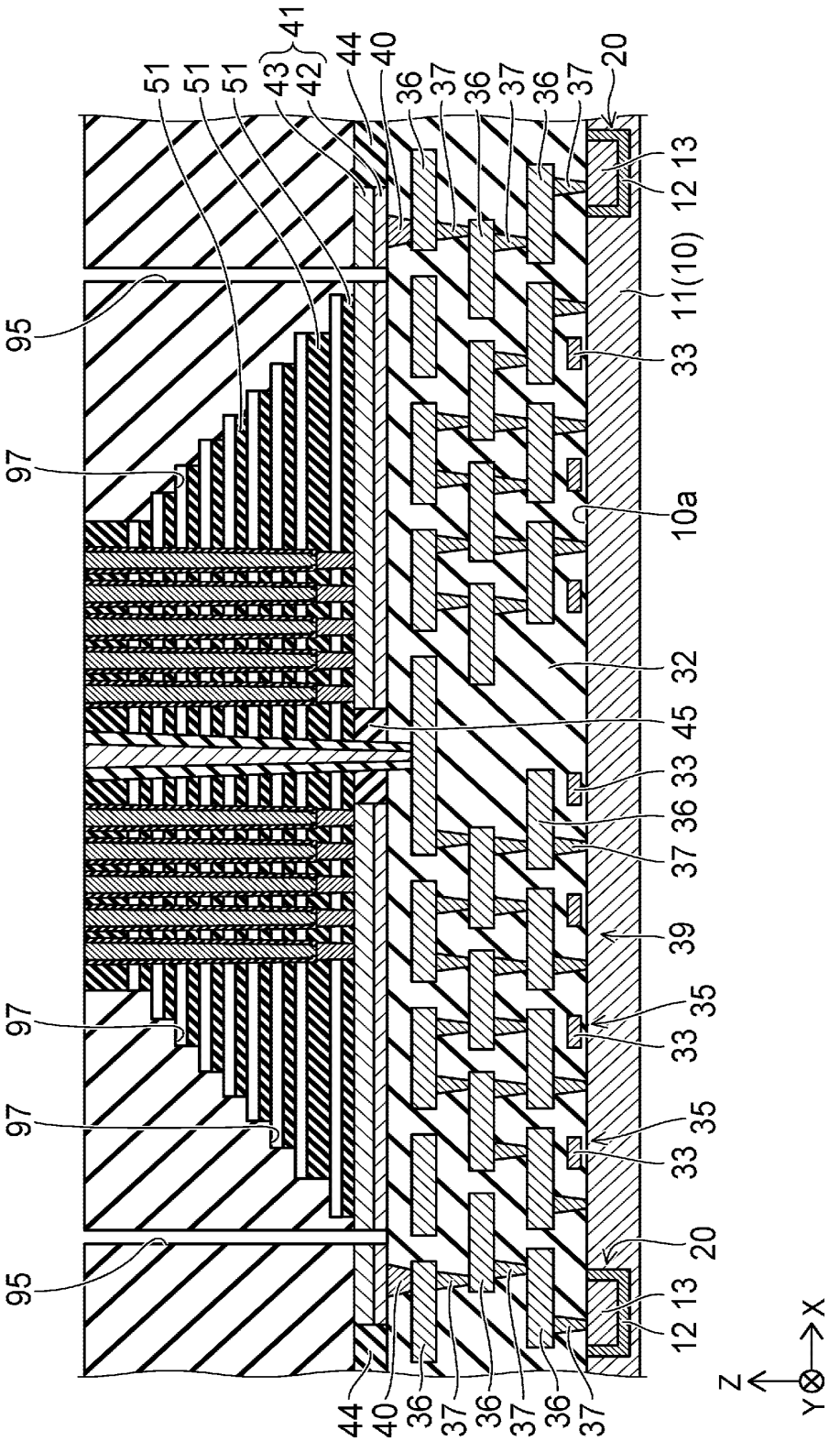

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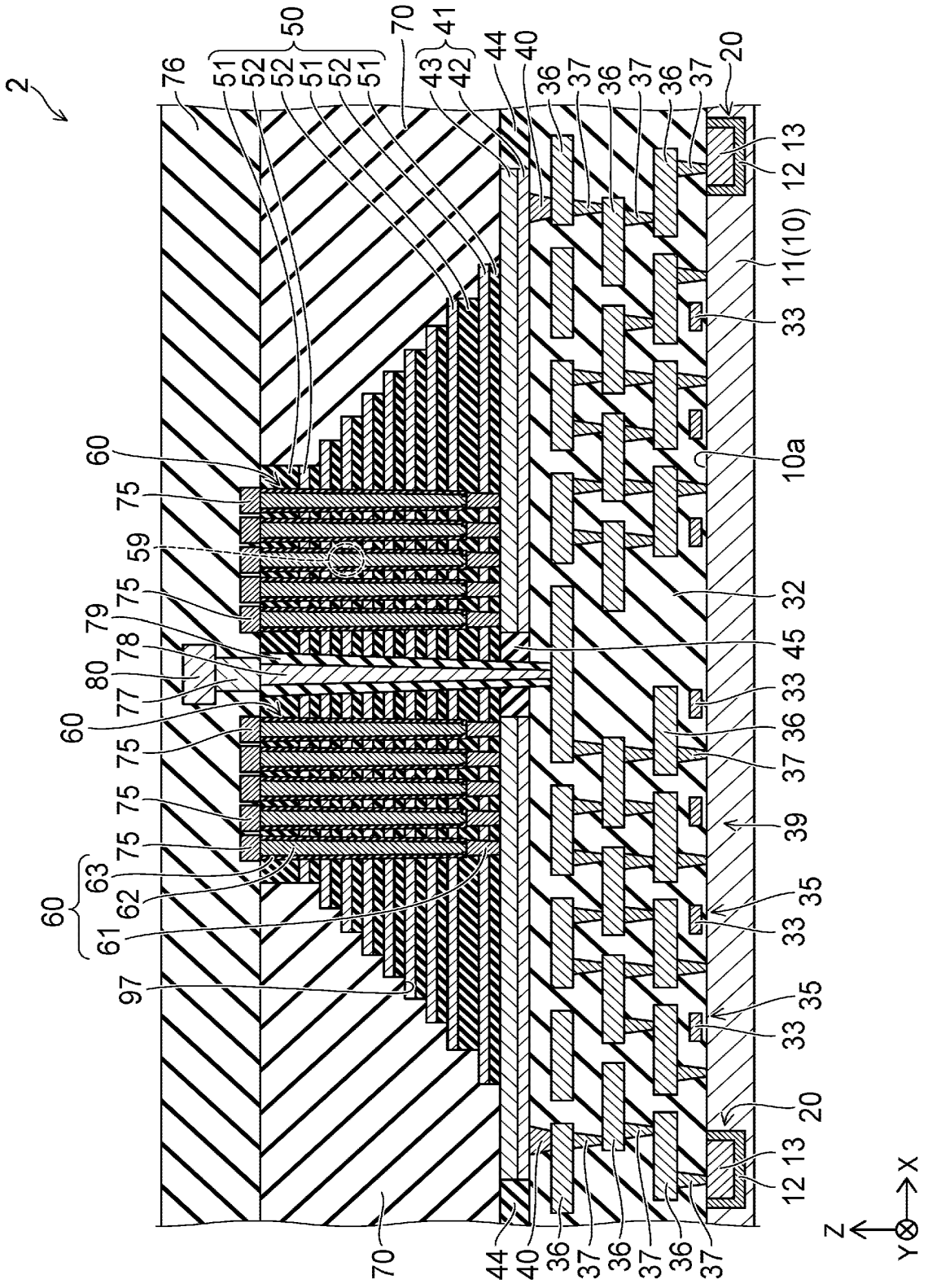

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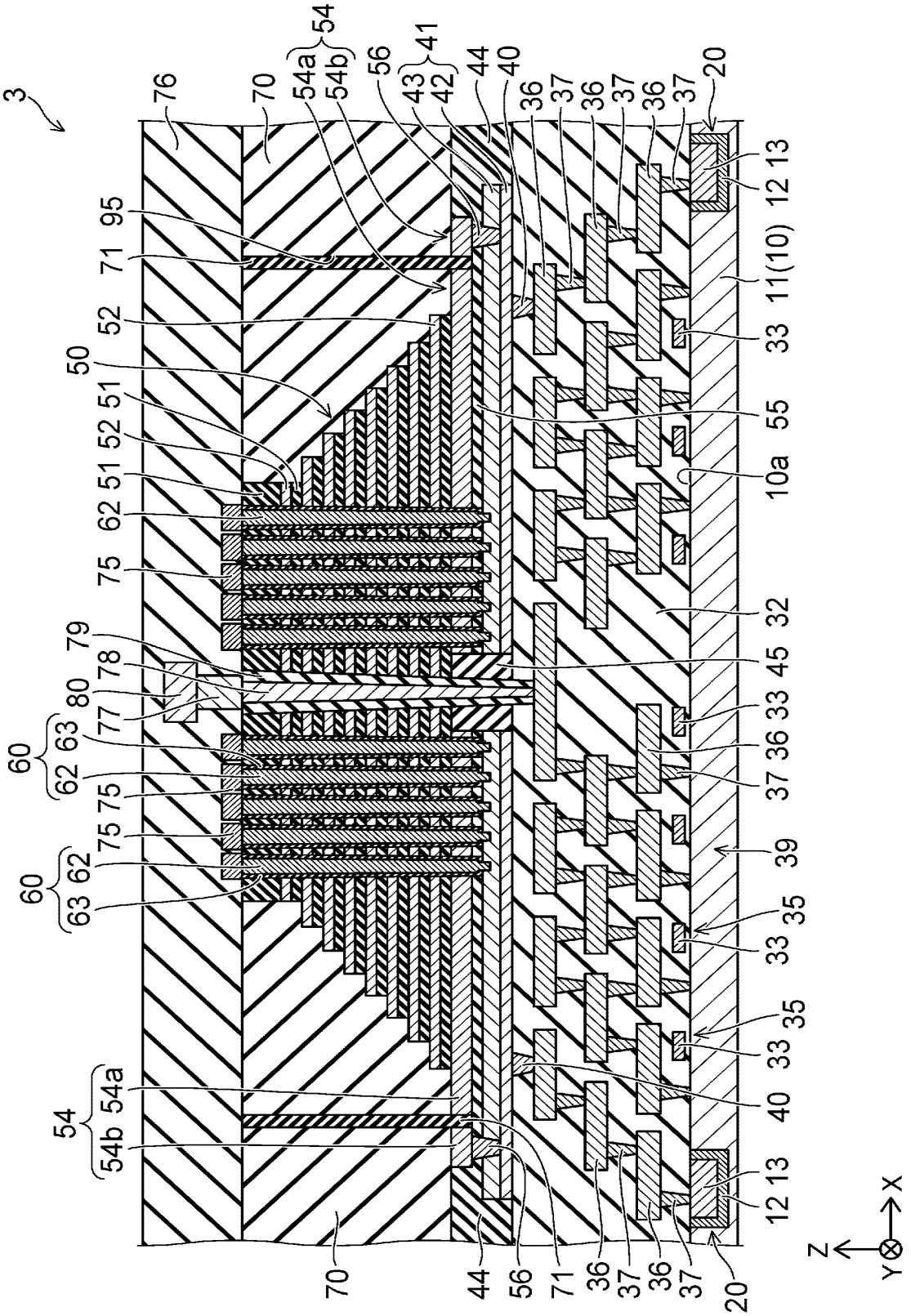

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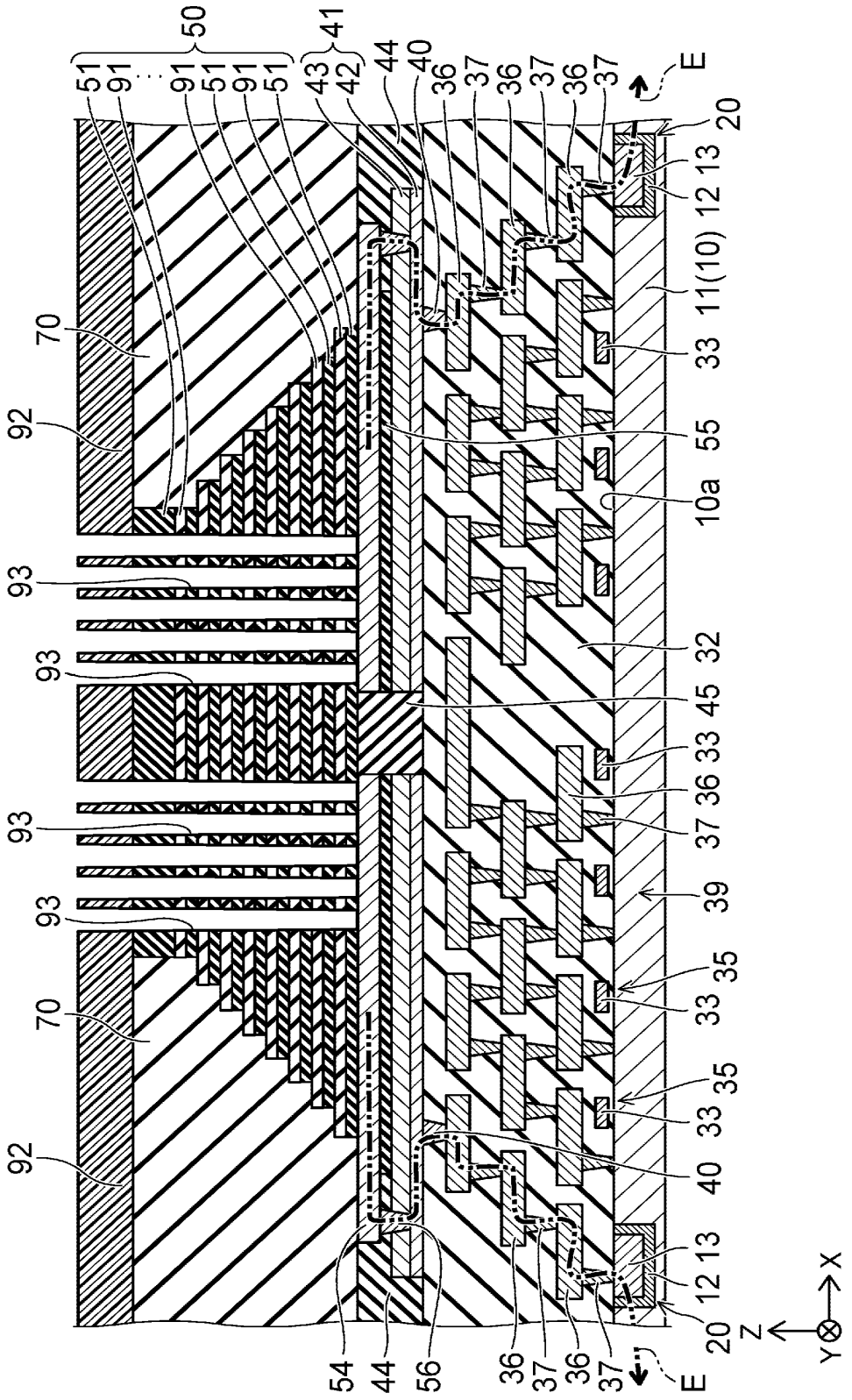

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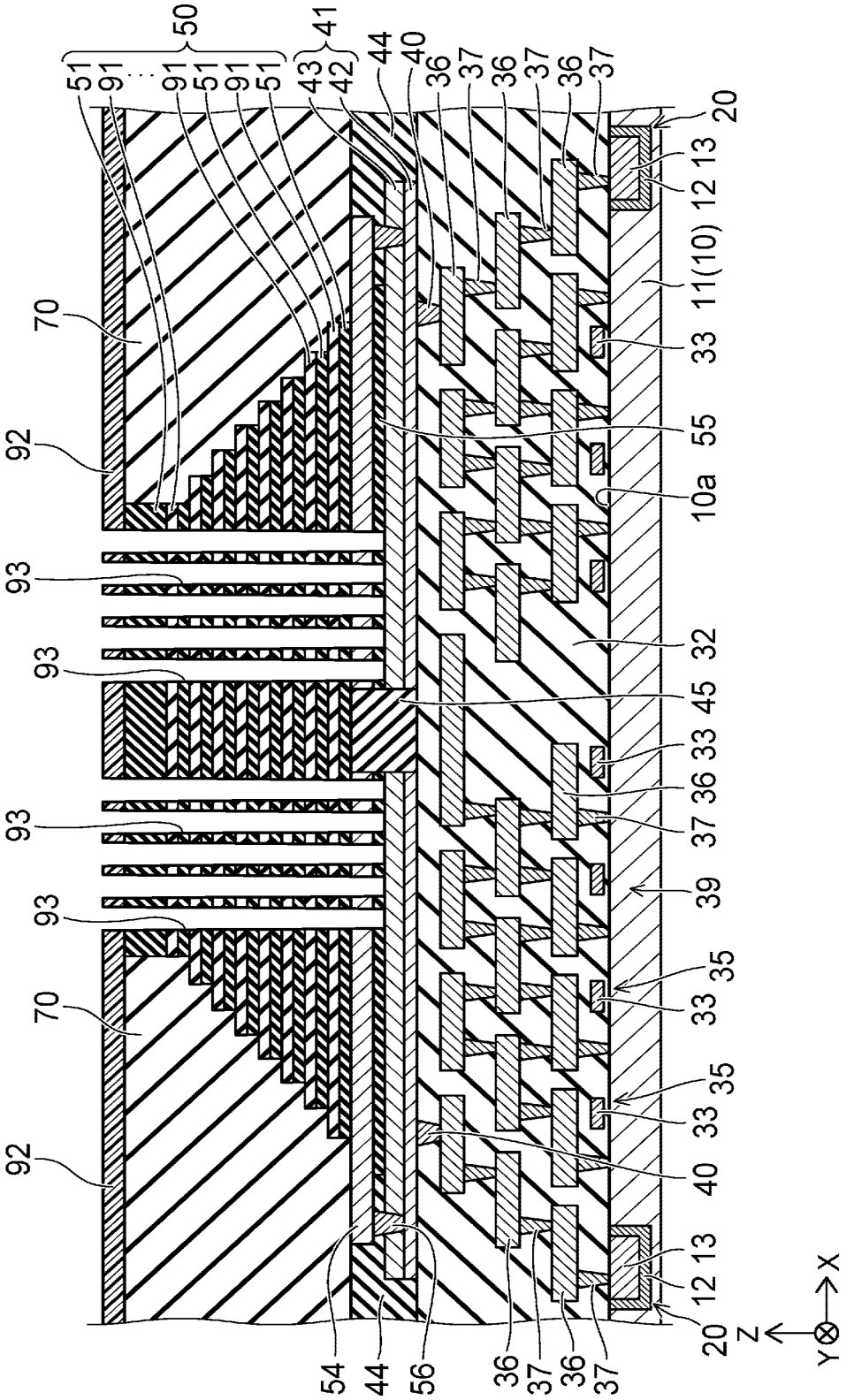

【書類名】　出願人名義変更届（一般承継）
【提出日】　平成30年 9月 5日
【あて先】　特許庁長官　　殿
【事件の表示】
　【出願番号】　特願2017-247987
【承継人】
　【識別番号】　318010018
　【氏名又は名称】　東芝メモリ株式会社
【承継人代理人】
　【識別番号】　100108062
　【弁理士】
　【氏名又は名称】　日向寺　雅彦
【提出物件の目録】
　【物件名】　閉鎖事項全部証明書　1
　　【援用の表示】　同日付で提出いたしました特願２０１４－２０１８０７号に関する出願人名義変更届（一般承継）に添付のものを援用し省略致します。
　【物件名】　委任状　1
　　【援用の表示】　同日付で提出いたしました特願２０１４－２０１８０７号に関する出願人名義変更届（一般承継）に添付のものを援用し省略致します。

出願人履歴

３１７００６０４１

20170411

新規登録

東京都港区芝浦一丁目１番１号

東芝メモリ株式会社

３１８０１００１８

20180705

新規登録

東京都千代田区丸の内一丁目１番１号　パレスビル５階

株式会社Ｐａｎｇｅａ

３１８０１００１８

20180801

名称変更　住所変更

東京都港区芝浦一丁目１番１号

東芝メモリ株式会社

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76) AND ASSIGNMENT FOR SINGLE ASSIGNEE

Title of Invention	SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR MANUFACTURING SAME

As the below named inventor, I hereby declare that:

This declaration ☐ **The attached application, or**

is directed to: ☒ **United States application or PCT international application number** 16/129,082 **filed on** September 12, 2018.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

WHEREAS, TOSHIBA MEMORY CORPORATION **(hereinafter referred to as "ASSIGNEE") having places of business at:** 1-1, Shibaura 1-chome, Minato-ku, Tokyo, Japan, **is desirous of acquiring the entire right, title and interest in and to said invention and in and to any Letters Patent that may be granted therefore in the United States and its territorial possessions and in any and all foreign countries;**

NOW, THEREFORE, in consideration of the sum of FIVE DOLLARS ($5.00), the receipt whereof is hereby acknowledged, and for other good and valuable consideration, I, by these presents do sell, assign and transfer unto said ASSIGNEE, the full and exclusive right to the said invention in the United States and its territorial possessions and in all foreign countries (including the right to claim priority under the terms of the International Convention and other relevant International Treaties and Arrangements from the aforesaid application) and the entire right, title and interest in and to any and all Letters Patent which may be granted therefor in the United States and its territorial possessions and in any and all foreign countries and in and to any and all divisions, reissues, continuations, substitutions and renewals thereof.

I hereby authorize and request the Patent Office Officials in the United States and its territorial possessions and any and all foreign countries to issue any and all of said Letters Patent, when granted, to said ASSIGNEE as the assignee of my entire right, title and interest in and to the same, for the sole use and behoof of said ASSIGNEE, its (his) successors and assigns, to the full end of the term for which said Letters Patent may be granted, as fully and entirely as the same would have been held by me had this Assignment and sale not been made.

Further, I agree that I will communicate to said ASSIGNEE or its (his) representatives any facts known to me respecting said invention, and testify in any legal proceeding, sign all lawful papers, execute all divisional, continuation, substitute, renewal and reissue applications, execute all necessary assignment papers to cause any and all of said Letters Patent to be issued to said ASSIGNEE, make all rightful oaths, and, generally do everything possible to aid said ASSIGNEE, its (his) successors and assigns, to obtain and enforce proper protection for said invention in the United States and its territorial possessions and in any and all foreign countries.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

LEGAL NAME OF INVENTOR

Inventor: Jun FUJIKI **Date:** Oct. 25, 2018

Signature: Jun Fujiki

OBLON, McCLELLAND, MAIER & NEUSTADT, L.L.P.
ATTORNEYS AT LAW
1940 DUKE STREET
ALEXANDRIA, VIRGINIA 22314

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LEGAL NAME OF INVENTOR

Inventor: Shinya ARAI Date: Oct. 4, 2018

Signature: Shinya Arai

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ATTORNEYS AT LAW
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ALEXANDRIA, VIRGINIA 22314

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76) AND ASSIGNMENT FOR SINGLE ASSIGNEE

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LEGAL NAME OF INVENTOR

Inventor: Kotaro FUJII **Date:** Oct. 4. 2018

Signature: Kotaro Fujii

OBLON, McCLELLAND, MAIER & NEUSTADT, L.L.P.
ATTORNEYS AT LAW
1940 DUKE STREET
ALEXANDRIA, VIRGINIA 22314

Electronic Acknowledgement Receipt

EFS ID:	34188286
Application Number:	16129082
International Application Number:	
Confirmation Number:	1059
Title of Invention:	SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR MANUFACTURING SAME
First Named Inventor/Applicant Name:	Jun FUJIKI
Customer Number:	22850
Filer:	Philippe Jean-Claude Signore/Connor Paul
Filer Authorized By:	Philippe Jean-Claude Signore
Attorney Docket Number:	516693US
Receipt Date:	01-NOV-2018
Filing Date:	12-SEP-2018
Time Stamp:	16:14:54
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Oath or Declaration filed	Dec-Assignment.pdf	218284 7ea46bc52be67300e7c83ac33424f7b2bff27444	no	3
Warnings:					

Information:	
Total Files Size (in bytes):	218284

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

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United States Patent and Trademark Office
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/129,082	09/12/2018	Jun FUJIKI	516693US

CONFIRMATION NO. 1059

22850
OBLON, MCCLELLAND, MAIER & NEUSTADT, L.L.P.
1940 DUKE STREET
ALEXANDRIA, VA 22314

PUBLICATION NOTICE

OC000000109233919

Title:SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR MANUFACTURING SAME

Publication No.US-2019-0198524-A1
Publication Date:06/27/2019

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Public Records Division. The Public Records Division can be reached by telephone at (571) 272-3150 or (800) 972-6382, by facsimile at (571) 273-3250, by mail addressed to the United States Patent and Trademark Office, Public Records Division, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently https://portal.uspto.gov/pair/PublicPair. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/129,082	09/12/2018	Jun FUJIKI	516693US	1059

22850 7590 07/22/2019

OBLON, MCCLELLAND, MAIER & NEUSTADT, L.L.P.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
REIDA, MOLLY KAY	

ART UNIT	PAPER NUMBER
2816	

NOTIFICATION DATE	DELIVERY MODE
07/22/2019	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

OBLONPAT@OBLON.COM
iahmadi@oblon.com
patentdocket@oblon.com

Office Action Summary	Application No. 16/129,082	Applicant(s) FUJIKI et al.	
	Examiner MOLLY K REIDA	Art Unit 2816	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 2 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 09/12/2018.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-20 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☐ Claim(s) _____ is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☑ Claim(s) 1-20 are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

Notice of Pre-AIA or AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Election/Restriction

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-15, drawn to a semiconductor device, classified in H01L27/11573 and/or H01L27/11582.

II. Claims 16-20, drawn to a method of manufacturing a semiconductor device, classified in H01L27/11573 and/or H01L27/11582.

The inventions are independent or distinct, each from the other because:

Inventions I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make another and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case the product as claimed can be made by another and materially different process; for example, replacing the second insulating material film with an electrode film before forming the semiconductor member; rather than after, as claimed.

Restriction for examination purposes as indicated is proper because all the inventions listed in this action are independent or distinct for the reasons given above and there would be a serious search and/or examination burden if restriction were not required because one or more of the following reasons apply: the inventions require a different field of search (e.g., searching different classes/subclasses or electronic resources, or employing different search strategies or search

queries); and/or the prior art applicable to one invention would not likely be applicable to another invention.

Applicant is advised that the reply to this requirement to be complete must include (i) an election of a invention to be examined even though the requirement may be traversed (37 CFR 1.143) **and (ii) identification of the claims encompassing the elected invention**.

The election of an invention may be made with or without traverse. To reserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the restriction requirement, the election shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement will result in the loss of right to petition under 37 CFR 1.144. If claims are added after the election, applicant must indicate which of these claims are readable upon the elected invention.

Should applicant traverse on the ground that the inventions are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the inventions to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103 or pre-AIA 35 U.S.C. 103(a) of the other invention.

Species Election

This application contains claims directed to the following patentably distinct species:

Should Applicant choose Group I:

Species A relating to Figs. 1-5

Species B relating to Fig. 11

Species C relating to Figs. 12-13

Species A is independent or distinct from Species B due at least to the presence or absence of insulating plate 71.

Species A is independent or distinct from Species C due to the differences described on pg. 14 line 31 to pg. 15 line 7

Species B is independent or distinct from Species C due at least to the presence or absence of insulating plate 71 and also due to the differences described on pg. 14 line 31 to pg. 15 line 7

In addition, these species are not obvious variants of each other based on the current record.

Should Applicant choose Group II:

Species D relating to Figs. 6-10

Species E relating to page 14 lines 2-23

Species F relating to Figs. 14-15

Species D is independent or distinct from Species E due at least to the presence or absence of forming insulating plate 71.

Species D is independent or distinct from Species F due to the differences described on pg. 14 line 31 to pg. 15 line 7 and the corresponding forming methods

Species E is independent or distinct from Species F due at least to the presence or absence of insulating plate 71 and also due to the differences described on pg. 14 line 31 to pg. 15 line 7 and the corresponding forming methods

In addition, these species are not obvious variants of each other based on the current record.

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species, or a single grouping of patentably indistinct species, for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, no claims are generic to all species.

There is a search and/or examination burden for the patentably distinct species as set forth above because at least the following reason(s) apply: the species require a different field of search (e.g., searching different classes/subclasses or electronic resources, or employing different search strategies or search queries); and/or the prior art applicable to one species would not likely be applicable to another species.

Applicant is advised that the reply to this requirement to be complete must include (i) an election of a species to be examined even though the requirement may be traversed (37 CFR 1.143) **and (ii) identification of the claims encompassing the elected species or grouping of patentably indistinct species**, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

The election may be made with or without traverse. To preserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the election of species requirement, the election shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement will result in the loss of right to petition under 37 CFR 1.144. If claims are added after the election, applicant must indicate which of these claims are readable on the elected species or grouping of patentably indistinct species.

Should applicant traverse on the ground that the species, or groupings of patentably indistinct species from which election is required, are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing them to be obvious variants or clearly admit on the

record that this is the case. In either instance, if the examiner finds one of the species unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103 or pre-AIA 35 U.S.C. 103(a) of the other species.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which depend from or otherwise require all the limitations of an allowable generic claim as provided by 37 CFR 1.141.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be corrected in compliance with 37 CFR 1.48(a) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. A request to correct inventorship under 37 CFR 1.48(a) must be accompanied by an application data sheet in accordance with 37 CFR 1.76 that identifies each inventor by his or her legal name and by the processing fee required under 37 CFR 1.17(i).

The examiner has required restriction between product or apparatus claims and process claims. Where applicant elects claims directed to the product/apparatus, and all product/apparatus claims are subsequently found allowable, withdrawn process claims that include all the limitations of the allowable product/apparatus claims should be considered for rejoinder. All claims directed to a nonelected process invention must include all the limitations of an allowable product/apparatus claim for that process invention to be rejoined.

In the event of rejoinder, the requirement for restriction between the product/apparatus claims and the rejoined process claims will be withdrawn, and the rejoined process claims will be fully examined for patentability in accordance with 37 CFR 1.104. Thus, to be allowable, the rejoined claims must meet all criteria for patentability including the requirements of 35 U.S.C. 101, 102, 103 and 112. Until all claims to the elected product/apparatus are found allowable, an otherwise proper restriction requirement between product/apparatus claims and process claims may be maintained. Withdrawn

process claims that are not commensurate in scope with an allowable product/apparatus claim will not be rejoined. See MPEP § 821.04. Additionally, in order for rejoinder to occur, applicant is advised that the process claims should be amended during prosecution to require the limitations of the product/apparatus claims. **Failure to do so may result in no rejoinder.** Further, note that the prohibition against double patenting rejections of 35 U.S.C. 121 does not apply where the restriction requirement is withdrawn by the examiner before the patent issues. See MPEP § 804.01.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MOLLY KAY REIDA whose telephone number is (571)272-4237. The examiner can normally be reached on M-F 8:30-5:00PM.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer

Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MOLLY K REIDA/
Examiner, Art Unit 2816

/ROBERT G BACHNER/
Primary Examiner, Art Unit 2898

DOCKET NO: 516693US

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF	:
JUN FUJIKI, ET AL.	: EXAMINER: REIDA, MOLLY K.
SERIAL NO: 16/129,082	:
FILED: SEPTEMBER 12, 2018	: GROUP ART UNIT: 2816
FOR: SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR MANUFACTURING SAME	:

ELECTION

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

Commissioner:

In response to the election requirement dated July 22, 2019, Applicant elects, without traverse, Group I, Claims 1-15, drawn to a semiconductor device, classified in H01L27/11573 and/or H01L27/11582. Further, Applicant elects Species C relating to Figs. 12-13 and identifies Claims 1-3 and 10-15 as corresponding to the elected species, for further examination on the merits. Applicant reserves the right to file one or more divisional applications directed to the non-elected species.

Accordingly, examination on the merits of Claims 1-3 and 10-15 is in order and is respectfully requested.

Respectfully Submitted,

OBLON, McCLELLAND,
MAIER & NEUSTADT, L.L.P.

Eckhard H. Kuesters
Attorney of Record
Registration No. 28,870

Customer Number
22850
Tel. (703) 413-3000
Fax. (703) 413-2220
(OMMN 07/09)

Electronic Acknowledgement Receipt

EFS ID:	37226635
Application Number:	16129082
International Application Number:	
Confirmation Number:	1059
Title of Invention:	SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR MANUFACTURING SAME
First Named Inventor/Applicant Name:	Jun FUJIKI
Customer Number:	22850
Filer:	Philippe Jean-Claude Signore/LaKisha Durham
Filer Authorized By:	Philippe Jean-Claude Signore
Attorney Docket Number:	516693US
Receipt Date:	20-SEP-2019
Filing Date:	12-SEP-2018
Time Stamp:	13:35:23
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		516693USElection.pdf	362066 f17f7f6848be4c2b8154da06e1fa1875003e1504	yes	3

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Miscellaneous Incoming Letter	1	1
	Response to Election / Restriction Filed	2	3
Warnings:			
Information:			
	Total Files Size (in bytes):	362066	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

OBLON

ATTORNEYS AT LAW

ECKHARD H. KUESTERS
(703) 413-3000
EKUESTERS@OBLON.COM

Docket No.: 516693US

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

RE: Application Serial No.: 16/129,082
Applicants: Jun FUJIKI, et al.
Filing Date: September 12, 2018
For: SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR MANUFACTURING SAME
Group Art Unit: 2816
Examiner: REIDA, MOLLY K.

Commissioner:

Attached hereto for filing are the following papers:

Election

Credit card payment is being made online (if electronically filed), or is attached hereto (if paper filed), in the amount of **$0.00** to cover any required fees. In the event any variance exists between the submitted amount and the U.S. Patent and Trademark Office fees for filing the above-noted documents, including any fees required under 37 C.F.R. 1.136 for any necessary Extension of Time to make the filing of the attached documents timely, please charge or credit the difference to our Deposit Account No. **15-0030**. Further, if these papers are not considered timely filed, then a petition is hereby made under 37 C.F.R. 1.136 for the necessary extension of time.

Respectfully submitted,

OBLON, McCLELLAND,
MAIER & NEUSTADT, L.L.P.

Eckhard H. Kuesters

Eckhard H. Kuesters
Registration No. 28,870

Customer Number
22850
(703) 413-3000 (phone)
(703) 413-2220 (fax)
(OMMN 02/12)

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

22850 7590 12/31/2019

OBLON, MCCLELLAND, MAIER & NEUSTADT, L.L.P.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER
REIDA, MOLLY KAY

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 12/31/2019

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/129,082	09/12/2018	Jun FUJIKI	516693US	1059

TITLE OF INVENTION: SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR MANUFACTURING SAME

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	03/31/2020

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PTOL-85 (Rev. 02/11)

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

22850 7590 12/31/2019

OBLON, MCCLELLAND, MAIER & NEUSTADT, L.L.P.
1940 DUKE STREET
ALEXANDRIA, VA 22314

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/129,082	09/12/2018	Jun FUJIKI	516693US	1059

TITLE OF INVENTION: SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR MANUFACTURING SAME

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	03/31/2020

EXAMINER	ART UNIT	CLASS-SUBCLASS
REIDA, MOLLY KAY	2816	257-324000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑ Issue Fee ❑ Publication Fee (if required) ❑ Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (08-18) Approved for use through 01/31/2020 OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/129,082	09/12/2018	Jun FUJIKI	516693US	1059

22850 7590 12/31/2019

OBLON, MCCLELLAND, MAIER & NEUSTADT, L.L.P.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
REIDA, MOLLY KAY	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 12/31/2019

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 02/11)

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 16/129,082	Applicant(s) FUJIKI et al.	
	Examiner MOLLY K REIDA	Art Unit 2816	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to communications filed 07/22/2019.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 1-20 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☑ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☑ All b) ☐ Some *c) ☐ None of the:

   1. ☑ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 09/12/2018.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☑ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/ROBERT G BACHNER/ Primary Examiner, Art Unit 2898	/MOLLY K REIDA/ Examiner, Art Unit 2816

Notice of Pre-AIA or AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Election/Restrictions

Claim 1 is are allowable. The restriction requirement between a semiconductor device and a method of manufacturing a semiconductor device, as set forth in the Office action mailed on 07/22/2019, has been reconsidered in view of the allowability of claims to the elected invention pursuant to MPEP § 821.04(a). **The restriction requirement is hereby withdrawn as to any claim that requires all the limitations of an allowable claim.** Specifically, the restriction requirement of 07/22/2019 is withdrawn. Claims 16-20, directed to a method of manufacturing a semiconductor device are no longer withdrawn from consideration because the claim(s) requires all the limitations of an allowable claim. Furthermore, claims 4-9 directed to a semiconductor device are no longer withdrawn from consideration because the claim(s) requires all the limitations of an allowable claim.

In view of the above noted withdrawal of the restriction requirement, applicant is advised that if any claim presented in a continuation or divisional application is anticipated by, or includes all the limitations of, a claim that is allowable in the present application, such claim may be subject to provisional statutory and/or nonstatutory double patenting rejections over the claims of the instant application.

Once a restriction requirement is withdrawn, the provisions of 35 U.S.C. 121 are no longer applicable. See In re Ziegler, 443 F.2d 1211, 1215, 170 USPQ 129, 131-32 (CCPA 1971). See also MPEP § 804.01.

Priority

Receipt is acknowledged of certified copies of papers required by 37 CFR 1.55.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 09/12/2018 has been considered by the examiner.

Allowable Subject Matter

Claims 1-20 are allowed.

The following is an examiner's statement of reasons for allowance:

Re independent claim 1, there is no teaching, suggestion, or motivation from the prior art of record, nor does the prior art of record otherwise make obvious the limitations of "…a semiconductor substrate including a formed in an upper layer portion of the semiconductor substrate; a first conductive film…coupled to the diode; a semiconductor member piercing the stacked body an being connected to first conductive film…", in combination with the other limitations.

Re independent claim 16, there is no teaching, suggestion, or motivation from the prior art of record, nor does the prior art of record otherwise make obvious the limitations of "…forming a diode in an upper layer portion of a semiconductor substrate…forming a conductive film…coupled to the diode…forming a semiconductor member…the semiconductor member being connected to the first conductive film…", in combination with the other limitations.

Re independent claim 19, there is no teaching, suggestion, or motivation from the prior art of record, nor does the prior art of record otherwise make obvious the limitations of "…forming a diode in an upper layer portion of a semiconductor substrate…forming a first conductive film…coupled to the

diode…forming a semiconductor member…the semiconductor member being connected to the first conductive film…", in combination with the other limitations.

Conclusion

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MOLLY KAY REIDA whose telephone number is (571)272-4237. The examiner can normally be reached on M-F 8:30-5:00PM.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see https://ppair-my.uspto.gov/pair/PrivatePair. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MOLLY K REIDA/
Examiner, Art Unit 2816

/ROBERT G BACHNER/
Primary Examiner, Art Unit 2898

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/129,082	FUJIKI et al.
	Examiner	**Art Unit**
	MOLLY K REIDA	2816

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☑ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	12/18/2019								
	1	=								
	2	=								
	3	=								
	4	=								
	5	=								
	6	=								
	7	=								
	8	=								
	9	=								
	10	=								
	11	=								
	12	=								
	13	=								
	14	=								
	15	=								
	16	=								
	17	=								
	18	=								
	19	=								
	20	=								

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/129,082	FUJIKI et al.
	Examiner	Art Unit
	MOLLY K REIDA	2816

CPC - Searched*		
Symbol	Date	Examiner
H01L27/0727,11563-11582	12/18/2019	mkr

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
Inventor(s)	12/18/2019	mkr
Applicant/Assignee	12/18/2019	mkr
EAST Text Search	12/18/2019	mkr

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
	US-PGPUB .clm. search	12/18/2019	mkr

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/129,082	FUJIKI et al.
	Examiner	**Art Unit**
	MOLLY K REIDA	2816

CPC						
Symbol					**Type**	**Version**
H01L	/	27	/	11582	F	2013-01-01
H01L	/	27	/	1157	I	2013-01-01
H01L	/	21	/	76897	I	2013-01-01
H01L	/	27	/	0727	I	2013-01-01
H01L	/	27	/	11573	I	2013-01-01

CPC Combination Sets								
Symbol					**Type**	**Set**	**Ranking**	**Version**
	/		/					

/MOLLY K REIDA/ Examiner, Art Unit 2816	18 December 2019	**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	20	
/ROBERT G BACHNER/ Primary Examiner, Art Unit 2898	19 December 2019	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2

U.S. Patent and Trademark Office — Part of Paper No.: 20191218

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/129,082	FUJIKI et al.
	Examiner	**Art Unit**
	MOLLY K REIDA	2816

INTERNATIONAL CLASSIFICATION					
CLAIMED					
H01L27/11582	/	27	/	11582	
H01L27/1157	/	27	/	1157	
H01L27/11573	/	27	/	11573	

NON-CLAIMED				
	/		/	

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**

CROSS REFERENCES(S)						
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**					

/MOLLY K REIDA/ Examiner, Art Unit 2816	18 December 2019	**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	20	
/ROBERT G BACHNER/ Primary Examiner, Art Unit 2898	19 December 2019	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2

U.S. Patent and Trademark Office — Part of Paper No.: 20191218

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/129,082	FUJIKI et al.
	Examiner	**Art Unit**
	MOLLY K REIDA	2816

☑ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original

/MOLLY K REIDA/ Examiner, Art Unit 2816	18 December 2019	**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	20	
/ROBERT G BACHNER/ Primary Examiner, Art Unit 2898	19 December 2019	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2

U.S. Patent and Trademark Office — Part of Paper No.: 20191218

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BIB DATA SHEET

CONFIRMATION NO. 1059

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
16/129,082	09/12/2018 RULE	257	2816	516693US

APPLICANTS
TOSHIBA MEMORY CORPORATION, Minato-ku, JAPAN;

INVENTORS
Jun FUJIKI, Mie, JAPAN;
Shinya ARAI, Yokkaichi, JAPAN;
Kotaro FUJII, Yokkaichi, JAPAN;

**** CONTINUING DATA ***************************

**** FOREIGN APPLICATIONS ***************************
JAPAN 2017-247987 12/25/2017

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****
10/01/2018

Foreign Priority claimed ☑ Yes ☐ No 35 USC 119(a-d) conditions met ☑ Yes ☐ No Verified and Acknowledged /MOLLY KAY REIDA/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		JAPAN	15	20	3

ADDRESS
OBLON, MCCLELLAND, MAIER & NEUSTADT, L.L.P.
1940 DUKE STREET
ALEXANDRIA, VA 22314
UNITED STATES

TITLE
SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR MANUFACTURING SAME

FILING FEE RECEIVED		
1880	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

Form PTO 1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY DOCKET NO. 516693US	SERIAL NO. New Application
LIST OF REFERENCES CITED BY APPLICANT	INVENTOR(S) Jun FUJIKI, et al.	
	FILING DATE Herewith	GROUP

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	AA	2011/0073866 A1	3/31/2011	KIM, Y. et al.			
	AB	2014/0085979 A1	3/27/2014	KONO, F.			
	AC	8,389,990 B2	3/5/2013	MIKAWA, T. et al.			
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						
	AM						
	AN						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION YES	TRANSLATION NO
	AO	2010-165794	7/29/2010	Japan (with English Abstract and Machine Generated English Translation)	X	
	AP					
	AQ					
	AR					
	AS					
	AT					
	AU					
	AV					

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)

	AW	
	AX	
	AY	
	AZ	☐ Additional References sheet(s) attached

Examiner	/MOLLY K REIDA/	Date considered	12/18/2019

*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.K.R/

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	3	("20110073866" | "20140085979" | "8389990").PN.	US-PGPUB; USPAT	OR	ON	2019/12/18 09:29
L2	267	((("FUJIKI") near3 ("Jun")) OR (("ARAI") near3 ("Shinya")) OR (("FUJII") near3 ("Kotaro"))).INV.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2019/12/18 09:31
L3	11	2 and diode	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2019/12/18 09:50
L5	1000175	((("TOSHIBA"))).AS,AANM,ASNM.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/12/18 10:05
L6	1982	H01L27/1157.cpc. and H01L27/11573.cpc. and H01L27/11582.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/12/18 10:15
L7	376	5 and 6	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/12/18 10:15
L8	2390977	H01L27/0727.cpc. diode	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/12/18 10:15
L9	21	7 and 8	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/12/18 10:15
L10	21290	H01L27/1157.cpc. H01L27/11573.cpc. H01L27/11582.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/12/18 10:26
L11	112	5 and 10 and 8	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2019/12/18 10:27

			DERWENT; IBM_TDB			
L12	101	(6 and 8) not 11	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/12/18 11:35
L13	904	(10 and 8) not (11 12)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/12/18 12:06
L14	16576	H01L27/11582.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/12/18 13:46
L15	185319	(diode with substrate)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/12/18 13:47
L16	0	(14 and 15) not (11 12 13)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/12/18 13:47
L18	30805	H01L27/11563-11582.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/12/18 13:48
L19	107	(18 and 15) not (11 12 13)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/12/18 13:49

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L20	753	(diode with substrate).clm. and (memory).clm.	US-PGPUB	OR	ON	2019/12/18 15:01

12/ 18/ 2019 3:18:23 PM
C:\ Users\ mreida\ Documents\ EAST\ Workspaces\ 16129082.wsp

Docket No.: 516693US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Jun FUJIKI, et al.

SERIAL NO:	16/129,082	GAU:	2816
FILED:	September 12, 2018	EXAMINER:	REIDA, MOLLY KAY

FOR: SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR MANUFACTURING SAME

REQUEST FOR CONTINUED EXAMINATION (RCE) TRANSMITTAL

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

Commissioner:

This is a Request for Continued Examination (RCE) under 37 C.F.R. §1.114 of the above-identified application.

Submission required under 37 C.F.R. §1.114

Previously Submitted:

☐ Consider the amendment(s)/reply under 37 C.F.R. §1.116 previously filed on

☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on

Enclosed:

☐ Amendment/Reply

■ Information Disclosure Statement (IDS)

☐ Track 1 Prioritized Examination

☐ Other:

FEES	RATE	CALCULATIONS
☐ Suspension of action on the above-identified application is requested under 37 C.F.R. §1.103(c) for a period of months.	$140.00	$0.00
■ RCE Fee required under 37 C.F.R. §1.17(e) - **1st request**	$1,300.00	$1,300.00
☐		$0.00
☐		$0.00
TOTAL OF ABOVE CALCULATIONS:		$1,300.00
☐ REDUCTION BY 50% FOR FILING AS SMALL ENTITY		$0.00
TOTAL:		$1,300.00

■ Credit card payment is being made online (if electronically filed), or is attached hereto (if paper filed), in the amount of **$1,300.00.**

■ Please charge any additional Fees for the papers being filed herewith and for which no payment is enclosed herewith, or credit any overpayment to Deposit Account No. **15-0030**.

■ If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 CFR 1.136, and any additional fees required under 37 CFR 1.136 for any necessary extension of time may be charged to Deposit Account No. **15-0030**.

Respectfully Submitted,

OBLON, McCLELLAND,
MAIER & NEUSTADT, L.L.P.

Eckhard H. Kuesters
Registration No. 28,870

Customer Number
22850
Tel. (703) 413-3000
Fax. (703) 413-2220
(OMMN 12/11)

Docket No. 516693US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF:	Jun FUJIKI, et al.		
SERIAL NO:	16/129,082	GAU:	2816
FILED:	September 12, 2018	EXAMINER:	REIDA, MOLLY KAY
FOR:	SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR MANUFACTURING SAME		

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

Commissioner:
Applicant(s) wish to disclose the following information.

REFERENCES

■ The applicant(s) wish to make of record the reference(s) listed on the attached form PTO-1449 and/or accompanying documents from a corresponding foreign application. Copies of the listed reference(s) are attached, where required, as are either statements of relevancy, English translations of the categories of cited documents for foreign search reports or English translations of foreign Office Actions which provide the statement of relevancy for the foreign language references cited therein, or any readily available partial or full English translations of pertinent portions of any non-English language reference(s).

☐ Credit card payment is being made online (if electronically filed), or is attached hereto (if paper filed), in the amount required under 37 CFR §1.17(p).

CERTIFICATION

☐ Each item of information contained in this information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement.

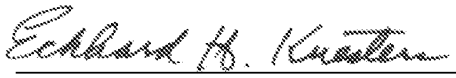
☐ No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to the knowledge of the undersigned, having made reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this statement.

DEPOSIT ACCOUNT

■ Please charge any additional fees for the papers being filed herewith and for which no payment is enclosed herewith, or credit any overpayment to deposit account number **15-0030**.

Respectfully submitted,

OBLON, McCLELLAND,
MAIER & NEUSTADT, L.L.P.



Eckhard H. Kuesters
Registration No. 28,870

Customer Number
22850

Tel. (703) 413-3000
Fax. (703) 413-2220
(OMMN 02/12)

Form PTO 1449 (Modified)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY DOCKET NO. 516693US	SERIAL NO. 16/129,082
LIST OF REFERENCES CITED BY APPLICANT		INVENTOR(S) Jun FUJIKI, et al.	
		FILING DATE September 12, 2018	GROUP 2816

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	AA	2018/0090509	03/29/2018	Zhang et al.			
	AB	2018/0323207	11/08/2018	Shim et al.			
	AC	2019/0081065	03/14/2019	Lee			
	AD	2019/0288003	09/19/2019	Shim et al.			
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						
	AM						
	AN						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION YES	TRANSLATION NO
	AO					
	AP					
	AQ					
	AR					
	AS					
	AT					
	AU					
	AV					

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)

	AW	
	AX	
	AY	
	AZ	☐ Additional References sheet(s) attached

Examiner		Date considered	

*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Electronic Patent Application Fee Transmittal

Application Number:	16129082
Filing Date:	12-Sep-2018
Title of Invention:	SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR MANUFACTURING SAME
First Named Inventor/Applicant Name:	Jun FUJIKI
Filer:	Philippe Jean-Claude Signore/LaKisha Durham
Attorney Docket Number:	516693US

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
RCE- 1ST REQUEST	1801	1	1300	1300
		Total in USD ($)		**1300**

Electronic Acknowledgement Receipt	
EFS ID:	39016543
Application Number:	16129082
International Application Number:	
Confirmation Number:	1059
Title of Invention:	SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR MANUFACTURING SAME
First Named Inventor/Applicant Name:	Jun FUJIKI
Customer Number:	22850
Filer:	Philippe Jean-Claude Signore/LaKisha Durham
Filer Authorized By:	Philippe Jean-Claude Signore
Attorney Docket Number:	516693US
Receipt Date:	31-MAR-2020
Filing Date:	12-SEP-2018
Time Stamp:	10:27:45
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$1300
RAM confirmation Number	E20203UA28023733
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		516693USRCEIDS.pdf	457906 4fe7a39751073ade6d35f8a807a17145633b3a58	yes	3

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Request for Continued Examination (RCE)	1	1
	Transmittal Letter	2	2
	Information Disclosure Statement (IDS) Form (SB08)	3	3

Warnings:

Information:

2	Fee Worksheet (SB06)	fee-info.pdf	30423 690e3f8a79f7377f9eb31f5553047f944da3c6cd	no	2

Warnings:

Information:

Total Files Size (in bytes):	488329

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

22850 7590 04/15/2020

OBLON, MCCLELLAND, MAIER & NEUSTADT, L.L.P.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER
REIDA, MOLLY KAY

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 04/15/2020

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/129,082	09/12/2018	Jun FUJIKI	516693US	1059

TITLE OF INVENTION: SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR MANUFACTURING SAME

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	07/15/2020

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PTOL-85 (Rev. 02/11)

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

22850 7590 04/15/2020

OBLON, MCCLELLAND, MAIER & NEUSTADT, L.L.P.
1940 DUKE STREET
ALEXANDRIA, VA 22314

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/129,082	09/12/2018	Jun FUJIKI	516693US	1059

TITLE OF INVENTION: SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR MANUFACTURING SAME

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	07/15/2020

EXAMINER	ART UNIT	CLASS-SUBCLASS
REIDA, MOLLY KAY	2816	257-324000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑ Issue Fee ❑ Publication Fee (if required) ❑ Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (08-18) Approved for use through 01/31/2020 OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/129,082	09/12/2018	Jun FUJIKI	516693US	1059

22850 7590 04/15/2020

OBLON, MCCLELLAND, MAIER & NEUSTADT, L.L.P.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
REIDA, MOLLY KAY	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 04/15/2020

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 02/11)

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 16/129,082	Applicant(s) FUJIKI et al.	
	Examiner MOLLY K REIDA	Art Unit 2816	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to RCE filed 03/31/2020.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 1-20 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☑ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☑ All b) ☐ Some *c) ☐ None of the:

   1. ☑ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 03/31/2020.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☑ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/MOLLY K REIDA/ Examiner, Art Unit 2816	/ROBERT G BACHNER/ Primary Examiner, Art Unit 2898

Notice of Pre-AIA or AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Request for Continued Examination Under 37 CFR 1.114

A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 03/31/2020 has been entered.

Election/Restrictions

Claim 1 is are allowable. The restriction requirement between a semiconductor device and a method of manufacturing a semiconductor device, as set forth in the Office action mailed on 07/22/2019, has been reconsidered in view of the allowability of claims to the elected invention pursuant to MPEP § 821.04(a). **The restriction requirement is hereby withdrawn as to any claim that requires all the limitations of an allowable claim.** Specifically, the restriction requirement of 07/22/2019 is withdrawn. Claims 16-20, directed to a method of manufacturing a semiconductor device are no longer withdrawn from consideration because the claim(s) requires all the limitations of an allowable claim. Furthermore, claims 4-9 directed to a semiconductor device are no longer withdrawn from consideration because the claim(s) requires all the limitations of an allowable claim.

In view of the above noted withdrawal of the restriction requirement, applicant is advised that if any claim presented in a continuation or divisional application is anticipated by, or includes all the

limitations of, a claim that is allowable in the present application, such claim may be subject to provisional statutory and/or nonstatutory double patenting rejections over the claims of the instant application.

Once a restriction requirement is withdrawn, the provisions of 35 U.S.C. 121 are no longer applicable. See In re Ziegler, 443 F.2d 1211, 1215, 170 USPQ 129, 131-32 (CCPA 1971). See also MPEP § 804.01.

Priority

Receipt is acknowledged of certified copies of papers required by 37 CFR 1.55.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 09/12/2018 and 03/31/2020 have been considered by the examiner.

Allowable Subject Matter

Claims 1-20 are allowed.

The following is an examiner's statement of reasons for allowance:

Re independent claim 1, there is no teaching, suggestion, or motivation from the prior art of record, nor does the prior art of record otherwise make obvious the limitations of "…a semiconductor substrate including a formed in an upper layer portion of the semiconductor substrate; a first conductive film…coupled to the diode; a semiconductor member piercing the stacked body an being connected to first conductive film…", in combination with the other limitations.

Re independent claim 16, there is no teaching, suggestion, or motivation from the prior art of record, nor does the prior art of record otherwise make obvious the limitations of "…forming a diode in

an upper layer portion of a semiconductor substrate…forming a conductive film…coupled to the diode…forming a semiconductor member…the semiconductor member being connected to the first conductive film…", in combination with the other limitations.

Re independent claim 19, there is no teaching, suggestion, or motivation from the prior art of record, nor does the prior art of record otherwise make obvious the limitations of "…forming a diode in an upper layer portion of a semiconductor substrate…forming a first conductive film…coupled to the diode…forming a semiconductor member…the semiconductor member being connected to the first conductive film…", in combination with the other limitations.

Conclusion

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MOLLY KAY REIDA whose telephone number is (571)272-4237. The examiner can normally be reached on M-F 8:30-5:00PM.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-1864. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see https://ppair-my.uspto.gov/pair/PrivatePair. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MOLLY K REIDA/
Examiner, Art Unit 2816

/ROBERT G BACHNER/
Primary Examiner, Art Unit 2898

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/129,082	FUJIKI et al.
	Examiner	Art Unit
	MOLLY K REIDA	2816

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☑ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	12/18/2019	04/07/2020							
	1	=	=							
	2	=	=							
	3	=	=							
	4	=	=							
	5	=	=							
	6	=	=							
	7	=	=							
	8	=	=							
	9	=	=							
	10	=	=							
	11	=	=							
	12	=	=							
	13	=	=							
	14	=	=							
	15	=	=							
	16	=	=							
	17	=	=							
	18	=	=							
	19	=	=							
	20	=	=							

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/129,082	FUJIKI et al.
	Examiner	**Art Unit**
	MOLLY K REIDA	2816

CPC						
Symbol					**Type**	**Version**
H01L	/	27	/	11582	F	2013-01-01
H01L	/	27	/	1157	I	2013-01-01
H01L	/	21	/	76897	I	2013-01-01
H01L	/	27	/	0727	I	2013-01-01
H01L	/	27	/	11573	I	2013-01-01

CPC Combination Sets								
Symbol					**Type**	**Set**	**Ranking**	**Version**
	/		/					

/MOLLY K REIDA/ Examiner, Art Unit 2816	07 April 2020	**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	20	
/ROBERT G BACHNER/ Primary Examiner, Art Unit 2898	10 April 2020	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2

U.S. Patent and Trademark Office — Part of Paper No.: 20200407

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/129,082	FUJIKI et al.
	Examiner	**Art Unit**
	MOLLY K REIDA	2816

INTERNATIONAL CLASSIFICATION					
CLAIMED					
H01L27/11582	/	27	/	11582	
H01L27/1157	/	27	/	1157	
H01L27/11573	/	27	/	11573	

NON-CLAIMED				
	/		/	

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**

CROSS REFERENCES(S)						
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**					

/MOLLY K REIDA/ Examiner, Art Unit 2816	07 April 2020	**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	20	
/ROBERT G BACHNER/ Primary Examiner, Art Unit 2898	10 April 2020	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2

U.S. Patent and Trademark Office — Part of Paper No.: 20200407

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/129,082	FUJIKI et al.
	Examiner	**Art Unit**
	MOLLY K REIDA	2816

☑ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original

/MOLLY K REIDA/ Examiner, Art Unit 2816	07 April 2020	**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	20	
/ROBERT G BACHNER/ Primary Examiner, Art Unit 2898	10 April 2020	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/129,082	FUJIKI et al.
	Examiner	Art Unit
	MOLLY K REIDA	2816

CPC - Searched*		
Symbol	Date	Examiner
H01L27/0727,11563-11582	12/18/2019	mkr

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
Inventor(s)	12/18/2019	mkr
Applicant/Assignee	12/18/2019	mkr
EAST Text Search	12/18/2019	mkr
Updated EAST Search	04/07/2020	mkr

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
	US-PGPUB .clm. search	12/18/2019	mkr
	US-PGPUB .clm. search	04/07/2020	mkr

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www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 1059

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
16/129,082	09/12/2018 RULE	257	2816	516693US

APPLICANTS
TOSHIBA MEMORY CORPORATION, Minato-ku, JAPAN;

INVENTORS
Jun FUJIKI, Mie, JAPAN;
Shinya ARAI, Yokkaichi, JAPAN;
Kotaro FUJII, Yokkaichi, JAPAN;

** **CONTINUING DATA** **********

** **FOREIGN APPLICATIONS** **********
JAPAN 2017-247987 12/25/2017

** **IF REQUIRED, FOREIGN FILING LICENSE GRANTED** **
10/01/2018

Foreign Priority claimed ☑ Yes ☐ No 35 USC 119(a-d) conditions met ☑ Yes ☐ No Verified and Acknowledged /MOLLY KAY REIDA/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		JAPAN	15	20	3

ADDRESS
OBLON, MCCLELLAND, MAIER & NEUSTADT, L.L.P.
1940 DUKE STREET
ALEXANDRIA, VA 22314
UNITED STATES

TITLE
SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR MANUFACTURING SAME

FILING FEE RECEIVED		
1880	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	4	("20180090509" | "20180323207" | "20190081065" | "20190288003").PN.	US-PGPUB; USPAT	OR	ON	2020/04/07 08:32
L2	279	((("FUJIKI") near3 ("Jun")) OR (("ARAI") near3 ("Shinya")) OR (("FUJII") near3 ("Kotaro"))).INV.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2020/04/07 09:37
L3	11	L2 and diode	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2020/04/07 09:37
L4	16	L2 and junction	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2020/04/07 09:37
L5	16	4 not 3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2020/04/07 09:37
L6	1005197	((("TOSHIBA"))).AS,AANM,ASNM.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/04/07 09:41
L7	2240	H01L27/1157.cpc. and H01L27/11573.cpc. and H01L27/11582.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/04/07 09:41
L8	423	L6 and L7	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2020/04/07 09:41

			DERWENT; IBM_TDB			
L9	2441379	H01L27/0727.cpc. diode	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/04/07 09:41
L10	21	L8 and L9	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/04/07 09:41
L11	22798	H01L27/1157.cpc. H01L27/11573.cpc. H01L27/11582.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/04/07 09:42
L12	116	L6 and L11 and L9	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/04/07 09:42
L13	119	(L7 and L9) not L12	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/04/07 09:42
L14	953	(L11 and L9) not (L12 L13)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/04/07 09:45
L15	189293	(diode with substrate)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2020/04/07 09:57

			DERWENT; IBM_TDB			
L16	32456	H01L27/11563-11582.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/04/07 09:57
L17	108	(L16 and L15) not (L12 L13 L14)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/04/07 09:57
L18	5	L8 and (junction with substrate)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/04/07 09:59
L19	23	L6 and L11 and (junction with substrate)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/04/07 10:01
L20	79	(L7 and (junction with substrate)) not L12	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/04/07 10:10
L22	74	(L7 and (junction with substrate)) not (12 19)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/04/07 10:11
L25	542	(L11 and (junction with substrate)) not (12 13 14 19 22)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2020/04/07 10:20

			DERWENT; IBM_TDB			
L26	139514	(junction with substrate)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/04/07 11:43
L27	32456	H01L27/11563-11582.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/04/07 11:43
L28	639	(26 and 27) not (12 13 14 19 22 25)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/04/07 11:44
S1	3	("20110073866" | "20140085979" | "8389990").PN.	US-PGPUB; USPAT	OR	ON	2019/12/18 09:29
S2	267	((("FUJIKI") near3 ("Jun")) OR (("ARAI") near3 ("Shinya")) OR (("FUJII") near3 ("Kotaro"))).INV.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2019/12/18 09:31
S3	11	S2 and diode	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2019/12/18 09:50
S4	1000175	((("TOSHIBA"))).AS,AANM,ASNM.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/12/18 10:05
S5	1982	H01L27/1157.cpc. and H01L27/11573.cpc. and H01L27/11582.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2019/12/18 10:15

			DERWENT; IBM_TDB			
S6	376	S4 and S5	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/12/18 10:15
S7	2390977	H01L27/0727.cpc. diode	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/12/18 10:15
S8	21	S6 and S7	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/12/18 10:15
S9	21290	H01L27/1157.cpc. H01L27/11573.cpc. H01L27/11582.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/12/18 10:26
S10	112	S4 and S9 and S7	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/12/18 10:27
S11	101	(S5 and S7) not S10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/12/18 11:35
S12	904	(S9 and S7) not (S10 S11)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2019/12/18 12:06

			DERWENT; IBM_TDB			
S13	16576	H01L27/11582.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/12/18 13:46
S14	185319	(diode with substrate)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/12/18 13:47
S15	0	(S13 and S14) not (S10 S11 S12)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/12/18 13:47
S16	30805	H01L27/11563-11582.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/12/18 13:48
S17	107	(S16 and S14) not (S10 S11 S12)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/12/18 13:49

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L29	762	(diode with substrate).clm. and (memory).clm.	US-PGPUB	OR	ON	2020/04/07 11:54

L30	998	(junction with substrate).clm. and (memory).clm.	US-PGPUB	OR	ON	2020/04/07 11:55
L31	947	30 not 29	US-PGPUB	OR	ON	2020/04/07 11:56
L32	122252	(vertical three 3D) with memory	US-PGPUB	OR	ON	2020/04/07 11:57
L33	268	31 and 32	US-PGPUB	OR	ON	2020/04/07 11:57
S18	753	(diode with substrate).clm. and (memory).clm.	US-PGPUB	OR	ON	2019/12/18 15:01

4/7/2020 12:07:27 PM
C:\Users\mreida\Documents\EAST\Workspaces\16129082.wsp

SHEET 1 OF 1

Form PTO 1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY DOCKET NO. 516693US	SERIAL NO. 16/129,082
LIST OF REFERENCES CITED BY APPLICANT	INVENTOR(S) Jun FUJIKI, et al.	
	FILING DATE September 12, 2018	GROUP 2816

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	AA	2018/0090509	03/29/2018	Zhang et al.			
	AB	2018/0323207	11/08/2018	Shim et al.			
	AC	2019/0081065	03/14/2019	Lee			
	AD	2019/0288003	09/19/2019	Shim et al.			
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						
	AM						
	AN						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION YES	TRANSLATION NO
	AO					
	AP					
	AQ					
	AR					
	AS					
	AT					
	AU					
	AV					

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)

	AW	
	AX	
	AY	
	AZ	☐ Additional References sheet(s) attached

Examiner	/MOLLY K REIDA/	Date considered	04/07/2020

*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.K.R/

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

CUSTOMER NUMBER
22850

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/129,082	09/12/2018	Jun FUJIKI	516693US	1059

TITLE OF INVENTION: SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR MANUFACTURING SAME

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	07/15/2020

EXAMINER	ART UNIT	CLASS-SUBCLASS
REIDA, MOLLY KAY	2816	257-324000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Oblon, McClelland,
2 Maier & Neustadt, L.L.P.
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: TOSHIBA MEMORY CORPORATION

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Minato-ku, JAPAN

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ☒ Corporation or other private group entity ❑ Government

4a. Fees submitted: ☒ Issue Fee ❑ Publication Fee (if required) ❑ Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

☒ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. 15-0030

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date Surinder Sachar 7/15/2020

Typed or printed name _____ Registration No. Registration No.: 34,423

PTOL-85 Part B (08-18) Approved for use through 01/31/2020 OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

DOCKET NO: 516693US

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF	:
JUN FUJIKI, ET AL.	: EXAMINER: REIDA, MOLLY KAY
SERIAL NO: 16/129,082	:
FILED: SEPTEMBER 12, 2018	: GROUP ART UNIT: 2816
FOR: SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR MANUFACTURING SAME	:

COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

Commissioner:

Applicants acknowledge with appreciation the indication of allowability of the claimed invention. In response to the Examiner's Statement of Reasons for Allowance in the Notice of Allowance of April 15, 2020, Applicants respectfully submit the following comments.

In the Examiner's Statement of Reasons for Allowance on pages 3-4 of the Notice of Allowance mailed April 15, 2020, the paragraph states in part:

> Re independent claim 1, there is no teaching, suggestion, or motivation from the prior art of record, nor does the prior art of record otherwise make obvious the limitations of "…a semiconductor substrate including a formed in an upper layer portion of the semiconductor substrate; a first conductive film…coupled to the diode; a semiconductor member piercing the stacked body an being connected to first conductive film…", in combination with the other limitations.

It is respectfully submitted that independent Claim 1 does not include all of the elements discussed above. Claim 1 does not recite "a semiconductor substrate including a formed in an upper layer portion of the semiconductor substrate." Accordingly, it is respectfully submitted that the above quoted statement does not apply to independent Claim 1

(and claims dependent therefrom), to the extent the language used in the statement differs from the language of the claims.

Respectfully Submitted,

OBLON, McCLELLAND,
MAIER & NEUSTADT, L.L.P.

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(OMMN 07/09)

Electronic Patent Application Fee Transmittal

Application Number:	16129082
Filing Date:	12-Sep-2018
Title of Invention:	SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR MANUFACTURING SAME
First Named Inventor/Applicant Name:	Jun FUJIKI
Filer:	Daniel J. Pereira/Dakota Brown
Attorney Docket Number:	516693US

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	1000	1000

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1000**

Electronic Acknowledgement Receipt

EFS ID:	40005132
Application Number:	16129082
International Application Number:	
Confirmation Number:	1059
Title of Invention:	SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR MANUFACTURING SAME
First Named Inventor/Applicant Name:	Jun FUJIKI
Customer Number:	22850
Filer:	Daniel J. Pereira/Dakota Brown
Filer Authorized By:	Daniel J. Pereira
Attorney Docket Number:	516693US
Receipt Date:	15-JUL-2020
Filing Date:	12-SEP-2018
Time Stamp:	12:01:31
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$1000
RAM confirmation Number	E20207EC01457796
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		516693us.pdf	1083659 b8240296eae91c112f5cefb37e97f6230d3295fd	yes	3

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Issue Fee Payment (PTO-85B)	1	1
	Post Allowance Communication - Incoming	2	3

Warnings:

Information:

2	Fee Worksheet (SB06)	fee-info.pdf	30488 d821b3044fd26e42b5e88dccec01c1d371a04a39	no	2

Warnings:

Information:

Total Files Size (in bytes):	1114147

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/129,082	08/25/2020	10756104	516693US	1059

22850 7590 08/05/2020

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ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

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Shinya ARAI, Yokkaichi, JAPAN;
Kotaro FUJII, Yokkaichi, JAPAN;