

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,

Petitioner,

v.

NETLIST, INC.,

Patent Owner

Case IPR2025-00002

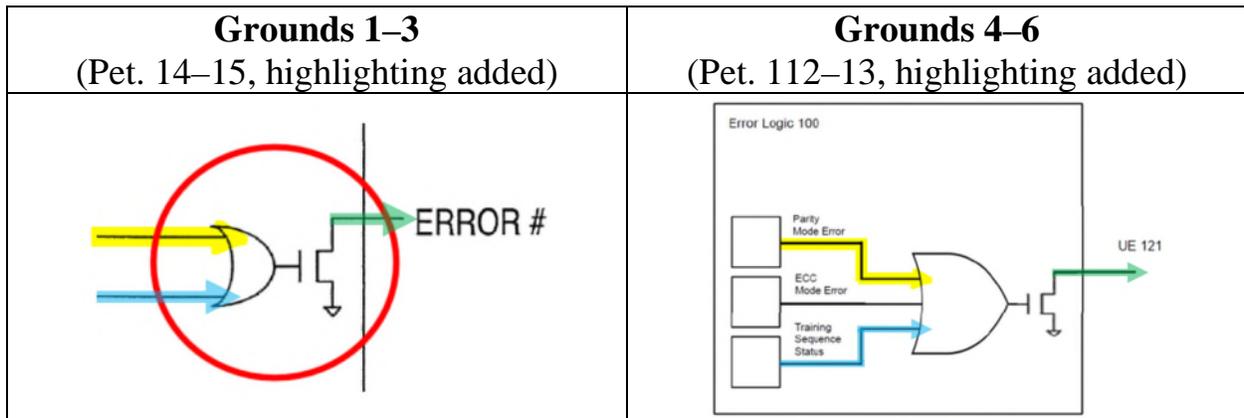
Patent 11,880,319

**PETITIONER'S AUTHORIZED RESPONSE TO
PATENT OWNER'S REQUEST FOR DIRECTOR REVIEW OF
DECISION GRANTING INSTITUTION**

A. *The Board properly analyzed the “[first/second] signaling interface via the open drain output” (ID 52–54, 59–61; DR Req. 8–10):* The Board properly understood the claimed “signaling interface[s]” in light of Figure 3 (below right), which everyone agrees illustrates the claim language, *see* DR Req. 2–3, 8; ID 8, 54; Pet. 21. Netlist’s arguments about the claimed “signaling interface[s]” ignore the express claim language requiring the *same* “open drain output” (green below) for *both* claimed signaling interfaces (below left):

319 claim language EX1001, 14:49–:56	Pet. 21 (highlighting added) (discussing Fig. 3 of the 319 Patent)
<p>[1.d.1] wherein the memory subsystem is configured to provide a first signaling interface via the open drain output during normal operations and</p> <p>[1.d.2] a second signaling interface via the open drain output during an initialization operation including initialization operation sequences, wherein the second signaling interface is distinct from the first signaling interface</p>	<div data-bbox="841 890 1235 1224" data-label="Diagram"> <p>The diagram shows a memory module 10 with an open-drain output 12. Inside the module, a transistor 36 is connected to the output line. The gate of transistor 36 is connected to a multiplexor 42. The multiplexor 42 has two inputs: a task_in_progress signal 44 and an error signal 46. The multiplexor 42 is controlled by a control signal 20. The output of the multiplexor 42 drives the gate of transistor 36. The transistor 36 is connected to the output line 12 and to ground. The output line 12 is also connected to a pull-up resistor 18. The entire module is enclosed in a dashed box 10.</p> </div> <p>Figure 3 illustrates an exemplary memory module (10) with an open-drain output (12) whose transistor (36) is controlled by a multiplexor (42) driving the transistor’s gate with either (i) a task_in_progress signal (44) “when the memory module 10 is in the initialization mode or is executing the at least one initialization sequence,” or (ii) an error signal (46) to report parity errors during operational mode. EX1001, Fig.3 (below), 11:15–:34; EX1003, ¶59.</p>

All grounds in the Petition relied on one of two structures, shown below, each of which is nearly identical to Figure 3 in the patent, shown above, because they include **both** a “*a first signaling interface [yellow arrow] via the open drain output [green]”* to report parity errors during normal operations, **and** a distinct “*second signaling interface [blue arrow] via the open drain output [green]”* to report training status during initialization. See Pet. 14–15, 40–41, 48 (citing pp.12–15), 63–69 (citing pp.47–50), 82–83, 112–15; Prelim. Reply (Paper 11) 1–2:



The Board agreed with Petitioner that the plain language of the claims requires the “*same ‘open drain output’ [green above] for both signaling interfaces.*” ID 23, 54, 61. Netlist concedes this critical point. DR Req. 2 (pointing to the *same* “open drain” for the “two distinct signaling interfaces”). And Netlist does not contest the Board’s finding that in Grounds 2 and 5 (corresponding to the two figures above, respectively), Petitioner identified “[f]or the first interface . . . Hazelzet’s disclosure of parity error signal PERR 111 applied, during parity mode, to open drain output UE 121 . . . [and] [f]or the second interface . . . a separate status

signal ***applied, during initialization, to open drain output UE 121***” ID 53–54, 59–61. That satisfies the claims, because there are two distinct signaling interfaces (yellow vs. blue), applied during two distinct operations (normal vs. initialization), to the same open drain output (green).

Netlist argues that the Board “did not consider the distinct signaling interfaces shown in Figure 3” and thus the Board supposedly “construed the claimed interfaces as signals.” DR Req. 6, 8–10. Neither is true. The Board expressly considered Figure 3, *see* ID 8, 54, and did not construe “interfaces as signals,” as asserted by Netlist, but rather rejected Netlist’s argument that there must be *distinct* first and second “interface *circuitry*,” ID 52–54. The claims do not say “interface *circuitry*” and instead require the *same* “open drain output” for *both* signaling interfaces. ID 23, 54. That is why the Board wrote, “the claims are only directed to *providing* distinct first and second signaling interfaces *via the open drain output*. This [is] not a reference to interface circuitry — it makes no sense to ‘provide’ circuitry ‘via the open drain output.’ Rather, two distinct interface *signals* are provided via the open drain output.” ID 54. Accordingly, the Board correctly concluded that the claims were obvious in light of the structures shown above (p.2) for the asserted Grounds. ID 52–54, 59–61.

B.1. Netlist waived its “waste of Board resources” argument (DR Req. 10–13): Netlist has waived the argument that institution would be a “waste of Board

resources” given the supposedly “voluminous record.” DR Req. 10–13. Netlist never presented this argument to the Board in the first place, which is fatal: “The Director will not consider . . . new arguments not part of the official record.” *See* <<https://www.uspto.gov/patents/ptab/decisions/director-review-process>> (§ 3.E).

Netlist’s argument is also incorrect. First, Netlist fails to identify any “Article III court” that will address these issues (DR Req. 10, 12–13), because currently there is no parallel district court litigation addressing unpatentability (Pet. 116–17), which is why Netlist never raised any *Fintiv* arguments. Second, there is no need for “third-party subpoena powers” (DR Req. 12), because both Netlist and Samsung are members of JEDEC and their employees were personally involved in the events in question (EX1046, 1; EX1037, 21), and JEDEC has voluntarily provided Netlist and Samsung with requested information (EX2007; EX1050; EX1092). Third, the public accessibility of the proposal to JEDEC (EX1015, EX1039) is not an issue on which Samsung has submitted “expert testimony” (DR Req. 12–13), because it is a legal issue based on non-technical fact questions. Fourth, public accessibility is not a complicated issue: Netlist’s provisional patent expressly references the “proposal in JEDEC” (EX1008, 22), and Netlist concedes that the relevant public would have “known” about this proposal (EX1105, 18; EX1003, 145–46), so the Institution Decision directed the parties to focus on narrow issues related to accessibility, such as who could “join JEDEC” (ID 35),

which is hardly a complicated issue.

B.2. The Board correctly rejected Netlist’s argument that “six grounds . . . is a waste of Board resources” (ID 17; DR Req. 13–15): The Board correctly concluded that “instituting a trial is an efficient use of the Board’s time and resources.” ID 17. That is because in both this IPR and the parallel IPR2025-00001, (i) all six grounds rely on Hazelzet as the primary reference, (ii) all six grounds challenge all claims using the same basic structure shown above (p.2), and (iii) two judges on the panel are already familiar with this structure and the relevant record from two related IPRs successfully challenging substantially identical claims. ID 17–24; EX1102, 6–8, 51–53, 66–67, 71–75; EX1103, 6–9, 50–52, 71–73, 78–82. Thus, Netlist is wrong to compare this IPR to *Adaptics* (DR Req. 15), “which involved potentially hundreds of distinct grounds.” *FreeWheel Media, Inc. v. Intent IQ, LLC*, IPR2024-00422, Paper 10, at 18 (PTAB Oct. 2, 2024). Furthermore, the Board correctly rejected Netlist’s argument that the Petition improperly “incorporated by reference from other documents.” DR Req. 13–14. The Board found that Petitioner provided “particularity and specificity” and “sufficient explanation and evidence.” ID 25–26. Citing to support in the record is not incorporation by reference. *See* 37 C.F.R. §§ 42.6(a)(3), .22(c).

Dated: June 5, 2025

/Eliot D. Williams/
Eliot D. Williams, Reg. #50,822
BAKER BOTTS L.L.P.
700 K Street, N.W.

Washington, D.C. 20001
T: (202) 639-1334
F: (202) 639-1167

Theodore W. Chandler
Reg. No. 50,319
BAKER BOTTS L.L.P.
1801 Century Park East
Suite 2400
Los Angeles, CA 90067
T: (213) 202-5702
F: (213) 202-5732

Ferenc Pazmandi
Reg. No. 66,216
BAKER BOTTS L.L.P.
101 California Street
Suite 3200
San Francisco, CA 94111
T: (415) 291-6255
F: (415) 291-6355

Brianna L. Potter
Reg. No. 76,748
BAKER BOTTS L.L.P.
1001 Page Mill Road
Building One, Suite 200
Palo Alto, CA 94304
T: (650) 739-7556
F: (650) 739-7656

*Counsel for Petitioner
Samsung Electronics Co., Ltd.*

CERTIFICATE OF COMPLIANCE

I hereby certify that this **Petitioner’s Authorized Response to Patent Owner’s Request for Director Review of Decision Granting Institution**, excluding the parts of the brief exempted by 37 C.F.R. § 42.24, complies with the page limits provided by the Director’s email on May 29, 2025, which stated: “Petitioner is authorized to submit a response limited to the issues raised in the Director Review requests, of no more than five pages, to be filed within five business days of this email. Any such responses must be filed in P-TACTS, i.e., by selecting the ‘Other: Other’ paper type and the paper must be titled ‘Authorized Response to Director Review Request’ or it may not be considered. No new evidence is permitted. No further briefings are authorized at this time.” EX3100.

Dated: June 5, 2025

/Eliot D. Williams/
Eliot D. Williams, Reg. #50,822
BAKER BOTTS L.L.P.
700 K Street, N.W.
Washington, D.C. 20001
T: (202) 639-1334
F: (202) 639-1167

*Counsel for Petitioner Samsung
Electronics Co., Ltd.*

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), I certify that on this 5th day of June, 2025,

Petitioner’s Authorized Response to Patent Owner’s Request for Director

Review of Decision Granting Institution was served by email on the following
counsel for Patent Owner:

Richard M. Bemben (Reg. No. 68,658) STERNE, KESSLER, GOLDSTEIN & FOX PLLC 1101 K Street NW, 10th Floor Washington, DC 20005 Phone: (202) 772-8549 Fax: (202) 371-2540 Email: PTAB@sternekessler.com rbemben-PTAB@sternekessler.com	Jennifer Meyer Chagnon (Reg. No. 55,440) STERNE, KESSLER, GOLDSTEIN & FOX PLLC 1101 K Street NW, 10th Floor Washington, DC 20005 Phone: (202) 772-8890 Fax: (202) 371-2540 Email: PTAB@sternekessler.com jchagnon-PTAB@sternekessler.com
Richard A. Crudo (Reg. No. 65,245) STERNE, KESSLER, GOLDSTEIN & FOX PLLC 1101 K Street NW, 10th Floor Washington, DC 20005 Phone: (202) 772-8549 Fax: (202) 371-2540 Email: PTAB@sternekessler.com rcrudo-PTAB@sternekessler.com	Raymond K. Chan (Reg. No. 66,164) NETLIST, INC. 111 Academy Way, Suite 100 Irvine, California 92617 Phone: (949) 679-0101 Fax: (949) 435-0031 Email: rchan@netlist.com
Tobin L. Hobbs (Reg. No. 63,260) NETLIST, INC. 111 Academy Way, Suite 100 Irvine, California 92617 Phone: (949) 679-0127 Fax: (949) 435-0031 Email: thobbs@netlist.com	

Dated: June 5, 2025

/Eliot D. Williams/
Eliot D. Williams, Reg. #50,822
BAKER BOTTS L.L.P.
700 K Street, N.W.
Washington, D.C. 20001

T: (202) 639-1334
F: (202) 639-1167

*Counsel for Petitioner Samsung
Electronics Co., Ltd.*