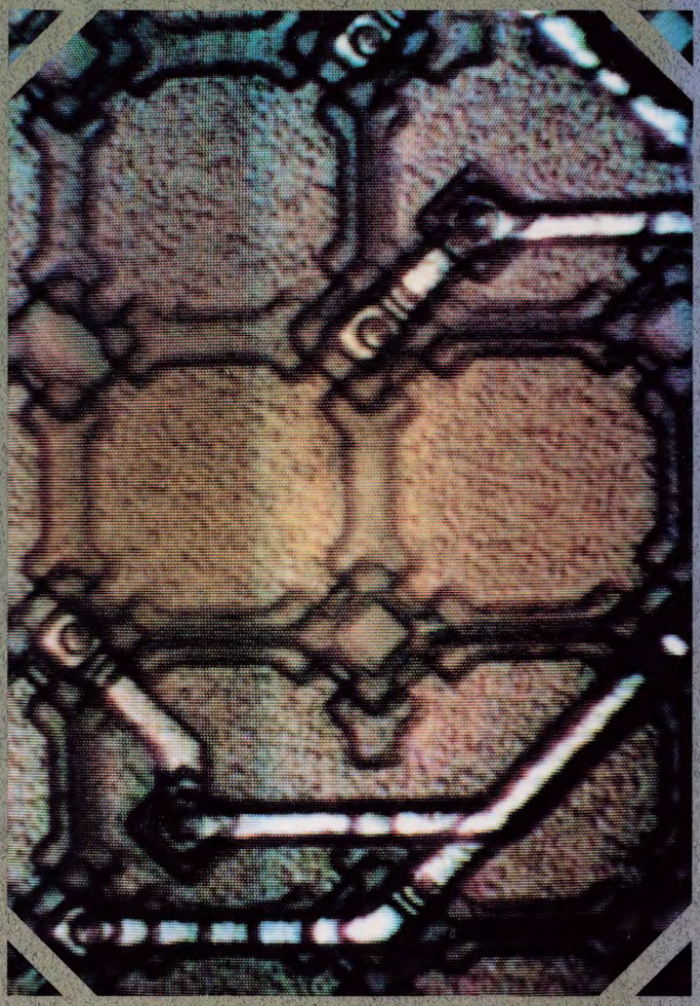
Second Edition

DESIGN OF ANALOG-DIGITAL VLSI CIRCUITS FOR TELECOMMUNICATIONS AND SIGNAL PROCESSING



JOSÉ E. FRANCA / YANNIS TSIVIDIS, Editors

FRANCA / TSIVIDIS

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VLSI is revolutionizing telecommunications and signal processing. To help readers keep pace, this volume examines the techniques that make this possible. **José E. Franca** and **Yannis Tsividis** enlist the aid of other top scientists, researchers, and educators to offer readers state-of-the-art theories, applications, and advances. The book covers circuits and systems.

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Contents

(1) Avoid the use of internal resistors. These can appear as op amp loads, forcing the need for complex buffer stages.

(2) Constrain the function around an op amp to an inverting configuration, avoiding such functions as voltage followers. The noninverting configuration requires an amplifier with large input common-mode range.

(3) Avoid configurations which use MOS switches around the feedback path of an op amp. This restriction is based on similar arguments as those applying to rule (2).

(4) Design the systems in such a way as to accommodate for a wide spread in the DC voltage gain. This uncertainty is mostly due to inaccuracies in the modelling of the MOS transistors in the simulators.

(5) In the case of analog-to-digital (ADC) or digital-to-analog converters (DAC), choose *sequential* techniques whenever possible. This approach, which is somehow opposed to the idea of parallelism, generally simplifies the amount of analog circuitry at the expense of some added digital complexity and reduced speed of operation.

(6) Design the systems using differential circuitry whenever possible. The op amps will be simpler, and most importantly, this may be the only way to achieve the desired specifications of dynamic range. The cost for this is an increased amount of internal elements and busing.

2. The Differential Circuit Approach

Digital circuitry generates a large amount of switching noise which appears in the power lines, the common substrate, and as parasitic capacitive coupling between the internal interconnections. This scenario imposes as one of the main goals for the designer that all the necessary precautions be taken in order to make the analog circuit highly immune to this noise coupling. Differential circuitry is a technique which provides a way to achieve this immunity. Furthermore, differential circuitry doubles the effective signal swing which increases the dynamic range, a very important feature in high-density technology where the maximum operating supply is limited to 5 volts or less. The use of differential circuits for the analog paths generally implies a larger number of components and interconnections. However, as will be seen later, op amps with comparable functionality are considerably simpler. Another

advantage of differential circuits is that the signal is immune to noise in the internal reference node (e.g., $1/2(V_{DD} - V_{SS})$, a feature which is very important in single supply systems.

For certain applications such as those requiring the processing of an input current (or charge), the use of differential circuitry cannot be easily implemented. In these cases, single-ended circuitry is the only practical alternative. However, if there is a significant amount of signal post-processing, one can always implement a single-ended to differential conversion as close to the input as possible, aiming at keeping the amount of single-ended circuitry to a minimum. With this consideration in mind, the need for single-ended op amps also arises, which in general will have to be subject to similar minimization arguments as those applying to their differential counterparts.

In a differential amplifier there is an additional *degree of freedom* over a single-ended amplifier. While the differential output should be proportional to a differential input signal, the average voltage of these two outputs should also be controllable with another input signal. This is usually referred to as the common-mode input. Fig. 1 shows a representation of a differential op amp where the inner amplifier represents the common-mode path.

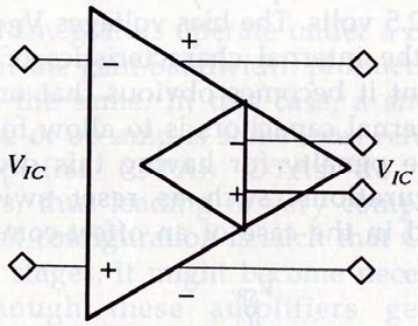

Fig. 1: Differential op amp.

In most applications, the common-mode input is fed with a signal derived from the average of the two outputs However, it could also be possible to superimpose another signal to that average which may or may not be directly related to the differential signal. Fig. 2 shows a differential switched-capacitor integrator with the averaging of the two outputs implemented by means of an additional set of switched-capacitors. C_U is usually the unit capacitor, while C_X has to be large enough to keep the common-mode switching noise within acceptable levels.

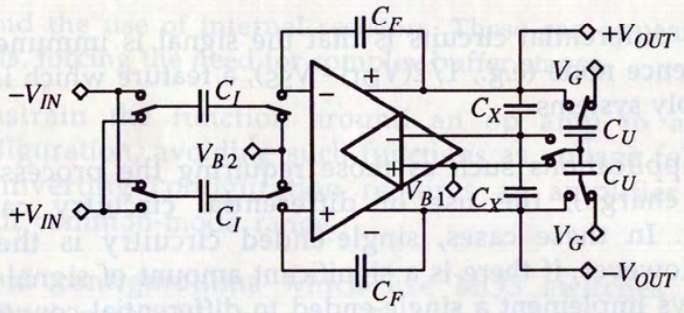

Fig. 2: Differential switched-capacitor integrator.

It should be noted that in Fig. 2 the bias point of the differential switched-capacitors can be chosen arbitrarely. In fact, V_{B2} and V_G do not have to be the same, and they can both be different from V_{B1}, the bias point for the common-mode switched-capacitors. This flexibility in choosing these bias points results in the possibility of superimposing DC voltages to the signal in order to avoid level-shifting operations inside the op amp. A numerical example can illustrate this idea: V_G is chosen to maximize the swing; therefore, for a single voltage supply of 5 volts, V_G=2.5V. This implies that the differential voltage V_{OUT} will have an average value of 2.5 volts. The bias voltages V_{B1} and V_{B2} can be chosen in such a way as to fit the internal characteristics of the amplifier or other requirements. At this point it becomes obvious that one of the main goals of level-shifting with the external capacitors is to allow for op amps with limited input common-range. The penalty for having this diversity of bias voltages precludes certain configurations, such as reset switches in parallel with capacitors, which is found in the case of an offset-compensated amplification-module (Fig. 3).

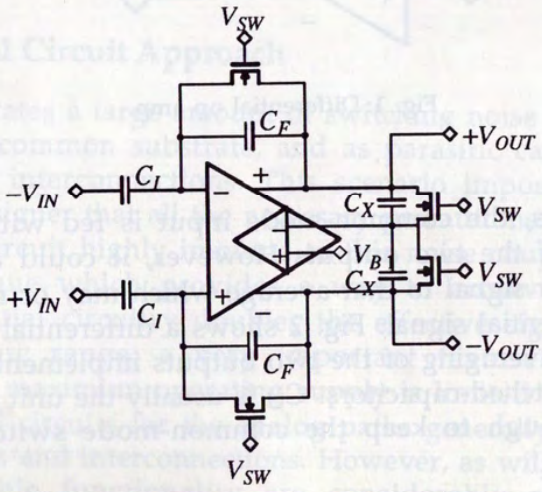

Fig. 3: Amplifier with MOS reset switch.

Fig. 4 describes a simplified schematic for an alternative solution that avoids the use of MOS switches while still performing the discharging of the feedback capacitor C_F. After examining the characteristics of different amplifiers, the reasons for avoiding certain configurations will become more obvious.

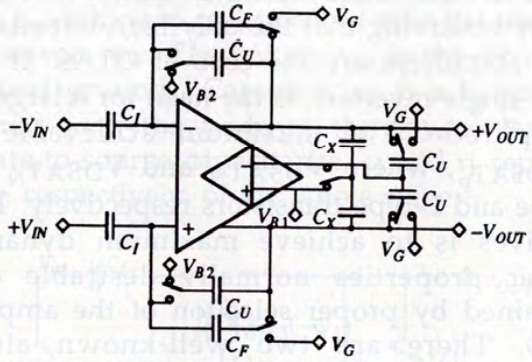

Fig. 4: Feedback reset without switch.

3. The Number of Internal Stages

Most switched-capacitor integrators operate under a condition in which $C_F >> C_I$ (Fig. 2). This implies that the gain-bandwidth products of the integrator and the op amp are essentially the same. In this case, a single voltage-gain stage is recommended. This type of op amp is sometimes referred to as an operational transconductance amplifier (OTA). OTAs do not require additional compensation capacitors, thus leading to very compact circuits. On the other hand, when the feedback configuration is such that $C_D << C_I$ (Fig. 3), such as in high-gain amplification stages, it might become necessary to have a multiple-stage amplifier. Although these amplifiers generally require phase-compensation, this can be reduced to minimum capacitance due to the low amount of feedback.

Another instance in which multiple-stage op amps are required is when heavy resistive and/or capacitive loads need to be driven, as in the case of off-chip drivers. These amplifiers can become very complex because of the limitations of MOS transistors as current drivers. Examples of these will be given later.

4. Cascode Op Amps

Fig. 5 shows a typical implementation of a simple cascode amplifier. It is well known from single amplifier theory that cascode stages increase the voltage gain by means of boosting their effective output impedance. This boost is