IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	G.R. MOHAN RAO
Application No.:	17/728,588
Confirmation No.:	2783
Filed:	April 25, 2022
Group No.:	2892
Examiner:	AJAY ARORA
For:	SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION OF DOUGLAS HOLBERG UNDER 37 USC SECTION 1.132

I. INTRODUCTION

I have been engaged by Greenthread LLC to opine on Application Serial Number 17/728,588 ('588). My opinions are set forth herein. I submit this Declaration on behalf of Greenthread LLC in connection with Examiner's Office Action dated July 18, 2024.

A. Education and Relevant Experience

My education includes a B.S. in Electrical Engineering from Texas A&M University in 1977, followed by a M.S. in Electrical Engineering from the University of Texas at Austin in 1989. I earned a Ph.D. in Electrical Engineering from the University of Texas at Austin in 1992.

I have over 40 years of experience in the electronics field. During that time, I have worked for several different electronics companies including: Mostek, Texas Micro Engineering (acquired by Crystal Semiconductor), Crystal Semiconductor, Cirrus Logic, Cygnal Integrated Products, and Silicon Laboratories. I joined Silicon Laboratories when they acquired Cygnal, which I co-founded in 1999.

I am a named inventor on 43 U.S. granted patents. I have held a variety of engineering positions throughout my career, from circuit designer, design manager, Director of Engineering, Chief Technology Officer (CTO), Vice President (V.P.) of Engineering, and V.P. of Technology. In addition to my engineering experience, I also have served as an adjunct faculty member at the University of Texas, where I taught CMOS analog and mixed-signal design for six years.

I am the co-author of the textbook CMOS Analog Circuit Design, the first edition of which published 1987. As explained in the Preface of the second edition, published in 2002, the objective of the textbook is to teach the fundamentals and background that are necessary to understand how a circuit works. It is now available in third edition and published in English and Chinese (first and second edition). This textbook is widely used throughout the world by new and experienced engineers in industry and by students in the classroom.

Upon graduating from Texas A&M University, I went to work for Mostek Corporation designing integrated circuits for telecommunications applications. I designed an integrated dual tone multi frequency (DTMF) generator. I received my first

patent for this integrated DTMF generator. After leaving Mostek, I joined a startup company, Texas Micro Engineering, as the second employee. At Texas Micro Engineering, I designed, among other things, a dual-channel (atrium-ventricle) pacemaker sense amplifier/filter using discrete-time switched-capacitor technology.

While enrolled in the Masters/Ph.D. program at the University of Texas at Austin, I worked on the application of bipolar technology to dynamic random access memory (DRAM) sense-amplifier architectures and circuit-simulation algorithms. While at The University of Texas at Austin, I also designed and laid out the mask set (The Holberg Mask Set) still in use by the fabrication class/lab.

Upon graduating with a Ph.D. in Electrical Engineering, I went to work for Crystal Semiconductor/Cirrus Logic, where I designed high frequency synthesizers for hard-disk read-channel applications. I managed a group designing charge-coupled device (CCD) interface circuits for digital camera applications, as well as television encoder chips and CMOS imagers.

Upon leaving Cirrus, I started a company called Cygnal Integrated Products that developed mixed-signal microcontrollers. At Cygnal, I was the founder, CTO, V.P. of Engineering, and an individual contributor. My company was later purchased by Silicon Labs, where I remained employed as a manager of the microcontroller group, followed by the position of V.P. of Technology.

I have read and am familiar with the file wrapper and specification of US Patent Application Serial Number 17/728,588. I am also familiar with the terminology utilized in describing the structure of semiconductor device.

My analyses set forth in this declaration are informed by my experience in the semiconductor industry. I consider myself skilled in the art of the operation of semiconductor devices,

The '588 Patent application is titled "SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS." Prior to reviewing the '588 Patent, I was well familiar with the subject matter described and claimed therein.

B. Materials Considered

The analysis that I provide in this Declaration is based on my education and experience as an engineer in the semiconductor industry. I have read and am familiar with the documents listed below. I am also familiar with the terminology utilized in describing the structure of semiconductor devices.

Item No.	Description
1	U.S. Patent Application 17/728,588 to Rao.
2	Prosecution History of U.S. Patent Application 17/728,588

II. ANALYSIS

In ¶[0011], a description of a p-n-p transistor is set forth specifically with respect to Figure 1:

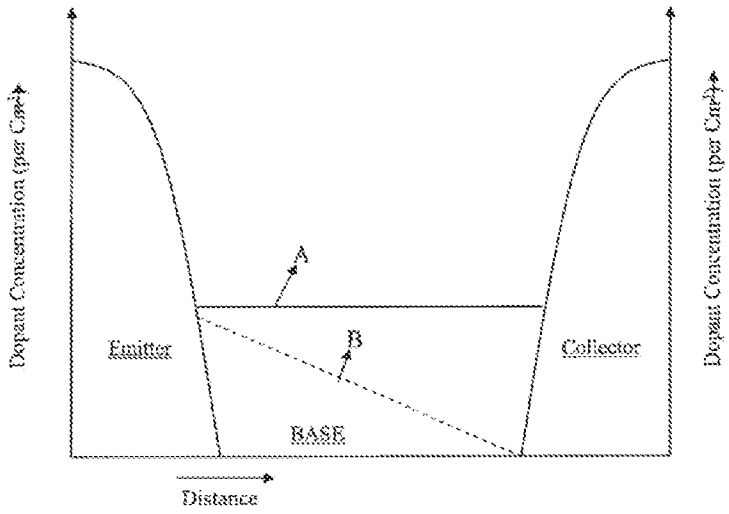


Figure 1 Prior Art

The structure of this transistor is described as having a base region that has a donor dopant concentration gradient that is high at the emitter-base junction and low at the base-collector injunction. This corresponds to the label "B" in Figure 1. This is defined as a "relative slope" which means nothing more than the fact that one-side is relatively lower than the other side. This slope is defined "throughout" the base to create "a suitable aiding drift electric field, to help the holes (p-n-p transistor) traverse from the emitter to collector." In an n-type material, the holes are "minority" carriers. The minority carriers are injected as a result of placing a voltage across the base-emitter

junction of the transistor. It is also noted that this is "applicable" to n-p-n transistors. In an n-p-n transistor, p-type minority carriers are transitioning across a p-type base and the minority carries for the p-type material are electrons. Thus, this ¶[0011] describes a gradient for aiding the movement of minority carriers from one point to another through a region. In order to do such, a drift electric field is created via the gradient. The purpose is not to assist movement of the minority carriers "partially" through the region but, rather, from one border to the other.

In the embodiment with respect to Figures 5A, 5B and 5C in ¶ [0013], the Specification at ¶0013] describes the use of the "donor gradient" as being of a benefit to very large scale integrated circuits. The purposes stated are a desire to remove minority carriers at the surface that are spuriously generated by clock switching, which can discharge various "actively held high" nodes. The use of the gradient dopant profile is noted as a "novel technique" that "creates a drift field to sweep these unwanted minority carriers from the active circuitry at the surface into the substrate in a monolithic die as quickly as possible." It is also stated that the creation of "subterranean" recombination centers underneath the wells "is not practical for VLSI circuits." Thus, it is my opinion that this statement teaches away from creating subterranean recombination centers below the wells. The embodiment initially refers to a subterranean n- layer as having a graded donor concentration (an n-type material) to sweep the minority carriers (holes) "deep into the substrate." Since this is an n-type material, it is a "donor" type material and would have a slope resulting in a drift field

that would aid in moving minority carriers (holes in an n-type material) in a direction away from the active circuitry and "into the substrate." In a p-type material, the minority carriers would be electrons.

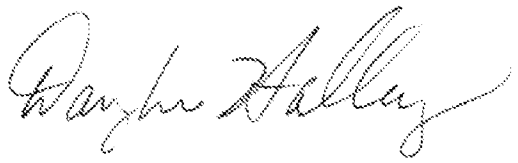
It is my opinion that a POSITA would recognize that the description of a donor dopant concentration for creating a drift electric field that aids movement of minority carriers within a region from one boundary of that region to the other boundary thereof in any embodiment in the Specification would necessarily define that gradient as to **all** embodiments. The function of the graded dopant concentration in the embodiment of Figure 1 (¶[0011]) is identical to the function of the graded dopant concentration described with respect to the embodiments of Figures5A, 5B and 5C. It is to create an electric field to aid in movement of minority carriers from one boundary to the other of any region.

The Examiner also stated with respect to how the donor gradient is described with respect to the description of ¶[0011] (Figure 1) as follows: "[t]hus, the disclosure of the graded dopant or 'relative slope' or 'donor concentration throughout the base' are only with respect to base of a p-n-p transistor." I disagree with this position. The description of the base and the concentration thereof is a description of a region having a boundary. This region is a region through which carriers are transmitted from one side to the other. The gradient therethrough is described with respect to a donor region, i.e., an n-type region, that just happens to be utilized as the base of a transistor in the disclosed embodiment. But it is still nothing more than a region through which carriers are

transmitted and the function of that gradient is to create "a suitable aiding drift electric field, to help the holes (minority carriers in a p-n-p transistor) traverse from emitter to collector." The emitter is just one boundary with the base and the collector is the other boundary with the base, but the base is just a region disposed therebetween through which holes (minority carriers for a p-n-p transistor or electrons as minority carriers for an n-p-n transistor) can traverse. The gradient just affects the function of that traversal within the particular region, which region just happens to be a base. But that function is not restricted only to a transistor; rather, it just describes a function of that region.

The Examiner has also asserted that the term "throughout" is only relevant to the function of the base of a transistor, which assertion is not a correct interpretation of how that term is utilized in the Specification. In the embodiment of ¶ [0011], the Specification refers to the benefits of using a "donor gradient" as "also" providing a benefit. This benefit is defined as creating "a drift field to sweep these unwanted minority carriers from the active circuitry at the surface into the substrate …" This language is consistent with the function of the donor gradient in the base of the transistor in the embodiment of ¶[0011]. This function cannot happen unless the gradient extends from one side of a region to the other. If not, then the minority carriers would be swept into some middle portion of a region and not "into the substrate." In my opinion, a POSITA would, from the reading of the embodiment of ¶[0013] understand that the donor gradient has a profile that is decreasing from one side to the other such that an electric drift field is created to aid movement of minority carriers from one side of the

region (or well) to the other side thereof. The Examiner's assertion that the description of the transistor base in the embodiment of ¶[0011] with respect to the functionality thereof is only applicable to the transistor embodiment is believed to be an incorrect interpretation. It seems that the Examiner is taking the position that a description of one embodiment, that of ¶[0011] and the description that the gradient profile extends from one side to the other, i.e., "throughout," is such that it only applies to the description with respect to the transistor and cannot be extended to any other embodiment. However, in my opinion, a POSITA would understand that the functionality provided by that doping profile and gradient relative to the operation of a transistor is the same functionality that is described with respect to the embodiment of ¶[0013] in that the minority carriers are moved from one area to another deep into the substrate with the gradient providing the same function i.e., creating an electric drift field to aid the movement of carriers. Additionally, it would be unreasonable for a POSITA to not consider that the gradient extends all the way through the region or well because the Specification specifically states that creation of "subterranean" recombination centers underneath the wells "is not practical for VLSI circuits." If the gradient does not extend all the way through the region, there is no way for the carriers to move into the substrate, as they would recombine within the region.



Executed on August 1, 2024 _____

Douglas Holberg.

No fee is due in this matter and, thus, none is included. Please charge any deficiency or credit any overpayment to deposit account number 50-0208/GRTD60-35367.

Respectfully submitted,
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