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Paper 21
Date: January 8, 2025

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MERCEDES-BENZ USA, LLC,
Petitioner,

v.

DAEDALUS PRIME LLC,
Patent Owner.

IPR2023-01343
Patent 8,898,494 B2

Before WILLIAM V. SAINDON, THOMAS L. GIANNETTI, and GREGG I. ANDERSON, *Administrative Patent Judges*.

GIANNETTI, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining No Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

A. Background

Mercedes-Benz USA, LLC ("Petitioner") filed a Petition requesting *inter partes* review of claims 1–7, 13–15, 17, and 18 (the "challenged claims") of U.S. Patent No. 8,898,494 B2 (Ex. 1001, the "'494 patent"). Paper 2 ("Pet."), 1. Daedalus Prime LLC ("Patent Owner") waived filing of a preliminary response. Paper 6.

We determined that Petitioner established a reasonable likelihood that it would prevail with respect to at least one claim challenged in the Petition. Paper 7 ("Institution Dec."). We therefore instituted *inter partes* review as to all of the challenged claims of the '494 patent and all of the asserted grounds of unpatentability. *See SAS Inst. Inc. v Iancu*, 138 S. Ct. 1348, 1356 (2018); 37 C.F.R. § 42.108 (a) ("When instituting *inter partes* review, the Board will authorize the review to proceed on all of the challenged claims and on all grounds of unpatentability asserted for each claim.").

Following institution of the trial, Patent Owner filed a Response (Paper 10, "PO Resp."), Petitioner filed a Reply (Paper 13, "Pet. Reply"), and Patent Owner filed a Sur-reply (Paper 14, "PO Sur-reply").

An oral hearing was held on November 13, 2024. A transcript of the hearing is part of the record. Paper 20 ("Hearing Tr.").

We have jurisdiction under 35 U.S.C. § 6. This decision is a Final Written Decision issued pursuant to 35 U.S.C. § 318(a). For the reasons we discuss below, we determine that Petitioner has not proven by a preponderance of the evidence that any of the challenged claims of the '494 patent are unpatentable.

B. Related Proceedings

The parties identify the following district court and ITC proceedings involving the '494 patent: (1) *Daedalus Prime LLC v. Arrow Electronics, Inc.*, 1:22-cv-01107 (D. Del.); (2) *Daedalus Prime LLC v. Mazda Motor Corporation*, 1:22-cv-01109 (D. Del.); (3) *Daedalus Prime LLC v. Mazda Motor Corporation*, 1:22-cv-01108 (D. Del.); (4) *Daedalus Prime LLC v. Samsung Electronics Co., Ltd.*, 2:22-cv-00352 (E.D. Tex.); (5) *Certain Integrated Circuits, Mobile Devices Containing the Same, and Components Thereof*, Inv. No. 337-TA-1335 (USITC); and (6) *Certain Semiconductors and Devices and Products Containing the Same, Including Printed Circuit Boards, Automotive Parts, and Automobiles*, Inv. No. 337-TA-1332 (USITC). Pet. 1–5; Paper 3, 2.

The '494 patent also was involved in IPR2023-00617, now terminated. Pet. 5; Paper 3, 3.

C. Real Parties-in-Interest

Petitioner identifies the following real parties-in-interest: Mercedes-Benz USA, LLC; Mercedes-Benz Group AG; Mercedes-Benz AG; and Mercedes-Benz Intellectual Property GmbH & Co. KG. Pet. 1. Patent Owner identifies Daedalus Prime LLC as the real party-in-interest. Paper 3, 2.

D. The '494 Patent

The '494 patent is titled "Power Budgeting Between a Processing Core, a Graphics Core, and a Bus on an Integrated Circuit When a Limit is Reached." Ex. 1001, (54). The '494 patent relates to an apparatus, method, and system for efficiently balancing performance and power between

processing elements or a communication bus by identifying and alleviating bottlenecks based on measured workloads. *Id.* at Abstract, 1:12–16. Bottlenecks can occur at the level of processing elements, such as a CPU or GPU, or at a communication bus, and can cause applications to slow down. *Id.* at 15:8–21, 17:4–7. The '494 patent describes alleviating bottlenecks by allocating more current or frequency to the bottlenecked component and capping or limiting competing devices. This strikes a dynamic balance between devices so that a device that needs more resources for better overall performance is allocated extra resources, while other devices are reduced in performance to meet a given power limit. *Id.* at 7:51–61, 17:4–41.

E. Illustrative Claims

The Petition challenges claims 1–7, 13–15, 17, and 18, of which claims 1 and 4 are independent. Claim 1 is illustrative of the claimed subject matter and is reproduced below:[1]

1. A processor comprising:

1[a] an integrated circuit including:

1[b] a first core;

1[c] a cache memory;

1[d] a communication bus coupled to the first core, the communication bus to connect the first core and the cache memory;

1[e] a core workload monitor configured to determine a core workload for the first core;

[1] Paragraph labeling is based on labeling provided by Petitioner.

1[f] a bus workload monitor configured to determine a bus workload for the communication bus; and

1[g] balancing control adapted to receive the bus workload from the bus workload monitor and

to dynamically tune power allocation between the first core and the communication bus based on a power limit for the integrated circuit and

a comparison between the bus workload and a bus workload threshold, the power limit corresponding to a maximum thermal dissipation capacity for the integrated circuit,

1[h] wherein a power consumption of one of the first core and the communication bus is to be reduced, the power consumption reduction to be limited to maintain operation of the one of the first core and the communication bus above a low limit.

Ex. 1001, 21:17–39. Independent claim 4 recites a non-transitory storage medium and is directed to similar subject matter. *Id.* at 21:60–22:20.

F. References and Other Evidence

The Petition relies on the following references:

Name	Reference	Publication/Issue Date	Exhibit(s)
Bose	US 7,421,601 B2	Sept. 2, 2008	Ex. 1005
White	US 7,263,457 B2	Aug. 28, 2007	Ex. 1006
Anderson	US 8,601,300 B2	Dec. 3, 2012	Ex. 1007
Simeral	US 2009/0150689 A1	June 11, 2009	Ex. 1008
Naffziger	US 8,510,582 B2	Aug. 13, 2013	Ex. 1009

In addition, Petitioner submits the Declaration of David Wyatt. Ex. 1003 ("Wyatt Decl."). Patent Owner submits the Declaration of Michael C. Brogioli, Ph.D. Ex. 2001 ("Brogioli Decl."). The parties have also submitted deposition transcripts for Mr. Wyatt and Dr. Brogioli.[2]

G. Asserted Grounds of Unpatentability

Petitioner asserts the challenged claims are unpatentable on the following grounds:

Claims Challenged	35 U.S.C. §[3]	References
1	102/103	Bose
3, 14, 15	103	Bose, White, Simeral
2	103	Bose, Anderson
13	103	Bose, Anderson, Naffziger
4, 7	103	White
5, 6	103	White, Anderson
17-18	103	White, Anderson, Naffziger

[2] Ex. 1010 ("Brogioli Dep."); Ex. 2002 ("Wyatt Dep.").

[3] Because the earliest application from which the '494 patent claims priority was filed before March 16, 2013, the pre-AIA ("America Invents Act") versions of §§ 102 and 103 apply. Leahy-Smith America Invents Act ("AIA"), Pub. L. No. 112-29, 125 Stat. 284, 285–88 (2011).

Claims Challenged	35 U.S.C. §[3]	References
1, 3, 14, 15	103	White, Simeral
2	103	White, Simeral, Anderson
13	103	White, Simeral, Anderson, Naffziger

See Pet. 6–7.

H. Overview of the Prior Art

1. Bose (Ex. 1005)

Bose discloses a system and method for controlling power and performance in a microprocessor system that includes a monitoring and control system. Ex. 1005, Abstract, 1:17–22. The monitoring and control system maintains the maximum power of the chip or system within a programmable limit, maintains the peak temperature of the monitored regions of the chip or system below a specified limit, and targets a net throughput for maximization. *Id.* at 2:16–24, 4:19–29. An example of a monitoring and control system is shown in Figure 1 from Bose (reproduced below).

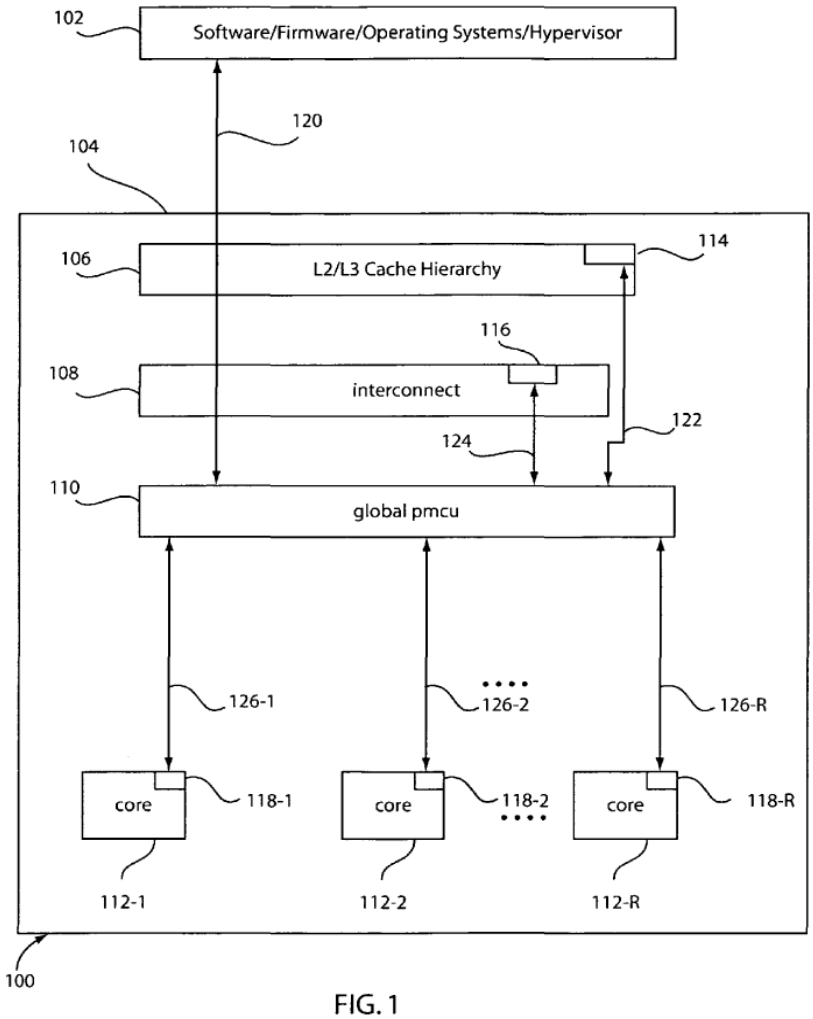

FIG. 1

Figure 1 "is a block diagram showing a hierarchical power-performance monitor and control unit (PMCU) integrated into a chip/system." Ex. 1005, 3:59–61. Figure 1 includes a monitoring and control system (100) with local components (114, 116, 118-1, 118-2, . . . 118-R) and global components (110) which monitor and control a multi-core chip (104). *Id.* at 5:61–67. The monitoring and control system is organized so that each core 112-1, 112–2, . . . 112–R or other element in the system is monitored using the local components, which report usage information (such as power usage and temperature usage) to a global monitoring and control unit that assesses the

information, determines a power mode, and chooses appropriate power optimizations for each core element. *Id.* at 6:56–7:17.

Bose discloses that "the performance of the chip or system may be targeted for maximization by one or more of the following: (a) use and deployment of one or more additional cores (that would otherwise be powered off or excluded from the design)" and "(b) at a given response point and given a choice of power mode allocations per core, an allocation is made such as to maximize the chip (or system)—level throughput performance." *Id.* at 12:21–29. The power modes are transmitted to each core such that their power levels are decreased or increased. *Id.* at 12:30–41.

2. White (Ex. 1006)

White discloses a processor or other integrated circuit with multiple logic cores that are configured to operate at independent frequencies and voltages and may be connected to other sub-systems, components, or peripherals external to the integrated circuit, such as memory or communications busses. Ex. 1006, 2:15–22, 2:45–67, 6:23–40. Figure 1 (reproduced below) depicts "a block diagram illustrating an integrated circuit including multiple logic cores configured to operate at independent voltages and/or frequencies." *Id.* at 5:18–31.

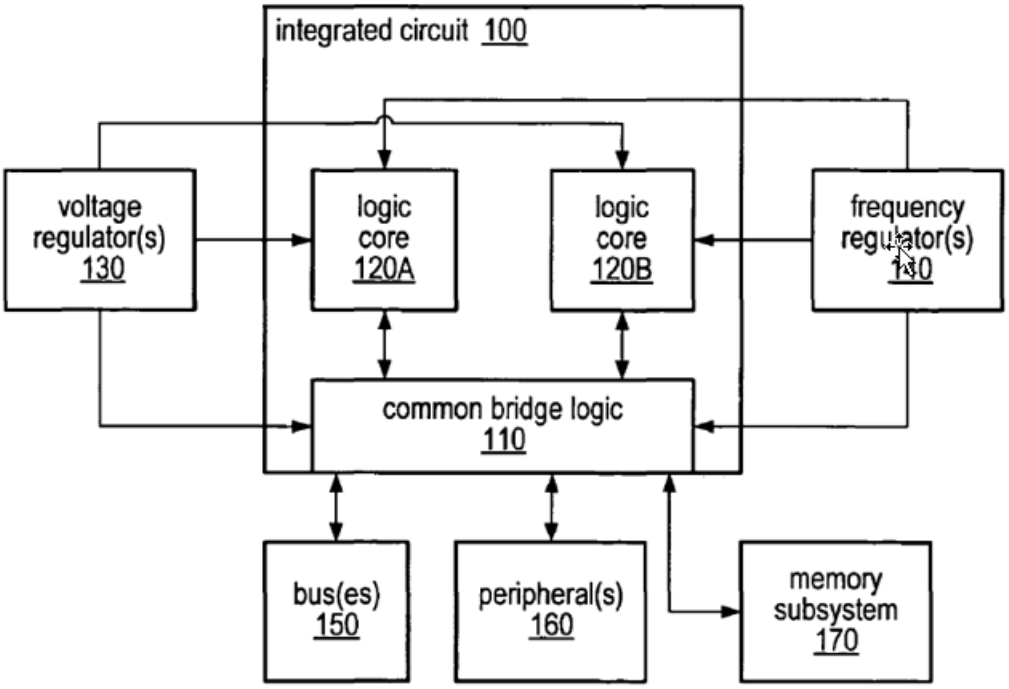

FIG. 1

Figure 1 depicts an integrated circuit (100) with two logic cores (120A, 120B), voltage regulators (130), frequency regulators (140), and common bridge logic (110) "configured to communicate with the logic cores as well as with other elements or peripherals either internal or external to integrated circuit 100, such as bus 150, peripheral 160 and/or memory subsystem 170." *Id.* at 6:41–7:7.

White explains that a system including an integrated circuit may also include power management logic that may be configured to control the operating characteristics, such as the operating voltage and/or operating frequency of the logic cores. *Id.* at Fig. 2A, 8:59–65. The processor's cores can be individually adjusted or adjusted as a group to operate at lower frequencies and/or voltages to save power or generate less heat to avoid an

unwanted shutdown. *Id.* at 2:22–44, 3:20–52. For example, if the system is running on battery power, power management logic can be configured to adjust the operating frequency and/or voltage of the logic cores to save power. *Id.* at 8:65–9:24.

In another example, temperature sensors measure the temperature of the integrated circuit, a region of the integrated circuit, or individual cores of the integrated circuit. *Id.* at Fig. 2B, 11:61–12:37. If the sensors detect that the temperature is too high, the operating frequency or the voltage of the components in the device may be decreased. *Id.* at 12:59–13:6. White also explains that the processor's cores can be adjusted to alleviate bottlenecks. *Id.* at 9:25–53. In such a case, the cores can be supplied with lower voltages and/or frequencies so the bottlenecked element can be supplied with a higher voltage and/or frequency. *Id.*

3. Anderson (Ex. 1007)

Anderson discloses a thermal power management system for a heterogeneous multi-core processor. Ex. 1007, Abstract. Anderson discloses chip 102 that includes applications central processing unit ("CPU") 110 with multiple CPU cores, such as core 0, core 1, and core N, each of which is a host processing core. *Id.* at 7:24–44, 9:66–10:7, Fig. 5A. Anderson also discloses that the same chip 102 comprises GPU cores, shown as graphics processors 135A-D. *Id.* at 10:30–57, Fig. 5A. Anderson further discloses that the CPU cores in a multicore processor "may implement message or instruction passing via network topologies such as bus, ring, mesh and crossbar topologies." *Id.* at 11:29–36, Fig. 5B.

4. Simeral (Ex. 1008)

Simeral discloses a data path controller, a computer device, an apparatus, and a method for integrating power management functions into a data path controller to manage power consumed by processors and peripheral devices. Ex. 1008, Abstract. The data path controller can manage power in different modes, which can be implemented separately or concurrently. *Id.* ¶ 20.

Simeral describes a mode in which the data path controller modifies operational characteristics of components to conserve power while providing sufficient resources to support a workload, and a mode in which the data path controller modifies operational characteristics of components as corrective action to bring one or more noncompliant activity levels back into compliance. *Id.* ¶¶ 20–21, 24. The modes may be operated according to different performance profiles that indicate priorities for various components of the system based on the use of the system. *Id.* ¶¶ 27–28. For example, if "the user desires a higher performing computing device over one that minimizes power consumption (e.g., higher operating speeds are preferred over extending battery life)," the performance profile may describe a range of frequencies and a range of voltages for operating the processor at high speeds, without necessarily conserving power. *Id.*

5. Naffziger (Ex. 1009)

Naffziger discloses a system and method for efficient power transfer on a die comprising two or more computation units (e.g., processors), using at least two different voltage regulators and a power manager. Ex. 1009, Abstract, 3:42–44. Naffziger explains that the activity levels of the

computation units can be measured and reported to the power manager, which uses the activity data to transfer power to or away from computation units to support the activity levels. *Id.* at 1:22–38, 1:66–2:29. Naffziger states that "[a]ny of a variety of techniques may be utilized to determine power consumption of a given computation unit," for example, by using thermal sensors or current sensors. *Id.* at 4:14–51.

Naffziger further explains that "[w]hen a given computation unit does not have a high or moderate workload, its activity level may decrease below a given threshold. Accordingly, its measured power usage value decreases." *Id.* at 5:28–31. Naffziger explains that "[t]he resulting reduced power usage value is conveyed to the power management unit." *Id.* at 5:31–32. Further, "[i]n response to the reduced power usage value, the power management unit . . . may redistribute the power credits of the die." *Id.* at 5:32–34. "For example, the power management unit . . . may lend power credits of a determined inactive computation unit to a computation unit that is determined to be highly active." *Id.* at 5:34–37.

II. ANALYSIS OF THE CHALLENGED CLAIMS

A. Level of Ordinary Skill in the Art

Petitioner contends a person of ordinary skill in the art of the '494 patent would have possessed "an undergraduate degree in electrical engineering, computer engineering, computer science, or similar disciplines, along with two years of professional experience working with the research, design and/or development of semiconductors, processors, power consumption and thermal power management, and related firmware and software or an equivalent level of skill, knowledge, and experience." Pet.

12–13 (citing Wyatt Decl. ¶ 21). Petitioner adds, "[t]he more education one has, the less experience needed to attain an ordinary level of skill. Similarly, more experience in the field may serve as a substitute for formal education." *Id.* at 13 (citations omitted).

As noted, Patent Owner expressly waived filing a preliminary response. Paper 9. At the institution stage, therefore, Patent Owner did not dispute Petitioner's description of a person of ordinary skill in the art or provide its own description. We regarded Petitioner's description as consistent with the prior art before us. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (prior art itself may reflect an appropriate level of skill). Thus, for the purpose of our Institution Decision, we adopted Petitioner's proposal. Institution Dec. 12–13.

In its Response, Patent Owner states that it "uses this definition" in its analysis. PO Resp. 15 (citing Brogioli Decl. ¶ 25). In view of the foregoing, for this Decision, we adopt the description of the person of ordinary skill articulated by Petitioner and used in our Institution Decision. In light of our review of the complete record, we find that this formulation is consistent with the '494 patent and the prior art of record, and is supported by the testimony of Mr. Wyatt. *See* Wyatt Decl. ¶ 21.

B. Claim Construction

We construe claim terms only as relevant to the parties' contentions and only to the extent necessary to resolve the issues in dispute. *See Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999); *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017).

Prior to institution, neither party proposed claim constructions for our consideration. Petitioner stated, "[u]nless indicated otherwise, all claim terms herein are given [their] ordinary and customary meaning." Pet. 12. Patent Owner filed no preliminary response, and thus did not dispute Petitioner's position or address claim construction. We determined that no claim terms needed to be construed at institution. Institution Dec. 13.

Post-institution, Patent Owner proposes a construction for the term "workload." PO Resp. 15–16. Patent Owner contends that "[a] person of ordinary skill in the art would understand that in the '494 patent, the term 'workload' means 'an amount of activity over a quantum or period of time.'" *Id.* at 15. Dr. Brogioli's testimony supports this construction, as does Mr. Wyatt's. Brogioli Decl. ¶¶ 36–38; Wyatt Dep. 34:14–36:9. The '494 patent also supports this construction. Ex. 1001, 8:20–22, 9:60–63. Petitioner does not dispute this proposed construction in its Reply. For the reasons given, we adopt Patent Owner's construction for "workload."

C. Anticipation and Obviousness

The Federal Circuit addressed the legal standard for anticipation in *Blue Calypso, LLC v. Groupon, Inc.*, 815 F.3d 1331 (Fed. Cir. 2016): "Under 35 U.S.C. § 102(b), a prior art reference will anticipate if it 'disclose[s] each and every element of the claimed invention . . . arranged or combined in the same way as in the claim.'" *Id.* at 1341 (citation omitted) (footnote omitted). The Federal Circuit went on to explain:

> However, a reference can anticipate a claim even if it 'd[oes] not expressly spell out' all the limitations arranged or combined as in the claim, if a person of skill in the art, reading the reference, would 'at once envisage' the claimed arrangement or combination.

Id. (quoting *Kennametal, Inc. v. Ingersoll Cutting Tool Co.*, 780 F.3d 1376, 1381 (Fed. Cir. 2015)).

A claim is unpatentable as obvious under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) where in evidence, so-called "secondary considerations," including commercial success, long-felt but unsolved needs, failure of others, and unexpected results. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). Neither party has presented any evidence on the fourth *Graham* factor.

D. Anticipation and Obviousness Challenges Based on Bose

1. Claim 1

Petitioner contends that independent claim 1 is anticipated by or would have been obvious in light of Bose. Pet. 15. Petitioner asserts that Bose teaches or suggests each limitation of claim 1 and provides an element-by-element analysis. *Id.* at 16–27; Wyatt Decl. ¶¶ 38–59. Patent Owner disagrees and contends Bose fails to disclose all limitations found in claim 1. *See* PO Resp. 19–33.

Upon consideration of Petitioner's explanations and supporting evidence in this record, and Patent Owner's arguments and supporting

evidence, we are not persuaded that Petitioner has demonstrated a by a preponderance of the evidence that Bose anticipates claim 1 or that claim 1 would have been obvious in light of Bose. Our reasoning follows.

Our analysis focuses on claim element 1[g], specifically "a comparison between the bus workload and a bus workload threshold." *See supra*, Section 1.E. The dispositive issue we discuss is whether Bose discloses the "comparison" as claimed. For context, however, we first review Petitioner's contentions as to other claim elements.

a. Claim Elements 1[a]-1[f] and 1[h]

Petitioner contends that the preamble[4] of claim 1 ("A processor comprising") is met by Bose's disclosure of a processor chip. Pet. 15–16 (citing Ex. 1005, Fig. 1).

Petitioner contends that element 1[a] ("an integrated circuit") is met by Bose's disclosure of microprocessor processor system 100 including multi-core chip 104. *Id.* at 16–17 (citing Ex. 1005, Fig. 1).

Petitioner asserts that element 1[b] ("a first core") is met by Bose's disclosure that multi-core chip 104 includes core 112-1. *Id.* at 17–18 (citing Ex. 1005, Fig. 1).

Petitioner contends that element 1[c] ("a cache memory") is met by Bose's disclosure that "multicore chip 104 includes an 'L2/L3 cache hierarchy' 106, which is a multi-level cache system including L2 and L3 cache memories." *Id.* at 18–19.

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[4] We do not express opinions as to whether the claim 1 or claim 4 preambles are limiting.

Petitioner contends that element 1[d] ("a communication bus . . . ") is met by Bose's disclosure that multi-core chip 104 includes interconnect 108. *Id.* at 19–20. Petitioner explains that "[i]nterconnect 108, first core 112-1 and L2/L3 cache hierarchy 106 are all 'core element[s]' within multi-core chip 104 that share an overall power budget and are subject to the same power management and control system." *Id.* at 19 (citing Ex. 1005, 5:64–67, 7:4–28) (second alteration in original). Petitioner concludes that "[b]ecause these components are interconnected in the power domain and are capable of simultaneous multithreading, a [person of ordinary skill] would have understood that the elements shown in Fig. 1 [of Bose] represents [sic] a physically interconnected system where interconnect 108 connects at least one core and the cache memories and performs the same interconnecting function as the 'communication bus' in the '494 [patent]." *Id.* at 20 (citing Ex. 1001, 15:38–39).

Petitioner contends that element 1[e] ("a core workload monitor . . .") is met by Bose's disclosure that microprocessor system 100 includes local PMCU 118-1 associated with core 112-1. *Id.* at 21–22 (citing Ex. 1005, Fig. 1). Petitioner explains, "local PMCU 118-1 is a core workload monitor as it monitors performance statistics reflecting workload of core 112-1." *Id.* (citing Wyatt Decl. ¶ 46).

Petitioner contends that element 1[f] ("a bus workload monitor . . .") is met by Bose's disclosure of local PMCU 116 associated with interconnect 108. *Id.* at 22–23. Petitioner explains that "[l]ocal PMCU 116 performs the same functions as local PMCU 118-1 (i.e., the core workload monitor)." *Id.* at 23 (citing Wyatt Decl. ¶¶ 48–49).

Element 1[h] calls for limiting the power consumption reduction "to maintain operation of the one of the first core and the communication bus above a low limit." Petitioner contends "Bose discloses that global PMCU selects and adjusts power mode for core 112-1 and interconnect 108." *Id.* at 27. Further, "Bose discloses operations of components will be maintained over a low limit of being powered off." *Id.* (citing Wyatt Decl. ¶¶ 58–59).

b. Claim element 1[g]

Petitioner contends that Bose meets claim element 1[g] ("balancing control adapted . . ."). Pet. 23–26. Referring to Figure 1 of Bose, Petitioner asserts that Bose discloses that chip-level global PMCU 110 functions as "balancing control." *Id.* at 23–24. Petitioner explains that PMCU 110 "receives the bus workload from local PMCU 116 ('bus workload monitor'), as PMCU 116 reports 'a summary of monitored results,' (i.e., workload of interconnect 118), upwards to global PMCU 110 ('balancing control')." *Id.* at 24 (citing Ex. 1005, 6:18–34). Petitioner further contends that Bose teaches dynamic tuning of power allocation by the balancing control as recited in element 1[g]. *Id.* at 24–25. Petitioner explains that "[g]lobal PMCU 110 'dynamically manage[s] chip power between the components . . . to meet the power limit with the expectation of increased system performance.'" *Id.* (second and third alterations in original).

Petitioner contends also that Bose discloses the claimed "comparison between the bus workload and [a] bus workload threshold." *Id.* at 25–26. As Petitioner explains, "a [person of ordinary skill in the art] would have understood that in Bose, selecting or adjusting power mode for a component entails comparing a workload threshold, such as predicted power and

performance associated with each power mode with real time statistics, such as the monitored workload of a component." *Id.* at 26 (citing Wyatt Decl. ¶¶ 55–56).

Patent Owner disputes Petitioner's argument that Bose meets this limitation. PO Resp. 23–33. Patent Owner observes that "[t]he petition makes no distinctions between its allegations of anticipation or obviousness of claim 1 with respect to Bose." *Id.* at 28. Relying on the testimony of Dr. Brogioli, Patent Owner asserts that "the claimed invention does not resemble the hierarchical and distributed control system described by Bose." *Id.* at 29 (citing Brogioli Decl. ¶¶ 51–52). Dr. Brogioli testifies that "[a person of ordinary skill] would recognize that Bose describes power allocation using a hierarchical control system." Brogioli Decl. ¶ 51 (citing Ex. 1005, 2:25). He continues, "[e]ach layer of the hierarchy has its own control." *Id.* (citing Ex. 1005, 2:25–35). He testifies further that "[t]his is in contrast to the control described in the '494 patent. In the '494 patent, a single power control module 'is able to balance and allocate power/frequency between devices of [the integrated circuit] to achieve maximum performance, even when [the integrated circuit] is under a power limit.'" *Id.* ¶ 52 (quoting Ex. 1001, 7:40–44) (alterations in original).

Specifically addressing the requirement of claim 1 for a "comparison between the bus workload and a bus workload threshold," Dr. Brogioli testifies that "Bose's system operates so as to make it unnecessary to perform any *comparisons* of bus workload to a bus workload threshold." *Id.* ¶ 55. He explains that in Bose, "[b]y providing a power-performance trade-off table with information concerning actual power level decreases or

increases for different power modes, no such comparison is needed." *Id.* (citing Ex. 1005, 2:62–65).

Petitioner responds that in Bose "the global PMCU adjusts the power mode of a component based on real time statistics stored in the Phase History Table 213 (i.e., the monitored power and performance levels) and the predicted power and performance for each power mode stored in the Power/Performance Trade-off Table 206 (*i.e.*, the 'workload threshold')." Pet. Reply 4. Petitioner continues, "[b]y comparing the monitored power and performance level (i.e., 'workload') with the predicted power and performance level (i.e., 'workload threshold'), the global PMCU determines whether the power budget assigned to the component is sufficient and assigns a power mode accordingly." *Id.*

This claim limitation was explored with Petitioner's counsel during the oral argument. *See*, *e.g.*, Hearing Tr. 12:14–17:20. Petitioner's counsel was asked to identify where in Bose the recited "comparison" is disclosed. *See id.* at 14:15–16. Counsel referred the panel to Figure 3 of Bose, reproduced below. *Id.* at 15:4–15.

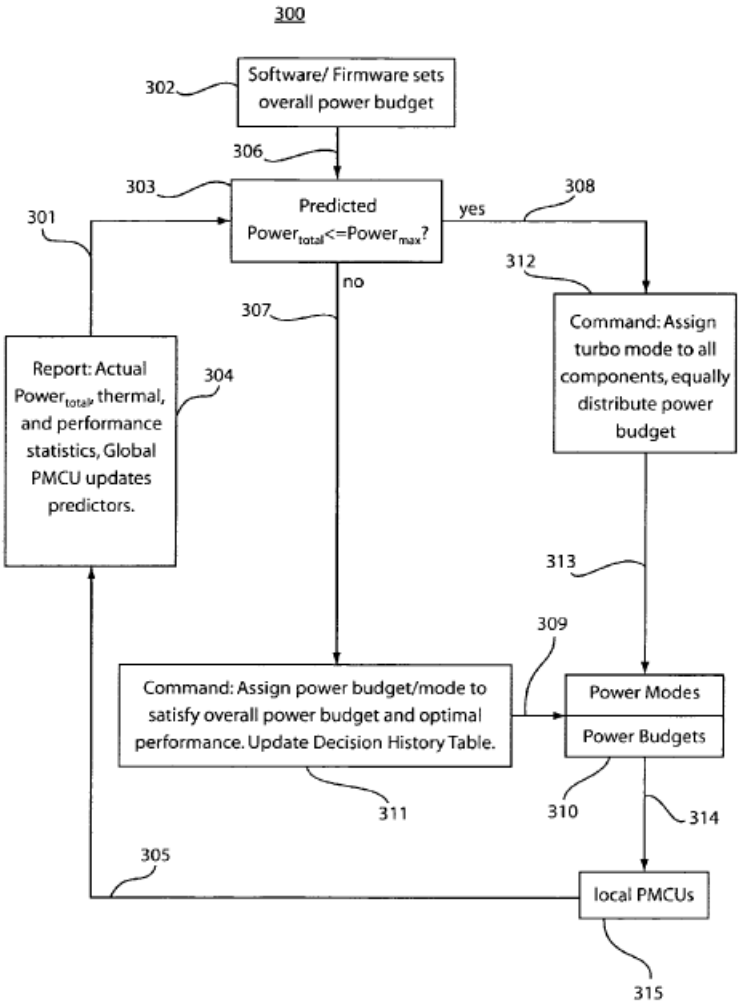

FIG. 3

Figure 3 of Bose "is a block/flow diagram showing a global power performance monitor and control unit (PMCU) loop for monitoring and controlling system power and performance." Ex. 1005, 3:65–67. Asked to identify where the "comparison" recited in claim 1 is shown in Figure 3, Petitioner's counsel referred specifically to step 311 in the above flow diagram:

> [COUNSEL:] So that comparison would be taking place as it's doing, you know, *when it's into the state 311, that's what*

> *it's going through*. So and it's this is continuing. Oh, it says here like we see here at the actual power is not below or equal to, there's this loop.

Hearing Tr. 15:4–7 (emphasis added). When asked by the panel to further identify where in step 311 the "comparison" is shown, Petitioner's counsel responded as follows:

> [THE BOARD:] So Counsel, based on your answer, does Figure 3 not have the comparison part of the limitation shown?
>
> [COUNSEL]: Well as shown? *No, it doesn't*, the one thing is *Bose doesn't use the work [sic: word] compare* here, but we do see in the figure where checking predicted power in Step 303, you know, we are checking predicted against the actual.
>
> . . . .
>
> [THE BOARD]: So just to put a fine point on it, . . . 303 is not the comparison that you're relying on. The comparison that you're relying on *takes place in Box 311*, Figure 3. Is that right?
>
> [COUNSEL] That's what we're showing here.

Hearing Tr. 17:2–20 (emphases added).

Patent Owner's counsel responded to this discussion, referring to step 303 in Figure 3: "There's a comparison, but it's a power comparison." Hearing Tr. 30:17–20. We agree with Patent Owner that the figure cited by Petitioner does not show or suggest a comparison as claimed. Petitioner's suggestion that such a comparison would have been obvious is not supported by the evidentiary record. We find that the only comparison discernable from Bose's Figure 3 is the comparison of $\text{Power}_{\text{Total}}$ to $\text{Power}_{\text{Max}}$ in step 303. Petitioner's counsel specifically stated at the hearing that Petitioner does not rely on this step to meet the comparison recited in claim element 1[h]. Hearing Tr. 17:16–20.

Step 311, in contrast to showing a comparison, refers to assigning the "power budget/mode to satisfy overall power budget and optimal performance," and updating the Decision History Table. Ex. 1005, Fig. 3 (311). We find no mention or suggestion there of a workload comparison as claimed.

In addition to Figure 3 itself, Petitioner relies on the description of Figure 3 in Bose's specification. *See* Hearing Tr. 46:2–18 (citing Bose, Ex. 1005, 9:14–30). The text from Bose cited by Petitioner at the hearing includes the following:

> From state 303, if the actual total power is not below or equal to the total power budget, the loop transitions through edge 307 into state 311, and the state 311 assigns power budget and power mode with consideration of: the commands from OS 120 (stored, e.g., in Control Registers 201 and total power budget from the Total Power Budget Registers 212, both depicted in FIG. 2), the real time statistics (stored e.g., in the Phase History Table 213 depicted in FIG. 2) and the power/performance trade-off of each mode for each thread in each core (stored, e.g., in the Power/Performance Trade-off Table 206, depicted in FIG. 2).

Ex. 1005, 9:14–24. From this citation to Bose, Petitioner argues that the assignment of a power mode in Step 311 "is done with a consideration of numerous things," and to take them into account, "[y]ou first have to do these comparisons including of the real time statistics of the monitored workload and those predicted power and performance statistics there." Hearing Tr. 46:16–18. Petitioner makes a similar argument in its Reply. *See* Pet. Reply 3–5. We are not persuaded by these arguments. As Patent Owner's counsel pointed out at the hearing, "Counsel [for Petitioner] wants to read the statement in Column 9 between lines 14 and 30 of Bose as

consideration must mean comparison. Where does the [Bose] Patent say that? Answer, it doesn't." Hearing Tr. 48:4–7.

Nowhere does Petitioner or its expert point to an explicit disclosure in Bose of making a comparison of the claimed "bus workload and a bus workload threshold." Instead, Petitioner relies on its expert's opinion as to what a person of ordinary skill might have known, without any additional supporting evidence. *See*, *e.g.*, Pet. 26 ("[A person of ordinary skill] would have understood global PMCU compares a workload threshold as exemplified by the predicted power and performance of each power mode and the monitored workload to select and adjust the power mode of a component" (citing Wyatt Decl. ¶¶ 54–55)). This opinion is not supported by the record. The only disclosure of a comparison in Bose that we have been shown is the comparison of $Power_{Total}$ to $Power_{Max}$ in step 303 of Figure 3, which Petitioner does not rely on to meet the "comparison" limitation in the claim. Hearing Tr. 17:16–20. Also without proper support is Petitioner's assertion that "a [person of ordinary skill] would have understood that in Bose, selecting or adjusting power mode for a component entails comparing a workload threshold, such as predicted power and performance associated with each power mode with real time statistics, such as the monitored workload of a component." Pet. 26 (citing Wyatt Decl. ¶¶ 55–56).

We determine that for the reasons given, Petitioner fails to demonstrate by a preponderance of the evidence that the claimed comparison element 1[g] of claim 1 is taught or suggested by Bose. We find, therefore, that Petitioner has not demonstrated that claim 1 is

anticipated by Bose, nor has Petitioner demonstrated that to a person of ordinary skill, claim 1 would have been obvious in light of Bose.

2. Claims 2, 3, and 13–15

Petitioner asserts claims 2 and 13 would have been obvious over Bose and Anderson (claim 2) or over those references further in view of Naffziger (claim 13). Pet. 39–50; Wyatt Decl. ¶¶ 80–97. Similarly, Petitioner asserts dependent claims 3, 14, and 15 would have been obvious over Bose, White, and Simeral. Pet. 27–39; Wyatt Decl. ¶¶ 60–79.

For these dependent claims, both parties rely on their arguments for claim 1. Patent Owner argues that "in each of these assertions, the petition relies on its analysis of the teachings of Bose with respect to claim 1 insofar as those elements of the various dependent claims are concerned." PO Resp. 33. Patent Owner therefore relies on its analysis of claim 1, discussed *supra*. *Id.* at 34 ("Each respective dependent claim is not unpatentable in view of the cited references for at least the same reasons as independent claim 1 is not unpatentable in view of Bose."). Petitioner responds: "Because Patent Owner's arguments regarding Bose with respect to claim 1 fail, its arguments regarding dependent claims 2-3, and 13-15 also fail." Pet. Reply 9.

We find for the reasons given for claim 1 that Petitioner fails to prove by a preponderance of the evidence that claims 2 and 13 would have been obvious over Bose, Anderson, and Naffziger or that claims 3, 14, and 15 would have been obvious over Bose, White, and Simeral.

3. Summary

For the reasons given, Petitioner has failed to demonstrate by a preponderance of the evidence that (1) claim 1 is anticipated by or would have been obvious over Bose; or (2) claims 2, 3, and 13–15 would have been obvious over Bose combined with the other references identified in these challenges.

b. Obviousness Challenges Based on White

1. Claims 4 and 7

As noted, independent claim 4 is directed to a "non-transitory storage medium" and recites many elements similar to those in independent claim 1. Ex. 1001, 21:60–22:20. Petitioner asserts that White teaches each limitation of claim 4. Pet. 50–59; Wyatt Decl. ¶¶ 98–112. For example, claim element 4[a] recites "receiving a bus workload for a communication bus and a first processing element workload for a first processing element based on an integrated circuit reaching a limit." Ex. 1001, 21:63–65. Referring to Figure 1 of White, reproduced *supra*, Petitioner identifies logic core 102A as the claimed "first processing element" and common bridge logic 110 as the claimed "communication bus." Pet. 51–52. Petitioner further contends that White discloses power management logic 200 that "receives workloads for common bridge logic 110 and logic core 120A, such as their operating voltages and frequencies" and is "configured to monitor and adjust the operating frequency and/or voltage of various portions of the integrated circuit 100, such as the logic cores 120 and common bridge logic 110." *Id.* at 53 (emphasis omitted). Petitioner further asserts, "White also discloses that power management unit 200 receives operating voltages/frequencies

based on the integrated circuit reaching a limit." *Id.* (citing Wyatt Decl. ¶ 104).

Patent Owner's arguments opposing this challenge focus on claim element 4[a]. PO Resp. 46–52. Patent Owner refers to its proposed construction for "workload" (adopted by us *supra*, in Section II.B) and contends that "White is clear that what is 'received' by power management logic is not workload – i.e., not activity levels. Instead, what is received by the power management logic is current operating voltages and operating frequencies." *Id.* at 48.

We agree with Patent Owner and find that there is a distinction between White's operating voltages and frequencies and the claimed workload, which we have construed in Section II.B as "an amount of activity over a quantum or period of time." Our reasoning follows.

We find that in contrast to workload, the current voltages and frequencies received by the power management logic in White are operating conditions that do not reflect the "amount of activity over a period of time." *See* Brogioli Decl. ¶¶ 64–66. Dr. Brogioli explains that "[a]ccording to White, the power management logic 200 controls the operating characteristics, such as operating voltage and/or operating frequency, of the logic cores." *Id.* ¶ 64 (citing Ex. 1006, 8:61–65, 9:2–6). He explains further that "[m]onitoring operating characteristics as described by White is not the same as monitoring workload using a core workload monitor, as recited in claim 1 of the '494 patent." *Id.* ¶ 66. He explains also that "[t]he '494 patent itself explains that performance metrics, such as frequency, can be altered independently of workload." *Id.* (citing Ex. 1001, 12:61–65).

Still further, "[b]y controlling the parameters under which a workload has to be processed, one can maintain operation of the core within desired boundaries." *Id.* He contrasts this with workload, which "is a function of the demands imposed by, e.g., applications running on the system, and may or may not be subject to direct control, whereas the conditions under which that workload is processed are controlled directly." *Id.*

Petitioner responds that "nothing in the '494 Patent indicates that determining a 'workload' cannot be done by monitoring operating frequencies and voltages, which provide indications of activity or use of a processing element." Pet. Reply 10. Petitioner quotes the '494 patent for support: "Determining a workload includes any known method for determining activity of hardware, a workload of software, a number of instructions executed or to execute, or any other metric for determining use of a processing element." *Id.* (emphasis omitted) (*see* Ex. 1001, 9:49–52; *see also id.* at 16:19–23). Patent Owner responds that "[y]es, the '494 patent states that many methods can be employed to monitor workload, and yes, the '494 patent states that if a GPU's frequency is below a threshold that frequency can be increased." PO Sur-reply 7 (citations omitted). Patent Owner continues, "[b]ut this is not an indication that monitoring frequency is determining workload." *Id.*

This subject was discussed at the oral argument. *See,* e.g., Hearing Tr. 21:13–23:11, 35:3–36:10, 37:20–38:13. At the hearing, to describe White's use of frequency and voltage adjustments, in an exchange with Petitioner's counsel, the Board drew an analogy to operating a lawnmower:

> [THE BOARD]: Well, Counsel, I guess to use an analogy, say I have a lawnmower and I have it at some throttle

> setting and I'm listening to it and I go to a thick patch of grass and I hear the engine bogging so I have to increase the throttle. Now it sounds to me like in this example, the workload is, you know, the RPMs of the engine and the throttle is what I'm controlling in order to manage my workload and it seems to me in the claims, the frequency and voltage, which are the drivers of the power, is what you're setting, but you need to know how to set it by monitoring something other than that.
>
> . . . .
>
> [COUNSEL]: Yes, so it's looking at both. And I think that's important. You know, in your situation where we have the throttle, that throttle is set at one level and that's it. Here we're looking at both operating frequency and voltage.

Hearing Tr. 22:20–23:11. Later on in the argument, Patent Owner's counsel compared adjusting of frequency to meet the workload in White to the "levers" in the lawnmower analogy previously discussed. *Id.* at 38:5–13. Addressing the discussion of adjusting frequency at column 10, line 65 to col 11, line 2, of the '494 patent, Patent Owner's counsel observed:

> [COUNSEL:] And I think that's in line with your lawn mower analogy. *This is one of the levers that can be used in order to meet the requirement*. But it's not saying, you know, I compare frequency. I mean, it's not speaking to the limitation in the claim about comparing the workload to the workload threshold.

Hearing Tr. 38:9–13 (emphasis added).

We are persuaded and find for the reasons given that Petitioner fails to prove by a preponderance of the evidence that White teaches or suggests "receiving a bus workload for a communication bus and a first processing element workload for a first processing element based on an integrated circuit reaching a limit." Patent Owner's expert Dr. Brogioli testifies that "[t]he workload is a function of the demands imposed by, e.g., applications

running on the system, and may or may not be subject to direct control, whereas the conditions under which that workload is processed are controlled directly." Brogioli Decl. ¶ 66. We agree with Dr. Brogioli and find that White's frequency and voltage monitoring and adjustments do not result in the power management logic receiving the bus workload as recited in claim element 4[a]. *Id.* ¶¶ 64–66.

We find the testimony of Mr. Wyatt on this issue unconvincing. Wyatt Decl. ¶ 103. In support of his opinion that "monitoring the operating voltages and frequencies of the logic core 120A and common logic bridge 110 is monitoring the workload of those components," he states: "It was well understood that operating frequency and voltage of a component reflect the activity and use, or workload, of that component." *Id.* However, he does not provide any evidentiary support for this statement. We, therefore, give it little weight. *See* PTAB Consolidated Trial Practice Guide 40 (Nov. 2019)[5] ("Opinions expressed without disclosing the underlying facts or data may be given little or no weight.") (citing *Rohm & Haas Co. v. Brotech Corp.*, 127 F.3d 1089, 1092 (Fed. Cir. 1997)).

Petitioner asserts also that claim 7 would have been obvious in view of White. Pet. 59. Claim 7 depends from claim 4, and therefore includes the limitation "receiving a bus workload for a communication bus . . ." we determine is not taught or suggested by White. Accordingly, we determine that Petitioner has not proven that claim 7 is unpatentable for the reasons given for claim 4.

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[5] *Available at* https://www.uspto.gov/TrialPracticeGuideConsolidated.

2. Claims 5, 6, 17, and 18

Petitioner asserts that claims 5 and 6 (depending from claim 4) would have been obvious over White and Anderson. Pet. 60–64; Wyatt Decl. ¶¶ 114–123. Petitioner asserts also that claims 17 and 18 (also depending from claim 4) would have been obvious over White, Anderson, and Naffziger. Pet. 64–66; Wyatt Decl. ¶¶ 124–127. For these dependent claims, both parties rely on their arguments for claim 4. PO Resp. 52–53; Pet. Reply 15. We find that for the reasons given for claim 4, Petitioner has failed to demonstrate by a preponderance of the evidence that these claims are unpatentable.

3. Claims 1–3 and 13–15

Petitioner asserts that claims 1, 3, 14, and 15 would have been obvious over White and Simeral and claims 2 and 13 would have been obvious over those references with the addition of Anderson (claim 2) or Anderson and Naffziger (claim 13). Pet. 66–84; Wyatt Decl. ¶¶ 128–150.

Patent Owner's response for claim 1 focuses on claim element 1[e] ("a core workload monitor configured to determine a core workload for the first core"). PO Resp. 42. Patent Owner's arguments mirror those for claim 4, discussed *supra*, in Section II.D.1. Thus, Patent Owner contends "[t]he petition alleges that in a White-Simeral combination, it is White that discloses a core workload monitor configured to determine a core workload for the first core, as recited in claim 1." *Id.* (citing Pet. 72). Patent Owner contends that "[i]n White, power management logic 200 controls operating characteristics of cores of an integrated circuit, such as operating voltage and/or operating frequency." *Id.* (citing Ex. 1006, 8:61–65, 9:3–6). Dr.

Brogioli testifies: "Monitoring operating characteristics as described by White is not the same as monitoring workload using a core workload monitor, as recited in claim 1 of the '494 patent, and a [person of ordinary skill] would not conflate the two." Brogioli Decl. ¶ 66. He continues, "[t]he '494 patent itself explains that performance metrics, such as frequency, can be altered independently of workload." *Id.* (citing Ex. 1001, 12:61–65). For the reasons given immediately above and in Section II.D.1, we find that White does not teach or suggest "a core workload monitor configured to determine a core workload for the first core" recited in claim element 1[e].

For the challenges to claims 2, 3, and 13–15, both parties rely on their arguments for claim 1. PO Resp. 45; Pet. Reply 11. We find that for the reasons given for claim 1, Petitioner has failed to demonstrate that these claims are unpatentable.

4. Summary

For the reasons given, Petitioner has not demonstrated by a preponderance of the evidence that claims 1–7, 13–15, 17, and 18 would have been obvious over White (claims 4, 7), White and Anderson (claims 5, 6), White, Anderson, and Naffziger (claims 17, 18), White and Simeral (claims 1, 3, 14, 15), White, Simeral, and Anderson (claim 2), or White, Simeral, Anderson, and Naffziger (claim 13).

III. CONCLUSION

For the foregoing reasons, we determine that Petitioner has not proven by a preponderance of the evidence that claims 1–7, 13–15, 17, and 18 of the '494 patent are unpatentable. In summary:

Claim(s)	35 U.S.C. §	Reference(s)/Basis	Claim(s) Shown Unpatentable	Claim(s) Not Shown Unpatentable
1	102	Bose		1
1	103	Bose		1
3, 14, 15	103	Bose, White, Simeral		3, 14, 15
2	103	Bose, Anderson		2
13	103	Bose, Anderson, Naffziger		13
4, 7	103	White		4, 7
5, 6	103	White, Anderson		5, 6
17, 18	103	White, Anderson, Naffziger		17, 18
1, 3, 14, 15	103	White, Simeral		1, 3, 14, 15
2	103	White, Simeral, Anderson		2
13	103	White, Simeral, Anderson, Naffziger		13
Overall Outcome				1–7, 13–15, 17, 18

IV. ORDER

For the foregoing reasons, it is

ORDERED that Petitioner has not demonstrated by a preponderance of the evidence that claims 1–7, 13–15, 17, or 18 of the '494 patent are unpatentable;

FURTHER ORDERED that that because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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