A 0.13μm CMOS Platform with Cu/ Low-k Interconnects for System On Chip Applications

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Abstract

We describe an advanced 0.13μm CMOS technology platform optimized for density, performance, low power and analog/mixed signal applications. Up to 8 levels of Copper interconnect with industries first true low-k dielectric (SiLK, k=2.7) [1] result in superior interconnect performance at aggressive pitches. A 2.28μm^2 SRAM cell is manufactured with high yield by introducing elongated local interconnects on the contact level without increasing process complexity. Trench based embedded DRAM is offered for large area memory. Modular analog devices as well as passive components like resistors, MIM capacitors and intrinsic inductors are integrated.

Process Flow/ Device Portfolio

The process architecture is based on a standard CMOS process flow with STI, retrograde wells with In/Sb channels, dual workfunction Co-silicided gates, strong halo implants, Nitride spacers, W-contacts and Copper metallization with low-k dielectric [2]. Key ground-rules with minimum pitches of 0.32μm are shown in Table 1.

SOC technologies need to accommodate a wide range of device options integrated on a single chip. A modular triple gate oxide process allows optimization of high performance devices with low active power (18Å), devices with low gate leakage (22Å) and of I/O devices (52Å) independently. All devices are derived from the standard V_t logic transistor pair (1.2V, 22Å gate oxide, RO delay=18.5ps, I_{off}<0.2nA/μm) that is used in core library books (Fig. 1). By adding optional masks Low V_t (RO delay=14ps@1.2V) and High V_t (Ioff< 10pA/μm) devices are integrated to balance performance and off-state leakage current. Higher performance can be achieved at 1.5V operation with 22 Å devices. All devices fulfill the reliability specifications up to 1.6V supply voltage. Two different thick-oxide devices are offered in the platform: A high speed 2.5V I/O device is obtained by modifying the extension/halo implants. Analog devices with low back-bias sensitivity and improved Early-Voltage are implemented and can also be used for 3.3V I/O applications. An overview about the various devices is given in Table 2.

Copper Interconnect with low-k dielectric

The process platform offers the first true low-k dielectric/Copper metallization (Fig. 2) with up to 8 levels of interconnect at dense pitches (M1: 0.32μm, Mx: 0.40μm). A spin-on low-k dielectric has been chosen as dielectric. The main challenges of mechanical stability and robustness with SiLK have been addressed. Reliability investigations show comparable electromigration data for SiLK relative to Oxide (Fig. 3): Careful selection of liner materials is necessary to provide good yield and reliability. The low-k dielectric provides up to 30% performance advantage compared to oxide based BEOL solutions: Fig. 4 shows simulated performance for a critical path of a synthesized DSP core. A speed increase from 153 Mhz (oxide) to 189 MHz can be achieved with low-k dielectric at 1.2V operation without special optimization of circuit for low-k.

Further challenges of the integration of low-k dielectric into BEOL have been addressed in the following areas:

- Optimizing the passivation stack to obtain good mechanical stability for wirebond.
- Dummy structures under bond pads to improve mechanical support.
- Naked Al fuses to allow fuse blow without damaging the low-k dielectric and without opening paths for oxygen and moisture ingress.

Thicker metal at 2x pitches is offered on upper levels to minimize resistance for long interconnect wires.

Functionality of a complex 8Mb SRAM product has been demonstrated in this 0.13μm technology platform (Fig. 5).

Lithography optimization

A 248nm lithography solution was developed for all critical levels by use of enhancement techniques including off-axis illumination, OPC, assist features, phase-shift masks with future migration to 193nm in manufacturing. A significant reduction of across-chip-linewidth-variation (ACLV 3sigma<10nm) on the gate level has been achieved by applying sub-resolution assist features (Fig. 6). OPC strategy (Table 3) is centered on a rule-based approach including serifs and flexible hammerheads at line ends. On the contact level OPC is applied in this technology to allow printing of contacts at very tight pitches (0.36μm) without sidelobes. Special optimization has been performed on the isolation level. By using a hardmask process and thinning the resist, a chrome-on-glass mask can be used to reduce cycle time from tapeout to first mask delivery.

Embedded memory

The technology offers 2.48μm^2 [2] and 2.28μm^2 SRAM cells (Fig. 7). The smaller cell size can be obtained by using elongated bar features on the contact level as local interconnect. Yield equivalency is shown in Fig. 8. OPC optimization of the contact layer (Fig. 9) and adjusting contact etch and liner optimization were crucial to achieve high yield. A trench-based embedded DRAM architecture with a cell size of 0.31 μm^2 was integrated into the process flow. The modular approach results in identical device performance in the logic part.

Mixed Signal/Analog/RF Elements

Compared to the 0.18μm generation [3] the optional MIM Capacitor was moved up into the passivation layer to decouple the processing of the MIM stack from low-k integration (Fig. 10). A Si-oxide based dielectric material (35nm) was selected to support area capacitance of 1fF/μm^2 without sacrificing reliability (Fig. 11). Various high precision resistors with sheet resistances between 75 Ohm/square and 1000 Ohm/square are formed with a salicide blocking mask. Intrinsic inductors are defined by the standard metallization options without adding any cost. By optimizing the designs a Q value of 4-6 can be achieved with 2 thin wire levels, higher Q>10 with thick wire on 2 last metal levels (Fig. 12). RF devices with cutoff frequency Ft of 100 GHz and noise figures NF_{min} of 0.7 dB, (Fig. 13, 14) are offered for RF CMOS circuits in wireless applications.

Conclusion

A modular process architecture has been presented for 0.13μm SOC applications. A modular device portfolio derived from a triple-gate-oxide process with up to 8 levels of Copper wiring with low-k dielectrics combined with analog features and dense embedded memories allows SOC to become mainstream.

Acknowledgment

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(1) R. D. Goldblatt et al.: *A High Performance 0.13 μm Copper BEOL Technology with Low-k Dielectric*, IITC 2000

(2) L.K. Han et al: *A Modular 0.13μm BULK CMOS Technology for High performance and Low Power Applications*, VLSI 2000, p. 12

(3) M. Armacost et al: *A High Reliability Metal Insulator Metal Capacitor for 0.18 μm Copper Technology*, IEDM 2000, p. 157

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Layer	Line (μm)	Space (μm)	Pitch (μm)
Isolation	0.16	0.18	0.34
N+/p+		0.64	
Gate	0.12	0.22	0.32
Contact	0.16	0.24 /0.20	0.40/0.36
M1	0.16	0.16	0.32
Via	0.20	0.20	0.40
Mx	0.20	0.20	0.40
Via last	0.40	0.40	0.80
M last	0.40	0.40	0.80

Table 1: Key ground rules of 0.13um technology

Device	Standard	HighVt	LowVt	High performance	I/O	Analog	
Vdd (V)	1.2	1.2	1.2	1.2	2.5	3.3	2.5
Tox (A)	22	22	22	18	52	52	
Ion (n/p) (μA/μm)	500/210	270/150	630/270	810/365	610/275	770/348	550/221
Ioff (n/p) (nA/μm)	0.2/0.2	0.01/0.01	2/2	30/30	0.01/0.01	0.02/0.02	0.02/0.02
RO delay (ps)	18.5	29	14	10	32	41	47

Table 2: Modular device portfolio of 0.13um technology platform

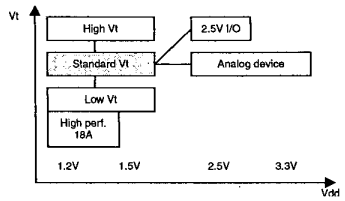

Fig. 1: Modular device portfolio of 0.13μm technology platform

Level	Rule based proximity correction	Line end extensions	Mask
Isolation	Nested-isolated correction	anchors	COG
Gate	Nested-isolated correction	Flexible hammerheads dependent on 2D environment	PSM + Assist features
Contact	OPC for dense contacts		PSM
M1	Nested-isolated correction	Flexible hammerheads dependent on 2D environment	PSM

Table 3: OPC strategy for critical levels

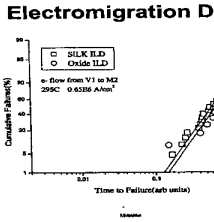

Fig. 3: Comparision of electromigration between SiLK and Oxide ILD

BEOL Materials	SiLK	Oxide
DSP Core speed (1.2V)	189MHz	153MHz
DSP Core speed (1.5V)	252Mhz	189Mhz

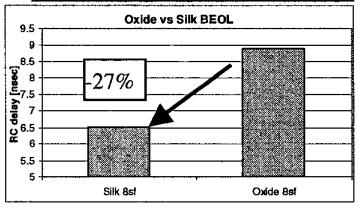

Fig.4: Performance Comparison between SiLK and Oxide ILD (simulation)

Fig. 2: SEM Cross-section

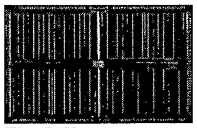

Fig. 5: Top down view of 8Mb SRAM chip

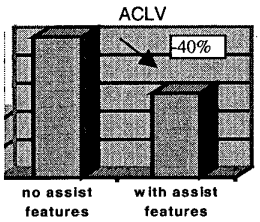

Fig. 6: Across-chip-linewidth-variation on gate level with and without sub-resolution assist features

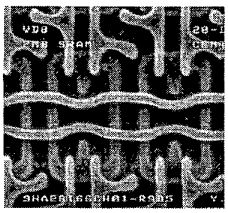

Fig. 7: 2.28μm2 SRAM cell / Top-down view of gate and isolation level

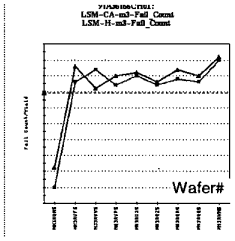

Fig. 8: SRAM yield comparision between 2.48μm2 and 2.28μm2 (with elongated contacts) cells

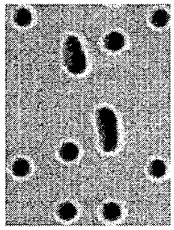

Fig. 9: Elongated Contacts printed in resist

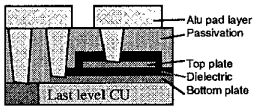

Fig.10: MIM Capacitor in Passivation layer on top of last Copper level

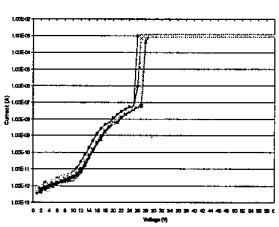

Fig. 11: I-V characteristics of MIM Capacitors until dielectric break down at high voltage

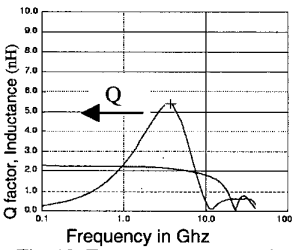

Fig. 12: Frequency response of spiral inductors with 2 thin wire levels

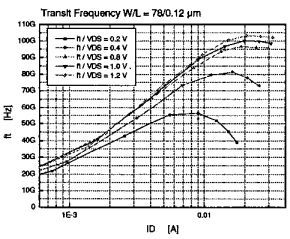

Fig. 13: RF characterization of standard Vt NFET device

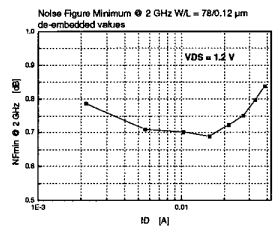

Fig. 14: Noise characterization of standard Vt device (NF min)