Trials@uspto.gov
571-272-7822

Paper No. 95
Entered: April 2, 2024

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD., MICRON TECHNOLOGY, INC., MICRON SEMICONDUCTOR PRODUCTS, INC., and MICRON TECHNOLOGY TEXAS LLC,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

IPR2022-00615
Patent 7,619,912 C1

Record of Oral Hearing
Held: January 31, 2024

Before JON M. JURGOVAN, DANIEL J. GALLIGAN, and KARA L. SZPONDOWSKI, *Administrative Patent Judges*.

APPEARANCES:

ON BEHALF OF THE PETITIONER, SAMSUNG ELECTRONICS CO., LTD., MICRON TECHNOLOGY, INC., MICRON SEMICONDUCTOR PRODUCTS, INC., and MICRON TECHNOLOGY TEXAS LLC:

THEODORE W. CHANDLER, ESQUIRE
ELIOT D. WILLIAMS, ESQUIRE
FERENC PAZMANDI, Ph.D.
BAKER BOTTS LLP
101 California Street, Suite 3200
San Francisco, California 94111
(415) 291-6259 (Chandler)
(202) 639-1334 (Williams)
(415) 291-6255 (Pazmandi)
eliot.williams@bakerbotts.com
ted.chandler@bakerbotts.com
ferenc.pazmandi@bakerbotts.com

MATTHEW A. HOPKINS, ESQUIRE
WINSTON & STRAWN LLP
1901 L Street NW
Washington, DC 20036
(202) 282-5862
mhopkins@winston.com

ON BEHALF OF THE PATENT OWNER, NETLIST, INC.:

HONG ANNITA ZHONG, ESQUIRE
JASON SHEASBY, ESQUIRE
IRELL & MANELLA LLP
1800 Avenue of the Stars, Suite 900
Los Angeles, California 90067
(310) 203-7183 (Zhong)
(310) 203-7096 (Sheasby)
hzhong@irell.com
jsheasby@irell.com

The above-entitled matter came on for hearing at 10:03 AM EST on Wednesday, January 31, 2024, at the U.S. Patent and Trademark Office, via Video-Conference.

P-R-O-C-E-E-D-I-N-G-S

10:03 a.m.

JUDGE JURGOVAN: We'll go on the record now. This is the trial hearing for the following case, IPR2022-00615, concerning U.S. Patent Number 7,619,912 B2. The date is January 31st, 2024. It is now 10:00 a.m. Eastern.

On the Panel of Judges today are Judge Galligan, Szpondowski, and myself, Judge Jurgovan. Who will be speaking on behalf of the Petitioner today?

MR. CHANDLER: Good morning, Your Honor. Theodore Chandler from Baker Botts on behalf of the Petitioner. With me is lead Counsel Eliot Williams, and backup Counsel Ferenc Pazmandi.

JUDGE JURGOVAN: Thank you. Who will be speaking on behalf of the Patent Owner today?

MS. ZHONG: This is Annita Zhong. I will be speaking on behalf of Patent Owner today. Together with me on the line is my colleague, Mr. Jason Sheasby.

JUDGE JURGOVAN: Thank you. As stated in the hearing order, each party will have up to 60 minutes to present their arguments. Since Petitioner bears the burden of proving its case by a preponderance of the evidence, Petitioner will begin, followed by the Patent Owner. Each party may reserve time for the rebuttal, limited to the opposing Party's presentation.

As you address the demonstratives, papers and exhibits in the record, please identify them clearly by paper or exhibit number, and the page

number or paragraph that you're referring to, so the record will be clear what you are pointing out in your presentation.

Please identify yourselves as you begin speaking so that the court reporter will know who you are. After the hearing, please remain on the line in case the court reporter has any questions to ask you of terms that may have been used during the hearing or other matters that may not have been fully understood.

As this hearing is public, third-parties may be listening on the line. There is information in the record that has been designated as confidential. If for some reason you need to discuss confidential information, please let the Judges know in advance so that we can address the matter.

If at any time you experience technical difficulties that impair your ability to represent your client, please alert us and contact the number given to you to resolve this issue.

Petitioner has filed a Motion to Exclude in this case. The parties may expend some of their time on the Motion to Exclude if they desire. However, it's unlikely that we'll decide that motion today at this hearing. Do the parties have any questions before we begin?

MR. CHANDLER: No, Your Honor.

JUDGE JURGOVAN: Okay.

MS. ZHONG: No questions, Your Honor.

JUDGE JURGOVAN: Thank you. Petitioner, how much time would you like to reserve for rebuttal?

MR. CHANDLER: I'd like to reserve 15 minutes for rebuttal. And I'd also like to note, Your Honor, that Counsel for Micron is on the line.

They're joined as an understudy so they will not be arguing, but I believe they would like to introduce themselves this morning.

JUDGE JURGOVAN: Thank you. Please.

MR. HOPKINS: Thank you, Ted. Petitioner for Micron. This is Matthew Hopkins from Winston & Strawn. Thank you, Your Honor.

JUDGE JURGOVAN: Thank you. Petitioner, you may begin when ready.

MR. CHANDLER: Thank you. I have some slides marked as Exhibit 1118 that I'm sharing. Judge Jurgovan, are you able to see the slides, and are you able to hear my voice clearly?

JUDGE JURGOVAN: Yes, I can. Thank you.

MR. CHANDLER: Thank you. May it please the Board, Slide 5 provides an overview of the 912 patent. As Highlighted in orange in the bottom left, the 912 patent claims priority to various provisional applications filed in 2004 and early 2005. But our contention is that Claim 16 in the 912 patent is not entitled to priority but for the application filed on July 1st, 2005, highlighted in yellow.

This dispute about priority does not matter for Grounds 1 and 2 where the asserted art predates all of the provisionals highlighted in orange. But the dispute about priority does matter for Ground 3 where the Ellsberry reference was filed on June 1st, 2005, one month before the application highlighted in yellow.

Slide 6 provides an overview of the problem identified by the 912 patent which was that high-density memory costs much more than low-density memory. You might think that if you doubled the density of a memory device that the cost would also double, but at the time of the 912

patent the cost was much more than double, which created an enormous economic incentive to replace one higher density memory device with two lower density memory devices.

To give a concrete example, imagine that a 1 Gigabyte memory device, or 1-Gigabit memory device costs $1,000 while a 512-Megabit memory chip only costs $200. In this example, if you could take two 512-Megabit memory chips and make them act like a single 1-Gigabit memory chip, you could save $600 and still have 1-Gigabit of memory.

So that's what the 912 patent proposes doing, using a technically referred to as rank multiplication where two ranks of low-density memory act like one rank of higher density memory. And rank multiplication also works if you want to expand the total capacity of the memory module.

Using the same example, let's say you want two Gigabits of memory. Instead of using two 1-Gigabit memory chips and two ranks at a cost of $2,000, you could use four 512-Megabit chips in four ranks at a cost of only $800. So now you're doubled your capacity and you've reduced your cost by $200 by using rank multiplication.

Slide 7 shows Figure 1a of the 912 patent on the right, which provides an example of rank multiplication. In the middle of Figure 1a is a logic device, highlighted in red, in Number 40. The logic device in Figure 1a receives, on the left, two Chip Select signals, highlighted in orange, where each Chip Select single corresponds to one rank of memory devices. The logic device on the right helps with four Chip Select signals, highlighted in blue, going to four ranks of memory devices, highlighted in yellow.

The result is that the host computer believes that there are two ranks of high-density memory devices on the memory module when in reality

there are four ranks of low-density memory devices on the memory module that emulate two ranks of high-density memory devices. This is an example of rank multiplication.

Slide 8 shows Claim 16 of the 912 patent on the right side of the slide. Claim 16 is the only claim challenged in this IPR. The middle of the slide shows Figure 1a again. And on the left side of the slide we've color coded some of the elements of Figure 1a, including the PLL (phase-lock loop device) 50 in brown, which transmits clock signals to the memory devices 30, in yellow, logic element 40, in red, and register 60 in green.

The bottom left of the slide provides an excerpt from the JEDEC standard which shows that read and write commands are the combination of five signals, highlighted in Footnote 1, labeled CS, RAS, CAS, WE, and CKE. You'll be hearing a lot about the CS signal, also known as the Chip Select signal used to select the rank of one or more memory devices that will perform the read or write command.

Slide 10 shows the instituted grounds. Grounds 1 and 2, highlighted in yellow, involve the Perego reference either alone or in combination with Amidi. Ground 3, highlighted in green, involves the Ellsberry reference. Again, there is a dispute about whether Claim 16 is entitled to a filing date before the Ellsberry reference, highlighted in green. But there is no dispute that Perego and Amidi, highlighted in yellow, are prior art, to Claim 16.

Slide 11 provides an overview of the Perego reference in Grounds 1 and 2. As shown in red, Perego discloses a buffer on a memory module that's backwards compatible with older generations of memory devices. One feature of Perego's buffer is that it can implement Rank multiplication.

Slide 12 provides an overview of the Amidi reference using Ground 2 in combination with Perego. Amidi is all about Rank multiplication. Just like the 912 patent, Amidi teaches having two ranks of low-density memory devices emulate one rank of higher density memory devices.

Thus, for example, as shown in Figure 6a, there are two Chip Select signals, highlighted in orange on the bottom left, that go into a logic device, highlighted in red. And that logic device, in red, outputs four Chip Select signals, shown in blue. That's very similar to Figure 1a of the 912 patent.

Slide 13 provides an overview of the Ellsberry reference used in Ground 3. Ellsberry was filed on June 1st, 2005, which we contend is at least one month before the earliest possible priority date for Claim 16 and 912 patent. Ellsberry is also all about Rank multiplication and remarkably similar to the 912 patent. As shown on the bottom right, Ellsberry teaches making two smaller capacity memory devices, to emulate a single higher capacity memory device just like the 912 patent.

Slides 14 through 31 concern the claim construction dispute over the term Rank. We contend that the proper construction for the term Rank includes one or more memory devices, while Netlist contends a Rank requires two or more memory devices. So the issue is whether just one memory device can be Rank.

Slide 15 shows that the Board has repeatedly construed the term Rank to include just one memory device rejecting Netlist's arguments to the contrary. There have been three Institution Decisions on this issue. In those three IPRs Netlist presented lengthy arguments spanning over 23 pages arguing that a Rank requires more than one memory device. But after considering those lengthy arguments I think five different judges on the

Board unanimously agreed that the proper construction included just one memory device, rejecting Netlist's arguments to the contrary.

Slide 16 shows that the District Court has also construed the term Rank to include just one memory device. Again, rejecting Netlist's lengthy claim construction arguments.

Slide 17 shows in the middle that the textbook definition of Rank includes one or more memory devices. Now Page 30 of the Institution Decision found the quote on the top of this slide to be ambiguous. But there is no ambiguity if you turn to the very next page of the textbook, which is quoted at the bottom of this slide.

The textbook states very clearly that there can be "one device per rank." The upper right of this slide shows that the JEDEC standard teaches that a rank is any DRAMs connected to the same physical Chip Signal. JEDEC does not require more than one DRAM in a rank. To the contrary, JEDEC permits any number of DRAMs connected to the same physical Chip Select signal to be a rank, including just one DRAM.

Slide 18 shows the Specification of the 912 patent. Uses the term rank consistent with the textbook definition that includes just one memory device per rank. On the upper left of this slide the Specification teaches that each rank of memory on the module has a bit width. The upper right of the slide teaches the bit width of a memory module can be 32-bits as well as other widths. Nothing in the 912 patent excludes memory modules that are 16-bits wide or 8-bits wide.

The bottom right of this slide shows the Specification teaches the width of each memory device can be 4-bits or 8-bits wide or 16-bits wide or 32-bits wide, as well as other bit widths. So that means the Specification

permits a 16-bit wide memory device on a 16-bit wide memory module, which would be an example where each rank has just one memory device. Or you could have 32-bit wide memory devices on a 32-bit wide memory module, which would be another example where each rank has just one memory device.

Slide 19 shows on the right that Netlist's expert admitted that nothing in Claim 16 limits the claim to memory devices with a particular width, and nothing limits Claim 16 to memory modules with a particular width. As a result, Claim 16 permits, for example, 32-bit width, 32-bit wide memory devices on a 32-bit wide memory module, which will be an example where each rank has just one memory device.

Slide 20 is a real world example of a memory module at the time of the 912 patent with one 32-bit wide DDR memory device per rank.

Slide 21 shows on the upper right that the related 215 patent expressly claims one memory device in each rank as recognized by the Institution Decision on the bottom left.

Slide 22 shows in the middle that the 912 patent discloses an embodiment where each rank has just one memory device, as recognized by the Institution Decision on the left. And as shown on the right, Netlist admitted that the corresponding disclosure in the provisional application embodies Claim 16. In other words, Netlist admits that a rank with just one memory device embodies Claim 16.

Slide 23 makes the point that Netlist proposed claim construction requiring multiple memory devices per rank would exclude the only embodiment for Claim 16 disclosed in the 912 patent. Which according to the quote from the Federal Circuit in the middle of this slide is rarely, if

ever, correct. Samsung's proposed construction, in contrast, is consistent with the only disclosed embodiment for Claim 16 shown on the previous slide where there is just one memory device in each rank.

Slide 24 shows that the reexamination of Claim 16 supports Samsung's claim construction. Before reexamination, Claim 16, as shown on the bottom left, depended from independent Claim 15, shown on the upper left. Independent Claim 15, shown in the upper left, was rejected during reexamination in light of Amidi, shown on the right. Amidi, as shown by the red boxes on the right, discloses multiple memory devices in each rank.

Claim 15 was rejected in light of Amidi because Claim 15 was broad enough to cover ranks with multiple memory devices in each rank. Dependent Claim 16, in contrast, survived reexamination because it does not encompass a rank with multiple memory devices, instead Claim 16 is limited to one memory device per rank consistent with the embodiment of the 912 patent, that I discussed on Slide 22.

Slide 25 –

JUDGE JURGOVAN: Counsel, can I interrupt for a second?

MR. CHANDLER: Please.

JUDGE JURGOVAN: I think that the Board's decision in the reexamination, which was affirmed on appeal to the Federal Circuit, found that the command signal is only sent to one DDR memory device when there are a plurality of memory devices in the rank. And so, I think what you're arguing here is not quite what the holding in the Board's reexamination case was.

MR. CHANDLER: Again, the claim construction, as recognized by the three Institution Decisions, is that a rank can include just one memory device. And with what I have here on Slide 24 is a quote from the Board's decision. Exhibit 1011 of Page 79. Is that Amidi clearly has multiple memory devices in a rank. And the Board rejected independent Claim 15 based on Amidi, but allowed Claim 16 to survive. The Board did not find that rank requires multiple memory devices, it just found that Claim 16 was not satisfied by Amidi because Amidi has multiple memory devices in rank.

I mean, that's the holding, it is, again, that independent Claim 15 was rejected by multiple memory devices in a rank whereas Claim 16 survives prior art with multiple memory devices in the rank. And the only difference between Claim 16 and Claim 15 is this last limitation where the command signal is transmitted to only one DDR memory device at a time.

And the way that ranks work is, the command signal, and this is what I was getting at on Slide 25, the way the rank works is the command signal is going to go to all the memory devices in the rank. That's the way DDR is setup, is that as shown in green, the address in command signals, other than Chip Select signal, go to all the memory devices.

So address and command, other than the Chip Select signal, goes to all the memory devices. And then as the Chip Select signal, which is considered part of the command code, that goes to the one or more memory devices that create the rank. So the only way to send a command to only one DDR memory device at a time, is if there is only one memory device in the rank. Or stated another way, if there is only one memory device connected to each Chip Select signal.

Are there follow-up questions on that, Your Honor?

JUDGE JURGOVAN: No. I think that answers the question. The Board's decision does have preclusive effect here, correct?

MR. CHANDLER: Well, the Board didn't provide an express claim construction. And the, I mean, we're not disputing that Amidi alone doesn't satisfy Claim 16, which is why we got Perego and we got Ellsberry. So the Board is going to be, the Board's decision is preclusive with respect to Amidi not satisfying Claim 16 alone.

But this statement in the Board's decision about the fact that requester has not provided a reasonable explanation as to why one skilled in the art would transmit a command signal to only DDR memory device at a time when there is a plurality of memory devices in a rank, that's referring to Amidi. Amidi has multiple memory devices in a rank.

The Board does not expressly provide a claim construction in this section. But the Institution Decision and the District Court have considered this statement and reexamined and have all agreed that the correct construction of rank includes just one memory device. And all of our arguments are consistent with what the Board is saying on this slide, Exhibit 1011 of Page 79.

There is nothing in this statement that requires multiple memory devices in a rank if put –

JUDGE JURGOVAN: Okay, but –

MR. CHANDLER: -- multiple memory devices in a rank does not require, by this decision.

JUDGE JURGOVAN: I think the Board said that Claim 16 distinguished over Amidi. The Claim 16 you're shown here. About what is now the last limitation. What the parties refer to as 16e.

MR. CHANDLER: Right.

JUDGE JURGOVAN: That distinguished over Amidi, and so that decision must be preclusive here, right? As affirmed by the Federal Circuit. So Amidi --

MR. CHANDLER: Correct.

JUDGE JURGOVAN: So Amidi does not teach that feature in other words?

MR. CHANDLER: Correct. And that's, and we agree with that.

JUDGE JURGOVAN: Okay.

MR. CHANDLER: We agree that Amidi teaches multiple memory devices in a rank. And so we're not relying on Amidi for that limitation. Perego teaches one memory device per rank, Ellsberry teaches one memory device per rank.

And it's important. I mean, this is the important point is that independent Claim 15 was broad enough to cover multiple memory devices in a rank, which is why it got rejected in light of Amidi. But Claim 16 is narrower than that. And Claim 16 is limited to one memory device in a rank, which is why Claim 16 survived over Amidi.

JUDGE JURGOVAN: Thank you.

MR. CHANDLER: But that's the only point I wanted to make.

JUDGE JURGOVAN: Thanks.

MR. CHANDLER: Yes.

JUDGE GALLIGAN: Counsel, this is Judge Galligan and I wanted to follow up on that. So in the Petition the Petitioner put forward a construction that a rank is an independent set of one or more memory

devices, but the argument, I think you said, can you confirm that a rank in Claim 16 can only be one memory device?

MR. CHANDLER: That's right.

JUDGE GALLIGAN: So, would the proper construction for Claim 16 to be that a rank is one memory device?

MR. CHANDLER: No, Your Honor. And I think part of your question is getting at, if you read Claim 16 as written now it seems a little odd to be written the way it is. But you got to remember, the way that Claim 16 came about, as shown on Slide 25, is that it was originally a dependent claim of Claim 15.

So Claim 15 is broad enough to cover both a situation where rank is one memory device, and a situation where a rank is multiple memory devices. That's why Claim 15 got rejected in light of Amidi, as shown on Slide 24. Is because rank, standing by itself, includes one or more memory devices and therefore Amidi, which is multiple memory devices in a rank, renders Claim 15 invalid. But then Claim 16 is a dependent claim so it narrows the scope of Claim 15 to the example of a rank with just one memory device.

JUDGE GALLIGAN: So –

MR. CHANDLER: So the construction of rank is the same for both independent Claim 15, independent Claim 16. But independent claim, independent Claim 16 is further eliminated to the situation where the rank has only one memory device. That's the only way that a command can be transmitted to only one DDR memory device at a time, as shown, for example, on Slide 25.

JUDGE GALLIGAN: Okay. This is Judge Galligan. So when construing the claim, what's currently Claim 16, and what was previously dependent Claim 16, then the Specification does not support anything more than a single device rank or the transmitting only, the command signal of only one DDR memory device at a time?

MR. CHANDLER: Correct. That's our position, as shown for example on Slide 22.

JUDGE GALLIGAN: Okay, great. Thanks.

MR. CHANDLER: Okay, thank you. Moving on to slide –

JUDGE JURGOVAN: Counsel, I have one more question.

MR. CHANDLER: Yes.

JUDGE JURGOVAN: And that is, going back to the claim if you would. There is some terminology in here about selecting one or two ranks.

MR. CHANDLER: Yes.

JUDGE JURGOVAN: What, is that dealing with the configurability or what does that mean exactly?

In your view does that mean that you could select one or you could select two, and if the prior art discloses either one of those then the claim would be unpatentable?

Or is it your view that that's like discussed that's a feature there that you can select one or you can select and both –

MR. CHANDLER: So –

JUDGE JURGOVAN: -- that capability to do both must be in the prior art in order for their, the claim to unpatentable?

MR. CHANDLER: The claim language you're referring to is in independent Claim 15.

JUDGE JURGOVAN: Right.

MR. CHANDLER: The ability to select one rank or two ranks. And that corresponds to Slide 22 where it talks about State 6 of Table 1, which is a refresh command. So a refresh command is often sent to all the ranks at the same time.

However, dependent Claim 16 further narrows the requirements of the limitation, of the claim, requiring the command signals transmit to only one DDR memory device at a time. So dependent Claim 16 does not cover the situation where the command is sent to rank. Sort of the situation where you select two ranks.

Again, dependent Claim 16 is much narrower. It requires transmitting the command signal to only one DDR memory device. That means there is one rank. But it also means that there is only one memory device in the rank because that's the only way that you can transmit a signal to one memory device at a time, as shown, for example, on Slide 25.

So the example that we point to is the read and write command. And a read and write command goes to one rank. So when you do a read and write command, as shown, for example, on Slide 22, you're going to select one rank.

The prior art clearly teaches read and write commands, and that's sufficient to invalidate dependent Claim 16. It's also sufficient, obviously, to invalidate independent Claim 15. We are not relying on a command like refresh in the prior art, which would be sent to all the ranks at the same time.

JUDGE JURGOVAN: So you're saying effectively the limitation of Claim 16 here, dependent Claim 16, vitiates that selecting two ranks?

MR. CHANDLER: Correct. You wouldn't be able to satisfy dependent Claim 16 if you're selecting two ranks because when you select two ranks there are at least two DDR memory devices and you would be transmitting, for example, the refresh command to both of those memory devices at the same time, which is contrary to the requirement of dependent Claim 16.

JUDGE JURGOVAN: Understand. Thank you.

MR. CHANDLER: Okay. Slide 26 makes the point that the figures Netlist points to do not embody Claim 16 because they transmit the command signal to multiple memory devices in a rank at a time. So to be clear, I mean, independent Claim 15 can be broad enough to have multiple memory devices in a rank at a time, but dependent Claim 16 is narrower. And the figures highlighted on Slide 26 don't satisfy the last limitation of Claim 16.

Slide 27 concerns the Verilog code in the 912 patent. The Verilog code is explained on the left. Concerns controlling FET switches for DQS strobe lines to avoid back-to-back adjacent read commands collisions, abbreviated BBARX, between the DQS strobe signals.

The FET switches create a fork in the road on the data path, as shown by Figure 6b on the right. The Verilog code has nothing to do with transmitting the command signal to the memory devices, all the Verilog code does is switch the DQS strobe signals from one fourth to the other fourth of the data path thus avoiding a collision.

Slide 29 shows that the JEDEC standard on the upper left permits the memory module that's 32-bits wide or less. And the bottom left shows that the JEDEC standard permits a memory device that's 32-bits wide. Thus, in

the JEDEC standard it is permissible to have a 32-bit wide memory device on a 32-bit wide memory module, which would mean each rank has just one memory device.

That's all I was planning to cover on the topic of claim structure, but before I go onto the next topic does the Board have any follow-up questions for me?

Slides 32 through 36 concern a legal issue raised by Netlist, which is whether a published patent application is a printed publication under 35 USC Section 311(b) as of the filing date. This legal question does not apply to Ground 1 because Perego is a patent, not a published patent application. Instead Netlist has only raised this legal issue with respect to Grounds 2 and 3 involving Amidi and Ellsberry, which are published patent applications.

And Amidi went on to issue, as U.S. Patent Number 8,250,295. So Netlist's argument is primarily directed towards Ground 3 involving Ellsberry, which published but did not issue as a patent.

Slide 35 shows the Board has repeatedly rejected the legal argument raised by Netlist and has repeatedly held that published patent applications are printed publications that are entitled to their 102(e) filing date under 35 USC Section 311(b). We've identified three decisions on this slide in our favor, submitted as Exhibits 1098, 1099 and 1100. Netlist's slides have identified a fourth decision in our favor, which is IPR2022-00149, Paper Number 33 at Pages 10 through 12.

So at least ten different judges on the Board have all agreed with our position on this issue. And we're not aware of a single judge ever agreeing with Netlist's position.

Slide 36 shows that the relevant language in 35 USC Section 311(b), on the left, mirrors the language in pre-AIA Section 301, quoted in the middle, which is shown on the bottom right, and has been understood for decades to include published patent applications under Section 102(e), it is therefore unsurprising that no judge has ever adopted Netlist's argument, which would upset the long-settled understanding for this statutory language.

And indeed, keep in mind the entire reexamination of Claim 16 was based on Amidi's published application. So if you were to except Netlist's theory, the entire reexamination of Claim 16 would be a nullity.

Before I go on to the next topic does the Board have any questions for me about Slides 32 through 36 concerning Section 311(b)?

All right. Slides 37 through 71 are just Grounds 1 and 2, where Ground 1 is Perego alone, and Ground 2 is Perego in combination with Amidi.

Slide 39 shows that Perego, in Ground 1, discloses a buffer device shown on the right in red. That works with DDR memory devices as explained on the left. The buffer device can translate protocols thus allowing for rank multiplication.

Slide 40 shows that Perego in Ground 1 also discloses transmitting a command to only one memory device at a time as required by Claim 16 of the 912 patent. Slide 41 shows that the Ground 2 combines Amidi on the right, which Perego on the left. Amidi, on the right, is all about rank multiplication and provides further details and further motivation to implement rank multiplication using DDR memory devices in Perego's buffer, on the left.

Slides 42 through 51 respond to Netlist's argument that Grounds 1 and 2 do not teach ranks or rank multiplication. Slide 43 shows that Amidi expressly discloses DDR memory devices, as stated on the bottom right highlighted in yellow. And those DDR memory devices are organized by Chip Select signals into ranks as highlighted in yellow in the figure on the right. And as explained by the texts on the left. Furthermore, the bottom left shows part of the JEDEC standard which confirms that the Chip Select signal, abbreviated CS, is what selects a rank.

Slide 44 shows that Perego also expressly discloses, on the left, using DDR memory devices. And the upper right, again, shows the JEDEC standard which requires each DDR memory device to receive a Chip Select signal which is the signal used to select a rank of memory devices as shown by the textbook on the bottom right.

Slide 45 shows that Amidi discloses rank multiplication. The truth table in Figure 5 of Amidi, on the right, shows that one address signal and two Chip Select signals can be used to generate four Chip Select signals for four ranks. Amidi is very similar to the disclosure in the 912 patent which also discloses using one address signal and two Chip Select signals to generate four chip Chip Select for four ranks.

Slide 46 shows that Perego also discloses rank multiplication. On the upper left, Column 15 of Perego, at Lines 37 through 45, teach that you can use address bits to select more independent banks. As explained by Dr. Wolfe in the middle of the slide, this is an example of rank multiplication where the address bit is used to generate additional Chip Select signals.

And as shown by the JEDEC standard on the right, for DDR memory devices you need the Chip Select signal to select a rank of memory devices,

you cannot use the address signal alone. All of this is consistent with the teaching of Amidi on the previous slide where the address bit is used in connection with Chip Select signals to generate additional Chip Select signals.

Slide 47 shows that it was obvious in light of Amidi's teachings on the upper right, and the JEDEC standard at the bottom, to use two cheaper lower density memory devices instead of one more expensive high-density memory device. For example, as shown on the bottom left, instead of using a single 1-Gigabit memory device, highlighted in red, it would be cheaper to use two 512-Megabit devices, such as those highlighted in blue, or those highlighted in green.

Similarly, as shown in the bottom right, instead of using a single 2-Gigabit memory device, highlighted in red, it would be cheaper to use two 1-Gigabit memory devices highlighted in blue.

Slide 49 shows that there was a motivation, implement rank multiplication, using 16-bit wide memory devices because they would save cost and power, improve performance as compared to 8-bit memory devices.

And Slide 50 says that Netlist's expert agreed that 16-bit wide memory devices could also save cost and power and improve performance and could be more readily available than higher density memory devices.

That's all I was planning to cover on this section before I go onto the next topic. Does the Board have any questions for me about ranks and rank multiplication in Grounds 1 and 2?

JUDGE JURGOVAN: Counsel, one question. Perego never mentions the Chip Select signal, is that correct?

MR. CHANDLER: That's correct. So Perego discloses the DDR as an option. And a person of ordinary skill would understand the Chip Select signal is required for a DDR memory device to work.

JUDGE JURGOVAN: Thank you.

MR. CHANDLER: And skipping ahead to that point, Your Honor, so Slide 60 shows that Amidi, in the middle at the bottom, teaches a logic element that receives Chip Select signals from the host computer. The JEDEC standard on the left, for DDR memory devices, confirms that CS stands for Chip Select.

And so Amidi here shows two Chip Select signals going into the CPLD. And Perego, on the right, discloses an embodiment using DDR memory devices. And in that embodiment, it would be obvious for the logic element, in red, to receive Chip Select signals as part of the input signals on the control lines, labeled RQ, because that's what the JEDEC standard requires.

And it's discussed further on the next slide, Slide 61. Which provides more detail of the RQ control line in Perego and why it would be obvious for those RQ lines to include Chip Select signals. As shown on the left in the middle, Perego discloses the RQ control lines are used for read and write commands.

And the next paragraph teaches an embodiment where the RQ control lines comprise individual control lines for row address strobe, column address strobe, et cetera. That disclosure corresponds directly to the JEDEC standard for DDR memory devices shown at the very bottom where a command comprises the signal RAS which standards for row address strobe,

CAS which stands for column address strobe, and CS, which stands for Chip Select signal.

Thus in the embodiment of Perego with DDR memory devices, as shown in the figure at the top in the middle, it would be obvious for the RQ control lines, going up to the logic in red, to include Chip Select signals for the DDR memory devices.

JUDGE JURGOVAN: Counsel, can you go back to Slide 60 please?

MR. CHANDLER: Yes.

JUDGE JURGOVAN: And here we see Amidi at the output of the CPLD shown in blue there. The lines that are selected by this data, the two Chip Select signals input, are always selecting pairs of what appears to be connections.

MR. CHANDLER: Yes.

JUDGE JURGOVAN: So how would you say that this is going to a single device if there are pairs of lines coming –

MR. CHANDLER: I –

JUDGE JURGOVAN: -- out of the CPLD?

MR. CHANDLER: We're not contending that Amidi alone sends commands to one memory device at a time, instead it's the combination of Amidi with Perego. So this is --

JUDGE JURGOVAN: Thank you.

MR. CHANDLER: -- back--

JUDGE JURGOVAN: You answered my question. Thank you.

MR. CHANDLER: Okay. All right.

JUDGE JURGOVAN: You've got about three minutes.

MR. CHANDLER: Okay. Let me –

JUDGE JURGOVAN: You can use additional time if you want to, but that will eat into your rebuttal.

MR. CHANDLER: Yes, I got you. Now Slide 67 through 69 address the PLL (phase-lock loop) limitation. On Slide 68, during prosecution, the examiner found that Amidi rendered obvious a PLL, shown on the far right in brown, operatively couped to CPLD logic in red, on the left, as well as the register in green. And the memory device is off to the right in yellow.

Now to be clear, Amidi shows the CPLD logic does not need to be coupled to the PLL, but the examiner found in the bottom left that it would have been an obvious implementation for the logic, in red, to be connected to the PLL, in brown.

Slide 69 shows that Perego also renders obvious the PLL, Numbered 570, inside the brown box in the figure on the left, operably coupled to the logic 540 in the middle. Also coupled to the registers and interface 590 highlighted in green in the bottom. And also coupled to the DDR memory devices connected to the interfaces on the left and right numbered 520. Now as shown in the upper right, JEDEC teaches a PLL, highlighted in brown, connected to memory devices, in yellow, as well as a register, highlighted in green.

As shown in the bottom right Amidi teaches essentially the same thing, a PLL, in brown, connected to the register, in green, and the memory devices, in yellow. Thus, it was obvious for Perego, on the left, to connect the PLL to the memory devices and the register. And furthermore, as explained in the middle, at the bottom from the petition, and consistent with the reasoning of the examiner –

JUDGE GALLIGAN: Counsel?

MR. CHANDLER: -- on the previous slide –

JUDGE GALLIGAN: Counsel, this is Judge Galligan. Can I interrupt for a moment?

MR. CHANDLER: Yes.

JUDGE GALLIGAN: We need to make sure that Patent Owner's Counsel is on the line. We may have lost her. Sorry about the interruption.

MR. CHANDLER: Okay, I understand.

JUDGE GALLIGAN: Okay, give us a moment. It appears she is not, there goes a normal reconnect.

(Pause.)

MS. ZHONG: Hello?

(Pause.)

JUDGE GALLIGAN: Okay, Patent Owner's Counsel is back. Where did you drop off?

MS. ZHONG: So I think I dropped off about five slides ago. Five or six slides ago.

MR. CHANDLER: I skipped a bunch of slides.

MS. ZHONG: Okay. So I dropped off about five minutes ago I think, let's just put it this way.

MR. CHANDLER: All right. What would the Board like me to do? I was covering PLL on Slide 68.

MS. ZHONG: That's just fine, you can continue.

MR. CHANDLER: Okay.

MR. SHEASBY: Yes, I, Your Honors, I sent notes to lead counsel, Dr. Zhong, when she dropped off so there is no need to repeat what Mr. Chandler said. She was looped into it.

JUDGE JURGOVAN: Thank you, Counsel. Petitioner, you can continue.

MR. CHANDLER: Okay.

JUDGE GALLIGAN: In the future just, when Counsel drops off we can just stop, you know, and pause and get her back on. Thanks.

MR. CHANDLER: All right. So picking up on Slide 69, I was discussing the text in the middle from the Petition. It was obvious for Perego on the left to connect the PLL to the memory devices in the register. Furthermore, as explained by the Petition in the middle of this slide, and consistent with the reasoning of the examiner on the previous slide, it is obvious to connect the PLL to the logic in Perego's buffer because the logic needs to be in sync with the memory devices so that the devices can generate Chip Select signals that will work with memory devices.

I've only got a few minutes left. Slide 71, the Board agreed that Perego discloses transmitting commands to only DDR memory device at a time. So to Judge Jurgovan's question, we're relying on the combination of this teaching by Perego with Amidi, we're not relying on multiple memory devices in a rank we're relying on the embodiment of Perego where there is only one memory device per rank and only one channel going to each rank.

I'll touch briefly on Ellsberry. The primary dispute on Ellsberry is the priority fight. So Slide 78 shows that the Institution Decision correctly concluded that in the 244 provisional, in the upper right, is not disclosed row address, bank address, and Chip Select signals. Especially the bank address signals.

And then, furthermore, the 436 patent, in the bottom right, is missing a register separate from a logic element. So the Institution Decision

recognized that the burden of production was on Patent Owner to show the subject matter of Claim 16, the 912 patent, as supported by its priority applications.

As explained on Slide 79, most of Netlist's arguments about Section 112 support for Claim 16 are based on obviousness. But the Federal Circuit has made clear that obviousness is not sufficient to satisfy Section 112, there has to be a written description within the four corners of the document to satisfy Section 112. So it's not an obviousness issue it's a question of whether there is actually a disclosure in the 244 provisional or the 436 patent.

For the 244 provisional, as shown on Slide 81, the big, one of the big things that's missing is the bank address signal. So the 912 patent, on the left, clearly shows the bank address signal, which is highlighted in red. The 244 provisional, on the right, the bank address signal is conspicuously missing. There is no bank address signal shown in the 244 provisional or discussed in the 244 provisional.

As discussed on Slide 82, there is reference, as shown on the top and the middle, to an address signal, but there is no reference to a bank address signal. Furthermore, the claim requires both a row column address and a bank address signal.

And there is no discussion of two address signals going into the logic, which is referred to as an ASIC decoder. Instead you see, at the bottom here, there are address signals going to the register. Those address signals might include a bank address, but there is nothing in the 244 provisional showing a bank address signal going into the logic.

Another thing that's missing from the 244 provisional is DDR memory devices, as explained on Slide 83. The 244 provisional just refers to DRAM, but there are lots of different types of DRAM. DDR is one type of DRAM but it's not necessarily the only type. Netlist's expert admitted on Slide 83 the 243 provisional does not refer to DDR.

And as explained on Slide 84, this issue of DDR is important because DDR memory is what introduced the DQS strobe signal. And it's the DQS strobe signal that results in the back-to-back adjacent read command collision.

So the whole BBARX collision that was addressed and solved by the 912 patent, on July 1st, 2005, doesn't exist in the 244 provisional because the 244 provisional doesn't mention DDR memory devices and therefore it does not mention DQS strobe signals and therefore has no discussion, whatsoever, of the fork in the road or using FET switches on the DQS strobe line to avoid this collision.

So that's why the, you know, two reasons why the 244 provisional doesn't provide support. And then with the 436 patent, there is an important legal issue here which is that the burden of production was on Netlist. And as shown on Slide 86, Netlist understood that it had a burden of production, and it tried to satisfy that burden of production for the 244 provisional which is why they included the claim chart in their Patent Owner response.

But for the 436 patent Netlist didn't do anything. Netlist did not try to address each and every limitation of the 436 patent, instead they waited to their sur-reply, which is improper, as explained on Slide 87.

As shown in the upper left, the Institution Decision made clear that the burden of production was on Netlist. And as explained on the bottom

left in the right, it's improper for Netlist to wait until its sur-reply to try to make the showing with respect to the 436 patent.

As shown on Slide 88, the key thing that's missing from the 436 patent is a PLL, in brown, that's coupled to a register, in green, as well as a logic element, in red. So that was disclosed in the 912 patent on the left. But the 436 patent on the right doesn't disclose a PLL and doesn't disclose a register, in green. A Netlist expert admitted in the bottom right there is no PLL shown in Figure 11a of the 436 patent, which is the figure that Netlist contends embodies Claim 16.

As shown on Slide 89, Amidi, in the middle, as well as JEDEC on the right, teach that you can have a PLL that's not connected to the logic. And this is what Netlist argued at the bottom of the slide during reexamination. Netlist argued Amidi doesn't teach a PLL connected to the logic, instead in Amidi and the JEDEC standard the PLL is just connected to the register and the memory devices.

Now the examiner found that it would be obvious for a PLL to be connected to the logic, but obviousness is not sufficient to satisfy Section 112, there has to be a written disclosure. And there is no written disclosure in the 436 patent of a PLL that's connected to both the logic and the register.

I think I will rest there, unless the Board has any questions for me on any of the arguments that I've raised.

JUDGE GALLIGAN: Counsel, I have a question on Ellsberry. The disclosure of Ellsberry.

MR. CHANDLER: Yes.

JUDGE GALLIGAN: There were the grounds based on Ellsberry that's not related to the priority issue. This is Judge Galligan.

On Petitioner's Reply, Pages 14 to 15, there is a discussion that the JEDEC standards make clear that the width of the module doesn't need to be 64, 72 bits, and can be smaller. Can be 8 or 16. And I wanted to ask you it. I've looked at Exhibits 1106 and 1107 at Pages 7 to 8 –

MR. CHANDLER: Yes.

JUDGE GALLIGAN: -- and I didn't see, and maybe you can point me to it, where it says the module width is, in some of these, is 64, 72, the device width could be 8 or 16. Where does it refer to the module in 8 or 16 in those references?

MR. CHANDLER: Yes, so this is addressed on Slide 101. And I think what you're getting at, Your Honor, is the way that the standard, Exhibit 1107 is laid out, is they don't print a row for every single possible entry, because that would be hundreds and hundreds of entries. Instead they use a hyphen to show when there is a range. So on the upper left, Exhibit 1107 shows that the width can be zero, and then the next row is a hyphen, and the next row is 32.

And as Netlist's expert admitted on the right side of this slide, Exhibit 1101 at Page 152, the JEDEC standard permits a width of zero through 255 to be specified. And you can understand this use of the hyphen on the bottom left where the text makes clear, for example, the width of the memory device. That the width can be X4, which is pronounced by 4 and refers to 4 bits wide.

It can be 4 bits wide, 8-bits wide, 16-bits wide or 32-bits wide. But if you actually go to the rows, there is only a row for 15, and then there is a dash. And then the next row is for 254. That's simply just to save space when they print out the document. They're not going to printout every

single row between 15 and 254, instead they just do a dash to indicate that a person of ordinary skill would understand that you just follow the same pattern of how you specify the bits for the bit width.

But it's clear, the text clearly states that you can have a 16-bit wide memory device, even though 16 is not specifically listed in the row. You can also have a 32-bit wide memory device, even though that's not specifically listed in the row. And of course the 912 patent itself also says that the width can be 16 or 32-bits. And with respect to the module width, the 912 patent also makes clear that other widths, other than 32, are also permissible.

JUDGE GALLIGAN: This is Judge Galligan. To follow up, you were mentioning memory device width, and I think Patent Owner's argument is that there is a memory module, obviously that's claimed, that's made up of memory devices. And the module width would basically be 64 or 72. Under the JEDEC standards the width of the device may be smaller.

And I'm looking there and there is the module width on page, for instance, 13 of Exhibit 1107, the module width says, or what's there on this Slide 101. It says, module width 64, 72. Where, and then it has device width. Where does module width -- where is the module width specified as smaller than 64 in this reference? In this JEDEC standard?

MR. CHANDLER: Well it expressly, so in the upper left you see I've got 32 highlighted --

JUDGE GALLIGAN: Yes.

MR. CHANDLER: -- right below the, so that's an expressed example of a module width that's --

JUDGE GALLIGAN: That's the module width, that's not the device width? The memory device width.

MR. CHANDLER: Bit 6 is the width of the entire memory module, and then Bit 13 is the width of each memory device.

JUDGE GALLIGAN: Okay. All right, thank you.

MR. CHANDLER: Okay. I'll reserve the rest for rebuttal.

JUDGE JURGOVAN: Okay, thank you. Let's go to Patent Owner. Patent Owner, how much time would you like to reserve for rebuttal?

MS. ZHONG: Fifteen minutes please, Your Honor.

JUDGE JURGOVAN: Fifteen minutes, okay. You may begin when ready.

MS. ZHONG: Good morning, Your Honors. This is Annita Zhong on behalf of Patent Owner, Netlist. Before I start, can Your Honors see my screen?

JUDGE JURGOVAN: Yes, we can.

MS. ZHONG: Okay. So let me start. This is not the first time the Office and the PTAB have reviewed the challenged claim 16 of the 912 patent. Between 2010 and 2019 the Board has twice affirmed the examiner's finding of validity of the challenge to Claim 16. And the Federal Circuit, as Your Honors have pointed out, affirmed the Board's finding. And Your Honors should again find the patent, Claim Number 16, valid this time.

I am on Slide Number 107. So as Judge Jurgovan pointed out, the one reason the Federal Circuit and the Board and the examiner found Claim 16 valid, despite of the ten years of reexamination history, is the requesters could not provide a reasonable explanation as to why one skilled in the art

would transmit a command signal to only one DDR memory device at a time when there are a plurality of the memory devices in the rank. This is Exhibit 1011, Page 79.

At this time the Petitioner still cannot show why this would be the case. In fact, as shown by their own admission, and this is from the Reply, page number 3, by Petitioner's own admission, if there were more than one memory device in the rank then the command signal would be transmitted to all the memory devices at the same time as a POSITA would have understood as to how the rank is organized and operates. If that is the case, Claim 16 cannot be obvious.

So, in order to overcome this particular problem, what they did is, they took the Board's, and the Federal Circuit's previous finding, as a roadmap and did some hypothetical construction. Construction in which there is only a single device per what they call the rank. They did that for Perego, they did that for Ellsberry.

What they did not show is, they don't even contend that it would be obvious to transmit a command signal to only one device at a time when there are multiple devices per DDR. Per rank.

So –

JUDGE JURGOVAN: Counsel, can I ask a question for a second?

MS. ZHONG: Sure.

JUDGE JURGOVAN: Is there any language in Claim 16 that says a rank includes multiple memory devices?

MS. ZHONG: Let me put it this way. I think, as the Counsel has conceded, rank means one or more. And there is nothing distinguishing the rank in Claim Number 16 from the rank before.

And Claim 16 would be, there would be no reason for the Board to have confirmed Claim 16 if it can be interpreted so trivially as covering transmitting a device. A command to only one device. "Only" there is but a single choice in that particular rank. And it would be meaningless.

So to give the meaning to Claim 16, and the last limitation, the claim needs to be interpreted in such a way that it requires the capability to transmit a command signal to only one device at a time. Even when there are multiple devices and rank per selection.

JUDGE GALLIGAN: Counsel –

MS. ZHONG: Otherwise –

JUDGE GALLIGAN: This is Judge Galligan. I wanted to follow-up on that. I mean, it's hard to imagine construing a claim based on an assertion of triviality if the claim indeed, you know, takes a rank that has multiple, you know, memory devices. And then it adds a limitation that says, this dependent claim applies to a rank of one memory device.

Why, if that's the case, why would we not construe it that way based on an assertion that the examiner would have thought it was trivial? I mean, I don't think we can really go there.

MS. ZHONG: Understand. First of all, I do believe the claim, the patent itself repeatedly discloses there are multiple devices per rank, including the Verilog code, and I can go there.

The second thing is, Ellsberry includes multiple devices per rank. They don't, in the deck interpretation the disclosure for Perego also include multiple devices per channel. Additionally, I really don't think, for Perego in particular, we need to go there. Whether there is a single rank, a single device per rank, or multiple devices per rank.

There are other grounds to affirm Perego because Perego involves a Rambus style structure that's completely different than what is claimed by Claim 16. Which is what a POSITA would understand. It's directed to a JEDEC style memory module.

JUDGE JURGOVAN: Counsel, can I ask one more question about Claim 16?

MS. ZHONG: Yes.

JUDGE JURGOVAN: And it's the same question I posed to Petitioner's Counsel. And that is, dealing with the selection of one or two ranks, do you agree with Petitioner that the limitation, the last limitation of Claim 16, walks back the option to select two ranks?

In other words, there is only the option now to select one rank when you consider the last limitation of Claim 16?

MS. ZHONG: I'm not sure that's true because there are possibilities, which we choose two ranks for write operation, for example. But you can, under the Claim 16 you can still, you still require to send the command signal to pick one device at a time.

So in fact, it will be only a single device in the particular rank, but it could still be selected two ranks. But the command signal somehow is still targeting a single device in those two selected ranks such that only one of the devices is returning data. And that's the whole advantage of the Claim 16.

Even though at the time of the invention, as Petitioner's Counsel has mentioned, the state of the art was such that all devices in the rank had to respond altogether, act together. What the inventors really thought about is, there may be possibility when you wanted to have that flexibility that only

one of them should be responding instead of having to force everyone to be responding at the same time.

JUDGE JURGOVAN: So what you're saying is the two rank selection means that there is a sequence of operations, like when a device is read out from one rank and then again another device from the second rank, one at a time each?

MS. ZHONG: Not necessarily the read operation. Read operation may be limited to one, I need to think about it. But in the write operation it says possible for you to write to both ranks at the same time. Basically the same data replicated to both ranks. There would not be collision problems as would be in the read operations at least. So that's a possibility.

Whether it's done commonly, probably not. But it's also not excluded. And it's also not impossible to do.

JUDGE JURGOVAN: Okay. One other thing that would be helpful for you to address is the disclosure at Column 8. And what is Patent Owner, I'm talking about Column 8 of the 912 patent --

MS. ZHONG: Okay.

JUDGE JURGOVAN: -- what does Patent Owner consider this to mean?

MS. ZHONG: Okay, let me pull up the patent.

JUDGE JURGOVAN: It's what Petitioner is relying on to assert that rank can be only one device.

MS. ZHONG: Okay. So it may be easier if I share my screen of Column 8 with –

JUDGE JURGOVAN: Yes.

MS. ZHONG: -- Your Honors.

JUDGE JURGOVAN: Thank you.

MS. ZHONG: If I can figure out how to do it. So can Your Honors see my screen?

JUDGE JURGOVAN: Yes, we can.

MS. ZHONG: Okay. Let me see --

JUDGE JURGOVAN: Okay now, starting with line, do you see Line 47, in certain embodiments?

MS. ZHONG: Yes. In such embodiments a command signal is sent to only one memory device, or the other memory device, so that data is supplied from one memory device at a time.

JUDGE JURGOVAN: Yes. But, I mean, I want you to start earlier there.

MS. ZHONG: Okay.

JUDGE JURGOVAN: It says, in certain embodiments the command signal is passed through to the selected rank only.

MS. ZHONG: Okay.

JUDGE JURGOVAN: In such embodiments the command signal is sent to only one memory device, or the other memory device, so that data is supplied from one memory device at a time.

MS. ZHONG: Okay.

JUDGE JURGOVAN: Doesn't that sound like a rank can have one device?

MS. ZHONG: No. I would say like, since the previous one is saying sending the command to only the selected device, and the next one is talking about, in that case, is sent to only one memory device or the other memory device.

JUDGE JURGOVAN: But that in such embodiments connects –

MS. ZHONG: No, no, no.

JUDGE JURGOVAN: -- the previous sentence to the next one.

MS. ZHONG: Yes. So a reasonable read is those memory devices are in that selected rank. Right?

JUDGE GALLIGAN: Counsel?

JUDGE JURGOVAN: Okay, I see your -- I see your point. Thank you.

MS. ZHONG: Thank you.

JUDGE JURGOVAN: Pardon me.

MS. ZHONG: Sorry.

JUDGE GALLIGAN: This is Judge Galligan, I have a question on that. So where is the disclosure in figures, or description, of where the read signals are further bifurcated or the read signals are further channeled to only one of the memory devices in the rank under your reading of it in Column 8?

MS. ZHONG: In Column 8? That's what it says, the command signal is sent to only one memory device.

JUDGE GALLIGAN: Right. So under your reading of it, if that's what it says, if there are multiple devices in here and it goes to one memory device –

MS. ZHONG: Yes.

JUDGE GALLIGAN: -- how is that done?

MS. ZHONG: Okay. So the Verilog actually gave you the answer for that. So let's go to Page 31. I hope this, yes. So the Counsel mentioned that this Verilog Number 2 is about controlling the DQS signal. As we have

shown on Slide 108 of Netlist, actually Micron's expert has conceded people would also consider DQS as a command signal. But beyond that, if you look at Verilog, the highlighted portion I am showing here, it has a beginning and an end. And the last few lines of the end is en_fet_a. Basically, enable FET. And there is another line for disable FET. And that's how it's done.

And before that, if you look at it, it's all adding zero, adding zero. Those are read and write. So those are our command. So actually a POSITA reading this would understand this is actually not about DQS signals but it's consistent with a disclosure elsewhere that it's actually monitoring the command signals and enabling the FETs as a result.

And if you look at here it says, enable FET A, enable, disable FET A, the A and the B are nomenclatures used in connection with memory devices. Let me see, Column 24. Let me see if I can get to there. My apology, Your Honors, my computer is a little bit slow.

So Column 24, the first paragraph, and the end of the sentence is saying, as shown in Figure 5, the last data strobe of memory device A. So you see like A is in connection with memory device, and B is also in connection with memory device. So that's how the commands are controlled through the FETs. To either enable, disable, and that's how the signals are sent to those devices.

JUDGE JURGOVAN: Okay, so how do we --

(Simultaneous speaking.)

JUDGE JURGOVAN: -- that, I'm sorry.

JUDGE GALLIGAN: Oh, I was going to --

JUDGE JURGOVAN: Sorry, go ahead, Dan.

JUDGE GALLIGAN: -- to follow -- oh, I was just going to ask, where in the Patent Owner's Response was there an explanation of the read signal going through these checks?

MS. ZHONG: I understand Dr. Brogioli has provided detailed explanation of how the Verilog works, and it would be there.

JUDGE JURGOVAN: So, Counsel, how do I know that your Verilog explanation is connected to the Column 8 description?

MS. ZHONG: So, let me, hold on. So before the Example Number 2 Verilog is discussed, describes what is the embodiment.

JUDGE JURGOVAN: Okay. So it says, Example 2 there. And how does that connect to the Column 8 disclosure. How do I know that Column 8 is talking about Example 2 of the Verilog code?

(Pause.)

MS. ZHONG: So, as I mentioned, in Verilog, in Example Number 2, you are talking about FET A and FET B. And A and B are devices, memory devices. And B, as described elsewhere, for example, in Column 24. And a POSITA would understand A and B are the memory devices in the rank. So that's how they would understand. That's --

JUDGE JURGOVAN: Okay, thank you.

MS. ZHONG: -- really is. I mean, as in the prior art you have to read the whole thing. The entire description. Where is the background knowledge of a POSITA.

As I've explained before, FET A and B, A and B are in connection with memory devices A and B. Like in Column 24. And Column Number 8 is talking about memory devices. One memory device and another memory device. So Device A and Device B, even though it's not expressly spelled

out, a POSITA would understand we are talking about sending to one and the other, to the enablement or disablement of the FETs.

JUDGE GALLIGAN: Counsel, one, this is Judge Galligan, I have one further question. Where are these FETs located?

MS. ZHONG: Those FETs --

(Pause.)

MS. ZHONG: I don't think the figures really show where the FETs in Example Number 2 are connected, but if you look at the language of the entire, the Verilog, it's talking about because it's controlling the command lines, right? Discovery RD. So those, the FETs will be on the connection point between the connect line from the ASIC to the devices. That's where the control is.

JUDGE GALLIGAN: Okay, thank you.

MS. ZHONG: Okay. So let me reshare my PowerPoint.

(Pause.)

MS. ZHONG: So, as I mentioned before, we don't, for Perego at least, we don't have to be hung up on the question of whether there is one device in the rank or two devices. Two or more devices in the rank. Because Perego's architecture is completely different. It does not use Chip Select signals, as Your Honors have observed. It does not have a concept of rank either.

And it certainly does not have any need for rank application because, as I'm going to go into it, the whole problem in rank multiplication really has to do with a limited number of Chip Select signals that a memory slot can route and a memory module can receive. If you don't have that limitation, there is no need for rank modification.

In fact, as far as Perego's architecture is concerned, it would be a step backward for it because it will lose the flexibility it has with existing address selection. It's like addressing existing signal, signaling protocol that can address one device at a time, two devices at a time, any device at a time, all devices at a time. And losses that flexibility.

It will be tied into the more restrictive JEDEC style addressing, which is limited to one or two ranks at a time. And also because of Perego's very vastly different architecture than what is claimed in Claim Number 16, Amidi is really not going to remediate that problem because Amidi, again, like Claim 16, is directed to a JEDEC style signaling protocol. It's not going to motivate a POSITA to look at a Perego with a completely different signaling architecture protocol and a memory module architecture to say, let's change the basic principle, operating principle, and a structure architecture of Perego and make that modification. As Your Honor is amply aware, changing the basic operation of the primary reference is an indicium of non-obviousness.

As to Ground Number 3, which is Ellsberry, we do believe 244 provides ample support for Claim Number 16. As a result, Ellsberry is not prior art. And even if Ellsberry is prior art it does not teach or suggest a -- limitation of Claim Number 16.

JUDGE JURGOVAN: Counsel, how do you address Petitioner's contention that you didn't show support in the 436, and Ellsberry is therefore --

MS. ZHONG: Um --

JUDGE JURGOVAN: -- you haven't shown the disclosure was there through the entire priority chain?

MS. ZHONG: Okay. First of all, the priority chain is not 436. The -- 912 independently claims priority to the 244. So there is no need for you to establish priority for the 436.

It incorporates by reference the 244 provisional and independently claims priority to the 244. So 244 alone should be able to support the claim 16. It doesn't have to go 436. 436 is an independent reason why Ellsberry does not quality as prior art. But those two, 244 analysis and 436 are two independent avenues.

JUDGE JURGOVAN: Okay, thank you.

MS. ZHONG: Yes.

JUDGE GALLIGAN: Counsel, I had a question on that. This is Judge Galligan.

MS. ZHONG: Yes.

JUDGE GALLIGAN: So the filing date of the 912 application was September 27th, 2007. The provisional, the 244 provisional was July 15th, 2004. So you can file a provisional and then over three years later you can file a patent based on that?

MS. ZHONG: No, no, no. No, no. So there is another one, 386, that's filed within a year of that provisional. And the 912 is a continuation of that application. The 386.

JUDGE JURGOVAN: Okay, I see.

MS. ZHONG: So that's a chain, yes.

JUDGE JURGOVAN: Did you show support in the 386 then?

MS. ZHONG: 386 is –

JUDGE GALLIGAN: Right.

MS. ZHONG: Okay. 386 is the July 1, 2005, filing date. And that's a date that Counsel has been talking about because 386, 912 is a continuation of 386. So 386 will have the same disclosure as 912.

JUDGE JURGOVAN: I see. Thank you.

MS. ZHONG: 386 –

JUDGE JURGOVAN: That answers my question.

MS. ZHONG: -- is, yes. Yes. 386 is the CIP for 436. And has, there is that dispute of whether 436 supports it.

But I also want to point out, we do have the burden of production, but our production, burden of production is commensurate with the arguments raised in the Petition. And I think I can look for the case law. I don't have it in hand right now, but there are case law, Board case law that says the burden of production is commensurate with the arguments raised in the Petition. In the Petition they never mention the PLL issue, they never mention the last limitation, those are new arguments. That's inappropriate for them to raise for the first time in the Reply.

But let me go back to Perego. And I'm on Slide Number 14. And I want to talk about missing limitation Number 1, which I will use the shorthand "rank modification" limitation.

What this limitation is really about is to say, the memory module is going to receive from the computer system a set of input signals. The problem with this set of input signals is that it can only control a few number of ranks and a few number of devices than that are actually on the memory module. And the actual number of devices and actual number of ranks are the first number of ranks. And the emulated, or the transparent number of

ranks and devices that the input signal can control at a second number of ranks.

So as Dr. Brogioli has testified, and which Petitioners do not really dispute, is that rank multiplication is used where the number of Chip Select signals that a memory controller can use or select a set of memory devices is less than a number of sets of memory devices on the memory module. If you don't have that problem there is no need for you to advise an ASIC to do the rank multiplication because an ASIC is very expensive.

And the reason for using rank multiplication, you don't just have to take Dr. Brogioli's word for it, let's go to Slide Number 18 and look at what Amidi says. Amidi Paragraph's 10 and 11 gave the reason why it did rank multiplication.

At the end of Paragraph 10 of Amidi it says, all standard memory modules have only two Chip Select signals per memory socket routed. And as a result of that, you cannot address a memory module with more than two ranks on the module. Which means, even if it is physically possible for you to have four ranks, eight ranks, you just cannot take advantage of that. So there is a need for you to somehow fool the system into thinking that you only have two ranks while you have four, and can still use every single one of the devices on the rank.

912 is not different. The same disclosure, on Page 17, Column 2, Lines 23 to 42 of the 912. Again, the problem is really that the standard memory slots and modules only support one rank or two rank memory modules at a time. It makes increased independency on the memory module difficult because you cannot tap into the additional ranks beyond rank Number 2.

But Perego does not have that problem. Perego does not have that problem. And I'm on Slide Number 19 showing you Perego Exhibit 1035, Columns 14, Line 52 through Column 15, Line 6. Perego addresses or selects a device by using addresses. The address of the transaction will determine which target subset of channels will be utilized for that particular data transfer. It does not need to use Chip Select. That is a very fundamental difference between Perego's architecture and what's at issue in Amidi, what is claimed by Claim Number 16.

Slide 20. Again, another passage from Perego in Column 15, Lines 31 to 45. Again, showing you how Perego is selecting its targeted devices, addressed bits. That's how it's doing it.

So what is the significance of that? The significance of that is shown on page, Slide Number 21, Column 10, Lines 22 through 40 of Perego. Perego can choose one rank, two ranks, four ranks, at will. It does not need additional support in order to tap into other devices on the memory module. It can choose one rank, if it suits its need. It can choose all ranks all at once with its existing input signals at once. It can choose two ranks or two channels if that's what it wants.

And this is not in dispute. Petition says, Perego discloses selecting one memory device and transmitting the corresponding signals to select memory device.

If that is true, as they describe, there is no need for the rank multiplication because contrary to what's required by the rank multiplication limitation, the input signal of Perego can already control the same number of devices and channels as the set, the actual number of devices and channels

that are on the memory module, it does not meet that rank multiplication since a technique that is required for Amidi in Claim 16.

Now I will quickly go to missing limitation Number 2 which is selecting one or two ranks of the first number ranks. And let's go to Slide Number 26. For that limitation, what the Petitioner relied on is Perego Column 15, Lines 37 to 40.

We asked Dr. Wolfe specifically whether that passage is related to selecting a particular group of devices to respond to a request. And he said, I don't think so. And we discussed with him the passages around what's exactly coded. And his conclusion is, again, I don't think the paragraph specifies how ranks are selected or enabled.

But what does a claim require? Selecting one or two ranks of the first numbered ranks. And what Dr. Wolfe is saying, whatever the Petition is relying on does not disclose that particular limitation. And the Petition does not rely on any other reference for this limitation so the combination fails as a result.

Now regarding the Chip Select signals. Petitioner concedes that Perego does not have Chip Select signals. And Chip Select signal is not a true signal. It is very important for this whole invention, especially for the rank multiplication limitation because as I mentioned before, the whole rank multiplication came about because the memory module can only support one or two Chip Select at a time. Chip Select is also important because Chip Select is indicative of a JEDEC style memory device, module, as was the term "rank."

Perego, on the other hand, is assigned to Rambus. And Rambus has, uses a completely different architecture. Rambus does not use Chip Select

network, that is a common knowledge as evidenced by Petitioner's own evidence, Exhibit 1033 at Page 338, as well as Exhibit 1034 at Page 12.

So to get around the fact that Perego does not Chip Select, Petitioner did a sleight of the hand. They did not look at what the input signals really are, as required by the claim, they looked instead at what the output signal would be for DDR2 SDRAMs. But the claim is looking at input signals and not the output signals to the DDR device.

Okay. They said that Perego is constantly using DDR devices on the memory module. That is true. But they do it in a different way. They use it through a translation protocol, as described in Perego, Column 10, Lines 54 to 67. Especially in the last sentence. They use a translation.

What that means is, they take a Rambus signaling protocol and translate that into what can be used by DDR devices. And that is a similar architecture than was shown in Perego for the 2a, the prior art architecture, where it uses a Rambus channel which is a Rambus signaling protocol. But it used a memory translator hub, MPH 250, to translate those signals to what the SDRAM can understand.

Now, the difference between Perego's invention and -- prior art is Perego used a configurable buffer width. And it also used point-to-point architecture. But the fact of using the Rambus signaling, followed by translation to the SDRAM understood output, that portion was not changed.

And also how do we know Chip Select is not involved in the Perego input signals - we know that DRQ is symbolic or indicative of Perego's Rambus RIMM architecture. That's shown in Exhibit 2054. And I'm on Slide Number 43. Exhibit 2054, which is a Samsung's RIMM datasheet. And the signal that's being received by the RIMMs, you can see there is

RQ7 through RQ0. Those are the column and row access control signals. No Chip Select signals. RQs are RQs.

RQs, the input signals, are those of the Rambus ones. They are not the JEDEC style ones. And if you read that paragraph that the Petitioner relied on, it never mentions Chip Select signals, it mentions RAS and it mentions CAS, but not Chip Select signals.

The Chip Select signal is a meaningful and a material limitation and needs to be disclosed in prior art, you cannot just take it as granted. That this Rambus signal would have that signal. A POSITA would not so understand.

So in the remaining time I want to go through, quickly, as to why 244 actually does provide support. The bank address is received by the logic element. And why BBARX is really not a problem.

So just want to remind you, the key dispute is whether the control signal would include the bank address signal that's received by the ASIC are used for the output to control the four ranks.

On Slide Number 66, which is the 244 provisional paragraph number 5. Control Signal is expressly disclosed as including an address signal. Which a POSITA would understand would include the bank address signal as well as row and column address signal. This is not about obviousness, it's about what a POSITA would have understood. Why they would understand address signals would include bank and row address.

Look at the Exhibit 1030 that Petitioner cites, Page 13. In this command truth table, address signals include bank and row address. This is on Slide Number 67.

Slide 68, it's an excerpt from a data sheet. Contemporaneous data sheet from Micron. Again, bank address signals, row/column address signals are both considered part of the address space.

And a POSITA would also understand, given the context of the 244, which is rank multiplication and the addressing space for DRAMs, for different densities of DRAMs, they would understand, for example, to differentiate a 512-Megabit density DRAM versus from a 1 Megabit. But density, that particular address bit would be bank address number two versus if you wanted to differentiate a 1-Gigabit versus a 2-Gigabit, you are talking about the row address bit 14.

That's why paragraph 5 of 244 provisional does not really say whether it's bank address or it's row address because a POSITA would understand. Based on that context and the invention, it's covering both the row column address, and the bank address signals but for different situations.

JUDGE JURGOVAN: Counsel, is the bank address, how does that distinguish from other address signals?

How do I know I have a bank address signal as compared to a row or a column address signal?

MS. ZHONG: So there are, in JEDEC style ones there are distinct lines with the bank address coming in. That's how you know, like, this is a bank address signals.

JUDGE JURGOVAN: But physically on the chip --

MS. ZHONG: On the --

JUDGE JURGOVAN: -- what --

(Simultaneous speaking.)

MS. ZHONG: -- decoders. So there are decoders.

JUDGE JURGOVAN: Yes.

MS. ZHONG: So --

JUDGE JURGOVAN: So, I mean, is the chip setup such that you have --

MS. ZHONG: Yes.

JUDGE JURGOVAN: -- units of memory --

MS. ZHONG: Yes.

JUDGE JURGOVAN: -- that are banks?

MS. ZHONG: Yes. So --

JUDGE JURGOVAN: Or is this just kind of a fictional --

MS. ZHONG: No, no, no, it's not.

JUDGE JURGOVAN: -- you have a most significant, the most significant bits of the address?

MS. ZHONG: So there are different signals coming in, bank address and address. And the memory array is set up in such a way. There are, for example, eight banks. Physical banks. And a row and a column would be in targeting with a particular bank. So bank would decide, bank address would decide, for example, on Slide Number 68, kind of a logic diagram. So you will see there it's Bank 0, so Bank 7.

JUDGE JURGOVAN: So if you --

MS. ZHONG: So the --

JUDGE JURGOVAN: If you put the chip, you would, you know, under a microscope you would see these different areas that are different banks --

MS. ZHONG: Yes.

JUDGE JURGOVAN: -- on the chip?

MS. ZHONG: Yes.

JUDGE JURGOVAN: Okay. All right.

MS. ZHONG: So there will be different, mainly arrays that line to different banks.

JUDGE JURGOVAN: Got it. Thank you.

MS. ZHONG: And in each memory bank, then there is a row and column to differentiate --

JUDGE JURGOVAN: I understand.

MS. ZHONG: -- like which cell it is. Yes.

JUDGE JURGOVAN: Thank you.

MS. ZHONG: Okay. And if Your Honors want to have additional evidence as to why a POSITA would understand a bank address is received, go to Exhibit 105, Paragraphs 10, 11 and 19. Which teaches that a control is used to, for controlled command such as read, write, refresh. And what are those command signals? If we go to the command truth table, bank address is, again, one of them.

Your Honors may ask, well, you said that Exhibit 1029 is talking about the DRAM, not the memory. JEDEC style ones, the, what's received by the DRAM is similar to the signals that's received on the DIMM level. I'm showing you Exhibit 1032, Page 11.

JUDGE JURGOVAN: Counsel, one minute. You can continue but you --

MS. ZHONG: Okay.

JUDGE JURGOVAN: -- would be getting into your Surrebuttal time.

MS. ZHONG: Yes, I will cover one thing quickly. As to why the, why I'm focusing on the, focusing on the JEDEC style ones.

We know a POSITA would understand the 244 provisional -- JEDEC style ones because of several reasons. One is, paragraph 1 is talking about using DRAM in connection with a personal computer. And Dr. Wolfe has confirmed, at the time of the invention, that disclosure would indicate to them DDR2 and DDR could be at issue.

Paragraph 2 of 244 provisional using, with the use of the word rank is again indication it's a JEDEC style memory module at issue. 64-bit, 72 bit, Dr. Brogioli has testified, in paragraph 19 of his deposition, of his declaration, that that's indicative of a JEDEC style memory module.

So what I want to say is the 244 provisional, through all those disclosures, as would be understood by a POSITA, they would understand this is a JEDEC style signaling protocol. They would understand by the express disclosure in exhibit, in Paragraph 5, address signal is part of the control signal and it would understand because the control signal is used for read, write, active, bank address would be part of that control signal.

As they would be understood from the general signaling, the address signaling protocol alone, bank address would be part of the addressing signals. And bank address signals, all the row bit address signals would be used to differentiate different density of memory devices.

I will stop there and reserve the rest of my time for rebuttal. Thank you, Your Honors.

JUDGE GALLIGAN: Counsel, this is Judge Galligan, I have one quick question for you.

MS. ZHONG: Sure.

JUDGE GALLIGAN: You mentioned Dr. Brogioli's testimony regarding the Verilog code. I just want to confirm, is that Paragraphs 36 through 43 in the Declaration?

MS. ZHONG: Can I check that during the break and get back to you on that?

JUDGE GALLIGAN: Yes.

MS. ZHONG: Okay.

JUDGE GALLIGAN: Thank you very much.

MS. ZHONG: Okay.

JUDGE JURGOVAN: Okay, at this point we can take a break for five minutes, if the parties would like to do that. If not, we'll just continue with rebuttal?

MR. CHANDLER: I'm ready for rebuttal, unless Your Honors would like a break.

JUDGE JURGOVAN: Counsel for Patent Owner?

MS. ZHONG: We can take a break. Five-minute break.

JUDGE JURGOVAN: Okay. Yes.

MS. ZHONG: If you don't really mind taking a break.

JUDGE JURGOVAN: We'll take a five-minute break and resume at, let's see here, 11:50 Eastern time.

MS. ZHONG: Thank you, Your Honor.

(Whereupon, the above-entitled matter went off the record at 11:46 a.m. and resumed at 11:50 a.m.)

JUDGE JURGOVAN: We are ready to begin with Surrebuttal when you're ready.

MR. CHANDLER: Thank you, Your Honor. I'd like to start first with the question of the Verilog code. Are you able to see Slide 27 that I have on the screen, Judge Jurgovan?

JUDGE JURGOVAN: Yes, we are.

MR. CHANDLER: All right. So the question from Judge Galligan was where Dr. Brogioli talks about the Verilog code. And that is shown, for example, on Netlist's Slide 100, which quotes from Paragraph 40 of Dr. Brogioli, his Declaration.

This is just one citation in the Patent Owner Response. This is not explained in the Patent Owner Response, there is just a citation to this paragraph.

One thing to point out though, is if you look at the top of paragraph 40 in the first sentence, Netlist's expert, Dr. Brogioli admits in the first sentence that the Verilog code in Example 2 transmits the command to both Rank 0 and Rank 1. That's contrary to the last limitation of Claim 16 requiring that the command signal is transmitted to only DDR memory device at a time.

So even under Dr. Brogioli's analysis, the Verilog code in Example 2 wouldn't satisfy Claim 16. Furthermore, if you look at our Slide 27, to Judge Galligan's question, which was, how do I know where the FET switch is located, the Verilog code does not tell you where the FET switch is located, the Verilog code just tells you when to enable to FET switch.

If you want to know where the FET switch is located you have to look at the schematics. And as Figure 6 of the 912 patent that shows you where the FET switch is located. And specifically Figure 6b on the right side of our Slide 27, is the example that's discussed in the Specification, which is quoted on the left side of Slide 27.

And it's very clear, the only FET switch that is shown anywhere in a 912 patent is on the data path. There is FET switches in Figure 6b on the DQS strobe line, there are alternative embodiments that also include a FET switch on the DQ data line, but the key is to have the switch on the DQS strobe line because that's how you solve the back-to-back adjacent read command collision problem, which is discussed in the upper left and the bottom left, on Slide 27. Is you need that FET switch to switch between the upper fork in the road and the bottom fork in the road so that the DQS strobe from one rank does not collide with the strobe from the other rank.

There is also the question from Judge Jurgovan about, how do I know what this Verilog code is related to. It's not related to column 8, Line 47. As you can see in the upper left of our Slide 27, the Specification at Column 14, Lines 8 through 14 explains that the Verilog code, Examples 1 and 2, includes logic to reduce potential problems due to back-to-back adjacent read commands, which is abbreviated BBARX.

And then when we go to Column 24, starting at Line 39, that's the discussion of the BBARX collisions and what the solution is. And the solution are the FET switches in Figure 6b. So all the Verilog code tells you is when to enable and disable the FET switches on the DQS strobe line. There is no disclosure of ever using FET switches on the command line.

There was a statement by opposing counsel that DQS can sometimes be considered a command signal. That's incorrect, as shown on the bottom right of Slide 17. According to the JEDEC standard the commands are defined by CS, RAS, CAS, WE and CKE. DQS strobe is not a command signal, it's related to the data lines and data path. The command signals are defined by CS, RAS, CAS, WE, and clock enabled.

Any follow-up questions on that issue?

JUDGE GALLIGAN: Yes. This is Judge Galligan.

MR. CHANDLER: Yes.

JUDGE GALLIGAN: I had a question about that last point you just raised. I was going to look back at the patents because we're construing these claims in light of the patent.

MR. CHANDLER: Yes.

JUDGE GALLIGAN: I thought the patent defined CAS signals as address signals, not command signals, in Columns 6, Lines 55 to 61?

MR. CHANDLER: Let me go to where you're looking. You said Column 6, 55?

JUDGE GALLIGAN: Yes.

MR. CHANDLER: CAS is – column address signal is not CAS.

JUDGE GALLIGAN: They call it a strobe.

MR. CHANDLER: Is that what you're getting at?

JUDGE GALLIGAN: Yes. It's called a strobe, right. Okay, great.

MR. CHANDLER: Yes. Yes, there is a difference. Yes.

JUDGE GALLIGAN: Okay, thanks.

MR. CHANDLER: All right. There was a related point sort of on claim construction where opposing Counsel was making the argument about, and there was some discussion with Judge Galligan about triviality and so forth. But this also ties into what was the meaning in the reexamination where the Board was talking about transmitting the command to only one signal at a time when there are multiple memory devices in Amidi.

And this, I just want to remind the Board, this was discussed in the Institution Decision on Page 47, in the middle. This is the same argument

that Netlist made in their Preliminary Response, that they also made today. And the argument goes that Claim 16 requires sending a command to a single device at a time even though there are multiple devices in each rank.

As the Board correctly recognized that's false. Because the claim construction of rank includes just one memory device and therefore you don't need to satisfy Claim 16 with the rank, with multiple memory devices, you can satisfy Claim 16 when there is just one memory device in the rank. And in fact, you know, our contention is that's the only disclosed embodiment in the patent is when there is just one memory device in the rank, as we discussed in our Slide 22.

Now turning to Perego, there was some discussion, for example, on Netlist Slide 19, that Perego only uses address signals for selecting a target channel and therefore you wouldn't need Chip Select signals and you wouldn't need rank multiplication and you wouldn't need anything. That's incorrect, because as shown on our Slide 58, on the bottom left, Perego discloses DDR2 memory devices as an embodiment.

Netlist focuses on the Rambus memory devices, and Rambus signaling, which is one embodiment of Perego. But Perego also has a different embodiment, which is the JEDEC style DDR2 memory devices. And when you have JEDEC style DDR2 memory devices it's undisputed that JEDEC requires a Chip Select signal. And in fact, if you listen to the argument from opposing Counsel about the 244 provisional, there were a lot of omissions about obviousness.

Opposing Counsel was relying heavily on the JEDEC standard to try to show that the 244 provisional shows things like bank address and Chip

Select and so forth. Those were admissions that is obvious when you have a DDR2 memory device that you need a Chip Select signal.

Now those admissions are insufficient for Section 112 priority because they need to show a written description, that can't just rely on obviousness. So they need to show a written description of bank address signals, they need to show a written description in the 244 provisional of DDR memory devices, which is nowhere in the 244 provisional.

But we agree with them that it would be obvious that if you had a DDR memory device that there would be Chip Select signals. And therefore in the embodiment of Perego with DDR memory devices you can't just use the address bit to select more ranks, you need to also use the Chip Select signal. And that's what's discussed on this Slide 58. It's also discussed, for example, on our Slide 61. This gets into the issue of the RQ control lines.

Again, Perego does have an embodiment about Rambus, but then he has this alternate embodiment discussed on the bottom left of Slide 61. And Perego says, in alternate embodiments control lines RQ may comprise individual control lines. In this embodiment, which corresponds to the JEDEC DDR2 embodiment, you don't have packets, you don't have Rambus memory devices, this corresponds to JEDEC DDR2 memory devices that have RAS, CAS and Chip Select.

And as shown on Slide 62, we know that the alternate embodiment where RQ has individual control lines refers to JEDEC and not to Rambus, because if we look at Rambus, which is shown in the upper right, Rambus does not disclose individual row address strobe, column address strobe. That's not in the Rambus standard. Row address strobe and column address

strobe is part of the JEDEC standard where JEDEC has individual control lines.

There was a statement about the burden of production for --

JUDGE JURGOVAN: Counsel, can I interrupt for one second?

MR. CHANDLER: Yes.

JUDGE JURGOVAN: And that is, do the Chip Select signals in DDR have to be used?

MR. CHANDLER: Yes, they do because it's required for the command. If you don't have the Chip Select signal nothing works. So if you look for example on Slide 17 in the bottom right, every single command requires a Chip Select signal. And that signal needs to either be high or low otherwise the device isn't going to know what to do.

So if you cut off the Chip Select signal and that signal was just floating, you get garbage because the memory device wouldn't know whether to act or to do nothing. To do nothing, which is a device deselect, you need a Chip Select signal that's not asserted. And this is CS overbar, which means a high signal indicates that the Chip Select is not being asserted whereas a low voltage indicates the Chip Select signal is being asserted.

So that memory device needs to know every clock cycle, am I supposed to do something or am I not supposed to do something. And the way the device knows is from the Chip Select signal. So the Chip Select signal is essential in a JEDEC style memory device. And of course, as always, don't take my word for it. Slide 25, right in the middle, quoting Exhibit 1034, the Jacob paper at Pages 2 to 3. The very top. The last bus,

the Chip Select bus, is essential in a JEDEC style memory system. You need the Chip Select bus.

JUDGE JURGOVAN: So, in other words, when Perego says that its translator connects to DDR devices, that implies that the chip signal is there?

MR. CHANDLER: Correct.

JUDGE JURGOVAN: That's being generated by the translator. Thank you.

MR. CHANDLER: Yes. And it would certainly be obvious.

JUDGE JURGOVAN: Thank you.

MR. CHANDLER: There was a statement about the burden on priority. And the opposing Counsel essentially said that our Petition needed to spell out all of the deficiencies in the 244 provisional and the 346 patent. And that's not the correct statement in the law.

So the Institution Decision provided the correct statement of the law which is, that under Dynamic Drinkware, once we point to Ellsberry as prior art, then the burden shifts to Patent Owner at that point. And therefore in the Patent Owner Response, Patent Owner needs to provide support for each limitation in the 244 provisional, or the 436 patent if they want to rely on that.

JUDGE JURGOVAN: One minute, Counsel.

MR. CHANDLER: Thanks. And so I just wanted to bring the Board's attention to this recent case from the Board. December 5th, 2023, on Page 28 where the Board stated that Petitioner was not required to rebut, in advance, Patent Owner's arguments and evidence alleging priority to the 421 application.

Under Dynamic Drinkware there is a shifting burden. We just had to raise the issue, then they had the burden. In this case it's Continental Automotive versus Intellectual Ventures, IPR2022-00972, Paper 49.

There was also this statement about Dr. Wolfe and his testimony. And about, again, this is back to Perego and whether address signals alone would be sufficient. And Netlist did not provide the complete context of that testimony in its slide. So there is testimony, or the colloquy is from Pages 202 through about 204 of Exhibit 2103. And so you can see, starting at Line 8, there is some questions about Perego, Column 15, Lines 37 to 40.

And at Line 24 Dr. Wolfe made clear, I don't think you would enable specific devices based on address bits alone. And that's because in a DDR style memory device, as I just discussed with Judge Jurgovan, you need a Chip Select signal, you can't select based only on the address. And this is also seen on our Slide 25, in the green highlighting.

The address signal goes to all the memory devices. All the memory devices in JEDEC receive the same address signal. The only way you can distinguish between ranks of memory devices is with the Chip Select signal. And that's why the Chip Select signal is so essential in a JEDEC style layout.

Last point I'll make was about bank address and the 244 provisional. And if we put up our Slide 62. Actually no, I'm sorry. Our slide -- I'll go here, our Slide 82. The key point here is that, yes, bank address signals need to go to the memory devices, on the far right of Figure 1, but the claim language requires the bank address to go to the logic element. And the Claim requires the logic element to use the bank address for rank multiplication.

And that's what's missing from the 244 provisional is this ASIC decoder in the middle, there is no teaching of a bank address going to the ASIC decoder or rank multiplication. And furthermore, the claim requires more than just a bank address, it requires a row column address and a bank address. And so at most what Figure 1 shows is one address signal. It certainly doesn't say bank address signal, it just says one address signal going to the ASIC decoder. But there is no disclosure of a bank address signal, plus a row column address going to the logic element to perform rank multiplication.

And if you look at Slide 81, again, the bank address signals, which are highlighted in red on the left in the 912 patent, they are conspicuously missing from the 244 provisional. Any questions from the Board? All right, thank you for the opportunity to be heard.

JUDGE JURGOVAN: Thank you. We'll hear from Patent Owner's Counsel for 17 minutes.

(Pause.)

MS. ZHONG: Thanks, Your Honor. Let me share my presentation again. So I will start from the last point. Counsel just said the 244 provisional does not disclose the ASIC using more than the one address signal. That is not correct. What is shown in Figure 1 on Slide Number 61 is the ASIC specifically has, as its input, CS0, CS1. Those are Chip Select signals.

A_{n+1} is undisputed, it's a row of column address signals. Also received by the ASIC decoder is the control signals. So the question, as we pose, is whether a POSITA would understand, based on the totality of the disclosure of 244 provisional, as well as background knowledge, the control

signal would include bank address signals. And we have found, in detail, why they would understand it.

Now, it is not about obviousness it's about what a POSITA would have understood based on the knowledge. The knowledge is, the state of the knowledge is, DRAM at the time of invention accounts for 90 percent of the production at the time.

So by disclosing DRAM and characteristic language as rank by 64 by 72, a POSITA would understand. The invention of the 244 is directed, at least, at JEDEC style memory modules. And that is why we brought in a lot of the disclosures from JEDEC Specification. That's because that's part of the background knowledge that the inventors do not need to repeat again. This is different than Perego.

Perego is a Rambus pattern. Rambus, as a POSITA would understand, has a completely different architecture. You cannot lift what is in JEDEC and assume that a POSITA would have the same understanding as to what a Rambus architecture would disclose.

Now, regarding translation, we agree that the DDR device needs to have a valid voltage on the Chip Select signal. That's true. But that has said nothing about what is the input to the translator or the buffer device. What's, all is needed is a back end. The output signal needs to have a valid Chip Select signal. It says nothing about what the input is.

In fact, you can think of scenario where one speed buffering device knows that the back end is DDR device, or DDR device, it could just generate a valid active signal to select all of them. And depends on other signals to determine which one will be selected.

Sorry, my jumping is not working right now so I have to go through the slides one-by-one. Okay.

(Pause.)

MS. ZHONG: Excuse me, Your Honors, let me go back to the non-presentation mode and I will go to that slide. So Slide 64, which is the command truth table.

True, the Chip Select is needed, but it's generally, except for when its device speed select it's usually just low. So it can be set to low always. And when you don't want to select it you can select the no op (no operation), as described in Ellsberry, and use the other RAS, CAS signals to indicate they are not selected. Do anything.

So what I'm trying to say here is, you do have to have a valid Chip Select signals, but that Chip Select signal is generally locally in Perego. The input signals don't have to have Chip Select information at all, it's just generated locally based on the address information that's inputted, outputted, or received from the host.

(Audio interference.)

COURT REPORTER: I'm sorry, your audio is breaking up.

(Pause.)

MS. ZHONG: It's not showing up. So if Your Honors can go to Exhibit 1034. And go to Page 9, second column. The right-hand column.

The Counsel just mentioned RAS and CAS is JEDEC SDRAM specific. That is not true. If you take a look at the column, the right-hand column of Exhibit 1034, RAS and CAS actually is also used, for example, in asynchronous DRAMs. Which is not DDR devices at all. So RAS and CAS

is not indicative of DDR devices, or the use of Chip Select for that matter, because asynchronous DRAMs do not use Chip Select signals.

And I also wanted to discuss briefly about the Verilog. I understand it is very confusing, but Counsel says the FET switches are only used with the DQ lines and the DQS lines. It is true in Verilog Number 1. And I am showing you Page 30. Verilog Example Number 1, the last few.

You can see that there it's specifically mentioned it's DQ FET enabled versus DQD FET enabled. In Example Number 1. Example Number 2, which we are relying on, don't have that limitation. And I'm showing you here. The paragraph here. It just says, ENT FET A at four enable FETs. And it is part of the language starting with RD0 NWR. So it cannot be talking about DQS and DQ in this context.

JUDGE GALLIGAN: Counsel, this is Judge Galligan. I want to follow up on that. So I just want to clarify. The testimony from Dr. Brogioli that you referred to --

MS. ZHONG: That is --

JUDGE GALLIGAN: -- is that, that's Paragraph 36 to 43 that we should --

MS. ZHONG: Yes, 36 --

JUDGE GALLIGAN: -- look at?

MS. ZHONG: Yes, 36 to 43. And most of it is going to be 37 to 43. That's correct.

JUDGE GALLIGAN: Okay, so I wanted to ask you about that. Petitioner pointed out that in paragraph 40 of Dr. Brogioli's testimony, he says that a command is transmitted to both ranks in Example 2. So how does that meet the limitation that it's only transmitted to one device?

MS. ZHONG: Okay. If, actually, if you read on to paragraph 40 it says, at the end of it, it says, providing for the selective enabling or disabling of FET switch associated with memory device A or memory device B, Example 2, how to transmit a command to a single memory device on a physical rank of multiple memory devices. Let me see whether I can get the sharing to work this time.

JUDGE GALLIGAN: I see that. And I was reading from elsewhere in, this is Judge Galligan, sorry.

MS. ZHONG: Yes. Under --

JUDGE GALLIGAN: Go ahead.

MS. ZHONG: Sorry.

JUDGE GALLIGAN: In page, in paragraph 40, if you go --

MS. ZHONG: Yes.

JUDGE GALLIGAN: -- up a bit in your screen.

MS. ZHONG: Yes. Understood. That's the beginning. But I think it's not worded eloquently. I think what the idea is, is that the selection is the Rank 0 and only Rank 1 will be selected. But the idea is how, he is trying to show how the code is actually showing you. Even when there are multiple devices per rank, the use of the FETs enables you to transmit a command to only device at a time. That's the conclusion for his paragraph 40. The end of paragraph 40.

So he is saying, by providing for the selective enabling or disabling the FET switch associated with memory device A or B, Example 2 teaches how to transmit a command to a single memory device on a memory rank of multiple memory devices. So --

JUDGE GALLIGAN: This is Judge Galligan. I want --

MS. ZHONG: -- I apologize --

JUDGE GALLIGAN: Yes, that's what I wanted to ask you about. So if you scroll up to earlier in paragraph 40 --

MS. ZHONG: Yes.

JUDGE GALLIGAN: -- after that first sentence that we just talked about.

MS. ZHONG: Yes.

JUDGE GALLIGAN: It's part of the first sentence. It's a colon. So it says that, he uses an example.

MS. ZHONG: Yes.

JUDGE GALLIGAN: He says, it provides two control signals, this is paragraph 40, specifically for controlling two separate FET switches. You have FET A and FET B. And it says, the corresponding FET A corresponds to one of the memory devices, example memory device A and physical rank 0, and that FET B would correspond to memory devices B and physical Rank 1.

MS. ZHONG: Yes.

JUDGE GALLIGAN: So I'm trying to figure out, that's an arbitrary designation by Dr. Brogioli. So what then, that presumes then there is an A and B in each rank I guess, or is this presenting that --

MS. ZHONG: Yes.

JUDGE GALLIGAN: Okay. So then how does, so what disables memory device B in physical rank 0 then?

MS. ZHONG: So it's the same, right? It's the same signal. You have signal. It depends on which value you assign to the FETs it's going to be enabled, disabled. So here --

JUDGE GALLIGAN: So it's not just enabling or disabling the entire rank?

MS. ZHONG: It's enabling specific, the device. The FET is associated with that particular device.

JUDGE GALLIGAN: And is the device a rank? The entire rank?

MS. ZHONG: No. No. It's the particular device. If you said the FET A associated with memory device A. See, if you have eight devices in their rank, let's say Device A, C, B, whatever, whatever you call it. So the FET is controlling, is only associated with Device A. So you can't control specifically to disable that particular rank. Particular device, yes. While like enabling the other devices. That's his, I mean, that's the whole gist of his explanation in this paragraph. Basically because each FET is associated with a device, that's how you achieve device level control.

There could be like ten devices in the rank, each one of them will have, associated with FET. And depends on whether that FET is enabled, disabled. Command, there is going to be response or no response. That's the explanation there.

JUDGE GALLIGAN: Okay. And I'm just trying to get, I'm just trying to understand this a little more. So the actual, the patent that talks about Example 2 in, I think Dr. Brogioli talks about it, it's in Column 17 to 18, in the middle there. It says, the exemplary code of Example 2 corresponds to a logic on 40 which receives one gated CAS signal, and the computer system generates two gated CAS signals.

So I'm trying to figure out, if the two gated CAS signals are two, and then there are two FETs, but there are multiple devices in each rank, and there are two ranks. So let's say there are at least two devices in each rank --

MS. ZHONG: Yes.

JUDGE GALLIGAN: -- that would mean you would need four FETs but the code only accounts for two FETs, A and B, which suggests to me that this is actually talking about selecting a rank.

MS. ZHONG: No, because the code is just logic. You can implement it for each one of them. So each of the FETs you can have it run the logic. So the RTL code is very, it's just logic level code.

JUDGE GALLIGAN: Right. So, this is Judge Galligan, let's assume I agree with all that, then you've enabled a FET, you've enabled one device and one memory, and you've disabled one device --

MS. ZHONG: The other ones.

JUDGE GALLIGAN: -- and another --

MS. ZHONG: Yes. The other ones. And you can repeat that for all the other ones. So you achieve individual control on that level, that way. That's the whole idea. You don't repeat it because it's already on the individual level. All you have to do is to repeat that whole, the code for the other ones as well. You don't --

JUDGE GALLIGAN: Well I, this is Judge Galligan. I understand you could do that, I'm just trying to figure out in the context of the patents if you were, if this is actually just talking about a single device rank is all.

MS. ZHONG: I don't believe so, I think, because if you look at the invention, right, let me stop sharing this one and let's go back to what I actual want to show. The, my presentation. Let me see. Looks like I've lost it.

JUDGE JURGOVAN: Counsel, you've got just the one minute left here.

MS. ZHONG: Okay.

JUDGE GALLIGAN: And this is Judge Galligan, we don't need to belabor this point if you have other points to make.

MS. ZHONG: Okay. Yes, I do have other points to make. And I think a very important point is, I want to point Your Honors to, I'm having trouble sharing right now, so let's just go to my presentation, Slide Number 103.

What I want to point to is Figure 1c and the related disclosure. You will see that Figure 1c is showing as if it's a single device rank on memory module 10. But if you read it more closely, of the rest of disclosure which talks about programs to describe the pair of 525 -- 512-Megabit memory devices, a pair of 1-Gigabits, but then the very next example, it says, for example, is to fabricate 1-Gigabit memory module with multiple devices per rank.

So even though Figure 1c may be showing as if there was only a single device per rank, if you read in the context it is very clear that it is talking about multiple devices per rank which means there is nothing in 912 patent ever suggesting a single-rank device. And that also has implementation for the Ellsberry disclosure. Because if Your Honors remember, the Ellsberry disclosure that they rely on are Figures 10 through 13, which seems to suggest it's talking about the entire device. The memory. But it is not.

It is, again, it's showing one slice of the entire memory module. So if we go to Slide 120 of this presentation, Your Honors found, in IPR2018 - 00362, that Figure 13 is, actually shows part of the memory module even though Figure 13, which is similar to Figure 12, is showing that one end

ASIC and one switch ASIC, one control ASIC, with some portion of the memory device. It's, again, it's showing one part, it's not the entire part.

And the next slide, Slide 121, Exhibit 2061 in IPR2022-00063, the Institution Decision, Your Honors found that Petitioner, Samsung themselves, stated Figure 13 is actually describing nine 8-bit memory devices per rank even though it shows only a single one. Again, evidence in the understanding that Figures 10 through 13 are only showing a part of Figures 2 and 5 and 6.

And then if we go to Slide number 117, just look at the description of Figure number 6. Even though Figure 6 indisputably is showing multiple devices per rank, but the description is, again, was in reference to Figure 11 that shows a single rank. Only a slice of it.

So Figures 10 and 12 must be read in the context, not as a complete module but a slice of module. And with that understanding Ellsberry is disclosing multiple devices per rank. And Petitioner pretty much conceded there is no reason to transmit only a single command to a device at a time.

And there is also the understanding that Ellsberry is JEDEC. But by eight, by four devices, memory devices that rely on for Figures 10 to 12, those were not known at the time of the invention. And that's admitted by Dr. Wolfe and Dr. Subramanian. And their testimony is shown on Slides 126 to 128.

A POSITA read Ellsberry, where is their knowledge of what was known, what is not known. They would read Ellsberry as including multiple devices per rank, not a single device rank. And --

JUDGE JURGOVAN: Counsel, if you could conclude your arguments that would be appreciated.

MS. ZHONG: Okay. Thank you very much, Your Honors. So our position is that Perego is disclosing a completely different architecture that does not require rank multiplication, has no rank, has no Chip Select input signals. And there is no reason for a POSITA to actually change that fundamental architecture to go to the JEDEC style architecture. Ellsberry is not prior art. Ellsberry does not disclosure single device ranks.

With that, I conclude my presentation. And thank you very much, Your Honors, for your patience.

JUDGE JURGOVAN: I want to thank the Counsel for their presentations. At this time the Judges will leave. We're now adjourned.

(Whereupon, the above-entitled matter went off the record at 12:30 p.m.)

PETITIONER:

Eliot D. Williams
Theodore W. Chandler
Ferenc Pazmandi
Eric J. Faragi
Brianna L. Potter
BAKER BOTTS LLP
eliot.williams@bakerbotts.com
ted.chandler@bakerbotts.com
eric.faragi@bakerbotts.com
brianna.potter@bakerbotts.com
dlsamsungnetlistiprs@bakerbotts.com
Matthew A. Hopkins
WINSTON & STRAWN LLP
mhopkins@winston.com
Winston-IPR-Netlist@winston.com

PATENT OWNER:

Hong Annita Zhong
Phillip Warrick
Jason Sheasby
IRELL & MANELLA LLP
hzhong@irell.com
pwarrick@irell.com
jsheasby@irell.com