UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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SAMSUNG ELECTRONICS CO., LTD
Petitioner.

v.

Netlist, Inc.,
Patent Owner.

_____

Case IPR2022-00064
Patent No. 10,474,595

_____

PATENT OWNER NETLIST'S NOTICE OF APPEAL

Pursuant to 35 U.S.C. §§ 141, 142, and 319, and in accordance with 37 C.F.R. §§ 90.2-90.3, Patent Owner Netlist, Inc. ("Netlist") appeals to the United States Court of Appeals for the Federal Circuit from the Final Written Decision of the Patent Trial and Appeal Board ("Board") entered on May 9, 2023 in IPR2022-00064 (Paper No. 54) ("Final Written Decision"), attached as Exhibit A, and from all underlying findings, determinations, rulings, opinions, orders, and decisions regarding the *inter partes* review (Case IPR2022-00064) of U.S. Patent No. 10,474,595 (the "595 Patent").

In accordance with 37 C.F.R. § 90.2(a)(3)(ii), Netlist states that the issues on appeal include, but are not limited to: the Board's determination that Claims 1-24 of the '595 Patent have been shown by a preponderance of the evidence to be unpatentable, the Board's denial of Patent Owner's motion to exclude, the Board's procedural rulings, including its rulings regarding the adequate and timely preservation of certain of the parties' arguments; the adequacy of the Board's consideration of the expert testimony, prior art, and other evidence in the record, including, but not limited to, evidence and testimony from related district court proceedings between Petitioner and Patent Owner; the Board's factual findings, conclusions of law, or other determinations supporting or related to those issues (such as motivation to combine or reasonable expectation of success); the adequacy of the Board's consideration of prior IPR proceedings concerning the challenged

claims, including the Board's prior Final Written Decision finding the challenged claims not unpatentable based on the same or similar prior art and the same or similar arguments and evidence; the Board's application of its policies and procedures; the Board's compliance with the Administrative Procedure Act, including whether the Final Written Decision is arbitrary, capricious, an abuse of discretion, not in accordance with law, or in excess of the Board's jurisdiction, and any procedural irregularities associated with the review proceeding; as well as all other issues decided adversely to Netlist in any orders, decisions, rulings, and opinions.

This Notice of Appeal is being e-filed with the Clerk's Office for the United States Court of Appeals for the Federal Circuit, along with payment of the required docketing fees. In addition, a copy of this Notice of Appeal is being filed simultaneously with the Patent Trial and Appeal Board and with the Director of the United States Patent and Trademark Office.

Respectfully submitted,

Dated: July 14, 2023

/Rex Hwang/

Rex Hwang
SKIERMONT DERBY LLP
633 West 5th Street, Suite 5800
Los Angeles, CA 90071
Tel: (213) 788-4500
Fax: (213) 788-4545
rhwang@skiermontderby.com
Registration No: 56,206

Sarah E. Spires
SKIERMONT DERBY LLP
1601 Elm Street, Suite 4400
Dallas, Texas 75201
Tel: (214) 978-6600
Fax: (214) 978-6601
sspires@skiermontderby.com
Reg. No. 61,501

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6, the undersigned certifies that on July 14, 2023 a copy of the foregoing **PATENT OWNER'S NOTICE OF APPEAL** was served by electronic mail, as agreed to by the parties, upon the following:

BAKER BOTTS L.L.P.
Eliot D. Williams, Reg. No. 50,822
Neil P. Sirota, Reg. No. 3,306
Theodore W. Chandler, Reg. No. 50,319
Ferenc Pazmandi, Reg. No. 66,216
Stephanie C. Kato, Reg. No. 73,814
DLSamsungNetlistIPRs@BakerBotts.com

I also certify that in addition to being filed electronically with the Board, a copy of this Notice of Appeal was deposited with Priority Mail Express on July 14, 2023 for delivery to the Director of the United States Patent and Trademark Office at the following address:

Director of the United States Patent and Trademark Office
c/o Office of the General Counsel
Mail Stop 8
P.O. Box 1450
Alexandria, VA 22313-1450

I further certify that a copy of the foregoing Notice of Appeal is being filed via CM/ECF on July 14, 2023 with the United States Court of Appeals for the Federal Circuit.

/Rex Hwang/

EXHIBIT A

Trials@uspto.gov
571-272-7822

Paper 54
Date: May 9, 2023

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

IPR2022-00064
Patent 10,474,595 B2

Before JON M. JURGOVAN, SHEILA F. McSHANE, and KARA L. SZPONDOWSKI, *Administrative Patent Judges.*

JURGOVAN, *Administrative Patent Judge*.

DECISION
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

A. Background and Summary

Samsung Electronics Co., Ltd. ("Petitioner") filed a Petition (Paper 1, "Pet.") for *inter partes* review of claims 1–24 ("Challenged Claims") of U.S. Patent 10,474,595 B2 (Ex. 1001, "the '595 patent"). Paper 1 ("Pet."). Netlist, Inc. ("Patent Owner") filed a Preliminary Response (Paper 7, "Prelim. Resp.") to the Petition. With our authorization (Paper 8), Petitioner filed a Preliminary Reply to the Preliminary Response (Paper 11, "Prelim. Reply") and Patent Owner filed a Preliminary Sur-Reply (Paper 12, "Prelim. Sur-Reply"). We instituted *inter partes* review under 35 U.S.C. § 314(a). Paper 14 ("Inst. Dec.").

During the trial, Patent Owner filed a Response (Paper 31, "Resp."), Petitioner filed a Reply (Paper 35), and Patent Owner filed a Sur-Reply (Paper 37). Petitioner and Patent Owner requested oral argument (Papers 38 and 39). A hearing was conducted on February 15, 2023. The hearing transcript is entered in the record. Paper 53 ("Tr.").

Petitioner and Patent Owner objected to evidence (Paper 32, 36) and filed Motions to Exclude (Papers 45, 46). The parties filed Oppositions to the respective Motions to Exclude (Papers 47, 48), and further filed Replies (Papers 49, 50) to the respective Oppositions. As discussed below, we dismiss-in-part and deny-in-part Patent Owner's Motion to Exclude, and dismiss Petitioner's Motion to Exclude.

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision is entered pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. Having reviewed the complete trial record, we determine that Petitioner has

shown, by a preponderance of the evidence, that the Challenged Claims are unpatentable.

B. Real Parties in Interest

Petitioner identifies Samsung Electronics Co., Ltd. and Samsung Semiconductor, Inc. as the real parties in interest. Pet. 1. Patent Owner identifies itself as the sole real party in interest. Paper 3, 3.

C. Related Matters

The parties advise that the '595 patent is related to *Samsung Electronics Co., Ltd., et al. v. Netlist, Inc.*, IPR2022-00062; *Samsung Electronics Co., Ltd., et al. v. Netlist, Inc.*, IPR2022-00063; and *Samsung Electronics Co., Ltd. v. Netlist, Inc.*, Case No. 1:21-cv-01453 (D. Del.) ("the parallel litigation"). Pet. 1; Paper 3, 3.

The parties advise that the '595 patent is related to the following legal proceedings, which are no longer pending: (1) *SK hynix Inc., et al. v. Netlist, Inc.*, IPR2020-01042; (2) *Netlist v. SK hynix Inc.,* Case No. 6:20-cv-000194-ADA (W.D. Tex.); (3) *Samsung Electronics Co., Ltd. v. Netlist, Inc.*, IPR2020-01044; (4) *SK hynix Inc., et al. v. Netlist, Inc.*, IPR2020-01044; (5) *Netlist, Inc. v. SK hynix Inc., et al.*, Case No. 8:17-cv-01030 (C.D. Ca.); (6) *In the Matter of Certain Memory Modules and Components Thereof, and Products Containing Same*, Inv. No. 337-TA-1089 (International Trade Commission); (7) *SK hynix Inc., et al v Netlist, Inc.*, IPR2018-00303; (8) *Netlist, Inc. v. SK hynix Inc., et al.*, Case No. 8:16-cv-01605 (C.D. Ca.); (9) *In the Matter of Certain Memory Modules and Components Thereof, and Products Containing Same*, Inv. No. 337-TA-1023 (International Trade Commission); and (9) *SK hynix Inc., et al. v. Netlist, Inc.*, IPR2017-00548. Pet. 1–2; Paper 3, 3–4.

D. The '595 Patent (Ex. 1001)

The '595 patent is titled "Memory Module Having an Open-Drain Output Pin for Parity Error in a First Mode and for Training Sequences in a Second Mode" and is generally directed to "systems and methods for handshaking with a memory module during or upon completion of initialization." Ex. 1001, code (54), 1:24–26.

The '595 patent explains that "[m]emory subsystems such as memory modules are generally involved in the initialization procedure for computer systems." *Id.* at 1:30–32. For example, "the system memory controller may request that the memory subsystem perform one or more requested tasks during system initialization." *Id.* at 1:37–39. However, the '595 patent states that there is no existing method of handshaking between the system memory controller and the memory module during initialization. *Id.* at 2:64–67. As a result, the system memory controller "does not monitor the error-out signal from the memory [module]" and therefore, "perform[s] blind execution." *Id.* at 3:1–3. According to the '595 patent, this has not been a serious issue because the system memory controller "generally has complete control over the initialization procedure." *Id.* at 3:3–8. However, certain configurations have the system memory controller "handing over one or more parts of the initialization operation sequence to the memory subsystem." *Id.* at 3:8–11. In these types of configurations, the system memory controller may insert a waiting period of predetermined length during which it is idle while the memory controller undergoes initialization. *Id.* at 3:16–19. However, this approach has shortcomings in that the time for the memory controller to complete the task may vary and may be longer or

shorter than the predetermined period of time that the system memory controller is idle. *Id.* at 3:19–41.

The '595 patent describes two methods of handshaking between a system memory controller and a memory module: notifying and polling. *Id.* at 3:42–43. In polling, the system memory controller "reads a status register in the memory subsystem controller to find out if the memory subsystem controller has completed the required or requested operation." *Id.* at 3:43–46. The '595 patent explains that polling is "generally inefficient because the system memory controller does not know exactly when the memory subsystem will have completed the required or requested operation." *Id.* at 3:48–52. Therefore, the notifying method, where the memory controller sends a signal to the system memory controller when it completes the required or requested operation, is described by the '595 patent as advantageous because it allows the system memory controller to execute one or more independent commands while it waits for the notification signal from the memory controller. *Id.* at 3:63–4:1.

The '595 patent describes embodiments establishing a handshake mechanism between the system memory controller and the memory module based upon notification signaling. *Id.* at 4:5–7. For example, Figure 3, depicted below, "shows a host computer system including example first and second memory modules configured to perform handshaking with a memory controller of the host system." *Id.* at 2:42–44.

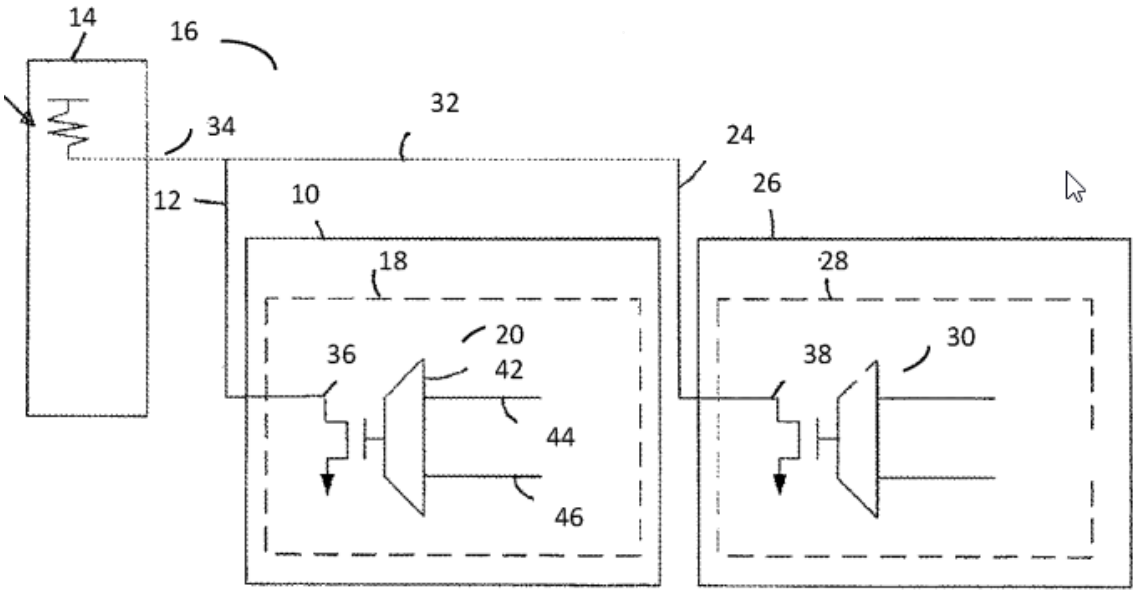

Figure 3

Figure 3, above, depicts host computer system 16, including memory modules 10 and 26, memory controller 14, controller circuit 18, notification circuit 20, and output 12. *Id.* at 11:15–40. "[M]emory module 10 is configured to operate in at least two modes comprising an initialization mode during which the memory module 10 executes at least one initialization sequence, and an operational mode." *Id.* at 4:29–33.

The "at least one initialization sequence may comprise one or more training sequences." *Id.* at 6:2–4. "The operational mode is the normal mode of the memory module 10." *Id.* at 6:45–46. In operational mode, "the system memory controller 14 may cause the memory module 10 to perform standard operations such as memory read/write, pre-charge, refresh, etc., while in operational mode." *Id.* at 6:50–53. Controller circuit 18 "may receive and process address and command signals (e.g., read, write commands) from the system memory controller 14 and transmit appropriate address and commands to the memory elements in response." *Id.* at

5:45–49. Notification circuit 20 is "configured to drive the at least one output 12[,] while the memory module 10 is in the initialization mode to provide at least one notification signal to the memory controller 14 indicating at least one status of the at least one initialization sequence." *Id.* at 4:36–42.

As shown in Figure 3, "the at least one first output 12 is operatively coupled to an error-out pin of the memory module 10, and a multiplexor 42 drives the transistor 36 with either of a task_in_progress signal 44 or an error signal 46 (e.g., parity error signal)." *Id.* at 11:19–23. "[F]or example, the multiplexor 42 may be configured to drive the transistor 36 with the task_in_progress signal 44 when the memory module 10 is in the initialization mode or is executing the at least one initialization sequence, and with the error signal 46 when the memory module 10 is in the operational mode." *Id.* at 11:24–29. The '595 patent explains that "the memory module 10 can be advantageously configured to both perform the standard (e.g., JEDEC-specified) error reporting functionality via the error-out pin during the operational mode and provide the status notification functionality during the system initialization mode." *Id.* at 11:29–34.

E. Illustrative Claim

Among challenged claims 1–24, claims 1, 10, 17, and 21 are independent. Independent claim 1, reproduced below with brackets noting Petitioner's identifiers, is illustrative of the claimed subject matter.

> 1. [1.a] A memory module operable with a memory controller of a host system, comprising:
>
> [1.b] a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge

connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections;

[1.c] dynamic random access memory elements on the printed circuit board;

[1.d] a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection; and

[1.e.i] wherein the memory module is configurable to operate in any of at least a first mode and a second mode;

[1.e.ii] wherein the memory module in the first mode is configurable to perform one or more normal memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections,

[1.e.iii] wherein the memory module in the second mode is not accessed by the memory controller for normal memory read or write operations, and

[1.e.iv] wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences;

[1.f.i] wherein the module controller is configurable to receive via the second edge connections the address and control signals associated with the one or more normal memory read or write operations,

[1.f.ii] wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and

[1.f.iii] wherein the module controller is further configurable to output via the open drain output and the error

> edge connection a signal indicating a parity error having occurred while the memory module is in the first mode;
>
> [1.g] wherein the module controller in the second mode is further configurable to provide information related to the one or more training sequences by driving the open drain output and the error edge connection to a first state or to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state.

Ex. 1001, 14:39–15:21.

F. Evidence

Petitioner relies on the following evidence:[1]

References		Date	Exhibit
Hazelzet[2]	U.S. Patent Pub. No. 2008/0098277 A1	April 24, 2008	1014
JEDEC[3]	JEDEC COMMITTEE LETTER BALLOT, LRDIMM DDR3	November 2009[4]	1015

[1] The '595 patent issued from Application 15/088,115, filed April 1, 2016, now U.S. Patent No. 9,585,218, which is a continuation of Application No. 13/942,721, filed July 16, 2013, now U.S. Patent No. 9,311,116 B1, which is a continuation of Application No. 12/815,339, filed June 14, 2010, now U.S. Patent No. 8,489,837 B1. Ex. 1001, codes (21, 22). The '595 patent also claims priority to Provisional Application No. 61/186,799, filed June 12, 2009. *Id.* at codes (60, 63).

[2] Petitioner contends Hazelzet is prior art under 35 U.S.C. §§ 102(a), (b) and (e). Pet. 24.

[3] Petitioner contends JEDEC is prior art under 35 U.S.C. § 102(a). Pet. 27.

[4] Petitioner contends JEDEC was distributed in November 2009. Patent Owner disputes that JEDEC was distributed. Resp. 8–12. Because we decide the case on other grounds, we do not address whether JEDEC was distributed in November 2009.

References		Date	Exhibit
	Memory Initialization Chapter Proposal		
Buchmann[5]	U.S. Patent No. 8,139,430 B2	Issued March 20, 2012 Filed July 1, 2008	1016
Kim	U.S. Patent No. 8,359,521 B2	Issued January 22, 2013 Filed January 22, 2008	1017

In addition, Petitioner relies on the Declaration of Dr. Donald Alpert (Ex. 1003) and other evidence. Patent Owner relies on the Declaration of Robert J. Murphy (Ex. 2027) and other evidence. The depositions for these experts have been entered into the record. Exs. 2023 (Alpert), 1077 (Murphy).

G. Prior Art and Asserted Grounds

Petitioner asserts that claims 1–24 are unpatentable on the following Grounds (Pet. 4):

Claims Challenged	35 U.S.C. §	Reference(s)/Basis
1–24	103(a)[6]	Hazelzet, JEDEC
1–24	103(a)	Hazelzet, Buchmann
3–7, 12–14, 20, 22, 23	103(a)	Hazelzet, JEDEC or Buchmann, Kim

[5] Petitioner contends Buchmann is prior art under § 102(e). Pet. 28.
[6] The Leahy-Smith America Invents Act, Pub. L. No. 112–29, 125 Stat. 284 (2011) ("AIA"), amended 35 U.S.C. § 103. Although the parties dispute whether the '595 patent is entitled to claim priority to the provisional application (*see, e.g.*, footnote 1; Pet. 5–10; PO Response 12–25), there is no dispute that the '595 patent's priority claim extends to Application No. 12/815,339, filed June 14, 2010. Ex. 1001, code (63). Because the filing date of this application is before the effective date of the applicable AIA amendment, we refer to the pre-AIA version of 35 U.S.C. § 103.

II. DISCUSSION

A. Principles of Law

In an *inter partes* review, a petitioner bears the burden of persuasion to prove "unpatentability by a preponderance of the evidence." *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015) (quoting 35 U.S.C. § 316(e)); *see* 37 C.F.R. § 42.1(d) (2022).

A claim is unpatentable under 35 U.S.C. § 103(a) if "the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) any objective evidence of nonobviousness, i.e., secondary considerations. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

B. Level of Ordinary Skill in the Art

Petitioner asserts a person of ordinary skill in the art "would have had a [B]achelor's degree in computer engineering, or a related field, and several years of additional experience working with computer memory systems. She would have been familiar with computer memory systems and basic CPU architecture documented in the literature, including standards, and generally available in commercial systems, including how computer components access a computer's memory, the role of a memory controller,

the basic operation of memory modules and devices, and the techniques used to couple memory devices to the other components of the computer system." Pet. 10 (citing Ex. 1003 ¶ 55). Patent Owner does not dispute Petitioner's proposed level of skill in the art. *See* Resp. 6.

We find Petitioner's proposal is consistent with the level of ordinary skill in the art reflected by the '595 patent and the prior art of record, and, therefore, adopt Petitioner's proposed level of ordinary skill in the art in this Decision. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).

C. Claim Construction

We construe each claim "in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent," the same standard used to construe the claim in a civil action. 37 C.F.R. § 42.100(b).

The words used in patent claims are interpreted in light of the intrinsic evidence of record, including the written description, drawings, and prosecution history. *Teleflex, Inc. v. Ficosa North America Corp.*, 299 F.3d 1313, 1324 (Fed. Cir. 2002). Absent "express intent to impart a novel meaning to claim terms, an inventor's claim terms take on their ordinary meaning." *Id.* at 1325. There is a heavy presumption that a patent claim carries its ordinary and customary meaning. *Id.*

Petitioner proposes the following constructions:

Claim Term	Proposed Construction
memory read or write operations	operations used to communicate data between the memory module and the memory controller in response to commands from the memory controller
normal memory read or write operations	memory read and write operations
mode	plain and ordinary meaning
training sequence	a set of operations occurring in a particular order and used for training
notification signal associated with the [one or more training sequences] / information related to the [one or more training sequences] / open-drain signals related to the [one or more training sequences]	unscheduled signal/information/open-drain signals provided without polling that indicate the status of the one or more training sequences

Pet. 18–24. Petitioner presents several arguments and support in favor of its proposed constructions. *Id.* Petitioner also contends that "normal memory read and write operations" are the same as "memory read and write operations." Pet. 19–21. Petitioner further argues that the term "mode" does not require construction. *Id.* at 21–22.

Patent Owner agrees that "mode" does not require construction, but disagrees with Petitioner's other proposed constructions, which "deviate from [the] plain and ordinary meaning." Resp. 3–6.

We find that several of Petitioner's proposals improperly alter the language of the respective claims to change their meaning, and also lack support in the intrinsic evidence of record. Petitioner's proposal concerning

"memory read or write operations" states that the data is communicated between the memory module and the memory controller in response to commands from the memory controller. Pet. 18–19. But claim 1 recites that the data signals are communicated "in response to *address and command signals*." Ex. 1001, 14:58–62 (emphasis added). We "cannot construe claims to read an express limitation or element out of the claims." *TDM America, LLC v. U.S.*, 85 Fed. Cl. 774, 787 (2009). We decline to adopt Petitioner's proposed construction. For the same reason, we decline to adopt Petitioner's proposed construction of "normal memory read or write operations" to mean the same as "memory read or write operations."

Since Petitioner and Patent Owner do not dispute the meaning of the term "mode," we apply the plain and ordinary meaning that would be given to the term by a person of ordinary skill in the art. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (only terms that are in controversy need to be construed, and then only to the extent necessary to resolve the controversy).

Petitioner's proposal for "training sequence" improperly introduces the concept of "a set of operations occurring in a *particular order*," which narrows the meaning considerably, and is not supported by the specification or file history. *See* Exs. 1001–1002. To the contrary, this proposal conflicts with the '595 patent, which states "in any method or process disclosed herein, the acts or operations making up the method/process may be performed *in any suitable sequence* and *are not necessarily limited to any particular disclosed sequence*." Ex. 1001, 14:24–28 (emphasis added). We decline to rewrite the claims as Petitioner proposes.

Petitioner's proposal for "notification signal" introduces the requirements of "unscheduled" (mentioned nowhere in the '595 patent or file history) and "without polling." The '595 patent identifies "polling" and "notifying" as different ways of "handshaking" between the Memory Controller Hub (MCH) or system memory controller, and the memory subsystem controller. Ex. 1001, 3:42–43. "Notifying" is described as "advantageous" in the '595 patent, and use of the term "notification signal" in the claims implies "notifying" as described in the '595 patent. *Id.* at 3:63–65. However, the term "unscheduled" in Petitioner's proposal is unsupported by the intrinsic evidence so we decline to adopt Petitioner's proposal.

Neither party avers that the outcome of this case turns on Petitioner's proposed constructions, and we agree. We decline to adopt Petitioner's proposals, and instead give the claim terms their plain and ordinary meanings.

D. Ground 1: Obviousness Over the Combination of Hazelzet and JEDEC

Petitioner contends that claims 1–24 would have been obvious over the combination of Hazelzet and JEDEC. Pet. 30–68. Petitioner and Patent Owner dispute whether JEDEC constitutes a prior art "printed publication" under 35 U.S.C. § 311(b). Pet. 25–28; Resp. 8–13; Reply 2–9; Sur-Reply 2–9. Since we find that other grounds demonstrate unpatentability of all Challenged Claims, we find it unnecessary to address this issue or ground in this Final Written Decision in order to resolve the dispute between the parties.

E. Ground 2: Obviousness Over the Combination of Hazelzet and Buchmann

Petitioner contends that claims 1–24 of the '595 patent are unpatentable as obvious over the combination of Hazelzet and Buchmann. Pet. 30–68. We address Hazelzet and Buchmann and their combination in the following section and conclude that Petitioner has shown claims 1–24 unpatentable for the reasons that follow.

1. Hazelzet (Ex. 1014)

Hazelzet was published on April 24, 2008 and is titled "High Density High Reliability Memory Module With Power Gating and a Fault Tolerant Address and Command Bus." Ex. 1014, codes (43), (54). Petitioner asserts that Hazelzet is prior art under 35 U.S.C. §§ 102(a), (b), and (e). Pet. 24.

Hazelzet is generally directed to a high density, high reliability memory controller/interface. Ex. 1014 ¶ 7. Figure 2, reproduced below, is a block diagram of the enhanced server memory arrangement:

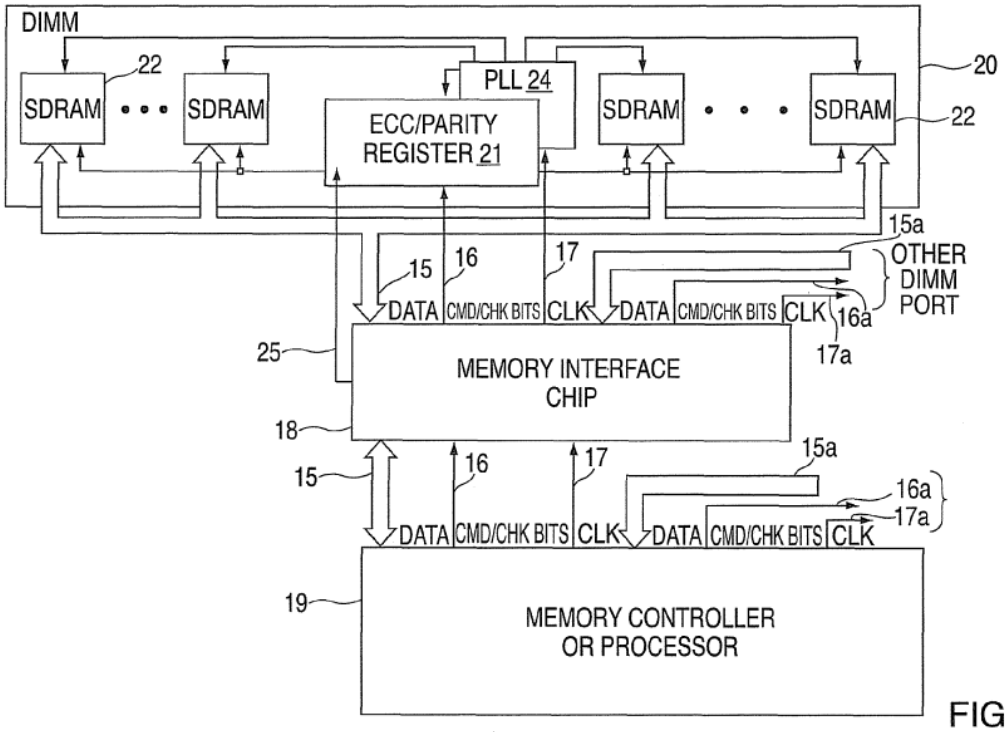

FIG. 2

Figure 2 depicts dual inline memory module ("DIMM") 20 with a "novel ECC/Parity Buffer chip 21" coupled to memory interface chip 18, which is coupled to memory controller or processor 19. *Id.* ¶ 38. Hazelzet describes that "DIMMs are printed circuit cards designed to carry a plurality of DRAMs 22 thereon and the DRAM output pins . . . are connected via the printed circuit to selected connectors 23 along the edge of both the back and front sides of the card." *Id.* ¶ 39. Figure 2 shows "the memory interface chip 18 sends and receives data from the DIMMs via the data line 15 and sends address and commands via line 16." *Id.* ¶ 38. "The memory interface chip 18 then sends and receives data, via line 15, to the memory devices, or DRAMs 22 and sends address and command information to the register chip 21 via add/cmd line 16 and check bits for error correction purposes to the ECC/Parity register chip 21 via line 25." *Id.*

Hazelzet further describes that the DIMM has "added error correction code logic (ECC) incorporated therein for correcting single bit errors while permitting continuous memory operation independent of the existence of these errors." *Id.* ¶ 64. Hazelzet also discloses "[a] parity operating mode . . . to permit the system to interrogate the device to determine the error condition." *Id.* In this way, Hazelzet describes two modes: "ECC Mode (/ECC Mode low)" and "parity mode (/ECC Mode high)." *Id.* ¶¶ 69–70; *see also* Ex. 1014, Fig. 8. In addition, Hazelzet describes error reporting circuitry, where "[t]wo open-drain outputs are available to permit multiple modules to share a common signal line for reporting an error that occurred during a valid command (/CS=low) cycle (consistent with the re-driven signals)." *Id.* ¶ 72. "/Error (CE) indicates that a correctable error occurred and was corrected by the ECC logic, /Error (UE) indicates that an uncorrectable error occurred and depending on the mode selected is an uncorrectable ECC error or a parity error." *Id.*

2. Buchmann (Ex. 1016)

Buchmann was filed on July 1, 2008, issued on March 20, 2012, and is titled "Power-On Initialization and Test for a Cascade Interconnect Memory System." Ex. 1016, codes (22), (45), (54). Petitioner asserts that Buchmann is prior art under 35 U.S.C. § 102(e). Pet. 28.

Buchmann is generally directed to "[a] memory buffer, memory system and method for power-on initialization and test for a cascade interconnect memory system." Ex. 1016, code (57). Buchmann describes that "the memory buffer includes logic for executing a power-on and initialization training sequence initiated by the memory controller." *Id.*

Buchmann discloses that it "is operable in a static bit communication (SBC) mode and a high-speed mode." *Id.* at 1:43–44.

Buchmann describes several training sequences, including training sequence TS0, which "is used to perform upstream (US) and downstream (DS) clock detection and repair (if necessary)." *Id.* at 5:51–53. During this training sequence, the memory module outputs various commands, including TS_done, which "indicates the local and all cascaded MBs are done with TS0." *Id.* at 6:1–20, Table 1. Buchmann also similarly describes other training sequences, TS2 and TS3. *Id.* at 7:15–8:45.

3. Motivation to Combine Hazelzet and Buchmann

Petitioner, with supporting testimony from Dr. Alpert, argues there is sufficient motivation to combine Hazelzet with Buchmann. Pet. 32–40 (citing Ex. 1003).

Petitioner argues that the prior art relied on in the Petition is analogous to the '595 patent both because it is in the same field of endeavor ("memory module design, including error detection and correction, initialization, training and the use of pins/paths for multiple purposes during different operations/modes") and reasonably pertinent to the same problems ("increasing memory module capacity, performance, and/or reliability by sharing an output pin/path to perform multiple functions during multiple operations/modes, including initialization/training"). *Id.* at 32–33.

In the Hazelzet-Buchmann combination, Petitioner relies on Hazelzet to teach memory modules modified to buffer data signals similar to the DDR3 LRDIMM standard, and an initialization mode into which each module could be switched and which includes training sequences whose completion is reported by the memory buffer using a status signal output

over Hazelzet's open drain output (UE 121). Pet. 30 (citing Ex. 1003 ¶ 164). Petitioner relies on Buchmann's TS0 and TS3 training sequences and contends that the open drain output signals signaling training status would be TS0_done and TS3_ack or TS3_done. *Id.* at 30–31 (citing Ex. 1016, 5:51–7:2, 8:24–9:18, Figs. 4, 6). Petitioner explains that Hazelzet's ECC/Parity register would be modified to implement Buchmann's training as part of an additional mode to run, for example, at initialization, to switch among modes when appropriate, and to use the UE 121 open drain output of Hazelzet to communicate the new notification signals. *Id.* at 31 (citing Ex. 1014 ¶ 123; Ex. 1016, 3:49–60). Petitioner contends that Hazelzet already uses the UE 121 open drain output for two different signals in two different modes, and that the ECC/Parity register necessarily includes circuitry for selecting which signal to drive on the UE 121 output depending on the mode of the module. *Id.* Petitioner contends it was well within the level of ordinary skill to modify such circuitry such that it instead selected among three different signals, depending on mode, and contends that "a Skilled Artisan could have made that modification without undue experimentation and with a reasonable expectation of success." *Id.* (citing Ex. 1003 ¶ 167).

Petitioner argues that the combinations are "merely an arrangement of old elements with each performing the same function it had been known to perform and yielding no more than what one would expect from such an arrangement." *Id.* at 33. Petitioner contends the combinations "would have been well within the level of ordinary skill in the art" and "would not have resulted in any unpredictable results." *Id.* This is a recognized reason to

combine under *KSR*, 550 U.S. at 417 (citing *Sakraida v. Ag Pro, Inc.*, 425 U.S. 273 (1976)).

Petitioner also provides arguments for why a person of ordinary skill in the art would be motivated to add training for the data buffers and other components of a memory module, to add training as a separate mode, and to use the same output for the added training mode. Pet. 33–40 (citing Ex. 1003). Petitioner argues that a person of ordinary skill in the art would be motivated to add training to Hazelzet "because it was known that training improved memory module reliability." *Id.* at 33–34 (citing Ex. 1014 ¶¶ 1–4, 7, 42, 44, 123; Ex. 1017, 12:36–53; Ex. 1025, 15–18; Ex. 1027, 1:35–2:12; Ex. 1003 ¶ 172). In addition, Petitioner argues that LR-DIMMs and their initialization were known in the art, and provided increased performance and capacity by adding the LR-DIMM's data buffering functionality to Hazelzet's RDIMM. Pet. 34–35 (citing Ex. 1008, 22; Ex. 1003 ¶ 173).

Petitioner also notes that Buchmann discloses a "training phase that allows more flexibility and improved control data exchange during start-up" to establish "reliable communication" on the bus. *Id.* at 36 (citing Ex. 1016, 3:64–67, 14:5–8, 14:28–35). Hence, Petitioner contends that combining Buchmann's training with Hazelzet improves reliability. *Id.* Petitioner further contends that one of ordinary skill in the art would have been motivated to add the functionality of buffering the data signals and corresponding training to Hazelzet's RDIMM because it was a known, reliable technique which improved performance and enabled higher capacity. *Id.* (citing Ex. 1003 ¶¶ 175–177, 179). Petitioner contends the combination of Hazelzet and Buchmann was well within the level of skill in the art at the time and provided no more than expected at the time, a DIMM

with a buffer to buffer data, address and command signals, and efficient training of that buffer during initialization to ensure optimal read and write performance during normal read and write performance during normal operation. *Id.* (citing Ex. 1003 ¶ 179).

Petitioner argues that a person of ordinary skill in the art would be motivated to add training in a separate mode from normal operation "because it was known that training before normal operation was necessary to minimize errors" in read and write operations. *Id.* at 37–38 (citing Ex. 1016, 12:60–13:41; Ex. 1025, 15–18; Ex. 1022 ¶¶ 32, 52, 88–89, Fig. 4; Ex. 1056, 18, 22, 25–26, 42–44; Ex. 1057, code (57), 2:13–34, 2:60–3:3, 9:11–10:44, Fig. 5; Ex. 1003 ¶¶ 180–182). Petitioner notes that Buchmanns's invention is an "initialization training sequence" that is completed at "power-on," which would suggest to a person of ordinary skill in the art "that training before normal operation is important." *Id.* at 37 (citing Ex. 1003 ¶ 180). Since Hazelzet also initializes upon power-on, Petitioner contends that Buchmann's training complements Hazelzet's initialization. *Id.* at 37 (citing Ex. 1014 ¶ 123; Ex. 1025, 15–18; Ex. 1027, 1:61–2:19, 6:24–25, 10:24–45). Petitioner contends that after updating Hazelzet's buffers to buffer both address and data signals, a person of ordinary skill in the art would have been motivated to combine the references such that training in an initialization mode occurred separate from normal operating modes/operations. *Id.* (citing Ex. 1003 ¶ 181).

Petitioner further argues that it would have been obvious to communicate training status in an initialization mode using the same open drain output already used in other modes/operations. Pet. 38 (citing Ex. 1003 ¶¶ 183–185). Petitioner contends that Hazelzet uses the same open

drain output to indicate an "uncorrectable error" in ECC mode and parity error in parity mode. Pet. 38–39 (citing Ex. 1014 ¶¶ 44, 49, 59, 64, 69, 72, 109, Figs. 4B, 7A; Ex. 1003 ¶ 164). Petitioner contends that this disclosure would have motivated a person of ordinary skill in the art to use the same output in the added training mode because the parity and ECC modes would not be using the open drain output while the training operation was running during initialization. *Id.* at 39 (citing Ex. 1003 ¶¶ 185–186).

Petitioner further notes that a person of ordinary skill would have been motivated because multiple use of a pin was known and would have been considered an efficient use of the limited number of output pins on integrated circuits. *Id.* Petitioner points to Kim as an example of use of an open-drain output on a memory module during multiple modes. *Id.* (citing Ex. 1017, 1:16–22, 5:49–57, 6:8–16). According to Petitioner, Kim discloses, in addition to sharing ECC and parity on the error output pin, that "[i]n alternate exemplary embodiments, other functions also share the error feedback pin." *Id.* (citing Ex. 1017, 6:16–18; Ex. 1003 ¶ 187). Petitioner contends that these disclosures would have motivated a person of ordinary skill in the art to use Hazelzet's UE 121 open-drain output to notify the memory controller that training was in progress or done. *Id.* (citing Ex. 1003 ¶ 188).

Dr. Alpert testifies that a person of ordinary skill in the art would have been motivated to arrange the modified Hazelzet "to communicate signals indicating training completion only when all memory modules have completed that training, in order to ensure that the entire memory system had been trained before proceeding to normal operation." *Id.* at 39–40. As Dr. Alpert explains, "[t]his would permit training to be completed in an

orderly and systematic manner, limiting the complexity of the control circuitry needed to implement the training, while using a known, efficient way to do so." *Id.* (citing Ex. 1043, 7:30–51; Ex. 1017, 5:65–6:12, Fig. 4; Ex. 1014 ¶¶ 18, 109; Ex. 1003 ¶ 189).

Petitioner contends that a person of ordinary skill in the art would have been further motivated to modify Hazelzet as described because Hazelzet's "memory system includes multiple memory modules in need of training." *Id.* (citing Ex. 1014 ¶¶ 18, 109; Ex. 1017, 5:65–6:12, Fig. 4; Ex. 1043, 7:30–51). Petitioner contends the combinations analyzed would "allow any module in the system to pull the open drain pin to 'low' . . . while still executing its training sequence, regardless of whether [the] other modules in the system have completed training and were no longer pulling that pin low, thereby delaying normal operations until the system is completely ready." *Id.* (citing Ex. 1003 ¶¶ 158–163, 190).

Patent Owner argues that Grounds 1–3 fail because a person of ordinary skill in the art would not have combined Hazelzet with Buchmann to arrive at the '595 patent claims. Resp. 28–70. Specifically, Patent Owner argues that each Ground requires redesigning Hazelzet's memory modules to buffer data signals, but that neither Hazelzet or Buchmann provide the motivation for a person of ordinary skill in the art to do so. Resp. 6, 32 (citing Ex. 2027 ¶ 87). Patent Owner argues that Hazelzet's memory modules are incompatible with Buchmann's training until after Hazelzet has been updated with a buffer for both address and data. *Id.* at 32–33 (citing Ex. 2002, 68:19–79:24, 81:18–83:5; Ex. 2019, 49; Ex. 2023, 210:15–18; Ex. 2027 ¶¶ 88–93; Pet. 37). However, Petitioner noted that Buchmann explicitly teaches a memory buffer which buffers both address and data.

Pet. 36–37 (citing Ex. 1014 ¶ 123; Ex. 1016, Fig. 1; Ex. 1025, 15–18; Ex. 1027, 1:61–2:19, 6:24–25, 10:24–45). Patent Owner's argument considers Hazelzet *in isolation* and does not properly consider what one of ordinary skill in the art would have understood from the *combination* of Hazelzet and Buchmann. "Non-obviousness cannot be established by attacking references individually where the rejection is based upon the teachings of a combination of references." *In re Merck & Co.*, 800 F.2d 1091, 1097 (Fed. Cir. 1986) (citing *In re Keller*, 642 F.2d 413, 425 (CCPA 1981)).

Patent Owner argues that Petitioner's grounds require redesign of Hazelzet's memory modules to add Buchmann's memory buffers to buffer data signals, i.e., to change Hazelzet's RDIMM to an LR-DIMM. Resp. 33–35; Sur-Reply 18–20. Patent Owner contends that Petitioner's argument for changing Hazelzet for "increased performance and capacity" is conclusory. Resp. 33. Patent Owner further contends that Petitioner is reaching outside of the ground for motivation, asking to Board to reconstitute its grounds to add the LR-DIMM Design Specification (Ex. 1036), which is improper. *Id.* at 33–34 (citing *Koninklijke Philips N.V. v. Google LLC*, 948 F.3d 1330, 1336 (Fed. Cir. 2020)). Patent Owner further contends the industry debated tradeoffs between LR-DIMMs and RDIMMs, and found RDIMMs less expensive with higher performance compared with LR-DIMMs. Resp. 34–35 (citing Ex. 2027 ¶¶ 94–101).

Patent Owner's arguments do not undermine Petitioner's showing of a motivation to combine Hazelzet and Buchmann. Petitioner has shown sufficiently that UDIMM, RDIMM, FBDIMM, and LR-DIMM modules were known alternatives with known tradeoffs at the time of the '595 patent. Reply 16–20 (citing Ex. 1077, 61:5–10; 98:11–16); Sur-Reply 18–20.

Under appropriate circumstances, such as the need for increased performance and memory capacity, it is clear from the record that one of ordinary skill in the art would have elected to use LR-DIMMs over RDIMMs. Pet. 35 (citing Ex. 1003 ¶¶ 175–177; Ex. 1028 ¶ 31); Reply 20–22. As Petitioner contends, load reduction in LR-DIMMs permits high-speed controllers to drive larger quantities of data and provides for a higher capacity memory module. Reply 21–22 (citing Ex. 2006, 4–5; Ex. 2017 1, 3). Although Patent Owner debates whether an LR-DIMM has "increased performance" over an RDIMM, Patent Owner does not dispute that an LR-DIMM has "increased capacity" relative to an RDIMM. Patent Owner contends that Petitioner's reasons of "increased performance and capacity" for upgrading Hazelzet's RDIMM to the LRDIMM of Buchmann are conclusory. Resp. 33–34; Pet. 33, 35–36. However, Hazelzet explicitly mentions its objectives as a "high density and enhanced reliability memory solution at low cost." *See* Ex. 1014 ¶ 7. Patent Owner does not explain why Hazelzet's enhanced reliability does not serve to increase performance, or why Hazelzet's higher density does not serve to increase capacity.

Thus, Petitioner's proposed motivation to combine is based on the teachings of the references and other evidence. Petitioner does not rely solely on Exhibit 1036 and the remaining evidence is sufficient to establish the motivation to combine Hazelzet and Buchmann. Accordingly, Patent Owner's arguments do not undermine Petitioner's motivation to combine.

Patent Owner argues that Hazelzet suggests an alternative to adding more complex data line buffers to its memory architecture. Resp. 35 (citing Ex. 1014 ¶ 14; Ex. 2027 ¶¶ 102–119, 128–132); *see also* Sur-Reply 21–22. Patent Owner argues that a person of ordinary skill in the art "would have

understood that implementing such a feature would not necessarily have been desired nor the right choice in designing a memory system." Resp. 36 (citing Ex. 2027 ¶¶ 107–114). For instance, Patent Owner contends that "memory modules that buffered data signals had several disadvantages, such as increased complexity, power consumption, and increased costs." *Id.* (citing Ex. 1027, 2:12–19). Patent Owner further contends that training sequences may require bi-directional data and corresponding circuitry which would increase device complexity and cost, and may worsen signal transmission characteristics and therefore reliability. *Id.* (citing Ex. 2027 ¶ 108).

Patent Owner's argument that adding data line buffers to a memory architecture may not be the right choice in designing a memory system in some cases does not negate Petitioner's contention that, in other cases, it would be the most advantageous option considering such factors as performance, complexity, power consumption, and cost. As noted, Petitioner's combination basically uses Hazelzet's RDIMM as a foundation and adds Buchmann's LR-DIMM data buffering and training to create a modified LR-DIMM memory module. Petitioner submitted persuasive evidence that LR-DIMMs are desirable for higher speed and capacity. Pet. 35–36 (citing Ex. 1036, 5; Ex. 1003 ¶¶ 175–179); Reply 21–23 (citing Ex. 2006, 4, 5).

Patent Owner contends that bi-directional data exchange would be *required* by Petitioner's combination, but Dr. Alpert testifies that bi-directional data exchange is a "possibility," not a requirement. Ex. 2023, 245:17–246:10. Furthermore, Patent Owner does not indicate what disadvantage would necessarily result from using bi-directional data

exchange. Resp. 36, 42. The evidence states only that bi-directional exchange "*may* require a disadvantageous addition of circuitry" which "*may* also worsen signal transmission characteristics." Resp. 36, 42–43 (citing Ex. 1027, 2:12–19) (emphasis added); Sur-Reply 22. This falls short of stating that bi-directional data exchange or addition of circuitry is *required* in Petitioner's proposed combination, or that such added circuitry *would* worsen signal transmission. And Patent Owner does not contend that RDIMM is *always* more advantageous than LR-DIMM.

Patent Owner further argues that "Hazelzet teaches that its solution strikes a balance between performance, capacity, reliability, and cost for low or midrange systems, which [a person of ordinary skill in the art] would have understood likely precludes memory modules that buffered data signals." Resp. 36 (citing Ex. 1014 ¶¶ 1–6; Ex. 2027 ¶¶ 115–119). Patent Owner contends that a person of ordinary skill in the art would have understood that Hazelzet's memory system accomplished those goals without requiring additional, more complex hardware, and counsels against doing so. *Id.* at 36–37 (citing Ex. 2027 ¶ 117). We do not discern any disclosure in the cited parts of Hazelzet that precludes buffering of data signals, or the addition of components such as a data buffer. Consequently, we do not agree with Patent Owner's arguments.

Patent Owner further argues that Hazelzet teaches away from more complex memory modules that buffered data signals by "eliminating the need to produce or procure two types of buffer devices or to re-design existing memory modules." *Id.* at 37–38 (citing Ex. 1014 ¶ 14; Ex. 2027 ¶ 118) (emphasis omitted). Patent Owner contends that a person of ordinary skill in the art would be led in a direction divergent from adding more costly

and complex memory components that buffer data signals, contrary to Hazelzet's intended purpose to use "reduced-function memory assemblies" for the "low or midrange server markets." *Id.* at 37 (citing *In re Gurley*, 27 F.3d 551, 553 (Fed. Cir. 1994)). Patent Owner argues that Petitioner's conclusory motivation is driven only by increased performance and capacity, and fails to consider Hazelzet's disclosure as a whole, which balances trade-offs between reliability, performance, capacity, and cost. *Id.* at 37–38.

We agree with Petitioner that Hazelzet does not '"criticize, discredit, or otherwise discourage' memory modules with data buffers." Reply 22; *see Galderma Laboratories, L.P. v. Tolmar, Inc.*, 737 F.3d 731, 738 (Fed. Cir. 2013) (a prior art reference does not teach away if it "does not criticize, discredit, or otherwise discourage investigation into the invention claimed"). To the contrary, Petitioner shows that adding data buffering lowers the load and enhances performance. Reply 22 (citing Pet. 34–35; Ex. 1003 ¶¶ 175–177, 179; Ex. 1077, 84:14–86:21).

Patent Owner further argues that the Petition failed to demonstrate how the proposed combination could have been done. Resp. 38–39. Patent Owner argues that Petitioner makes a conclusory contention that "[s]uch an upgraded LRDIMM would have worked even in Hazelzet's RDIMM platforms (with appropriate BIOS changes)." *Id.* at 38. Patent Owner contends that the document that Petitioner cites as supportive of its contention states that "the controller must have the capability to do address mirroring." *Id.* at 38. Patent Owner contends that "Hazelzet does not have a controller with the capability to do address mirroring." *Id.* (citing Ex. 2027 ¶ 110). Patent Owner further contends that Petitioner does not address the problems associated with LR-DIMMs in the contemporaneous art (such as

complication of memory configuration, mismatch of signals between host and memory interface, and reduced timing margins), or address how a person of ordinary skill in the art would implement LR-DIMMs in Hazelzet. *Id.* at 38–39 (citing Ex. 2007, 1:37–61; Ex. 2008, 2:12–30; Ex. 2009 ¶ 3; Ex. 2010, 4:8–61; Ex. 2027 ¶¶ 111–115). Patent Owner contends each of these problems is associated with the resulting performance and reliability of LR-DIMMs, and associated read and write functionality in normal operation. *Id.* According to Patent Owner, "modifying Hazelzet to implement an LR-DIMM would introduce many problems when performing the read and write operations required by the claims." *Id.* (citing Ex. 2027 ¶¶ 113–114).

Although Patent Owner indicates several alleged problems with LR-DIMMs, LR-DIMMs were known alternatives for RDIMMs like Hazelzet. Reply 22–23; *see also* Ex. 2007, Fig. 2; Ex. 1077, 95:9–96:25; Ex. 2023, 294:5–296:4. Petitioner also notes that "address mirroring" was merely an optional technique for LR-DIMMs that was already standardized for UDIMMs. Reply 22–23 (citing Ex. 1077, 181:8–17, 188:8–11). Patent Owner does not explain why "address mirroring" would be necessary in Petitioner's combination, or why the alleged problems with the LR-DIMMs of Petitioner's combination could not have been overcome by a person of ordinary skill in the art.

Patent Owner also contends that Petitioner's expert previously admitted that his analysis was "not concerned with the physical embodiments and how . . . those structures might be physically modified. . . . I haven't considered what—you know, exactly how those changes would be made." Resp. 39 (citing Ex. 2002, 68:19–69:20; Ex. 2027 ¶ 114). Patent Owner's argument is premised on "physical" or "bodily"

incorporation of the teachings of one reference into the other, which is not the standard by which obviousness is determined. "[I]t is not necessary that the inventions of the references be physically combinable to render obvious the invention under review." *In re Sneed*, 710 F.2d 1544, 1550 (Fed. Cir. 1983) (citing *Orthopedic Equip. Co. v. United States*, 702 F.2d 1005, 1013 (Fed. Cir. 1983); *In re Andersen*, 391 F.2d 953, 958 (CCPA 1968)). We find no error in Petitioner's expert's approach for it is the concepts taught by the Hazelzet and Buchmann that are being combined in the obviousness analysis, not necessarily any physical embodiments.

Patent Owner argues that "the conclusory testimony of Petitioners' expert does not provide an articulated motivation to change Hazelzet's memory modules to add . . . Buchmann's memory buffers, or demonstrate that such combination could even be done." Resp. 39–40 (citing Ex. 2027 ¶ 115). Patent Owner contends that "[c]onclusory statements do not amount to substantial evidence." *Id.* at 40 (citing *TQ Delta, LLC v. Cisco Sys., Inc.*, 942 F.3d 1352, 1358 (Fed. Cir. 2019)).

We do not agree that Petitioner's expert's testimony was conclusory or failed to explain how the combination would be done. Petitioner's expert references the '595 patent, Hazelzet, Buchmann, and other evidence as supporting his testimony and establishing a reasonable expectation of success. Ex. 1003 ¶¶ 167, 170. For example, the Petition specifically identifies that a problem addressed by the '595 patent, Hazelzet, and Buchmann is "increasing memory module capacity, performance, and/or reliability by sharing an output pin/path to perform multiple functions during multiple operations/modes, including initialization/training." Pet. 33 (citing Ex. 1001, code (57), 5:66–6:14, 8:4–48; Ex. 1014, code (57), ¶¶ 7, 69–70,

123; Ex. 1016, 1:7–9, 3:49–60, 4:51–5:50, 12:60–13:41, 14:1–63, 20:20–21:19, 33:45–67; Ex. 1022 ¶¶ 4, 5, 32–33, 52; Ex. 1025, 15–18; Ex. 1027, 1:61–2:19, 6:24–25, 10:24–45; Ex. 1017, 1:16–22, 5:49–57, 6:8–18, 11:20–34, 12:36–53; Ex. 1003 ¶ 169). The motivation to combine may be found in the nature of problem to be solved, leading one to look to references relating to possible solutions to that problem. *Ruiz v. A.B. Chance Co.*, 357 F.3d 1270, 1276–77 (Fed. Cir. 2004).

Patent Owner further argues that Buchmann provides no motivation to combine because "Petitioner points to nothing in Buchmann that would have motivated [a person of ordinary skill in the art] to modify Hazelzet's memory buffer to also buffer the data signals." Resp. 40–41. Patent Owner argues that both references recognize that, "in designing a memory system, various constraints[] including power, performance, and costs[] need to be considered." *Id.* at 41. Patent Owner contends that Buchmann would have recognized that adding the functionality of buffering data signals would require various factors, such as decreased speeds and higher cost. *Id.* at 41. Patent Owner contends that both references considered tradeoffs, but reached two very different solutions for different purposes. *Id.*

Hazelzet teaches a memory module "capable of meeting the *desired* density, performance and reliability requirements." Ex. 1014 ¶ 7 (emphasis added). Similarly, Buchmann teaches that "placing more technology-specific functionality local to the memory subsystem, such benefits as improved performance, increased design flexibility/extendibility, etc., may be obtained, often while making use of unused circuits within the subsystem." Ex. 1016, 32:30–34. Hence, Hazelzet's and Buchmann's

purposes and solutions are aligned with respect to capacity (density, extendibility) and performance, contrary to Patent Owner's argument.

Patent Owner argues that there is no motivation to add a separate training mode in Hazelzet, let alone the specific training of Buchmann. Resp. 41–52; Sur-Reply 22–24. Patent Owner argues that adding training to Hazelzet would have added unnecessary complexity and cost. Resp. 42–44. However, Patent Owner's expert admitted that it was "very well known to one of ordinary skill in the art that there was an initialization mode, and there was a normal mode," for both RDIMMs (like Hazelzet) and LR-DIMMs (with data buffers). Reply 23 (citing Ex. 1077, 110:9–20). Patent Owner's expert further admitted that persons of ordinary skill in the art "knew about the need to train memory modules, including LR-DIMMs, in an initialization mode, especially as the speed of the memory devices increases." *Id.* at 23–24 (citing Ex. 1077, 155:7–22 ("training is required to . . . set the timing optimally so that part can achieve its highest performance and have its best reliability"); Ex. 2027 ¶¶ 104–105). We agree with Petitioner that high-speed operations require training, and that cost and complexity are lesser concerns when high-speed performance is required. *See* Reply 23–24.

Patent Owner further argues that Hazelzet provides no motivation to combine because it is silent regarding training. Resp. 44–47. Petitioner notes that Hazelzet does not exclude training during initialization, and teaches that its initialization will depend "on the available interface busses, the desired initialization speed, available space, cost/complexity objectives, subsystem interconnect structures, the use of alternate processors. . . etc." Reply 24 (citing Ex. 1014 ¶ 123). We agree with Petitioner that Hazelzet is

not limited to any specific initialization, and Buchmann discloses training during initialization, with undisputed benefits for the data buffer. Reply 24–25 (citing Ex. 1016, code (57)).

Patent Owner further argues that Hazelzet and Buchmann teach different solutions to different problems. Resp. 48–52. Patent Owner argues training per Buchmann and error correction code (ECC) are not the same because training seeks to correct errors prior to transmission whereas ECC corrects errors after transmission. *Id.* at 49–50. Petitioner agrees "that ECC is not a substitute for training, and that training would be required for reliable high-speed operations" using data buffers, as discussed above, but, in any event, Patent Owner's argument does not negate Petitioner's motivation to combine. Reply 25.

Patent Owner argues that the Petition relies on hindsight. Resp. 53–58. Patent Owner argues that Petitioner relied on adding training to Hazelzet to "improve reliability" but indicates there would be no reason to implement a memory buffer just to add training to Hazelzet. *Id.* at 53. Petitioner contends that Patent Owner's hindsight argument repeatedly ignores Petitioner's motivation for adding a data buffer to Hazelzet. Reply 25–26. We agree with Petitioner that Patent Owner's arguments do not adequately address Petitioner's reasons to combine. *See* Pet. 32–40. Nor does Petitioner change its argument relative to a previous IPR since it was not involved in that IPR. Reply 26; Resp. 55–57. Patent Owner further argues that Petitioner's expert engages in hindsight by looking at the training sequences to see if any satisfy the claim limitations. Resp. 57. We agree with Petitioner that Patent Owner's assertion takes Petitioner's expert's testimony out of context, and that Dr. Alpert first made the combination

from the point of view of a person of ordinary skill in the art, and then considered whether the combination satisfied the claim language. Reply 26 (citing Ex. 2023, 221:22–222:8, 227:21–228:11). In any case, any judgment on obviousness is in a sense "necessarily a reconstruction based upon hindsight reasoning, but so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made and does not include knowledge gleaned only from applicant's disclosure, such a reconstruction is proper." *In re McLaughlin*, 443 F.2d 1392, 1395 (C.C.P.A. 1971).

Patent Owner contends that all grounds fail because there is no teaching, suggestion, or motivation to use Hazelzet's UE line to communicate training signals. Resp. 58–70. Petitioner contends that the Petition explained the motivation for using Hazelzet's open-drain line for notifications signals in Grounds 1–3, and that Patent Owner's arguments to the contrary attack and mischaracterize the references individually. Reply 26–27 (citing Pet. 38–40). We agree with Petitioner. For example, Petitioner shows that multiple use of a pin was known to communicate error information during a normal mode and training information during a training mode. Pet. 38–40 (citing Ex. 1017, 1:16–22, 5:49–57, 6:8–18; Ex. 1022 ¶¶ 4–5, 32–33, 52; Ex. 1003 ¶¶ 183–190).

Patent Owner contends that Hazelzet describes using a bus to perform initialization distinct from the UE line. Sur-Reply 25. Patent Owner contends that the bus is needed for reporting or responding to operational subsystem information. *Id.* (citing Ex. 1014 ¶¶ 124–125; Ex. 2027 ¶¶ 175–180). Petitioner's combination does not exclude use of a bus—it merely uses the UE line to report training completion. That other

information may be exchanged between the controller and memory module does not negate Petitioner's combination.

Patent Owner further argues that Buchmann does not implement the claimed notification signal with an open drain (*id.* at 26), which is an attack on Buchmann alone without considering its combination with Hazelzet. *See Merck, supra*. Patent Owner's argument that Hazelzet has other unused pins available during initialization (*id.* at 26) does not negate that Petitioner's motivation stems from using a pin that has a dual purpose, suggesting it would also be useful for a separate training mode. And we do not agree with Patent Owner's argument that Petitioner fails to support its contention that use of open-drain signaling was a known efficient way to indicate that all modules had completed training. Petitioner shows that Hazelzet has multiple modules and that normal operations would be delayed until all modules completed training and were no longer pulling the UE pin low. Pet. 40 (citing Ex. 1003 ¶¶ 158–163, 190). And Dr. Alpert relies on evidence in Hazelzet describing use of the open drain UE pin by multiple modules. Ex. 1003 ¶ 190 (citing Ex. 1014 ¶¶ 18, 109). Thus, it is not true his testimony lacked support.

Hazelzet uses the same open drain output UE 121 to indicate "uncorrectable error" in ECC mode and parity error in parity mode. Pet. 38 (citing Ex. 1014 ¶¶ 44, 49, 59, 64, 69, 72, 109, Figs. 4B, 7A). One would have been motivated to use the same output for the training mode/operation separate from the ECC and parity modes. *Id.* at 39 (citing Ex. 1003 ¶¶ 185–186). And multiple use of a pin was known. *Id.* at 39 (citing Ex. 1017, 1:16–22, 5:49–57, 6:8–18; Ex. 1022 ¶¶ 4, 5, 32–33, 52; Ex. 1003 ¶¶ 187–188). Petitioner contends that these disclosures would have

motivated a person of ordinary skill in the art to use Hazelzet's UE 121 open-drain output to notify the memory controller that the training was in progress or done. *Id.* (citing Ex. 1003 ¶ 188). And Dr. Alpert explains that a person of ordinary skill in the art "would have been motivated to arrange the modified Hazelzet to communicate signals indicating training completion only when all memory modules have completed that training, in order to ensure that the entire memory system had been trained before proceeding to normal operation." *Id.* at 39–40 (citing Ex. 1003 ¶ 189). Petitioner contends that this "would permit training to be completed in an orderly and systematic manner, limiting the complexity of the control circuitry needed to implement the training, while using a known, efficient way to do so." *Id.* (citing Ex. 1043, 7:30–51; Ex. 1017, 5:65–6:12, Fig. 4; Ex. 1014 ¶¶ 18, 109; Ex. 1003 ¶ 189).

Patent Owner contends that Hazelzet "teaches away" from using its open-drain UE line during initialization. Resp. 60–63. Patent Owner, however, has not identified any teaching in Hazelzet that "criticizes, discredits, or otherwise discourages" using the UE line during initialization. *See Galderma Laboratories, supra*. Patent Owner's expert admitted that an open-drain output was a simple well-known technique for implementing a logical OR function as a way to indicate whether all memory modules had completed their training using an open-drain line not otherwise used during initialization. Reply 27 (citing Ex. 1077, 178:21–179:25; Ex. 1003 ¶¶ 187–190; Pet. 38–40). Patent Owner argues that Hazelzet discloses only error reporting on the open-drain UE line, but ignores its combination with Buchmann which teaches notifying training status. *Id.* Hazelzet's UE line provides notifications in two different modes, thus motivating a person of

ordinary skill in the art "to use it for the additional function of notifying training completion in an initialization mode when combined" with Buchmann. Reply 28 (citing Ex. 1003 ¶¶ 185–188). We agree with Petitioner that one of ordinary skill in the art "would have understood the advantages of using an open-drain line like Hazelzet's UE line efficiently for the specific task of notifying training completion by all of multiple modules." *Id.* (citing Ex. 1003 ¶¶ 189–190) (emphasis omitted).

Patent Owner argues that Hazelzet discloses using a bus for some initialization tasks. Resp. 61–63. Petitioner contends Hazelzet does not require using the bus, explaining that "[i]nitialization of the memory subsystem may be completed via one or more methods, based on the available interface busses, the desired initialization speed, available space, cost/complexity objectives, subsystem interconnect structures." Reply 28 (citing Ex. 1014 ¶ 123). This statement implies flexibility in how initialization is carried out. We agree with Petitioner that since the UE line was available for training during initialization, it would have been obvious to use the UE line to signal completion of training by a module. *Id.*

Patent Owner further argues that Buchmann does not disclose an open drain for training signals. Resp. 63–67. This is again an attack on the reference individually without considering it in combination with Hazelzet, as proposed by Petitioner. *See Galderma Laboratories, supra.* Petitioner combines Hazelzet with Buchmann such that Buchmann's training completion is communicated through Hazelzet's open-drain UE line, providing obvious advantages. Reply 29 (citing Pet. 30–32, 38–40).

Patent Owner argues that Buchmann's UE line is not open-drain and is not used for training, and that instead a 6-bit bus carries training. Resp.

64–66. Petitioner explains, however, that Buchmann's UE line is not between the memory modules and the memory controller, but is inside SBC receiver circuity, which would have motivated a person of ordinary skill in the art to use Hazelzet's open-drain UE line between the memory controller and multiple modules to indicate in a simple and efficient way that all modules completed training. Ex. 1003 ¶¶ 183–190.

Petitioner contends that Patent Owner crops Petitioner's expert's testimony to create confusion about Dr. Alpert's testimony. Reply 29; Resp. 66–67. Petitioner contends that Dr. Alpert's testimony is consistent that "the memory controller in Hazelzet would be modified to initiate training commands, training sequences like Buchmann does, and that the success or failure of those training sequences would be indicated by a status on the UE signal line that comes back from the module to the memory controller in Hazelzet." Reply 29 (citing Ex. 2003, 121:16–22).

Petitioner further argues that in the final written decision for IPR2018-00303, Paper 42 (Ex. 1034), the Board determined similar limitations in another patent of Patent Owner obvious over the combination of Hazelzet and Buchmann. Reply 30 (citing Ex. 1034, 15, 22). As we address the merits of this case, and determine all challenged claims unpatentable, we do not reach Petitioner's argument that Patent Owner is collaterally estopped in this proceeding by the final written decision in IPR2018-00303.

Patent Owner argues that a person of ordinary skill in the art would not have implemented a notification signal associated with a training sequence via an open drain output because there are at least two other "straight forward" implementations that the references would have instructed a person of ordinary skill in the art to do. Resp. 68–70 (citing

Ex. 2027 ¶ 188). According to Patent Owner, one implementation is to use the memory controller, and not a component on the memory module, to conduct the training. Resp. 68–69. Since the memory controller conducts the training, no notification signal is needed to indicate to it when training is completed. *Id.* In the other implementation, Patent Owner contends that Hazelzet teaches to use a separate, distinct bus, and not the UE line. Resp. 69–70 (citing Ex. 2027 ¶ 190).

That there may be other ways to combine Hazelzet and Buchmann does not negate Petitioner's showing of a motivation to combine in the particular way that Petitioner indicated a person of ordinary skill in the art would have pursued. On this record, we are persuaded that Petitioner has provided sufficient reasoning to combine Hazelzet with Buchmann. More specifically, Petitioner has provided sufficient evidence of motivation to add Buchmann's buffering of data signals to Hazelzet, similar to a DDR3 LRDIMM, because it was a known, reliable technique to improve performance and increase capacity of Hazelzet's memory module. Pet. 35–36 (citing Ex. 1014, code (57), ¶ 36, Fig. 1; Ex. 1028 ¶ 31; Ex. 1036, 5; Ex. 1003 ¶¶ 175–177). Petitioner has also provided the motivation to add Buchmann's training to Hazelzet in order to improve reliability. *Id.* at 34 (citing Ex. 1014 ¶¶ 1–4, 7, 42, 44, 123; Ex. 1017, 12:36–53; Ex. 1025, 15–18; Ex. 1027, 1:35–2:12; Ex. 1003 ¶ 172). Petitioner further provides evidence that adding training in an initialization mode before normal operation was necessary to minimize errors and ensure correct read and write operations. *Id.* at 37 (citing Ex. 1014 ¶ 123; Ex. 1025, 15–18; Ex. 1022, Fig. 4, ¶¶ 32, 52, 88–89; Ex. 1027, 1:61–2:19, 6:24–25, 10:24–45; Ex. 1056, 18, 22, 25–26, 42–44; Ex. 1057, Fig. 5, code (57), 2:13–34,

2:60–3:3, 9:11–10:44; Ex. 1003 ¶¶ 180–181). Petitioner further sets forth motivation to communicate training status in an initialization mode using the same open drain output used in other modes/operations. *Id.* at 38–40 (Ex. 1003 ¶¶ 158–163, 183–190; Ex. 1014 ¶¶ 18, 44, 49, 59, 64, 69, 72, 109, Figs. 4B, 7A; Ex. 1022 ¶¶ 4–5, 32–33, 52; Ex. 1043, 7:30–51).

In its Sur-Reply, Patent Owner argues that Hazelzet and Buchmann are not analogous art. Sur-Reply 15–18. This is largely new argument, which is improper in a sur-reply. *See* 37 C.F.R. § 42.23(b); Consolidated Trial Practice Guide "TPG"[7] 73–75. In any case, we do not agree with Patent Owner that Petitioner overstates the field of endeavor as memory module design. Hazelzet and Buchmann repeatedly mention "design" in the context of a memory module and its components. Ex. 1014 ¶¶ 39, 65, 67–68, 83, 90, 105; Ex. 1016, 2:30–51. Patent Owner insists that the problem addressed in Hazelzet is not increasing memory module capacity, performance, and reliability, but the reference is titled "High Density High Reliability Memory Module . . . ." that is "capable of meeting desired density, performance and reliability requirements" at "low cost." Ex. 1014, code (54), ¶ 7. And, Buchmann identifies benefits that "[b]y placing more technology-specific functionality local to the memory subsystem, such benefits as improved performance, increased design flexibility/extendibility, etc., may be obtained, often while making use of unused circuits within the subsystem." Ex. 1016, 32:30–34 (*see also* 32:7–30). These overlapping or identical problems and solutions would have drawn the person of ordinary skill in the art to consider Hazelzet and Buchmann together.

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[7] The Consolidated Trial Practice Guide "TPG" is available at www.uspto.gov/TrialPracticeGuideConsolidated.

In the Sur-Reply, Patent Owner contends that the combinations in the asserted grounds are not a "mere arrangement of old elements performing known functions yielding expected results." Sur-Reply 17. Patent Owner contends that adding data buffers to Hazelzet's module, adding a new training mode, and using a UE line on Hazelzet's redesigned module to report notifications of the new training mode would require substantial reconstruction and redesign of the elements without expectation of success. *Id.* Although data buffers and training may be "new" in the sense that Hazelzet does not have them, they are not new in the art, as Buchmann shows. *See* Ex. 1016, code (57). And understanding that Hazelzet uses a dual-purpose open drain output to signal different parameters in different modes, simply adding another training mode and a notification signal for that open drain output would have been straightforward for a person of ordinary skill in the art. *See* Ex. 1014 ¶ 59, Fig. 4B.

Patent Owner argues that there is no motivation to combine data buffers with Hazelzet. Sur-Reply 18. Patent Owner argues that Petitioner goes outside the bounds of Hazelzet and Buchmann by relying on Kim and Exhibits 1036 and 1037 and other evidence for ground 2 (Kim is expressly relied upon as evidence in ground 3 of the Petition (Pet. 4)). As discussed below, there is no need to reach Kim or Exhibits 1036 and 1037 to find the claims unpatentable over the combination of Hazelzet and Buchmann alone.

Patent Owner further argues that Buchmann provides no motivation to add training to a system like Hazelzet's which lacks a data buffer. Sur-Reply 20–24. Patent Owner contends that merely adding training to Hazelzet would not teach, suggest, or motivate a person of ordinary skill in the art "to add training in a way that would implement the novel notification

signal required by all claims." *Id.* at 20 (emphasis omitted). Further, Patent Owner contends that if one added training, one of ordinary skill in the art would have used Hazelzet's existing architecture with Hazelzet's memory controller. *Id.* at 20–21.

Patent Owner's arguments fail to take into account Buchmann's teachings that "[a]dditional functions that may reside local to the memory subsystem . . . include write and/or read buffers, . . . error detection and/or correction circuitry on one or more busses, . . . operational and/or status registers, initialization circuitry, self-test circuitry (testing logic and/or memory in the subsystem), performance monitoring and/or control, . . . and other functions that may have previously resided in the processor, memory controller or elsewhere in the memory system." Ex. 1016, 32:7–22. Buchmann further states "[b]y placing more technology-specific functionality local to the memory subsystem, such benefits as improved performance, increased design flexibility/extendibility, etc., may be obtained, often while making use of unused circuits within the subsystem." *Id.* at 32:30–34. In other words, Buchmann identifies the design trend of moving functionality from the system processor or memory controller to the memory module. *See KSR*, 550 U.S. at 418 ("Often, it will be necessary for a court to look to . . . the effects of demands known to the design community . . . to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue").

Patent Owner argues that "Petitioner did not rebut [Patent Owner's] evidence that teaches away from adding complex and costly training to Hazelzet." Sur-Reply 21 (emphasis omitted). We do not consider new arguments in a Sur-Reply. *See* 37 C.F.R. § 42.23(b); TPG 73–74. In any

case, the only "teaching away" argument in the Response relates to adding a notification signal to Hazelzet's UE line. *See* Resp. 60–63.

In sum, we find that one of ordinary skill in the art would have been motivated to combine Hazelzet and Buchmann for the reasons Petitioner has stated, notwithstanding Patent Owner's arguments to the contrary. We now consider whether each of the limitations of claim 1 are met by the combination of Hazelzet and Buchmann.

1. Analysis of Independent Claim 1

a) Limitation 1.a: "A memory module operable with a memory controller of a host system, comprising"

Petitioner contends "Hazelzet discloses dual inline memory modules ('DIMMs') configured to operate with the 'memory controller' of the host system." Pet. 41 (citing Ex. 1014 ¶¶ 36–39, Figs. 2, 3A–3D; Ex. 1003 ¶ 193).

Patent Owner does not respond to Petitioner's contention concerning the preamble. *See* Resp. Petitioner has shown that Hazelzet discloses claim 1's preamble, to the extent it is limiting.[8]

b) Limitation 1.b: "a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge

[8] Since we agree with Petitioner that the preamble is taught or at least suggested by the combination of Hazelzet and Buchmann, we do not decide whether the preamble is limiting.

connection in addition to the first edge connections and the second edge connections"

Petitioner contends Hazelet's DIMM comprises a printed circuit board which fits in the slot of the host system. Pet. 42–44 (citing Ex. 1014 ¶¶ 15, 37, 39, 97, Figs. 2, 3A–3D, 9, 11; Ex. 1003 ¶¶ 196–198). Petitioner further contends "the printed circuit board has a first set of edge connections for communicating data signals between the module and the memory controller" (Pet. 45 (citing Ex. 1014 ¶¶ 15, 35, 38, 41, Figs. 7A–7C; Ex. 1003 ¶ 199)) and a "second set of edge connections for communicating address and control signals from the memory controller" (Pet. 45 (citing Ex. 1014 ¶¶ 15, 35, 38, 41, Figs. 7A–7C; Ex. 1003 ¶ 200)). Petitioner further contends Hazelzet "has an error edge connection coupled to the open drain output of the module controller." Pet. 45–46 (citing Ex. 1014 ¶¶ 72, 109, Figs. 4B, 7A; Ex. 1003 ¶ 201).

Patent Owner does not specifically respond to these arguments. *See* Resp. Based on our review and consideration of the record, we determine that Petitioner has shown that Hazelzet teaches this limitation.

c) Limitation 1.c: "dynamic random access memory elements on the printed circuit board"

Petitioner contends Hazelzet's memory module includes DRAMs on the printed circuit board. Pet. 46 (citing Ex. 1014 ¶ 15, Figs. 2, 3A–3D; Ex. 1003 ¶ 204).

Patent Owner does not specifically respond to this argument. *See* Resp. Based on our review and consideration of the record, we determine that Petitioner has shown that Hazelzet teaches this limitation.

d) Limitation 1.d: "a module controller on the printed circuit board and coupled to the dynamic random

access memory elements, the module controller having an open drain output coupled to the error edge connection"

Petitioner contends Hazelzet's ECC/parity register discloses a module controller, and has an uncorrectable error output 121, which is an open drain output. Pet. 46 (citing Ex. 1014 ¶¶ 44, 59, 72, Figs. 3A–3D, 4A–4B). Petitioner contends Hazelzet's ECC/parity register is on the printed circuit board and is coupled to the DRAMs. *Id.* (citing Ex. 1014 ¶¶ 39, 42, Figs. 3A–3D; Ex. 1003 ¶ 207). Petitioner contends Hazelzet's UE 121 is coupled to the error edge connection of the module. *Id.* (citing Ex. 1014 ¶¶ 59, 72, Figs. 4B, 7A (pin 142); Ex. 1003 ¶¶ 208–211).

Patent Owner does not specifically respond to these arguments. *See* Resp. Based on our review and consideration of the record, we determine that Petitioner has adequately shown that Hazelzet teaches this limitation.

e) Limitation 1.e.i: "wherein the memory module is configurable to operate in any of at least a first mode and a second mode"

Petitioner contends Hazelzet's memory module operates in the parity mode, corresponding to the claimed "first mode" and an ECC mode. Pet. 46–47 (citing Ex. 1014 ¶¶ 64, 69–72, Fig. 8; Ex. 1003 ¶ 213). Petitioner contends the claimed "second mode" corresponds to a training mode carried out using Buchmann's training sequences. *Id.* at 46–47*; see also* Pet. 38–39.

Patent Owner does not specifically respond to these arguments. *See* Resp. Based on our review and consideration of the record, we determine that Petitioner has shown that Hazelzet and Buchmann teaches this limitation.

f) Limitation 1.e.ii: "wherein the memory module in the first mode is configurable to perform one or more

> *normal memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections"*

Petitioner contends that Hazelzet's memory module is configurable to receive address and control signals via the edge connections. Pet. 47 (citing Ex. 1014 ¶¶ 15, 35, 38, 41, Figs. 2, 7A–7B; Ex. 1003 ¶ 214). Petitioner further contends Hazelzet's memory module communicates address and command information normally as a JEDEC compliant device, sending address and control to the register and data to the DRAMs. *Id.* (citing Ex. 1014 ¶¶ 44, 75, Fig. 8; Ex. 1024, 1, 14, 16; Ex. 1003 ¶¶ 215, 219). Petitioner contends Hazelzet discloses that these operations occur during the parity mode, which is a normal mode of operation. *Id.* at 48–50 (citing Ex. 1014 ¶¶ 38, 64, 70, 75; Ex. 1003 ¶¶ 221–223, 225).

Patent Owner does not specifically respond to these arguments. *See* Resp. Based on our review and consideration of the record, we determine that Petitioner has shown that Hazelzet teaches this limitation.

> *g) Limitation 1.e.iii: "wherein the memory module in the second mode is not accessed by the memory controller for normal memory read or write operations"*

Petitioner contends that the combination includes Buchmann's "training sequences in a training mode ('second mode') during initialization separate from any mode that includes memory read and write operations in response to memory controller commands, thereby satisfying this limitation." Pet. 50 (citing § V.D) (emphasis omitted). Petitioner further argues that neither Hazelzet nor Buchmann disclose memory read and write operations occurring during training operations, so their silence additionally

satisfies this limitation. *Id.* (citing Ex. 1003 ¶ 229; *Süd-Chemie, Inc. v. Multisorb Technologies, Inc.*, 554 F.3d 1001, 1004–05 (Fed. Cir. 2009)).

Patent Owner does not specifically respond to these arguments. *See* Resp. Based on our review and consideration of the record, we determine that Petitioner has shown that Hazelzet and Buchmann teach this limitation.

> *h) Limitation 1.e.iv: "wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences"*

Petitioner contends that the proposed combination includes "a separate training mode ('second mode') into which the module can be placed and in which the module can implement ('configurable to perform') various training sequences (e.g., Write Leveling and Read Enable Training per JEDEC/TS0 and TS3 per Buchmann) ('operations related to one or more training sequences')". Pet 50 (citing § V.D) (emphasis omitted). Petitioner contends that "[e]ach of these operations includes a set of operations occurring in a particular order, used for training the memory module." *Id.* at 51 (citing Ex. 10165:51–57, 8:24–9:18, Figs. 4, 6; Ex. 1018, Fig. 4; Ex. 1040, 14:1–15.3; Ex. 1003 ¶ 230).

Patent Owner does not specifically respond to these arguments. *See* Resp. Based on our review and consideration of the record, we determine that Petitioner has adequately shown that Hazelzet and Buchmann teach this limitation.

> *i) Limitation 1.f.i: "wherein the module controller is configurable to receive via the second edge connections the address and control signals associated with the one or more normal memory read or write operations"*

Petitioner contends, as explained for claim limitations 1.b and 1.e.ii, that Hazelzet's module receives address and control signals associated with

normal memory read and write operations over edge connections. Pet. 51 (citing Ex. 1014 ¶¶ 15, 35, 38, 41, 64, 70, Figs. 2, 7A–7B; Ex. 1024, 13–14, 16; Ex. 1003 ¶ 232).

Patent Owner does not specifically respond to these arguments. *See* Resp. Based on our review and consideration of the record, we determine that Petitioner has adequately shown that Hazelzet teaches this limitation.

> *j) Limitation 1.f.ii: "wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals"*

Petitioner contends, as explained for claim limitations 1.b and 1.e.ii, that Hazelzet discloses a printed circuit board that has a first set of edge connections for communicating data signals between the DRAM and the system memory controller. Pet. 51 (citing Ex. 1014 ¶¶ 15, 35, 38, 41, Figs. 7A–7C). Petitioner contends the communication of data signals occurs while the memory module is in the "parity mode" and in accordance with the received address and control signals. *Id.* (citing Ex. 1014 ¶¶ 15, 35, 38, 41, 64, 70, Figs. 2, 8). Petitioner contends, as explained for claim limitation 1.e.ii, "data communication between the memory module and the memory controller is 'in accordance with the address and control signals.'" *Id.* at 51–52 (citing Ex. 1014 ¶¶ 15, 35, 38, 41, 64, 70, Figs. 2, 7A–7C, 8; Ex. 1024, 13; Ex. 1003 ¶¶ 214–223, 233) (emphasis omitted).

Patent Owner does not specifically respond to these arguments. *See* Resp. Based on our review and consideration of the current record, we determine that Petitioner has adequately shown that Hazelzet teaches this limitation for purposes of institution.

k) Limitation 1.f.iii: "wherein the module controller is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred while the memory module is in the first mode"

Petitioner contends, as explained in claim limitations 1.b and 1.d, that "the error edge connection (pin 142) is coupled to the open drain output (UE 121) of the ECC/Parity register ('module controller')." Pet. 52 (citing Ex. 1014 ¶¶ 59, 72, Figs. 4B, 7A (pin 142); Ex. 1003 ¶ 234) (emphasis omitted). Petitioner contends the ECC/Parity register includes an "SEC/DED ECC 90" with "parity generator/checker circuit 231." *Id.* (citing Ex. 1014, ¶¶ 28, 76, Figs. 4B, 5; Ex. 1003 ¶ 235). Petitioner notes that "[w]hen the memory module is in the parity mode ('first mode'), the 'parity generator/checker circuit 231' generates and sends the 'parity error signal (PERR)' to the 'error logic circuit' 100." *Id.* (citing Ex. 1014 ¶¶ 70, 76, Figs. 4, 5; Ex. 1003 ¶ 236) (emphasis omitted). Petitioner contends the "error logic circuit" 100 outputs the parity error signal (PERR) to the memory controller through the output line UE 121, which is an open-drain output coupled to the memory controller using pin 142. *Id.* (citing Ex. 1014 ¶¶ 38, 59, 70, 72, Fig. 7A (pin 142); Ex. 1003 ¶¶ 237–240).

Patent Owner does not specifically respond to these arguments. *See* Resp. Based on our review and consideration of the record, we determine that Petitioner has shown that Hazelzet teaches this limitation.

l) Limitation 1.g: "wherein the module controller in the second mode is further configurable to provide information related to the one or more training sequences by driving the open drain output and the error edge connection to a first state or to a second state, one of the first state and the second state being a low logic

level and the other one of the first state and the second state being a high impedance state"

Petitioner contends that in the proposed combination, the Hazelzet module would be modified to be configurable to enter a training mode and output Buchmann training status signals to the system memory controller via an open drain output UE 121. Pet. 52–53 (citing § V.D). According to Petitioner, each of the status signals analyzed (TS0_done, TS3_ack, TS3_done) represent the '"information related to the one or more training sequences' because each provides status about the related sequences, such as whether it has been completed or whether all memory buffers have returned an acknowledgement." *Id.* at 53 (emphasis omitted). Petitioner contends this combination satisfies "wherein the module controller in the second mode is further configurable to provide information related to the one or more training sequences." *Id.* (citing Ex. 1003 ¶¶ 164–167, 243) (emphasis omitted).

Petitioner further contends Hazelzet's "memory system involves sharing the open drain output so that the memory controller can receive notification signals from multiple modules using the open drain output." *Id.* (citing Ex. 1014 ¶¶ 18, 72, 109; Ex. 1003 ¶ 244). Petitioner states that a person of ordinary skill in the art would understand that, in the combination, "the added training status signals would be at a low logic level" over Hazelzet's open drain output (UE 121) "until the related operations are completed for all modules of the system and the gate signals to the transistors of all the open drain circuits in all the modules are low, at which time the signals would be in a high impedance state, indicating completion." *Id.* at 53–54 (citing Ex. 1017, 5:65–6:12, Fig. 4; Ex. 1003 ¶ 245). Petitioner

contends the high and low gate signals to the transistors represent "driving the open drain output and the error edge connection to a first state or to a second state." *Id.* at 54 (citing Ex. 1003 ¶ 245) (emphasis omitted).

Petitioner states that "open drain signals would be changed from a high impedance state to a low state as the gate of the transistor changes from a low to a high to indicate the related training operations were in progress, and changed from a low state to a high impedance state as the gate of the transistor driving the signal changes from a high to a low to indicate when the related operations complete in each memory module." *Id.* (citing Ex. 1014 ¶¶ 59, 70, 72, Fig. 4B; Ex. 1017, 5:65–6:12, Fig. 4; Ex. 1016, 3:52–54, 5:51–7:2, 8:24–9:18, 26:30–32, 27:18–21, Figs. 4, 6; Ex. 1003 ¶ 246). Petitioner contends each combination therefore satisfies "one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state." *Id.* (emphasis omitted).

Patent Owner does not specifically respond to these arguments. *See* Resp. Based on our review and consideration of the record, we determine that Petitioner has shown that Hazelzet and Buchmann teach this limitation.

m) Conclusion for Claim 1

Petitioner has shown by a preponderance of the evidence that one of ordinary skill in the art would have had reasons to combine Hazelzet and Buchmann as proposed in the Petition, with a reasonable expectation of success in arriving at the memory module recited in claim 1. Petitioner has further shown by a preponderance of the evidence that the combination of Hazelzet and Buchmann teaches or at least suggests all limitations of

claim 1. Consequently, claim 1 of the '595 patent is unpatentable as obvious over the combination of Hazelzet and Buchmann.

2. Analysis of Independent Claim 10

Claim 10 is an independent method claim and recites similar limitations to claim 1. *See* Ex. 1001, 15:59–16:44. Petitioner contends claim 10 is unpatentable, relying on similar disclosure in Hazelzet and Buchmann as with independent claim 1, as follows. Pet. 61–64.

a) Limitation 10.a: "A memory module operable with a memory controller of a host system, comprising:"

Petitioner contends that the preamble is satisfied for the reasons set forth for claim element 1.a. Pet. 61. Patent Owner does not dispute the preamble. *See* Resp. We agree with Petitioner's contention.[9]

b) Limitation 10.b: "a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections;"

Petitioner contends that this limitation is satisfied for the reasons set forth for claim limitation 1.b. Pet. 61. Patent Owner does not dispute Petitioner's contention. We agree with Petitioner's contention.

[9] *See* footnote 9.

c) Limitation 10.c: "dynamic random access memory elements on the printed circuit board;"

Petitioner contends that this limitation is satisfied for the reasons set forth for claim limitation 1.c. Pet. 61. Patent Owner does not dispute Petitioner's contention. We agree with Petitioner's contention.

d) Limitation 10.d: "a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection and configurable to drive the open drain output from a first state to a second state and from the second state to the first state, one of the first state and the second state being a low logic level, and the other one of the first state and the second state being a high impedance state; and"

Petitioner contends that this limitation is satisfied for the reasons set forth for claim limitations 1.d and 1.g. Pet. 61–62. Petitioner notes that limitation 10.d recites "configurable to drive the open drain output from a first state to a second state and from the second state to the first state." *Id.* at 61–62 (citing Ex. 1003 ¶ 319) (emphasis omitted). Petitioner contends this additional language is similar to claim 7 and is satisfied because "the open drain signals would be low logic levels to indicate the training sequence" MB-DRAM/TS0 or TS3 was in progress "(*i.e.*, the logic levels of the open drain output changes from a high impedance state to a low state, because the gate of the transistor changes from a low to a high)." *Id.* at 62. On the other hand, Petitioner contends "the open drain signal would be at a high-impedance (*i.e.*, the logic level of the open drain output changes from a low state to a high impedance state, because the gate of the transistor changes from a high to a low) when th[e] sequence completed in all memory

modules." *Id.* (citing Ex. 1014 ¶¶ 59, 70, 72, 76, Figs. 4B, 5; Ex. 1017, 5:65–6:18, Figs. 4, 5; Ex. 1003 ¶¶ 158–163, 168, 320).

Patent Owner does not dispute Petitioner's contention. We agree with Petitioner's contention.

> *e) Limitation 10.e: "wherein the memory module is operable in at least a first mode in which the memory module is configurable to perform one or more memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections, and a second mode in which the memory module is not accessed by the memory controller for memory read or write operations, and wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences without communicating data signals via the first edge connections;"*

Petitioner contends that the analysis of claim limitation 1.e and claim 9 satisfies this claim element. Pet. 62–63 (citing Ex. 1003 ¶ 323). Petitioner contends that the memory module is not accessed by the memory controller for memory read and write operations during MB-DRAM training, TS0 training or TS3 training. *Id.* at 63 (citing Ex. 1003 ¶ 323).

Patent Owner does not dispute Petitioner's contention that Hazelzet and Buchmann teach this claim limitation. We agree with Petitioner's contention.

> *f) Limitation 10.f: "wherein the module controller in the first mode is configurable to receive via the second edge connections the address and control signals associated with the one or more memory read or write operations, wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections*

> *in accordance with the address and control signals, and wherein the module controller in the first mode is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred in the memory module while the memory module is in the first mode;"*

Petitioner contends that this limitation is satisfied for the reasons set forth for claim limitation 1.f. Pet. 63. Patent Owner does not dispute Petitioner's contention, with which we agree.

> *g) Limitation 10.g: "wherein the module controller in the second mode is further configurable to output to the memory controller open-drain signals related to the one or more training sequences via the open drain output and the error edge connection while the memory module is in the second mode."*

Petitioner contends that this limitation is satisfied for the reasons set forth for claim limitation 1.g. Pet. 63. Patent Owner does not dispute Petitioner's contention, with which we agree.

h) Conclusion for Claim 10

Petitioner has shown by a preponderance of the evidence that one of ordinary skill in the art would have had reasons to combine Hazelzet and Buchmann as proposed in the Petition, with a reasonable expectation of success in arriving at the method recited in claim 10. Petitioner has further shown by a preponderance of the evidence that the combination of Hazelzet and Buchmann teaches or at least suggests all limitations of claim 10. Consequently, claim 10 of the '595 patent is unpatentable as obvious over the combination of Hazelzet and Buchmann.

3. Analysis of Independent Claim 17

Claim 17 is an independent method claim and recites similar limitations to claim 1. *See* Ex. 1001, 17:14–48. Petitioner contends claim 17 is unpatentable, relying on similar disclosure in Hazelzet and Buchmann as with independent claim 1, as follows. Pet. 64–65.

a) *Limitation 17.a: "A method, comprising:"*

Petitioner contends that the preamble is satisfied by operation of the combined system analyzed in connection with claim 1. Pet. 64 (citing Ex. 1003 ¶ 341). Patent Owner does not dispute Petitioner's contention. *See* Resp. We agree with Petitioner's contention.[10]

> *b) Limitation 17.b: "at a memory module coupled with a memory controller of a host system, the memory module including a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections, the memory module further including dynamic random access memory elements on the printed circuit board;"*

Petitioner contends that this limitation is satisfied for the reasons set forth for claim limitations 1.a, 1.b and 1.c. Pet. 64. Patent Owner does not dispute this limitation. *See* Resp. We agree with Petitioner's contention.

> *c) Limitation 17.c: "receiving via the second edge connections address and control signals associated with one or more memory read or write operations; controlling the dynamic random access memory elements*

[10] *See* footnote 9.

> *to communicate data signals corresponding to the one or more memory read or write operations via the first edge connections in response to the address and control signals; outputting via an open drain output coupled to the error edge connection a signal indicating a parity error having occurred in the memory module while the memory module is being accessed by the memory controller for a memory read or write operation;"*

Petitioner contends that this limitation is satisfied for the reasons set forth for claim limitations 1.e and 1.f. Pet. 64. Petitioner contends that Hazelzet "discloses normal memory operations that entail the module receiving address and control signals from a system memory controller via the respective address and control edge connections, and in response communicating data between the system memory controller and the module DRAMs via the data edge connections under the control of the module controller." *Id.* (citing § VI.A.1(2); Ex. 1003 ¶¶ 214–221, 345). Petitioner contends that, similarly, Hazelzet "discloses the module outputting, in the 'first mode,' a parity error signal via an open drain output (UE 121) in connection with memory read and write operations accessing the module." *Id.* (citing § VI.A.1.f; Ex. 1003 ¶¶ 231–241, 345) (emphasis omitted). Patent Owner does not dispute this limitation. *See* Resp. We agree with Petitioner's contention that Hazelzet and Buchmann teach or at least suggest limitation 17.c.

> *d) Limitation 17.d: "performing operations related to one or more training sequences while the memory module is not accessed by the memory controller for memory read or write operations; and outputting to the memory controller via the open drain output and the error edge connection open-drain signals related to the*

> *one or more training sequences and unrelated to any memory read or write operation."*

Petitioner contends that this limitation is satisfied for the reasons set forth in claim limitation 1.e and 1.g. Pet. 65. Petitioner contends that the combination of Hazelzet and Buchmann "include a module that performs training sequence operations unrelated to memory read or write operations in response to commands from the memory controller." *Id.* (citing Ex. 1003 ¶¶ 231–241). Petitioner contends that, "[s]imilarly, the module of the combined system outputs to the system memory controller training notification signals (*e.g.*, . . . TS0_done, TS[0]_ack, TS3_done, TS3_ack) via an open drain output (UE 121)," which notification signals are related solely to Buchmann "training sequences and not to any memory controller operations that seek to communicate data with the module or seek to read or write to the memory devices during the training mode analyzed here." *Id.* (citing §VI.A.1.g; Ex. 1003 ¶¶ 164–165, 180–181, 229, 347).

Patent Owner does not dispute this limitation. *See* Resp. We agree with Petitioner's contention.

e) Conclusion for Claim 17

Petitioner has shown by a preponderance of the evidence that one of ordinary skill in the art would have had reasons to combine Hazelzet and Buchmann as proposed in the Petition, with a reasonable expectation of success in arriving at the memory module recited in claim 17. Petitioner has further shown by a preponderance of the evidence that the combination of Hazelzet and Buchmann teaches or at least suggests all limitations of claim 17. Consequently, claim 17 of the '595 patent is unpatentable as obvious over the combination of Hazelzet and Buchmann.

4. Analysis of Independent Claim 21

Claim 21 is an independent method claim and recites similar limitations to claim 1. *See* Ex. 1001, 18:4–52. Petitioner contends that claim 21 is unpatentable, relying on similar disclosure in Hazelzet and Buchmann as with independent claim 1, as follows. Pet. 65–68.

a) Limitation 21.a: "A memory module operable with a memory controller of a host system, comprising:"

Petitioner contends that the preamble is satisfied by the combination of Hazelzet and Buchmann for the reasons set forth for claim element 1.a. Pet. 65. Patent Owner does not dispute Petitioner's contention. *See* Resp. We agree with Petitioner's contention.[11]

b) Limitation 21.b: "a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections;"

Petitioner contends that this limitation is satisfied by the combination of Hazelzet and Buchmann for the reasons set forth for claim limitation 1.b. Pet. 65. Patent Owner does not dispute Petitioner's contention. *See* Resp. We agree with Petitioner's contention.

c) Limitation 21.c: "dynamic random access memory elements on the printed circuit board; and"

Petitioner contends that this limitation is satisfied by the combination of Hazelzet and Buchmann for the reasons set forth for claim limitation 1.c.

[11] *See* footnote 9.

Pet. 65–66. Patent Owner does not dispute Petitioner's contention. *See* Resp. We agree with Petitioner's contention.

> *d) Limitation 21.d: "a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller including a transistor having a gate and an open drain output coupled to the error edge connection; wherein the module controller is configurable to drive the gate of the transistor so as to drive the open drain output to a first state or a second state, the first state being a low logic level and the second state being a high impedance state;"*

Petitioner contends that this limitation is satisfied for the reasons set forth for claim limitation 1.d and claims 3 and 4. Pet. 66. Specifically, Petitioner contends that the Hazelzet and Buchmann satisfy "a module controller on the printed circuit board and coupled to the dynamic random access memory elements" of claim 21 for the reasons set for the claim element 1.d. *Id.* (citing Ex. 1003 ¶¶ 206–209) (emphasis omitted). Petitioner contends "the module controller including a transistor having a gate and an open drain output coupled to the error edge connection" is satisfied for the reasons that Petitioner set forth for claim 3. *Id.* (citing Ex. 1003 ¶¶ 251–255) (emphasis omitted).

Specifically, Petitioner contends that Hazelzet discloses that the ECC/Parity register has "open drain output[s]" such as UE 121. Pet. 55 (citing Ex. 1014 ¶¶ 44, 59, 72, Fig. 4B; Ex. 1003 ¶ 252) (emphasis omitted). Petitioner contends that "a Skilled Artisan would understand an open drain output to necessarily include, a field effect transistor having gate, source, and drain." *Id.* at 7, 55 (citing § V.D). Petitioner further contends that a "Skilled Artisan would have also understood that the disclosed 'open drain' output is the output of 'a transistor having an open drain' while the 'source'

of that transistor is 'coupled to the ground.'" *Id.* at 55–56 (citing Ex. 1017, 5:65–6:18, Figs. 4–5; Ex. 1020, title, 4:28–37; Ex. 1003 ¶¶ 158–163, 168, 253–254) (emphasis omitted).

Petitioner further contends that the combination of Hazelzet and Buchmann satisfy claim 21's language reciting "wherein the module controller is configurable to drive the gate of the transistor so as to drive the open drain output to a first state or a second state, the first state being a low logic level [e.g., ground] and the second state being a high impedance state" for the reasons set forth for claim 4. Pet. 66 (citing §VI.A.4; Ex. 1003 ¶¶ 271, 361) (emphasis omitted).

Specifically, Petitioner contends that the combination of Hazelzet and Buchmann has an "open drain output configured such that the transistor output is driven low (ground) while training is still occurring and driven high upon completion." Pet. 56. "[T]o drive the output low (i.e., ground), the gate of the transistor must be high, causing the transistor to conduct and connect the drain to ground." *Id.* "[T]o drive the output high (which would be a high impedance state), the gate of the transistor must be low, turning the transistor off." *Id.* (citing Ex. 1003 ¶¶ 168, 272–275).

Petitioner thus contends that in the combination of Hazelzet and Buchmann, "the ECC/Parity register is configurable (for example, by placing it in the training mode) 'to drive a gate of the transistor high so as to drive open drain output and the error edge connection to ground, or to drive the gate of the transistor low so as to drive the open drain output and the error edge connection to the high impedance state," and thereby output training sequence status signals." *Id.* (citing Ex. 1003 ¶ 274) (emphasis omitted).

Patent Owner does not dispute Petitioner's contentions. *See* Resp. We agree with Petitioner's contentions.

> *e) Limitation 21.e: "[i] wherein the module controller is configurable to receive via the second edge connections memory commands associated with normal memory read or write operations and to output a set of address and control signals for each of the normal memory read or write operations; [ii] wherein the dynamic random access memory elements are configurable to communicate one or more N-bit-wide data signals with the memory controller via the first edge connections in response to the set of address and control signals, where N is at least 32; [iii] wherein the module controller is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred during any of the memory read or write operations by driving the open drain output and the error edge connection to the first state;"*

Petitioner contends that this limitation is satisfied by the combination of Hazelzet and Buchmann for the same reasons set forth for claim limitations 1.f.i–iii. Pet. 66–68.

For limitation 21.e.i, Petitioner contends that Hazelzet "discloses that the ECC/Parity register is configurable *(e.g.*, when placed in parity mode) to receive address command signals" that a person of ordinary skill in the art "would understand to be associated with normal memory read and write operations ('memory commands associated with normal memory read or write operations')." *Id.* at 66–67 (citing Ex. 1003 ¶¶ 214–221; Ex. 1014, ¶¶ 15, 35, 38, 41, 64, 70, Figs. 2, 7A–7B) (emphasis omitted). "[A]nd that, in response to such commands, the ECC/Parity register outputs associated address and control signals to the DRAMs of the module." *Id.* at 67 (citing

Ex. 1014 ¶¶ 42, 75). Hazelzet therefore discloses claim element 21.e.i. *Id.* (citing Ex. 1003 ¶ 364).

Petitioner contends, to the extent one might argue that Hazelzet does not sufficiently disclose claim limitation 21.e.i, "it would have been obvious to include it in the combined system." *Id.* In particular, Petitioner contends that Hazelzet "clearly discloses the ECC/Parity register receiving address and command information associated with memory commands." *Id.* (citing Ex. 1014 ¶¶ 15, 38, 41–42, 64, 70, 75, Figs. 2, 7A–7B). Petitioner contends that a person of ordinary skill in the art "would have been motivated to configure the register to correspondingly output associated address and control signals to the DRAMs, and it would have been common sense to do so, because that would be necessary to carry out the memory operations and access the DRAMs." *Id.* (citing Ex. 1003 ¶ 365).

Petitioner contends that Hazelzet "also discloses that the DRAMs are configurable (*i.e.*, when connected to the address, control, data and PLL lines of the module, as described in Hazelzet, [Ex.] 1014, [Fig.] 2), to communicate data signals with the system memory controller over the disclosed edge connections in response to address and control signals." *Id.* Petitioner contends that Hazelzet "discloses pinout information for one embodiment of his module, which includes 64 data lines (DQ0-DQ63)" to "communicate a 64-bit wide data signal." *Id.* at 67–68 (citing Ex. 1014, Figs. 7A–7C; Ex. 1003 ¶¶ 231–241). Alternatively, Petitioner contends that Hazelzet discloses a 72 bit wide (i.e., 9x8=72) embodiment. *Id.* at 68 (citing Ex. 1014 ¶ 92). Petitioner contends that Hazelzet therefore discloses claim limitation 21.e.ii. *Id.* (citing Ex. 1003 ¶ 366).

Petitioner further contends that, to the extent Patent Owner argues that a single "dynamic random access memory element" must be able to "communicate one or more N-bit-wide data signals . . . where N is at least 32," to satisfy the limitation in claim limitation 21.e.ii, Petitioner contends that this limitation would nevertheless have been obvious. *Id.* (emphasis omitted). Petitioner contends that "modifying the memory system to use SDRAMs with high bit widths (*e.g.*, 32 bit wide) was not only known (or at least obvious), but also well within the skill of a [person of ordinary skill in the art] by the effective filing date of the [']595 Patent." *Id.* (citing Ex. 1024, i; Ex. 1029, 1; Ex. 1014 ¶ 113; Ex. 1003 ¶ 367).

Petitioner contends that the combination of Hazelzet and Buchmann discloses claim limitation 21.e.iii for the reasons set forth above for claim limitation 1.f.iii. *Id.* (citing Ex. 1003 ¶¶ 231–241, 368).

Patent Owner does not dispute Petitioner's contention that Hazelzet and Buchmann teach this claim limitation. We agree with Petitioner's contention.

> *f) Limitation 21.f: "wherein the memory module is configurable to perform operations related to one or more training sequences while the memory module is not accessed by the memory controller for memory read or write operations; and wherein the module controller is configurable to provide information related to the one or more training sequences by driving the open drain output and the error edge connection from one of the first state and the second state to the other one of the first state and the second state."*

Petitioner contends that this limitation 21.f is satisfied for the reasons set forth for claim limitations 1.e, 1.g, and 10.e. Pet. 68. Patent Owner does not dispute Petitioner's contentions, with which we agree.

g) Conclusion for Claim 21

Petitioner has shown by a preponderance of the that one of ordinary skill in the art would have had reasons to combine Hazelzet and Buchmann as proposed in the Petition, with a reasonable expectation of success in arriving at the method recited in claim 21. Petitioner has further shown by a preponderance of the evidence that the combination of Hazelzet and Buchmann teaches or at least suggests all limitations of claim 21. Consequently, claim 21 of the '595 patent is unpatentable as obvious over the combination of Hazelzet and Buchmann.

5. Claims 2 and 11

Claim 2 depends from claim 1 and recites "wherein the module controller comprises an integrated circuit." Ex. 1001, 15:22–23. Claim 11 depends from claim 10 and recites the same limitation. *Id.* at 16:45–46.

Petitioner contends that Hazelzet's ECC/Parity register ("module controller") "comprises in integrated circuit." Pet. 54 (citing Ex. 1014 ¶ 38) (emphasis omitted). Petitioner contends that Hazelzet "explains that the module support devices, including 'buffers,' 'registers,' and 'PLL' may be comprised of 'multiple separate chips' or may be 'combined onto a single package or even integrated onto a single device.'" *Id.* (citing Ex. 1014 ¶¶ 39, 42 115, Figs. 3A–3D; Ex. 1003 ¶¶ 249–250, 329). Patent Owner does not dispute Petitioner's contentions. We agree with Petitioner that Hazelzet teaches the limitations of claims 2 and 11 of the '595 patent.

6. Claim 3

Claim 3 depends from claim 1 and recites "wherein the module controller includes a notification circuit comprising a transistor having an

open drain coupled to the open drain output and source coupled to the ground." Ex. 1001, 15:24–27.

Petitioner contends that, as explained for claim limitation 1.d, Hazelzet discloses that the ECC/Parity register has an open drain output. Pet. 55. Petitioner contends that Hazelzet's "ECC/Parity register has an 'error correction code circuit ECC segment 21b,' which is a 'notification circuit'" which "outputs signals notifying the system memory controller of correctable, uncorrectable, and parity errors." *Id.* (citing Ex. 1014 ¶ 44) (emphasis omitted). Petitioner contends that the "error correction code circuit ECC segment 21b" (within the ECC/Parity register) includes circuitry for determining whether the errors occurred, and provides an "open-drain" output for a notification signal such as UE 121. *Id.* (citing Ex. 1014 ¶¶ 59, 72, Fig. 4B; Ex. 1003 ¶ 252). Petitioner contends that a person of ordinary skill in the art would have understood that an open drain output includes a field effect transistor having gate, source, and drain, and that an "open drain" output is an output of "a transistor having an open drain" while the source of that transistor is "coupled to the ground." *Id.* at 55–56 (citing Ex. 1017, 5:65–6:18, Figs. 4–5; Ex. 1020, 1 (Title), 4:28–37; Ex. 1003 ¶¶ 158–163, 253–254) (emphasis omitted).

Patent Owner does not dispute Petitioner's contentions. *See* Resp.

We agree with Petitioner that the combination of Hazelzet and Buchmann teaches these limitations. Hazelzet teaches that the ECC/Parity register includes an error correction code circuit that notifies the memory controller of errors, that has "[t]wo open-drain outputs are available to permit multiple modules to share a common signal line for reporting an

error." Ex. 1014 ¶¶ 59, 72, 109, Fig. 4B. This is sufficient to teach the "notification circuit" limitation of claim 3 of the '595 patent.

7. Claim 4

Claim 4 depends from claim 3 and recites "wherein the module controller is configurable to drive a gate of the transistor high so as to drive open drain output and the error edge connection to ground, or to drive the gate of the transistor low so as to drive the open drain output and the error edge connection to the high impedance state." Ex. 1001, 15:28–33.

Petitioner contends (as explained in § V.D of the Petition) that in the combination of Hazelzet and Buchmann "the open drain output is configured such that the transistor output is driven low (ground) while training is still occurring[,] and driven high upon completion." Pet. 56. According to Petitioner, "to drive the output low (i.e., ground), the gate of the transistor must be high, causing the transistor to conduct and connect the drain to ground." *Id.* "[T]o drive the output high (which would be a high impedance state), the gate of the transistor must be low, turning the transistor off." *Id.* (citing Ex. 1003 ¶¶ 168, 272–275). Petitioner contends that, in the combination of Hazelzet and Buchmann, "the ECC/Parity register is configured (for example, by placing it in the training mode) 'to drive a gate of the transistor high so as to drive open drain output and the error edge connection to ground, or to drive the gate of the transistor low so as to drive the open drain output and the error edge connection to the high impedance state,' and thereby output training sequence status signals." *Id.* (citing Ex. 1003 ¶ 274) (emphasis omitted).

Patent Owner does not dispute Petitioner's contentions. *See* Resp.

We credit Dr. Alpert's testimony concerning what one of ordinary skill in the art would have understood of the structure and operation of an open drain transistor as taught by Hazelzet. *See* Ex. 1003 ¶¶ 272–275. Although Hazelzet does not specifically mention the gate of an open drain transistor being driven high, it does mention the output being driven low which would require the gate to be driven high in light of Dr. Alpert's testimony of what a person of ordinary skill in the art would have understood about the structure and operation of an open drain transistor. *Id.* Conversely, Dr. Alpert testifies to drive the output high (which would be the high impedance state), the gate of the transistor must be low, turning the gate off. Ex. 1003 ¶ 272 (citing ¶ 168). We agree with Petitioner that the combination of Hazelzet and Buchmann teaches, or at least suggests, the limitation of claim 4 of the '595 patent.

8. Claim 5

Claim 5 depends from claim 4 and recites "wherein the module controller is configurable to output the signal indicating a parity error having occurred by driving the gate of the transistor high to provide a low impedance path between the open drain output and the ground." Ex. 1001, 15:34–38. Petitioner contends that Hazelzet's "ECC/Parity register has 'open-drain output[s]' capable of using 'parity error signals' (PERR) to output signal UE 121 to the host indicating a parity error." Pet. 56 (citing Ex. 1014 ¶¶ 59, 70, 72, 76). "[W]hen the memory module is in the parity mode ('first mode'), the 'parity generator/checker circuit 231' (within SEC/DED ECC circuit 90) generates and sends the 'parity error signal (PERR)' to the 'error logic circuit' 100." *Id.* at 56–57 (citing Ex. 1014 ¶¶ 59, 70, 72, 76, Figs. 4B, 5; Ex. 1003 ¶ 278). Hazelzet states that in the

parity mode, the parity error "will be reported two clock pulses later via the Uncorrectable Error (UE) line (driven low for two clock pulses)." *Id.* at 57 (citing Ex. 1014 ¶¶ 18, 70; Ex. 1003 ¶ 279) (emphasis original).

Petitioner further contends that, as explained for claim 4, "Hazelzet discloses that its open-drain output is driven 'low' (i.e., to ground) when the driver is enabled (i.e., the gate receives a high voltage), and further explains that the open-drain 'output [is] permitted to return to an un-driven state (high impedance)' when the 'driver [is] disabled.'" *Id.* (citing Ex. 1014 ¶ 99; Ex. 1003 ¶ 280) (emphasis omitted).

Petitioner contends that, accordingly, Hazelzet discloses its open-drain output UE 121 is configured to "output the signal indicating a parity error having occurred by driving the gate of the transistor high to provide a low impedance path between the open drain output and the ground." *Id.* (citing Ex. 1017, 5:65–6:18, Figs. 4, 5; Ex. 1003 ¶¶ 158–163, 281) (emphasis omitted). Petitioner also refers to the Petition's analysis for claim 4.

Patent Owner does not dispute Petitioner's contentions. *See* Resp.

Petitioner shows sufficiently that the limitation of claim 5 is taught or at least suggested by the combination of Hazelzet and Buchmann. Hazelzet teaches that its ECC/Parity buffer includes an error correction code circuit segment 21b that outputs a parity error signal that is driven low to indicate a parity error. Ex. 1014 ¶¶ 59, 70, 72, 76, Figs. 4A–4B. Although Hazelzet does not specifically mention the gate of an open-drain transistor being driven high to provide a low impedance path from drain to ground, Dr. Alpert testifies that a person of ordinary skill in the art would have understood an open-drain transistor to be structured and to operate in this

way. Ex. 1003 ¶¶ 280–282. We agree with Petitioner that the limitation of claim 5 is taught or at least suggested by the combination of Hazelzet and Buchmann.

9. Claims 6, 13, and 22

Claim 6 depends from claim 3 and recites "wherein the notification circuit further includes a multiplexor or a logic circuit having a [sic] output coupled to a gate of the transistor and configurable to drive the gate of the transistor with either a first signal related to the parity error or a second signal related to the one or more training sequences." Ex. 1001, 15:39–44. Claim 13 depends from claim 10, and recites a similar limitation. *Id.* at 16:62–67. Claim 22 depends from claim 21 and recites a similar limitation. *Id.* at 18:53–59.

Petitioner contends that Hazelzet's "notification circuit" includes "Error Logic 100" which receives "US [sic] 110" signal and the "PERR 111" signal, and outputs one of these signals to the same "/ERROR (UE)" pin 121 depending on the mode of the memory module. Pet. 57–58 (citing Ex. 1014 ¶¶ 44, 59, 69–72, Fig. 4B; Ex. 1003 ¶ 285). Petitioner contends that the circuitry would be modified to implement the additional training mode, in which the UE 121 open drain output would, when the module is in the training mode, be used to send the notification/status signals identified above. *Id.* at 58 (citing Ex. 1003 ¶¶ 162, 167, 286, 333, 372).

Dr. Alpert testifies that a person of ordinary skill in the art would have understood that "the UE 121 open drain output is driven by a transistor in an open drain configuration, and that such a transistor . . . has 'a gate' that can be driven to assert the open drain output." *Id.* at 58 (citing Ex. 1003 ¶¶ 158–163, 286) (emphasis omitted). According to Petitioner, because "the

Error Logic 100 receives 'U[E] 110' signal and the 'PERR 111' signal and the training mode notification signals, but uses only one such signal to drive the UE 121 output, depending on mode," a person of ordinary skill in the art "would also understand that Error Logic 100 would necessarily include logic circuitry to determine which signal should be used to drive the transistor." *Id.* (citing Ex. 1017, 5:65–6:18, Figs. 4, 5) (depicting in Fig. 5 an "OR" gate used for such purpose). Petitioner regards additional circuitry as a "logic circuit," which necessarily has "an output coupled to a gate of the transistor," because that is how a transistor in an open drain configuration is driven. *Id.* (citing Ex. 1003 ¶¶ 286–287) (emphasis omitted). Petitioner further contends that "the signal driving that gate is necessarily related to one of the signals input to Error Logic 100 (*e.g.*, 'PERR 111' ('first signal') or the training notification signals ('second signal'), depending on mode, so the additional logic circuitry is 'configurable to drive the gate of the transistor with either a first signal related to the parity error or a second signal related to the one or more training sequences.'" *Id.* at 58–59 (citing Ex. 1003 ¶¶ 288, 333, 372) (emphasis omitted).

Patent Owner does not dispute Petitioner's contentions. *See* Resp.

Although Hazelzet does not specifically mention an OR logic circuit, we agree with Petitioner that one of ordinary skill in the art would understand that an OR logic circuit is implied by Hazelzet's teaching that "[w]hen *either* error line (CE) 109 *or* uncorrectable error line (UE) 110 is low . . . [t]he error lines 120, 121 will be active . . . in ECC mode or . . . in parity mode." Ex. 1014 ¶ 59, Fig. 4B. We agree with Petitioner that Hazelzet's "either/or" signifies use of a logic circuit performing an OR operation, and that extending the logic circuit to perform OR operation for

the training signals' status in training mode would have been straightforward. Accordingly, we agree with Petitioner that this limitation of claims 6, 13, and 22 is taught by the combination of Hazelzet and Buchmann.

10. Claims 7 and 14

Claim 7 depends from claim 1 and recites "wherein the module controller is configurable to provide the information related to the one or more training sequences by driving a gate of the transistor with the second signal so as to drive the open drain output from the high impedance state to ground or from ground to the high impedance state." Ex. 1001, 15:45–50. Claim 14 recites a similar limitation. *Id.* at 17:1–6.

Petitioner contends that, in the combination of Hazelzet and Buchmann, "the open drain output is configured such that the transistor output is driven low (ground) while training is still occurring and driven high upon completion." Pet. 59. Petitioner also contends "to drive the output low (i.e., ground), the signal at the gate of the transistor ('the second signal' when the system is in training mode) must be high, causing the transistor to conduct and connect the drain to ground." *Id.* (emphasis omitted). Petitioner further contends "to drive the output high (which would be a high impedance state), the gate of the transistor must be low, turning the transistor off." *Id.* (citing Ex. 1003 ¶¶ 168, 292–295).

Petitioner contends, in the combination of Hazelzet and Buchmann, "the ECC/Parity register is configurable (for example, by placing it in the training mode) 'to provide the information related to the one or more training sequences by driving a gate of the transistor with the second signal

so as to drive the open drain output from the high impedance state to ground or from ground to the high impedance state.'" *Id.*

Patent Owner does not dispute Petitioner's contentions. *See* Resp.

We agree with Petitioner that the combination of Hazelzet and Buchmann teaches, or at least suggests, that the module controller provides information for the training sequences by driving the gate of a transistor with the second signal so as to drive the open drain output from the high impedance state to ground or from ground to the high impedance state. Ex. 1003 ¶¶ 291–296, 334–335. Accordingly, we agree with Petitioner that the combination of Hazelzet and Buchmann teaches or at least suggests the limitations of claims 7 and 14.

11. Claims 8, 9, 15, 16, 18, 19, and 24

Claim 8 depends from claim 1 and recites "wherein the second edge connections include one or more pins that are not active while the memory module is in the second mode." Ex. 1001, 15:51–53. Claims 9, 15, 18, 19, and 24 depend from respective claims 1, 10, 17, and 21, and recite similar limitations. *Id.* at 15:54–58 (claim 9); 17:7–9 (claim 15); 17:49–52 (claim 18); 17:53–56 (claim 19); and 19:3–7 (claim 24).

Petitioner contends that in the combination of Hazelzet and Buchmann, "in which only the TS0 training operations are carried out in the training mode ('second mode'), the address/control and data pins (including the high order address/control pins) of the module edge connections would not be active during that training because TS0 training involves training of the "clock" itself, and no address/control or data signals are transmitted between the host and the memory module during such training." Pet. 60 (citing Ex. 1016, 5:51–7:2; Ex. 1003 ¶¶ 300, 306–307, 349, 376) (emphasis

omitted). Petitioner contends that this teaching satisfies the limitations of each of these dependent claims. *Id.*

Petitioner contends that, "[t]o the extent one might argue otherwise, it would have been obvious not to send any data or address/control signals while the clock is being trained because a [person of ordinary skill in the art] would have been motivated to keep the pin(s) for those signals inactive to conserve power and/or avoid unreliable operation during periods that the clock may be unstable." *Id.* at 60–61 (citing Ex. 1003 ¶¶ 301, 308).

Petitioner also contends that neither Hazelzet nor Buchmann "disclose address/control or data pins being active while the memory module is in a MB-DRAM Training or TS0 training mode during initialization/power-on." *Id.* at 61. "Because these claims each recite a negative limitation," Petitioner further contends that "silence also satisfies these claims." *Id.* (citing Ex. 1003 ¶¶ 302, 309) (quoting *Süd-Chemie*, 554 F.3d at 1004–05).

Patent Owner does not dispute Petitioner's contentions *See* Resp.

Petitioner has shown sufficiently that the combination of Hazelzet and Buchmann teaches the limitations of claims 8, 9, 15, 16, 18, 19, and 24. Specifically, Petitioner shows that the pins for the address and control signals in the Hazelzet-Buchmann combination would not be active during training of the memory module. *See, e.g.*, Ex. 1003 ¶¶ 300–303.

12. Claims 12, 20, and 23

Claim 12 depends from claim 10 and recites "[12.a] wherein the module controller includes a notification circuit having a transistor with an open drain coupled to the open drain output and a source coupled to the ground, [12.b] wherein the module controller is configurable to output to the memory controller the open-drain signals related to the one or more training

sequences by driving a gate of the transistor high so as to drive, the open drain output and the error edge connection to ground, and by driving the gate of the transistor low as to drive the open drain output and the error edge connection to the high impedance state, and [12.c] wherein the notification circuit is configurable to output the signal indicating a parity error having occurred by driving the gate of the transistor high to provide a low impedance path between the open drain output and ground." Ex. 1001, 16:47–61.

Claim 20 depends from claim 17 and recites "[20.a] wherein the memory module includes a notification circuit having a transistor with an open drain coupled to the open drain output and a source coupled to ground, [20.b] wherein outputting via an open drain output coupled to the error edge connection a signal indicating a parity error having occurred in the memory module comprises driving a gate of the transistor high to provide a low impedance path between the open drain output and ground, and [20.c] wherein outputting the open-drain signals related to the one or more training sequences and unrelated to any memory read or write operation comprises driving the gate of the transistor to drive the open drain output from a high impedance state to ground and from ground to the high impedance state." *Id.* at 17:57–18:3.

Claim 23 depends from claim 22 and recites "[23.a] wherein the transistor has a source coupled to ground, [23.b] wherein the module controller is configurable to output the signal indicating a parity error having occurred by driving the gate of the transistor high to provide a low impedance path between the open drain output and ground, and [23.c] wherein the module controller is configurable to provide the information

related to the one or more training sequences by driving the open drain output from a high impedance state to ground or from ground to the high impedance state." *Id.* at 18:60–19:2.

Petitioner contends that these claims are satisfied by the Hazelzet-Buchmann combination for the same reasons set forth for claims 3, 4, and 5. Pet. 63 (citing Ex. 1003 ¶¶ 331, 353, 374). In particular, Petitioner contends that the analysis for claim 3 satisfies claim limitation 12.a, the analysis for claim 4 satisfies claim limitation 12.b, and the analysis for claim 5 satisfies claim limitation 12.c. *Id.*

Similarly, Petitioner contends that the analysis in claim 3 satisfies claim limitations 20.1 and 23.a, the analysis in claim 5 satisfies claim limitations 20.b and 23.b, and the analysis in claim 4 satisfies claim limitations 20.c and 23.c. *Id.*

Petitioner further contends that in the Hazelzet-Buchmann combination, the open drain signals relating to the training signals (e.g., TS0_done, TS3_ack, TS3_done) are "unrelated to any memory read or write operation" because they are related solely to the Buchmann training sequences, "and not to any memory controller operations that seek to communicate data with the module or seek to read or write to the memory devices." *Id.* at 63–64 (citing § VI.A.1.g, Ex. 1003 ¶¶ 164, 180, 229, 347).

Patent Owner does not dispute Petitioner's contentions. *See* Resp. For the reasons stated for claims 3, 4 and 5, we agree with Petitioner that the Hazelzet-Buchmann combination teaches or at least suggests the limitations of claims 12, 20, and 23.

13. Conclusion for Ground 2

Petitioner has shown by a preponderance of the evidence that a person of ordinary skill in the art would have had reason to combine Hazelzet and Buchmann with a reasonable expectation of success in arriving at claims 1–24 of the '595 patent. Petitioner has further shown that the combination of Hazelzet and Buchmann teaches or at least suggests the limitations of claims 1–24. Accordingly, Petitioner has shown by a preponderance of the evidence that claims 1–24 would have been obvious over the combination of Hazelzet and Buchmann.

F. Ground 3: Obviousness Over the Combination of Hazelzet, Buchmann, and Kim

Petitioner, alternatively, contends claims 3–7, 12–14, 20, 22 and 23 would have been obvious over the combination of Hazelzet, JEDEC or Buchmann, and Kim. Pet. 69–74. For the reasons that follow, we are persuaded that the evidence, including Dr. Alpert's testimony, sufficiently supports Petitioner's arguments for the combination of Hazelzet, Buchmann, and Kim, and, therefore, establishes by a preponderance of the evidence the unpatentability of claims 3–7, 12–14, 20, 22, and 23. Because we determine that the combination of Hazelzet, Buchmann, and Kim establishes unpatentability under this ground, we need not address the combination of Hazelzet, JEDEC, and Kim. *See also* Section II.D.

1. Kim (Ex. 1017)

Kim was filed on January 22, 2008, issued on January 22, 2013, and is titled "Providing a Memory Device Having a Shared Error Feedback Pin." Ex. 1017, codes (22), (45), (54). Kim is generally directed "to a memory

device having a shared error feedback pin." Ex. 1017, 1:6–8. Kim's Figure 4 is reproduced below.

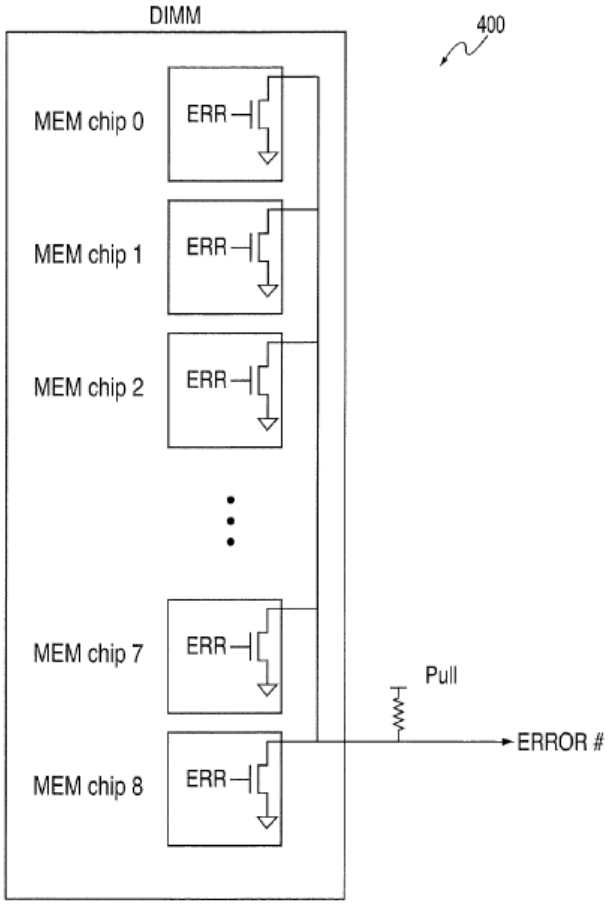

FIG. 4

Kim's Figure 4 shows "a block diagram of a memory module [400] having an error feedback pin that is shared among multiple device[s]." *Id.* at 3:13–16. Kim's Figure 4 further depicts "the error output line from the memory devices are dotted together via open drain drivers to a single error line that is output from the memory module 400." *Id.* at 6:1–3.

Kim's Figure 5 is reproduced below.

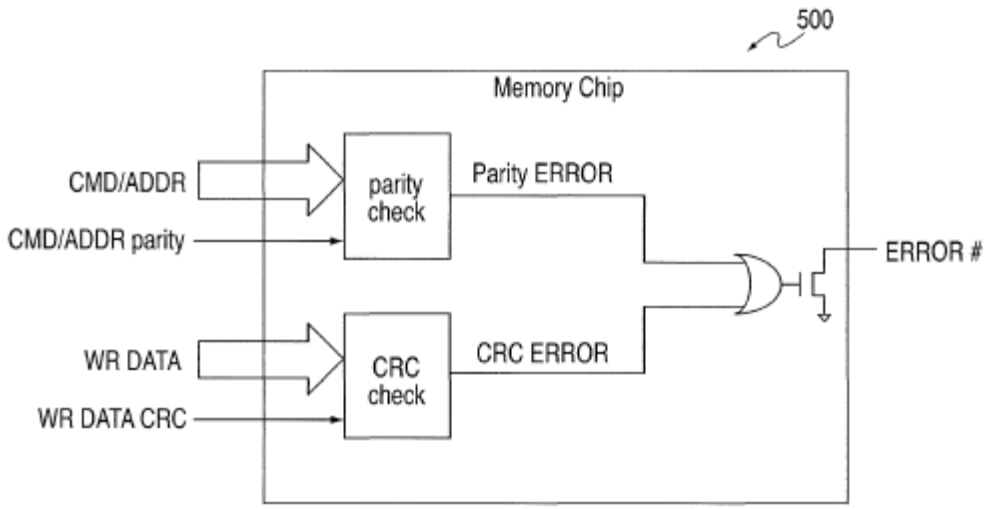

FIG. 5

Kim's Figure 5 depicts "a block diagram of a memory device 500 that shares an error feedback pin between data CRC and address parity." *Id.* at 6:13–15.

2. Analysis

Petitioner contends that Kim teaches an "'open drain output' with an output pin coupled to the drain of a transistor, which includes a gate, a source, and a drain." Pet. 69 (citing Ex. 1017, Fig. 4). Petitioner also contends that Kim discloses "using a logic element (an OR gate) such that multiple error signals could drive the gate of the open-drain transistor." *Id.* at 70 (citing Ex. 1017, 6:13–18, Fig. 5). Petitioner proposes combining Kim's "open drain transistor configuration" with Hazelzet's error logic circuit 100 "such that signals indicating parity mode error, ECC mode error and training status would be provided to a logic gate, such as an OR gate, as in Kim, which would select among them based on the mode of the module,

as in Hazelzet." Pet. 71 (emphasis omitted). Petitioner contends the combined circuit would include the transistor configurations and signaling recited in claims 3–5 (Ex. 1003 ¶¶ 265, 276, 283), the multiplexor configuration recited in claims 6, 13 and 22 (Ex. 1003 ¶¶ 161, 180, 196), the open drain training sequence signals of claims 7 and 14 (Ex. 1003 ¶¶ 163, 181), and the transistor signaling of claims 12, 20, and 23 (Ex. 1003 ¶¶ 180, 187, 197). Pet. 73.

Petitioner contends that a person of ordinary skill in the art would be motivated to combine Kim with Hazelzet and Buchmann because (1) Kim is assigned to the same company as Hazelzet and contains some of the same disclosures, as well as some additional disclosures; (2) using the output-pin scheme of Kim in the system of Hazelzet would have been "the use of known techniques for their known purposes to achieve predictable results, i.e., using an open-drain output to provide error or status information from multiple components"; (3) "it represented a well-known (and therefore reliable) and simple technique to provide error and/or status information from a number of components and in different modes"; and (4) it would "simplify[] the design of the system and sav[e] pins on the various integrated circuits connected to the bus." *Id.* at 73–74 (citing § V.E; Ex. 1017, 1:16–22, 5:49–57, 5:65–6:18, Figs. 4, 5; Ex. 1003 ¶¶ 251, 257, 267–270, 330–335, 353, 372, 374; Ex. 1014 ¶¶ 72, 122).

Beyond the arguments previously addressed, Patent Owner does not specifically address these assertions. *See* Resp. Based on our review and consideration of the record, we determine that Petitioner has shown that one of ordinary skill in the art would have had reason to combine Hazelzet, Buchmann, and Kim, and that the combination teaches the limitations in

claims 3–7, 12–14, 20, 22, and 23. As Dr. Alpert establishes, Kim's disclosure overlaps substantially with Hazelzet, and discloses additional details regarding use of an open-drain output on a memory module to notify a memory controller of errors during parity and ECC modes, as well as initialization operations to train a memory module and output training status on a shared error feedback pin. Ex. 1003 ¶¶ 166–169. Thus, we determine that Petitioner has established by a preponderance of the evidence that claims 3–7, 12–14, 20, 22, and 23 of the '595 patent are unpatentable as obvious over the combination of Hazelzet, Buchmann, and Kim.

G. Motions to Exclude

1. Patent Owner's Motions to Exclude

Patent Owner seeks to exclude Exhibits 1015, 1024–1025, 1036–1037, 1039, 1048–1049, 1051, 1056, 1071–1076, and 1080–1081. Paper 45, 9–14.

We did not rely on Exhibits 1015, 1037, 1039, 1048, 1049, 1051, 1071–1076 or 1080–1081 in rendering this Final Written Decision. Consequently, Patent Owner's Motion to Exclude is moot as to these Exhibits.

Patent Owner contends that Exhibits 1024–1025, 1036–1037, and 1056 should be excluded because they are not authenticated. FRE 901(a). Petitioner contends that some of these Exhibits are authenticated by the declaration of Julie Carlson (Ex. 1050) who was responsible for "maintenance and publication of JEDEC documents and standards" and a declaration from "Sung Joo Park, who participated in JEDEC at the relevant time and has personal knowledge of the documents he authenticates." Ex. 1055 ¶ 5. Paper 48, 6. Petitioner contends these declarations

authenticate Exhibits 1036 and 1037. We agree. Petitioner contends that Exhibits 1024–1025 and 1056 "are similar JEDEC documents and contain the same indicia of authenticity under FRE 901(b)(4) and 902(7), including similar cover pages, tables of contents, fonts, logos, technical contents, and revision logs." *Id.* We agree and determine that sufficient evidence has been provided to authenticate these Exhibits.

Patent Owner further contends we should exclude Exhibits 1024–1025, 1036–1037, and 1056 because they are inadmissible hearsay under FRE 801 and 802. Paper 45, 12–14. Petitioner contends that the declaration of Julie Carlson establishes that Exhibits 1036–1037 are business records of JEDEC under FRE 803(6) as of the dates shown on the documents. Paper 48, 13. We agree that Exhibits 1036–1037 fall under the business records exception to the hearsay rule.

Comparison of Exhibits 1036 and 1037 to Exhibits 1024, 1025, and 1056 leads us to conclude that these Exhibits also are authenticated business records (standards or committee letter ballots) of JEDEC. They have similar cover pages, tables of contents, fonts, logos, technical contents, and revision logs. Patent Owner has introduced no evidence to suggest that these Exhibits are not what they appear to be.

Consequently, Patent Owner's Motion to Exclude is *dismissed-in-part* as moot as to Exhibits 1015, 1037, 1039, 1048, 1049, 1051, 1071–1076, and 1080–1081, and is *denied-in-part* as to Exhibits 1024–1025, 1036–1037, and 1056.

2. Petitioner's Motions to Exclude

Petitioner seeks to exclude Exhibit 2017 and paragraphs 20–21 of Exhibit 2026. Paper 46, 1. We *dismiss* Petitioner's Motion to Exclude as

moot because we did not rely on Exhibits 2017 or 2026 to reach our Final Written Decision.

III. CONCLUSION

For the foregoing reasons, we determine that Petitioner establishes by a preponderance of the evidence that claims 1–24 of the '595 patent are unpatentable.

IV. ORDER

Accordingly, it is:

ORDERED that claims 1–24 of the '595 patent have been shown to be unpatentable;

FURTHER ORDERED that Patent Owner's Motion to Exclude is *dismissed-in-part* as moot as to Exhibits 1015, 1037, 1039, 1048, 1049, 1051, 1071–1076, and 1080–1081, and is *denied-in-part* as to Exhibits 1024–1025, 1036–1037, and 1056;

FURTHER ORDERED that Petitioner's Motion to Exclude is dismissed; and

FURTHER ORDERED that any party seeking judicial review must comply with the notice and service requirements of 37 C.F.R. § 90.2.[12]

In summary:

Claim(s)	35 U.S.C. §	Reference(s)/Basis	Claim(s) Shown Unpatentable	Claim(s) Not shown Unpatentable
1–24	103[13]	Hazelzet, JEDEC		
1–24	103	Hazelzet, Buchmann	1–24	
3–7, 12–14, 20, 22, 23	103	Hazelzet, Buchmann, Kim	3–7, 12–14, 20, 22, 23	
Overall Outcome			1–24	

[12] Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this Decision, we draw Patent Owner's attention to the April 2019 Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding. *See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

[13] We do not reach this ground for the reasons discussed in Section II.D.

FOR PETITIONER:

Eliot D. Williams
Neil P. Sirota
Theodore W. Chandler
Stephanie C. Kato
Ferenc Pazmandi
BAKER BOTTS LLP
eliot.williams@bakerbotts.com
neil.sirota@bakerbotts.com
ted.chandler@bakerbotts.com
stephanie.kato@bakerbotts.com
ferenc.pazmandi@bakerbotts.com

FOR PATENT OWNER:

Sarah Spires
Rex Hwang
SKIERMONT DERBY LLP
sspires@skiermontderby.com
rhwang@skiermontderby.com