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Paper 53
Date: May 3, 2023

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

IPR2022-00063
Patent 10,217,523 B1

Before JON M. JURGOVAN, SHEILA F. McSHANE, and KARA L. SZPONDOWSKI, *Administrative Patent Judges*.

SZPONDOWSKI, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining No Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

We instituted an *inter partes* review of claims 1–34 of U.S. Patent No. 10,217,523 B1 (Ex. 1001, "the '523 patent"), in response to a Petition (Paper 1, "Pet.") filed by Samsung Electronics Co., Ltd. ("Petitioner"). Paper 13 ("Dec."). During the trial, Netlist, Inc. ("Patent Owner") filed a Response to the Petition (Paper 28, "PO Resp."), Petitioner filed a Reply (Paper 31, "Reply"), and Patent Owner filed a Sur-reply (Paper 34, "Sur-reply"). In addition, both parties filed Motions to Exclude Evidence (Papers 43 ("PO Mot. Excl."), 44 ("Pet. Mot. Excl.)), Oppositions to the motions (Papers 45 ("PO Opp. Excl."), 46 ("Pet. Opp. Excl.)), and Replies to the Oppositions (Papers 48 ("Pet. Reply Excl.), 50 ("PO Opp. Excl.)).

An oral hearing was held on February 1, 2023, and a copy of the transcript was entered into the record. Paper 52 ("Tr.").

We have jurisdiction under 35 U.S.C. § 6. This Decision is a Final Written Decision under 35 U.S.C. § 318(a) as to the patentability of the claims on which we instituted trial. Based on the complete record, Petitioner has not shown, by a preponderance of the evidence, that claims 1–34 of the '523 patent are unpatentable.

II. BACKGROUND

A. Real Parties in Interest

Petitioner identifies Samsung Electronics Co., Ltd. and Samsung Semiconductor, Inc. as real parties in interest. Pet. 1. Patent Owner identifies itself as the sole real party in interest. Paper 3, 3.

B. Related Matters

Petitioner indicates *Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.,* No. 1:21-cv-01453 (D. Del. filed Oct. 15, 2021) involves the '523

patent. Pet. 1. Petitioner and Patent Owner also identify many other related matters. Pet. 1–3; Paper 3, 3–5; Paper 5.

The Board previously instituted trial in IPR2020-01421 on the same claims of the '523 patent and on the same grounds presented here, but with different petitioners. *See* Ex. 1043. That IPR was terminated after institution because settlement was reached. Ex. 1044.

C. The '523 Patent (Ex. 1001)

The '523 patent is titled "Multi-Mode Memory Module with Data Handlers" and issued on February 26, 2019, from an application filed on March 29, 2014. Ex. 1001, codes (22), (45), (54).

The '523 patent is directed to a self-testing memory module for testing a plurality of memory devices mounted thereon. Ex. 1001, 5:4–27. Figure 2, reproduced below, is a block diagram illustrating component blocks of memory module 10 and memory controller 14. *Id*. at 5:28–34, 8:41–62, 9:22–42, Fig. 2.

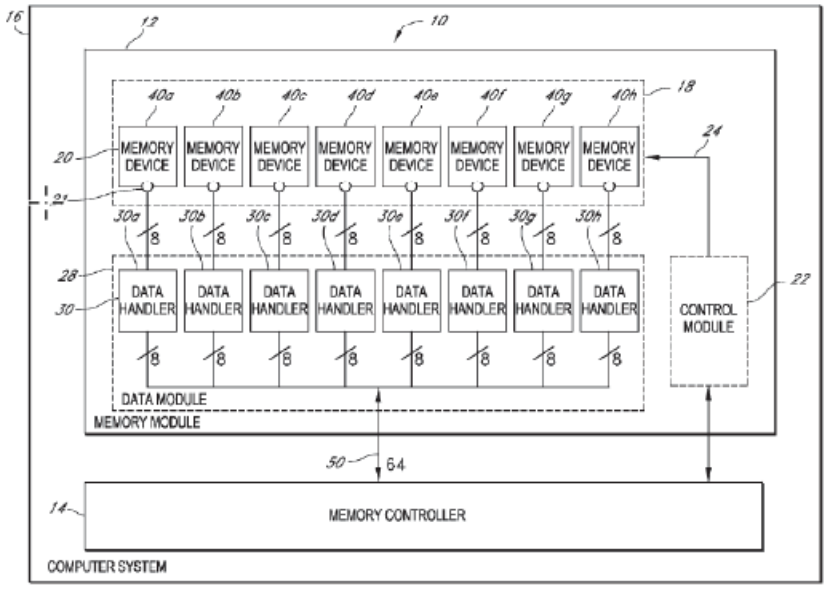


FIG. 2

Figure 2, above, shows memory module 10 includes control module 22 that generates address and control signals for testing memory devices 20 and data module 28 that includes a plurality of distributed data handlers 30. Ex. 1001, 5:12–16. Data handlers 30 of data module 28 generate test patterns to write to memory devices 20 and compare test patterns read from memory devices 20 to the written patterns to identify faults. *Id.* at 5:28–34.

Figure 3, reproduced below, provides additional detail regarding the control module, data handlers and their components and interconnections. Ex. 1001, Fig. 3.

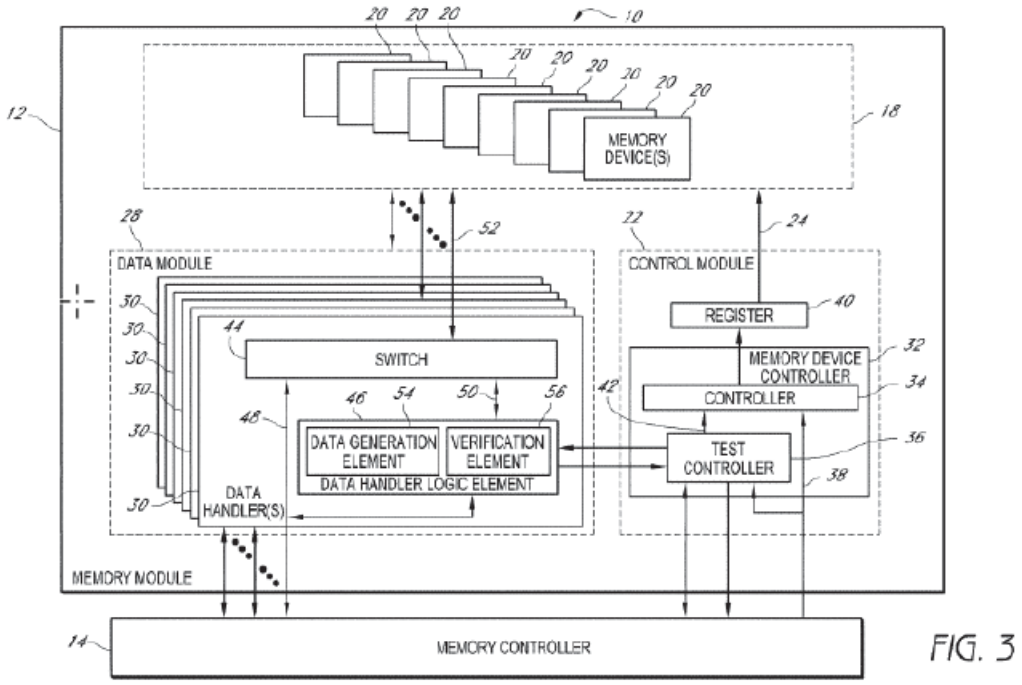


FIG. 3

Figure 3, above, shows additional control module 22, data module 28, plurality of memory devices 18, and certain components thereof. Ex. 1001, 9: 32–36, Fig. 3. Control module 22 includes memory device controller 32 with memory controller 34 and test controller 36. *Id*. at 9:38–40, Fig. 3. Data module 28 includes data handlers 30, switch 44, and data handler logic

element 46, which includes data generation element 54 and verification element 56. *Id*. at 10:7–21, 10:38–40.

"In one embodiment, the memory device controller 34 receives signals 38 (e.g., address and control signals) from the system memory controller 14 and signals 42 (e.g., address and controls signals) from the test controller 36." *Id.* at 9:45–49. "The control module 22 of certain embodiments is configured to selectively input to the address and control ports of the plurality memory devices 18 either the address control signals 38 from the system memory controller 14 or the address and control signals 42 from the control module 22 (e.g., from the test controller 36)." *Id.* at 9:49–55. "For example, the memory device controller 34 may send either the signals 38 from the system memory controller 14 or, alternatively, the signals 42 from the test controller 36, to the register 40 depending on whether the memory module 10 is in normal (non-test) mode or in a test mode, respectively." *Id.* at 9:55–60. "The test controller 36 controls the generation of the address and control signal sequences to be used during the self-testing operation of the memory module 10 and also communicates with the data module 28." *Id.* at 9:63–66.

"The data module 28 . . . may be in communication with one or more of the memory devices 20, the control module 22, and the memory controller." *Id.* at 10:7–10. "Each of the data handlers 30 of certain embodiments comprises a switch 44," which "may include a data multiplexer/demultiplexer." *Id.* at 10:13–15. "In certain embodiments, the switch 44 is configured to selectively input to the corresponding plurality of data ports either data signals 48 from the system memory controller 14 or data signals 50 from the data handler logic elements 46." *Id.* at 10:17–21.

"The switch 44 of certain embodiments may further be configured to receive data signals 52 (e.g., during a read operation) from the plurality of memory devices 18 and to propagate the data signals 52 to the data handler logic element 46 and/or the memory controller 14." *Id.* at 10:21–25. "In some embodiments, for example, the switch 44 selectively inputs the data signals 48 to be written to the plurality of memory devices 18 from the system memory controller 14 when the memory module 10 is a normal (non-test mode) mode and, alternatively, inputs the data signals 50 from the data handler logic element 46 during a test mode." *Id.* at 10:26–31.

D. Illustrative Claims

Petitioner challenges claims 1–34 of the '523 patent. Pet. 5–6. Claims 1 and 19 are independent. Ex. 1001, 16:55–17:30, 19:4–45. Claim 1, reproduced below with brackets noting Petitioner's identifiers, is illustrative of the subject matter of the challenged claims:

> 1. [a] A memory module accessible in a computer system by a system memory controller via a system memory bus, comprising:
>
> [b] memory devices mounted on a circuit board, the memory devices having address and control ports and data ports;
>
> [c] a data module mounted on the circuit board and coupled between the data ports of the memory devices and the system memory bus, the data module including data handler logic elements;
>
> [d] a control module mounted on the circuit board and coupled to the data module, the address and control ports of the memory devices, and the system memory bus; and
>
> [e] wherein the memory module is operable in any of a plurality of modes including a first mode and a second mode;
>
> [f] [i] wherein the control module in the first mode is configured to receive system address and control signals from the system memory controller and to output first memory

address and control signals to the memory devices according to the system address and control signals, and [ii] the data module in the first mode is configured to propagate one or more first data signals between the memory devices and the system memory controller, [iii] the one or more first data signals being transmitted or received by at least a portion of the memory devices in response to the first memory address and control signals; and

[g] [i] wherein the control module in the second mode is configured to output second memory address and control signals to the address and control ports of the memory devices, and [ii] the data module in the second mode is configured to isolate the memory devices from being accessed by the system memory controller and to transmit one or more second data signals including data patterns provided by the data handler logic elements to the data ports of the memory devices according to one or more commands output from the control module, and [iii] wherein at least a portion of the memory devices are configured to receive the one or more second data signals according to the second memory address and control signals from the control module.

Ex. 1001, 16:55–17:30.

E. Prior Art and Asserted Grounds

Petitioner asserts that claims 1–34 of the '523 patent are unpatentable based on the following grounds:

Claims Challenged	35 U.S.C. §[1]	Reference(s)
1–34	103(a)	Ellsberry,[2] Jeddeloh[3]
1–34	103(a)	Ellsberry, Jeddeloh, Averbuj[4]
14, 17–34	103(a)	Ellsberry, Jeddeloh, Lee[5]
14, 17–34	103(a)	Ellsberry, Jeddeloh, Averbuj, Lee

Pet. 5–6.

In addition, Petitioner relies on the Declarations of Dr. Vivek Subramanian (Exs. 1003, 1061). Patent Owner relies on the Declarations of Dr. Michael Brogioli (Exs. 2001, 2004). Deposition transcripts have been entered into the record for Dr. Subramanian (Exs. 2005, 2016) and Dr. Brogioli (Ex. 1064).

III. ANALYSIS

A. Legal Standards

A claim is unpatentable under 35 U.S.C. § 103(a) if "the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

[1] The Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) ("AIA"), amended 35 U.S.C. § 103, and was effective on March 16, 2013. Because the '523 patent has a filing date before the effective date of the applicable AIA amendments, we refer to the pre-AIA versions of 35 U.S.C. § 103.
[2] US Pub. No. 2006/0277355 A1, published December 7, 2006. Ex. 1005.
[3] US 7,310,752 B2, issued December 18, 2007, claiming priority to Application No. 10/660,844, filed on Sept 12, 2003. Ex. 1006.
[4] US Pub. No. 2005/0257109 A1, published November 17, 2005. Ex. 1007.
[5] US Pub. No. 2006/0095817 A1, published May 4, 2006. Ex. 1008.

invention was made to a person having ordinary skill in the art to which said subject matter pertains." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) objective evidence of nonobviousness, i.e., secondary considerations.[6] *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

A patent claim "is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art." *KSR*, 550 U.S. at 418. An obviousness determination requires finding "both 'that a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention, and that the skilled artisan would have had a reasonable expectation of success in doing so.'" *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1367–68 (Fed. Cir. 2016); *see KSR*, 550 U.S. at 418. Further, an assertion of obviousness "cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *KSR*, 550 U.S. at 418; *In re NuVasive, Inc.*, 842 F.3d 1376, 1383 (Fed. Cir. 2016) (a finding of a motivation to combine "must be supported by a 'reasoned explanation'").

B. Level of Ordinary Skill in the Art

Petitioner contends a person of ordinary skill in the art at the time of the invention would have a "Bachelor's degree in electrical engineering,

[6] The parties did not present evidence relating to objective indicia of nonobviousness.

computer engineering, or in a related field and at least one year of work experience relating to memory systems, and would be familiar with the design of memory devices, memory modules, and BIST." Pet. 6. Petitioner contends that this level of ordinary skill in the art was adopted by the Board in IPR2014-00970, which challenged U.S. Patent No. 8,001,434 ("'434 patent"). *Id.* The '523 patent is a continuation of the '434 patent. Ex. 1001, code (63).

In our Institution Decision, we preliminarily adopted Petitioner's unopposed[7] proposed level of ordinary skill in the art. Paper 13, 14. In the Response, Patent Owner does not challenge Petitioner's characterization of the level of ordinary skill in the art, and Dr. Brogioli testifies that "I accept this proposed level of ordinary skill in the art." PO Resp. 6; *see* Ex. 2004 ¶ 22. Nothing in the full record persuades us that our preliminary finding as to the level of ordinary skill in the art was incorrect. Accordingly, we maintain our adoption of Petitioner's proposed level of ordinary skill in the art, as consistent with the level of ordinary skill in the art reflected by the prior art of record. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).

C. Claim Construction

We construe each claim "in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent," the same standard used to construe the claim in a civil action. 37 C.F.R. § 42.100(b) (2020). Under this standard, the words of a claim generally are given their

[7] Patent Owner did not challenge the proposed level of ordinary skill in the art in the Preliminary Response. Paper 7, 5.

"ordinary and customary meaning," which is the meaning the term would have to a person of ordinary skill at the time of the invention, in the context of the entire patent including the specification. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc).

For the terms "configured to" and "operate independently," Petitioner offers the Board's previous construction in IPR2014-00970, and further states that the Board declined to construe these terms in IPR2020-01421. Pet. 13. For the term "rank," Petitioner offers a construction, and also contends that the Board declined to construe this term in IPR2020-01421. *Id.* However, for each of the foregoing three terms, Petitioner also contends that "[e]ither way, the prior art invalidates the 523 Patent." *Id.* Petitioner contends that the term "mode" should be given its plain and ordinary meaning, and also offers the construction adopted by the district court in the Western District of Texas, and further contends that the Board declined to construe this term in IPR2020-01421. *Id.* at 14. For the terms "data handler," "data handler logic element[s]," and "data module," Petitioner provides the constructions adopted by the district court in the Western District of Texas. *Id.* at 14–15.

Although in Response, Patent Owner states "[t]o the extent Petitioner or its expert have proffered or applied constructions inconsistent with the plain and ordinary meaning of these terms, Patent Owner explicitly disagrees with those constructions," in the Sur-reply, Patent Owner states that "the Board needn't construe any disputed terms because . . . they do not bear on the issues in dispute." PO Resp. 4; Sur-reply 1.

We agree with Patent Owner that it is not necessary to provide an express interpretation of any terms for purposes of this Decision. *See*

Realtime Data, LLC v. Iancu, 912 F.3d 1368, 1375 (Fed. Cir. 2019) ("The Board is required to construe 'only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.'" (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

D. Ground 1: Obviousness Based on Ellsberry and Jeddeloh

Petitioner contends claims 1–34 would have been obvious over the combination of Ellsberry and Jeddeloh. Pet. 26–104. After reviewing the entire record developed at trial, we determine that Petitioner has not shown, by a preponderance of the evidence, that claims 1–34 are unpatentable over Ellsberry and Jeddeloh.

1. Ellsberry (Ex. 1005)

Ellsberry relates to "a device, system, and method for expanding the memory capacity of a memory module." Ex. 1005, code (57). "A control unit and memory bank switch are mounted on a memory module to selectively control write and/or read operations to/from memory devices communicatively coupled to the memory bank switch." *Id.* "By selectively routing data to and from the memory devices, a plurality of memory devices may appear as a single memory device to the operating system." *Id.*

Figure 2 of Ellsberry, reproduced below, "illustrates a block diagram of a capacity-expanding memory system 200 according to one embodiment." *Id.* ¶ 28. System 200 has DIMM (dual inline memory module) interface 202 that couples to a memory socket and communication bus over which data, memory addresses, commands, and control information are transmitted. *Id.* The capacity-expanding feature of the invention is accomplished by a combination of control unit 204 and one or more memory bank switches 206, 208. *Id.*

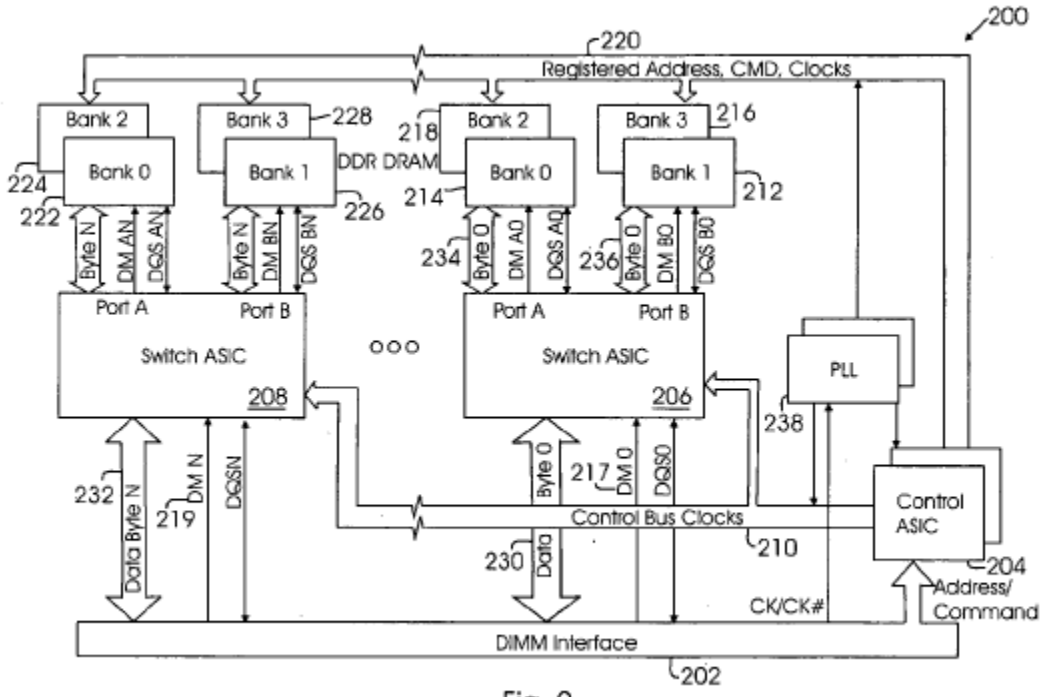


Fig. 2

Figure 2 of Ellsberry, above, illustrates system 200 with control ASIC 204 that receives addresses and commands from DIMM interface 202 and generates corresponding control signals on bus 210 and addresses and command information on bus 220 to selectively connect memory banks 212–228 to DIMM interface 202 via switch ASICs 206, 208. *Id*. ¶¶ 28–29.

Specifically, control unit 204 receives memory addresses and commands from DIMM interface 202 and controls switches 206 and 208 via control bus 210 to indicate how data from DIMM interface 202 should be received from and/or stored in memory banks 212–228. *Id*. ¶¶ 29–30, Fig. 2. Control unit 204 also generates address and command information on address bus 220 to access memory banks 212–228. *Id.* Switches 206 and 208 receive data from, or provide data to, DIMM interface 202 via data buses 230 and 232. *Id.*

Control unit 404 and switches 206 and 208 are further illustrated in Figures 3 and 4. Figure 3, reproduced below, "illustrates a block diagram of an address and command processing system 300" which "may be implemented as part of the control unit 204." *Id.* ¶ 39.

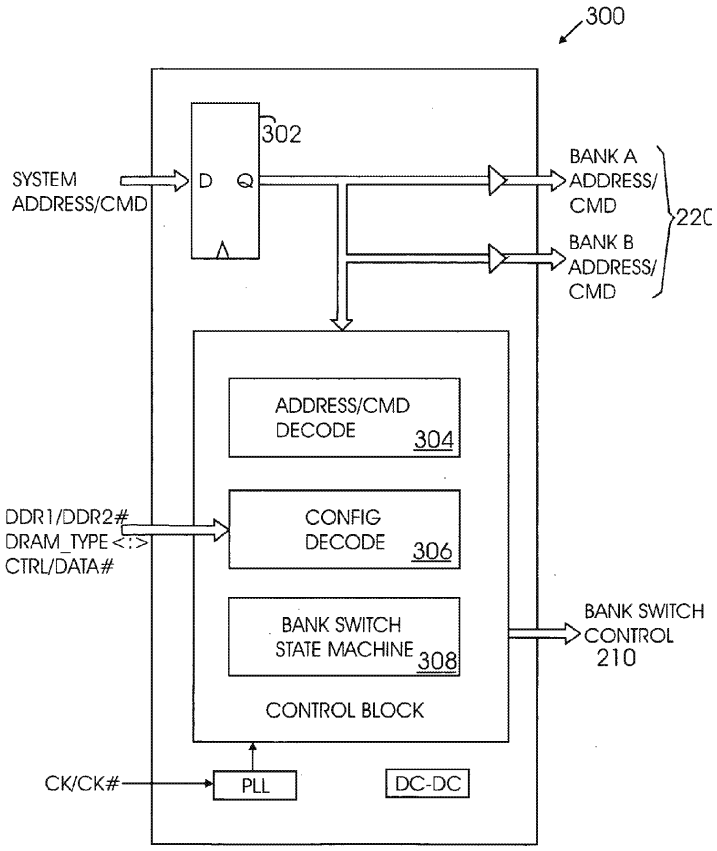


Fig. 3

Figure 3, above, depicts that "[m]emory addresses and command information are received from the DIMM interface 202, buffered in a register 302 and sent to all memory banks . . . over address bus 220." *Id.* In addition, "[t]he memory address and command information is also decoded 304 and memory configuration information 306 is determined." *Id.* "A bank switch state machine 308 then determines which memory bank should be activated or accessed." *Id.* "The state machine 308 sends control

information to the memory bank switches 206 & 208 via the control bus 210 to indicate which memory banks should be activated/deactivated or accessed." *Id.*

Figure 4, reproduced below, "illustrates a block diagram of a data processing system 400," which "may be implemented as part of the memory bank switch 206." *Id.* ¶ 45.

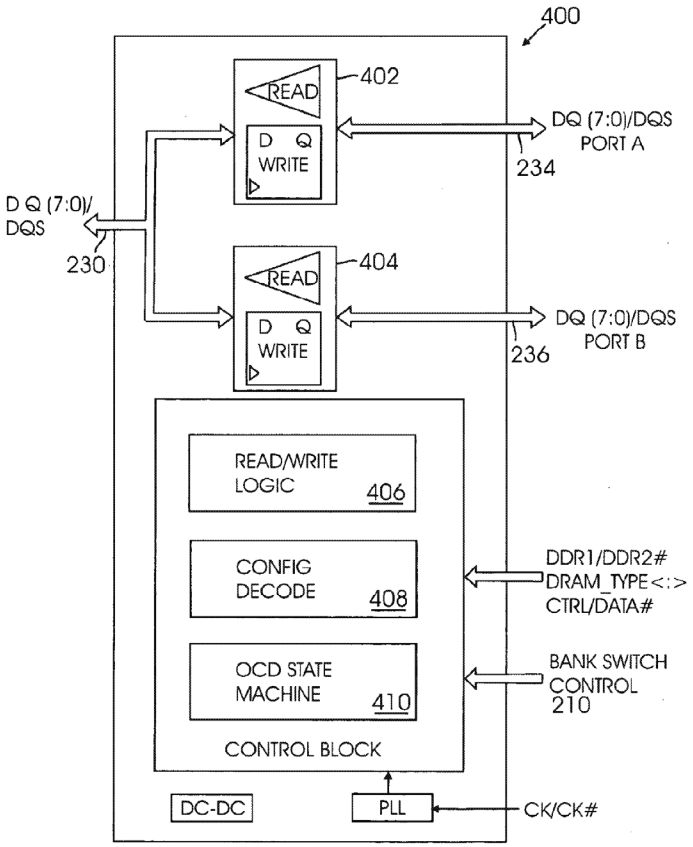


Fig. 4

Figure 4, above, depicts that "[d]ata is transmitted from the DIMM interface 202 via the data bus 230 to bidirectional signal drivers 402 & 404 that transmit and receive data over separate data busses 234 and 236 to the different sets of memory banks." *Id.* "A read/write logic unit 406 determines whether data is being read from or written to the memory devices

(e.g., 212)." *Id.* "Memory configuration information 408 is obtained from the control unit." *Id.*

2. Jeddeloh (Ex. 1006)

Jeddeloh relates to "[a] memory module [that] includes several memory devices coupled to a memory hub [that] includes several link interfaces coupled to . . . a self-test module." Ex. 1006, code (57).

Jeddeloh's Figure 2, reproduced below, shows an embodiment of a memory hub 200.

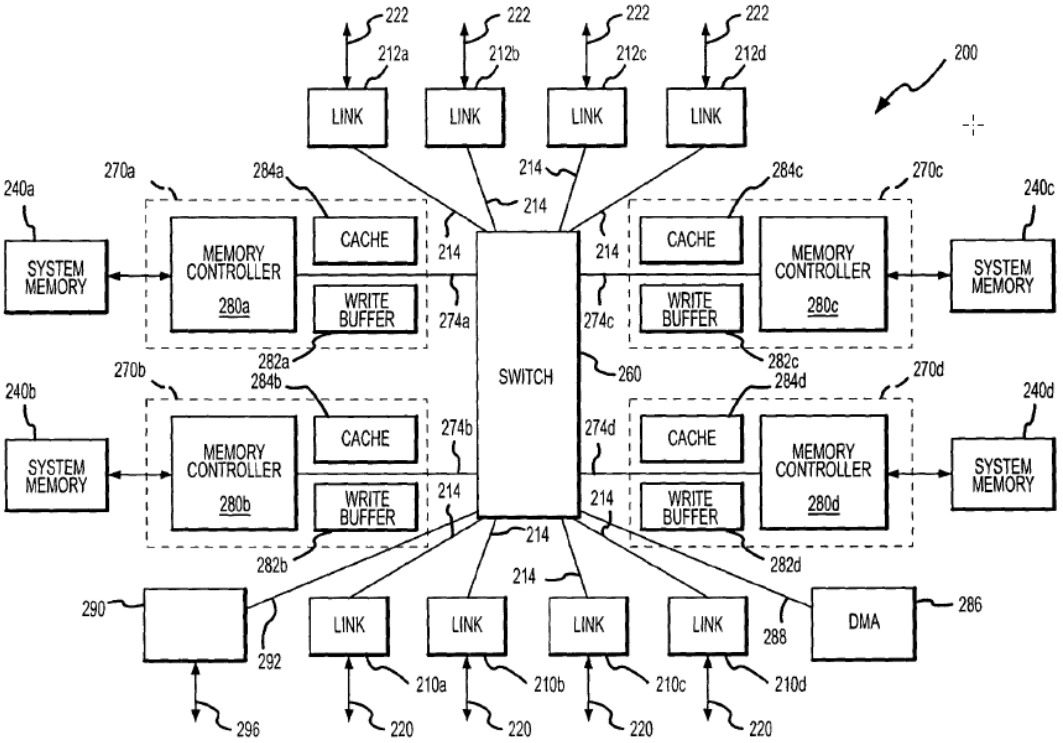


FIG.2

Figure 2, above, depicts memory hub 200 coupled to memory devices 240a-d. Link interfaces 210a-d and 212a-d are coupled to switch 260, and switch 260 is further coupled to memory interfaces 270a-d, which are, in turn, coupled to memory devices 240a-d. Each of the memory interfaces

270a-d includes a memory controller 280a-d, a write buffer 282a-d, and a cache memory unit 284a-d. Self-test module 290 is coupled to the switch 260 through a test bus 292.

Jeddeloh's Figure 3, reproduced below, illustrates a self-test module 308:

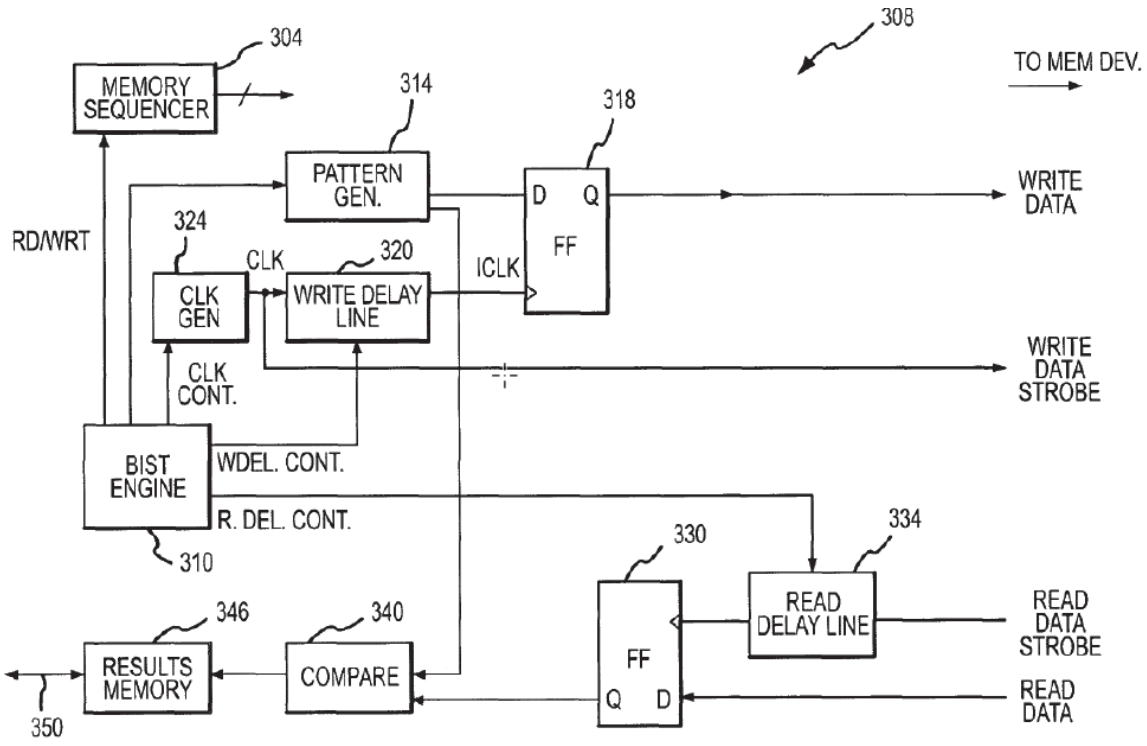


FIG.3

Figure 3 above, shows self-test module 308, including BIST (built-in self test) engine 310 and memory sequencer 304 that generate and distribute address and command/control signals during testing, and pattern generator 314, compare circuit 340, and results memory 346 that generate, distribute, and compare test patterns, and store fault information. *Id.* at 9:57–67, 10:30–51. Jeddeloh states that Figure 3 "is a functional block diagram representative of a suitable self-test module," and "[t]he functional blocks shown . . . are conventional, and can be implemented using well known

techniques and circuitry." *Id.* at 9:45–50. Jeddeloh also discloses use of a SMBus to communicate with off-module components, for instance, a test apparatus can use it to "set memory testing parameters and receive test results." *Id.* at 8:26–53, 10:47–51.

3. Analysis of Independent Claim 1

Petitioner asserts that Ellsberry alone or Ellsberry combined with Jeddeloh teaches all the limitations in claim 1, and that one of ordinary skill in the art would have been motivated to combine Ellsberry and Jeddeloh. Pet. 26–61. Petitioner relies on Ellsberry to teach limitations 1[a], 1[b], 1[d], 1[f][i], 1[f][ii], 1[f][iii], and on the combination of Ellsberry and Jeddeloh to teach limitations 1[c], 1[e], and 1[g][i], 1[g][ii], and 1[g][iii]. *Id.* at 37–61. Petitioner contends it would have been obvious to modify Ellsberry with Jeddeloh's teachings to include self-test functionality, and to distribute Jeddeloh's test circuit functionality among Ellsberry's Control ASIC and Switch ASICs. *Id.* at 25–37.

a) Petitioner's Proposed Combination

Petitioner contends that Ellsberry discloses a memory module (limitation 1[a]) that separates circuitry into handling address and control signals and handling data signals, as shown in Petitioner's annotated Figure 2 below. Pet. 26–27, 38 (citing Ex. 1005, Fig. 2).

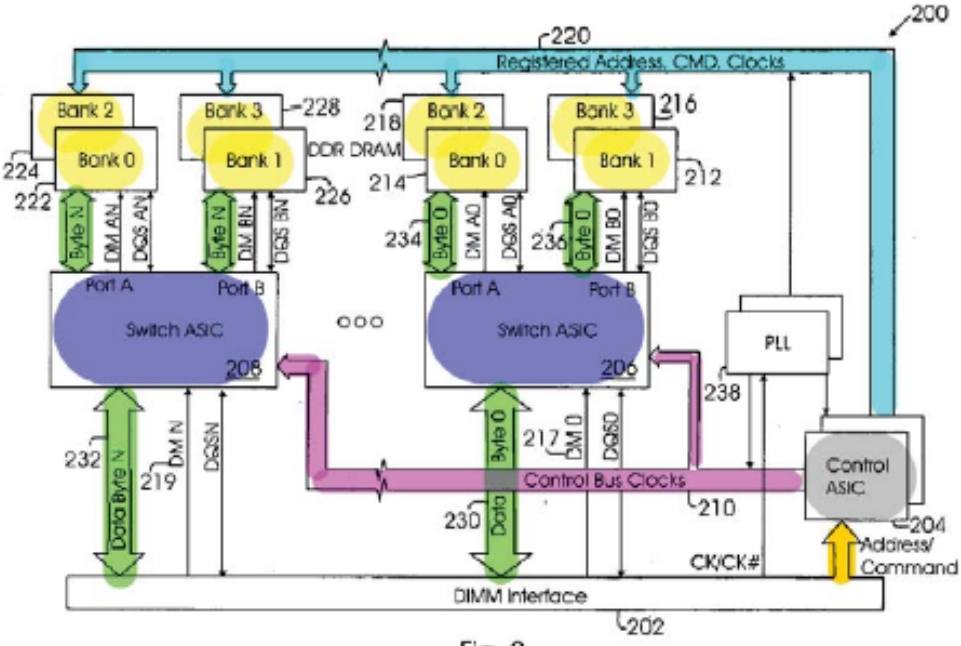


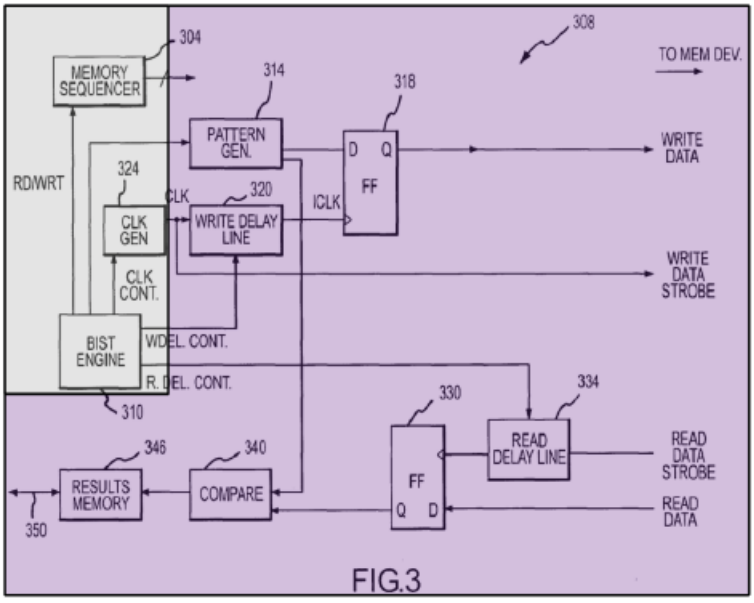
Fig. 2

Petitioner's annotated Figure 2 of Ellsberry above shows address/control signals are handled by Control ASIC 204 (grey) and data signals are handled by a plurality of distributed Switch ASICs 206 thru 208 (purple). *Id*. at 26–27. According to Petitioner, Control ASIC 204 is coupled to Switch ASICs (purple) via bus 210 (pink), and ASIC 204 is also coupled to the address and control ports of the memory devices (DRAMs) (yellow) via bus 220 (blue). *Id.* at 44. Petitioner asserts that Control ASIC 204 receives system address and control signals over DIMM interface 202 (orange), and outputs address and command signals to the memory devices (yellow) on bus 220 (blue). *Id.* at 48–49. Petitioner further contends that the Switch ASICs (purple) pass data between the memory devices and the memory bus/memory controller (green). *Id.* at 40.

Petitioner contends that Ellsberry's memory devices (DRAMs) teach the claimed "memory devices" (limitation 1[b]), Ellsberry's Switch ASICs

teach the claimed "data module" (limitation 1[c]), and Ellsberry's Control ASIC teaches the claimed "control module" (limitation 1[d]). *Id.* at 38–46.

Petitioner relies on Jeddeloh to teach a test mode with self-test functionality. *Id.* at 26. Jeddeloh discloses a "functional block diagram" of a self-test module, as shown in Petitioner's annotated Figure 3 below. *Id.* at 29 (citing Ex. 1006, Fig. 3).



Petitioner's annotated Figure 3 of Jeddeloh above shows BIST engine 310, clock generator 324, and memory sequencer 304 (in grey) that generate and distribute address and command/control signals during testing, and pattern generator 314, compare circuit 340, and results memory 346 (in purple) that generate, distribute, and compare test patterns, and store fault information. *Id.*

Petitioner contends that Ellsberry teaches operation in a first (normal) mode (limitations 1[e], 1[f][i], 1[f][ii], 1[f][iii]). *Id.* at 46–56. In the first mode, Petitioner contends that Ellsberry's Control ASIC "*receive[s] system address and control signals from the system memory controller*" over

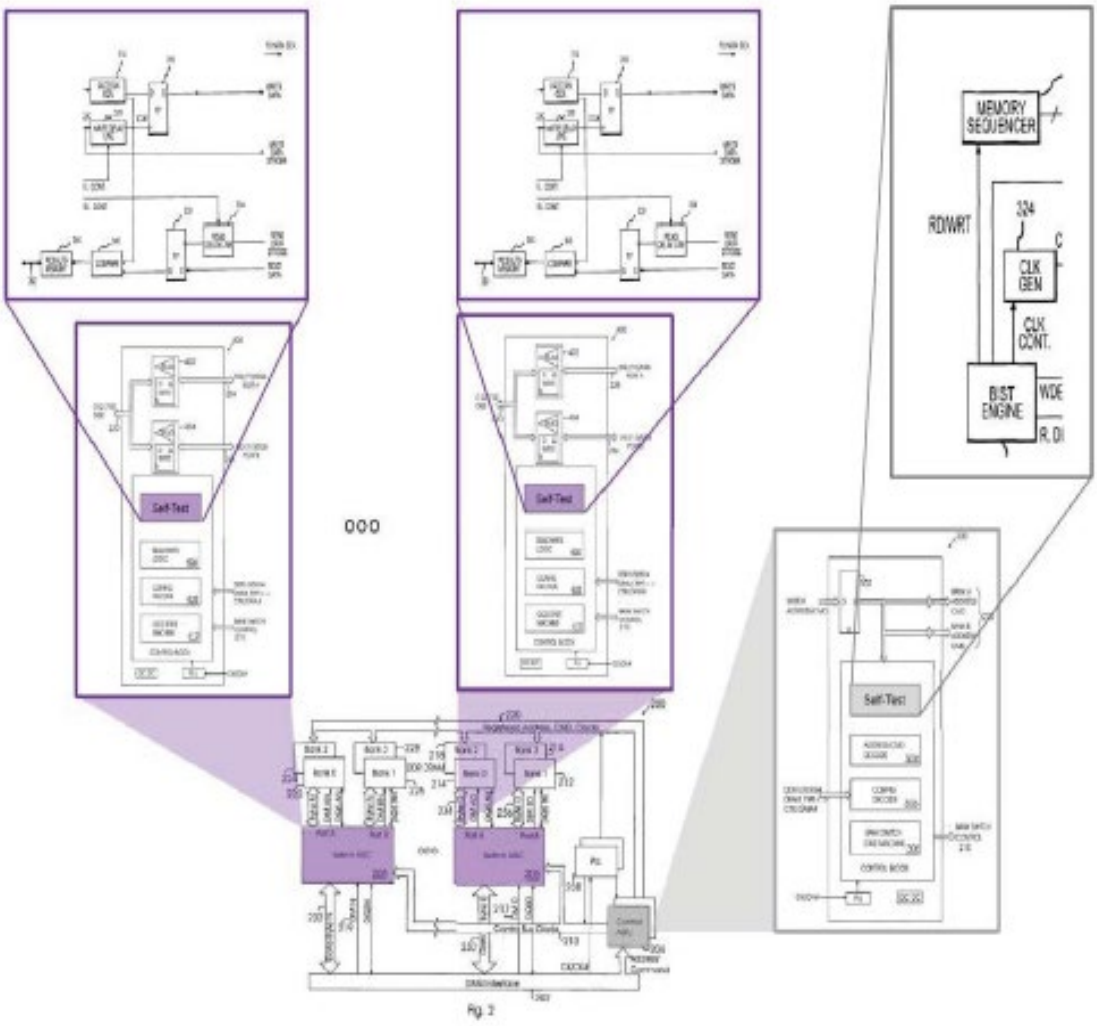
DIMM interface 202 and outputs address and command signals ("*first memory address and control signals*") to the memory devices on bus 220 (limitations 1[f][i], 1[f][iii]). *Id.* at 48–51, 55. Petitioner contends that Ellsberry's Switch ASICs "*propagate*" 8-bit sections of "*first data signals*" between "*the memory devices*" (DRAM) and DIMM interface 202 (connected to the "*system memory controller*") via buses (limitations 1[f][ii], 1[f][iii]). *Id.* at 52–56.

Petitioner contends that, as combined with Jeddeloh, Ellsberry operates in a test (second) mode (limitations 1[e], 1[g][i], 1[g][ii], 1[g][iii])). *Id.* at 48, 56–62. According to Petitioner, the proposed combination is "straightforward": Ellsberry's "memory modules would be modified to include a test mode implementing self-test functionality, such as disclosed in" Jeddeloh. *Id.* at 26. In the proposed combination, Jeddeloh's self-test module is divided between circuitry for handling address/control signals and circuitry for handling data signals. *Id.* at 28. Specifically, "[s]elf-test address/control signal circuitry would be implemented in Ellsberry's Control ASIC to send commands to self-test data signal circuitry implemented in Ellsberry's distributed Switch ASICs and address and control information to the memory devices in order to carry out the testing functionality described in" Jeddeloh. *Id.* (emphasis omitted).

Petitioner contends that the functionality of Jeddeloh's BIST engine 310, clock generator 324, and memory sequencer 304 would be incorporated into Ellsberry's Control ASIC 204, and the functionality of Jeddeloh's pattern generator 314, compare circuit 340, and results memory 346 would be incorporated into Ellsberry's distributed Switch ASICs. *Id.* at 29–30. So, for example, in the proposed combination, the recited "data handler logic

elements" in limitation 1[c] would also include "logic elements implementing the functionality of [Jeddeloh's] pattern generator and compare circuitry." *Id.* at 43.

The proposed combination is shown in Petitioner's annotated compilation of Figures 2, 3, and 4 of Ellsberry and Figure 3 of Jeddeloh, reproduced below. *Id.* at 30 (citing Ex. 1006, 9:46–51, Fig. 3).



Petitioner's annotated compilation of Figures 2, 3, and 4 of Ellsberry and Figure 3 of Jeddeloh, above, shows the following: (1) added "Self-Test" functionality to the control blocks in Ellsberry's Figure 3 (Control ASIC)

and Figure 4 (Switch ASIC); (2) within the new "Self-Test" functionality of the Switch ASIC, Petitioner places the purple annotated sections of Jeddeloh's Figure 3 (i.e., pattern generator 314, compare circuit 340, and results memory 346); and (3) within the new "Self-Test" functionality of the Control ASIC, Petitioner places the grey annotated sections of Jeddeloh's Figure 3 (i.e., BIST engine 310, clock generator 324, and memory sequencer 304). *See* Pet. 29–30.

Petitioner asserts that to enter test mode and carry out the self-test functionality in the proposed combination, the memory module would receive mode commands (e.g., over a maintenance bus), as taught by Jeddeloh. *Id.* at 30 (citing Ex. 1006, 8:26–53, 10:3–6). Petitioner contends that the modified Control ASIC would "*output second memory address and control signals to the address and control ports of the memory devices*" (limitation 1[g][i]), "similar to how [Ellsberry's] Control ASIC outputs address/control signals during normal operation." *Id.* at 56 (citing Ex. 1003 ¶¶ 243–250; Ex. 1006, Fig. 3, 9:51–10:2, 10:24–29). That is, "[t]o carry out that self-test functionality, the self-test circuitry in the modified Control ASIC would send address/control signals to the memory devices (*e.g.*, over Bus 220 of Ellsberry Figure 2)." *Id.* at 30–31. Petitioner contends that in test mode, the address/control signals are generated from Jeddeloh's memory sequencer 304 in the modified Control ASIC and output to the ports of the memory devices 204 (limitations 1[g][i], 1[g][iii]). *Id.* at 61.

Petitioner further contends that "the self-test circuitry in the modified Control ASIC would send . . . command signals to the Switch ASICs (*e.g.*, over Bus 210 of Ellsberry Figure 2)" (limitation 1[g][ii]). *Id.* at 30–31 (citing Ex. 1005 ¶ 56, Fig. 13; Ex. 1006, 10:30–51; Ex. 1003 ¶ 143)

(emphasis omitted). Petitioner contends that the command signals are generated from Jeddeloh's BIST engine in the modified Control ASIC, and therefore teach "*one or more commands output from the control module*." (limitation 1[g][ii]). *Id.* at 60.

Petitioner contends that in the proposed combination, "there are two sources of data for the memory devices: (i) the system memory controller (during normal mode) and (ii) the pattern generator/compare circuit functionality in each Switch ASIC (during test mode)." *Id.* at 57. For limitation [g][ii], Petitioner asserts that "[d]uring test mode, the pattern generator functionality of the modified Switch ASICs '*transmit[s] one or more second data signals including data patterns provided by the data handler logic elements to the data ports of the memory devices*,' similar to how [Ellsberry's] Switch ASICs transmit data during normal operation." *Id.* at 60 (citing Ex. 1003 ¶¶ 273–274; Ex. 1006, Fig. 3, code (54), 10:3–23). According to Petitioner, "[e]ach source communicates data along a different path in the Switch ASICs, so that '*the system memory controller*' is '*isolate[d]*' from the '*memory devices*' during test mode ('*second mode*') according to commands from the Control ASIC ('*control module*')." *Id.* at 57 (citing Ex. 1003 ¶ 255).

Petitioner asserts that "in normal mode [e.g., limitations 1[f][ii], 1[f][iii]], data from the system memory controller will travel over DIMM interface 202 and data buses 230-232, through the Switch ASICs, and over a port bus (e.g., 234 or 236)." *Id.* at 57. According to Petitioner, "within each Switch ASIC, the data travels from the data bus to one of two output ports, such as Port A, according to commands from the Control ASIC." *Id.* Petitioner's annotated Fig. 2, reproduced below, depicts such a path:

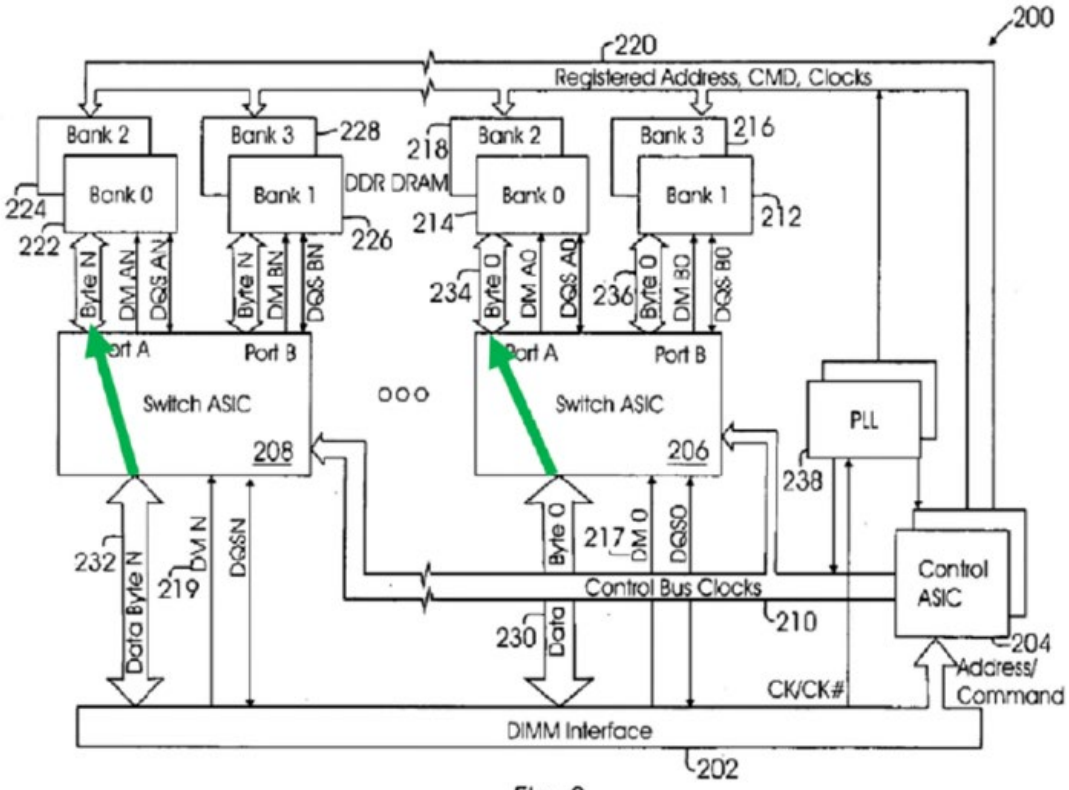
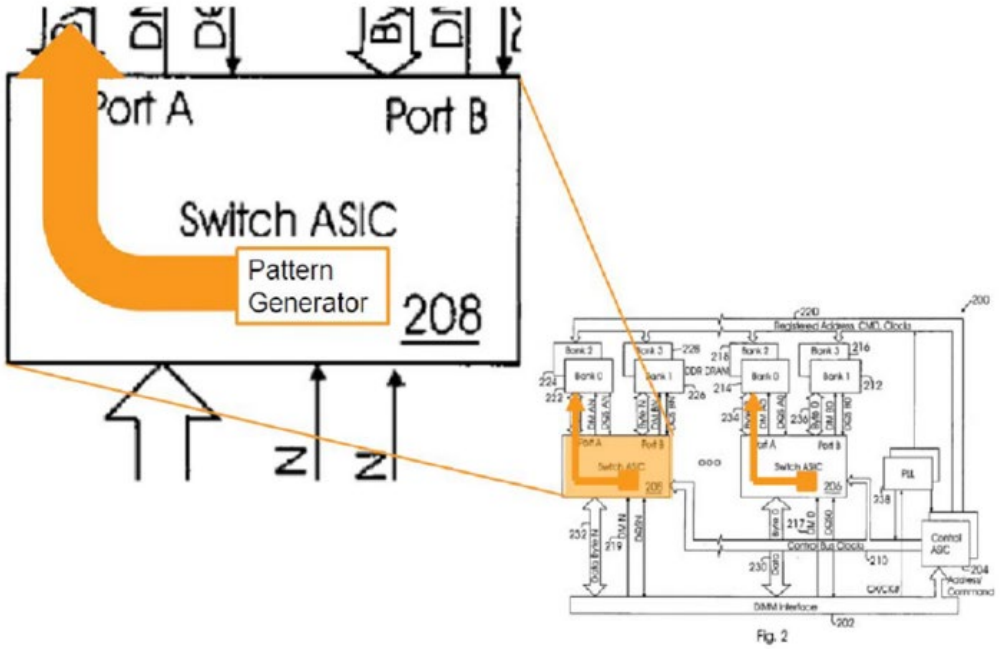


Fig. 2

Id. at 58 (citing Ex. 1003 ¶ 256). Petitioner's annotated Figure 2, above, shows a diagonal green arrow from data bus 232, through Switch ASIC 208, and up to Port A of Bank 0. The same annotation is shown for data bus 230, through Switch ASIC 206, and up to Port A of Bank 0.

Petitioner contends that in the proposed combination, "[i]n test mode, [e.g., limitations 1[g]ii], 1[g][iii]], each Switch ASIC will output data from its pattern generator to the applicable output port, with the Control ASIC signaling the Switch ASIC ('*according to one or more commands output from the control module*') whether to output test data or normal data just as the Control ASIC sends command signals during normal operations." *Id.* at 58 (citing Ex. 1003 ¶ 257; Ex. 1005, Figs. 2–3, ¶¶ 30–31). Petitioner provides annotated Figure 2, reproduced below, depicting that path.



Id. at 59 (citing Ex. 1003 ¶ 257). Petitioner's annotated Figure 2, above, shows Figure 2 on the right, and enlarged Switch ASIC 208 on the left, with "Pattern Generator" added inside Switch ASIC 208, and an orange arrow from "Pattern Generator" to Port A of Bank 0.

Petitioner asserts that "in the Combined System data travels over two different data paths in the two different modes. Because each path merges into the same port on the Switch ASIC, only one path can be used at a time, using for instance a MUX/DEMUX as was well-known, otherwise there could be data collisions." *Id.* (citing Ex. 1003 ¶ 258). In the Reply brief, Petitioner further asserts that "the proposed combination would use a MUX to isolate the *address/control* signals . . . just like the data signals." Reply 10 (citing Ex. 1061 ¶¶ 701, 741, 754).

Petitioner asserts for limitation 1[g][iii] that the modified Control ASIC generates address/control signals with memory sequencer 304 that are output to the ports of the memory devices 240, and command signals with

BIST engine 310, to Switch ASICs, which generate "*second data signals*" via pattern generator 314. *Id.* at 61 (citing Ex. 1006, Fig. 3, 9:51–60, 9:66–10:2, 10:24–28, cl. 7; Ex. 1003 ¶¶ 279–280. Therefore, according to Petitioner, "the Control ASIC would gain the functionality of generating its own address/command signals when in a self-test mode, and the Switch ASICs would gain the functionality of generating their own data signals when in self-test mode." Reply 24; *see also* Pet. 58–61.

(1) Petitioner's Rationale for the Combination

Petitioner asserts that:

> [A] Skilled Artisan would have considered the Combined System to be an arrangement of old elements each performing its known functions (Ellsberry's module acting as computer memory and Jeddeloh[]'s self-test functionality performing self-test on that module) and yielding what one would expect from the arrangement (a memory module with self-test). Ellsberry and Jeddeloh[] each employ known signaling and testing techniques found in many prior art systems. EX1006, 9:46-51. Combining them would therefore have been well within a Skilled Artisan's abilities, would not have resulted in any unpredictable results and could have been readily accomplished without undue experimentation and with a reasonable expectation of success. EX1003, ¶¶146-147.

Pet. 32 (emphasis omitted). Petitioner additionally provides purported rationale why a person of ordinary skill in the art would be motivated to (1) add the testing mode to Ellsberry and (2) divide the self-test functionality of Jeddeloh's Figure 3 between Ellsberry's Control ASIC and distributed Switch ASICs, set forth below. *Id.* at 32–37.

(a) Motivation to Add Testing to Ellsberry

Petitioner contends there are several reasons why a person of ordinary skill in the art would be motivated to add a testing mode to Ellsberry. *Id.* at 32–34; Ex. 1003 ¶¶ 149–53.

First, Petitioner contends, quoting U.S. Patent No. 7,181,659, a non-asserted reference, that "[a]s chips become faster in frequency, there is a greater need for hardware to include self-test logic." *Id.* at 32 (citing Ex. 1018, 1:14–18). Moreover, Petitioner contends that Ellsberry discloses that its modules are JEDEC compliant and JEDEC standards at the time required self-testing. *Id.* (citing Ex. 1005 ¶ 50, claims 10, 19; Ex. 1016, 1–2, 25–28, 55–66; Ex. 1017, 2–11).

Second, Petitioner contends that because Ellsberry's Control ASIC configures the memory devices on the module "rather than [being] directly programmed by the host system," a person of ordinary skill would have been motivated to have a built-in testing capability in the Control ASIC itself. *Id.* at 33 (citing Ex. 1005 ¶ 44; Ex. 1003 ¶ 150).

Third, Petitioner contends that Jeddeloh emphasizes the need for testing circuitry in memory modules because of the increasing significance of signal timing. *Id.* (citing Ex. 1006, 2:41–51, 3:47–52).

Fourth, Petitioner contends that because Ellsberry describes that its Control ASIC configures the memory devices, one of ordinary skill would be motivated to add testing and, further, because Ellsberry has a "Mode" pin, to operate in other modes, a skilled artisan would have been motivated to

provide functionality to switch between additional modes. *Id.* at 33–34 (citing Ex. 1005 ¶ 33; Ex. 1003 ¶ 152).

Fifth, Petitioner also contends a person of ordinary skill in the art "would have been motivated to add testing in a mode separate from normal operating mode because the purpose of testing was to confirm the module would operate appropriately in normal mode." *Id.* at 34 (citing Ex. 1006, 2:43–50, 3:47–53; Ex. 1016, 1–2, 25–28 55–66; Ex. 1017, 2–11. Ex. 1003 ¶ 153).

Sixth, Petitioner would add testing mode because "normal operation where the host sends read/write commands to the Control ASIC would interfere with such testing." *Id.*

(b) Motivation to Distribute Jeddeloh's Components into Ellsberry

Petitioner contends there are several reasons why a person of ordinary skill in the art would be motivated to divide the self-test functionality of Jeddeloh's Figure 3 between Ellsberry's Control ASIC and Switch ASICs. Pet. 34–37.

First, Petitioner contends that such distribution is consistent with Ellsberry's architecture, and how Ellsberry handles address/control signal mapping in the Control ASICs and data signal routing in the Switch ASICs. Pet. 35. According to Petitioner, a person of ordinary skill in the art would have been motivated to divide the added functionality from Jeddeloh in a similar manner in order to simplify the design and minimize changes to Ellsberry. *Id.* (citing Ex. 1003 ¶¶ 155–156).

Second, Petitioner contends such a distribution of self-test functionality is consistent with how each of Ellsberry's Switch ASICs

already included logic elements and connections for implementing data transactions in 8-bit portions. *Id.* at 35–36. According to Petitioner, a person of ordinary skill in the art "would have understood that additional logic functionality related to communicating data to and from data devices, such as that of [Jeddeloh], could be readily and efficiently included in the Switch ASICs, and configured to receive command signals from the added [Jeddeloh] testing-related functionality in the modified Control ASIC and report results thereto, without undue experimentation." *Id.* at 36 (citing Ex. 1003 ¶ 158).

Third, Petitioner contends that a person of ordinary skill in the art would have been motivated to make such a design because other references teach placement of such self-test functionality in distributed data buffers similar to Ellsberry's Switch ASICs. *Id.* (citing Ex. 1019[8] ¶¶ 77, 97, Figs. 5, 18; Ex. 1020,[9] 15:57–65, 18:63–19:23, 35:10–37:1, Figs. 5, 18, 36; Ex. 1007 ¶¶ 49–50, 53, 55–57, Figs. 1, 6–7; Ex. 1025, 30).

Fourth, Petitioner contends that an additional reference, Lepejian,[10] teaches that, in order to reduce busing area, pattern generators should be distributed to each of the Switch ASICs. *Id.* (citing Ex. 1021, 3:45–53; Ex. 1003 ¶ 162).

Fifth, Petitioner contends that a person of ordinary skill in the art "would have been motivated to place self-test pattern generator functionality, such as [Jeddeloh's], in [Ellsberry's] Switch ASICs in order to place it close to its associated memory devices, thereby simplifying the

[8] Tsern, US Patent Pub. 2007/0070669 A1 (published Mar. 29, 2007).
[9] Shaeffer et al., US 7,562,271 B2 (issued July 14, 2009).
[10] Lepejian et al., US 6,011,748 (issued Jan. 4, 2000).

wiring plan on the circuit board, reducing capacitance/propagation delay of the data lines, and reducing the inductance/crosstalk of the data lines," *Id.* at 36–37 (citing Ex. 1002, 6–7; Ex. 1023, 2:27–3:6, Ex. 1024, 23–25, 207; Ex. 1009, 52, 54; Ex. 1003 ¶ 163) (internal citations omitted).

Finally, quoting another reference, Zimmerman,[11] Petitioner argues it was known that "functionality shown embodied in a single integrated circuit or functional block may be implemented using multiple cooperating circuits or blocks, or vice versa." *Id.* at 37 (citing Ex. 1026, 7:43–46; Ex. 1027, 7:7–14; Ex. 1003 ¶ 165).

b) Patent Owner's Arguments

Patent Owner contends that Petitioner has failed to show that a person of ordinary skill in the art would be motivated to combine Ellsberry and Jeddeloh in the manner required to achieve the claims of the '523 patent. PO Resp. 35–70. Specifically, Patent Owner argues that Petitioner "provides no motivation to combine elements of Ellsberry and its *distributed* architecture with and Jeddeloh and its *centralized* architecture in the way the '523 [p]atent claims require," and thus, "Petitioner's arguments are based only on hindsight." *Id.* at 37 (citing Ex. 2004 ¶ 122); *see also id.* at 39–43. Patent Owner contends that Petitioner's expert, Dr. Subramanian, admitted that he was "unaware of any prior memory module with a similar architecture to Ellsberry *ever* having incorporated self-test functionality as the '523 [p]atent does, despite its general architecture being known in the art *for years*." *Id.* at 36 (citing Ex. 2005, 47:20–48:8, 48:14–17, 52:1–7, 148:14–19; Ex. 2004 ¶¶ 118, 120–121); *see also id.* at 54–55.

[11] Zimmerman, US 7,177,211 B2 (issued Feb. 13, 2007).

Patent Owner also argues that Petitioner's combination "goes directly against the explicit teachings of Jeddeloh" because it distributes "pieces of Jeddeloh's centralized self-test logic differently . . . across disparate circuits and placing them in direct communication with the memory devices" and without Jeddeloh's memory interface components. *Id.* at 46. Patent Owner further argues that Petitioner's combination requires a MUX/DEMUX circuit in each of Ellsberry's switch ASICs, which is not consistent with the teachings in Ellsberry or Jeddeloh, and further would introduce memory timing issues that Jeddeloh tries to avoid. *Id.* at 47–48.

In addition, Patent Owner argues that Petitioner's arguments regarding motivation to add testing to Ellsberry are deficient for various reasons. *Id.* at 49–53. Patent Owner also argues that Petitioner's contentions regarding motivation to distribute pieces of Jeddeloh's self-test module to separate parts of Ellsberry are likewise deficient. *Id.* at 54–59.

Patent Owner further argues that Petitioner has not established that a person of ordinary skill in the art would have had a reasonable expectation of success in achieving the claimed invention from the combination because, according to Patent Owner, the combined system would not result in a functional device and would have required multiple further modifications and engineering. *Id.* at 59–60. Patent Owner also argues that "Petitioner has identified a relatively low level of experience as being ordinary in the field," and the challenges encountered by the combination "would have been beyond such a [person of ordinary skill in the art's] ability to reasonably resolve them." *Id.* at 60 (citing Ex. 2004 ¶¶ 83–84); *see also id.* at 61–70.

c) Analysis

For the reasons set forth below, we agree with Patent Owner that Petitioner has not explained persuasively why one of ordinary skill in the art, absent hindsight and use of the '523 patent as a roadmap, would have been motivated to combine Ellsberry and Jeddeloh in the manner proposed. *See In re Fritch*, 972 F.2d 1260, 1266 (Fed. Cir. 1992) (citing *In re Gorman*, 933 F.2d 982, 987 (Fed. Cir. 1991)) ("It is impermissible to use the claimed invention as an instruction manual or 'template' to piece together the teachings of the prior art so that the claimed invention is rendered obvious."). Specifically, we determine that Petitioner has not provided sufficient rationale establishing why a person of ordinary skill in the art would have been motivated to divide the self-test functionality of Jeddeloh's Figure 3 between the Control ASIC and Switch ASICs of Ellsberry and with a reasonable expectation of success in doing so.[12] *See KSR*, 550 U.S. at 418 (establishing that an invention would have been obvious requires "a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements *in the way* the claimed new invention does") (emphasis added).

Petitioner's proposed combination requires (1) adding a test mode with self-test functionality to Ellsberry; (2) modifying Jeddeloh's self-test

[12] Because we determine that Petitioner has not provided sufficient reasoning why a person of ordinary skill in the art would have been motivated to divide the self-test functionality of Jeddeloh's Figure 3 between the Control ASIC and Switch ASICs of Ellsberry with a reasonable expectation of success, we need not reach whether Petitioner has sufficiently established motivation to add testing to Ellsberry with a reasonable expectation of success.

module, i.e., dividing the self-test functionality and related circuitry shown in Jeddeloh's Figure 3; (3) incorporating the divided self-test functionality and related circuitry in Ellsberry's Control ASIC and Switch ASICs; and (4) adding MUX/DEMUX to each of Ellsberry's Switch ASICs, and further using a MUX to isolate the address/control signals. Pet. 25–37; Reply 10. As a result of incorporating the divided self-test functionality and related circuitry in Ellsberry's Control ASIC and Switch ASICs, Petitioner further asserts that the Control ASIC would generate its own address/control/command signals when in a self-test mode, and the Switch ASICs would generate their own data signals when in self-test mode. Reply 24; Pet. 56–61. That is, according to Petitioner, while in self-test mode, the added memory sequencer functionality in the Control ASIC would generate address and control signals, the added BIST functionality in the Control ASIC would generate command signals, and the added pattern generator/compare circuit functionality in the Switch ASIC would generate data signals. Pet. 56–61. Petitioner's changes therefore require multiple levels of modifications in order to purportedly teach the claimed second mode (limitation 1[e]), and the functionality of the claimed second mode (limitations 1[c], 1[g][1], 1[g][ii], and 1[g][iii]).

A number of facts are undisputed. There is no dispute that Ellsberry's distributed architecture was well known. PO Resp. 36; Ex. 2004 ¶¶ 56–57, 127; Reply 18. There is no dispute that Ellsberry does not teach testing. PO Resp. 36; Ex. 2004 ¶ 63; Pet. 32 (describing asserted motivations to add a testing mode to Ellsberry); Ex. 2005, 64:23–25. There is no dispute that Jeddeloh employs a centralized architecture that is different from Ellsberry's distributed architecture. PO Resp. 39; Reply 14. There is no dispute that

neither reference teaches distributing self-test functionality as in the claimed invention. PO Resp. 36, 38; Pet. 34 (describing dividing the self-test functionality of Jeddeloh); Reply 36 ("the Petition is not asserting anticipation, so it is irrelevant whether any single reference discloses the combination of elements at issue"). Moreover, both Dr. Subramanian and Dr. Brogioli testified that they were not aware of any memory module with a similar architecture to Ellsberry ever having incorporated self-test functionality as configured in the claimed invention, despite Ellsberry's distributed architecture being well known in the art. Ex. 2004 ¶¶ 18, 126–127, 143; Ex. 2005, 47:20–48:8, 48:14–17, 52:1–7, 148:14–19.

Although Petitioner contends that the combination of Ellsberry and Jeddeloh is merely an arrangement of old elements, each performing the same function (Pet. 31–32), Petitioner has not identified persuasive evidence that supports these contentions. Petitioner identifies Ellsberry's memory module and Jeddeloh's self-test functionality, but Petitioner has not identified any "old element" where self-test functionality is divided in the manner in which Petitioner proposes to divide Jeddeloh's functionality. In other words, this is not a situation where each element is purportedly taught, in some manner, by one of the references, and the elements are merely rearranged and combined. *KSR*, 550 U.S. at 418 (in an obviousness analysis, one must "determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue."); *Sundance, Inc. v. DeMonte Fabricating Ltd.*, 550 F.3d 1356, 1366–1367 (Fed. Cir. 2008) (a combination of prior art is "more likely to be obvious where it 'simply arranges old elements with each performing the same function it had been known to perform' and yields no more than one would expect from

such an arrangement."). Here, the proposed combination involves modifying *both* references in order to reach the claimed invention, and in particular, to purportedly teach the specific requirements of limitations 1[c], 1[e], 1[g][i], 1[g][ii], and 1[g][iii].

Petitioner's first, second, fifth, and sixth reasons to distribute Jeddeloh's functionality into Ellsberry all rely on Ellsberry's distributed architecture as a basis for providing motivation to divide the added functionality and circuitry from Jeddeloh, i.e., in manner consistent with Ellsberry's architecture. We first address these rationales. Both parties identify the different architectures of Ellsberry and Jeddeloh as a basis for their arguments, but Petitioner contends that these differences provide motivation to combine the references, whereas Patent Owner contends the opposite – that these differences do not support a motivation to combine.[13]

Petitioner relies on Ellsberry's distributed architecture as the rationale to divide Jeddeloh's self-test module circuitry, but Ellsberry itself does not teach a testing mode. *See* Reply 36 (Ellsberry's "distributed architecture ***itself*** provides a motivation for a [person of ordinary skill in the art] to distribute the BIST functionality from" Jeddeloh). Although the motivation

[13] In the Reply, Petitioner refers to Ellsberry as an LRDIMM architecture and Jeddeloh as an FBDIMM architecture. *See generally* Reply. Patent Owner contends this is a new argument, and that neither Ellsberry nor Jeddeloh mention LRDIMM or FBDIMM, and that the LRDIMM and FBDIMM module types postdate both references. Sur-reply 10. We agree that neither Ellsberry nor Jeddeloh mention LRDIMM or FBDIMM. *See id*. Regardless of how the architectures of Ellsberry and Jeddeloh are labelled, we agree with Patent Owner that the question is whether Ellsberry would be combined with Jeddeloh, not whether LRDIMM would be combined with FBDIMM. *Id.* at 11. We, therefore, focus our analysis on the disclosures in Ellsberry and Jeddeloh.

to combine may come from the references themselves, *WMS Gaming, Inc. v. International Game Tech.,* 184 F.3d 1339, 1355 (Fed. Cir. 1999), there still must be evidence that "the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed." *In re Rouffet,* 149 F.3d 1350, 1357 (Fed. Cir. 1998); *see also In re Werner Kotzab,* 217 F.3d 1365, 1371, (Fed. Cir. 2000) ("[A] rejection cannot be predicated on the mere identification ... of individual components of claimed limitations. Rather, particular findings must be made as to the reason the skilled artisan, with no knowledge of the claimed invention, would have selected these components for combination in the manner claimed."). To that end, we agree with Patent Owner that Petitioner's proposed rationale for the combination appears circular, and based on hindsight. *See* Sur-reply 17; *Monarch Knitting Mach. Corp. v. Sulzer Morat Gmbh,* 139 F.3d 877, 880 (Fed. Cir. 1998) ("[d]efining the problem in terms of its solution reveals improper hindsight in the selection of the prior art relevant to obviousness").

That is, we are not persuaded that simply because Ellsberry has a distributed architecture, that, with no knowledge of the claimed invention, one of ordinary skill in the art would select Jeddeloh's self-test module, divide that self-test module functionality, implement it into Ellsberry's Control ASIC and Switch ASICs, and then make the extensive further modifications required to Ellsberry that are necessary to achieve the claimed invention. As the various modifications required to teach the claims (particularly, limitations 1[c], 1[e], 1[g][i], 1[g][ii], and 1[g][ii]), become more complex and untethered to the design of Ellsberry and Jeddeloh, the

influence of impermissible hindsight bias emerges, as further discussed below.

Petitioner's contentions that the proposed combination is "straightforward because it would not require any new data or control paths and thus would not create any new timing issues" because it would take advantage of the existing data and control paths of Ellsberry's module, are not persuasive because they oversimplify the changes required, as discussed further below. *See* Reply 14–15, 19–20 ("implementing self-test functionality in either [a centralized or distributed] architecture would have been straightforward, because a [person of ordinary skill in the art] could simply use the ***existing*** buffers for data and address/command on the memory module to add self-test functionality without any ***new*** data or control paths"); Ex. 1061 ¶¶ 664–666. For similar reasons, we do not find persuasive Petitioner's arguments that "the proposed combination is much more straightforward than alternative implementations proposed by the ['523 patent] (but not explained in any detail) that would require ***new*** structures and/or signal paths." Reply 15 (citing Ex. 1061 ¶ 688). Nor are we persuaded that the necessary modifications to both references would "simplify the design and minimize the changes to Ellsberry, and thereby likely avoid design problems and produce a more reliable system," as Dr. Subramanian testifies. *See* Ex. 1003 ¶¶ 155, 158 (emphasis omitted).

Modifying Jeddeloh's self-test module to divide the functionality and circuitry creates the need to continue modifying the various components of Ellsberry in order to achieve the claimed invention. For example, the modification requires that Ellsberry's Control ASIC must generate address/control/command signals in a new self-test mode (limitations 1[e],

1[g][i], 1[g][ii], 1[g][iii]), and similarly, Ellsberry's Switch ASICs must generate data signals in a new self-test mode (limitations 1[c], 1[e], 1[g][ii], 1[g][iii]. Reply 24; Pet. 56–61. Furthermore, Ellsberry's Switch ASICs require a MUX/DEMUX in order to handle the different data paths in normal and new self-test mode (limitation 1[e], 1[g][ii]). *See* Pet. 59. Thus, in order to meet each of these claim limitations that require a new testing mode to be added to Ellsberry, Petitioner simply continues to modify the references in a way that conveniently results in the same configuration as the claimed invention. That is, the claims require that the testing data and address/control logic is separated between the data module and the control module. Although the wiring and signaling rerouting itself may not be complex, the combination of functionality and circuitry that requires modification to achieve the correct timing and synchronization results from the knowledge of the particular claim limitations, not any motivation to combine asserted by Petitioner. *See* Ex. 2004 ¶¶ 82–83.

Petitioner cites to supporting testimony from Dr. Subramanian on the combination, but Dr. Subramanian's testimony is unavailing because it essentially repeats what is stated in the Petition, and states that Ellsberry and Jeddeloh "employ known signaling and testing techniques found in many prior art systems," and combining Ellsberry and Jeddeloh "would therefore have been well within a Skilled Artisans's abilities, would not have resulted in any unpredictable results and could have been readily accomplished without undue experimentation and with a reasonable expectation of success." Pet. 32 (citing Ex. 1003 ¶¶ 146–147). We find this testimony to be conclusory, at a minimum, particularly in light of the relatively low level

of skill in the art advanced by Petitioner. Further, as discussed below, Dr. Subramanian's testimony is misguided.

We find more persuasive Patent Owner's contentions that "[p]ortions of Jeddeloh's self-test module cannot be disassembled and distributed across Ellsberry's memory module as proposed by Petitioner without creating new pathways or changing how existing components work, which creates timing issues and issues synchronizing the various signals sent to and received from the memory devices." PO Resp. 62–63 (citing Ex. 2004 ¶ 83). For example, Dr. Brogioli explains that "two new circuits have been created using components disclosed in Jeddeloh and deployed to a distributed, and markedly different architecture than Jeddeloh. Not only are new pathways required within Ellsberry's architecture that are not contemplated by Jeddeloh, but these pathways in some instances require being bidirectional." Ex. 2004 ¶ 83. We find this testimony credible, given the nature and extent of the modifications proposed by Petitioner.

This is exemplified in Petitioner's modifications to Ellsberry's Control ASIC in order to teach limitations 1[e], 1[g][i], 1[gii], and 1[g[iii]. Dr. Subramanian testifies that Jeddeloh's "self-test functionality would be implemented in Ellsberry such that the address and command signals are generated in Ellsberry's control unit instead of receiving those address and command signals from the system bus." Ex. 1061 ¶ 665; *see also id.* ¶ 678 (modification involves "adding an address/command generator to Ellsberry's Control ASIC").

Patent Owner argues that the Control ASIC in Petitioner's combined system "would be unable to properly access the memory devices in a 'second' mode," i.e., a testing mode. PO Resp. 66 (citing Ex. 2004 ¶ 97).

Patent Owner argues that any address and control signals originating from the modified Control ASIC's Control Block[14] during test mode will bypass register 302, a necessary component of the Control ASIC that helps control the timing of the signals received from the system. PO Resp. 66; Ex. 2004 ¶¶ 96–97. Dr. Brogioli testifies that "register 302 buffers address and command information received from the DIMM interface," so if testing mode is used, "signals would not pass through register 302 and hence the timing would change, and thus the functioning." Ex. 2004 ¶ 96 (citing Ex. 1005 ¶ 39). According to Dr. Brogioli, "without register 302, the carefully synchronized data and address/control signals would no longer be synchronized." *Id.*

For convenience, Petitioner's modified Fig. 3 of Ellsberry is reproduced below:

[14] Patent Owner contends that without Jeddeloh's memory controller, which is not part of the proposed combination, the proposed combination is unable to generate address signals during test mode in accordance with limitation [1.g.i]. PO Resp. 28–30. Petitioner contends that Jeddeloh's memory sequencer 304 generates address signals for testing because it "receives read and write commands" and then "generates properly timed signals for *controlling* the operation of the memory device." Reply 5 (citing Ex. 1006, 9:58–59); *see also id.* at 3–6. Petitioner contends that Jeddeloh omitted address and control signal lines from Figure 3 "to avoid unnecessarily obscuring the present invention." *Id.* at 6 (citing Ex. 1006, 9:51–54, 9:61–64; Ex. 1061 ¶ 736). We find that the cited disclosure from Jeddeloh better supports Petitioner's position.

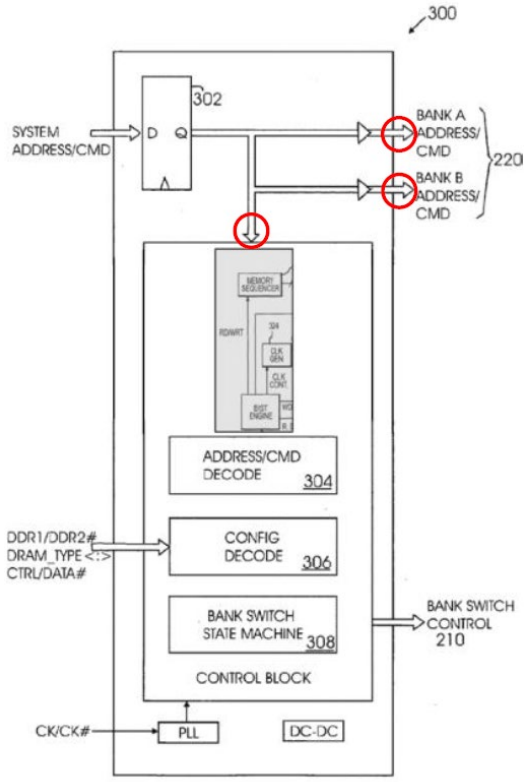


Fig. 3

Reply 40. Petitioner's modified Figure 3, depicted above, shows Ellsberry's Figure 3 with the proposed added functionality from Jeddeloh (BIST engine 310, clock generator 324, and memory sequencer 304) in gray in the Control Block. A directional right arrow is depicted on the top left, labelled "system address/cmd" going into register 302, with two single directional right arrows coming out of register 302 and to the right into bank A and bank B address cmd 220 and a single directional down arrow into the Control Block that are labelled with red circles. In the Control Block are four blocks: the added functionality from Jeddeloh in gray, address/cmd decode 304, config decode 306, and bank switch state machine 308. There is a directional right arrow coming out of the Control Block to bank switch control 210.

Patent Owner contends "the single-directional arrow from register 302

to the control block and to bus 220 faces the wrong direction" and "the link would have to be bidirectional before the [combined system] would be able to generate any useful test signals." PO Resp. 67 (citing Ex. 2004 ¶¶ 97–98). Dr. Brogioli testifies that a person of ordinary skill in the art "would need to account for the change in signal timing resulting from the test address/control signals skipped register 302 in order to synchronize the data and address/control signals." Ex. 2004 ¶ 98. According to Dr. Brogioli, a person of ordinary skill in the art "would then be met with the problem that if you make the unidirectional arrows shown above bidirectional, that would introduce issues over who is controlling the line (the system or control block), and how." *Id.* Dr. Brogioli further testifies that a person of ordinary skill in the art would "not be familiar with how to manage a bidirectional interconnect in this context, and how to effectively control the end points that are intended to transmit data over the bidirectional interconnect, in a shared manner, at the speeds that Ellsberry contemplates." *Id*.

Petitioner responds that Patent Owner's arguments "misinterpret the normal operation" of Ellsberry. Reply 39 (citing Ex. 1061 ¶¶ 724–731). According to Petitioner, "the connection to the 'Control Block' . . . is ***already*** bidirectional, such that signals output on bus 220 come from the 'Control Block' in the Control ASIC, not directly from register 302, which is how the Control ASIC can output different signals than it receives." *Id.* at 39–40 (citing Ex. 1061 ¶¶ 726, 729). Petitioner contends that "in order for the Control Block to output signals on bus 220 in normal mode, that connection must already be bidirectional," and "[t]he same is true in the proposed combination," as shown in Petitioner's annotated Figure 3, above.

Id. at 40 (citing Ex. 1061 ¶ 729).

Dr. Subramanian testifies that "[i]n normal mode, the role of register 302 is to provide address and command signals from the system bus that are *input* to the Control Block, which decodes that information and, in response, outputs the signals to control the memory bank switches (using 210) and memory devices (using 220)." Ex. 1061 ¶ 726 (citing Ex. 1005, Figs. 3, 8B, 9, ¶¶ 12, 32, 44). Dr. Subramanian, therefore, contends that "[t]he signals from the Control ASIC come from the 'Control Block,' not directly from register 302, and thus register 302 does not affect the timing of the *output* from the 'Control Block,' since the timing is set by the Control Block, not by the register 302." *Id.* Dr. Subramanian testifies that a person of ordinary skill in the art would have understood "that the arrows in Figure 3 are not indicating universal unidirectional communication from the register 302 into the Control Block and to bus 220 as Dr. Brogioli argues, but also include signals coming out from the Control Block going to bus 220, meaning the connection to the Control Block is already bidirectional." *Id.* at ¶ 729. Dr. Subramanian further testifies that a person of ordinary skill in the art would have understood "how to route signals to implement self-test functionality inside an ASIC or similar integrated circuit, as evidenced by the prior art." Ex. 1061 ¶ 730 (citing Ex. 1006, Figs. 1–3; Ex. 1016 at 3, 25–28; Ex. 1058 at 3, 26–29).

We find that the disclosure in Ellsberry better supports Patent Owner's arguments. *See* Sur-reply 22–26. Central to the dispute is whether Ellsberry's Figure 3 discloses bidirectional communication, i.e., whether there are already signals coming *from* the Control Block *to* bus 220. Patent Owner and Dr. Brogioli rely on paragraph 39 of Ellsberry, which describes

Figure 3. Sur-reply 22–26; Ex. 2004 ¶ 96. Paragraph 39 of Ellsberry states:

> The command processing system 300 controls physical bank selection and bank switching direction. *Memory addresses and command information are received from the DIMM interface 202, buffered in a register 302 and sent to all memory banks (e.g., Bank 0, Bank 1, Bank 2 and Bank 3) over address bus 220. The memory address and command information is also decoded 304 and memory configuration information 306 (e.g., DRAM type. etc.) is determined.* The memory configuration information may be determined from preset information. A bank switch state machine 308 then determines which memory bank should be activated or accessed. In one embodiment of the invention, this state machine 308 is a logical translation table that maps a primary space address to a secondary space address based on the memory configuration present. For example, the state machine 308 may be the address mapping table illustrated in FIGS. 7A-F, which was previously described. *The state machine 308 sends control information to the memory bank switches 206 & 208 via the control bus 210 to indicate which memory banks should be activated/deactivated or accessed.*

Ex. 1005 ¶ 39 (emphasis added). In other words, Ellsberry teaches that memory address and command information is received from DIMM interface 202, buffered in register 302, and sent to memory banks over address bus 220. It further teaches that the memory address and command information is also decoded (i.e., address/cmd decode block 304 in the control block) to determine memory configuration information (i.e., config decode block 306), and that state machine 308 determines which memory bank switch should be activated or accessed and sends control information to the memory bank switches 206 and 208 over control bus 210. This disclosure in Ellsberry does not disclose that any information is sent *from* the Control Block and *to* bus 220; rather, it only indicates that information is

provided *to* the Control Block and then *to* bus 210. The citations from Ellsberry that Dr. Subramanian relies upon do not state otherwise. For example, paragraph 32 of Ellsberry states that "[a]lthough address information may be sent to all memory banks over address bus 220, the memory bank switch 206 and/or control unit 204 determine which memory devices or banks are accessed." Petitioner does not persuasively rebut Patent Owner's arguments or Dr. Brogioli's testimony as to the disclosure in paragraph 39. We, accordingly, afford more weight to Dr. Brogioli's testimony on this point, as well as his testimony describing the extent of the modifications required of the proposed combination. *See, e.g.*, Ex. 2004 ¶¶ 83, 98.

As discussed above, Petitioner contends that the proposed combination involves using the same data control mechanisms and pathways (e.g., Reply 24–27, 37), and Dr. Subramanian testifies that adding the self-test functionality to Ellsberry "does not require any new timing or routing at the module level." Ex. 1061 ¶¶ 678, 682; *see* Reply 25. However, Dr. Subramanian admits that the proposed combination requires that Ellsberry's Switch ASICs and Control ASIC must be redesigned to add the relevant functionality from Jeddeloh. *See* Ex. 2016, 153:18–154:17, 158:13–23, 160:17–162:7. This is consistent with Dr. Brogioli's testimony that "two new circuits have been created using components disclosed in Jeddeloh and deployed to a distributed, markedly different architecture than Jeddeloh." Ex. 2004 ¶ 83.

In addition to the modifications to the Control ASIC, Dr. Subramanian testifies that modifications are required to the Switch ASIC, "such that the write data signals are generated in Ellsberry's memory bank switches instead

of receiving write data from the system bus, and the memory bank switches then handle the data transfers the same way, and with the same timing, as before." Ex. 1061 ¶ 665 (emphasis omitted); *see id.* ¶ 678 ("a data generator as taught by Jeddeloh is added to each memory bank switch in Ellsberry to provide data signals in a self-test mode instead of providing the data signals from the system memory bus when in a normal mode"). Dr. Subramanian further testifies that Ellsberry had "already solved the timing and synchronization issues between its control unit and the distributed memory bank switches by following the timing requirements of the relevant JEDEC standards." Ex. 1061 ¶ 684 (citing Ex. 1005 ¶¶ 46, 50). As discussed, the modification to Ellsberry also requires adding a MUX to isolate the data signals in the Switch ASIC and the address/control signals in the Control ASIC. Pet. 59, Reply 10. According to Dr. Subramanian, "the prior art confirms that a [person of ordinary skill in the art] would have known how to use a multiplexer or demultiplexer . . . without any timing and signal issues." Ex. 1061 ¶ 701; *see id.* ¶¶ 741, 754, Ex. 1003 ¶ 258.

In our view, Petitioner minimizes the extent of the redesign required to make the proposed combination, and due to that, we find Dr. Brogioli's testimony to be more credible. *See, e.g.*, Ex. 2004 ¶¶ 81–86. For example, we find persuasive Dr. Brogioli's testimony that "[w]hen attempting to adapt circuitry and functions meant for one type of architecture for use in a different architecture, a [person of ordinary skill in the art] would have understood that technical problems would arise, such as issues coordinating signals between functional units that were intended to remain united, and issues managing shared buses or data lines, for example." Ex. 2004 ¶ 82. We also find credible Dr. Brogioli's testimony that a person of ordinary skill

in the art "would have been met with substantial challenges coordinating data and address signaling circuitry of Jeddeloh once you split up and distributed it into Ellsberry's specific architecture." *Id.* at ¶ 83. Dr. Brogioli testifies "[n]ot only are new pathways required within Ellsberry's architecture that are not contemplated by Jeddeloh, but these pathways in some instances require being bidirectional," as was shown above in connection with the modifications to the Control ASIC. *Id.* We afford weight to Dr. Brogioli's testimony that "Jeddeloh's self-test module cannot be disassembled and distributed across Ellsberry's memory module as proposed by Petitioner without creating new pathways or changing how existing components work" in view of the extent of the modifications required. *Id.*

Dr. Subramanian's testimony that Ellsberry "already solved the timing and synchronization issues between its control unit and the distributed memory bank switches by following the timing requirements of the relevant JEDEC standards," merely supports that Ellsberry, standing alone and without the proposed modifications, is JEDEC compatible, not that Ellsberry "solved the timing and synchronization issues between its control unit and the distributed memory bank switches" in the proposed combination with the proposed modifications to Ellsberry, including the addition of self-test functionality from Jeddeloh. *See* Ex. 1061 ¶ 684.

The record supports that the proposed modifications were informed by the requirements of the claims. The fact that a person of ordinary skill in the art "could" make these changes does not inform us that a person of ordinary skill in the art "would" make these changes. *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015) ("obviousness concerns whether a

skilled artisan not only *could have made* but *would have been motivated to make* the combinations or modifications of prior art to arrive at the claimed invention"); *see ActiveVideo Networks, Inc. v. Verizon Commc'ns, Inc.,* 694 F.3d 1312, 1327 (Fed. Cir. 2012) ("[T]he expert's testimony on obviousness was essentially a conclusory statement that a person of ordinary skill in the art would have known, based on the 'modular' nature of the claimed components, how to combine any of a number of references to achieve the claimed inventions. This is not sufficient and is fraught with hindsight bias."). As discussed by Patent Owner, Dr. Subramanian conceded that there were multiple ways a person of ordinary skill in the art could add self-testing to Ellsberry. *See* PO Resp. 57 (citing Ex. 2004 ¶¶ 46, 47, 128, 129, 146; Ex. 2005, 121–125). For example, a person of ordinary skill in the art could have incorporated all of Jeddeloh's self-test logic into Ellsberry's Control ASIC or duplicated Jeddeloh's self-test logic into Ellsberry's Switch ASICs. *See* Ex. 2004 ¶ 129; Ex. 2005, 121–125, 184–185. Dr. Brogioli credibly testifies that these alternative designs would have been more similar to what was seen in the prior art. Ex. 2004 ¶¶ 46, 47, 128, 129, 146. Accordingly, the record supports that Petitioner's specific modifications were driven by hindsight view of the roadmap provided by the claim limitations, e.g., the testing data and address/control logic is separated between the data module and the control module (limitations 1[e], 1[g][i], 1[g][ii], 1[g][ii]).

Petitioner also asserts that a person of ordinary skill in the art would have understood that Jeddeloh has a central hub 140 which functions like an AMB in an FBDIMM to buffer both data and address/command signals for the memory devices. Reply 20. Petitioner further asserts that Jeddeloh

teaches implementing the BIST self-test functionality in the central hub, "i.e., an AMB that buffers data and address/command signals." *Id.* at 21 (citing Ex. 1061 ¶ 672; Ex. 1006, 5:47–49, 8:26–29, 9:44–60). Petitioner asserts that the '523 patent "admits that self-test functionality could be implemented in an AMB." *Id.* (citing Ex. 1001, 4:41–44). Dr. Subramanian testifies that the '523 patent "express[es] concerns about concentration of self-test circuitry in a combined address/control and data buffer, as [Jeddeloh] does, and these known concerns with prior art implementations would have further motivated" a person of ordinary skill in the art to divide Jeddeloh's circuitry functionality between Ellsberry's Control ASIC and Switch ASICs to avoid "these very issues." Ex. 1003 ¶ 156 (citing Ex. 1001, 4:41–56); *see* Reply 21.

We agree with Patent Owner (Sur-reply 12–13) that whether self-test can be implemented in an AMB or a centralized architecture such as Jeddeloh does not inform whether the combination of Ellsberry and Jeddeloh is obvious. *See Innogenetics N.V. v. Abbott Laboratories*, 512 F.3d 1363, 1373 (Fed. Cir. 2008) ("knowledge of a problem and motivation to solve it are entirely different from motivation to combine particular references to reach the particular claimed method"). Instead, motivation must be demonstrated to combine the particular references, i.e., Ellsberry and Jeddeloh. *See id.* at 1373–1374; *see also W.L. Gore & Assoc., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1553 (Fed. Cir. 1983) ("To imbue one of ordinary skill in the art with knowledge of the invention in suit, when no prior art reference or references of record convey or suggest that knowledge,

is to fall victim to the insidious effect of a hindsight syndrome wherein that which only the inventor taught is used against its teacher.")

For the third rationale for distributing Jeddeloh's functionality into Ellsberry, Petitioner relies upon several references—Tsern, Schaffer, and Averbuj—to support its contentions that a person of ordinary skill in the art "would have been motivated to make such a design because other references teach [a person of ordinary skill in the art] to place such self-test functionality in distributed data buffers similar to [Ellsberry's] Switch ASICs." Pet. 36 (citing Ex. 1019 ¶¶ 77, 97, Figs. 5, 18; Ex. 1020, 15:57–65, 18:63–19:23, 35:10–37:1, Figs. 5, 18, 36; Ex. 1007 ¶¶ 49–50, 53, 55–57, Figs. 1, 6–7; Ex. 1025, 30). In the Reply, Petitioner expands on this, arguing that a person of ordinary skill in the art "would be motivated to distribute the self-test functionalities in a way that matches how those functionalities are distributed in the memory module." Reply 36–37 (citing Ex. 1061 ¶ 786 (citing Ex. 1016 at 3, 25; Ex. 1058 at 3, 26; Ex. 1017 at 2–12; Ex. 1018 at 2:38–67; Ex. 1019, Figs. 1, 8)).

Dr. Subramanian testifies that the prior art teaches the use of the same interfaces and signal traces that are used during normal operation. Ex. 1061 ¶ 783. For example, he testifies that Jeddeloh "teaches to put all the self-test functionality blocks in the central hub (self-test module 290) and use the existing data/address/command interfaces (270) and connections from the central hub to the memory devices (240) which are also used during normal operation." *Id.* (citing Ex. 1006, Fig. 2). Dr. Subramanian further testifies that "Tsern also teaches to follow the existing structure of its module where each of the distributed buffers (100a-d) has existing address/command lines (103) and data lines (102) to the memory devices (101), and put a separate

self-test module (1883) in each of those buffers." *Id.* (citing Ex. 1019, Figs. 1, 18). To that end, Dr. Subramanian testifies that "if the memory module as a central hub . . . which uses address/command and data signals to interface with the memory devices, then the corresponding self-test functionalities of generating test address/command and data signals would also be implemented in that central hub." Ex. 1061 ¶ 786 (citing Ex. 1016 at 3, 26; Ex. 1017 at 2-12; Ex. 1018 at 2:38–67; Ex. 1058 at 3, 26). Dr. Subramanian further testifies that "if the memory module has distributed buffers," like in Tsern, "where each buffer handles both address/command and data signals, the corresponding self-test functionalities of generating test address/command and data signals are distributed the same way, replicating the self-test functionalities in each buffer." *Id.* (citing Ex. 1019, Figs. 1, 18). Dr. Subramanian compares Tsern's distributed data buffers to Ellsberry's Switch ASICs. Ex. 1003 ¶ 159; *see also* Pet. 36.

We do not see how these references support Petitioner's proposed combination, or provide a motivation to a person of ordinary skill in the art to divide Jeddeloh's circuitry and functionality and incorporate it into Ellsberry's Switch ASIC and Control ASIC. Rather, Petitioner's arguments here are similar to its arguments relying on Ellsberry's distributed architecture as motivation to divide Jeddeloh's circuitry and functionality, as discussed above.

Although each of Tsern, Schaffer, and Averbuj disclose a distributed buffer, akin to the Switch ASICs in Ellsberry, none of the references cited by Petitioner teaches separating testing data and address logic, as in the proposed combination. *See* Sur-reply 14. As Dr. Brogioli testifies, each of these references "kept data and address/control generation elements

consolidated on the PCBs of their respective memory modules, unlike how the '523 Patent teaches." Ex. 2004 ¶ 149; *see* PO Resp. 58, Sur-reply 17. This testimony is supported by the disclosure in these references. For example, Tsern discloses a single redundancy and repair unit 1883 in buffer 100a that sends address/control signals over path 1005 and data signals over path 1006. PO Resp. 58; *see* Ex. 1019, Figs. 5, 18. Dr. Subramanian even testified that each of the repeating components in Tsern's buffers (i.e., data slice) includes all of the same circuitry and functionality. Ex. 2005, 159:11–160:22; see Ex. 1019, Fig. 5. Schaffer provides a similar disclosure to Tsern. *See* Ex. 1020, Figs. 5, 18, 36. Averbuj discloses both address generation unit 42 and data generation unit 44 in memory interfaces 41. Ex. 1007, ¶¶ 48–51, Fig. 6. Moreover, Dr. Subramanian testified during his deposition that "none of these references teach breaking up the self-test functional blocks the way the '523 Patent does." Ex. 2004 ¶ 148; Ex. 2004, 181:19–182:4, 182:9–19, 183:10–15.

Although these references may support placing self-test functionality into distributed data buffers, i.e., Ellsberry's Switch ASICs, they do not fully support the combination proposed by Petitioner, that is, dividing the data logic in one location (i.e., Ellsberry's Switch ASIC) and the address/control in a different location (i.e., Ellsberry's Control ASIC) in the context of a self-test environment. In other words, all Petitioner has established is that the self-test functionality in the cited references was in the same location, e.g., a central hub or repeated in distributed buffers, but not that it was split, as in the proposed combination, and as is required by the claims. We find that the disclosure in these references does not support the proposed combination; rather, it further reinforces that the proposed combination is

driven by hindsight. We agree with Patent Owner that "Petitioner cites no example anywhere attempting disaggregated data and address handling for testing, much less doing so into distributed memory architecture like Ellsberry." PO Resp. 38 (citing Ex. 2004 ¶¶ 123–125, 143).

For the fourth rationale for distributing Jeddeloh's functionality into Ellsberry, Petitioner relies upon the Lepejian reference, asserting that it "teaches [a person of ordinary skill in the art] that, in order to reduce busing area, pattern generators should be distributed to each of the Switch ASICs." Pet. 36 (citing Ex. 1021, 3:45–53; Ex. 1003 ¶ 162). However, similar to Petitioner's reliance on the other references discussed above, this merely establishes that Lepejian discloses redundantly distributing functionality across Switch ASICs, but does not provide motivation for the proposed combination, i.e., distributing the self-test functionality across the Switch ASIC and Control ASIC. *See* PO Resp. 58–59.

In view of the number and extent of modifications necessary to achieve the proposed combination of Ellsberry and Jeddeloh, this indicates that the series of proposed modifications are the result of hindsight. *See Metalcraft of Mayville, Inc. v. The Toro Co*., 848 F.3d 1358, 1367 (Fed. Cir. 2017) ("[W]e cannot allow hindsight bias to be the thread that stitches together prior art patches into something that is the claimed invention."); *InTouch Techs., Inc. v. VGO Commc'ns, Inc*., 751 F.3d 1327, 1351 (Fed. Cir. 2014) (criticizing use of the challenged patent as a "roadmap" for putting what the expert referred to as "pieces of a 'jigsaw puzzle'" together). We, therefore, find that the evidence does not show that a person or ordinary skill in the art would have been motivated to make the alleged modifications to Jeddeloh and Ellsberry without the benefit and knowledge of the '523

patent. See *In re NTP, Inc.*, 654 F.3d 1279, 1299 (Fed. Cir. 2011) (internal quotations omitted) (an obviousness analysis must "avoid hindsight reconstruction by using the patent in suit as a guide through the maze of prior art references, combining the right references in the right way so as to achieve the result of the claims in suit."). Specifically, we determine that Petitioner has not provided sufficient reasoning establishing why a person of ordinary skill in the art would have been motivated to divide the self-test functionality of Jeddeloh's Figure 3 between the Control ASIC and Switch ASICs of Ellsberry and that the skilled artisan would have had a reasonable expectation of success in doing so.

Accordingly, for the foregoing reasons, we determine that Petitioner has not established that claims 1–34 are unpatentable over Ellsberry and Jeddeloh.

E. Grounds 2–4; Obviousness Over Ellsberry, Jeddeloh, and Averbuj/Lee/Averbuj and Lee

Petitioner relies on the same motivation to combine Ellsberry and Jeddeloh in the remaining grounds. *See* Pet. 104–113. Therefore, for the same reasons as set forth above for Ground 1, we determine that Petitioner has not established that claims 1–34 are unpatentable.

IV. MOTIONS TO EXCLUDE

A. Petitioner's Motion to Exclude

Petitioner contends that in its Sur-reply, Patent Owner improperly relies upon testimony from Petitioner's expert reading from certain documents in order to "backdoor" certain exhibits into evidence. Pet. Mot. Excl. 4. Petitioner identifies these as Exhibits 2010, 2011, 2012, and 2014, but states that Patent Owner did not submit these exhibits with its Sur-reply.

Id. This testimony is purportedly related to when the labels "LRDIMM" and "FBDIMM" were first introduced. *Id.* at 3–4. Petitioner, therefore "requests that the Board exclude any attempt by Patent Owner to use any testimony related to Exhibits 2010, 2011, 2012, or 2014 concerning when the labels 'LRDIMM' and 'FBDIMM' were first introduced." *Id.* at 5.

Patent Owner argues that the deposition excerpts at Exhibit 2016, 57:17–58:15 and 79:8–80:1 show permissible questioning regarding information within Dr. Subramanian's personal knowledge. PO Opp. Mot. Excl. 1–4. In addition, Patent Owner contends that Petitioner's motion to exclude is improper in that it (1) seeks to exclude evidence that is not cited or relied upon; (2) cites to no authority for the Board to strike testimony based on speculation as to what might occur in the future; and (3) is overbroad in that it is unclear what is encompassed by the request. *Id.* at 5.

In Reply, Petitioner argues that the cited testimony shows that Dr. Subramanian lacked personal knowledge, and, is therefore inadmissible. Pet. Mot. Excl. Reply 2–4.

Although Petitioner cites to testimony as part of its arguments, Petitioner does not clearly identify what testimony it seeks to exclude. Petitioner cites to Exhibit 2016 at 48:20–49:11, 49:17–50:6, 50:25–51:15, 52:3–7, 57:17–58:15, 71:21–72:16, 74:2–4, 76:1–24, 77:1–78:2, 79:8–80:1. *See* Pet. Mot. Excl. 3–5; Pet. Mot. Exclude Reply 2–3. In the Reply, Petitioner also cites to Exhibit 2016, 80:2–81:1. Pet. Mot. Excl. Reply 4.

We do not rely on any of the foregoing testimony in this Decision. *See supra*, Section III.D.3, including fn. 9. Therefore, Petitioner's Motion to Exclude is dismissed as moot.

B. Patent Owner's Motion to Exclude

Patent Owner seeks exclusion, in whole or in part, of Exhibits 1012, 1014–1017, 1022, 1024, 1028, 1029, and 1031, as well as any related testimony that is relied upon by Petitioner. PO Mot. Excl. 1. Patent Owner contends that Petitioner (1) has not properly authenticated these exhibits and (2) that they are inadmissible hearsay. PO Mot. Excl. 5–8; PO Mot. Excl. Reply 1–4. In response, Petitioner contends that (1) for various reasons, each of the exhibits have been properly authenticated, and (2) the exhibits are not inadmissible hearsay because they are merely used to "show the state of the art and the knowledge of one of ordinary skill in the art." Pet. Opp. Mot. Excl. 1–14.

We do not rely on any of these exhibits in rendering our Decision. *See supra* Section III.D.3. Therefore, Patent Owner's Motion to Exclude is dismissed as moot.

V. CONCLUSION

For the foregoing reasons, we are not persuaded that Petitioner has established by a preponderance of the evidence that claims 1–34 of the '523 patent are unpatentable.

In summary:

Claims	35 U.S.C. §	Reference(s)/Basis	Claims Shown Unpatentable	Claims Not shown Unpatentable
1–34	103(a)	Ellsberry, Jeddeloh		1–34
1–34	103(a)	Ellsberry, Jeddeloh, Averbuj		1–34
14, 17–34	103(a)	Ellsberry, Jeddeloh, Lee		14, 17–34
14, 17–34	103(a)	Ellsberry, Jeddeloh, Averbuj,		14, 17–34

		Lee		
Overall Outcome				1–34

VI. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that claims 1–34 of the '523 patent have not been shown to be unpatentable under 35 U.S.C. § 103(a); and

FURTHER ORDERED that Petitioner's Motion to Exclude (Paper 44) is *dismissed as moot*; and

FURTHER ORDERED that Patent Owner's Motion to Exclude (Paper 43) is *dismissed as moot*; and

FURTHER ORDERED that, because this is a final written decision, parties to this proceeding seeking judicial review of our Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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