UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

OCEAN SEMICONDUCTOR LLC, *Plaintiff*, **vs. MEDIATEK INC., ET AL.**, *Defendant*.	**NO. 6:20-cv-01210-ADA**
OCEAN SEMICONDUCTOR LLC, *Plaintiff*, **vs. NVIDIA CORPORATION**, *Defendant*.	**NO. 6:20-cv-01211-ADA**
OCEAN SEMICONDUCTOR LLC, *Plaintiff*, **vs. NXP SEMICONDUCTORS NV, ET AL.**, *Defendant*.	**NO. 6:20-cv-01212-ADA**
OCEAN SEMICONDUCTOR LLC, *Plaintiff*, **vs. RENESAS ELECTRONICS CORPORATION, ET AL.**, *Defendant*.	**NO. 6:20-cv-01213-ADA**
OCEAN SEMICONDUCTOR LLC, *Plaintiff*, **vs. SILICON LABORATORIES INC.,** *Defendant*.	**NO. 6:20-cv-01214-ADA**
OCEAN SEMICONDUCTOR LLC, *Plaintiff*, **vs. STMICROELECTRONICS INC.**, *Defendant*.	**NO. 6:20-cv-01215-ADA**
OCEAN SEMICONDUCTOR LLC, *Plaintiff*, **vs. WESTERN DIGITAL TECHNOLOGIES, INC.**, *Defendant*.	**NO. 6:20-cv-01216-ADA**

DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS

Pursuant to the Court's Scheduling Order dated July 15, 2021, each of Defendants MediaTek Inc.; MediaTek USA Inc.; NVIDIA Corporation; NXP USA, Inc.; Renesas Electronics Corporation; Renesas Electronics America, Inc.; Silicon Laboratories Inc.; STMicroelectronics, Inc.; and Western Digital Technologies, Inc. (collectively "Defendant" or "Defendants") hereby submits the following Preliminary Invalidity Contentions regarding U.S. Patent Nos. 6,660,651 ("the '651 patent"), 6,907,305 ("the '305 patent"), 6,725,402 ("the '402 patent"), 6,968,248 ("the '248 patent"), 7,080,330 ("the '330 patent"), 6,836,691 ("the '691 patent"), 8,676,538 ("the '538 patent"), 6,420,097[1] ("the '097 patent"), 8,120,170[2] ("the '170 patent"), and 8,847,383[3] ("the '383 patent") (collectively, "the Asserted Patents").

Plaintiff Ocean Semiconductor LLC ("Ocean") alleges in its July 2, 2021, Preliminary Infringement Contentions that certain Defendants infringe the following claims of the Asserted Patents (collectively, the "Asserted Claims"):

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[1] The '097 Patent is asserted only against NXP USA, Inc. and STMicroelectronics, Inc. in No. 6:20-cv-01212 and No. 6:20-cv-01215, respectively. All references to the '097 Patent in these Invalidity Contentions apply only to NXP USA, Inc. and STMicroelectronics, Inc. and not to the other Defendants or their cases, although the other Defendants reserve the right to rely on the '097 Patent and its prior art as appropriate to demonstrate invalidity of the patents asserted against them.

[2] The '170 Patent is asserted only against NVIDIA Corporation in No. 6:20-cv-01211. All references to the '170 Patent in these Invalidity Contentions apply only to NVIDIA Corporation and not to the other Defendants or their cases, although the other Defendants reserve the right to rely on the '170 Patent and its prior art as appropriate to demonstrate invalidity of the patents asserted against them.

[3] The '383 Patent is asserted only against NVIDIA Corporation in No. 6:20-cv-01211. All references to the '383 Patent in these Invalidity Contentions apply only to NVIDIA Corporation and not to the other Defendants or their cases, although the other Defendants reserve the right to rely on the '383 Patent and its prior art as appropriate to demonstrate invalidity of the patents asserted against them.

Patent	Asserted Claims
6,660,651	Claims 19, 20, 21, 22, 23, 24, 31, 32, 34, 35, 36, 37, 72, 73, 74, 75, 77, 78, 79, 80, 81
6,907,305	Claims 1, 2, 3, 4,[4] 5, 7, 8,[5] 9,[6] 10, 11
6,725,402	Claims 1, 2, 3, 4, 5, 6, 7
6,968,248	Claims 1, 2, 3, 4, 5, 6,[7] 7, 8, 9, 10, 11, 12
8,676,538	Claims 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16
7,080,330	Claims 19, 20, 21
6,836,691	Claims 1, 2, 3, 4, 5, 6, 7, 8, 9
6,420,097[8]	Claims 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 17
8,120,170[9]	Claims 1, 8, 9, 10, 11, 12, 13
8,847,383[10]	Claims 1, 2, 8, 9

Defendant reserves the right to supplement and/or amend these Preliminary Invalidity Contentions should Plaintiff supplement and/or amend its Preliminary Infringement Contentions or otherwise alter its theory of the case.[11] Nothing in these Preliminary Invalidity Contentions constitutes an admission of validity as to any other non-asserted claims of the Asserted Patents.

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[4] This claim is only asserted against STMicroelectronics, Inc., Western Digital Technologies, Inc. ("WDT"), MediaTek Inc., and MediaTek USA Inc. (collectively "MediaTek").

[5] This claim is only asserted against NVIDIA Corporation, WDT, and MediaTek.

[6] This claim is only asserted against STMicroelectronics, Inc., WDT, and MediaTek.

[7] This claim is only asserted against NVIDIA Corporation, WDT, and MediaTek.

[8] As noted *supra*, this patent is not asserted against all Defendants.

[9] As noted *supra*, this patent is not asserted against all Defendants.

[10] As noted *supra*, this patent is not asserted against all Defendants.

[11] Including in view of any inconsistent positions Ocean may take between *inter partes* review proceedings relating to the Asserted Patents, e.g., in its preliminary responses and other briefing, and this litigation.

As discussed below, Defendant contends that each Asserted Claim is invalid under at least 35 U.S.C. §§ 101, 102, 103, and/or 112.

A. PRELIMINARY STATEMENT AND RESERVATION OF RIGHTS

Defendant's Preliminary Invalidity Contentions reflect its present knowledge and understanding of Ocean's Preliminary Infringement Contentions regarding the Asserted Claims. Defendant's Preliminary Invalidity Contentions are based on Defendant's current knowledge, understanding, and belief as to the facts and information available as of the date of these Preliminary Invalidity Contentions. Defendant has not yet completed its investigation, discovery, or analysis of matters relating to the invalidity of the Asserted Claims, including without limitation invalidity due to on-sale or public use statutory bars. In addition, Defendant's search for prior art is ongoing. Accordingly, Defendant reserves the right to amend, modify, and supplement, without prejudice, these Preliminary Invalidity Contentions as additional information is discovered or otherwise identified or appreciated, including testimony about the scope and content of the claimed inventions or state of the prior art.

Defendant submits these Preliminary Invalidity Contentions without waiving Defendant's position that Ocean's Infringement Contentions do not adequately identify with sufficient specificity the basis for Ocean's contention that any accused product is manufactured by a process that meets the limitations of any of the Asserted Claims. Nothing stated herein is or shall be treated as an admission or suggestion that Defendant agrees with Ocean regarding either the scope of any of the Asserted Claims or the claim constructions advanced directly or implicitly by Ocean's Preliminary Infringement Contentions or in any other pleading, discovery request or response, or written or verbal communications with Defendant. Additionally, nothing in these Preliminary Invalidity Contentions shall be treated as an admission that any accused products meet any limitation of the Asserted Claims. The disclosures herein are not and should not be construed as

a statement that no other persons have discoverable information, that no other documents, data compilations, or tangible things exist that Defendant may use to support its claims or defenses, or that no other legal theories or factual bases will be pursued.

In the absence of a claim construction order from the Court, Defendant has based these Preliminary Invalidity Contentions upon its knowledge and understanding of the potential scope of the Asserted Claims at this time, and, in part, upon the apparent constructions of the Asserted Claims advanced by Ocean in its Preliminary Infringement Contentions. Furthermore, Ocean's Preliminary Infringement Contentions contradict how a person of ordinary skill in the art would understand the Asserted Patents and the claim terms, and are vague and conclusory concerning how certain claim limitations supposedly read on the accused products or activities. Thus, Defendant is unable to discern Ocean's position regarding the construction of numerous claim limitations and has provided these Preliminary Invalidity Contentions based in part on its present understanding of Ocean's apparent constructions. Finally, Defendant's Preliminary Invalidity Contentions do not represent Defendant's agreement or view as to the meaning of any claim term contained therein, and Defendant may disagree with Ocean's interpretation of the meaning of terms and phrases in the Asserted Claims. In addition, Defendant's Preliminary Invalidity Contentions do not represent Defendant's agreement or view as to whether any claim preamble is limiting.

Defendant also anticipates that the Court's construction of claim terms may significantly affect the scope of the Asserted Claims. Therefore, Defendant reserves the right to supplement, without prejudice, these Preliminary Invalidity Contentions as appropriate depending upon the Court's construction of the Asserted Claims, any findings as to the priority date of the Asserted

Patents, and positions that Ocean or its expert witnesses may take concerning claim interpretation, infringement, or invalidity issues.

Defendant provides certain claim charts as described herein. The claim charts reflect the theories of invalidity described in each chart, including anticipation and obviousness. The suggested obviousness combinations are in the alternative to Defendant's anticipation contentions. The disclosed obvious combinations are not meant to be exhaustive and should not be construed to suggest that any reference does not anticipate claims of the Asserted Patents. As reflected in the attached exhibits, the discussion herein, and in the references themselves, all elements of Ocean's Asserted Claims were disclosed in the art and in the general knowledge of a person of ordinary skill before the Asserted Patents' earliest possible priority date. Furthermore, one of ordinary skill in the art would have readily combined their teachings. Each of the references cited herein, including the identified prior art systems, or in the attached exhibits may be combined and modified in several obvious ways to achieve the claimed systems and methods, including those disclosed in the attached exhibits or the discussion herein.

Defendant further contends that various asserted claims of the Asserted Patents are invalid under 35 U.S.C. § 101 for failure to claim patentable subject matter and/or under 35 U.S.C. § 112 for failure to satisfy the enablement, written description, and/or definiteness requirements. Defendant's contentions of invalidity under § 101 and/or § 112 are based in whole or in part on its present understanding of the Asserted Claims and Ocean's apparent construction of those claims in its Preliminary Infringement Contentions. Accordingly, Defendant's Preliminary Invalidity Contentions may reflect alternative positions as to claim construction and scope of the Asserted Claims. Further, by asserting grounds for invalidity based on Ocean's apparent claim construction

or any other particular claim construction, Defendant is not adopting Ocean's claim construction, nor admitting to the accuracy of any particular claim construction.

Defendant provides invalidity claim charts as exhibits as shown below:

Patent	Exhibits for Corresponding Charts
6,660,651	A
6,907,305	B
6,725,402	C
6,968,248	D
8,676,538	E
7,080,330	F
6,836,691	G
6,420,097	H
8,120,170	I
8,847,383	J

B. PRIORITY AND CONCEPTION DATES FOR THE ASSERTED CLAIMS

In its Preliminary Infringement Contentions, Ocean contends that the Asserted Claims of some Asserted Patents are entitled to priority based on the filing dates of U.S. Application No. 10/135,145, U.S. Application No. 12/110,798, U.S. Application No. 11/469,194, and U.S. Application No. 11/469,194. Defendant disputes whether any Asserted Claim is entitled to any priority date earlier than the filing dates of the applications for the Asserted Patents.

Ocean further contends that the alleged inventions of the Asserted Claims were conceived as of February 12, 2001 for the '651 patent; January 29, 1999 for the '402 patent; May 3, 2002 for the '330 patent; January 7, 2003 for the '691 patent; and November 7, 1999 for the '097 patent.

Defendant disputes whether any Asserted Claim is entitled to a conception date earlier than the filing dates of the applications for the Asserted Patents.

C. INVALIDITY UNDER 35 U.S.C. §§ 102 AND 103

Defendant contends that each Asserted Claim is invalid at least under 35 U.S.C. § 102, including pre-AIA subsections 102(a), 102(b), 102(e), and 102(g), AIA subsections 102(a)(1) and 102(a)(2), and/or under 35 U.S.C. § 103. Pursuant to the Order Governing Proceedings, Defendant's detailed contentions as to how each identified prior art reference either anticipates or renders obvious the Asserted Claims are attached as Exhibits. For each Asserted Patent, the Exhibits contain a separate chart for each anticipating and/or primary obviousness reference detailing where that reference teaches each limitation of the Asserted Claims. For each Asserted Patent, the Exhibits also contain an omnibus combination reference chart detailing which limitations are taught by each combination reference. Defendant reserves the right to combine each anticipating and/or primary obviousness reference with (1) other anticipating and/or obviousness references, (2) any reference described in the omnibus reference chart, or (3) a combination thereof. Defendant also reserves the right to rely on other references disclosed or incorporated by reference in these Preliminary Invalidity Contentions, in the Asserted Patents, any patents or applications related to the Asserted Patents, in the file history of the Asserted Patents or any related patents or applications, and in the attached Exhibits.

Defendant's claim charts may disclose multiple theories of invalidity in a single chart. Each chart directed to an anticipatory product/system may also describe that the product/system alone, in light of the knowledge and skill in the art, or in light of one or more other prior art references, renders each Asserted Claim obvious.

Where Defendant cites to a particular figure in a prior art reference, the citation should be understood to encompass the caption and description of the figure as well as any text relating to

the figure in addition to the figure itself. Conversely, where a cited portion of text refers to a figure, the citation should be understood to include the figure as well. Furthermore, while Defendant has generally identified at least one citation per limitation present in a reference or combination, each and every disclosure of the same or similar limitation in the same reference or combination is not necessarily identified. To focus the issues, Defendant cites only particularly pertinent portions of identified references, even where a reference or combination may contain additional support for a particular claim element. Thus, Defendant may rely on uncited portions of the prior art references for additional support for a particular element. Defendant may rely upon other prior art identified in future supplements, corroborating references, documentation, source code, products, and testimony, including materials obtained through further investigation and third-party discovery of the prior art identified herein, that demonstrates the invalidating functionality identified in these Preliminary Invalidity Contentions or that show the state of the art in the relevant time period (irrespective of whether such references themselves qualify as prior art to the Asserted Patent), and expert testimony to provide context to or aid in understanding the cited portions of the identified prior art. Similarly, where there are multiple references relating to a single prior art product or system, Defendant may cite only to a single reference for a particular limitation, even though other references may also contain similar teachings. Thus, Defendant may rely on uncited references relating to a particular prior art document or system for additional support for a particular element. Any prior art disclosed as anticipating a limitation also renders that limitation obvious.

Certain of the Asserted Claims are also invalid due to obviousness-type double patenting based on the grounds discussed in Section d.3 below.

Additionally, persons of ordinary skill in the art at the time of the alleged inventions generally read a prior art reference as a whole and in the context of other publications and literature. Numerous prior art references, including those identified herein and in the attached exhibits, reflect common knowledge and the state, scope, and content of the prior art before the priority date of the Asserted Claims of the Asserted Patents. Defendant may rely on uncited portions of the prior art references and on other publications and expert testimony to provide context and as aids to understanding and interpreting the portions that are cited.

In general, a claimed invention is invalid due to obviousness "if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art." 35 U.S.C. § 103; *Graham v. John Deere Co*., 383 U.S. 1, 13-14 (1966). The ultimate determination of whether an invention is or is not obvious is a legal conclusion based on underlying factual inquiries including: "(1) the scope and content of the prior art; (2) the differences between the prior art and the claims; (3) the level of ordinary skill in the art at the time of invention; and (4) objective evidence of nonobviousness." *Miles Labs., Inc. v. Shandon, Inc.*, 997 F.2d 870, 877 (Fed. Cir. 1993); *see Graham*, 383 U.S. at 17-18. The U.S. Supreme Court decision in *KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1739 (2007) reaffirmed *Graham*, but further held that a claimed invention can be obvious even if there is no explicit teaching, suggestion, or motivation for combining the prior art to produce that invention.

To the extent that any claim limitation is not anticipated pursuant to 35 U.S.C. § 102, Defendant contends that any purported differences are such that the claimed subject matter as a whole would have been obvious to one skilled in the art at the time of the alleged inventions, in view of the state of the art and knowledge of those skilled in the art under 35 U.S.C. § 103. Each

Asserted Claim would have been obvious in view of each reference cited in the attached Exhibits either alone or combined with the knowledge that was possessed by one of ordinary skill in the art. Additionally, each Asserted Claim would have been obvious to one of ordinary skill in the art in view of the combination of any one of the prior art references identified in the attached Exhibits with one or more of the other references identified or discussed in the same Exhibits.

In particular, those of ordinary skill in the art at the time of the alleged inventions of the Asserted Patents would have been motivated to modify or combine the prior art references because, for example: (a) the references in general deal with the same or related subject matter; (b) one of ordinary skill in the art would have been motivated by the problem that the inventor was attempting to solve, or with other problems that would have been faced in reaching a solution, and would have looked to references that concerned similar issues or taught how to overcome the problems faced; (c) the combinations were obvious to try and would have operated in their known and expected way; (d) the combinations were within the technical skill and understanding of a person of ordinary skill in the art; (e) the combinations would have been motivated by the developments in technology; and (f) the combinations reflect various design choices that would have been known to one of ordinary skill in the art and within that person's technical capability to implement (i.e., technically feasible).

The various motivations described above provide a basis for combining or modifying references, as detailed below, to render each of the Asserted Claims obvious. In addition, the Court can consider the inferences and creative steps a person of ordinary skill in the art would employ in making such combinations. *See KSR*, 127 S. Ct. at 1741 ("a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ").

If, and to the extent, Ocean challenges the correspondence of the references in the Exhibits with respect to particular limitations of the Asserted Claims of the Asserted Patents, Defendant reserves the right to supplement these Preliminary Invalidity Contentions to identify additional combinations, motivations to modify, or explanations for particular references with additional particularity.

Additionally, Defendant believes that certain non-parties and current or former employees thereof may have possession of relevant information and/or documents constituting prior art to the Asserted Patents, including prior art products and systems. Defendant has identified several prior art products and systems in these Preliminary Invalidity Contentions. Defendant is continuing its investigation into these and other companies and their products. Defendant reserves the right to supplement these Preliminary Invalidity Contentions to identify additional references, combinations, motivations to modify, or explanations for particular references based on any information and/or documents provided by the former employees and/or successors-in-interests of companies or individuals who may possess relevant information and/or documents constituting prior art to the Asserted Patents, including information and documents about prior art systems. The concepts disclosed and claimed in each of the Asserted Patents are not new, and had been disclosed, used, offered for sale, sold, and practiced by others prior to the claimed priority date of the patents. The prior art identified herein and in the Exhibits, individually or in combination, invalidates the asserted claims under 35 U.S.C. §§ 102 (a), (b), (e), (g) and §103. Because discovery has not yet opened, Defendants expect to gather additional information about the identified prior art, and other prior art, through third party discovery or other discovery, and will thus amend and supplement these invalidity contentions once they obtain that discovery and have meaningful and reasonable time to analyze it.

Moreover, Defendant reserves the right to rely on inventor admissions concerning the scope of the prior art relevant to the Asserted Patents found in, inter alia, the prosecution histories of the Asserted Patents or related patents and/or patent applications, any testimony or declarations of the named inventors concerning the Asserted Patents or related patents, and any papers or evidence submitted by Plaintiff in connection with this litigation, any other pending or future litigation brought by Plaintiff involving the Asserted Patents or related patents, or *inter partes* review proceedings involving the Asserted Patents or related patents. Defendants also may establish what was known to a person having ordinary skill in the art through treatises, published industry standards other publications, products, and/or testimony.

a. The '651 Patent

1. Identification of Prior Art

The tables below list prior art that anticipates and/or renders obvious one or more of the asserted claims. The attached claim charts in Exhibits A1-A14 demonstrate where each limitation of the claims is found in certain of the references listed below, either expressly or inherently in the larger context of the passage, as understood by a person having ordinary skill in the art. The following patents, publications, products and/or services are prior art under at least 35 U.S.C. §§ 102(a), (b), or (e).

a. Prior Art Patents, Patent Publications, And Printed Publications To The Asserted Claims of the '651 Patent.

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
A1	International Publication No. WO 01/22480	September 20, 1999	March 29, 2001	Tanaka
A1	U.S. Patent No. 6,940,582	May 21, 2001	September 6, 2005	Tanaka '582
A2	Japanese Patent Application Publication No. JP H11-274031	March 20, 1998	October 8, 1999	Wakui

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
A2	U.S. Patent No. 6,327,026	March 17, 1999	December 4, 2001	Wakui '026
A4	Sluijk et al., *Performance results of a new generation of 300-mm lithography systems*, Optical Microlithography XIV, Proceedings of SPIE Vol. 4346, 544-557 (2001)	N/A	February 25, 2001	Sluijk
A5	U.S. Patent No. 6,416,635	July 24, 1995	July 9, 2002	Hurwitt
A6	U.S. Patent No. 6,086,727	June 5, 1998	July 11, 2000	Pinarbasi
A7	U.S. Patent App. Pub. No. 2002/0039179	October 4, 2001	April 4, 2002	Tanaka '179
A8	U.S. Patent No. 6,258,220	April 8, 1999	July 10, 2001	Dordi
A9	European Patent Appl. No. EP 0 973 067	July 15, 1999	January 19, 2000	Loopstra
A10	International Publication No. WO 98/022638	November 7, 1997	May 28, 1998	Hawkins
A11	U.S. Patent No. 6,486,492	June 29, 1999	November 26, 2002	Su
A11	U.S. Patent No. 6,150,664	June 29, 1999	November 21, 2000	Su '664
A12	U.S. Patent No. 6,861,614	July 7, 2000	March 1, 2005	Tanabe
A13	International Publication No. WO 99/005703	July 23, 1997	February 4, 1999	Li
A14	U.S. Patent No. 6,707,529	February 12, 1999	March 16, 2004	Aoki
	Butler, et al., "*Scanning stage for exposure tools,*" Microlithography World (Spring 1999)	N/A	Spring 1999	Butler
	U.S. Patent No. 6,068,784	October 3, 1989	May 30, 2000	Collins '784
	U.S. Patent No. 6,251,792	July 31, 1990	June 26, 2001	Collins '792
	U.S. Patent No. 4,836,905	July 16, 1987	June 6, 1989	Davis
	U.S. Patent No. 6,538,720	February 28, 2001	March 25, 2003	Galburt
	U.S. Patent No. 4,952,858	May 18, 1988	August 28, 1990	Galburt '858

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
	International Publication No. WO 00/058994	March 1999, 31	October 5, 2000	Hao
	U.S. Patent No. 6,961,113	May 28, 1999	November 1, 2005	Hayashi
	U.S. Patent No. 6,133,982	November 15, 1996	October 17, 2000	Inoue
	European Patent Appl. No. EP 1 030 351	November 12, 1997	August 23, 2000	Magome
	U.S. Patent No. 5,474,647	November 15, 1993	December 12, 1995	Poultney
	International Publication No. WO 99/034257	December 29, 1997	July 8, 1999	Sperling
	U.S. Patent No. 5,877,843	September 12, 1995	March 2, 1999	Takagi
	U.S. Patent No. 5,926,690	May 28, 1997	July 20, 1999	Toprac
	Zwart et al., "*Performance of a Step and Scan System for DUV Lithography*," Proc. SPIE, Optical Microlithography (Mar. 1997)	N/A	March 1997	Zwart
	Japanese Patent Application Publication No. JP H 10-177942	October 16, 1996	June 30, 1998	Kida
	Japanese Patent Application Publication No. JP H 6-204107	December 25, 1992	July 22, 1994	Nose
	Japanese Patent Application Publication No. JP H 10-125586	October 16, 1996	May 15, 1998	Hoshino '586
	Japanese Patent Application Publication No. JP H 6-145974	October 29, 1992	May 27, 1994	Hoshino '974
	U.S. Patent No. 6,614,050	October 25, 2000	September 2, 2003	Yamada
	U.S. Patent No. 6,512,571	April 28, 1999	January 28, 2003	Hara
	Japanese Unexamined Patent Application Publication No. 2001-143984	November 16, 1999	May 25, 2001	Sai
	U.S. Patent No. 5,701,041	October 3, 1994	December 23, 1997	Akutsu
	Japanese Patent Application Publication No. JP H 07-111238	October 12, 1993	April 25, 1995	Akutsu '238
	European Patent Application No. EP 1 037 117	February 24, 2000	September 20, 2000	Jasper

b. Prior Art Systems/Services To The Asserted Claims of the ’651 Patent

Exhibit	System/Service	Relevant Dates	Persons/Entities Involved in Prior Use, Sale, or Offers for Sale	Short Cite
A3	ASML TWINSCAN™ System	At least as early as November 8, 2000	ASML TSMC	TWINSCAN
N/A	Applied Materials Centura System	1995	Applied Materials	Centura

2. Obviousness Combinations

To the extent that any one of the anticipation references is found not to disclose a limitation recited in the asserted claims from the ’651 patent, it would have been obvious to one of ordinary skill in the art at the time of the alleged invention of the ’651 patent either (i) to modify the reference to include this limitation and any remaining limitations of this claim and any claim(s) from which this claim depends and/or (ii) to combine said reference with any other of the references in Exhibits A1 to A14 and/or with a person having ordinary skill in the art’s (“POSITA’s”) general knowledge. Generally, motivation to combine any of these references with others exists within the references themselves, as well as within the knowledge of those of ordinary skill in the art at the relevant time. A person having ordinary skill in the art would have been motivated to combine any of the references described in attached Exhibits A1 to A14, including for the reasons described below. A person having ordinary skill in the art at the time of filing of the asserted ’651 patent would have understood the references listed above, alone or in combination, to contain explicit and/or implicit teaching, suggestion, and/or rationales to combine them for at least the following exemplary reasons.

Defendant contends that it would have been obvious to modify the above-listed prior art to include any allegedly missing element, in view of the knowledge of one of ordinary skill in the art, the admitted prior art of the '651 patent, and/or in combination with any of the other prior art references identified for the '651 patent. By way of example, and without limitation, Defendant provides the following exemplary combinations for particular claim limitations based on teachings of the cited prior art references. Defendant reserves the right to rely upon any combination of prior art references whether listed herein or otherwise.

A person of ordinary skill in the art having knowledge of the above-listed patents, articles, and systems, among other things, would be motivated, taught, and suggested to combine the prior art discussed in Exhibits A1 to A14 with one another, in any number of ways, including as detailed below.

As a threshold matter, the Asserted Claims of the '651 patent simply arrange old elements known in the field of semiconductor fabrication technology, with each performing the same function it had been known to perform, and yield no more than what one would expect from such an arrangement. Such combinations of the prior art are obvious, as further detailed below.

The '651 patent uses entirely (and admittedly) conventional processing-tool components (*e.g.*, a wafer stage, actuators such as pneumatic cylinders, and a process chamber). As the '651 patent explains, the alleged novelty is simply to make adjustable the wafer stage surface of an otherwise conventional processing tool. And, even when it adds adjustability to the wafer stage, the patent relies on admittedly conventional actuators. Indeed, the patent does not purport to have invented any new actuator or processing tool component.

Of note, the '651 patent itself admits that a number of the claimed elements were commonly known, and conventional, prior to the date of the alleged invention. *See also, e.g.*, Exhibits A1–

A14 (evidencing that the components were common and conventional). For example, the '651 patent discloses that:

- "In general, semiconductor manufacturing operations involve, among other things, the formation of layers of various materials, e.g., polysilicon, insulating materials, metals, etc., and the selective removal of portions of those layers by performing known photolithographic and etching techniques. These processes, along with various ion implant and heating processes, are continued until such time as the integrated circuit device is complete." '651 patent at 1:51-58.

- "In manufacturing semiconductor devices, many deposition processes and etching processes may be performed. For example, a variety of process layers, e.g., layers of polysilicon, metal or insulating materials, may be formed by performing a variety of deposition processes, e.g., chemical vapor deposition ('CVD'), plasma enhanced chemical vapor deposition ('PECVD'), physical vapor deposition ('PVD'), etc. Additionally, a variety of etching processes, such as a dry plasma etching process, may be performed to pattern an underlying process layer." *Id.* at 2:25-34.

- "As stated previously, in manufacturing integrated circuit devices, many deposition and etching processes, e.g., CVD, PECVD and PVD deposition processes, chemical etching processes, sputter etching processes, reactive ion etching processes, etc., may be performed. The processing tools for performing such processes, i.e., deposition tools and etch tools, may have various physical configurations that depend upon a variety of factors, e.g., the manufacturer, the type of process to be performed, etc. U.S. Pat. Nos. 6,068,784 and 6,251,792 B1 depict illustrative processing tools that may be used in modern semiconductor manufacturing. Both of these patents are hereby incorporated by reference in their entirety. However, many, if not all, of such tools have a process chamber, where processing operations will be performed, and a wafer stage or chuck in the process chamber that is adapted to hold a wafer in position during processing, typically through use of vacuum pressure or one or more clamps." *Id.* at 5:3-20.

- "A mechanism useful in adjusting the position of the wafer stage 40 may be comprised of any of a variety of devices, such as pneumatic, hydraulic, electromagnetic or mechanical systems. … The pneumatic cylinders 46 may be any type of pneumatic cylinders useful for performing the function of adjusting the surface 42 of the wafer stage 40…." *Id.* at 5:65-6:21; *see also* 6:66-7:16.

- "The process tool 72 may be any type of processing tool commonly found in semiconductor manufacturing operations." *Id.* at 7:28-34.

A person of ordinary skill in the art would have had good reason to pursue and/or combine known options, with the goal of reducing process variation to meet increased demand for integrated circuits, and demand for increased operating speed of the same. As the '651 patent describes in

the "Description of Related Art" section, there was a known, strong felt need at the time to accomplish both goals:

> There is a constant drive within the semiconductor industry to increase the operating speed of integrated circuit devices, e.g., microprocessors, memory devices, and the like. This drive is fueled by consumer demands for computers and electronic devices that operate at increasingly greater speeds. This demand for increased speed has resulted in a continual reduction in the size of semiconductor devices, e.g., transistors. That is, many components of a typical field effect transistor (FET), e.g., channel length, junction depths, gate insulation thickness, and the like, are reduced. For example, all other things being equal, the smaller the channel length of the transistor, the faster the transistor will operate. Thus, there is a constant drive to reduce the size, or scale, of the components of a typical transistor to increase the overall speed of the transistor, as well as integrated circuit devices incorporating such transistors.

Id. at 1:13-30. This is further evidenced by the prior art described herein and in the accompanying exhibits. Moreover, as the '651 patent admits, a person of ordinary skill in the art would have easily understood that across-wafer variations were problematic to achieving those goals:

> Unfortunately, many processes used in manufacturing integrated circuit devices, such as deposition and etch processes, tend to exhibit across-wafer variations. For example, a deposition process may tend to produce process layers that are thicker near an edge region of the wafer than near a center region of the wafer, and vice versa. Moreover, this variation may not be uniform around the circumference of the wafer, i.e., the thickness variation may occur in only one quadrant of the wafer. Similarly, etching processes may exhibit across-wafer non-uniformity characteristics. For example, the etching rate may be greater near a center region of the wafer than it is near an edge region of the wafer. Moreover, as with deposition processes, these variations may not be uniform around the circumference of the wafer, i.e., they may occur in localized areas.
>
> Such variations are problematic in modem integrated circuit manufacturing. Such variations, even if small in absolute magnitude, may adversely impact the ability to form features on integrated circuits with the precision required for modem integrated circuit devices. Additionally, such process variations may require adjustments to subsequent processing operations in an attempt to compensate for the across-wafer variations. For example, a

> deposition process may result in a process layer that is thicker at the edge of the wafer than it is at the center of the wafer, i.e., the process layer may have a surface profile that is approximately concave. In that situation, a subsequent chemical mechanical polishing ("CMP") process may be performed in which parameters of the CMP process are adjusted in an effort to increase the polishing performed near the edge region of the wafer. Accordingly, such across-wafer variations resulting from certain processing operations are undesirable.

Id. at 2:35-67. This too is further evidenced by the prior art described herein and in the accompanying exhibits.

It was well-known and commonplace to a person of ordinary skill in the art prior to the '651 patent that, in process tools for semiconductor fabrication, the tools included a process chamber with a wafer stage therein (which is a requirement when using various processing techniques, including lithography (*e.g.*, vacuum ultraviolet), deposition, and etching), on which a wafer is held in place for processing on the stage's surface. This is discussed in, and evidenced by, a number of the prior references listed above, including (without limitation) Inoue, Tanaka, Tanaka '179, Hayashi, Tanabe, Aoki, Takagi, Magome, Collins '784, Collins '792, Davis, Galburt, Hao, Pinarbasi, Hurwitt, Dordi, Li, Hawkins, Sluijk, and TWINSCAN. Those references show that it was necessary, obvious, and commonplace to use a process chamber in conventional processing tools and that such a process chamber results in a number of known advantages (such as improving temperature control, improving wafer output and accuracy, reducing contaminants, isolating various gases, and absorbing gases from the optical path during processing), all of which results in more accurate and improved wafer processing. In fact, further confirming the conventionality and obviousness of including a process chamber with processing tools, the '651 patent itself admits that "many, if not all, of [processing tools used in modern semiconductor manufacturing] have a process chamber, where processing operations will be performed, and add a wafer stage or chuck in the process chamber that is adapted to hold a wafer in position during

processing, typically through use of vacuum pressure or one or more clamps." '651 patent at 5:15-20.

To the extent that any prior art reference or system is found not to disclose a process chamber, it would have been obvious to add such a chamber for the reasons discussed here and in the corresponding charts. For example, it would have been obvious to add a process chamber (such as disclosed in Tanaka, Inoue, Tanaka, Tanaka '179, Tanabe, Hayashi, Aoki, Takagi, Magome, and the TWINSCAN) to the processing tools of Wakui, Su '664, or Loopstra, or in the second embodiment in Tanaka (to the extent found not to be disclosed).

It was well-known and commonplace to a person of ordinary skill in the art prior to the '651 patent that, in process tools for semiconductor fabrication, the tools included a wafer stage that was adjustable in multiple degrees of freedom (*e.g.*, by raising, lowering, and tilting the stage) using a variety of known actuators (*e.g.*, pneumatic/air cylinder actuators, hydraulic actuators or electromagnetic actuators, such as Lorentz actuators) to improve the performance of the tool and the wafers processed on the stage therein. This is discussed in, and evidenced by, a number of the prior art references listed above, including (without limitation) Tanaka, Tanaka '179, Tanabe, Hayashi, Aoki, Takagi, Magome, Wakui, Inoue, Sperling, Davis, Galburt, Galburt '858, Butler, Zwart, TWINSCAN, Pinarbasi, Hurwitt, Dordi, Loopstra, Nose, Sluijk and Li—which teach the advantages of making a wafer stage adjustable using a variety of known actuators.

And, the '651 patent itself admits that pneumatic cylinders were conventional, and that "[a] mechanism useful in adjusting the position of the wafer stage 40 may be comprised of any of a variety of devices, such as pneumatic, hydraulic, electromagnetic or mechanical systems." '651 Patent at 5:65-6:1. Furthermore, "[t]he pneumatic cylinders 46 may be of any type of pneumatic

cylinders useful for performing the function of adjusting the surface 42 of the wafer stage 40." *Id*. at 6:14-16. The '651 patent also explains that:

- "A mechanism useful in adjusting the position of the wafer stage 40 may be comprised of any of a variety of devices, such as pneumatic, hydraulic, electromagnetic or mechanical systems."
- "For example, the pneumatic cylinders 46 may be dual-acting pneumatic cylinders. The stroke, size and supply pressure to such cylinders may vary depending upon the particular application. Air or an inert gas may be supplied to the cylinders 46 at the required pressure through flexible hoses (not shown)."
- "The illustrative pneumatic cylinder 46 depicted in FIG. 2 is comprised of a housing 47, a shaft 49 and a ball 51 coupled to the shaft 49."
- "The ball 51 of the cylinder 46 is operatively coupled to a housing 50 in a ball and socket arrangement 48."
- "the particular details of the manner in which the cylinders 46 are operatively coupled to the wafer stage 40 should not be considered limitations of the present invention unless such details are specifically set forth in the appended claims."

Id. at 5:65-6:40.

To the extent that any prior art reference or system is found not to disclose an adjustable wafer stage, it would have been obvious to add such an adjustable wafer stage for the reasons discussed here and in the corresponding charts (including to substitute known actuators for each other with the actuators performing according to their known, conventional and intended purposes). For example, it would have been obvious to add an adjustable wafer stage (such as disclosed in Wakui, Tanaka, Tanabe, Loopstra, Sperling, TWINSCAN, Sluijk, Davis, Galburt, Galburt '858, Butler, Nose, and Zwart) to the processing tools of Pinarbasi, Hurwitt, Dordi, Su '664, and Hawkins.

A person of ordinary skill in art would have known to use an adjustable wafer stage as it would allow for multiple degrees of freedom to alleviate variations in the wafer, including by alleviating vibrations, and also reduce the cost of the microlithography system. For example, as

early as 1988, Galburt '858 disclosed an "electro-magnetic alignment apparatus" with six independent degrees of freedom for use with "microlithographic instruments" and "which is particularly adapted, among other possible uses, for use in aligning the wafer in a microlithography system." Galburt '858 at 1:5-9, 2:66-3:20. Galburt '858 recognized that its apparatus would alleviate "vibration in the sub-stage, thereby permitting the sub-stage to be of a lower cost design, mounted without isolation from ground vibration." *Id*. at 5:28-38. These known advantages are further evidenced by the other prior art (including Wakui, Tanaka, Tanabe, Loopstra, Sperling, TWINSCAN, Sluijk, Davis, Galburt, Galburt '858, Butler, Nose, and Zwart) that describe the known improvements to wafer manufacturing (and the resulting wafers) when wafer stage adjustment mechanisms are implemented.

A person of ordinary skill in art would have known that the use of a pneumatic cylinder—a device that was well known in the art at the time of the purported invention—would provide improved accuracy for adjusting the wafer stage. For example, Loopstra, recognized limitations in the "positioning accuracy" of the device disclosed by Galburt '858. Loopstra, ¶¶ 5-7. To improve the accuracy, Loopstra implemented an adjustable wafer stage using a "pneumatic cylinder." *Id.*, ¶ 8-10. Similarly, Tanaka '179 recognized that the use of a pneumatic actuator is advantageous because such actuators are "non-magnetic and have minimal electrical conductivity," therefore providing an apparatus "that can be driven with multiple degrees of freedom of motion without disturbing neighboring magnetic fields, thereby improving the accuracy and precision of [the] process being conducted." Tanaka '179, ¶¶ 60, 66, *see also* ¶ 3 ("To ensure maximal flexibility in positioning measurement and control, many degrees of freedom of movement of the stage are desirable.").

It was also well recognized in the art that more precise adjustable wafer stages allow for improved precision in the scanning and processing of the wafer, allowing for the manufacture of improved semiconductors that were high in demand, faster scanning times, and higher throughput. *See, e.g.*, Zwart (describing the use of "step and scan technology" with a "wafer leveling system" to "increase the field size beyond 22 x 22 mm and to improve CD-control below 0.25 mm resolution."); Sluijk (describing a wafer stage with 6 degrees of freedom, and a "novel approach to wafer leveling provides a solution to the increasing requirements in focus accuracy."); Butler (describing "state-of-the-art step-and-scan stages" having a wafer stage that is controlled in six degrees-of-freedom allow for "High scanning and stepping speeds. . . essential for high throughput," and further noting that "The mechanical performance of these moving stages is as critical for scanner imaging.").

Ocean incorrectly asserts in its contentions that a Lorentz actuator can be likened to a pneumatic cylinder. Regardless, using a Lorentz actuator to adjust a wafer stage was well known in the art. The following references disclose a wafer stage that is adjusted using a Lorentz actuator: TWINSCAN, Sluijk, and Loopstra. A person of ordinary skill in the art would have found it obvious to replace the Lorentz actuator of that system (*e.g.*, the TWINSCAN, Sluijk, and Loopstra systems) with a pneumatic cylinder as such replacement would only require a simple substitution of two well-known elements. By way of example, the above-listed prior art references and systems disclose various known actuators. For example, Tanaka '179 describes—like the '651 patent—that any of a number of known actuators can be used for wafer-stage adjustment: "any of the various other types of actuators can be used such as ultrasonic, mechanical, and hydraulic/pneumatic actuators," as well as "electromagnetic (e.g., Lorentz-type, EI core, etc.) or magnetostrictive." Tanaka '179 ¶ 60. Wakui similarly discloses that it was known and

commonplace in the prior art to use various actuators, including "[a] hydraulic actuator, an air pressure cylinder, an electric motor and a ball screw, a combination of an electric motor, a decelerator, and a ball screw, a linear motor, or the like. Wakui ¶¶ 7, 26.

To the extent that any prior art reference or system is found not to disclose an adjustable wafer stage coupled to the pneumatic cylinders with a ball and socket connection, it would have been obvious to add such a ball and socket connection for the reasons discussed here and in the corresponding charts. For example, it would have been obvious to add a ball and socket connection (such as disclosed in Wakui, Loopstra, Sperling, Nose, and TWINSCAN) to the processing tools of Tanaka, Pinarbasi, Hurwitt, Dordi, Tanabe, and Sluijk. It would have been obvious to use a ball and socket connection between each pneumatic cylinder and the stage to enable further freedom of rotation, uniformly distribute supporting forces, and to reduce stresses, that may result from moving the stage with the pneumatic cylinder. *See, e.g.*, Sperling at 3 (noting that "driving forces exerted on the first part by the motors of the positioning device during operation can be transmitted to the object holder in a uniform manner by means of a comparatively light and simple stiffening construction of the first part."); *see also* Abstract, 7:20-29.

It was also well-known and commonplace to a person of ordinary skill in the art prior to the '651 patent that, process tools for semiconductor fabrication to receive a wafer on a wafer stage after the wafer stage has been adjusted (*e.g.*, raised, lowered or tilted). This occurs, for example, when the stage is returned to its original position after a processed wafer is removed from the stage so that the next wafer can be placed on the stage. This is discussed in a number of the prior references listed above, including (without limitation) Tanaka, Wakui, TWINSCAN, Hurwitt, Loopstra, Kida, Li, and Sluijk.

To the extent that any prior art reference or system is found not to disclose such timing, it would have been obvious to do so for the reasons discussed here and in the corresponding charts. For example, it would have been obvious to receive a wafer on a wafer stage after the wafer stage has been adjusted (such as disclosed in Tanaka, Kida, Wakui, TWINSCAN, Loopstra, Li, Hurwitt, and Sluijk) for the processing tools of, *e.g.*, Hawkins, Su '664, Dordi, and Pinarbasi. Further by way of example, Hurwitt explains that changes to the position of the wafer stage "might be made after every fifty wafers are processed, or at one hundred or more times over the life of a target." Hurwitt at 4:1-20.

It was also well-known and commonplace to a person of ordinary skill in the art prior to the '651 patent that process tools for semiconductor fabrication would measure a number of wafers to determine across-wafer variations, and adjust process parameters based on the across-wafer variations. This is discussed in a number of the prior references listed above, including (without limitation) TWINSCAN, Sluijk, Hurwitt, Su '664, Hawkins, Toprac, Poultney, Hoshino '586, and Hao. For example, Su '664 discloses a "method and apparatus for reducing lot to lot CD variation in semiconductor wafer processing," and where "measured parameters deviate from desired values, a linked etch recipe to correct the error is fed forward to the etcher and implemented automatically." Su '664 at Abstract. Su 664's "feedback and feed-forward mechanism improves lot to lot CD control . . ." *Id*. Su '664 explains that the motivation of its purported invention was "demands for high density and performance associated with ultra large scale integration [that] require submicron features, increased transistor and circuit speeds and improved relatability." *Id.*, 1:18-25; *see also* 1:56-65. Su '664 further explains that "CD control necessarily involves monitoring and adjusting both the photolithography and etch processes to address CD variations from field to field (FTF) within a wafer, from wafer to wafer (WTW) and from lot to lot (LTL)."

Id. at 1:66-2:16. Other references similarly disclose a need to maintain and improve process uniformity across wafers. *See, e.g.,* Hawkins at Abstract (describing a need to "improve . . . process uniformity."); Toprac at 2:36-3:14 (describing "a control method [that] employs a control system using photoresist etch time as a controlling variable in either a feedforward or a feedback control configuration to control critical dimension variation during semiconductor fabrication," so that "many advantages are achieved including a reduced lot-to-lot variation, an increased yield, and increased speed of the fabricated circuits."); Poultney (describing an advantageous "feedback control process" that "provides near real time control of the etching process."); Hao (describing a process whereby a "second wafer is then processed on the configured electrostatic chuck to produce substantially uniform process result.").

A person of ordinary skill in the art would have been very familiar with the desire and necessity to keep process parameters consistent from wafer to wafer and from lot to lot. Indeed, the '651 patent itself admits that it was well known at the time of the purported invention that "many processes used in manufacturing integrated circuit devices, such as deposition and etch processes, tend to exhibit across-wafer variations," which "adversely impact the ability to form features on integrated circuits with the precision required for modem integrated circuit devices," and "may require adjustments to subsequent processing operations in an attempt to compensate for the across-wafer variation." '651 patent at 2:35-67. This is further evidenced by the prior art discussed herein and in the accompanying claim charts.

A person of ordinary skill in the art would have recognized that wafer to wafer and lot to lot variations can be reduced using an adjustable wafer stage, as it would allow for multiple degrees of freedom to alleviate variations in the wafer (as explained above). Further, a number of prior art references and systems disclose the use of an adjustable wafer stage to adjust process parameters

to reduce wafer to wafer variations. By way of example, Hawkins discloses a wafer stage that can be moved in a process chamber. *See* Hawkins at 5:9-12 ("a substrate is supported on a platform-like structure which is commonly referred to in the art as a susceptor which is indicated herein by the reference numeral 20."), 10:34-45 ("The motor 216 is preferably mounted on a fixed frame and includes adjustment mechanisms for positioning the susceptor 208 within the chamber 200."), 1:22-24 ("For example, one may need to adjust the position of the heating lamps as well as their orientation relative to a wafer in the chamber.").

To the extent that any prior art reference or system is found not to disclose adjusting process parameters, or adjusting a wafer stage, based on across-wafer variations, it would have been obvious to do so for the reasons discussed here and in the corresponding charts. For example, it would have been obvious to adjust process parameters based on across-wafer variations (such as disclosed in TWINSCAN, Sluijk, Hurwitt, Su '664, Hawkins, Toprac, Poultney, Hoshino '586, and Hao) for the processing tools of Tanaka, Wakui, Dordi, Li, Loopstra, Tanabe, and Pinarbasi.

Further, motivation exists because the prior art references and systems all are commonly related and are from the same field of art, and a person of ordinary skill in the art would draw equally from the field of art to solve the problem allegedly presented in the '651 Patent. The combinations suggested below reflect at least combinations of prior art elements according to known methods to yield predictable results, simple substitutions of known elements to obtain predictable results, and combinations that are obvious to try. Further elaboration and information shall be provided with the Defendant's expert report(s).

The combinations of references provided above are exemplary and are not intended to be exhaustive. Additional obviousness combinations of the references identified here are possible, and Defendant may rely on such combination(s) in this litigation. In particular, Defendant is

currently unaware of Ocean's allegations with respect to the level of skill in the art and the qualifications of the typical person of ordinary skill in the art. Defendant is also unaware of the extent, if any, to which Ocean may contend that limitations of the claims at issue are not disclosed in the prior art identified by defendants as anticipatory, and the extent to which Ocean will contend that elements not disclosed in the asserted patent specifications would have been known to persons of skill in the art. And Defendant does not yet know how the Court will construe terms in the Asserted Claims. Defendant is also continuing its investigation of the large universe of prior art to identify potential prior art systems, publications related to those systems, and third parties that may have information about those systems. Ocean may also be in possession of prior art that Defendant may receive after discovery opens in this case. Defendant reserves the right to amend and supplement these contentions to identify other prior art and combinations rendering the asserted claims obvious.

b. The '305 Patent

1. Identification of Prior Art

The tables below list prior art that anticipates and/or renders obvious one or more of the asserted claims. The attached claim charts in Exhibits B1-B22 demonstrate where each limitation of the claims is found in certain of the references listed below, either expressly or inherently in the larger context of the passage, as understood by a person having ordinary skill in the art. The following patents, publications, products and/or services are prior art under at least 35 U.S.C. §§ 102(a), (b), or (e).

a. Prior Art Patents and Patent Publications To The Asserted Claims of the '305 Patent.

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
B1	U.S. Pat. No. 7,069,101	July 29, 1999	June 27, 200	"Arackaparambil"
B2	Weiming Shen and Douglas H. Norrie, "Agent-Based Systems for Intelligent Manufacturing: A State-of-the-Art Survey," Knowledge and Information Systems 1 (1999) 129-156	May 1, 1999	May 1, 1999	"Shen 1999"
B3	U.S. Pat. No. 7,072,731	April 3, 2001	July 4, 200	"Barto"
B4	U.S. Pat. No. 5,260,868	October 15, 1991	November 9, 1993	"Gupta"
B5	U.S. Pat. No. 5,442,561	May 10, 1993	August 15, 1995	"Yoshizawa"
B6	U.S. Pat. No. 6,418,350	June 9, 2000	July 9, 2002	"Hamidzadeh"
B7	U.S. Pat. No. 6,519,498	March 10, 2000	February 11, 2003	"Jevtic"
B8	Stefan A. Bussmann, "Multi-Agent Approach to Dynamic, Adaptive Scheduling of Material Flow," Pre-Proceedings, Pre-Proceedings, MAAMAW-94, Odense, Denmark, August 1994	August 1994	August 1994	"Bussmann"
B9	U.S. Pat. No. 6,671,570	October 16, 2001	December 30, 2003	"Schulze"
B10	Fletcher, M. & S. Misbah Deen, "Fault-tolerant holonic manufacturing	January 2001	January 2001	"Fletcher"

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
	systems," Concurrency Computat.: Pract. Exper.: 2001; 13:43-70			
B11	U.S. Pat. App. Pub. No. 2003/0139952	January 24, 2002	July 24, 2003	"Lubash"
B12	U.S. Pat. No. 6,470,227	December 2, 1998	October 22, 2002	"Rangachari"
B13	Richards, H.D., et al., "Manufacturing Systems: Flow of orders through a virtual enterprise their proactive planning and scheduling, and reactive control," Computing & Control Engineering Journal (Aug. 1997): 173-179	August 1997	August 1997	"Richards"
B14	Sauer, Jurgen, "Towards agent-based multi-site scheduling," Proc. of the 14th Workshop, New Results in Planning, Scheduling and Design (PuK2000), Berlin, 21-22 August 2000	August 2000	August 2000	"Sauer"
B15	Shen, W. and D. H. Norrie, "Dynamic manufacturing scheduling using both functional and resource related agents," Integrated Computer-Aided Engineering 8 (2001) 17-30 (2001)	January 2001	January 2001	"Shen 2001"
B16	Shin, Y. et al., "Modeling and implementing a real time scheduler for dual-armed cluster tools,"	May 2001	May 2001	"Shin"

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
	Computers in Industry 45 (2001) 13-27			
B17	Sun, J., "An Intelligent Manufacturing System for Predictive Scheduling and Reactive Scheduling," Proc. of the 2000 ASME Des. Eng. Tech. Conf., September 10-13, 2000	September 2000	September 2000	"Sun"
B18	Japanese Unexamined Patent Application Publication No. 2000-308949	April 27, 1999	November 7, 2000	"Toba"
B19	Japanese Published Patent Publication JP-A-9-11092	June 20, 1995	January 14, 1997	"Morii"
B20	U.S. Pat. No. 5,757,648	September 12, 1996	May 26, 1998	"Nakamura"
B21	U.S. Pat. No. 6,757,578	June 22, 2000	June 29, 2004	"Jang"
B22	PCT Publication No. WO 00/34908	October 15, 1999	June 15, 2000	"Smirnov"
B23	U.S. Pat. No. 4,796,194	August 20, 1986	January 3, 1989	"Atherton"
N/A	U.S. Pat. App. Pub. No. 2002/0156548	February 28, 2002	October 24, 2002	"Arackaprambil 2"
N/A	U.S. Pat. No. 4,888,692	November 10, 1988	December 19,1989	"Gupta 2"
N/A	PCT Publication WO 2000/034908	October 15, 1999	June 15, 2000	"Smirnov"
N/A	U.S. Pat. No. 4,796,194	August 20, 1986	January 3, 1989	"Atherton"
N/A	SEMI E105-0701	October 2000	October 2000	"SEMI E105-0701"

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
N/A	Japanese Published Patent Publication JP-A-9-19853	July 3, 1995	January 21, 1997	"Kobayashi"
N/A	U.S. Pat. No. 6,263,358	August 25, 1998	July 17, 2001	"Lee"
N/A	U.S. Pat. No. 6,889,178	October 1, 1997	May 3, 2005	"Chacon"
N/A	S. Dauzere-Peres, W. Roux, J.B. Lasserre, "Multi-resource shop scheduling with resource flexibility," European Journal of Operational Research Volume 107, Issue 2, 1 June 1998, Pages 289-305	June 1998	June 1998	"Dauzere-Peres 1998"
N/A	S. Dauzere-Peres, J. Paulli. "An integrated approach for modeling and solving the general multiprocessor job-shop scheduling problem using tabu search," Annals of Operations Research volume 70, pages281–306 (1997)	April 1997	April 1997	"Dauzere-Peres 1997"
N/A	Japanese Patent Publication No. JPH08287140	April 12, 1995	November 1, 1996	"Mitsutake"
N/A	B.L. MacCarthy and J. Liu, "Addressing the Gap in Scheduling Research: A Review of Optimization and Heuristic Methods in Production Scheduling," Int. J. Prod. Pres., Vol. 31, No. 1, 59-79 (1993)	1993	1993	"MacCarthy 1993"

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
N/A	W. Shen, L. Wang and Q. Hao, "Agent-based Distributed Manufacturing Process Planning and Scheduling: A State-of-the-art survey, "IEEE Transactions on Systems, Man, and Cybernetics, Part C (Applications and Reviews), vol. 36, no. 4, pp. 563-577 (July 2006)	July 2006	July 2006	"Shen 2006"
N/A	W. Shen, "Distributed manufacturing scheduling using intelligent agents," IEEE Intelligent Systems, vol. 17, no. 1, 88-94 (Jan.-Feb. 2002)	Jan.-Feb. 2002	Jan.-Feb. 2002	"Shen 2002"
N/A	M. Yamamoto and S. Y. Nof, "Scheduling/rescheduling in the manufacturing operating system environment," International Journal of Production Research, 23:4, 705-722 (1985)	1985	1985	"Yamamoto 1985"
N/A	J. Sun and D. Xue, "A Dynamic Reactive Scheduling Mechanism for Responding to Changes of Production Orders and Manufacturing Resources," Computers in Industry, 189-207 (2001)	2001	2001	"Sun 2001"
N/A	J. McGehee, "The	1994	1994	"McGehee 1994"

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
	MMST Computer-Integrated Manufacturing System Framework," IEEE Transactions on Semiconductor Manufacturing, 7: 107-16 (1994)			
N/A	P. Cowling and M. Johansson, "Using Real Time Information for Effective Dynamic Scheduling," European Journal of Operational Research 139, 230-244 (2002)	2002	2002	"Cowling 2002"
N/A	P. Diwan and D. Kothari, "Role of Automation and Robotics in Semiconductor Industry," IETE Technical Review, 7: 368-77 (1990)	1990	1990	"Diwan 1990"
N/A	N.R. Jennings and M. Wooldridge, "Applications of Intelligent Agents," Agent Technology, 3-28 (1998)	1998	1998	"Jennings 1998"
N/A	J.Y. Pan and J.M. Tenenbaum, "Toward an Intelligent Agent Flamework for Enterprise Integration," AAAI (1991)	1991	1991	"Pan 1991"
N/A	H. Fargher and R. Smith, "Planning for the Semiconductor Manufacturer of the Future," AAAI (1992)	1992	1992	"Fargher 1992"

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
N/A	W. Shen and D. Norrie, "A Hybrid Agent-Oriented Infrastructure for Modeling Manufacturing Enterprises" (1998)	1998	1998	"Shen 1998"
N/A	K. Kouiss, H. Pierreval, and N. Mebarki, "Using Multi-Agent Architecture in FMS for Dynamic Scheduling," J. Intelligent Manufacturing, vol. 8, no. 1, 41–47 (Feb. 1997)	Feb. 1997	Feb. 1997	"Kouiss 1997"
N/A	S. Parthasarathy and S.H. Kim, "Manufacturing Systems: Parallel System Models and Some Theoretical Results," International Journal of Computer Applications in Technology, Vol. 3, No. 4, 225-238 (1990)	1990	1990	"Parthasarathy 1990"
N/A	R. Uzsoy, C. Lee, and L. Martin-Vega, "Models in the Semiconductor Industry Part I: System Characteristics, Performance Evaluation and Production Planning," IIE Transactions, 24:4, 47-60 (1992)	1992	1992	"Uzsoy 1992"
N/A	H. Fargher, et al., "A Planner and Scheduler for Semiconductor Manufacturing," IEEE Transactions on Semiconductor	May 1994	May 1994	"Fargher 1994"

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
	Manufacturing, Vol. 7, No. 2, 117-28 (May 1994)			
N/A	R. Leachman and D. Hodges, "Benchmarking Semiconductor Manufacturing" (2001)	May 1994	May 1994	"Leachman 1994"
N/A	J. Macher et al., "E-Business and Semiconductor Industry Value Chain: Implications for Vertical Specialization and Integrated Semiconductor Manufacturers," East-West Center Working Papers Economics Series No. 47 (May 2002)	May 2002	May 2002	"Macher 2002"
N/A	G. Tassey, "Standardization in Technology-Based Markets" (June 1999)	June 1999	June 1999	"Tassey 1999"
N/A	R. Langlois, "Capabilities and Vertical Disintegration in Process Technology: The Case of Semiconductor Fabrication Equipment" (January 1998)	January 1998	January 1998	"Langlois 1998"

b. Prior Art Systems/Services to The Asserted Claims of the '305 Patent.

System/Service	Relevant Dates	Persons/Entities Involved in Prior Use, Sale, or Offer for Sale[12]
AARIA	1998	Parunak et al 1998 ITI, U of Cincinnati
ABACUS	1998	McEleney et al 1998 UCB, UMIST
ADDYMS	1992	Butler & Ohtsubo 1992
AMACOIA	1996	Sprumont & Muller 1996 U. of Neuchatel
AMC	1998	Goldsmith & Interrrante 1998 Sandia Lab
ARMOSE	1994	Overgaard et al 1994 Odense U.
CAMPS	1998	Miyashita 1998
CORTES	1991	Sadeh & Fox 1989, Sycara et al 1991 CMU
DAS	1991	Burke & Prosser 1991 U. of Strathclyde
I-Control	1998	Brennan et al 1997, Wang et al 1998, U of Calgary
IFCF	1992	Lin and Solberg 1992 Purdue
LMS	1994	Fordyce & Sullivan 1994
MAPP	1998	Hayes 1998 U. of Minnesota
MASCADA	1998	Bruckner et al 1998 Daimler-Benz AG, KULeuven
MASCOT	1993	Parunak 1993 ITI
Reagere	1998	Berry & Kumura 1998 Penn State U.
Sensible Agents	1998	Barber et al 1998 U of Texas at Austin
SFA	1996	Parunak 1996 NCMS
YAMS	1987	Parunak 1987 ITI

[12] References further cited in Shen 1999.

System/Service	Relevant Dates	Persons/Entities Involved in Prior Use, Sale, or Offer for Sale[12]
Unknown	1991	Baker 1991 U. of Cincinnati
Unknown	1997	Choi and Park 1997
Unknown	1986	Duffie & Piper 1986 U. Wisconsin
Unknown	1994	Fischer 1994 DFKI
Unknown	1994	Hasegawa et al 1994 Toshiba
Unknown	1998	Interrante & Goldsmith 1998 Sandia Lab
Unknown	1995	Saad et al 1995 Vanderbilt
Unknown	1997	Kouiss et al 1997
Unknown	1995	Liu & Sycara 1994, 1995 CMU
Unknown	1997	Murthy et al 1997
Unknown	1998	Ouelhadj et al 1998 U. of Toulouse
Unknown	1997	Patriti et al 1997, Schaefer et al 1996 CRAN GGP
Unknown	1997	Sousa & Ramos 1997 ISEP/IPP
Unknown	1997	Tseng et al 1997 HKUST
Unknown	1989	Gupta et al Texas Instruments
Unknown	1992	Fargher and Smith 1992 Texas Instruments

2. Obviousness Combinations

To the extent that any one of the anticipation references is found not to disclose a limitation recited in the asserted claims from the ’305 patent, it would have been obvious to one of ordinary skill in the art at the time of the alleged invention of the ’305 patent either (i) to modify the reference to include this limitation and any remaining limitations of this claim and any claim(s) from which this claim depends, and/or (ii) to combine said reference with any other of the references in Exhibits B1-B22 or disclosed in the tables above, and/or (iii) modify, implement, or

combine the reference in view of (or with) a POSITA's general knowledge. Generally, motivation to combine any of these references with others exists within the references themselves, as well as within the knowledge of those of ordinary skill in the art at the relevant time. A person having ordinary skill in the art would have been motivated to combine any of the references described in attached Exhibits B1-B22 including, among the other reasons described below, because each of the references described in Exhibits B1-B22 pertain to methods employing scheduling agents in automated manufacturing environments. A person having ordinary skill in the art at the time of filing of the asserted patents would also have understood the references listed above, alone or in combination, to contain explicit and/or implicit teachings, suggestions, and/or rationales to combine them, including as further described below.

As non-limiting examples, the motivation to combine is provided in the nature of the problem allegedly solved by the '305 patent, the teachings of the cited prior art itself, and/or the knowledge of a person of ordinary skill in the art, as reflected in the background prior art, such as Dauzere-Peres, S. and J. Paulli, An integrated approach for modeling and solving the general multiprocessor job-shop scheduling problem using tabu search, *Annals of Operations Research* 70(1997) 281-306 and Dauzere-Peres, S., et. al., Multi-resource shop scheduling with resource flexibility, *European Journal of Operational Research* 107 (1998) 289-305.

For example, the identified combinations would have been combined or modified using: known methods to yield predictable results; common sense; known techniques in the same way; a simple substitution of one known, equivalent element for another to obtain predictable results; and/or a teaching, suggestion, or motivation in the prior art generally. In addition, it would have been obvious to try combining or modifying the identified prior art because there were only a finite number of predictable solutions and/or because known work in one field of endeavor prompted

variations based on predictable design incentives and/or because of market forces either in the same field or a different one. In addition, the combination of the prior art references would have been obvious because the combination represents known potential options with a reasonable expectation of success, and/or would be the product of routine experimentation. For example, a person of ordinary skill would have been aware that careful scheduling, and timely rescheduling based on operational events, are critical to the efficiency of an automated semiconductor fabrication facility like the system disclosed in Schulze. A person of ordinary skill seeking to enhance the efficiency of the Schulze system and reduce costs would have recognized that software-implemented dynamic scheduling was a way to leverage already present data gathering capabilities in order to enhance resource utilization and productivity and thus would have sought out an effective scheduling solution that would not create unacceptable delays or drain computational resources, yet was powerful enough to flexibly adapt to the manufacturing process. A person of skill in the art searching for such a solution would have recognized that the automated software scheduler disclosed in Gupta could do so without requiring significant alteration to the existing system.

Additional evidence that there would have been a motivation to combine or modify the prior art includes the interrelated teachings of multiple prior art references; the effects of demands known to the design community or present in the marketplace; the existence of a known problem for which there was an obvious solution encompassed by the asserted claims; the existence of a known need or problem in the relevant field of endeavor at the time of the alleged invention(s); and the background knowledge, skill, or creativity that would have been possessed by a person of ordinary skill in the art. Defendant may rely on uncited portions of the prior art references cited and produced, other publications and testimony, and the testimony of experts to establish that a

person of ordinary skill in the art would have been motivated to modify or combine certain of the cited references so as to render the claims obvious.

For example, to the extent that any of the references charted in these Preliminary Invalidity Contentions does not disclose "notifying" wherein "an indication of the occurrence" is sent to a publisher, the publisher publishes "the occurrence from the publisher to a subscribing listener," which then calls "the software scheduling agent," ('305 patent, cl. 8), the '305 patent admits that "the use of publishers and subscribers via listeners and notifiers in this manner is known to the art." '305 patent at 8:36-38. The prior art listed above also suggests that any of the charted references may be combined with or modified to incorporate publishers or subscribing listeners. For example, it would have been obvious to combine any of the charted references with, for example, Schulze, Yoshizawa, Jevtic, Arackaparambil, or Shen 1999. As detailed in Exhibit B9, Schulze discloses sending an indication of the occurrence to a "publisher" (*e.g.*, Schulze's "system bus"). *See e.g.*, Schulze at 6:49-8:19; FIGS. 1-2. Schulze also discloses publishing the occurrence from the publisher to a "subscribing listener" (*e.g.*, Schulze's "bus controller" in its first embodiment, and "software bridge" in its second embodiment). *See e.g.*, Schulze at 7:10-31; 7:62-8:12; FIGS. 1-2. Finally, Schulze discloses calling the software agent (*e.g.*, Schulze's "monitoring and assessment system") from the subscribing listener. *See e.g.*, Schulze at 7:10-31; 7:62-8:12; FIGS. 1-2. Likewise, as detailed in Exhibit B5, Yoshizawa discloses that "the host computing machine 46 displays results of scheduling in the display machine." Yoshizawa at 14:38-40. A POSITA would have understood that a standard host computing machine has both audio and video output and that the results of scheduling would have easily been published to listeners rather than displayed on a screen depending on the needs of the manufacturing environment. Similarly, as detailed in Exhibit B7, Jevtic discloses that a computer system executes the software routines for

scheduling. Jevtic at 5:32-34. This computer system "contains input/output circuitry 210 that forms an interface between conventional input/output (I/O) devices such as a keyboard, mouse, and display as well as an optional interface to a multi-cluster tool. The computer system 200 is a general-purpose computer that is programmed to perform wafer scheduling analysis in accordance with the present invention." *Id.* at 5:38-44. Further, as detailed in Exhibit B1, Arackaparambil discloses that the "FW and application SW elements are referred to as components because they are separate SW entities, each with its own database, server, and standard GUI. The components inter-operate through a public set of communication standards such as DCOM (MICROSOFT®—Microsoft is a registered trademark of Microsoft Corporation, Redmond, Wash.13 distribute common object model) APIs (application programming interface) or CORBA (common object request broker architecture)." Arackaparambil at 8:15-33. Arackaparambil further discloses a "[p]ublish and subscribe messaging building block for publish subscribe messaging," Arackaparambil at 10:7-8, and that "EVMC (event monitor component) monitors/subscribes to events published by DFS/F services. A DFS/F service can be executed (including launching a VWC job) when a monitored event occurs," Arackaparambil at 11:19-23. Likewise, as detailed in Exhibit B2, Shen 1999 also discloses developing agent based scheduling systems using CORBA (Shen 1999 at 145), and that "Facilitators, Brokers and Mediators" approaches can be used (Shen 1999 at 140). Each of the above examples address the same technical issues and teach similar solutions to similar problems in the same types of automated manufacturing environments discussed in the other charted references in Exhibit B, and a POSITA would have been motivated to use such teachings to enable notification of scheduling systems of occurrences in automated manufacturing environments.

As another example, to the extent that any of the references charted in these Preliminary Invalidity Contentions does not disclose the detection of the occurrence of the predetermined event, including "detecting an unplanned event or an unexpected event" ('305 patent, cl. 2), it would have been obvious to combine that reference with Schulze, Shen 1999, or Gupta. As detailed in Exhibit B9, Schulze discloses detecting an unplanned or unexpected event. *See e.g.*, Schulze at 11:51-55; 12:33-35; 12:51-53; 12:57-59; 13:15-17; 19:3-6. Furthermore, as detailed in Exhibit B2, Shen 1999 discloses that a "system may be asked to do additional tasks that were not anticipated" because "[c]ertain resources can become unavailable, and additional resources introduced." Shen 1999 at 133. As detailed in Exhibit B4, Gupta discloses detecting events such as "[b]roken machines [that] will tend to develop large queues until they are fixed." Gupta at 16:34-48. Each of the above examples address the same technical issues and teach similar solutions to similar problems in the same types of automated manufacturing environments discussed in the other charted references in Exhibit B, and a POSITA would have been motivated to use such teachings to handle unexpected or unplanned events in automated manufacturing environments.

A person of ordinary skill in the art at the time of the alleged invention would have combined the references because the prior art identified by Defendant addresses the same technical issues and suggests similar solutions to those discussed in the '305 patent and generally known at the time of the alleged invention. As demonstrated in Defendant's invalidity charts and explained above, a person of ordinary skill in the art would have been motivated to combine one or more of the disclosed references because they are related to similar methods and teach similar solutions to similar problems. The subject matter claimed in the asserted claims of the '305 patent involve nothing more than combining prior art elements according to known methods to yield predictable

results, and/or applying a known technique to a known method for improvement to yield predictable results. Thus, among other rationales, the motivation to combine the teachings of the prior art disclosed herein is found in the references themselves and in: (1) the nature of the problems being solved; (2) the express, implied, and inherent teachings of the prior art; (3) the knowledge of persons of ordinary skill in the art; (4) the fact that the prior art is generally directed towards the same problems; and/or (5) the predictable results obtained in combining the different elements of the prior art.

The combinations of references provided above are exemplary and are not intended to be exhaustive. Additional obviousness combinations of the references identified here are possible, and Defendant may rely on such combination(s) in this litigation. In particular, Defendant is currently unaware of Ocean's allegations with respect to the level of skill in the art and the qualifications of the typical person of ordinary skill in the art. Defendant is also unaware of the extent, if any, to which Ocean may contend that limitations of the claims at issue are not disclosed in the prior art identified by defendants as anticipatory, and the extent to which Ocean will contend that elements not disclosed in the asserted patent specifications would have been known to persons of skill in the art. And Defendant does not yet know how the Court will construe terms in the asserted claims. Defendant is also continuing its investigation of the large universe of prior art to identify potential prior art systems, publications related to those systems, and third parties that may have information about those systems. Ocean may also be in possession of prior art that Defendant may receive after discovery opens in this case. Defendant reserves the right to amend and supplement these contentions to identify other prior art and combinations rendering the asserted claims obvious.

c. The ’402 Patent

1. Identification of Prior Art

The tables below list prior art that anticipates and/or renders obvious one or more of the asserted claims. The attached claim charts in Exhibits C1-C12 demonstrate where each limitation of the claims is found in certain of the references listed below, either expressly or inherently in the larger context of the passage, as understood by a person having ordinary skill in the art. The following patents, publications, products and/or services are prior art under at least 35 U.S.C. §§ 102(a), (b), or (e).

a. Prior Art Patents and Patent Publications To The Asserted Claims of the ’402 Patent.

Exhibit	Reference	Filing/Priority Date	Date of Issue or Publication	Short Cite
C1	SEMI E81-0699 Provisional Specification for CIM Framework Domain Architecture	N/A	January 1999	“SEMI E81”
C2	U.S. Pat. No. 6,216,054	September 4, 1998	April 10, 2001	“Jang”
C3	U.S. Pat. No. 5,307,346	March 19, 1991	April 26, 1994	“Fieldhouse”
C4	U.S. Pat. No. 6,370,448	October 13, 1997	April 9, 2002	“Eryurek”
C5	U.S. Pat. No. 6,487,472	April 27, 1999	November 26, 2002	“Song”
C6	Sachs, et al., Process Control System for VLSI Fabrication	N/A	May 1991	“Sachs”
C7	U.S. Pat. No. 6,115,643	February 3, 1998	September 5, 2000	“Stine”
C8	EP 0 932 194	December 30, 1997	July 28, 1999	“Coronel ’194”
C9	SEMI E93-0200 Provisional Specification for CIM Framework	N/A	1999/2000	“SEMI E93”

Exhibit	Reference	Filing/Priority Date	Date of Issue or Publication	Short Cite
	Advanced Process Control Component			
	U.S. Pat. No. 5,479,340	September 20, 1993	December 26, 1995	"Fox"
	U.S. Pat. No. 5,805,816	May 12, 1992	September 8, 1998	"Picazo"
	U.S. Pat. No. 6,363,294	December 29, 1998	March 26, 2002	"Coronel '294"
	U.S. Pat. No. 6,197,116	August 29, 1997	March 6, 2001	"Kosugi"
	Japanese Patent Publication No. JPH5-181720	December 27, 1991	July 23, 1993	"Okubo"
	Japanese Patent Publication No. JP H8-202775	January 23, 1995	August 9, 1996	"Ito"
	Japanese Patent Publication No. JPH6-333791	May 25, 1993	December 2, 1994	"Miyatake"
	U.S. Patent No. 5,339,257	May 15, 1991	August 16, 1994	"Layden"
C10	U.S. Patent No. 6,564,268	May 17, 1999	May 13, 2003	"Davis"
C11	G. Barna, APC in the Semiconductor Industry, History and Near Term Prognosis	N/A	1996	"Barna"
C12	U.S. Pat. No. 5,754,451	February 29, 1996	May 19, 1998	"Williams"

b. Prior Art Systems/Services To The Asserted Claims of the '402 Patent

System/Service	Relevant Dates	Persons/Entities Involved in Prior Use, Sale, or Offers for Sale	Short Cite
ProcessWORKS APC; Jerry A. Stefani and Mike Anderson, Practical Issues in the Deployment of a Run-to-Run Control System in a Semiconductor Manufacturing Facility, Proc. SPIE 3742,	1999	Texas Instruments Adventa Control Technologies, Inc.	"Stefani"

System/Service	Relevant Dates	Persons/Entities Involved in Prior Use, Sale, or Offers for Sale	Short Cite
Process and Equipment Control in Microelectronic Manufacturing, 52-64 (April 23, 1999)			
SilverBox		Richard Mousties, CEO of Si Automation	"SilverBox"
Promis	1997	Promis Systems Sony Semiconductor of America	"Promis"

2. Obviousness Combinations

To the extent that any one of the anticipation references is found not to disclose a limitation recited in the asserted claims from the '402 Patent, it would have been obvious to one of ordinary skill in the art at the time of the alleged invention of the '402 Patent either (i) to modify the reference to include this limitation and any remaining limitations of this claim and any claim(s) from which this claim depends and/or (ii) to combine said reference with any other of the references in Exhibit C and/or with a POSITA's general knowledge. Generally, motivation to combine any of these references with others exists within the references themselves, as well as within the knowledge of those of ordinary skill in the art at the relevant time. A person having ordinary skill in the art would have been motivated to combine any of the references described in Exhibit C, including for the reasons described below. A person having ordinary skill in the art at the time of filing of the asserted patents would also have understood the references listed above, alone or in combination, to contain explicit and/or implicit teaching, suggestion, and/or rationales to combine them, including as further described below.

As non-limiting examples, the motivation to combine is provided in the nature of the problem allegedly solved by the '402 Patent, the teachings of the cited prior art itself, and/or the knowledge of a person of ordinary skill in the art, as reflected in the background prior art.

For example, the identified combinations would have been combined or modified using: known methods to yield predictable results; common sense; known techniques in the same way; a simple substitution of one known, equivalent element for another to obtain predictable results; and/or a teaching, suggestion, or motivation in the prior art generally. In addition, it would have been obvious to try combining or modifying the identified prior art because there were only a finite number of predictable solutions and/or because known work in one field of endeavor prompted variations based on predictable design incentives and/or because of market forces either in the same field or a different one. In addition, the combination of the prior art references would have been obvious because the combination represents known potential options with a reasonable expectation of success, and/or would be the product of routine experimentation.

Additional evidence that there would have been a motivation to combine or modify the prior art includes the interrelated teachings of multiple prior art references; the effects of demands known to the design community or present in the marketplace; the existence of a known problem for which there was an obvious solution encompassed by the asserted claims; the existence of a known need or problem in the relevant field of endeavor at the time of the alleged invention(s); and the background knowledge, skill, or creativity that would have been possessed by a person of ordinary skill in the art. Defendant may rely on uncited portions of the prior art references cited and produced, other publications and testimony, and the testimony of experts to establish that a person of ordinary skill in the art would have been motivated to modify or combine certain of the cited references so as to render the claims obvious.

As a preliminary matter, well before the '402 Patent, the semiconductor device fabrication field was already integrating multiple computer-driven tools and methods to implement process controls as evidenced in the Preliminary Invalidity Contentions. References described in Exhibits C-01 thorough C-08 and C-10 through C-12 disclose all limitations of claims 1-7. For example, SEMI E81 and Jang disclose all limitations of claim 1. *See, e.g.*, SEMI E81; Jang. Fieldhouse and Eryurek disclose interfaces for receiving tool state data and translation of one communication protocol into another. *See, e.g.*, Fieldhouse at 1:5-15 (disclosing interfacing a host computer to a field device), 1:37-46 (disclosing monitoring a field device and receiving data therefrom), 2:14-19 (disclosing a network field interface), 3:18-42 (disclosing a program module that uses a selected protocol program to map, or translate, a READ or WRITE service of a network communication protocol to a field device specific protocol); Eryurek at 2:53-57 (disclosing a process device coupled to a process communication device or interface), 3:26-35 (disclosing that the process device can send a process parameter and can control the process), 3:37-62 (disclosing translation between the Fieldbus protocol and the Ethernet protocol). Williams discloses receiving tool state data from a processing tool. *See, e.g.*, Williams at 2:52-3:9 (receiving data representing the state of a machine at an input/output card from a manufacturing equipment). Williams also discloses a fault detection tool. *See, e.g.*, Williams at 3:10-19 (disclosing that a preventive maintenance device can function as a diagnosis tool), 3:62-65 (disclosing that the preventive maintenance device can detect a fault in a part of a manufacturing equipment). Williams's preventive maintenance device can provide automatic warnings if a fault is detected. *See, e.g.*, Williams at 4:38-46.

A person of ordinary skill in the art would have been motivated to implement these systems and/or portions thereof, to defect faults within process tools to drive a reduction in costs by improving yield and/or to drive an increase in device quality. Design needs and market pressures,

which the ’402 Patent itself recognizes, provide ample reason to combine prior art elements in the manner recited in the claims. *See* ’402 Patent at 1:14-28.

The ’402 Patent also recognizes a known desire in communicating faults expeditiously in semiconductor manufacturing to avoid expending resources producing faulty processing pieces such as wafers. The prior art similarly recognizes this desire for efficiency and real-time monitoring, data analysis, and/or control. *See, e.g.*, Song at 12:46-50 (“Accordingly, by employing the diagnosis system of claim 14 of the present invention and comparing the monitored data, the fabrication systems’ operations can be tested, and as result of the data analysis, the abnormal systems can be detected, thereby increasing the processing efficiency.”), Stine at 7:31-46 (“A computerized method capable of identifying unacceptable levels of defects in work centers of a manufacturing process on a real time basis and initiating corrective action utilizing a plurality of interconnected, computerized work centers . . . .”), Coronel ’294 at 1:6-20 (“In a dedicated tool controlled by a computer, a method is developed which includes the steps of monitoring in realtime in-situ a plurality of process parameters . . . .”), Sachs at 136 (“For use by the run by run controller, the real time *in situ* measurements made during a run are summarized by the parameter extraction module. The run by run controller serves the multiple purposes of local optimization, feedback control, and feedforward control.”). To benefit from monitoring, analysis, and/or control of manufacturing processes of the references described in these Preliminary Invalidity Contentions, a person of ordinary skill in the art would have recognized that combining systems or portions thereof, such as providing memory components or data processing components to a system, simply involves implementing or adapting hardware and/or software to perform their known function.

For example, to the extent that any of the references charted in these Preliminary Invalidity Contentions does not explicitly disclose “a data collection unit” and/or “accumulating the state

data at the data collection unit" ('402 Patent, cl. 1), a person of ordinary skill in the art would have readily understood and appreciated that data and/or signals received at a communication interface would be stored in memory, as taught, for example, in Fox, Picazo, Coronel '294, or Layden. The claimed features were known in the prior art. *See, e.g.*, Fox at 3:26-32, 7:5-10 (disclosing storing wafer related RF data in data collection memory); Williams at 2:52-3:9, 5:3-24; Picazo at 31:22-31, 4:58-5:5 (disclosing a buffer for received data); Song at 7:30-31; Coronel '294 at 2:46-49, 8:24-30, 13:64-14:55 (disclosing a supervisor device/process that stores measurement data for immediate or subsequent processing); Okubo at ¶¶[0002], [0007]-[0009] (disclosing a database management system for storing data associated with a large scale integrated circuit manufacturing line); Ito at ¶¶[0007]-[0010] (disclosing analysis of successively collected data); Layden at 6:50-54. A person of ordinary skill in the art would have applied the known teachings in the prior art because, for example, it would have been predictable to use a memory or some other data storage to collect data. The purpose of memory or other data storage devices is to store data. It also would have been beneficial to store tool state data so that the information could have been used after its collection, including for fault detection or some other purpose. *See, e.g.*, Coronel '294 at 13:64-14:55.

A person of ordinary skill in the art would have also known that a communication interface can be implemented in hardware, software, or as a combination, and that the memory in which the received data is stored may be associated with the communication interface and/or with another system component. Therefore, a person of ordinary skill in the art would have understood the data collection unit to be integrated with the communication interface (e.g., when they share memory) or to be a separate unit, in some cases. A person of ordinary skill in the art would have also understood configuring the communication interface and the data collection unit as a single

component or as separate components to be nothing more than ordinary design choices. A person of ordinary skill in the art would have also understood that the different ordinary choices can beneficially improve the overall system, e.g., efficient use of the available memory in separate components or at a shared location, reduced complexity of components, and improved performance of communication interface.

Likewise, a person of ordinary skill in the art would have readily understood that when data is received at a communication interface according to one communication protocol and transmitted from a data collection unit according to a different communication protocol, the received data would be accumulated. A person of ordinary skill in the art would have known such accumulation to be beneficial, if not necessary, because, for example, the data reception and transmission rates can be different since the corresponding protocols are different. Even when the two rates are the same, data accumulation may be predictably beneficial or necessary because the conversion of the data from one format, corresponding to one protocol, into another format, corresponding to the other protocol, may take some time. A person of ordinary skill in the art would have also recognized other predictable benefits of accumulating the received data, such as preserving historical records of the performance of the processing tool from which the data is collected and performing subsequent batch processing of such data.

To a person of ordinary skill in the art, providing a separate data collection unit and accumulation of data would have been nothing more than a simple substitution of one known element (a data collection unit integrated with a communication interface) with another known element (a separate data collection unit). Alternatively, to a person of ordinary skill in the art, it would have been a simple combination of known elements – an interface disclosed in one reference described in Exhibit C and a data collection unit, where data is stored/accumulated, disclosed in

another reference described in Exhibit C. Additionally, a person of ordinary skill in the art would have recognized such a substitution or combination to improve a system disclosed in the references discussed in Exhibit C to achieve the predictable benefits discussed above. The above examples address the same technical issues and teach similar solutions to similar problems in the same types of automated manufacturing environments discussed in the other charted references in Exhibit C, and a POSITA would have been motivated to use such teachings to enable accumulating state data at a data collection unit.

To the extent that any of the references charted in these Preliminary Invalidity Contentions does not explicitly disclose "receiving at a first interface operational state data of a processing tool related to the manufacture of a processing piece" ('402 patent, cl. 1), it would have been obvious to combine that reference with, for example, SEMI E93, Picazo, Coronel '294, or Layden. The claimed features were known in the prior art. *See, e.g.*, SEMI E93 at 2; Williams at Abstract, 2:52-3:9, 5:42-48; Picazo at 1:19-30, 15:1-6, Figs. 7, 9; Song at 2:48-54, 8:5-7; Sachs at 136; Layden at 4:65-5:32. For example, Coronel '294 and SEMI E93 disclose receiving operational state data of a processing tool. *See, e.g.*, Coronel '294 at 2:13-25 (disclosing receiving wafer measurement data); SEMI E93 at 2 (disclosing a data collection plan for process machines). A person of ordinary skill in the art would have applied the known teachings in the prior art because, for example, receiving a tool's operational state data through an interface would have facilitated the predictable result of monitoring a tool's operation and allowing for adjustments to tool operation when needed. *See, e.g.*, SEMI E81 at 19, cols. 1-2; SEMI E93 at 2. Moreover, interfaces between system components were known to have the benefit of allowing integration of those components. *See, e.g.*, SEMI E81 at 11, col. 1; Fieldhouse at 2:14-19; Picazo at 15:1-6. The above examples address the same technical issues and teach similar solutions to similar problems in the same types of

automated manufacturing environments discussed in the other charted references in Exhibit C, and a POSITA would have been motivated to use such teachings to enable receiving operational state data of a processing tool at a first interface.

To the extent that any of the references charted in these Preliminary Invalidity Contentions does not explicitly disclose "sending the state data from the first interface to a fault detection unit" ('402 patent, cl. 1), it would have been obvious to combine that reference with, for example, Fox, SEMI E93, Picazo, Coronel '294, Miyatake, or Layden. The claimed features were known in the prior art. *See, e.g.*, Fox at 5:46-62 (disclosing a computer performing Hotelling's T^2 computations for process control / fault detection); SEMI E93 at 2; Williams at 3:45-55; Picazo at 37:31-34; Stine at 3:54-56; Coronel '294 at 10:21-46 (disclosing a supervisor device/process that determines semiconductor wafer state); Miyatake, ¶¶[0009]-[0011] (disclosing a cause analysis process); Layden at 5:33-6:3. A person of ordinary skill in the art would have applied the known teachings in the prior art because, for example, sending tool state data to a fault detection unit would have allowed for the predictable result of analyzing the data to ascertain whether the tool was experiencing faults. *See, e.g.*, Jang at 3:34-50 ("The PM controlling module 10 receives automatically, in real time, the operational parameter data from the respective equipment 3 through the equipment servers 4 (S10). The operational parameter data can be checked to determine if an equipment error is indicated (S15)."); Song, 7:61-8:4 ("Further, by installing the same algorithm as that of the diagnosis system 10 inside the personal computer, it is possible to monitor the fabrication process and the operation in the fabrication systems 1 to N at a remote area, see the results on a monitor, output an alarm signal when necessary, and control the process and the operation as well."). Further, a person of ordinary skill in the art would have applied the known teachings in the prior art to realize the benefits of detecting fault conditions. Detecting fault

conditions was beneficial because it allowed a system to correct those faults and prevent the fabrication of defective workpieces caused by tool operation outside of desired conditions. The above examples address the same technical issues and teach similar solutions to similar problems in the same types of automated manufacturing environments discussed in the other charted references in Exhibit C, and a POSITA would have been motivated to use such teachings to enable sending state data from the first interface to a fault detection unit.

To the extent that any of the references charted in these Preliminary Invalidity Contentions does not explicitly disclose "translating the state data from a first communications protocol to a second communications protocol compatible with the fault detection unit" ('402 patent, cl. 1), it would have been obvious to combine that reference with, for example, Fox or Picazo. The claimed features were known in the prior art. *See, e.g.*, Fox at 5:46-61; Williams at 3:7-10; Picazo at 6:58-7:32 (disclosing that segments on the opposite sides of a bridge may use different communication protocols), 7:62-67 (disclosing translation from a twisted-pair protocol to a coaxial cable protocol), 15:1-29 (disclosing a translating bridge translating between Token Ring and Ethernet protocols), 34:45-65 (disclosing translation between ATM/FDDI and regular Ethernet protocols); Sachs at 136. A person of ordinary skill in the art would have applied the known teachings in the prior art because, for example, communication protocols such as SECS II, GEM, ARAMS, RMS, and MMMS were well understood and widely used in the art and it would have been obvious to use them to obtain the predictable result of allowing for interaction between different system components. *See, e.g.*, SEMI E81 at 11, col. 1. In addition, translating between different protocols would have been beneficial to allow different system components to communicate even when they used separate communications protocols, increasing the skilled artisan's ability to choose components best suited to perform the claimed purposes (collecting operation state data and

determining if a fault condition exists) notwithstanding their use of distinct communication protocols. Picazo at 15:1-5 ("This type bridge provides network connection services to local area networks that employ different protocols at physical and data link layers."). The above examples address the same technical issues and teach similar solutions to similar problems in the same types of automated manufacturing environments discussed in the other charted references in Exhibit C, and a POSITA would have been motivated to use such teachings to enable translating the state data from a first communications protocol to a second communications protocol compatible with the fault detection unit.

To the extent that any of the references charted in these Preliminary Invalidity Contentions does not explicitly disclose "sending the translated state data from the data collection unit to the fault detection unit" ('402 patent, cl. 1), it would have been obvious to combine that reference with, for example, Fox, SEMI E93, Picazo, or Layden. The claimed features were known in the prior art. *See, e.g.*, Fox at 5:57-6:28, 7:5-8:4; SEMI E93 at 2; Williams at 3:10-20, 3:45-55, 3:62-65; Picazo at 31:22-31, 37:31-34; Layden at 5:33-6:3. A person of ordinary skill in the art would have applied the known teachings in the prior art because, for example, sending tool state data to a fault detection unit would have provided the predictable result and benefit of allowing for analysis of the state data to identify anomalies to avoid wasteful production of defective processing pieces. *See, e.g.*, SEMI E81 at 19, cols. 1-2. The above examples address the same technical issues and teach similar solutions to similar problems in the same types of automated manufacturing environments discussed in the other charted references in Exhibit C, and a POSITA would have been motivated to use such teachings to enable sending the translated state data from the data collection unit to the fault detection unit.

To the extent that any of the references charted in these Preliminary Invalidity Contentions does not explicitly disclose "determining if a fault condition exists with the processing tool based upon the state data received by the fault detection unit" ('402 patent, cl. 1), it would have been obvious to combine that reference with, for example, Fox, Coronel '294, or Layden. The claimed features were known in the prior art. *See, e.g.*, Williams at Abstract, 7:33-53; Song at 8:30-40; Stine at 7:31-46, Sachs at 141; Fox, 5:53-6:28 (disclosing detection of process faults by computing and comparing Hotelling's T^2 values); Coronel '294 at 9:63-10:15 (disclosing real-time transmission of measurement data to a supervisor device/process), 13:64-14:55 (disclosing that a supervisory process can detect a fault by analyzing variations in the received measurement data); Layden at 5:33-6:3, 6:55-7:6. A person of ordinary skill in the art would have applied the known teachings in the prior art because, for example, using a fault detection unit to determine whether a fault exists would have accomplished the foreseeable result of identifying tool faults. It would have been advantageous to identify tool faults so that a system could respond to those faults, including by taking corrective actions, as described below. Doing so would have corrected workpiece processing errors and avoided producing defective devices. The above examples address the same technical issues and teach similar solutions to similar problems in the same types of automated manufacturing environments discussed in the other charted references in Exhibit C, and a POSITA would have been motivated to use such teachings to enable determining if a fault condition exists based upon the state data received by the fault detection unit.

To the extent that any of the references charted in these Preliminary Invalidity Contentions does not explicitly disclose "performing a predetermined action on the processing tool in response to the presence of a fault condition" ('402 patent, cl. 1), it would have been obvious to combine that reference with, for example, Jang, Song, Fox Coronel '294, Ito, Miyatake, or Layden. The

claimed features were known in the prior art. Fox at 7:5-8:4; Williams at Abstract; Stine at 2:41-50; Sachs at 139; Coronel '294 at 10:50-11:16; Ito at ¶¶[0007]-[0010], ¶[0019]; Miyatake at ¶¶[0009]-[0011]; Layden at 6:15-26, 8:29-35. For example, Jang discloses "[a] method for controlling preventative maintenance cycles in a semiconductor fabrication system." Jang at Abstract. Jang further discloses that if the system "indicate[s] that an error has occurred," the system goes "into a preventative maintenance state." Jang at 3:41-45. Song teaches that the operator, in response to the presence of an alarm indicative of an abnormal condition, "controls the process and the operation in the fabrication systems." Song at 8:63-67. A person of ordinary skill in the art would have applied the known teachings in the prior art because, for example, reacting to a detected fault by performing a predetermined action would have provided the predictable result of allowing for a rapid response to the detected fault that would minimize wasteful production of defective processing pieces. Performing a predetermined action also would have been beneficial to correct faults without any need to determine a solution in real-time, avoiding unfavorable consequences flowing from the fault, such as defective processing pieces. Furthermore, implementing an automatic predetermined action would have "considerably increased efficiency" because it would have eliminated the need for comparatively time-consuming "intervention of the operators." *See, e.g.*, Jang at 3:28-41. The above examples address the same technical issues and teach similar solutions to similar problems in the same types of automated manufacturing environments discussed in the other charted references in Exhibit C, and a POSITA would have been motivated to use such teachings to enable performing a predetermined action on the processing tool in response to the presence of a fault condition.

To the extent that any of the references charted in these Preliminary Invalidity Contentions does not explicitly disclose "sending an alarm signal indicative of the fault condition to an

advanced process control framework from the fault detection unit providing that a fault condition of the processing tool was determined by the fault detection unit" ('402 patent, cl. 1), it would have been obvious to combine that reference with, for example, Coronel '294, Ito, or Layden. The claimed features were known in the prior art. *See, e.g.*, Williams at 3:62-65, 4:38-46, 7:33-53; Song, 8:35-40, Abstract; Stine at 5:58-6:17; Sachs at 141; Coronel '294 at 10:50-11:16; Ito at ¶¶[0007]-[0010], ¶[0019]; Layden at 6:27-49, 8:3-35. A person of ordinary skill in the art would have applied the known teachings in the prior art because, for example, sending an alarm signal to an advanced control framework would have achieved the predictable result and benefit of communicating information that a fault had been detected, allowing a process control system (advanced process control framework) to respond to the detection. *See, e.g.*, SEMI E81 at 20, cols. 1-2. The above examples address the same technical issues and teach similar solutions to similar problems in the same types of automated manufacturing environments discussed in the other charted references in Exhibit C, and a POSITA would have been motivated to use such teachings to enable sending an alarm signal indicative of the fault condition to an advanced process control framework.

To the extent that any of the references charted in these Preliminary Invalidity Contentions does not explicitly disclose "sending a signal by the framework to the first interface reflective of the predetermined action" ('402 patent, cl. 1), it would have been obvious to combine that reference with, for example, Coronel '294, Ito, or Miyatake. The claimed features were known in the prior art. *See, e.g.*, Stine at 5:66-6:27; Coronel '294 at 10:50-11:16; Ito at ¶¶[0007]-[0010]; Miyatake at ¶¶[0009]-[0011]. Likewise, these and other Combination References teach providing an alarm signal upon the detection of a fault. A person of ordinary skill in the art would have applied the known teachings in the prior art because, for example, sending a signal reflecting a

predetermined action via the first interface would have ensured the foreseeable result that the information relating to the action would reach the desired processing tool experiencing a fault. The interface would have been reliable because it was used to gather data relating to potential faults from the processing tool in the first place. The above examples address the same technical issues and teach similar solutions to similar problems in the same types of automated manufacturing environments discussed in the other charted references in Exhibit C, and a POSITA would have been motivated to use such teachings to enable sending a signal by the framework to the first interface reflective of the predetermined action.

To the extent that any of the references charted in these Preliminary Invalidity Contentions does not explicitly disclose "shutting down the processing tool providing that a faulty condition exists" ('402 patent, cl. 2), it would have been obvious to combine that reference with, for example, Fox, Coronel '294, Ito, Miyatake, or Layden. The claimed features were known in the prior art. *See, e.g.*, Williams at 4:65-5:2; Fox at 7:5-8:6 (disclosing and out-of-tolerance control signal that can, e.g., terminate a process in which a fault may have occurred); Coronel '294 at 10:50-11:16 (disclosing identification of abnormal situations and providing, in response, a defined action); Ito at ¶¶[0007]-[0010] (disclosing that if a measured value exceeds a control value, an alarm is generated or the lot is stopped); Miyatake at ¶¶[0009]-[0011] (disclosing stopping a lot upon detecting a fault); Layden at 6:21-26, 8:28-35. A person of ordinary skill in the art would have applied the known teachings in the prior art because, for example, shutting down a tool experiencing a fault would have led to the predictable result that the tool would cease to operate under faulty conditions. That approach had the benefit of stopping tool operations to avoid expending resources producing defective processing pieces such as wafers. The above examples address the same technical issues and teach similar solutions to similar problems in the same types

of automated manufacturing environments discussed in the other charted references in Exhibit C, and a POSITA would have been motivated to use such teachings to enable shutting down the processing tool providing that a faulty condition exists.

To the extent that any of the references charted in these Preliminary Invalidity Contentions does not explicitly disclose "receiving additional state data of the processing tool from a sensor that is coupled to the processing tool" ('402 patent, cl. 3), it would have been obvious to combine that reference with, for example, Fox, Coronel '294, Ito, or Layden. The claimed features were known in the prior art. *See, e.g.*, Williams at 2:62-3:3, 5:3-17; Fox at 2:46-47 (disclosing a sensor connected to a processing tool); Coronel '294 at 2:13-25 (disclosing etch end-point detection controllers, and receiving wafer thickness data therefrom), 10:50-11:16 (disclosing drift of process parameters from a normal situation to an abnormal situation), 13:64-14:55 (disclosing an analysis algorithm that can recognize a deviation from a normal process, and storing wafer history that may be used to detect process deviations); Ito at ¶¶[0007]-[0010] (disclosing automatically updating a quality control value using successively collected data); Layden at 5:3-9. A person of ordinary skill in the art would have applied the known teachings in the prior art because, for example, the use of sensors to monitor process conditions was well known in the art and allowed for the predictable result of detecting fault conditions to avoid expending resources producing faulty processing pieces such as wafers. Sensors provide a known and specific means for collecting fault detection data. Fox at 2:46-47 ("A sensor 15 is coupled to processing tool 10 in order to monitor a particular property resident within chamber 13."). The above examples address the same technical issues and teach similar solutions to similar problems in the same types of automated manufacturing environments discussed in the other charted references in Exhibit C, and a POSITA

would have been motivated to use such teachings to enable receiving additional state data of the processing tool from a sensor that is coupled to the processing tool.

To the extent that any of the references charted in these Preliminary Invalidity Contentions does not explicitly disclose "sending the additional state data to the fault detection unit" ('402 patent, cl. 3), it would have been obvious to combine that reference with known prior art for the same reasons described above relating to the limitation of claim 1 regarding sending state data to a fault detection unit.

To the extent that any of the references charted in these Preliminary Invalidity Contentions does not explicitly disclose "translating the state data from the sensor from a first communications protocol" ('402 patent, cl. 4), it would have been obvious to combine that reference with known prior art for the same reasons described above relating to the limitation of claim 1 regarding translating state data from a first communications protocol to a second communications protocol.

To the extent that any of the references charted in these Preliminary Invalidity Contentions does not explicitly disclose "comparing the state data received at the first interface to a predetermined state data at the fault detection unit" ('402 patent, cl. 5), it would have been obvious to combine that reference with, for example, Fox, Coronel '294, or Layden. The claimed features were known in the prior art. *See, e.g.*, Fox at 6:1-60; Williams at 4:25-37, 5:18-33, 7:33-53; Coronel '294 at 10:50-11:16; Layden at 6:62-7:6, 7:41-40. A person of ordinary skill in the art would have applied the known teachings in the prior art because, for example, comparing collected state data with predetermined state data would have provided for the predictable result of detecting when collected state data corresponded to a fault. This would have been the case when the predetermined state data reflected normal and expected tool operation. It also would have been obvious to perform the claimed comparison for the purpose of detecting a fault so that a system

could react to tool performance outside of normal and expected operation to avoid expending resources producing faulty processing pieces such as wafers. The above examples address the same technical issues and teach similar solutions to similar problems in the same types of automated manufacturing environments discussed in the other charted references in Exhibit C, and a POSITA would have been motivated to use such teachings to enable comparing the state data received at the first interface to a predetermined state data at the fault detection unit.

As another example, to the extent that any of the references charted in these Preliminary Invalidity Contentions does not explicitly disclose "comparing the state data received to fault model data that is derived from other similar-type wafers, where it was previously known that such wafers were processed within acceptable operational limits" ('402 patent, cl. 6), it would have been obvious to combine that reference with Kosugi. Kosugi discloses that "[t]he computing unit 44 substitutes measured values of electric signals sampled by the electric signal sampling unit 42 into the model expression stored in the model expression memory 48 to compute etching characteristics, such as an etching rate, etching uniformity, etc., and computes actual values of the etching characteristics, such as an etching rate, etching uniformity, etc., based on endpoint information supplied by the endpoint detector 46." Kosugi at 6:27-62, FIG. 2. Kosugi further discloses that "[t]he prediction/diagnosis/control unit 50 compares the predicted values and the actual values given by the computing unit 44 with each other to thereby predict and diagnose etching characteristics and a plasma condition and, based on a result of the comparison, make a feedback to following processing conditions." Kosugi at 6:27-62, FIG. 2; *see also* Fox at 6:1-60; Coronel '294 at 14:56-15:9 (disclosing the use of batch statistics); Ito at ¶¶[0007]-[0010] (disclosing automatically updating a quality control value using successively collected data).

A POSITA would have used the models disclosed in Kosugi to compare measurements (or other data) from "wafers [that] were processed within acceptable operational limits" to "state data." That comparison would have provided information about whether wafers being processed by a tool matched those processed under desired conditions, which indicates whether the tool is experiencing faults. Additionally, such a comparison would have been commonplace for a POSITA at the time the '402 Patent was filed. Further, the fault-related data generated by a comparison would have been useful for a system to identify and rectify fault conditions. *See, e.g.*, Kosugi at 6:27-62 ("The prediction/diagnosis/control unit 50 compares the predicted values andthe actual values given by the computing unit 44 with each other to thereby predict and diagnose etching characteristics and a plasma condition and, based on a result of the comparison, make a feedback to following processing conditions."). The above examples address the same technical issues and teach similar solutions to similar problems in the same types of automated manufacturing environments discussed in the other charted references in Exhibit C, and a POSITA would have been motivated to use such teachings to enable comparing the state data received to fault model data that is derived from other similar-type wafers.

To the extent that any of the references charted in these Preliminary Invalidity Contentions does not explicitly disclose "sending the accumulated state data from the data collection unit to the fault detection unit while a processing piece is being processed by the tool" ('402 patent, cl. 7), it would have been obvious to combine that reference with, for example, Kosugi, Fox, Coronel '294, Miyatake, or Layden. The claimed features were known in the prior art. *See, e.g.*, Fox at 6:30-40, 7:5-8:25 (disclosing real-time analysis of tool data for real-time feedback): Kosugi at 15:14-21 (disclosing real-time analysis of plasma condition in a processing chamber); Coronel '294 at 11:17-13:62 (disclosing that the supervisor device/process may receive data from a tool

and may perform real-time analysis); Miyatake, at ¶¶[0006]-[0007] (disclosing a real-time inspection process); Layden at Abstract. A person of ordinary skill in the art would have applied the known teachings in the prior art because, for example, the collection of tool state data during tool operation to process a workpiece provided the benefit of identifying potential faults in real time and allowing for prompt interruption of the manufacturing process to avoid wasteful production of defective processing pieces and correction of any faults that might be detected. *See, e.g.*, Kosugi at 15:14-21 ("When a practical wafer is processed, a plasma condition can be realtime seen. For example, every time one sheet of wafer is plasma processed, it can be automatically monitored whether or not the wafer is properly processed. In a case of a defective wafer, the processing is immediately stopped to investigate causes, or processing conditions are automatically or manually corrected to continue the processing"). The above examples address the same technical issues and teach similar solutions to similar problems in the same types of automated manufacturing environments discussed in the other charted references in Exhibit C, and a POSITA would have been motivated to use such teachings to enable sending accumulated state data from the data collection unit to the fault detection unit while a processing piece is being processed by the tool.

A person of ordinary skill in the art at the time of the alleged invention would have combined the references because the prior art identified by Defendant addresses the same technical issues and suggests similar solutions to those discussed in the '402 Patent and generally known at the time of the alleged invention. As demonstrated in Defendant's invalidity charts and explained above, a person of ordinary skill in the art would have been motivated to combine one or more of the disclosed references because they are related to similar methods and teach similar solutions to similar problems. The subject matter claimed in the asserted claims of the '402 Patent involve

nothing more than combining prior art elements according to known methods to yield predictable results, and/or applying a known technique to a known method for improvement to yield predictable results. Thus, among other rationales, the motivation to combine the teachings of the prior art disclosed herein is found in the references themselves and in: (1) the nature of the problems being solved; (2) the express, implied, and inherent teachings of the prior art; (3) the knowledge of persons of ordinary skill in the art; (4) the fact that the prior art is generally directed towards the same problems; and/or (5) the predictable results obtained in combining the different elements of the prior art.

Specifically, in light of the ordinary design choices and/or predicable benefits of employing a data collection unit integrated with or separately from a communication interface, accumulating the collected data, using sensors, using models in fault detection, providing an alarm when a fault is detected, etc., a person of ordinary skill in the art would have understood each of the references charted in these Preliminary Invalidity Contentions to disclose these features. Moreover, various other references, including those charted in Exhibit C9, e.g., Kosugi, Fox, and SEMI E93, disclose these limitations.

A person of ordinary skill in the art would have also understood that well-known system design and configuration techniques, such as providing memory for data storage, managing incoming and outgoing data pipes, etc., can be used to implement the substitution and/or combination described above. Moreover, a person of ordinary skill in the art would have recognized that the above-described modifications and/or combinations would not adversely affect the functionality of any of the references discussed in Exhibit C. Therefore, a person of ordinary skill in the art would have understood these combinations to have at least a reasonable expectation

of success. At least for these reasons, a person of ordinary skill in the art would have been motivated to combine references discloses in Exhibit C with each other.

The combinations of references provided above are exemplary and are not intended to be exhaustive. Additional obviousness combinations of the references identified here are possible, and Defendant may rely on such combination(s) in this litigation. In particular, Defendant is currently unaware of Ocean's allegations with respect to the level of skill in the art and the qualifications of the typical person of ordinary skill in the art. Defendant is also unaware of the extent, if any, to which Ocean may contend that limitations of the claims at issue are not disclosed in the prior art identified by defendants as anticipatory, and the extent to which Ocean will contend that elements not disclosed in the asserted patent specifications would have been known to persons of skill in the art. And Defendant does not yet know how the Court will construe terms in the asserted claims. Defendant is also continuing its investigation of the large universe of prior art to identify potential prior art systems, publications related to those systems, and third parties that may have information about those systems. Ocean may also be in possession of prior art that Defendant may receive after discovery opens in this case. Defendant reserves the right to amend and supplement these contentions to identify other prior art and combinations rendering the asserted claims obvious.

d. The '248 Patent

1. Identification of Prior Art

The tables below list prior art that anticipates and/or renders obvious one or more of the asserted claims. The attached claim charts in Exhibits D1-D22 demonstrate where each limitation of the claims is found in certain of the references listed below, either expressly or inherently in the larger context of the passage, as understood by a person having ordinary skill in the art. The

following patents, publications, products and/or services are prior art under at least 35 U.S.C. §§ 102(a), (b), or (e).

a. Prior Art Patents and Patent Publications To The Asserted Claims of the '248 Patent.

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
D1	U.S. Pat. No. 7,069,101	July 29, 1999	June 27, 200	"Arackaparambil"
D2	Weiming Shen and Douglas H. Norrie, "Agent-Based Systems for Intelligent Manufacturing: A State-of-the-Art Survey," Knowledge and Information Systems 1 (1999) 129-156	May 1, 1999	May 1, 1999	"Shen 1999"
D3	U.S. Pat. No. 7,072,731	April 3, 2001	July 4, 200	"Barto"
D4	U.S. Pat. No. 5,260,868	October 15, 1991	November 9, 1993	"Gupta"
D5	U.S. Pat. No. 5,442,561	May 10, 1993	August 15, 1995	"Yoshizawa"
D6	U.S. Pat. No. 6,418,350	June 9, 2000	July 9, 2002	"Hamidzadeh"
D7	U.S. Pat. No. 6,519,498	March 10, 2000	February 11, 2003	"Jevtic"
D8	Stefan A. Bussmannn, "Multi-Agent Approach to Dynamic, Adaptive Scheduling of Material Flow," Pre-Proceedings, Pre-Proceedings, MAAMAW-94, Odense, Denmark, August 1994	August 1994	August 1994	"Bussmann"

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
D9	U.S. Pat. No. 6,671,570	October 16, 2001	December 30, 2003	"Schulze"
D10	Fletcher, M. & S. Misbah Deen, "Fault-tolerant holonic manufacturing systems," Concurrency Computat.: Pract. Exper.: 2001; 13:43-70	January 2001	January 2001	"Fletcher"
D11	U.S. Pat. App. Pub. No. 2003/0139952	January 24, 2002	July 24, 2003	"Lubash"
D12	U.S. Pat. No. 6,470,227	December 2, 1998	October 22, 2002	"Rangachari"
D13	Richards, H.D., et al., "Manufacturing Systems: Flow of orders through a virtual enterprise their proactive planning and scheduling, and reactive control," Computing & Control Engineering Journal (Aug. 1997): 173-179	August 1997	August 1997	"Richards"
D14	Sauer, Jurgen, "Towards agent-based multi-site scheduling," Proc. of the 14th Workshop, New Results in Planning, Scheduling and Design (PuK2000), Berlin, 21-22 August 2000	August 2000	August 2000	"Sauer"
D15	Shen, W. and D. H. Norrie, "Dynamic manufacturing scheduling using both functional and resource related agents," Integrated Computer-	January 2001	January 2001	"Shen 2001"

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
	Aided Engineering 8 (2001) 17-30 (2001)			
D16	Shin, Y. et al., "Modeling and implementing a real time scheduler for dual-armed cluster tools," Computers in Industry 45 (2001) 13-27	May 2001	May 2001	"Shin"
D17	Sun, J., "An Intelligent Manufacturing System for Predictive Scheduling and Reactive Scheduling," Proc. of the 2000 ASME Des. Eng. Tech. Conf., September 10-13, 2000	September 2000	September 2000	"Sun"
D18	Japanese Unexamined Patent Application Publication No. 2000-308949	April 27, 1999	November 7, 2000	"Toba"
D19	Japanese Published Patent Publication JP-A-9-11092	June 20, 1995	January 14, 1997	"Morii"
D20	U.S. Pat. No. 5,757,648	September 12, 1996	May 26, 1998	"Nakamura"
D21	U.S. Pat. No. 6,757,578	June 22, 2000	June 29, 2004	"Jang"
D22	PCT Publication No. WO 00/34908	October 15, 1999	June 15, 2000	"Smirnov"
D23	U.S. Patent No. 4,796,194	August 20, 1986	January 3, 1989	"Atherton"
N/A	U.S. Pat. App. Pub. No. 2002/0156548	February 28, 2002	October 24, 2002	"Arackaprambil 2"
N/A	U.S. Pat. No. 4,888,692	November 10, 1988	December 19,1989	"Gupta 2"

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
N/A	PCT Publication WO 2000/034908	October 15, 1999	June 15, 2000	"Smirnov"
N/A	U.S. Pat. No. 4,796,194	August 20, 1986	January 3, 1989	"Atherton"
N/A	SEMI E105-0701	October 2000	October 2000	"SEMI E105-0701"
N/A	Japanese Published Patent Publication JP-A-9-19853	July 3, 1995	January 21, 1997	"Kobayashi"
N/A	U.S. Pat. No. 6,263,358	August 25, 1998	July 17, 2001	"Lee"
N/A	U.S. Pat. No. 6,889,178	October 1, 1997	May 3, 2005	"Chacon"
N/A	S. Dauzere-Peres, W. Roux, J.B. Lasserre, "Multi-resource shop scheduling with resource flexibility," European Journal of Operational Research Volume 107, Issue 2, 1 June 1998, Pages 289-305	June 1998	June 1998	"Dauzere-Peres 1998"
N/A	S. Dauzere-Peres, J. Paulli. "An integrated approach for modeling and solving the general multiprocessor job-shop scheduling problem using tabu search," Annals of Operations Research volume 70, pages281–306 (1997)	April 1997	April 1997	"Dauzere-Peres 1997"
N/A	Japanese Publication JPH08287140	April 12, 1995	November 1, 1996	"Mitsutake"
N/A	B.L. MacCarthy and J. Liu, "Addressing the Gap	1993	1993	"MacCarthy 1993"

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
	in Scheduling Research: A Review of Optimization and Heuristic Methods in Production Scheduling," Int. J. Prod. Pres., Vol. 31, No. 1, 59-79 (1993)			
N/A	W. Shen, L. Wang and Q. Hao, "Agent-based Distributed Manufacturing Process Planning and Scheduling: A State-of-the-art survey, "IEEE Transactions on Systems, Man, and Cybernetics, Part C (Applications and Reviews), vol. 36, no. 4, pp. 563-577 (July 2006)	July 2006	July 2006	"Shen 2006"
N/A	W. Shen, "Distributed manufacturing scheduling using intelligent agents," IEEE Intelligent Systems, vol. 17, no. 1, 88-94 (Jan.-Feb. 2002)	Jan.-Feb. 2002	Jan.-Feb. 2002	"Shen 2002"
N/A	M. Yamamoto and S. Y. Nof, "Scheduling/rescheduling in the manufacturing operating system environment," International Journal of Production Research, 23:4, 705-722 (1985)	1985	1985	"Yamamoto 1985"
N/A	J. Sun and D. Xue, "A Dynamic Reactive Scheduling Mechanism for Responding to	2001	2001	"Sun 2001"

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
	Changes of Production Orders and Manufacturing Resources," Computers in Industry, 189-207 (2001)			
N/A	J. McGehee, "The MMST Computer-Integrated Manufacturing System Framework," IEEE Transactions on Semiconductor Manufacturing, 7: 107-16 (1994)	1994	1994	"McGehee 1994"
N/A	P. Cowling and M. Johansson, "Using Real Time Information for Effective Dynamic Scheduling," European Journal of Operational Research 139, 230-244 (2002)	2002	2002	"Cowling 2002"
N/A	P. Diwan and D. Kothari, "Role of Automation and Robotics in Semiconductor Industry," IETE Technical Review, 7: 368-77 (1990)	1990	1990	"Diwan 1990"
N/A	N.R. Jennings and M. Wooldridge, "Applications of Intelligent Agents," Agent Technology, 3-28 (1998)	1998	1998	"Jennings 1998"
N/A	J.Y. Pan and J.M. Tenenbaum, "Toward an Intelligent Agent Flamework for Enterprise	1991	1991	"Pan 1991"

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
	Integration," AAAI (1991)			
N/A	H. Fargher and R. Smith, "Planning for the Semiconductor Manufacturer of the Future," AAAI (1992)	1992	1992	"Fargher 1992"
N/A	W. Shen and D. Norrie, "A Hybrid Agent-Oriented Infrastructure for Modeling Manufacturing Enterprises" (1998)	1998	1998	"Shen 1998"
N/A	K. Kouiss, H. Pierreval, and N. Mebarki, "Using Multi-Agent Architecture in FMS for Dynamic Scheduling," J. Intelligent Manufacturing, vol. 8, no. 1, 41–47 (Feb. 1997)	Feb. 1997	Feb. 1997	"Kouiss 1997"
N/A	S. Parthasarathy and S.H. Kim, "Manufacturing Systems: Parallel System Models and Some Theoretical Results," International Journal of Computer Applications in Technology, Vol. 3, No. 4, 225-238 (1990)	1990	1990	"Parthasarathy 1990"
N/A	R. Uzsoy, C. Lee, and L. Martin-Vega, "Models in the Semiconductor Industry Part I: System Characteristics, Performance Evaluation and Production Planning," IIE	1992	1992	"Uzsoy 1992"

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
	Transactions, 24:4, 47-60 (1992)			
N/A	H. Fargher, et al., "A Planner and Scheduler for Semiconductor Manufacturing," IEEE Transactions on Semiconductor Manufacturing, Vol. 7, No. 2, 117-28 (May 1994)	May 1994	May 1994	"Fargher 1994"
N/A	R. Leachman and D. Hodges, "Benchmarking Semiconductor Manufacturing" (2001)	May 1994	May 1994	"Leachman 1994"
N/A	J. Macher et al., "E-Business and Semiconductor Industry Value Chain: Implications for Vertical Specialization and Integrated Semiconductor Manufacturers," East-West Center Working Papers Economics Series No. 47 (May 2002)	May 2002	May 2002	"Macher 2002"
N/A	G. Tassey, "Standardization in Technology-Based Markets" (June 1999)	June 1999	June 1999	"Tassey 1999"
N/A	R. Langlois, "Capabilities and Vertical Disintegration in Process Technology: The Case of Semiconductor Fabrication Equipment" (January 1998)	January 1998	January 1998	"Langlois 1998"

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
N/A	U.S. Pat. No. 4,796,194	August 20, 1986	January 3, 1989	"Atherton"

b. Prior Art Systems/Services To The Asserted Claims of the '248 Patent.

System/Service	Relevant Dates	Persons/Entities Involved in Prior Use, Sale, or Offer for Sale[13]
AARIA	1998	Parunak et al 1998 ITI, U of Cincinnati
ABACUS	1998	McEleney et al 1998 UCB, UMIST
ADDYMS	1992	Butler & Ohtsubo 1992
AMACOIA	1996	Sprumont & Muller 1996 U. of Neuchatel
AMC	1998	Goldsmith & Interrrante 1998 Sandia Lab
ARMOSE	1994	Overgaard et al 1994 Odense U.
CAMPS	1998	Miyashita 1998
CORTES	1991	Sadeh & Fox 1989, Sycara et al 1991 CMU
DAS	1991	Burke & Prosser 1991 U. of Strathclyde
I-Control	1998	Brennan et al 1997, Wang et al 1998, U of Calgary
IFCF	1992	Lin and Solberg 1992 Purdue
LMS	1994	Fordyce & Sullivan 1994
MAPP	1998	Hayes 1998 U. of Minnesota
MASCADA	1998	Bruckner et al 1998 Daimler-Benz AG, KULeuven
MASCOT	1993	Parunak 1993 ITI
Reagere	1998	Berry & Kumura 1998 Penn State U.

[13] References further cited in Shen 1999.

System/Service	Relevant Dates	Persons/Entities Involved in Prior Use, Sale, or Offer for Sale[13]
Sensible Agents	1998	Barber et al 1998 U of Texas at Austin
SFA	1996	Parunak 1996 NCMS
YAMS	1987	Parunak 1987 ITI
Unknown	1991	Baker 1991 U. of Cincinnati
Unknown	1997	Choi and Park 1997
Unknown	1986	Duffie & Piper 1986 U. Wisconsin
Unknown	1994	Fischer 1994 DFKI
Unknown	1994	Hasegawa et al 1994 Toshiba
Unknown	1998	Interrante & Goldsmith 1998 Sandia Lab
Unknown	1995	Saad et al 1995 Vanderbilt
Unknown	1997	Kouiss et al 1997
Unknown	1995	Liu & Sycara 1994, 1995 CMU
Unknown	1997	Murthy et al 1997
Unknown	1998	Ouelhadj et al 1998 U. of Toulouse
Unknown	1997	Patriti et al 1997, Schaefer et al 1996 CRAN GGP
Unknown	1997	Sousa & Ramos 1997 ISEP/IPP
Unknown	1997	Tseng et al 1997 HKUST
Unknown	1989	Gupta et al Texas Instruments
Unknown	1992	Fargher and Smith 1992 Texas Instruments

2. Obviousness Combinations

A To the extent that any one of the anticipation references is found not to disclose a limitation recited in the asserted claims from the ’248 Patent, it would have been obvious to one of ordinary skill in the art at the time of the alleged invention of the ’248 Patent either (i) to modify

the reference to include this limitation and any remaining limitations of this claim and any claim(s) from which this claim depends, and/or (ii) to combine said reference with any other of the references in Exhibits D1-22 or disclosed in the tables above, and/or (iii) modify, implement, or combine the reference in view of (or with) a POSITA's general knowledge. Generally, motivation to combine any of these references with others exists within the references themselves, as well as within the knowledge of those of ordinary skill in the art at the relevant time. A person having ordinary skill in the art would have been motivated to combine any of the references described in attached Exhibits D1-D22 including, among the other reasons described below, because each of the references described in Exhibits D1-D22 pertain to methods employing scheduling agents in automated manufacturing environments. A person having ordinary skill in the art at the time of filing of the asserted patents would also have understood the references listed above, alone or in combination, to contain explicit and/or implicit teaching, suggestion, and/or rationales to combine them, including as further described below.

As non-limiting examples, the motivation to combine is provided in the nature of the problem allegedly solved by the '248 patent, the teachings of the cited prior art itself, and/or the knowledge of a person of ordinary skill in the art, as reflected in the background prior art, such as Dauzere-Peres, S. and J. Paulli, An integrated approach for modeling and solving the general multiprocessor job-shop scheduling problem using tabu search, *Annals of Operations Research* 70(1997) 281-306 and Dauzere-Peres, S., et. al., Multi-resource shop scheduling with resource flexibility, *European Journal of Operational Research* 107 (1998) 289-305. For example, the identified combinations would have been combined or modified using: known methods to yield predictable results; common sense; known techniques in the same way; a simple substitution of one known, equivalent element for another to obtain predictable results; and/or a teaching,

suggestion, or motivation in the prior art generally. In addition, it would have been obvious to try combining or modifying the identified prior art because there were only a finite number of predictable solutions and/or because known work in one field of endeavor prompted variations based on predictable design incentives and/or because of market forces either in the same field or a different one. In addition, the combination of the prior art references would have been obvious because the combination represents known potential options with a reasonable expectation of success, and/or would be the product of routine experimentation. For example, a person of ordinary skill would have been aware that careful scheduling, and timely rescheduling based on operational events, are critical to the efficiency of an automated semiconductor fabrication facility like the system disclosed in Schulze. A person of ordinary skill seeking to enhance the efficiency of the Schulze system and reduce costs would have recognized that software-implemented dynamic scheduling was a way to leverage already present data gathering capabilities in order to enhance resource utilization and productivity and thus would have sought out an effective scheduling solution that would not create unacceptable delays or drain computational resources, yet was powerful enough to flexibly adapt to the manufacturing process. A person of skill in the art searching for such a solution would have recognized that the automated software scheduler disclosed in Gupta could do so without requiring significant alteration to the existing system.

Additional evidence that there would have been a motivation to combine or modify the prior art includes the interrelated teachings of multiple prior art references; the effects of demands known to the design community or present in the marketplace; the existence of a known problem for which there was an obvious solution encompassed by the asserted claims; the existence of a known need or problem in the relevant field of endeavor at the time of the alleged invention(s); and the background knowledge, skill, or creativity that would have been possessed by a person of

ordinary skill in the art. Defendant may rely on uncited portions of the prior art references cited and produced, other publications and testimony, and the testimony of experts to establish that a person of ordinary skill in the art would have been motivated to modify or combine certain of the cited references so as to render the claims obvious.

For example, to the extent that any of the references charted in these Preliminary Invalidity Contentions does not disclose "notifying" wherein "an indication of the occurrence" is sent to a publisher, the publisher publishes "the occurrence from the publisher to a subscribing listener," which then calls "the software scheduling agent," ('248 patent, cl. 6), the '248 patent admits that "the use of publishers and subscribers via listeners and notifiers in this manner is known to the art." '248 Patent at 8:8-11. The prior art listed above also suggests that any of the charted references may be combined with or modified to incorporate publishers or subscribing listeners. For example, it would have been obvious to combine any of the charted references with Schulze, Yoshizawa, Jevtic, Arackaparambil, or Shen 1999. As detailed in Exhibit D9, Schulze discloses sending an indication of the occurrence to a "publisher" (*e.g.*, Schulze's "system bus"). *See e.g.*, Schulze at 6:49-8:19; FIGS. 1-2. Schulze also discloses publishing the occurrence from the publisher to a "subscribing listener" (*e.g.*, Schulze's "bus controller" in its first embodiment, and "software bridge" in its second embodiment). *See e.g.*, Schulze at 7:10-31; 7:62-8:12; FIGS. 1-2. Finally, Schulze discloses calling the software agent (*e.g.*, Schulze's "monitoring and assessment system") from the subscribing listener. *See e.g.*, Schulze at 7:10-31; 7:62-8:12; FIGS. 1-2. Likewise, as detailed in Exhibit D5, Yoshizawa discloses that "the host computing machine 46 displays results of scheduling in the display machine." Yoshizawa at 14:38-40. A POSITA would have understood that a standard host computing machine has both audio and video output and that the results of scheduling easily be published to listeners rather than displayed on a screen

depending on the needs of the manufacturing environment. Similarly, as detailed in Exhibit D7, Jevtic discloses that a computer system executes the software routines for scheduling. Jevtic at 5:32-34. This computer system "contains input/output circuitry 210 that forms an interface between conventional input/output (I/O) devices such as a keyboard, mouse, and display as well as an optional interface to a multi-cluster tool. The computer system 200 is a general-purpose computer that is programmed to perform wafer scheduling analysis in accordance with the present invention." *Id.* at 5:38-44. Further, as detailed in Exhibit D1, Arackaparambil discloses that the "FW and application SW elements are referred to as components because they are separate SW entities, each with its own database, server, and standard GUI. The components inter-operate through a public set of communication standards such as DCOM (MICROSOFT®—Microsoft is a registered trademark of Microsoft Corporation, Redmond, Wash.13 distribute common object model) APIs (application programming interface) or CORBA (common object request broker architecture)." Arackaparambil at 8:15-33. Arackaparambil further discloses a "Publish and subscribe messaging building block for publish subscribe messaging," Arackaparambil at 10:7-8, and that "EVMC (event monitor component) monitors/subscribes to events published by DFS/F services. A DFS/F service can be executed (including launching a VWC job) when a monitored event occurs," Arackaparambil at 11:19-23. Likewise, as detailed in Exhibit D2, Shen 1999 also discloses developing agent based scheduling systems using CORBA (Shenn 1999 at 145), and that "Facilitators, Brokers and Mediators" approaches can be used (Shen 1999 at 140). Each of the above examples address the same technical issues and teach similar solutions to similar problems in the same types of automated manufacturing environments discussed in the other charted references in Exhibit D, and a POSITA would have been motivated to use such teachings to notify scheduling systems of occurrences in automated manufacturing environments.

As another example, to the extent that any of the references charted in these Preliminary Invalidity Contentions does not disclose "detecting the occurrence of an alarm event," ('248 patent, cl. 12) it would have been obvious to combine that reference with Schulze, Shen 1999, Gupta, or Morii. As detailed in Exhibit D9, Schulze discloses detecting an occurrence of an alarm event. *See, e.g.*, Schulze at 7:31-42; 8:13-19; 8:65-9:9; 9:55-63; 15:49-58; 17:10-15; 18:17-28; FIB 10B. Furthermore, as detailed in Exhibit D2, Shen 1999 discloses that a "system may be asked to do additional tasks that were not anticipated" because "[c]ertain resources can become unavailable, and additional resources introduced." Shen 1999 at 133. As detailed in Exhibit D4, Gupta discloses detecting events such as "[b]roken machines [that] will tend to develop large queues until they are fixed." Gupta at 16:34-48. As detailed in Exhibit D19. Morii discloses an automated scheduling system that detects events and alarms. *See, e.g.*, Morii at ¶¶ 36, 41, 44, 45, 53, 54, 83. Each of the above examples address the same technical issues and teach similar solutions to similar problems in the same types of automated manufacturing environments discussed in the other charted references in Exhibit D, and a POSITA would have been motivated to use such teachings to handle alarm events in automated manufacturing environments.

As an additional example, to the extent that any of the references charted in these Preliminary Invalidity Contentions does not disclose the detection of the occurrence of the predetermined event, including "detecting an unplanned even tor an unexpected event" ('248 patent, cl. 2), it would have been obvious to combine that reference with Schulze. As detailed in Exhibit D9, Schulze discloses detecting an unplanned or unexpected event. *See e.g.*, Schulze at 11:51-55; 12:33-35; 12:51-53; 12:57-59; 13:15-17; 19:3-6. Each of the above examples address the same technical issues and teach similar solutions to similar problems in the same types of automated manufacturing environments discussed in the other charted references in Exhibit D, and

a POSITA would have been motivated to use such teachings to handle unexpected or unplanned events in automated manufacturing environments.

A person of ordinary skill in the art at the time of the alleged invention would have combined the references because the prior art identified by Defendant addresses the same technical issues and suggests similar solutions to those discussed in the '248 patent and generally known at the time of the alleged invention. As demonstrated in Defendant's invalidity charts and explained above, a person of ordinary skill in the art would have been motivated to combine one or more of the disclosed references because they are related to similar methods and teach similar solutions to similar problems. The subject matter claimed in the asserted claims of the '248 patent involve nothing more than combining prior art elements according to known methods to yield predictable results, and/or applying a known technique to a known method for improvement to yield predictable results. Thus, among other rationales, the motivation to combine the teachings of the prior art disclosed herein is found in the references themselves and in: (1) the nature of the problems being solved; (2) the express, implied, and inherent teachings of the prior art; (3) the knowledge of persons of ordinary skill in the art; (4) the fact that the prior art is generally directed towards the same problems; and/or (5) the predictable results obtained in combining the different elements of the prior art.

The combinations of references provided above are exemplary and are not intended to be exhaustive. Additional obviousness combinations of the references identified here are possible, and Defendant may rely on such combination(s) in this litigation. In particular, Defendant is currently unaware of Ocean's allegations with respect to the level of skill in the art and the qualifications of the typical person of ordinary skill in the art. Defendant is also unaware of the extent, if any, to which Ocean may contend that limitations of the claims at issue are not disclosed

in the prior art identified by defendants as anticipatory, and the extent to which Ocean will contend that elements not disclosed in the asserted patent specifications would have been known to persons of skill in the art. And Defendant does not yet know how the Court will construe terms in the asserted claims. Defendant is also continuing its investigation of the large universe of prior art to identify potential prior art systems, publications related to those systems, and third parties that may have information about those systems. Ocean may also be in possession of prior art that Defendant may receive after discovery opens in this case. Defendant reserves the right to amend and supplement these contentions to identify other prior art and combinations rendering the asserted claims obvious.

3. Obviousness-Type Double Patenting

Asserted claims 1-12 of the ’248 patent are invalid for obviousness type double patenting over at least claims 1-11 of the ’305 patent in view of the knowledge of a person of ordinary skill in the art and/or other references such as the references identified in Defendant’s invalidity contentions.

e. The ’538 Patent

1. Identification of Prior Art

The tables below list prior art that anticipates and/or renders obvious one or more of the asserted claims. The attached claim charts in Exhibits E1-E15 demonstrate where each limitation of the claims is found in certain of the references listed below, either expressly or inherently in the larger context of the passage, as understood by a person having ordinary skill in the art. The following patents, publications, products and/or services are prior art under at least 35 U.S.C. §§ 102(a), (b), or (e).

a. Prior Art Patents and Patent Publications To The Asserted Claims of the '538 Patent.

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
E1	Bode, Ko, and Edgar. "Run-to-run Control and Performance Monitoring of Overlay in Semiconductor Manufacturing,"	2002	2002	"Ko"
E2	U.S. Patent Pub. No. 2004/0159397	February 13, 2004	August 19, 2004	"Bode '397"
E3	U.S. Patent No. 7,198,964	February 3, 2004	April 3, 2007	"Cherry"
E4	U.S. Patent No. 5,910,011	May 12, 1997	June 8, 1999	"Cruse"
E5	U.S. Patent App. 2005/0252884	June 27, 2003	November 17, 2005	"Lam"
E6	U.S. Patent No. 6,912,439	Jun 8, 2004	November 4, 2004	"Mouli"
E7	U.S. Patent No. 6,915,177	September 30, 2002	April 1, 2004	"Phan"
E8	U.S. Patent No. 6,895,293	April 11, 2001	May 9, 2002	"Reiss"
E9	U.S. Patent No. 8,615,314	September 2, 2004	December 24, 2013	"Sonderman"
E10	U.S. Patent No. 6,410,351	July 13, 2000	June 25, 2002	"Bode '351"
E11	U.S. Patent App. Pub. No. 2006/0259198	May 26, 2006	November 16, 2006	"Brcka"
E12	Jonathan Tenner, "Optimisation of the Heat Treatment of Steel using Neural Networks," Thesis submitted to the Department of Automatic Control & Systems Engineering in partial fulfilment for the degree of Doctor of Philosophy, October 1999	October 1999	October 1999	"Tenner"
E13	Japan Patent No. 2000-252179	March 4, 1999	September 14, 2000	"Aida"

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
E14	Japan Published Patent Publication JPH-10-223499	February 6, 1997	August 21, 1998	"Anan"
E15	U.S. Patent No. 7,580,767	July 11, 2005	March 8, 2007	"MacDonald"
E15	U.S. Patent No. 7,337,091	October 31, 2002	February 26, 2008	"Markle"
E15	U.S. Patent No. 7,337,019	May 1, 2002	February 26, 2008	"Reiss II"
E15	U.S. Patent No. 6,564,119	July 20, 1999	February 3, 2000	"Vaculik"
E15	U.S. Patent No. 7,075,651	June 30, 2003	March 25, 2004	"Tsukakoshi"
E15	U.S. Patent Pub. No. U.S. 2005/0080572	March 25, 2004	April 14, 2005	"Lin"
E15	U.S. Patent No. 6,330,526	September 30, 1998	December 11, 2001	"Yasuda"
E15	U.S. Patent No. 6,625,785	April 19, 2001	June 13, 2002	"Chatterjee"
E15	U.S. Patent No. 6,778,873	July 31, 2002	August 17, 2004	"Wang"
E15	U.S. Patent No. 7,054,786	July 3, 2001	January 10, 2002	"Sakano"
E15	Japan Patent No. 2000-21854	June 30, 1998	January 21, 2000	"Yoshida"
E15	Yue et al., "Fault Detection of Plasma Etchers Using Optical Emission Spectra," IEEE TRANSACTIONS ON SEMICONDUCTOR MANUFACTURING, VOL. 13, NO. 3, AUGUST 2000	August 2000	August 2000	"Yue"
E15	Kano, Strauss, and Ohno, "Contribution Plots for Fault Identification Based on the Dissimilarity of Process Data," AIChE 2000 Annual Meeting, Los Angeles, CA, Nov. 15, Session 255	November 15, 2000	November 15, 2000	"Kano"

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
E15	Goodlin et al., "Simultaneous Fault Detection and Classification for Semiconductor Manufacturing Tools," Journal of The Electrochemical Society, May 12-17, 2002	May 12-17, 2002 or October 23, 2003	May 12-17, 2002 or October 23, 2003	"Goodlin"
E15	Nomikos and MacGregor, "Multivariate SPC Charts for Monitoring Batch Process," Technometrics, 37:1, 41-59.	February 1995	February 1995	"Nomikos"
E15	Guo, "A real-time equipment monitoring and fault detection system," 1998 Semiconductor Manufacturing Technology Workshop, IEEE	1998	1998	"Guo"
E15	Stanley et al., "Cost and revenue impact of advanced process control (APC) with an emphasis on run-to-run control (R2R)," Proc. SPIE 5044, Advanced Process Control and Automation, (1 July 2003)	July 1, 2003	July 1, 2003	"Stanley"
E15	PhD Thesis of Christopher Bode, "Run-to-Run Control of Overlay and Linewidth in Semiconductor Manufacturing," 2001	May 2001	May 2001	"Bode Thesis"
E15	PhD Dissertation of Jiangxin Wang, "Equipment and Process Modeling and Diagnostics in	Fall 2001	Fall 2001	"Wang Dissertation"

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
	Semiconductor Manufacturing"			
E15	Kourti and MacGregor, "Multivariate SPC Methods for Process and Product Monitoring," Journal of Quality Technology, 28:4, 409-428	1996	1996	"Kourti I"
E15	Yoon and MacGregor, "Statistical and Causal Model-Based Approaches to Fault Detection and Isolation," AiChE Journal Vol. 46, No. 9, September 2000	September 2000	September 2000	"Yoon"
E15	Kourti, Lee, and MacGregor, "Experiences with Industrial Applications of Projection Methods for Multivariate Statistical Process Control," Computers Chem. Engng Vol. 20. Suppl., pp. S745-S750, 1996	1996	1996	"Kourti II"
E15	Yang, Lu, Wang, and Ma, "A new fault detection and diagnosis method based on principal component analysis in multivariate continuous processes," Proceedings of the 4th World Congress on Intelligent Control and Automation June 10-14, 2002, Shanghai, P.R. China	June 10-14, 2002	June 10-14, 2002	"Yang"
E15	Yue and Qin, "Reconstruction-Based Fault Identification Using a Combined	August 30, 2001	August 30, 2001	"Yue II"

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
	Index," Ind. Eng. Chem. Res. 2001, 40, 4403-4414			
E15	Stich, Spoerre, and Velasco, "The Application of Artificial Neural Networks to Monitoring and Control of an Induction Hardening Process," Journal of Industrial Technology, Volume 16, Number 1 - November 1999 to January 2000	January 2000	January 2000	"Stich"
E15	T. Brozek et al., "Characterization Challenges and Solutions for FDSOI Technologies," 2019 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), 2019, pp. 1-3	14-17 Oct. 2019	14-17 Oct. 2019	"Brozek"
E15	Xiao, "Using the Modified Back-propagation Algorithm to Perform Automated Downlink Analysis," MIT Thesis	June 11, 1996	June 11, 1996	"Xiao"

b. Prior Art Systems/Services To The Asserted Claims of the '538 Patent.

System/Service	Relevant Dates	Persons/Entities Involved in Prior Use, Sale, or Offers for Sale	Short Cite
SilverBox		Richard Mousties, CEO of Si Automation	"SilverBox"
Maestria	2003	SI Automation and PDF Solutions	"Maestria"

System/Service	Relevant Dates	Persons/Entities Involved in Prior Use, Sale, or Offers for Sale	Short Cite
ModelWare RT	2001	Triant Technologies	"ModelWare"
Promis	1997	Promis Systems Sony Semiconductor of America	"Promis"

2. Obviousness Combinations

In *KSR International Co. v. Teleflex Inc.*, 550 U.S. 398 (2007), the United States Supreme Court clarified the standard for what types of inventions are patentable. The Supreme Court emphasized that inventions arising from ordinary innovation, ordinary skill, or common sense are not patentable. *Id.* at 415-27. In that regard, a patent claim may be obvious if the combination of elements was obvious to try or there existed at the time of the invention a known problem for which there was an obvious solution encompassed by the patent's claims. *Id*. at 417. In addition, when work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. *Id*. The Supreme Court recognized that if a person of ordinary skill can implement a predictable variation, Section 103 likely bars its patentability. *Id*.

All of the following rationales recognized in *KSR* support a finding of obviousness:

1. Combining prior art elements according to known methods to yield predictable results;
2. Simple substitution of one known element for another to obtain predictable results;
3. Use of known technique to improve similar devices (methods, or products) in the same way;

4. Applying a known technique to a known device (method, or product) ready for improvement to yield predictable results;

5. "Obvious to try"—choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;

6. Known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations would have been predictable to one of ordinary skill in the art; and

7. Some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

Certain of these rationales are discussed more specifically below. That others are not discussed more specifically should not be interpreted as an admission or concession that it does not apply. To the contrary, the discussion below simply provides more explanation of these specific rationales. Defendant may also rely on contemporaneous textbooks, treatises, and/or publications and/or on the testimony of fact and expert witnesses that bear on these rationales and on the reasons to combine the prior art.

Because the '538 Patent simply arranges old elements, with each performing the same function it had been known to perform, and yields no more than what one would expect from such an arrangement, the combinations of these old elements are obvious. Further, in the prior art there were well recognized design needs and market pressures to develop the alleged invention claimed in the '538 Patent.

Those of ordinary skill in the art would have been (and indeed were) motivated to combine known prior art solutions in the manner claimed in the '538 Patent. Design needs and market

pressures provided ample reason to combine prior art elements in the manner recited in the claims. Moreover, since there were a finite number of predictable solutions, a person of ordinary skill in the art had good reason to pursue the known options. The prior art used those familiar elements for their primary or well-known purposes in a manner well within the ordinary level of skill in the art. A person of ordinary skill in the art would thus have had a reasonable expectation that the combination would succeed in producing the invention as claimed.

To the extent that any one of the anticipation references is found not to disclose a limitation recited in the asserted claims from the '538 Patent, it would have been obvious to one of ordinary skill in the art at the time of the alleged invention of the '538 Patent either (i) to modify the reference to include this limitation and any remaining limitations of this claim and any claim(s) from which this claim depends and/or (ii) to combine said reference with any other of the references in Exhibits E1-E15 and/or with a POSITA's general knowledge. Generally, motivation to combine any of these references with others exists within the references themselves, as well as within the knowledge of those of ordinary skill in the art at the relevant time. A person having ordinary skill in the art would have been motivated to combine any of the references described in attached Exhibits E1-E15, including for the reasons described below. A person having ordinary skill in the art at the time of filing of the asserted patents would also have understood the references listed above, alone or in combination, to contain explicit and/or implicit teaching, suggestion, and/or rationales to combine them, including as further described below.

The alleged invention of the '538 Patent relates to fault detection through feedback operations in semiconductor manufacturing. Fault detection in semiconductor manufacturing was well known in the prior art before the alleged priority date of the '538 Patent. Semiconductor manufacturing has always been a complex process, involving hundreds or more processing steps

by the 1990s. Robert C. Leachman and David A. Hodges, Benchmarking Semiconductor manufacturing, IEEE Transactions on Semiconductor Manufacturing, 9: 158-69 (1996) at 158; John McGehee, The MMST Computer-Integrated Manufacturing System Framework, IEEE Transactions on Semiconductor Manufacturing, 7: 107-16 (1994) at 107. Semiconductor fabrication facilities ("fabs") are specially-designed factories that house the semiconductor manufacturing process tools in nearly particle-free environments. Robert C. Leachman and David A. Hodges, Benchmarking Semiconductor manufacturing, IEEE Transactions on Semiconductor Manufacturing, 9: 158-69 (1996) at 158; John McGehee, The MMST Computer-Integrated Manufacturing System Framework, IEEE Transactions on Semiconductor Manufacturing, 7: 107-16 (1994) at 107; Guo at 112; Gardner, et al., Equipment Fault Detection Using Spatial Signatures, IEEE Transactions on Components, Packaging, and Manufacturing Technology—Part C, 20: 295-304 (1997) at 295. Even decades ago, each fab cost hundreds of millions, if not billions, to construct. Robert C. Leachman and David A. Hodges, Benchmarking Semiconductor manufacturing, IEEE Transactions on Semiconductor Manufacturing, 9: 158-69 (1996) at 158; Gardner, et al., Equipment Fault Detection Using Spatial Signatures, IEEE Transactions on Components, Packaging, and Manufacturing Technology—Part C, 20: 295-304 (1997) at 295.

A fault at any semiconductor manufacturing step could lead to significant production losses. John McGehee, The MMST Computer-Integrated Manufacturing System Framework, IEEE Transactions on Semiconductor Manufacturing, 7: 107-16 (1994) at 107; Guo at 112. Therefore, systems were developed to assess the in-process data for most semiconductor operations. Fazel Famili, et al., Data Pre-Processing and Intelligent Data Analysis, Int'l J. on Intel. Data Analysis 1 (1997) at 16-17; U.S. Dep't. of Comm., Nat'l Bureau of Standards, Semiconductor Measurement Technology, NBS Special Pub. 400-36 (Jul. 1978). A fault during the

semiconductor manufacturing process may include an abnormal tool condition, such as when a parameter strays beyond its acceptable boundary. Int'l Org. for Standardization, ISO 13372:2004(E): Condition Monitoring and Diagnostics of Machines – Vocabulary (2004) at § 1.8. As was well known in the art, by detecting faults, a fab can avoid needlessly continuing to process faulty products and determine the step that is the source of the problem. Fazel Famili, et al., Data Pre-Processing and Intelligent Data Analysis, Int'l J. on Intel. Data Analysis 1 (1997) at 16; Guo at Abstract, 112.

By the 1990s, not only was it well known how to detect faults, but multivariate methods were used to diagnose detected faults, including principal component analysis ("PCA") and partial least squares ("PLS"), which "provide[d] a much greater capability for diagnosing assignable causes." J. F. Macgregor & T. Kourti, Statistical Process Control of Multivariate Processes, 3 Control Eng'g Prac. 403 (1995) at 404-07, 409. PCA variants were also developed and used in fault detection, such as recursive PCA and dynamic PCA. Wenfu Ku, Robert H. Storer, & Christos Georgakis, Disturbance Detection and Isolation by Dynamic Principal Component Analysis, 30 Chemometretrics & Intel. Lab. Sys. 179 (1995); Weihua Li, et al., Recursive PCA for Adaptive Process Monitoring, 10 J. Process Control 471 (2000). Real-time (in situ) data availability further allowed these analyses to provide feedback for real time control of processes. S. Joe Qin, et al., Control and Monitoring of Semiconductor Manufacturing Processes: Challenges and Opportunities, 37 IFAC Proceedings Volumes 125 (2004) at 125-26; Guo at 112; John Musacchio, et al., On the Utility of Run to Run Control in Semiconductor Manufacturing, IEEE International Symposium on Semiconductor Manufacturing Conference Proceedings, D-9–D-12 (1997) at D-9.

By the late 1990s, and well before the '538 patent, fault detection analyses were able to account for historical trends in fault detection data. *See* Taber H. Smith & Duane S. Boning,

Artificial Neural Network Exponentially Weighted Moving Average Controller for Semiconductor Processes, 15 J. Vacuum Sci. & Tech. 1377 (1997). More advanced analyses could also account for more complex correlations, such as asymmetric parameter tolerances, where the same deviation above a target value might lead to a greater likelihood of failure than the same deviation below the target value. W. L. Pearn, K.S. Chen, & G. H. Lin, A Generalization of Clements' Method for Non-Normal Pearsonian Processes with Asymmetric Tolerances, 16 Int'l J. Quality & Reliability Management 507 (1999) at 509-12, 518-20. More advanced fault detection analyses could also assess the severity of a fault, *e.g.*, critical, major, or minor. Guo at 118.

Before 2004, many different types of fault detection analyses were used to monitor processes, including neural networks and other types of machine learning. *E.g.*, Wen-Hui Chen, Chih-Wen Liu, & Men-Shen Tsai, On-Line Fault Diagnosis of Distribution Substations Using Hybrid Cause-Effect Network and Fuzzy Rule-Based Method, 15 IEEE Trans. on Power Delivery 710 (2000) at 710, Edward A. Reitman, Suresh H. Patel, & Earl R. Lory, Modeling and Control of Semiconductor Manufacturing Process with an Automata Network: An Example in Plasma Etch Processing, 23 Computers and Operations Rsch. 573 (1996). In neural networks, an input layer is mapped to an output layer using transfer functions and weight values, where these weight values represent the influence that an input layer node has upon an output layer node. Howard Demuth & Mark Beale, Neural Network Toolbox, Version 3.0 (4th prtg. 1997) at 1-2, 5-2, 5-7, 5-56. To "learn," neural networks adjust the weight values using a learning rule so that the network output matches a target output. Howard Demuth & Mark Beale, Neural Network Toolbox, Version 3.0 (4th prtg. 1997) at 3-11, 3-12. By 2004, many transfer functions and learning rules were common including, for example, Rectified Linear Unit (ReLU), Sigmoid, and hyperbolic tangent functions. Ludmila I. Kuncheva, Combining Pattern Classifiers: Methods and Algorithms (2004).

In sum, by the time the ’538 patent was filed, it was well known to perform fault detection in semiconductor manufacturing to assess in-process data, that such fault detection could use multivariate methods like PCA and PLS to diagnose detected faults, that such detection could be done in real time and provide feedback for real time process control of the semiconductor manufacturing process, that such fault detection could account for historical trends in the fault detection data, that such fault detection could also account for more complex correlations, such as asymmetric parameter tolerances, where the same deviation above a target value might lead to a greater likelihood of failure than the same deviation below the target value, that such fault detection could also assess the severity of a fault, *e.g.*, critical, major, or minor, and that such fault detection could use weighted analysis and machine learning. Given that all of the above was well known in the art before the ’538 patent, and persons of skill in the art would have known that any and/or all of these above techniques could be combined to create a fault detection system for use in semiconductor manufacturing system. Furthermore, this general background knowledge would have provided the basis for combining any number of known fault detection techniques to create different fault detection systems. Because all of these techniques were already known in the art for use in semiconductor manufacturing, a person of skill in the art would have understood that combining any/all of these techniques would have yielded predictable results, would have been a simple substitution of one known technique for another to obtain predictable results, would have used known techniques to improve similar techniques in the same way, would have applied a known technique to a known method that was ready for improvement to yield predictable results, would have been obvious to try because the techniques were all known and there was reasonable expectation of success in combining them, would have been obvious to try to improve semiconductor manufacturing accuracy to reduce production costs, and would have been obvious

because all techniques were already known and combined in various fashions before. With respect to the prior art references in Exhibits E1-E15, a person of ordinary skill in the art would have been motivated to combine any of the references identified as prior art to the '538 Patent for these reasons provided above, and the additional reasons provided below.

First, all of the prior art references identified as prior art to the '538 Patent teach similar fault detection techniques in semiconductor processing, were authored, designed, and developed during the same time period, and a person of ordinary skill in the art would have been motivated to apply the teachings of any one reference to any other reference because they would improve upon such a reference's teachings. For example, as outlined in further detail in the charts, the references all teach performing fault detection in a semiconductor process. *See, e.g.*, Lam at [0009] ("The present invention further advantageously provides a method for detecting a fault in a material processing system using a process performance prediction model."), Cherry at Abstract ("A method for identifying faults in a semiconductor fabrication process includes storing measurements for a plurality of parameters of a wafer in the semiconductor fabrication process. A first subset of the parameters is selected."), Brcka at [0002] ("The present invention relates to control systems, particularly to a system in a semiconductor processing facility designed to monitor performance, predict failures"), Ko at Abstract ("In the manufacture of semiconductor products, overlay is one of the most critical design specifications….In this research a process model and a run-to-run control scheme was developed for overlay control, based on linear model predictive control (LMPC), and successfully implemented in a commercial facility."), Bode '397 at Paragraph [0018] ("The photolithography stepper is configured to process wafers in accordance with an operating recipe. The overlay metrology tool is configured to measure overlay errors associated with the processing of the wafers in the photolithography stepper."), Cruse at Abstract

("A method and apparatus that provides process monitoring within a semiconductor wafer processing system using multiple process parameters. Specifically, the apparatus analyzes multiple process parameters and statistically correlates these parameters to detect a change in process characteristic…"), Mouli at Abstract ("The best-guess process flow is modeled using an inverse modeling technique."), Phan at 2:36-48 ("The present invention tailors Semiconductor fabrication processes according to process control parameters such as critical dimensions (CD), overlay, and defect."), Reiss at 2:34-38 ("Embodiments of the present invention relate to methods for fault detection of a semiconductor processing tool."), Sonderman at 4:45-48 ("Embodiments of the present invention provide for performing a qualitative analysis of an upstream process and making a feed-forward adjustment to a subsequent downstream process based upon the qualitative analysis."), Bode '351 at Abstract ("The process controller is adapted to store a thickness profile model of the deposition tool, generate predicted process layer thicknesses for the wafers not measured by the metrology tool based on the process layer thickness measurements of the wafers in the sample and the thickness profile model, and modify the operating recipe of the etch tool based on the predicted process layer thicknesses."), Aida [0004] ("by using a production control system (consisting of a production condition control, inspection result control, product progress control, facility history control, and production/quality monitoring subsystem) that correlates desired manufacturing processes and desired manufacturing facilities in a production line to prepare control standard data for each of them, collects product inspection data in the desired manufacturing processes and work data in the desired manufacturing facilities, evaluates the presence or absence of anomalies in the product quality or characteristics by comparing the collected product inspection data in the desired manufacturing processes with control standard data in the desired manufacturing facilities prepared in the relationship, evaluates the presence or

absence of abnormalities in the manufacturing facilities by comparing the collected work data in the desired manufacturing facilities with control standard data in the desired manufacturing facilities prepared in the relationship, and warns when the abnormalities are evaluated in each evaluation A system for producing a product by means of said production line is described"), Anan at [0006] ("the operation state and the processing state of the plurality of processing processes device are inspected, the article after processing is inspected, the inspection data is accumulated, the data processing is performed, and the processing state and the processing result by the plurality of processing processes device are compared. Based on this, the processing states of the plurality of processing processes device are managed so that the processing results of the articles by the plurality of processing processes device do not affect the subsequent processes in terms of quality control. In addition, when the defect processing occurs, the cause of the defect is identified and improved based on the result of the above comparison."). In addition, all the references teach some form of determining a relationship between a measured parameter and a detected fault; they all teach some form of adjusting the weighting of the parameter based on the determined relationship; and they all teach performing further fault detection based on the adjusted weighting. *See, e.g.*, Lam at [0054]-[0080], Ko at 393-397, Bode '397 at [0047]-[0049], Brcka at [0039]-[0045], Cherry at 8:15-9:64, Cruse at 4:53-5:30, Mouli at Mouli at 7:8-65, Phan at 6:25-7:44, Reiss at 7:14-8:1, Sonderman at 7:40-9:9, Bode '351 at 4:28-5:50, Aida at [0151]-[0155], Anan at [0017]-[0018]. Given these similarities, a person of ordinary skill in the art would have recognized the compatibility between the teachings of the prior art references. As explained above, it was common fault detection in semiconductor manufacturing to employ different fault detection and process control techniques, and a person of ordinary skill in the art would have regarded the combination of teachings from different references as typical in the field. Indeed, as also explained

above, it was common in the art of fault detection to use different comparisons and analysis methods to optimize the fault detection ability for the particular applications, processes, and metrology data being tested.

Second, and more specifically, a person of ordinary skill in the art would have been motivated and found it obvious to apply references teachings fault detection generally employing weighted analysis to other references also teaching fault detection employing weighted analysis, albeit in a different and/or more specific way (*i.e.*, determining if a fault was important or significant, adjusting weighting for parameters which were determined to be an important or significant fault, determining a relationship between pressure data, temperature data, humidity data, or gas flow rate data and a fault; using PCA as the fault detection analysis method; adjusting weighting associated with a parameter based upon a relationship of the parameter to a detected fault by increasing said weighting associated with said parameter based upon said relationship; adjusting weighting associated with a parameter based upon a relationship of the parameter to a detected fault by increasing said weighting associated with said parameter based upon said relationship and requiring a smaller fluctuation of said parameter during said fault detection analysis to determine that a fault occurred; or adjusting weighting associated with a parameter based upon a relationship of the parameter to a detected fault by increasing said weighting associated with said parameter based upon said relationship and requiring a larger fluctuation of said parameter during said fault detection analysis to determine that a fault occurred). *See, e.g.*, Lam at [0054]-[0080], Ko at 393-397, Bode '397 at [0047]-[0049], Brcka at [0039]-[0045], Cherry at 8:15-9:64, Cruse at 4:53-5:30, Mouli at Mouli at 7:8-65, Phan at 6:25-7:44, Reiss at 7:14-8:1, Sonderman at 7:40-9:9, Bode '351 at 4:28-5:50, Aida at [0151]-[0155], Anan at [0017]-[0018]. A person of ordinary skill in the art would have also been motivated and found it obvious to replace

and/or combine a reference's exact method of weighted fault detection with the teachings regarding other methods of weighted fault detection for all the reasons provided above and below.

These modifications would have been a simple substitution of one known element for another, which would have obtained predictable results because it was already well known in the art that multiple techniques of weighted fault detection could be used in semiconductor fabrication processes, and the exact technique would just depend on the specific criteria of fault detection needed for a given process. The substitution of one for the other would not have changed the principle of operation for either reference in any combination because the references all use similar mechanisms for a similar purpose: weighted fault detection for a semiconductor fabrication process. This is thus a combination of prior art elements (weighted fault detection) according to known methods (the exact weighted fault detection processes) to yield predictable results (a working fault detection process). A person of ordinary skill in the art would have been motivated to combine these teachings, and to make these replacements, because all of these weighted fault detection techniques were widely-used techniques. Accordingly, a person of ordinary skill in the art would have had a reasonable expectation of success given considerations discussed above, the similarities in the teachings and systems, and given that all the claimed weighted fault detection techniques were all well-known at the time. Implementing the combination and any necessary modifications would have been routine and within the scope of the prior art references' teachings.

As one specific example, to the extent that Ko does not disclose any of the limitations in the asserted claims, and particularly the claims/limitations related to determining a relationship between a detected fault and at least one of pressure data, temperature data, humidity data, or gas flow rate data associated with processing a workpiece, and performing a PCA, it would have been obvious to combine Ko with Lam and/or Cherry to teach said limitations. It would have been

obvious to a person of skill in the art to take the multi-variable fault detection techniques described in Ko and combine them with the multi-variable fault detection techniques described in Lam and/or Cherry, specifically, for example, Cherry and Lam's described techniques of determining a relationship between a detected fault and at least one of pressure data, temperature data, humidity data, or gas flow rate data associated with processing a workpiece and Cherry's described use of PCA, because all three references are directed to the same technology areas—fault detection in semiconductor manufacturing, including the use of multi-variable fault detection—and the combination/substitution of Lam's and/or Cherry's techniques with/for Ko's would have yielded predicted results of a more robust fault detection system. The combination of Ko, Lam and/or Cherry would have been well known and obvious to try because all three references taught well known techniques in fault detection in semiconductor manufacturing, and the combination of the three references would have simply created a more robust fault detection system, which would have been an obvious goal because it would have allowed for even an even better fault detection system, which could further lower errors in the semiconductor manufacturing process, which would ultimately decrease the cost of manufacture, which would be an obvious and common goal for a person of skill in the art.

As another specific example, to the extent that Bode '351 does not disclose any of the limitations in the asserted claims, and particularly the claims/limitations related to determining a relationship of a parameter to a detected fault by determining the importance or significance of a parameter relating to a detected fault, determining significant fault and adjusting the weighting of the fault if it is significant, it would have been obvious to combine Bode '351 with Lam to teach said limitations. It would have been obvious to a person of skill in the art to take the multi-variable fault detection techniques described in Bode '351 and combine them with the multi-variable fault

detection techniques described in Lam, specifically, for example, Lam's described techniques of determining a relationship of a parameter to a detected fault by determining the importance or significance of a parameter relating to a detected fault and Lam's described techniques of determining if a fault is a significant fault and adjusting the weighting of the fault if it is significant, because both references are directed to the same technology areas—fault detection in semiconductor manufacturing, including the use of multi-variable fault detection—and the combination/substitution of Lam's techniques with/for Bode '351's would have yielded predicted results of a more robust fault detection system. The combination of Bode '351 and Lam would have been well known and obvious to try because both references taught well known techniques in fault detection in semiconductor manufacturing, and the combination of the two references would have simply created a more robust fault detection system, which would have been an obvious goal because it would have allowed for even an even better fault detection system, which could further lower errors in the semiconductor manufacturing process, which would ultimately decrease the cost of manufacture, which would be an obvious and common goal for a person of skill in the art.

As another specific example, to the extent that Bode '351 does not disclose any of the limitations in the asserted claims, and particularly the claims/limitations related to determining a relationship of a parameter to a detected fault by determining the importance or significance of a parameter relating to a detected fault, determining significant fault and adjusting the weighting of the fault if it is significant, it would have been obvious to combine Bode '351 with Ko to teach said limitations. It would have been obvious to a person of skill in the art to take the multi-variable fault detection techniques described in Bode '351 and combine them with the multi-variable fault detection techniques described in Ko, specifically, for example, Ko's described techniques of

determining a relationship of a parameter to a detected fault by determining the importance or significance of a parameter relating to a detected fault and Ko's described techniques of determining if a fault is a significant fault and adjusting the weighting of the fault if it is significant, because both references are directed to the same technology areas—fault detection in semiconductor manufacturing, including the use of multi-variable fault detection—and the combination/substitution of Ko's techniques with/for Bode '351's would have yielded predicted results of a more robust fault detection system. The combination of Bode '351 and Ko would have been well known and obvious to try because both references taught well known techniques in fault detection in semiconductor manufacturing, and the combination of the two references would have simply created a more robust fault detection system, which would have been an obvious goal because it would have allowed for even an even better fault detection system, which could further lower errors in the semiconductor manufacturing process, which would ultimately decrease the cost of manufacture, which would be an obvious and common goal for a person of skill in the art.

As another specific example, to the extent that Aida does not disclose any of the limitations in the asserted claims, and particularly the claims/limitations related to performing a PCA, it would have been obvious to combine Aida with Cherry to teach said limitations. It would have been obvious to a person of skill in the art to take the multi-variable fault detection techniques described in Aida and combine them with the multi-variable fault detection techniques described in Cherry, specifically, for example, Cherry's described use of PCA, because both references are directed to the same technology areas—fault detection in semiconductor manufacturing, including the use of multi-variable fault detection—and the combination/substitution of Cherry's techniques with/for Aida's would have yielded predicted results of a more robust fault detection system. The combination of Aida and Cherry would have been well known and obvious to try because both

references taught well known techniques in fault detection in semiconductor manufacturing, and the combination of the two references would have simply created a more robust fault detection system, which would have been an obvious goal because it would have allowed for even an even better fault detection system, which could further lower errors in the semiconductor manufacturing process, which would ultimately decrease the cost of manufacture, which would be an obvious and common goal for a person of skill in the art.

As one specific example, to the extent that Brcka does not disclose any of the limitations in the asserted claims, it would have been obvious to combine Brcka with Lam and/or Cherry to teach said limitations. It would have been obvious to a person of skill in the art to take the multi-variable fault detection techniques described in Brcka and combine them with the multi-variable fault detection techniques described in Lam and/or Cherry because all three references are directed to the same technology areas—fault detection in semiconductor manufacturing, including the use of multi-variable fault detection—and the combination/substitution of Lam's and/or Cherry's techniques with/for Brcka's would have yielded predicted results of a more robust fault detection system. The combination of Brcka, Lam and/or Cherry would have been well known and obvious to try because all three references taught well known techniques in fault detection in semiconductor manufacturing, and the combination of the three references would have simply created a more robust fault detection system, which would have been an obvious goal because it would have allowed for even an even better fault detection system, which could further lower errors in the semiconductor manufacturing process, which would ultimately decrease the cost of manufacture, which would be an obvious and common goal for a person of skill in the art.

As another example, to the extent that any of the references charted in these Preliminary Invalidity Contentions does not disclose "performing in said computer said fault detection analysis

further comprises performing a principal component analysis (PCA) relating to said processing of said workpiece," ('538 patent, cl. 12) it would have been obvious to combine that reference with Cherry. Cherry discloses performing PCA in the fault detection analysis. Cherry at 4:64-5:14 ("As described in greater detail below, the fault monitor 140 employs a principal component analysis (PCA) technique to identify fault conditions with the manufactured devices."). A person of ordinary skill in the art at the time of the alleged invention would have combined Cherry and the reference because, as described above, the prior art identified by Defendant addresses the same technical issues and suggests similar solutions to those discussed in the '538 Patent and generally known at the time of the alleged invention. A person of ordinary skill in the art would have been motivated to combine Cherry and the reference because they are related to similar methods and teach similar solutions to similar problems, the subject matter claimed in the asserted claims of the '538 Patent involve nothing more than combining prior art elements according to known methods to yield predictable results, and/or applying a known technique to a known method for improvement to yield predictable result, and thus, among other rationales, the motivation to combine the teachings of Cherry and the reference is found in the references themselves and in: (1) the nature of the problems being solved; (2) the express, implied, and inherent teachings of the prior art; (3) the knowledge of persons of ordinary skill in the art; (4) the fact that the prior art is generally directed towards the same problems; and/or (5) the predictable results obtained in combining the different elements of the prior art.

As another example, to the extent that any of the references charted in these Preliminary Invalidity Contentions does not disclose "performing in said computer said fault detection analysis further comprises performing a principal component analysis (PCA) relating to said processing of said workpiece," ('538 patent, cl. 12) it would have been obvious to combine that reference with

Bode ’397. Bode ’397 discloses performing PCA in the fault detection analysis. Bode ’397 at [0052] (“The control model may be a relatively simple equation based model, as described above (e.g., linear, exponential, weighted average, etc.), or a more complex model, Such as a neural network model, principal component analysis (PCA) model, or a projection to latent structures (PLS) model.”). A person of ordinary skill in the art at the time of the alleged invention would have combined Bode ‘397 and the reference because, as described above, the prior art identified by Defendant addresses the same technical issues and suggests similar solutions to those discussed in the ’538 Patent and generally known at the time of the alleged invention. A person of ordinary skill in the art would have been motivated to combine Bode ‘397 and the reference because they are related to similar methods and teach similar solutions to similar problems, the subject matter claimed in the asserted claims of the ’538 Patent involve nothing more than combining prior art elements according to known methods to yield predictable results, and/or applying a known technique to a known method for improvement to yield predictable result, and thus, among other rationales, the motivation to combine the teachings of Bode ‘397 and the reference is found in the references themselves and in: (1) the nature of the problems being solved; (2) the express, implied, and inherent teachings of the prior art; (3) the knowledge of persons of ordinary skill in the art; (4) the fact that the prior art is generally directed towards the same problems; and/or (5) the predictable results obtained in combining the different elements of the prior art.

As another example, to the extent that any of the references charted in these Preliminary Invalidity Contentions does not disclose “performing in said computer said fault detection analysis further comprises performing a principal component analysis (PCA) relating to said processing of said workpiece,” (’538 patent, cl. 12) it would have been obvious to combine that reference with Bode ’351. Bode ’351 discloses performing PCA in the fault detection analysis. Bode ’351 at

5:29-38 ("Various modeling techniques, well known to those of ordinary skill in the art, are Suitable. Exemplary modeling techniques include neural network modeling, principal com ponent analysis (PCA), projection to latent structures (PLS), statistical response surface models (RSM), and first principle physics and chemistry-based models."). A person of ordinary skill in the art at the time of the alleged invention would have combined Bode '351 and the reference because, as described above, the prior art identified by Defendant addresses the same technical issues and suggests similar solutions to those discussed in the '538 Patent and generally known at the time of the alleged invention. A person of ordinary skill in the art would have been motivated to combine Bode '351 and the reference because they are related to similar methods and teach similar solutions to similar problems, the subject matter claimed in the asserted claims of the '538 Patent involve nothing more than combining prior art elements according to known methods to yield predictable results, and/or applying a known technique to a known method for improvement to yield predictable result, and thus, among other rationales, the motivation to combine the teachings of Bode '351 and the reference is found in the references themselves and in: (1) the nature of the problems being solved; (2) the express, implied, and inherent teachings of the prior art; (3) the knowledge of persons of ordinary skill in the art; (4) the fact that the prior art is generally directed towards the same problems; and/or (5) the predictable results obtained in combining the different elements of the prior art.

As another example, to the extent that any of the references charted in these Preliminary Invalidity Contentions does not disclose "performing in said computer said fault detection analysis further comprises performing a principal component analysis (PCA) relating to said processing of said workpiece," ('538 patent, cl. 12) it would have been obvious to combine that reference with Brecka. Brecka discloses performing PCA in the fault detection analysis. Brecka at [0032]-[0038]

("In such an approach, equipment operating parameters may be analyzed using some procedure, such as Principle Components Analysis (PCA), for finding relevant variables (components). This procedure may be used to analyze, for example, data collected during calibration and/or operation of the semiconductor processing equipment."). A person of ordinary skill in the art at the time of the alleged invention would have combined Brecka and the reference because, as described above, the prior art identified by Defendant addresses the same technical issues and suggests similar solutions to those discussed in the '538 Patent and generally known at the time of the alleged invention. A person of ordinary skill in the art would have been motivated to combine Brecka and the reference because they are related to similar methods and teach similar solutions to similar problems, the subject matter claimed in the asserted claims of the '538 Patent involve nothing more than combining prior art elements according to known methods to yield predictable results, and/or applying a known technique to a known method for improvement to yield predictable result, and thus, among other rationales, the motivation to combine the teachings of Brecka and the reference is found in the references themselves and in: (1) the nature of the problems being solved; (2) the express, implied, and inherent teachings of the prior art; (3) the knowledge of persons of ordinary skill in the art; (4) the fact that the prior art is generally directed towards the same problems; and/or (5) the predictable results obtained in combining the different elements of the prior art.

As another example, to the extent that any of the references charted in these Preliminary Invalidity Contentions does not disclose "wherein performing in said computer said principal component analysis further comprises utilizing a PCA model in said computer to perform said PCA, wherein said parameter is an input parameter to said PCA model," ('538 patent, cl. 13) it would have been obvious to combine that reference with Cherry. Cherry discloses performing

PCA in the fault detection analysis in a computer and where a parameter is an input parameter to the PCA model. Cherry at 4:64-5:14 ("As described in greater detail below, the fault monitor 140 employs a principal component analysis (PCA) technique to identify fault conditions with the manufactured devices."). A person of ordinary skill in the art at the time of the alleged invention would have combined Cherry and the reference because, as described above, the prior art identified by Defendant addresses the same technical issues and suggests similar solutions to those discussed in the '538 Patent and generally known at the time of the alleged invention. A person of ordinary skill in the art would have been motivated to combine Cherry and the reference because they are related to similar methods and teach similar solutions to similar problems, the subject matter claimed in the asserted claims of the '538 Patent involve nothing more than combining prior art elements according to known methods to yield predictable results, and/or applying a known technique to a known method for improvement to yield predictable result, and thus, among other rationales, the motivation to combine the teachings of Cherry and the reference is found in the references themselves and in: (1) the nature of the problems being solved; (2) the express, implied, and inherent teachings of the prior art; (3) the knowledge of persons of ordinary skill in the art; (4) the fact that the prior art is generally directed towards the same problems; and/or (5) the predictable results obtained in combining the different elements of the prior art.

As another example, to the extent that any of the references charted in these Preliminary Invalidity Contentions does not disclose "wherein performing in said computer said principal component analysis further comprises utilizing a PCA model in said computer to perform said PCA, wherein said parameter is an input parameter to said PCA model," ('538 patent, cl. 13) it would have been obvious to combine that reference with Bode '397. Bode '397 discloses performing PCA in the fault detection analysis in a computer and where a parameter is an input

parameter to the PCA model. Bode ’397 at [0052] (“The control model may be a relatively simple equation based model, as described above (e.g., linear, exponential, weighted average, etc.), or a more complex model, Such as a neural network model, principal component analysis (PCA) model, or a projection to latent structures (PLS) model.”). A person of ordinary skill in the art at the time of the alleged invention would have combined Bode ‘397 and the reference because, as described above, the prior art identified by Defendant addresses the same technical issues and suggests similar solutions to those discussed in the ’538 Patent and generally known at the time of the alleged invention. A person of ordinary skill in the art would have been motivated to combine Bode ‘397 and the reference because they are related to similar methods and teach similar solutions to similar problems, the subject matter claimed in the asserted claims of the ’538 Patent involve nothing more than combining prior art elements according to known methods to yield predictable results, and/or applying a known technique to a known method for improvement to yield predictable result, and thus, among other rationales, the motivation to combine the teachings of Bode ‘397 and the reference is found in the references themselves and in: (1) the nature of the problems being solved; (2) the express, implied, and inherent teachings of the prior art; (3) the knowledge of persons of ordinary skill in the art; (4) the fact that the prior art is generally directed towards the same problems; and/or (5) the predictable results obtained in combining the different elements of the prior art.

As another example, to the extent that any of the references charted in these Preliminary Invalidity Contentions does not disclose “wherein performing in said computer said principal component analysis further comprises utilizing a PCA model in said computer to perform said PCA, wherein said parameter is an input parameter to said PCA model,” (’538 patent, cl. 13) it would have been obvious to combine that reference with Bode ‘351. Bode ‘351 discloses

performing PCA in the fault detection analysis in a computer and where a parameter is an input parameter to the PCA model. Bode ’351 at 5:29-38 (“Various modeling techniques, well known to those of ordinary skill in the art, are Suitable. Exemplary modeling techniques include neural network modeling, principal com ponent analysis (PCA), projection to latent structures (PLS), statistical response surface models (RSM), and first principle physics and chemistry-based models.”). A person of ordinary skill in the art at the time of the alleged invention would have combined Bode ‘351 and the reference because, as described above, the prior art identified by Defendant addresses the same technical issues and suggests similar solutions to those discussed in the ’538 Patent and generally known at the time of the alleged invention. A person of ordinary skill in the art would have been motivated to combine Bode ‘351 and the reference because they are related to similar methods and teach similar solutions to similar problems, the subject matter claimed in the asserted claims of the ’538 Patent involve nothing more than combining prior art elements according to known methods to yield predictable results, and/or applying a known technique to a known method for improvement to yield predictable result, and thus, among other rationales, the motivation to combine the teachings of Bode ‘351 and the reference is found in the references themselves and in: (1) the nature of the problems being solved; (2) the express, implied, and inherent teachings of the prior art; (3) the knowledge of persons of ordinary skill in the art; (4) the fact that the prior art is generally directed towards the same problems; and/or (5) the predictable results obtained in combining the different elements of the prior art.

As another example, to the extent that any of the references charted in these Preliminary Invalidity Contentions does not disclose “wherein performing in said computer said principal component analysis further comprises utilizing a PCA model in said computer to perform said PCA, wherein said parameter is an input parameter to said PCA model,” (’538 patent, cl. 13) it

would have been obvious to combine that reference with Brecka. Brecka discloses performing PCA in the fault detection analysis in a computer and where a parameter is an input parameter to the PCA model. Brecka at [0032]-[0038] ("In such an approach, equipment operating parameters may be analyzed using some procedure, such as Principle Components Analysis (PCA), for finding relevant variables (components). This procedure may be used to analyze, for example, data collected during calibration and/or operation of the semiconductor processing equipment."). A person of ordinary skill in the art at the time of the alleged invention would have combined Brecka and the reference because, as described above, the prior art identified by Defendant addresses the same technical issues and suggests similar solutions to those discussed in the '538 Patent and generally known at the time of the alleged invention. A person of ordinary skill in the art would have been motivated to combine Brecka and the reference because they are related to similar methods and teach similar solutions to similar problems, the subject matter claimed in the asserted claims of the '538 Patent involve nothing more than combining prior art elements according to known methods to yield predictable results, and/or applying a known technique to a known method for improvement to yield predictable result, and thus, among other rationales, the motivation to combine the teachings of Brecka and the reference is found in the references themselves and in: (1) the nature of the problems being solved; (2) the express, implied, and inherent teachings of the prior art; (3) the knowledge of persons of ordinary skill in the art; (4) the fact that the prior art is generally directed towards the same problems; and/or (5) the predictable results obtained in combining the different elements of the prior art.

The citation to references and any combinations thereof provided above are exemplary and are not intended to be exhaustive. Additional obviousness combinations of the references identified here are possible, and Defendant may rely on such combination(s) in this litigation. In

particular, Defendant is currently unaware of Ocean's allegations with respect to the level of skill in the art and the qualifications of the typical person of ordinary skill in the art. Defendant is also unaware of the extent, if any, to which Ocean may contend that limitations of the claims at issue are not disclosed in the prior art identified by defendants as anticipatory, and the extent to which Ocean will contend that elements not disclosed in the asserted patent specifications would have been known to persons of skill in the art. And Defendant does not yet know how the Court will construe terms in the asserted claims. Defendant is also continuing its investigation of the large universe of prior art to identify potential prior art systems, publications related to those systems, and third parties that may have information about those systems. Ocean may also be in possession of prior art that Defendant may receive after discovery opens in this case. Defendant reserves the right to amend and supplement these contentions to identify other prior art and combinations rendering the asserted claims obvious.

f. The '330 Patent

1. Identification of Prior Art

The tables below list prior art that anticipates and/or renders obvious one or more of the asserted claims. The attached claim charts in Exhibits F1-F14 demonstrate where each limitation of the claims is found in certain of the references listed below, either expressly or inherently in the larger context of the passage, as understood by a person having ordinary skill in the art. The following patents, publications, products and/or services are prior art under at least 35 U.S.C. §§ 102(a), (b), or (e).

a. Prior Art Patents and Patent Publications To The Asserted Claims of the '330 Patent.

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
F1	U.S. Pat. No. 7,656,528	April 10, 2001	February 2, 2010	"Abdulhalim"
F2	U.S. Pat. No. 6,673,637	September 20, 2000	January 6, 2004	"Wack"
F3	U.S. Pat. Pub. App. No. 2002/0192577	June 15, 2001	December 19, 2002	"Fay"
F4	WO 01/97279	June 9, 2000	December 20, 2001	"Miller"
F5	U.S. Pat. No. 6,891,627	September 20, 2000	May 10, 2005	"Levy"
F6	U.S. Pat. No. 6,819,426	February 12, 2001	November 16, 2004	"Sezginer"
F7	U.S. Pat. No. 6,440,759	June 29, 2001	August 27, 2002	"Commons"
F8	U.S. Pat. No. 6,716,646	July 16, 2001	April 6, 2004	"Wright"
F9	U.S. Pat. No. 7,804,994	February 15, 2002	September 28, 2010	"Adel"
F10	U.S. Pat. Pub. App. No. 2002/0072001	May 4, 2000	June 13, 2002	"Brown"
F11	U.S. Pat. Pub. App. No. 2003/0160163	February 25, 2002	August 28, 2003	"Wong"
F12	U.S. Pat. No. 6,215,551	December 8, 1994	April 10, 2001	"Nikoonahad 551"
F13	U.S. Pat. No. 6,710,876	August 14, 2000	March 23, 2004	"Nikoonahad 876"
F14	U.S. Pat. No. 5,701,013	June 7, 1996	December 23, 1997	"Hsia"

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
	U.S. Pat. No. 6,407,396	June 24, 1999	June 18, 2002	"Mih"
	U.S. Pat. No. 6,699,624	February 27, 2001	March 2, 2004	"Niu"
	U.S. Pat. No. 7,280,230	December 19, 2001	October 9, 2007	"Shchegrov"
	U.S. Pat. Appl. No. 2002/0064718	February 25, 2000	May 30, 2002	"Honeycutt"
	US Pat. Publication 2003/0026471	June 27, 2001	Feb. 6, 2003	"Adel 471"
	Wolf et al., Silicon Processing for the VLSI Era, Volume 1: Process Technology, Lattice Press, 2000 (excerpt)	2000	2000	"Wolf"
	Bishop et al. Grating line shape characterization using scatterometry, Proc. SPIE 1545, International Conference on the Application and Theory of Periodic Structures, Oct. 1, 1991	Oct., 1991	Oct., 1991	"Bishop"
	1993 DARPA Final Report, Overlay and Grating Line Shape Metrology Using Optical Scatterometry (unclassified), unlimited release Nov. 20, 2001	Nov, 2001	Nov, 2001	"Darpa"

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
	Murnane et al., Scatterometry for 0.24-0.70 um developed photoresist metrology, Proc. SPIE 2439, Integrated Circuit Metrology, Inspection, and Process Control IX, May 22, 1995	May, 1995	May, 1995	"Murnane"
	Mori et al., Multi-batch Preparation of Standard Samples from a Single Doped Solution for Cross-Checking in Surface Metal Analyses of Silicon Wafers, Analytics Sciences, Vol. 16, Sept. 2000	Sept. 2000	Sept. 2000	"Mori"
	J. R. McNeil, et al., Scatterometry applied to microelectronic processing, Microlithography World 1(15), 1992	1992	1992	"McNeil"
	U.S. Pat. No. 6,429,943 to Opsal et al	March 29, 2000	August 6, 2002	"Opsal"
	Niu et al., "Specular Spectroscopic Scatterometry," IEEE Transactions on Semiconductor Manufacturing, Vol. 14, No. 2, May 2001	May 2001	May 2001	"Specular Spectroscopic"
	U.S. Pat. No. 6,458,605	June 28, 2001	October 1, 2002	"Stirton"

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
	US Pat. No. 6,388,253	June 29, 1999	May 14, 2002	"Su"
	US Pat. No. 6,304,999	October 23, 2000	October 16, 2001	"Toprac"
	Rangarajan, Optimal Sampling Strategies for sub-100-nm overlay, Proc. SPIE 3332, Metrology, Inspection, and Process Control for Microlithography XII, (8 June 1998)	June 1998	June 1998	"Rangarajan"
	US Pat. No. 6,427,093	Oct. 7, 1999	July 30, 2002	"Toprac 093"
	US Pat. No. 6,128,403	February 19, 1998	October 3, 2000	"Ozaki"
	US Pat. No. 6,278,957	January 24, 1994	August 21, 2001	"Yasuda"
	US Pat. No. 5,499,099	February 25, 1994	March 12, 1996	"Sato"
	US Pat. Appl. No. 2002/0042664	May 31, 2001	April 11, 2002	"Kikuchi"
	Japanese Unexamined Patent Publication No. 2000-156336	June 6, 2000	June 6, 2000	"Yasuda 336"
	US Pat. No. 5,498,877	Nov. 30, 1994	March 12, 1996	"Shiraki"
	Japanese Patent Publication No. JP H08-162392	December 8, 1994	June 21, 1996	"Kawakubo"
	US Patent Publication No. 2002/0183989	August 1, 2001	December 5, 2002	"Chien"

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
	US Patent Publication No. 2003/0002878	June 28, 2001	January 2, 2003	"Singh"

2. Obviousness Combinations

A person having ordinary skill in the art would have been motivated to combine any of the references described in attached Exhibits F1-F14, including for the reasons described below. A person having ordinary skill in the art at the time of filing of the asserted patents would also have understood the references listed above, alone or in combination, to contain explicit and/or implicit teaching, suggestion, and/or rationales to combine them, including as further described below.

Each of the references cited in F1-F14 is analogous art to the claimed invention of the '330 Patent: (1) each reference is from the same field of endeavor as the alleged invention (even if the reference addresses a different problem); and/or (2) each reference is reasonably pertinent to the problem faced by the named inventors of the '330 Patent (even if the reference is not in the same field of endeavor as the claimed invention). It therefore would have been obvious for someone of ordinary skill in the art to identify and combine elements from these references and devices.

No showing of a specific motivation to combine prior art is required to combine the references disclosed above and in the attached charts. The Supreme Court identified in *KSR International Co. v. Teleflex, Inc.*, 550 U.S. 398 (2007), a number of rationales that would support a finding that the Asserted Claims are obvious:

A. the Asserted Claims combine prior art elements according to known methods to yield predictable results;

B. the Asserted Claims involve the simple substitution of one known element for another to obtain predictable results;

C. the Asserted Claims involve the use of a known technique to improve similar devices (methods, or products) in the same way;

D. the Asserted Claims apply a known technique to a known device (method, or product) ready for improvement to yield predictable results;

E. the Asserted Claims involve combinations of prior art references that would have been "obvious to try"—i.e., a person of ordinary skill in the art could have reached the Asserted Claims by choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;

F. the Asserted Claims are simply variations of work from one field of endeavor or a different one that would have been prompted based on design incentives or other market forces because the variations were predictable to one of ordinary skill in the art.

KSR, 550 U.S. at 414-18 (rejecting Federal Circuit's "rigid" application of motivation-to-combine test, and instead espousing "expansive and flexible" approach); *see also* Examination Guidelines for Determining Obviousness Under 35 U.S.C. 103 in View of the Supreme Court Decision in *KSR International Co. v. Teleflex Inc.*, 72 Fed. Reg. 57,526 (Oct. 10, 2007). The Supreme Court has also held that a person of ordinary skill in the art is "a person of ordinary creativity, not an automaton," that a motivation to combine may be simply "common sense," and that "familiar items may have obvious uses beyond their primary purposes, and in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle." *KSR*, 550 U.S. at 420-21. The Supreme Court further held that it is sufficient that a combination of elements was "obvious to try," holding that, "[w]hen there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp." *Id.* at 421.

The '330 Patent itself recognizes that a drive for higher device densities in the semiconductor industry has demanded precise control of fabrication processes. '330 Patent, 1:5-33. The '330 Patent also recognizes two specific aspects that must be precisely controlled: (1) "[t]he dimensions of and between features [which] can be referred to as critical dimensions (CDs)"

and (2) the "precision in which features can be placed on a wafer" with respect to layer-to-layer alignment, such to avoid "layers [that] are not aligned within acceptable tolerances" referred to as "overlay errors." '330 Patent, 1:38-48. As a threshold matter, the asserted claims of the '330 Patent simply use conventional methods to perform these known measurements typically monitored during semiconductor fabrication processes—critical dimension and overlay—and apply conventional methods of process control.

For example, Claim 19 recites "**mapping the plurality of wafers into one or more logical grids** ...." To the extent Ocean argues that any of the references in charts F1-F14 do not alone disclose mapping the plurality of wafers into one or more logical grids, a person of ordinary skill in the art at the time of the '330 Patent's claimed invention would have found this element obvious in view of the prior art references, alone, or in combination with the knowledge of a person of ordinary skill in the art, or in combination with one or more of the other prior art references that disclose it. The step of mapping the plurality of wafers into one or more logical grids during a method for monitoring and controlling a fabrication process was well-known in the art as shown in charts F1 to F14. For example,

- *Wack* at 140:55-59: "For example, the data may be grouped across the specimen as a continuous function of radius, binned by radial range, binned by stepper field, by x-y position (or range of x-y positions, such as on a grid), by nearest die, and/or other suitable methods."

- *Brown* at [0060]: "The data gathered in accordance with the present invention may be analyzed, organized and displayed by any suitable means. For example, the data could be grouped across the wafer as a continuous function of radius, binned by radial range, binned by stepper field, by x-y position (or range of x-y positions, such as on a grid), by nearest die, and/or other suitable methods. The variation in data may be reported by standard deviation from a mean value, the range of values, and/or any other suitable statistical method."

- *Adel* at 2:31-41: "Each wafer in the lot is comprised of many exposure fields from the lithography processing tools (e.g. steppers, scanners, etc.). Within each exposure field can be typically 1 to many die. A die is the functional unit which

eventually becomes a single chip. On product wafers, overlay metrology marks are typically placed in the scribeline area (for example in the 4 corners of the field). This is a region that is typically free of circuitry around the perimeter of the exposure field (and outside the die). Sometimes overlay targets are placed in the streets, which are regions between the die but not at the perimeter of the field."

- *Stirton* at 5:61-6:5: "The structures 200, 220, 240 of FIGS. 2A-2C may be features formed in production devices, or alternatively, a test structure having the same general configuration as production features formed on the wafer 110 may be employed. The test structures, if employed, may be formed in a region of the wafer 110 not normally used for forming devices (e.g., in the periphery region where identification codes are typically scribed or in the scribe lines between production die). The wafer 110 may include multiple structures 200, 220, 240 having differing orientations for measuring the overlay error in different directions (e.g., X and Y)."

- *Nikoonahad* 551 at 8:61-9:2: "As shown in FIG. 6, at one instant in time, beam 38 illuminates an area 10 on surface 40. Area or spot 10 is divided into sixteen pixels by grid lines x1-x5, y1-y5. In this context, the term "pixel" is meaningful only in reference to the taking of data samples across the intensity distribution such as that in FIG. 1B and subsequent data processing and is borrowed from data sampling and processing in other technologies such as video technology. The pixel that is bounded by grid lines x2, x3 and y2, y3 is pixel P shown as a shaded area in FIG. 6."

- *Nikoonahad 876* at 1:14-18: "The alignment of the two overlay targets from two consecutive processes is measured for a number of locations on the wafer and the overlay error map across the wafer is analyzed to provide feedback for the alignment control of lithography steppers."

- *Rangarajan* at Abstract: "Overlay control is a critical requirement of the lithographic process... a number of different sampling plans that measure 25 points on a wafer were tested. ... We have identified several effective sampling patterns, and the improved performance of these plans is attributed to the fact that these patterns achieve greater coverage of the wafer and measure a larger number of wafer (or grid) points than the other sampling plans."

- *Su* at 7:55-7:62: "At step 490, the user maps field to field CD variations across a number of wafers prior to inspection using the present methodology. This is a standard process control technique practiced by virtually all wafer fabricators. It indicates which areas of the wafer typically have small CD variations from the design value, and which areas of the wafer typically have a large CD variation."

- *Ozaki* at 1:7-11: "The present invention relates to a wafer map analysis aid system and a wafer map analyzing method for analyzing various defects such as product failures caused in a semiconductor manufacturing process by using an image of a wafer map which is displayed on a monitor."

Semiconductor devices are fabricated on a wafer, which comprises a plurality of die. Die are typically formed on the wafer in a grid format. *See*, *e.g.*, *Adel* at Fig. 15 and production dies 326; *Wack* at FIG. 1 and a plurality of dies 12; *Honeycutt* at [0053], FIG. 19. A person of ordinary skill in the art would have had reason to map the plurality of wafers into one or more logical grids as part of a method for monitoring and controlling a semiconductor process. First, this is simply applying a known technique of a considering the wafer as a grid, just as implemented in the arrangement of die on the wafer. Second, the mapping of the plurality of wafers allows for designating the location of particular portions of a wafer for investigation and/or comparison of those portions within a wafer or across a set of wafers. For example, a person of ordinary skill in the art would appreciate the benefits of mapping a logical grid to aid in evaluating, comparing, and tracking data from different regions of a wafer to understand variations within that wafer. Within wafer variation is a critical metric of a semiconductor fabrication processes such as lithography processes. *See*, *e.g.*, *Brown* at [0009]; *Levy* at 139:35-41. Having a mapping of a logical grid allows for an easy reference to refer to the individual regions for comparison.

Claim 19 also recites "**concurrently measuring one or more critical dimensions and overlay in a wafer undergoing the fabrication process**." To the extent Ocean argues that any of the references in charts F1-F14 do not alone disclose concurrently measuring one or more critical dimensions and overlay alone, a person of ordinary skill in the art at the time of the '330 Patent's claimed invention would have found this element obvious in view of the prior art references, alone, or in combination with the knowledge of a person of ordinary skill in the art, or in combination with one or more of the other prior art references that disclose it. First, as discussed

above, the ’330 Patent itself admits that measuring critical dimensions and measuring overlay during semiconductor fabrication was common practice well before the ’330 Patent. Simply performing these known measurements *concurrently* is an obvious method for their performance, with a clear advantage of efficiencies. Second, concurrently measuring one or more critical dimensions and overlay was well-known in the art as shown in charts F1 to F14. For example,

- *Wack* at 41:46-50: “In addition, the system may be configured to determine a critical dimension and an overlay misregistration of a specimen sequentially or substantially simultaneously.”

- *Commons* at 3:50-55: “Another object of the present invention is to provide methods for combining the CD structure and overlay structure into a single feature during manufacturing of semiconductor devices to permit the CD and overlay measurements to be made in a single pass in the CD SEM.”

- *Sezginer* at 7:31-34: “The critical dimension (CD) and line profile also may be measured, simultaneously or with additional, similar measuring and data processing steps.”

- *Abdulhalim* at 2:16-18: “An advantage of the target is the use of the same diffraction system and the same target to measure critical dimension and overlay misregistration.”

- *Fay* at [0014]: “The meritorious effects of the invention include provision of an optical metrology technique which does not rely upon imaging of features for inspection, increased resolution and quantitative accuracy and repeatability which can be performed with apparatus of much reduced expense and complexity at greatly increased throughput, and simultaneous and non destructive overlay position and feature profile measurements.”

- *Levy* at 53:1-11: “In this manner, the system may be configured to determine a critical dimension of the specimen, an overlay misregistration of the specimen, and a presence, a number, a location, and/or a type of defects on one or more surfaces of the specimen sequentially or substantially simultaneously.”

- *Hsia* at Abstract : "[W]afer overlay and critical dimension disposition may be made simultaneously, reducing the need to perform multiple measurements at each testing step."

- *Wong* at [0101]: "The analysis will provide a result (925), which may include a result for the pitch of each periodic structure on the optical metrology target, the bias between periodic structures, the overlay registration between different layers in a multi-layer device, and also may provide information about the width of the features making up the periodic structure. In this process 900, the measurements of all of the periodic structures on the optical metrology target are obtained simultaneously."

- *Shchegrov* at 10:6-12: "The profile parameters can include, for example, CD, height, sidewall angle, parameters associated with polynomial expressions such as the coefficient a and height of quartic profiles, parameters of the bottom rounding and of the spacers, and the indices of refraction (n and k) parameters of materials of the line profile."

- *Mih* at Abstract: "A wafer metrology structure for measuring both critical dimension features of multiple patterns of a semiconductor device and overlay measurements of one pattern with respect to another. The measurements are readable by a single, one-dimensional scan of a metrology system."

- *Shiraki* at 5:12-20: "Therefore, alignment and size errors can be simultaneously measured in one step."

A person of ordinary skill in the art would have had good reason to pursue combining known measurement options, with the goal, for example, of reducing process time to meet demand for semiconductor devices, reducing equipment requirements, and/or achieving desired device structures. In addition to the clear efficiencies gained in throughput, one advantage is using the same hardware equipment for multiple optical measurements. *See*, *e.g.*, *Sezginer* at 7:10-22; *Abdulhalim*. at 5:57-6:3; *Hsia* at Abstract; *Mih* at 6:64-7:5; *Fay* at [0014]. Eliminating separate equipment would provide advantages in cost and space requirements. Another accessible advantage to implementing a concurrent measurement of critical dimensions and overlay is the elimination of a different grating structure, or different target features on a wafer, to measure each

parameter. *See*, *e.g.*, *Abdulhalim* at 5:57-6:3; *Adel* at 21:49-57. A person of ordinary skill in the art readily recognizes the value of the available real estate on a wafer and would appreciate a reduction in space dedicated to structures for measurement. The prior art explicitly summarizes these motivations for implementing concurrent measurements in semiconductor fabrication: "In this manner, such a system may be more cost, time, and space efficient ..." *Levy* at 41:48-51.

Claim 19 also recites "**a grating structure for use in concurrent measurements is formed**." The '330 Patent describes an embodiment of a grating structure in its Figure 2, which illustrates a structure having an underlying grating and an overlying grating, each represented as a series of rectangular features in cross-section. Such structures were known and used to measure critical dimensions and overlay as illustrated by references found in charts F1-F14. For example,

- *Abdulhalim* at 3:46-49: "FIG. 2 a is a cross-sectional view of a target 11 comprising two periodic structures 13, 15 on two layers 31, 33 of a device 17. The second periodic structure 15 is overlying or interlaced with the first periodic structure 13. The layers and the periodic structures may be at the same or different heights."

- *Wong* at Figure 7 discloses that "layer 701 is located on top of layer 702," where layer 701 has gratings 705A and 710A that, as shown in Figure 7, are "over" the underlying gratings 705B and 710B on the second layer

- *Fay* at [0030]: "FIG. 2 shows two levels 20, 22 of exemplary features in accordance with the present invention. In theory, any series of repeated shapes with intervening repeated shapes in another level could be used in accordance with the basic principles of the invention."

- *Sezginer* at 9:63-66: "Grating 30 is formed on the lower layer, i.e., at an earlier stage of fabrication. Grating 32 is subsequently formed on the upper layer, which needs to be well aligned laterally with the lower layer."

- *Niu* at 4:37-40: "FIGS. 5A-5D are process diagrams of various examples of adding one or more layers in a line-in-line overlay patterned grating."

- *Mih* at 5:51-5:59: "It should be understood that the cross section showing the first and second patterns formed, respectively, in the first and second levels of FIGS. 2A, 2B, and 2C, are exemplary only. In an alternative embodiment, the first pattern may be an unfilled trench formed within the substrate. In yet other alternate embodiments, either the first or second pattern may be formed within a permanent or temporary material formed above the substrate."

Applying any one of the grating structures of the prior art would have been obvious as it is merely applying a known structure to a similar device to perform is recognized function of providing target features for measurement(s) during semiconductor device fabrication. As discussed above, a person of ordinary skill in the art would recognize implementing a grating structure for use in concurrent measurement of critical dimensionss (CD) and overlay removes the need to provide a different grating structure, or different target features on a wafer, to measure each of critical dimensions and overlay. *See*, *e.g.*, *Abdulhalim* at 5:57-6:3; *Adel* at 21:49-57.

Asserted Claim 19 also includes steps of "**determining if one or more of the critical dimensions are outside of acceptable tolerances**," "**determining whether an overlay error is occurring**," "**developing control data based upon one or more concurrent measurements...**," and "**feeding forward or backward the control data to adjust one or more fabrication components or one or more operating parameters**..." To the extent Ocean argues that any of the references in charts F1-F14 do not alone disclose these elements, a person of ordinary skill in the art at the time of the '330 Patent's claimed invention would have found these elements obvious in view of the prior art references, alone, or in combination with the knowledge of a person of ordinary skill in the art, or in combination with one or more of the other prior art references that disclose it. These steps, culminating with the feeding forward or backward the control data, are typical process control steps of semiconductor fabrication at the time of the purported invention of the '330 Patent. For example,

- *Wolf* at 447: “There are two aspects of feature sizes that must be controlled in lithographic/ etching process: a) the absolute size of a minimum feature, including linewidth, spacing, or contact dimensions (also referred to as a critical dimension, or CD); and b) the variations of the minimum feature sizes as they cross steps on the wafer surface.”

- *Wack* at 72:42-51: “The method may also include generating an output signal if the determined properties of the specimen are outside of the predetermined range for the property... In addition, the output signal may be configured to indicate which of the determined properties is outside of the predetermined range and the extent to which the determined property is outside of the predetermined range.”

- *Darpa* at 4: “The development of critical dimension (CD) metrology techniques has become crucial as the CDs of semiconductor devices have shrunk toward 0.25μm. The tolerances of the fabrication process, or error budget, are approximately 10% of the CD.”

- *Mih* at 1:34-55 “For a pattern formed according to 0.25 μm design rules, for example, the overlay of one pattern with respect to a pattern formed in a previous level will be in the range of 0.025 μm. Overlay measurements are critical to semiconductor manufacturing.”

- *Wack* at 72:66—73:20: “the method may also include altering a parameter of an instrument coupled to a measurement device in response to at least one of the determined properties of the specimen using a feedback control technique. For example, if a property of the specimen is determined to be outside of a predetermined range, the method may include increasing a sampling frequency of a measurement device prior to determining at least two properties of additional specimens with the measurement device. … In an additional embodiment, the method may include altering a parameter of an instrument coupled to a measurement device in response to at least one of the determined properties of a specimen using a feedforward control technique.”

- *Abdulhalim* at 14:45-58: “Misalignment of overlying or interlaced periodic structures can be determined using the database in a preferred embodiment. ... The output signal 85 is compared with the database to determine the misalignment between the overlying or interlaced periodic structures. In another embodiment, misalignment of overlying or interlaced periodic structures is determined using the slope measurement technique.”

- *Abdulhalim* at 10:42-44: "The deposition tool uses the misalignment information to correct for any misalignment before providing another layer or periodic structure on wafer 91 in step 301."

- *Fay* at [0037]: "The optical spectroscopic reflectometry or ellipsometry sensor is very compact and can therefore be incorporated in a process tool such as a resist track developer to provide on-line metrology capability where it can provide direct feedback on the alignment system performance of the stepper. The same sensor could also be central to a standalone overlay metrology tool for in-line metrology applications."

- *Sezginer* at 1:42-44: "Overlay metrology provides the information that is necessary to correct the alignment of the stepper-scanner and thereby minimize overlay error on subsequent wafers."

- *Brown* at Abstract: "Methods and systems for evaluating and controlling a lithography process are provided. For example, a method for reducing within wafer variation of a critical metric of a lithography process may include measuring at least one property of a resist disposed upon a wafer during the lithography process. A critical metric of a lithography process may include, but may not be limited to, a critical dimension of a feature formed during the lithography process. The method may also include altering at least one parameter of a process module configured to perform a step of the lithography process to reduce within wafer variation of the critical metric. The parameter of the process module may be altered in response to at least the one measured property of the resist."

- *Shchegrov* at 1:22-28: "It is becoming increasingly important to have an accurate measurement of submicron linewidth and quantitative description of the profile of the etched structures on a pattern wafer at each process step. Furthermore, there is a growing need for wafer process monitoring and close-loop control such as focus-exposure control in photolithography."

- *Stirton* at 9:60-9:67: "Returning now to FIG. 1, after receiving the overlay error from the scatterometry tool 130, the controller 140 may take a variety of autonomous actions. The actions may include fault detection and/or process control functions. In one embodiment of the present invention, the controller 140 is adapted to modify the operating recipe of the photolithography tool 120 based on the overlay metric to control operations on subsequently processed wafers."

- *Toprac* at 3:54-58: In one embodiment, the computer system 130 sends control input signals on a line 120 to the first and second machine interfaces 115, 117. The

> computer system 130 employs a manufacturing model 140 to generate the control input signals on the line 120. In one embodiment, the manufacturing model contains a recipe that determines a plurality of control input parameters that are sent on the line 120.

- *Miller* at p. 2, lns. 20-25: "Error data is acquired by analyzing the acquired metrology data. A determination is made whether the error data merits modification to the processing of semiconductor devices. A feedback modification of the processing of semiconductor devices is performed in response to the determination that the error data merits modification to the processing of semiconductor devices. A feed-forward modification of the processing of the semiconductor devices is performed in response to the determination that the error data merits modification to the processing of semiconductor devices."

A person of ordinary skill in the art would have recognized that measurements such as critical dimensions and overlay have target values to effectuate the device to include its defined features. The purpose of measuring these dimensions, including as taught in the references of Exhibits F1-F14, is to determine if they are outside of tolerances. This is a common part of processing semiconductor wafers, and manufacturing in general. If measurements are out of tolerance, a person of ordinary skill in the art would be further motivated to make required adjustments in order to improve the performance of the manufacturing processes.

To the extent a reference does not explicitly discuss elements of determining control data and feeding forward or backward the control data to adjust one or more fabrication components or one or more operating parameters, a person of ordinary skill in the art at the time of the alleged invention would have combined the relevant teachings of references in Exhibits F1-F14 because implementing process control steps in a semiconductor fabrication process allows the fabrication process to run within its desired limits, beneficially impacting the quality and reliability of the fabricated devices. The manufacturing processes at the time of the purported invention of the '330 Patent included a large number of important steps that each required a number of inputs that should be fine-tuned to maintain proper manufacturing control. *See*, *e.g.*, *Miller* at 1, lns. 8-11. As

features sizes of semiconductor devices shrink, controlling the critical parameters has and continues to be increasingly important. *See*, *e.g.*, *Brown* at [0005]. Thus, a person of ordinary skill in the art would have recognized that process control steps, including such as provided by Advanced Process Control (APC) systems, were known processes suitable for implementation to advantageously drive a reduction in variabilities in processed semiconductor wafers. *See*, *e.g.*, *Miller* at 1-2; *Stirton* at 2:23-42; *Toprac* at 5:11-28.

Claims 20 and 21 recite, in part, the concurrent measurements are performed ***using scatterometry techniques***. As shown throughout numerous references discussed in Exhibits F1-F14, scatterometry techniques were well-known for measuring critical dimensions and overlay. *See*, *e.g.*, *Shchegrov* at 2:31-39; *Bishop* at 64; *Stirton* at 7:1-37; *Wack* at 3:2-42; *Miller* at p. 2, lns. 7-16; *Fay* at Abstract; *Wong* at [0006]; *Brown* at [0055]; *Sezginer* at 6:63-7:9. To the extent it is argued that any one of the references of F1-F14 do not explicitly discuss the use of scatterometry and/or discuss the use of other techniques (such as a scanning electron microscope (SEM), which is also discussed and claimed in the '330 Patent), a person of ordinary skill in the art would have found it obvious to implement scatterometry as a measurement technique. This is merely applying a known technique to perform a similar measurement on a similar device. Further, scatterometry has an advantage of being a "rapid, non-destructive, inexpensive, and potentially useful for on-line control during several microlithographic processing steps." *See Murnane* at 427; *see also*, *e.g., McNeil* at 16; *Stirton* at 7:38-8:29; *Specular Spectroscopic* at 97.

The citation to references and any combinations thereof provided above are exemplary and are not intended to be exhaustive. Additional obviousness combinations of the references identified here are possible, and Defendant may rely on such combination(s) in this litigation. In particular, Defendant is currently unaware of Ocean's allegations with respect to the level of skill

in the art and the qualifications of the typical person of ordinary skill in the art. Defendant is also unaware of the extent, if any, to which Ocean may contend that limitations of the claims at issue are not disclosed in the prior art identified by defendants as anticipatory, and the extent to which Ocean will contend that elements not disclosed in the asserted patent specifications would have been known to persons of skill in the art. And Defendant does not yet know how the Court will construe terms in the asserted claims. Defendant is also continuing its investigation of the large universe of prior art to identify potential prior art systems, publications related to those systems, and third parties that may have information about those systems. Ocean may also be in possession of prior art that Defendant may receive after discovery opens in this case. Defendant reserves the right to amend and supplement these contentions to identify other prior art and combinations rendering the asserted claims obvious.

g. The '691 Patent

1. Identification of Prior Art

The tables below list prior art that anticipates and/or renders obvious one or more of the asserted claims. The attached claim charts in Exhibits G01-G11 demonstrate where each limitation of the claims is found in certain of the references listed below, either expressly or inherently in the larger context of the passage, as understood by a person having ordinary skill in the art. The following patents, publications, products and/or services are prior art under at least 35 U.S.C. §§ 102(a), (b), or (e).

a. Prior Art Patents and Patent Publications To The Asserted Claims of the '691 Patent.

Corresponding Chart	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
G-01	6,061,640	October 31, 1996	May 9, 2000	"Tanaka"

Corresponding Chart	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
G-02	5,768,144	December 18, 1992	June 16, 1998	"Nagase"
G-03	2005/0047645	March 29, 2002	March 3, 2005	"Funk '465"
G-04	7,123,980	September 30, 2002	October 17, 2006	"Funk '980"
G-05	Israel Beinglass, "Meeting the challenges of process module and fab-wide active control for 300 mm, 130 nm and beyond" published in the Proceedings of the SPIE, Vol. 4692, pp. 136-146 (2002)	2002	2002	"Beinglass"
G-06	2002/0193899	June 19, 2001	April 13, 2010	"Shanmugasundram"
G-07	"Run-to-Run Control and Performance Monitoring of Overlay in Semiconductor Manufacturing" by C.A. Bode et al. published in the 15th Triennial World Congress, Barcelona, Spain	2002	2002	"Bode"
G-08	5,483,636	February 3, 1993	January 9, 1996	"Saxena"

Corresponding Chart	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
G-09	6,587,744	June 22, 1999	July 1, 2003	"Stoddard"
G-10	6,891,627	September 20, 2000	May 10, 2005	"Levy"
G-11	2003/0014145	July 16, 2001	February 26, 2008	"Reiss"
G-12	Japanese Patent Publication No. JP2001-155979	November 24, 1999	June 8, 2001	"Hamaguchi"
G-13	Japanese Patent Publication No. JPH9-50949	May 17, 1996	February 18, 1997	"Takahashi"
G-14	Japanese Patent Publication No. JPH10-209230	January 23, 1997	August 7, 1998	"Ono"
G-15	Japanese Patent Publication No. JPH11-176713	December 12, 1997	July 2, 1999	"Kotani"
G-00	U.S. Patent No. 6,460,002	Feb. 9, 2000	Oct. 10, 2002	"Bone"
	U.S. Patent No. 6,405,096	Aug. 10, 1999	June 11, 2002	"Toprac"
	Funk, "A common APC Architecture for 200 & 300nmm Etch"	2002	2002	"Funk NPL"
	Japanese Patent Publication No. JP2000-252179	Mar. 4, 1999	Sept. 14, 2000	"Aida"
	Japanese Patent Publication No. JPH9-011092	Jun. 20, 1995	Jan. 14, 1997	"Morii"
	Japanese Patent Publication No.	Oct. 8, 1998	Apr. 21, 2000	"Someya"

Corresponding Chart	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
	JP2000-114150			
	Japanese Patent Publication No. JPH10-116872	Oct. 8, 1996	May 6, 1998	"Azumi"
	Japanese Patent Publication No. JP2002-269109	Mar. 12, 2001	Sept. 20, 2002	"Hitachi"
	U.S. Patent No. 5,864,773	Nov. 1, 1996	Jan. 26, 1999	"Barna"

b. Prior Art Systems/Services To The Asserted Claims of the '691 Patent.

System/Service	Relevant Dates	Persons/Entities Involved in Prior Use, Sale, or Offer for Sale
Automated Image Retrieval	2001	Tobin Oak Ridge National Laboratory
ModelWare	2001	Markle Triant Technologies, Inc.
Maestria	2003	SI Automation, PDF Solutions
Promis	1997	Promis Systems, Sony Semiconductor of America

2. Obviousness Combinations

A person having ordinary skill in the art would have been motivated to combine any of the references described in attached Exhibits G00-G11 including for the reasons described below. A person having ordinary skill in the art at the time of filing of the '691 Patent would also have understood the references listed above, alone or in combination, to contain explicit and/or implicit

teaching, suggestion, and/or rationales to combine them, including as further described below. In particular, a person of ordinary skill in the art, through the motivations described below, in addition to technical incentives and market forces, would have been motivated to combine the well-known techniques described in the references and attached Exhibits G01-G11 to yield predictable results.

As a threshold matter, the '691 Patent itself admits that a number of the claimed elements were commonly known, and conventional, prior to the date of the alleged invention. For example, the '691 patent discloses that:

- "Generally, a set of processing steps is performed on a wafer using a variety of processing tools, including photolithography steppers, etch tools, deposition tools, polishing tools, rapid thermal processing tools, implantation tools, etc. One technique for improving the operation of a semiconductor processing line includes using a factory wide control system to automatically control the operation of the various processing tools. The manufacturing tools communicate with a manufacturing framework or a network of processing modules. Each manufacturing tool is generally connected to an equipment interface. The equipment interface is connected to a machine interface which facilitates communications between the manufacturing tool and the manufacturing framework. The machine interface can generally be part of an advanced process control (APC) system. The APC system initiates a control script based upon a manufacturing model, which can be a software program that automatically retrieves the data needed to execute a manufacturing process." ('691 Patent at 1:27-45) (e.g., "collecting metrology data related to the processing of workpieces in a

plurality of tools," "conducting a process control activity related to one of the tools based on [] metrology data")

- "Often, semiconductor devices are staged through multiple manufacturing tools for multiple processes, generating data relating to the quality of the processed semiconductor devices. Pre-processing and/or post-processing metrology data is collected on a regular basis, generally in accordance with a sampling plan, for process control purposes. The collected metrology data is used by the process controllers for the tools. Operating recipe parameters are calculated by the process controllers based on the performance model and the metrology information to attempt to achieve post-processing results as close to a process target value as possible. Reducing variation in this manner leads to increased throughput, reduced cost, higher device performance, etc., an of which equate to increased profitability." ('691 Patent at 1:46-60) (e.g., "collecting metrology data related to the processing of workpieces in a plurality of tools," "generating context data for the metrology data, the context data including collection purpose data," "conducting a process control activity related to one of the tools based on the [] metrology data")
- "Metrology data is also used for other purposes not related to process control. One such use is for fault detection and classification (FDC). Fault monitors apply FDC techniques to identify devices or tools with fault conditions. For example, if a particular device has a critical dimension outside a predetermined range, it is flagged as being defective. The wafer may be reworked, the die may be marked defective, or the wafer may be scrapped, depending on the magnitude and nature of the fault condition. Process tools may be monitored during their processing runs. If

an anomaly is observed during the processing, the tool may be shut down for maintenance. The wafers processed by the tool may be flagged for subsequent metrology to determine if the tool anomaly caused a degradation of the devices formed thereon. Again, the suspect wafers may be reworked or scrapped." ('691 Patent at 1:61-2:9) (e.g., "collecting metrology data related to the processing of workpieces in a plurality of tools," "generating context data for the metrology data, the context data including collection purpose data," "filtering the metrology data based on the collection purpose data," "conducting a process control activity related to one of the tools based on the filtered metrology data")

- "Typically, when a process controller gathers metrology data to update its control model or generate a control action for subsequent processing, it retrieves metrology data related to wafers processed in the tool or tools under its control and employs that data to perform its control task. The data retrieved includes metrology data collected through the regular sampling plans implemented in the facility, and the metrology data collected for other purposes. Some of the metrology data does not accurately reflect the state of the process or the devices manufactured. For example, devices processed by a tool that was malfunctioning may have characteristics that were affected by the malfunction (i.e., a special cause) rather than by normal process variation (i.e., common cause)." ('691 Patent at 2:10-27) (e.g., "collecting metrology data related to the processing of workpieces in a plurality of tools," "generating context data for the metrology data, the context data including collection purpose data," "filtering the metrology data based on the collection

purpose data," "conducting a process control activity related to one of the tools based on the filtered metrology data")

The '691 Patent further notes that a person of ordinary skill in the art had motivation to improve upon these commonly known, conventional, processing steps by pursuing and/or combining known options:

- "Employing this data for use in process control routines may introduce a source of variation that cannot be addressed by the process controller and thus reduce the effectiveness of the process controller." ('691 Patent at 2:23-26)
- "There is a constant drive within the semiconductor industry to increase the quality, reliability and throughput of integrated circuit devices, e.g., microprocessors, memory devices, and the like. This drive is fueled by consumer demands for higher quality computers and electronic devices that operate more reliably. These demands have resulted in a continual improvement in the manufacture of semiconductor devices, e.g., transistors, as well as in the manufacture of integrated circuit devices incorporating such transistors. Additionally, reducing the defects in the manufacture of the components of a typical transistor also lowers the overall cost per transistor as well as the cost of integrated circuit devices incorporating such transistors." ('691 Patent at 1:13-25)
- "Reducing variation in this manner leads to increased throughput, reduced cost, higher device performance, etc., an of which equate to increased profitability." ('691 Patent at 1:57-60)

A person having ordinary skill in the art would have been motivated to combine any of the references described in attached Exhibits G00-G11 at least because each of the references is related

to semiconductor manufacturing and/or process control, and the semiconductor industry recognized that process control improved cost effectiveness of semiconductor manufacturing by controlling manufacturing parameters to reduce defects and ultimately increase yield. Many of the references in Exhibits G00-G11 are to Advanced Process Control (APC) systems in semiconductor fabrication. Flexibility in the APC systems was recognized as improving the effectiveness of APC systems, such as by modularizing the APC system to (1) accept metrology data, context data, and other data from multiple sources, (2) perform customized processing of the collected data, and/or (3) store data in known structures such as relational databases. Combining different process control techniques known from one reference into a process control system of another reference would have been mere application of a known technique to a piece of prior art ready for the improvement and would have reasonably expected to successful combine different process control techniques. For example, Funk '980 describes a modular APC system and would have been readily modifiable by a person of ordinary skill in the art based on disclosure in other references, such as Stoddard. In one particular combination, a person of ordinary skill in the art would have been motivated to modify Funk '980 with Stoddard's disclosure of storing metrology data collected from metrology tools measuring characteristics of workpieces processed by the same types of tools as used in Funk '980 in a relational database, and using the data to modify process variables based on feedback and/or feed-forward control algorithms. Additional background materials and description of motivation for using different aspects of process control techniques that would have been known by a person of ordinary skill in the art may be found in "The economics of yield-driven processes" by Roger E. Bohn published in the Journal of Operations Management (1999), PCT Publication No. 2004/031875, "Benchmarking Semiconductor Manufacturing" by Robert C. Leachman published in IEEE Trans. On

Semiconductor Manufacturing (1996), “Equipment Fault Detection Using Spatial Signatures” by Martha M. Gardner published in IEEE Trans. On Components, Packaging, and Manufacturing Tech. (1997), “The MMST Computer-Integrated Manufacturing System Framework” by John McGehee published in IEEE Trans. On Semiconductor Manufacturing (1994), “Comparing the Economic Impact of Alternative Metrology Methods in Semiconductor Manufacturing” by Payman Jula published in IEEE Trans. On Semiconductor Manufacturing (2002), “Data requirements and communication issues for advanced process control” by Richard J. Markle published in JVST A (2001), “On the Utility of Run-to-Run Contorl in Semiconductor Manufacturing” by John Musacchio published by the IEEE (1997), “Practical issues in the deployment of a run-to-run control system in a semiconductor manufacturing facility” by Jerry Stefani published by SPIE (1999), “APC in the Semiconductor Industry, History and Near Term Prognosis” by Gabriel G. Barna by IEEE (1996), “Monitoring and Control of Semiconductor Manufacturing Processes” by Suttipan Limanond published by IEEE (1998), “Fault Diagnosis of Plasma Etch Equipment” by Anna M. Ison in IEEE (1997), “Metrology needs for the semiconductor industry over the next decade” by Mark Melliar-Smith by AIP (1998), “New tools for yield improvement in integrated circuit manufacturing: can they be applied to reliability?” by Chris J. McDonald in Microelectronics Realiability (1999), “Handbook of Thin Film Deposition (2d ed.)” ed. By Krishna Seshan by Noyes Publications (2002), “Integarted applications of inspection data in the semiconductor manufacturing environment” by Kenneth Tobin in SPI (2001), “Real-Time Statistical Process Control Using Tool Data” by Costas J. Spanos by IEEE (1992), “Equipment Analysis and Wafer Parameter Prediction Using Real-time Tool Data” by Sherry F. Lee by IEEE (1994), “RTSPC: A Software Utility for Real-Tiime SPC and Tool Data Analysis” by Sherry F. Lee in IEEE (1995), “Prediction of Wafer State After Plasma Processing

Using Real-Time Tool Data" by Sherry F. Lee by IEEE (1995), and "Real-Time Diagnosis of Semiconductor Manufacturing Equipment Using a Hybrid Neural Network Expert System" by Byungwhan Kim by IEEE (1997). Some exemplary citations of particular features of the claims of the '691 patent and their disclosure in the prior art of Exhibits G00-G11 are listed below and may be combined with any of the other references of Exhibits G00-G11 and the knowledge of a person of ordinary skill including the knowledge reflected in the references listed herein and in Exhibits G00-G11.

"collecting metrology data related to the processing of workpieces in a plurality of tools" (claim 1) / "**storing the metrology data and the context data in a data store**" (claim 9): To the extent that any of the references charted in these Preliminary Invalidity Contentions does not disclose "collecting metrology data related to the processing of workpieces in a plurality of tools," it would have been obvious to combine that reference with any of the other references that disclose this feature, such as Funk '980, Stoddard, and Reiss. For example, Funk '980 describes that "a processing tool comprises internal sensors" such that "the processing tool can be considered a sensor" and that data collected as "integrated metrology (IM)." Funk '980 at 5:7-21, 3:52-57. In Funk '980, that "data can be sent to the APC system," such as in "data files" in addition to other data such as "tool trace data, maintenance data, and EPD data." Funk '980 at 5:7-21. In particular, Funk '980's APC system can collect data related to "a plurality of tools." Funk '980 describes that "[t]he data obtained from the processing tools, the processing chambers, the sensors, and the APC system is stored in tables." Funk '980 at 7:4-14. As another example, Stoddard describes "an advanced run-to-run controller for … taking metrology measurements from the processing tools" through "an interface for receiving metrology data from the metrology tools." Stoddard at 2:19-35. Further, Reiss notes that "any number of metrology tools or sensors 190 may be

positioned upstream or downstream from each of the one or more tools 150 for measuring wafer properties immediately before or after processing by the one or more tools 150." Reiss at [0026]-[0028]. A person of ordinary skill in the art at the time of the alleged invention would have combined the references because collecting metrology data from a variety of tools was a common part of processing semiconductor wafers that provides information that assists with understanding operations and faults in the semiconductor processing. The collection of such metrology data allows for the use of run-to-run control, which a person of ordinary skill in the art would have been motivated to use because run-to-run control improves the yield of semiconductor manufacturing and manufacturing processes in general. Bode describes this motivation in stating that "[t]he deployment of the run-to-run controller eliminated the need for engineering intervention to maintain and distribute overlay recipe settings to the exposure tools, thereby increasing the uptime for the tools and the amount of engineering resources that can be applied to other tasks within the module. The control state is updated each time new metrology data are made available, producing control settings that are based on all available process information." Bode at 6. Bode adds that the collection of metrology data and its use in run-to-run control allowed "the task of overlay control [to be] greatly simplified through the implementation of run-to-run control" and "reduce[d] the maximum site-level error, averaged over all controlled masking operations, by 43% over manual methods." Bode at 6. The yield of a process can be improved by improving efficiency, and a person of ordinary skill in the art would be motivated collect metrology data from a plurality of tools to use run-to-run control in semiconductor processing. Reiss notes that "measurements of any number of wafer properties are collected … by wafer management system" and "[r]un-to-run process 230 analyzes the wafer properties measured by wafer measurement system 240 and determines whether any modifications can be made to the tool's process recipe (via e.g., control

process 210) to increase efficiency." Reiss at [0033]. A person of ordinary skill in the art would understand a relational database as in Stoddard is one well-known data store for storing context data and would be motivated to use a relational database because of its' flexibility in storing and accessing data.

"generating context data for the metrology data, the context data including collection purpose data" (claim 1) / "**storing the metrology data and the context data in a data store**" (claim 9): To the extent that any of the references charted in these Preliminary Invalidity Contentions does not disclose "generating context data for the metrology data, the context data including collection purpose data," it would have been obvious to combine that reference with any of the other references that disclose this feature, such as Funk '980, Beinglass, and/or Stoddard. Funk '980 describes that different kinds of data can be configured to be collected for each wafer, and that "wafer context information can include tool ID, module ID, slot ID, recipe ID, cassette ID, start time and end time." Funk '980 at 6:22-34. As another example, Taneka describes that "apparatus histories, e.g. as regards which apparatus has manufactured the product, the producing conditions in the operation, and in-line measurement values as the results of each operation are accumulated as the information on factors which may affect the quality of products." Tanaka at 3:18-29. As a further example, Beinglass describes generating "process history" with "[t]ool-state and wafer-state information is incorporated into the process model and compensated for accordingly." Beinglass at 138, 142-43. As yet another example, Stoddard describes that "[o]nce the metrology information is acquired, it is stored in a Metrology Database 85 along with the Date, Time, Tool, MiniSpec, Lot ID and Run Number." Stoddard at 5:40-50. A person of ordinary skill in the art at the time of the alleged invention would have combined the references because the generation and collection of context data corresponding to the collected metrology data would

have provided more information for improving the yield and efficiency of semiconductor manufacturing. For example, the collected metrology data may be used to adjust a run-to-run controller or perform other system control through feedback of the metrology data, and context information, such as the apparatus history or information about the wafers and recipes used, allow identification of operations on a particular tool in a plurality of tools that may be faulty, which allows the controller to more quickly achieve increased yield and increased efficiency. The context data would in particular improve the ability to mine and analyze the collected metrology data. Indeed, Beinglass describes that "[g]athering all of this metrology and process history into common and linked data-base to support critical metric monitoring and data analysis is required prior to undertaking an enterprise level data mining effort" and that "[d]ata mining is an ever more important activity within semiconductor manufacturing facilities." Beinglass at 142-43. A person of ordinary skill in the art would understand a relational database as in Stoddard is one well-known data store for storing context data and would be motivated to use a relational database because of its' flexibility in storing and accessing data.

"filtering the metrology data based on the collection purpose data" (claim 1): To the extent that any of the references charted in these Preliminary Invalidity Contentions does not disclose "filtering the metrology data based on the collection purpose data," it would have been obvious to combine that reference with any other reference that teaches this feature, such as Funk '980, Stoddard, Tanaka, Bode and/or Nagase. For example, Funk '980 describes the use of a "multivariate analysis of summary data using models based upon historical data," which encompasses filtering the metrology data based on Plaintiff's allegations that the use of multivariate analysis in fault detection and classification algorithms meets this limitation. Indeed, Funk '980 describes that "[f]ault forecasting can be based either on a complex multivariate model

or a simple univariate relationship (e.g. APO angle for a wet clean in etch)." Funk '980 at 11:20-30. As another example, Stoddard describes the use of a variable parameters table (VPT) that "relate[s] received metrology data to one or more variables for a processing tool." Stoddard at 2:19-35. As a further example, Tanaka describes "analyzing the causal relation between the yield data and the producing apparatus history data, various other information may be used for analysis such as data on electric characteristics instead of the yield data, or data on producing conditions or in-line measurement values." Tanaka at 4:40-51. As still a further example, Bode describes the use of a "linear model predictive control (LMPC)," which are "control algorithms that use a linear process model and a linear or quadratic open-loop objective function and linear constraints to compute the requisite manipulated variables over a future time horizon." Bode at 1. In each of these examples, the filtering of the metrology data is based on collected data, which includes the generated context data comprising the collection purpose data. A person of ordinary skill in the art at the time of the alleged invention would have combined the references because large sets of metrology data can be collected during semiconductor fabrication and would be reduced to facilitate the processing of the metrology data, such as when performing fault analysis or fault prediction. Improving the efficiency of analyzing the metrology data, such as by filtering the metrology data based on collection purpose data, improves the efficiency in the use of "fault forecasting … to predict when a tool, process module, and/or sensor might fail, and when to perform maintenance on a tool, process module, and/or sensor." Funk '980 at 11:20-30. Indeed, a person of ordinary skill in the art would have recognized the benefits of such models that incorporate filtering of the metrology data. For example, Bode describes that "[r]ecent applications of run-to-run control by Bode (2001), Campbell (1999), and Edgar et al. (1999) have shown that multivariable control that allows for constraints offers definite benefits over

conventional control strategies." Bode describes an example "open-loop estimation of the original state vector and linear filtering of [a] disturbance vector," in which "[t]he number of states that can be estimated from a single metrology event is necessarily less than or equal to the number of measurements from that metrology." Bode at 3. In one particular example, the efficiency of analysis of metrology data can be improved by filtering such that "abnormal measured value is deleted from the extracted data." Nagase at 1:27-29. Nagase also describes a more general "data extractor [that] may provide for dynamically creating a record selecting formula standing for a record extracting condition by using a retrieved data context variable table and a common index information context variable table in the relations and for extracting data in a manner to independently separate a client module for creating the record selecting formula and retrieve request information from a server module for creating a data retrieving program based on the retrieve request information and executing the data retrieving program and to communicate the client module with the server module." Nagase at 2:27-38. More generally, a person of ordinary skill would recognize that a data collection plan would enable efficient collection of metrology data for us in identifying high quality product with desirable physical and electrical characteristics, and that identification of high quality product is the basic requisite for improving the operation of a processing tool (e.g., to allow defining a "good" or "target" product result). Filtering the metrology data to separate data regarding high quality product would be known to a person of ordinary skill as a manner of improving control of the processing. To the extent any reference does not describe filtering specifically based on the context data comprising collection purpose data, a person of ordinary skill in the art would have understood that such data was useful in filtering the data by removing, e.g., wafer IDs associated with abnormal measured values or

abnormal process results, or, e.g., by specifically excluding or selecting data from lower quality products or data collected from dummy wafers. *See, e.g.,* Funk '980 at 24:20-26:56.

"conducting a process control activity related to one of the tools based on the filtered metrology data" (claim 1) / **"determining at least one parameter of an operating recipe employed by one of the tools"** (claim 7): To the extent that any of the references charted in these Preliminary Invalidity Contentions does not disclose "conducting a process control activity related to one of the tools based on the filtered metrology data," it would have been obvious to combine that reference with any of the references that disclose the feature, such as Funk '980, Stoddard, Nagase, and/or Levy. For example, Funk '980 describes an "Advanced Process Control (APC) system for controlling a processing tool in a semiconductor processing environment" using collected data by a monitoring system such as stored in a database that is filtered as part of analyzing the collected data. Funk '980 at 2:1-18. As another example, Stoddard describes that "[t]he parameters of the VPT 37 are calculated and updated based on metrology data for the particular process implemented by the associated processing tool." Stoddard at 3:66-4:14. As a further example, Levy describes: "the processor may be configured to alter the monitored parameter of the instrument in response to the determined relationship. For example, the processor may be configured to use a determined relationship to alter a parameter of an instrument coupled to the resist apply chamber such that the temperature and humidity of the resist apply chamber may be altered in response to a determined presence of defects on the surface of the specimen." Levy at 64:67-65:31. A person of ordinary skill in the art at the time of the alleged invention would have combined the references because process control was a well-known art that improves manufacturing, including semiconductor manufacturing. Process control can improve manufacturing efficiency and yield, and ultimately reduce costs associated with components

manufactured in the semiconductor processing. Funk '980 describes what a person of ordinary skill in the art would have known about the benefits of process control: "[t]he goal of the APC system is to use real-time and historical data to improve the semiconductor processing system's performance. To achieve this goal, potential problems can be predicted and corrected before they occur, thus reducing equipment downtime and the number of non-product wafers that are produced. This can be accomplished by collecting data and then feeding that data into a software algorithm that models the behavior of a particular tool, process module, and/or sensor. The APC system outputs process parametric adaptations that are then either fed forward or back to keep the tool performance within the specified limits." Funk '980 at 10:66-11:11. Further, Nagase describes that a person of ordinary skill in the art would have been motivated to conduct a process control activity: "[t]he present invention relates to a system for supporting data analysis in a VLSI process, and more particularly to a system which is capable of efficiently deriving a process parameter(s) (condition), analyzing device characteristics and improving yields of a semiconductor device in developing a process for a semiconductor electronic device such as a VLSI device." Nagase at 1:6-12. A person of ordinary skill in the art would have additionally known that one manner of conducting a process control activity involves determining a parameter of an operating recipe employed by one of the tools, as recited in claim 7. For example, Funk '980 describes that "[t]he operation of the APC system can be established using context driven strategies and plans. A strategy is used to define what should happen during a set of sequences on the APC system. This set of sequences can be associated with a lot, a batch, a wafer, a recipe, or a set of machine activities." Funk '980 at 19:42-20:17.

"generating identification data associated with the metrology data" / **"filtering the metrology data based on the identification data and the collection purpose data"** (claim 2):

To the extent that any of the references charted in these Preliminary Invalidity Contentions does not disclose "generating identification data associated with the metrology data" and/or "filtering the metrology data based on the identification data and the collection purpose data," it would have been obvious to combine that reference with any of the references that disclose that feature, such as Stoddard, Saxena, and/or Funk '980. For example, Stoddard describes that "[o]nce the metrology information is acquired, it is stored in a Metrology Database 85 along with the Date, Time, Tool, MiniSpec, Lot ID and Run Number." Stoddard at 5:16-6:67. As another example, Saxena describes that "[a]s a plurality of wafers are processed, a plurality of process parameters are measured. A wafer tracking database is created which contains the plurality of process parameters and a plurality of identifying information associated with each wafer." Saxena at 2:15-60. As a further example, Funk '980 describes "that different kinds of data can be configured to be collected for each wafer," and that "wafer context information can include tool ID, module ID, slot ID, recipe ID, cassette ID, start time and end time." Funk '980 at 6:22-34. A person of ordinary skill in the art at the time of the alleged invention would have combined the references to obtain identification data associated with the metrology data because the availability of context information, such as identification data, can improve analysis, such as filtering, of the metrology data by allowing the identification of particular sets of data within the metrology data, and potentially the removal of certain sets of data within the metrology data. For example, data associated with wafers processed through particular tools or at particular times or with particular recipes or data associated with dummy wafers may be selected or excluded from the metrology data prior to performing process control using, for example, SQL statements as described in Funk '980.

"generating collection purpose data indicating at least one of a process control sampling purpose, a fault detection sampling purpose, and a targeted fault detection purpose" (claim 3): To the extent that any of the references charted in these Preliminary Invalidity Contentions does not disclose "generating collection purpose data indicating at least one of a process control sampling purpose, a fault detection sampling purpose, and a targeted fault detection purpose" it would have been obvious to combine that reference with any of the other references that disclose that feature, such as Funk '980. For example, Funk '980 discloses a "tool health control strategy," i.e., "[a] control strategy… to determine tool health status," where "diagnostic wafer data can be collected" and the context can be tool diagnostics. Funk '980 at 25:18-29. A "tool health control strategy" would be recognized as possible to associate with a data collection plan (and its associated data collection plan ID, (i.e., collection purpose data)) where the context is tool diagnostics. Funk '980 at 25:18-29, 24:57-65. The "tool diagnostic" context would be a "targeted fault detection purpose" as recited in claim 3 of the '691 patent. This disclosure of Funk '980 would motivate a person of ordinary skill to implement a "tool health control strategy" for collecting metrology data for tool diagnostics (e.g., a targeted fault detection purpose) when combined with any other reference disclosing collection of data, such as collection of metrology data.

"changing the collection purpose data responsive to identifying the fault condition" (claim 4) / **"changing the collection purpose data responsive to identifying the absence of the fault condition"** (claim 5): To the extent that any of the references charted in these Preliminary Invalidity Contentions does not disclose "changing the collection purpose data responsive to identifying the fault condition" and/or "changing the collection purpose data responsive to identifying the absence of the fault condition" it would have been obvious to combine that

reference with any of the other references that disclose that feature, such as Shanmugasundram and Reiss. For example, Shanmugasundram describes the use of a "sampling plan" and that "the frequency at which wafers are measured ('wafer-to-wafer') is adjusted, following an event that suggests that more (or fewer) wafers should be measured" and that in a "second variation, the spatial resolution of the measurements of those wafers selected for measurement ('withinwafer') is increased or decreased, following an event that suggests each wafer which is measured should be measured in greater (or lesser) detail." As a further example, Shanmugasundram describes the use of "a dynamic metrology plan utilizes an initial sampling plan and adjusts the sampling responsive to certain events or non-events. As an example of an adjustment due to a non-event, if the last ten wafers measured are all the same, and if the processing device did not change, and if the recipe on the processing device did not change, one could reasonably assume that the next series of wafers will have measurements that are also all the same. That being the case, then in order to increase throughput and decrease the time it takes to do measurements, the invention provides for dynamically adjusting the measurements, for example, such that every third wafer instead of every wafer is measured. This invention thus detects and adjusts for not only potential errors, which could arise for example upon a recipe change, but also for accuracy." Shanmugasundram at [0034]-[0044]. Reiss further describes process control involving a fault or no fault detection system: "[d]uring execution of the process, as will be discussed below, fault detection system 110 monitors the tool for tool faults or tool failures and the wafers for wafer property failures (STEP 320). The analysis conducted by fault detection system or, in other words, whether a fault is detected, is forwarded to run-to-run controller 120 (STEP 324). For example, a fault detection index may be passed to controller 120 (from fault detection system 110) for identifying the presence or absence of a fault. In accordance with one or more embodiments of the

present invention, this information is then used to determine those instances where a recipe should (and should not) be modified according to run-to-run techniques." Reiss at [0037]-[0040A person of ordinary skill in the art at the time of the alleged invention would have combined the references because modification of the collection purpose data based on the presence of a fault condition may allow more effective filtering of metrology data, such as filtering metrology data received during a manufacturing process to improve the yield, increase efficiency, and reduce cost. For example, Shanmugasundram describes "a dynamic metrology plan utilizes an initial sampling plan and adjusts the sampling responsive to certain events or non-events. As an example of an adjustment due to a non-event, if the last ten wafers measured are all the same, and if the processing device did not change, and if the recipe on the processing device did not change, one could reasonably assume that the next series of wafers will have measurements that are also all the same. That being the case, then in order to increase throughput and decrease the time it takes to do measurements, the invention provides for dynamically adjusting the measurements, for example, such that every third wafer instead of every wafer is measured. This invention thus detects and adjusts for not only potential errors, which could arise for example upon a recipe change, but also for accuracy." Shanmugasundram at [0034]-[0044]. Further, "dynamic metrology is performed to better meet a certain specification. For example, if recipe parameters are changed on the processing device, to adjust the thickness of a film that is deposited on the wafer, it may be desirable to more closely check whether the specification is still being achieved by performing measurements." Shanmugasundram at [0034]-[0044].

"**updating a state of a control model employed by a process controller associated with one of the tools**" (claim 6): To the extent that any of the references charted in these Preliminary Invalidity Contentions does not disclose "updating a state of a control model employed by a

process controller associated with one of the tools," it would have been obvious to combine that reference with any of the other references that disclose that feature, such as Funk '980. Funk '980 describes that a data collection plan uses data "collected during production runs that yield high quality product … to establish 'good tool state' data, and data collected subsequently can be compared with this baseline data to determine if a tool is performing correctly in real-time." Funk '980 at 25:13-17. The baseline established by filtering metrology data based on data collection plan to identify data associated with good products could be used by a person of ordinary skill in the art to determine whether a tool is performing correctly and establish a baseline in a control model the APC associated with that tool (e.g., by using a tool ID). Further, a person of ordinary skill in the art would understand that conducting a process control activity involves updating a state of a control model employed by a process control, because control models were well-known techniques for controlling manufacturing processes.

"excluding metrology data associated with a potential defect condition based on the collection purpose data" (claim 8): To the extent that any of the references charted in these Preliminary Invalidity Contentions does not disclose "excluding metrology data associated with a potential defect condition based on the collection purpose data," it would have been obvious to combine that reference with any of the other references that disclose that feature, such as Beinglass or Funk '980. For example, Beinglass describes that "[a] golden set of "good" wafers is selected and the statistical characteristic of these wafers is extracted and establishes the model parameters. The model is generated automatically based on this set of wafers." Beinglass at 137. The selection of good wafers would result in the exclusion of defective wafers. As another example, Funk '980 describes that "[d]ata collected during production runs that yield high quality product can be used to establish "good tool state" data, and data collected subsequently can be compared with this

baseline data to determine if a tool is performing correctly in real-time." Funk '980 at 25:13-17. As yet another example, Bode describes "[a]s a first pass at removing some of the variation from the overlay control signal which is subject to a significant amount of noise, outlier rejection was used to cull significantly aberrant data from the process. It was generally clear from operating experience when a lot is a outlier by the magnitude of the error generated from metrology. Simple limits on the allowable measured error can successfully identify those lots which have overlay performance that significantly departs from the rest of the line. One may also set a limit on the amount of residual error in the fitted model, though this only captures those cases when the metrology results are erroneous." Bode at 4-5. As a further example, Saxena describes that a "query generator (10) can also have domain filters (30) to prevent generation of queries that are a-priori known to be uninteresting. For example, any queries that result in lower than a given yield loss are removed from consideration." Saxena at 4:45-48. As yet another example, Stoddard describes that a "'golden model' created from the 'golden data set' can be restored as in the case with models that have adapted over time." Stoddard at 9:23-59. A person of ordinary skill in the art at the time of the alleged invention would have combined the references because excluding data with potential defect conditions based on the collection purpose data, such as to filter out data associated with diagnostic collections because doing so would improve the process control performed based on the filtered metrology data such that the semiconductor manufacturing processes result in higher yield.

Further, motivation for combining references exists because the prior art references and systems all are commonly related and are from the same field of art, and a person of ordinary skill in the art would draw equally from the field of art to solve the problem allegedly presented in the '691 Patent. The combinations suggested above reflect at least combinations of prior art elements

according to known methods to yield predictable results, simple substitutions of known elements to obtain predictable results, and combinations that are obvious to try.

Further elaboration and information shall be provided with the Defendant's expert report(s). The combinations of references provided above are exemplary and are not intended to be exhaustive. Additional obviousness combinations of the references identified here are possible, and Defendant may rely on such combination(s) in this litigation. In particular, Defendant is currently unaware of Ocean's allegations with respect to the level of skill in the art and the qualifications of the typical person of ordinary skill in the art. Defendant is also unaware of the extent, if any, to which Ocean may contend that limitations of the claims at issue are not disclosed in the prior art identified by defendants as anticipatory, and the extent to which Ocean will contend that elements not disclosed in the asserted patent specifications would have been known to persons of skill in the art. And Defendant does not yet know how the Court will construe terms in the asserted claims. Defendant is also continuing its investigation of the large universe of prior art to identify potential prior art systems, publications related to those systems, and third parties that may have information about those systems. Ocean may also be in possession of prior art that Defendant may receive after discovery opens in this case. Defendant reserves the right to amend and supplement these contentions to identify other prior art and combinations rendering the asserted claims obvious.

h. The '097 Patent

1. Identification of Prior Art

The tables below list prior art that anticipates and/or renders obvious one or more of the asserted claims. The attached claim charts in Exhibits H1-H9 demonstrate where each limitation of the claims is found in certain of the references listed below, either expressly or inherently in the

larger context of the passage, as understood by a person having ordinary skill in the art. The following patents, publications, products and/or services are prior art under at least 35 U.S.C. §§ 102(a), (b), or (e).

a. Prior Art Patents and Patent Publications To The Asserted Claims of the '097 Patent.

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
H1	Applicant Admitted Prior Art	N/A	N/A	"AAPA"
H2	U.S. Pat. No. 5,705,321	Sept. 30, 1993	Jan. 6, 1998	"Brueck"
H3	U.S. Pat. No. 5,976,769	July 14, 1995	Nov. 2, 1999	"Chapman"
H4	U.S. Pat. No. 6,319,822	Oct. 1, 1998	Nov. 20, 2001	"Chen"
H5	U.S. Pat. No. 6,362,111	Dec. 9, 1998	Mar. 26, 2002	"Laaksonen"
H6	U.S. Pat. No. 6,010,829	May 31, 1996	Jan. 4, 2000	"Rogers"
H7	U.S. Pat. No. 5,977,601	July 17, 1998	Nov. 2, 1999	"Yang"
H8	U.S. Pat. No. 6,027,861	Mar. 20, 1998	Feb. 22, 2000	"Yu"
H9	V. Rao, et al., *Ultrathin photoresists for EUV lithography*, Proc. SPIE 3676, Emerging Lithographic Technologies III (June 25, 1999)	June 25, 1999	June 25, 1999	"Rao"
	G. Becker, et al., *A comparative study of resist stabilization techniques for metal etch processing*, Proc. SPIE 3678, Advances in Resist Technology and Processing XVI (June 11, 1999)	June 11, 1999	June 11, 1999	"Becker"
	Q. Lin, et al., *Dual-layer inorganic SiON bottom ARC for 0.25-*	June 11, 1999	June 11, 1999	"Lin"

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
	um DUV hard mask applications, Proc. SPIE 3678, Advances in Resist Technology and Processing XVI (June 11, 1999)			
	U.S. Pat. No. 6,319,655	June 11, 1999	Nov. 20, 2001	"Wong"
	K. Nguyen, et al., *Characterization of the manufacturability of ultrathin resist*, J. Vac. Sci. Technology B 17(6), Nov/Dec 1999	Nov./Dec. 1999	Nov./Dec. 1999	"Nguyen"
	C.S. Huang, et al., *A Novel UV Baking Process to Improve DUV Photoresist Hardness*, IEEE 1999 International Symposium on VLSI Technology, Systems, and Applications. Proceedings of Technical Papers (June 1999)	June 1999	June 1999	"Huang"
	W. Krisa, et al., *0.25-um multilevel interconnect with DUV processing*, Proc. SPIE 3051, Optical Microlithography X (July 7, 1997)	July 7, 1997	July 7, 1997	"Krisa (SPIE)"
	W.L. Krisa, et al., *DUV resist etch selectivity improvement using UV stabilization*, Microelectronic Engineering 35 (1997)	1997	1997	"Krisa (ME)"
	U.S. Pat. No. 5,773,199	Sept. 9, 1996	June 30, 1998	"Linliu"

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
	W. Lee, et al., *Fabrication of 0.06-um poly-Si gate using DUV lithography with a designed $Si_xO_yN_z$ film as an arc and hardmask*, IEEE 1997 Symposium on VLSI Technology Digest of Technical Papers (June 1997)	June 1997	June 1997	"Lee"
	J. Hryniewicz, *Chemically Assisted Ion Beam Etching for Photonics Applications*, Ph.D. dissertation, University of Maryland (1998)	1998	1998	"Hryniewicz"
	M. Armacost, et al., *Plasma-etching processes for ULSI semiconductor circuits,* IBM J. Res. Develop. 43 (Jan-Mar 1999)	Jan.-Mar. 1999	Jan.-Mar. 1999	"Armacost"
	R.A. Cirelli, et al., *A multilayer inorganic antireflective system for use in 248 nm deep ultraviolet lithography*, J. Vac. Sci. Technology B 14(6), Nov/Dec 1996	Nov./Dec. 1996	Nov./Dec. 1996	"Cirelli"
	U.S. Pat. No. 6,020,269	Dec. 2, 1998	Feb. 1, 2000	"Wang"
	U.S. Pat. No. 5,885,887	Apr. 21, 1997	Mar. 23, 1999	"Hause"
	U.S. Pat. No. 6,358, 672	July 7, 1998	Dec. 20, 2001	"Jeoung"
	T. Ko, et al., *Implementation of organic bottom antireflective coating in 0.35-um polycide*	Aug. 14, 1997	Aug. 14, 1997	"Ko"

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
	fabrication, Proc. SPIE 3183, Microlithographic Techniques in IC Fabrication (August 14, 1997)			
	T. Azuma, et al., *Impact of reduced resist thickness on deep ultraviolet lithography*, J. Vac. Sci. Technology B 14(6), Nov/Dec 1996	Nov./Dec. 1996	Nov./Dec. 1996	"Azuma"
	U.S. Pat. No. 5,698,072	June 29, 1992	Dec. 16, 1997	"Fukuda"
	Ning Gu, et al., *Application of poly(methyl methacrylate) ultrathin resist supported by a flowing subphase method in electron-beam fabrication of a 4 in. high-resolution mask*, J. Vac. Sci. Technology, Vol. B15(1), Jan/Feb 1997	Jan/Feb 1997	Jan/Feb 1997	"Gu"
	Qizhi He, et al., *Inorganic antireflective coating process for deep-UV lithography*, Proc. SPIE 3334, Optical Microlithography XI (June 29, 1998)	June 29, 1998	June 29, 1998	"He"
	Laurence Stuart Hordon, *Ultra-low energy electron optics for lithography and microscopy*, Ph.D. dissertation, Stanford University (1994)	1994	1994	"Hordon"

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
	U.S. Pat. No. 6,291,361	Mar. 24, 1999	Sept. 18, 2001	"Hsia"
	Japanese Patent Publiction. No. JPH0482217	July 24, 1990	Mar. 16, 1992	"JP'217"
	U.S. Pat. No. 7,087,962	May 3,1995	Aug. 8, 2006	"Codama"
	Japanese Patent Publication No. JPH0722396	June 23, 1993	Jan. 24, 1995	"JP'396"
	Wei W. Lee, et al., *ARC for Sub-0.18μm Logic and Gigabit DRAM Frontend and Backend Processes*, IEEE Symposium on VLSI Technology Digest of Technical Papers (1998)	1998	1998	"Lee (IEEE)"
	Carol Lee, et all., *Feasibility of a CVD-resist-based lithography process at 193-nm wavelength*, Proc. SPIE 3333, Advances in Resist Technology and Processing XV (June 29, 1998)	June 29, 1998	June 29, 1998	"Lee (SPIE)"
	Mike Nault, et al., *Single layer chemical vapor deposition photoresist for 193 nm deep ultraviolet photolithography*, J. Vac. Sci. Technology, Vol. B16(6) (Nov/Dec 1998)	Nov/Dec 1998	Nov/Dec 1998	"Nault"
	G. M. Wallraff and W.D. Hinsberg, *Lithographic Imaging Techniques for the*	June 25, 1999	June 25, 1999	"Wallraff"

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
	Formation of Nanoscopic Features, Chem. Rev. 1999, Vol. 99, No. 7 (June 25, 1999)			
	Johannes van Wingerden, *Optimization of substrate reflectivity resist thickness and resist absorption for CD control and resolution*, Proc. SPIE 3679, Optical Microlithography XII (July 26, 1999)	July 26, 1999	July 26, 1999	"Wingerden"
	U.S. Pat. No. 6,358,670	Dec. 28, 1999	Mar. 19, 2002	"Wong II"
	Qi Xiang, et al., *Sub-100-nm and deep sub-100-nm MOS transistor gate patterning*, Proc. SPIE 3506, Microelectronic Device Technology II (September 4, 1998)	Sept. 4, 1998	Sept. 4, 1998	"Xiang"
	U.S. Pat. No. 5,962,195	Sept. 10, 1997	Oct. 5, 1999	"Yen"

2. Obviousness Combinations

A person having ordinary skill in the art would have been motivated to combine the teachings of any of the references described in attached Exhibits H1-H9, including for the reasons described below. A person having ordinary skill in the art at the time of filing of the asserted patent would also have understood the references listed above, alone or in combination, to contain explicit and/or implicit teachings, suggestions, and/or rationales to combine their teachings, including as further described below.

The references identified in Exhibits H2-H8 provide interrelated teachings related to methods of forming circuit structures that are smaller than what was purportedly achievable at the time by conventional UV lithographic techniques using a hardmask layer positioned between a resist layer and a device layer (such as polysilicon) and a three-step etching process for trimming the hardmask by (1) anisotropically etching exposed portions of the hardmask layer; (2) isotropically etching subsequently the hardmask layer underneath the resist mask to form a hardmask having a final linewidth which is narrower than the initial line width of the resist mask and corresponds to a desired structure linewidth; and (3) anisotropically etching the device layer as defined by the hardmask to form a structure having a width substantially equal to the final linewidth of the hardmask, as claimed in independent claim 1. *See, e.g.*, Brueck at 2:52-63, 4:14-29, 4:63-5:20, Figs. 1A-H; Chapman at 1:57-61, 5:40-41, 5:49-52, 5:63-65, Figs. 8(d)-8(e); Chen at 3:57-4:64, Figs. 2-4; Laaksonen at 1:52-67, 2:34-53, 3:30-34, 3:34-66, 4:18-19, 4:33-35, Figs. 5-6; Rogers at 2:29-3:64, 4:44-48, Figs. 1-6; Yang at 4:13-36, 5:5-27, Figs. 2(a)-2(b); Yu at 2:13-22, 2:47-51, 3:36-58, 4:57-5:39, Figs. 1-3, Figs. 8-10. Each of these references discloses, either expressly or inherently, every element of one or more Asserted Claims, thereby anticipating those claims.

To the extent that any of the references charted in these Preliminary Invalidity Contentions does not disclose "isotropically etching subsequently the hardmask layer underneath the resist mask to form a hardmask having a final linewidth which is narrower than the initial line width of the resist mask and corresponds to a desired structure linewidth," it would have been obvious to combine that reference with, for example, AAPA, Linliu, JP'217, or JP'396. *See, e.g.*, '097 patent at 3:17-23 ("The trim etch process includes isot[r]opically etching away a portion (the area outside of the dotted line 24) of the resist mask 20 so as to reduce simultaneously the thickness with the

lateral dimension until a final resist mask 26 is obtained. This is depicted in FIG. 1(c) in which a final linewidth 26 is produced corresponding to approximately the desired gate linewidth."), Fig. 1(c); Linliu at 8:40-44 ("[A]lthough it is not specifically illustrated within FIG. 3, it is also possible within the method of the present invention that the patterned focusing layer 20a may be undercut with respect to the etched patterned photoresist layer 22a'."), 9:14-18 ("[T]he patterned focusing layer 20a is etched from the blanket focusing layer 20 for a time period which includes an over-etch of from about 50 to about 70 percent with respect to an endpoint . . . ."); JP'217 at ¶ 1 ("By removing the object by the isotropic etching, the etching mask pattern is formed so as to form the etching object pattern having a size smaller than that of the etching mask pattern without causing damage to the substrate surface."); JP'396 at ¶ 9 ("[T]he present inventor is isotropic to the material film directly under the etching mask among the material films constituting the multilayer film. It was considered to etch the underlying material film using the above mentioned materials film having a narrowed pattern width as a mask after removing the etching mask by inserting an undercut under various etching conditions to narrow the patter width."). A person of ordinary skill in the art at the time of the alleged invention would have been motivated to employ an isotropic etch to etch the hardmask layer because, for example, the process was known in the art as a method for further narrowing mask patterns beyond the pattern achieved by resist exposure alone.

To the extent that any of the references charted in these Preliminary Invalidity Contentions does not disclose a method of forming circuit structures "wherein the device layer is formed of silicon," it would have been obvious to combine that reference with, for example, AAPA, Lee, or Cirelli. *See, e.g.*, '097 patent at 2:67-3:1 ("Typically, the gate conductive layer 16 is a layer of polycrystalline silicon . . . ."), Fig. 1(a); Lee at 131 ("We report fabrication of sub-0.1μm poly-Si gates using conventional DUV lithography with an optimized $Si_xO_yN_z$ film"), Cirelli at 4233

("Samples were prepared with ARC/160 nm oxide hard mask over a WSi_x /poly gate stack . . . ."). A person of ordinary skill in the art at the time of the alleged invention would have been motivated to use silicon for the device layer because, for example, it was a known material used for semiconductor device fabrication and its use would have accomplished the predictable result of allowing the creation of conductive circuit structures such as transistor gates.

For the same reasons, to the extent that any of the references charted in these Preliminary Invalidity Contentions does not disclose a method of forming circuit structures wherein the device layer is formed of silicon and "wherein the silicon has a thickness between 500 Å to 5000 Å," it would have been obvious to combine that reference with, for example, AAPA, Fukuda, Codama, Lee (SPIE), or Nault. *See, e.g.*, '097 patent at 2:67-3:2 ("Typically, the gate conductive layer 16 is a layer of polycrystalline silicon having a thickness between 500 Å to 5000 Å."); Fukuda at 7:21-22 ("[A] poly Si layer 3 and a refractory metal silicide layer 2 are formed in this order on an oxide film bed 4, ..."), 7:58-60 ("[A]n n+ poly Si layer 3 having the thickness of, for instance, 100 nm is formed on the gate oxide film bed 4 . . . ."); Codama at 5:48-49 ("After a passivation film was formed on a glass substrate 1, an amorphous silicon film 2 was formed in 1000 Å thick . . . ."); Lee (SPIE) at 626 ("Studies using the single-layer hardmask implementation were performed using wafers that were coated with 500Å CVD oxide, followed by 2500Å amorphous-Si, followed by at 1500Å thick layer of PPMS."); Nault at 3733 ("As a demonstration of this application, 1500 Å of CVD resist was used to pattern 2500 Å polysilicon over 500 Å oxide.").

To the extent that any of the references charted in these Preliminary Invalidity Contentions does not disclose a method of forming circuit structures "wherein the ultra-thin resist layer has a thickness of less than 2500 Å," it would have been obvious to combine that reference with, for example, AAPA, Rao, Wong, Nguyen, Wang, Hause, Azuma, Hordon, Lee (SPIE), or Nault. *See,*

e.g., '097 patent at 3:38-40 ("As can be seen in FIG. 2(a), an UTR layer 18a has a thickness of less than 2500 Å as compared to the thicker resist layer 18 of FIG. 1(a)."), Fig. 2(a); Rao at 626 ("We have been able to demonstrate that the use of ultra-thin resists (1000 Å) can be effective for EUV lithography"); Wong at 2:13-15 ("Polyhydroxystyrene based resists can be used in top surface imaging application in which a very thin (~500 Å) layer of resist is required to be transparent at the ArF wavelength."); Nguyen at 3039, Wang at 5:14-15 ("Ultra-thin photoresists in accordance with the present invention have a thickness of about 2,000 Å or less . . . ."); Hause at 4:16-17 ("[P]hotoresist layer 114 has a thickness of merely 2000 angstroms."); Azuma at 4251 ("[T]he thinner resist process could provide more advantages not only in lithography process but also in etch process."); Hordon at 33 ("The film thickness was precisely controlled by the number of deposition cycles . . . . The PMMA films consisted of 5 monolayers (4.5nm) or 17 monolayers (14nm), while the poly(vinyl cinnamate) films comprised 11 monolayers (10nm)."); Lee (SPIE) at 626 ("Studies using the single-layer hardmask implementation were performed using wafers that were coated with 500Å CVD oxide, followed by 2500Å amorphous-Si, followed by at 1500Å thick layer of PPMS."); Nault at 3733 ("As a demonstration of this application, 1500 Å of CVD resist was used to pattern 2500 Å polysilicon over 500 Å oxide."). A person of ordinary skill in the art at the time of the alleged invention would have combined the references because, for example, ultra-thin photoresist layers were known in the art to replicate image patterns more accurately than thicker photoresist layers. *See, e.g.*, Hause at 2:40-50; '097 patent at 1:32-39.

To the extent that any of the references charted in these Preliminary Invalidity Contentions does not disclose a method of forming circuit structures "wherein the hardmask is made of an inorganic material," it would have been obvious to combine that reference with, for example, Lin, Lee, Armacost, Cirelli, Wang, He, Wallraff, or Wingerden. *See, e.g.*, Lin at 186; Lee at 131;

Armacost at 44; Cirelli at 4229; Wang at 5:1-3 ("The silicon nitride layer 18 has a thickness suitable for functioning as a hard mask for etching the underlying oxide layer."); He at 338 ("The inorganic ARC film can not only function as an ARC layer, but also serve as a hardmask for the pattern transfer etch process. The hardmask function offered by $Si_xO_yN_z$ ARC is crucial and beneficial to the fabrication of continuously scaled process features."); Wallraff at 1808 ("After patterning the thin resist layer, the image is transferred to the underlying inorganic film which is employed as a "hardmask" in the subsequent substrate etch."); Wingerden at 905 ("[T]he use of inorganic BARC as a hard mask for etching allows for a thinner resist layer. This reduction of the resist thickness is advantageous for obtaining high resolution."). A person of ordinary skill in the art at the time of the alleged invention would have combined the references because inorganic hardmask materials were compatible with commonplace manufacturing processes and able to be tuned to the underlying substrate to optimize antireflective properties. *See, e.g.*, Cirelli at 4230. Inorganic hardmasks were also known in the art and would have been used to achieve the predictable result of being trimmed to allow for etching an underlying layer to a reduced linewidth.

For the same reasons, to the extent that any of the references charted in these Preliminary Invalidity Contentions does not disclose a method of forming circuit structures wherein the hardmask is made of an inorganic material and "wherein the inorganic material is one of silicon dioxide, silicon nitride, silicon oxynitride, and titanium nitride," it would have been obvious to combine that reference with, for example, Lin, Lee, Armacost, Cirelli, Wang, He, Lee (IEEE), Wingerden, or Xiang. *See, e.g.*, Lin at 187; Lee at 131; Armacost at 60; Cirelli at 4230; Wang at 5:1-3 ("The silicon nitride layer 18 has a thickness suitable for functioning as a hard mask for etching the underlying oxide layer."); He at 338 ("The inorganic ARC film can not only function as an ARC layer, but also serve as a hardmask for the pattern transfer etch process. The hardmask

function offered by SixOyNz ARC is crucial and beneficial to the fabrication of continuously scaled process features."); Lee (IEEE) at 86 ("The $Si_xO_yN_z$ film has dual functions: reducing substrate reflectivity to a minimum and serving as a hardmask for poly and metal etch."); Wingerden at 905; Xiang at 244 ("SiON BARC was found essential for patterning sub-100nm poly gates with a nearly vertical profile, for it played a role of "hard mask" as well.").

To the extent that any of the references charted in these Preliminary Invalidity Contentions does not disclose a method of forming circuit structures "wherein the hardmask is made of an organic material," it would have been obvious to combine that reference with, for example, Linliu, Lee, Armacost, Cirelli, Ko, Wingerden, or Yen. *See, e.g.*, Linliu at 7:18-20 ("With respect to the blanket focusing layer 20, the blanket focusing layer 20 is formed from an organic anti-reflective coating (ARC) material . . . ."); Lee at Fig. 10(b); Armacost at 45 ("[O]rganic ARC etching can be considered the forerunner of more elaborate lithographic and dielectric etch options . . . ."); Cirelli at 4229 ("Organic bottom ARC materials are the most common and widely used of all of antireflective schemes . . . ."); Ko at 209 ("[T]he application of organic BARC would enhance the manufacturability of devices with geometry of 0.35 μm and below."); Wingerden at 905; Yen at 3:55-59 ("To practice the method of the present invention, there is first provided a substrate having formed thereover a blanket target layer. There is then formed upon the blanket target layer a blanket focusing layer formed from an organic anti-reflective coating (BARC) material, ..."). A person of ordinary skill in the art at the time of the alleged invention would have combined the references because, for example, the use of organic hardmask materials was common for an antireflective scheme. *See, e.g.*, Cirelli at 4229. Organic hardmasks were also known in the art and would have been used to achieve the predictable result of being trimmed to allow for etching an underlying layer to a reduced linewidth.

For the same reasons, to the extent that any of the references charted in these Preliminary Invalidity Contentions does not disclose a method of forming circuit structures wherein the hardmask is made of an organic material and "wherein the organic material is a bottom anti-reflective coating," it would have been obvious to combine that reference with, for example, Armacost, Cirelli, Ko, or Wingerden. *See, e.g.*, Linliu at 7:18-20 ("With respect to the blanket focusing layer 20, the blanket focusing layer 20 is formed from an organic anti-reflective coating (ARC) material . . . ."); Lee at Fig. 10(b); Armacost at 44 ("The configuration most commonly used in the industry is the absorptive, organic, underlying antireflective coating ("bottom antireflective layer," or BARL)."); Cirelli at 4229 ("Organic bottom ARC materials are the most common and widely used of all of antireflective schemes . . . ."); Ko at 209 ("[T]he application of organic BARC would enhance the manufacturability of devices with geometry of 0.35 μm and below."), Wingerden at 905. Organic BARC layers were known in the prior art and would have been used to achieve the predictable result of being trimmed to allow for etching an underlying layer to a reduced linewidth.

To the extent that any of the references charted in these Preliminary Invalidity Contentions does not disclose a method of forming circuit structures "wherein the hardmask layer has a thickness between 50 Å to 500 Å," it would have been obvious to combine that reference with, for example, Lin, Lee, or Cirelli. *See, e.g.*, Lin at 186 ("Conventional single layer SiON BARC (300A~500A) on poly; . . . ."); Lee at Fig. 3 ("[O]ptimal ARC thickness at 290Å . . . ."); Cirelli at Fig. 3. A person of ordinary skill in the art at the time of the alleged invention would have combined the references because, for example, hardmask thickness control was known to be a significant factor in optimizing antireflective properties and obtaining good photo performance. *See, e.g.*, Lin at 186. Also, a person of ordinary skill in the art would have wanted to retain the

photoresist residue liftoff benefits associated with the BARC hardmask having a thickness of 500Å. *See, e.g.*, Chapman at 6:14-16, 6:35-38. Finally, using a thinner hardmask layer would have improved manufacturing efficiency by decreasing the amount of time required for both deposition and etch of the hardmask. *See, e.g.*, Laaksonen at 3:30-66.

To the extent that any of the references charted in these Preliminary Invalidity Contentions does not disclose a method of forming circuit structures "further comprising the step of exposing the resist layer to a UV bake prior to the step of isotropic over-etching so as to enhance selectivity to the hardmask layer," it would have been obvious to combine that reference with, for example, Becker, Wong, Huang, Krisa (SPIE), Krisa (ME), Hyrniewicz, or Jeoung. *See, e.g.*, Becker at 427 ("One way to improve the performance of the resist is to apply a stabilization process to the resist prior to subsequent steps where the resist is used as a mask . . . . In this study electron beam stabilization is evaluated and compared with a more conventional UV-bake process . . . . The UV-bake process considered was the process of record in an existing production process flow."); Wong at 8:29-36 ("After removal of the coated wafers from the developing solution, an optional, although not required, post-development heat treatment or bake may be employed to increase the adhesion of the coating as well as resistance to etching solutions and other substances."); Huang at 135 ("UV baking has been accepted as one of the effective methods to improve etch resistance of DUV PR."); Krisa (SPIE) at 5 ("Improvement of selectivity was accomplished by the addition of a UV bake . . . ."); Krisa (ME) at 209 ("A combination of improving the etch selectivity and implementing a stabilization process with DUV resists allows the use of thinner resist. We demonstrate improvements in etch selectivity at the contact level using UV/Bake™ stabilization of the resist films."); Hryniewicz at 89 ("Hardening processes for resist commonly involve baking . . . and/or exposure to hard UV radiation."); Jeoung at 9:36-40 ("[T]he photoresist pattern is UV

baked (S32), the photoresist pattern is irradiated with a UV light applying heat, and Cross Linking reaction occurs inside the photoresist so that the thermal stability of the photoresist pattern is improved, ...”). A person of ordinary skill in the art at the time of the alleged invention would have combined the references because, for example, UV baking was a conventional photoresist stabilization process used in semiconductor manufacturing and known to improve etch resistance and result in a more accurate etch (*i.e.*, more vertical walls and a decrease in “footing”). *See, e.g.*, Becker at 428-29.

To the extent that any of the references charted in these Preliminary Invalidity Contentions does not disclose a method of forming circuit structures “further comprising the step of curing the resist layer by an electron beam prior to the step of isotropic over-etching so as to enhance selectivity to the hardmask layer,” it would have been obvious to combine that reference with, for example, Becker, Wong, or Wong II. *See, e.g.*, Becker at 428 (“The electron interaction with the resist material [during electron beam stabilization] creates radicals that can then rearrange and crosslink, effectively increasing the molecular weight of the material. This improves the thermal stability and enhances the etch resistance of the resist.”); Wong at 3:1-6 (“It has now been found according to the present invention, that subjecting a developed photoresist to electron beam irradiation, a resist image is produced which is still sufficiently transparent for radiation with a wavelength of approximately 193 nm and which is now sufficiently stable to permit plasma etching.”); Wong II at 2:46-48 (“[T]he etch resistance of image-wise exposed and developed photoresists may be increased by an overall flood exposure with an electron beam.”). A person of ordinary skill in the art at the time of the alleged invention would have combined the references because, for example, electron beam curing was another known photoresist stabilization process

proven to increase etch resistance and result in more accurate etching. *See, e.g.*, Becker at 428-29.

To the extent that any of the references charted in these Preliminary Invalidity Contentions does not disclose a method of forming circuit structures "wherein the hardmask layer is formed of a multi-layer material," it would have been obvious to combine that reference with, for example, Lin, Armacost, Cirelli, Wang, or Hsia. *See, e.g.*, Lin at 188 ("Fig. 5 shows the substrate reflectivity as function of hard mask thickness with optimum dual layer BARC. It is seen that with the optimum dual layer BARC, substrate reflectivity is minimum (less than 0.006) with any range of oxide hard mask thickness."); Armacost at Fig. 28; Cirelli at 4231 ("The multilayer ARC stack is deposited using a standard production PE-CVD deposition tool either alone or in combination with an SiO_2 hard mask."); Wang at 8:25-29 ("The patterned oxide layer 16a and 16b serves as an etch hard mask layer for processing or etching the underlying metal layer 12 and/or as part of a hard mask in combination with the patterned silicon nitride layer 18a and 18b for etching the underlying metal layer 12."); Hsia at 5:23-27 ("[P]rior art processing paradigms often employ a stacked metal layer 302, for example comprising a middle metal layer 314 sandwiched between a top anti-reflective coating (ARC) layer 312, and a bottom thin film barrier layer 316."), 5:48-52. A person of ordinary skill in the art at the time of the alleged invention would have combined the references because, for example, the near-zero reflectivity achievable through multilayer hardmasks would have improved accuracy achieved during lithography and increased control during the etching processes. Additionally, multilayer hardmasks would have reduced the need for strict layer thickness control during fabrication, which simplifies the manufacturing process. *See, e.g.*, Lin at 196.

For the same reasons, to the extent that any of the references charted in these Preliminary Invalidity Contentions does not disclose a method of forming circuit structures wherein the hardmask layer is formed of a multilayer material and "wherein the multi-layer material consists of a top anti-reflective layer and a bottom etchstop layer," it would have been obvious to combine that reference with, for example, Lin, Armacost, Cirelli, Wang, or Hsia. *See, e.g.*, Lin at 186-87 ("The design of dual layer BARC is: the top layer serves as the phase shift cancellation layer and the bottom layer serves as the light absorption layer with high k value (>1.0) . . . The hard mask can be oxide or nitride . . . ."); Armacost at 45 ("Dielectric etching applications typically rely on . . . etchstopping on underlying layers."); Cirelli at 4231 ("To illustrate the effectiveness of the multilayer approach, simulations were run with . . . a sample that included an additional layer of 75 nm oxide between the ARC and silicon . . . ."); Wang at 6:39-47 ("The developer is selected so that it does not degrade or etch the material of the silicon nitride layer 18, or at least degrades or etches the material of the silicon nitride layer 18 at a relatively smaller rate as compared to the rate that the material of the ultra-thin photoresist layer 20 is developed. In other words, the silicon nitride layer 18 serves as an etch-stop layer when developing the ultra-thin photoresist layer 20."); Hsia at 5:23-27, 5:48-52 ("Further, in an effort to protect the integrity of patterned microelectronic structures produced using thin photoresist pattern layers, prior art practice has utilized an oxide layer prior to the organic ARC layer to provide hardmask protection.").

For the same reasons, to the extent that any of the references charted in these Preliminary Invalidity Contentions does not disclose a method of forming circuit structures wherein the hardmask layer is formed of a multi-layer material consisting of a top anti-reflective layer and a bottom etchstop layer and "wherein the top anti-reflective layer is formed of a nitride film," it would have been obvious to combine that reference with, for example, Lin, Cirelli, or Hsia. *See,*

e.g., Lin at 190, "[D]ual SiON BARC were deposited with PECVD on top of 2.25kA oxide hard mask."); Cirelli at 4230 ("A method which is increasing in popularity and has shown great promise is the use of inorganic bottom antireflective layers. These are films made up of silicon rich nitrides or oxy-nitrides . . . ."); Hsia at 5:40-42 ("Initial ARC layers, for example, such as ARC layer 312, are made from a metallic material, for example titanium nitride, often referred to as tinitride.").

To the extent that any of the references charted in these Preliminary Invalidity Contentions does not disclose a method of forming circuit structures "wherein the resist mask used in the isotropic etching step is maintained on top of the hardmask during the anisotropic etching step of the device layer," it would have been obvious to combine that reference with, for example, Wang. *See, e.g.*, Wang at 8:62-66 ("Referring to FIG. 7, the patterned photoresist 20a and 20b (not shown), if still present, the patterned silicon nitride layer 18a and 18b (not shown), if still present, and the patterned oxide layer 16a and 16b (not shown) are then stripped or removed from the substrate."); Chapman at 5:63-64; Laaksonen at Figs. 5-6. A person of ordinary skill in the art at the time of the alleged invention would have combined the references because, for example, there were only two possible options for dispositioning the photoresist after the isotropic hardmask etch and before etching an underlying layer: (1) maintain it or (2) remove it. Depending on the material to be etched and the etch chemistry, both approaches would have led to the same predictable result of an underlying layer being successfully etched to a linewidth narrower than achievable by conventional UV lithography.

The combinations of references provided above are exemplary and are not intended to be exhaustive. Additional obviousness combinations of the references identified here are possible, and Defendant may rely on such combination(s) in this litigation. In particular, Defendant is currently unaware of Ocean's allegations with respect to the level of skill in the art and the

qualifications of the typical person of ordinary skill in the art. Defendant is also unaware of the extent, if any, to which Ocean may contend that limitations of the claims at issue are not disclosed in the prior art identified by Defendant as anticipatory, and the extent to which Ocean will contend that elements not disclosed in the asserted patent specifications would have been known to persons of skill in the art. And Defendant does not yet know how the Court will construe terms in the asserted claims. Defendant is also continuing its investigation of the large universe of prior art to identify potential prior art systems, publications related to those systems, and third parties that may have information about those systems, including potential prior art systems relating to AMD, IBM, and/or any of the prior art references discussed in this section. Ocean may also be in possession of prior art that Defendant may receive after discovery opens in this case. Defendant reserves the right to amend and supplement these contentions to identify other prior art and combinations rendering the asserted claims obvious.

i. The ’170 Patent

1. Identification of Prior Art

The tables below list prior art that anticipates and/or renders obvious one or more of the asserted claims. The attached claim charts in Exhibits I1-I14 demonstrate where each limitation of the claims is found in certain of the references listed below, either expressly or inherently in the larger context of the passage, as understood by a person having ordinary skill in the art. The following patents, publications, products and/or services are prior art under at least 35 U.S.C. §§ 102(a), (b), or (e).

a. Prior Art Patents, Patent Publications, and Non-Patent Publications To The Asserted Claims of the '170 Patent.

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
I1	TWI 233679 B	May 20, 2003	June 1, 2005	Chuang
I2	JP 9/293808	April 25, 1996	November 11, 1997	Akai
I3	JP 2000/232260	February 9, 1999	August 22, 2000	Ogawa
I4	US 6,313,521 B1	November 3, 1999	November 6, 2001	Baba
I5	US 6,407,334 B1	November 30, 2000	June 18, 2002	Jimarez
I6	US 6,903,278 B2	June 29, 2001	June 7, 2005	Sathe
I7	US 7,045,890	September 28, 2001	May 16, 2006	Xie
I8	US 6,214,640 B1	August 3, 1999	April 10, 2001	Fosberry
I9	US Pub. No. 2004/0105241 A1	December 3, 2002	June 3, 2004	Ranade
N/A	JP2002-329839	September 14, 2001	November 15, 2002	Maruyama
N/A	JP2004-328505	April 25, 2003	November 18, 2004	Horie
N/A	US 2003/0104652 A1	December 3, 2001	June 5, 2003	LaBonheur
N/A	JP8-306820	April 28, 1995	November 22, 1996	Haga
N/A	JP2001-274628	March 23, 2000	October 5, 2001	Hirano
N/A	JP2004-072649	August 9, 2002	March 4, 2004	Harima 649
N/A	JP2004-088533	August 28, 2002	March 18, 2004	Harima 333
N/A	JP2005-217673	January 28, 2004	August 11, 2005	Miura 673
N/A	JP2005-217729	January 29, 2004	August 11, 2005	Miura 729
N/A	JP2006-147652	November 16, 2004	June 8, 2006	Aoki
N/A	US 5,471,027	July 22, 1994	November 28, 1995	Call
N/A	US 6,011,304	May 5, 1997	January 4, 2000	Metrol
I14	US 6,906,414	October 31, 2002	June 14, 2005	Zhao

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
N/A	US 7,443,016	October 13, 2005	December 28, 2008	Tsai
N/A	US 7,489,021	February 17, 2004	February 10, 2009	Juskey
N/A	US 7,566,591	October 31, 2005	July 28, 2009	Zhao
N/A	US 2002/0038913 A1	December 10, 2001	April 4, 2002	Farquhar
N/A	US 2002/0149027 A1	March 19, 1998	October 17, 2002	Takahashi
N/A	US 2002/016797 A1	March 12, 2002	November 14, 2002	DiStefano
N/A	US 2004/40174682 A1	May 19, 2003	September 9, 2004	Lin
N/A	US 2006/0087033 A1	February 3, 2004	April 27, 2006	Goh
N/A	US 4,748,495	August 8, 1985	May 31, 1988	Kucharek
N/A	US 5,050,039	June 26, 1990	September 17, 1991	Edfors
N/A	US 5,182,632	December 2, 1991	January 26, 1993	Bechtel
N/A	US 5,250,843	September 8, 1992	October 5, 1993	Eichelberger
N/A	US 5,471,366	July 28, 1994	November 28, 1995	Ozawa
N/A	US 5,589,711	December 28, 1994	December 31, 1996	Sano
N/A	US 5,717,245	March 24, 1995	February 10, 1998	Pedder
N/A	US 5,966,290	September 3, 1997	October 12, 1999	Sammakia
N/A	US 6,002,171	September 22, 1997	December 14, 1999	Desai
N/A	US 6,229,216	January 11, 1999	May 8, 2001	Ma
N/A	US 6,292,369	August 7, 2000	September 18, 2001	Daves
N/A	US 6,326,686	August 31, 1998	December 4, 2001	Baek
N/A	US 6,653,730	December 14, 2000	November 25, 20003	Chrysler
N/A	US 6,680,532	October 7, 2002	January 20, 2004	Miller

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
N/A	US 6,706,562	December 21, 2001	March 16, 2004	Mahajan
N/A	US 7,042,084	January 2, 2002	May 9, 2006	Takeuchi
N/A	US 5,909,056	June 3, 1997	June 1, 1999	Mertol
N/A	US 7,002,246 B2	July 2, 2004	February 21, 2006	Ho
N/A	US 7,166,9717 B2	January 5, 2005	January 23, 2007	Yang
N/A	US 2002/0171144 A1	May 7, 2001	November 21, 2002	Zhang
N/A	"Development of Very Thin (0.5 mmt) Transfer-molded TAB Packages" by Seung-Ho Ahn of Semiconductor Business, Samsung Electronics Co. and Yoshikatsu Maeda of Toray Industries Co.		December 1995	Ahn
N/A	"Development of Chip Scale Packages (CSP) for Center Pad Devices" by Masazumi Amagai, Hiroyuki Sano, Takayuki Maeda, Takahiro Imura, and Tadashi Saitohof the New Package Development (NDP) Dept., Texas Instruments Japan		May 1997	Amagai
N/A	"TBGA Package Technology" by Frank E. Andros and Richard B. Hammer, from IEEE Transactions on Components, Packaging, and Manufacturing Technology, Part B, Vol. 17, No. 4		November 1994	Andros

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
N/A	"Thermal Characterization of Cavity-Down TBGA Package with Flotherm Simulation" by Eric Cho of Flotrend Co, Eric Tan of Taiwan Semiconductor Technology Co., Yu-Tsai Lin, Associate Professor of the Mechanical Engineering Department at Yuan-Ze Yniversity, Taiwan, from the Sixteenth IEEE Semi-Therm Symposium		March 2000	Cho
N/A	"TBGA Substrate for Lead-Free and Halogen-Free Applications" by C Q Cui and Kelvin Pun of Compass Technology Co., Ltd., from the 2004 International IEEE Conference on Asian Green Electronics		September 2004	Cui
N/A	"Design and Optimization of High-Q RF Passives on SOP-Based Organic Substrates," by Sidharth Dalmia, Joseph Martin Hobbs, Venky Sundaram, Madhavan Swaminathan, Seock Hee Lee, Farrokh		May 2002	Dalmia

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
	Ayazi, George White and Swapan Bhattacharya, affiliated with the School of Electrical and Computer Engineering, Packaging Research Center, Georgia Institute of Technology and the Oelphi Automotive Systems Fellow, Delphi Packard Electric Systems, from the 2002 Electronic Components and Technology Conference			
N/A	"Thermal Performance of Tape Based Ball Grid Array Over Molded Packages," by Darvin Edwards and Paul Hundt of Texas Instruments, Inc. from the Fourteenth IEEE SEMI-THERM Symposium		March 1998	Edwards
N/A	"High-Performance Package Tape," by L. Fox, C. Davidson, and S. Hansen of the Manufacturing Design and Technology and K. Brown and A. Oscilowski of Semiconductor Operations of the Digital Equipment		1992	Fox

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
	Corpoation, from 1992 IEEE Publication			
N/A	"Development of a 4-Layer Low Cost Flip Chip Packaging Technology" by Anand Govind, and Farshad Ghahghahi of LSI Logi Corp from the 2003 Electronic Components and Technology Conference		May 2003	Govind
N/A	"Development of Organic Flip Chip Packaging Technology for Nanometer Silicon Incorporating Copper Metallization and Low-k Dielectric" by Anand Govind, and Farshad Ghahghahi of LSI Logi Corp from the 2004 Electronic Components and Technology Conference		2004	Govind
N/A	"Comparative Analysis of two heat spreader desims for a Wire Bond TBGA Package" by Satish C. Guttikonda', Bahgat G. Sammakia, Dept. of Mechanical Engineering, T.J.Watson School		2002	Guttikonda

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
	of Engineering, State University of New York at Binghamton, from the 2002 Inter Society Conference on Thermal Phenomena			
N/A	"Thermal & Electrical Performance and Reliability Results for Cavity-Up Enhanced BGAs," by Terry F. Hayden, Paul M. Harvey, Randy D. Schueller, and William J. Clatanoff of the 3M Electronic Products Division Laboratory from the 1999 Electronics Components and Technology Conference		1999	Hayden
N/A	"High Density BGA Substrates Fabricated by Laser Technologies" by Tadashi Hirakawa" and Fumitaka Sato of Fuji Machinery Mfg & Electronics CO , Ltd.		1997	Hirakawa
N/A	"Moisture Resistance Of Epoxy Resin Used For Extremely Low Profile Ic Modules" by Hiroki Hirayama, Norio Totsuka and Seigo Nambu of		1989	Hirayama

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
	Production Engineering Center, OK1 Electric Industry Co., Ltd. from the IEEE/CHMT '89 Japan IEMT Symposium			
N/A	"Understanding the Strength of Epoxy-Polyimide Interfaces for Flip-Chip Packages" by Pat Hoontrakul, Les H. Sperling, and Raymond A. Pearson from IEEE Transactions On Device And Materials Reliability, Vol. 3, No. 4, December 2003		December 2003	Hoontrakul
I14	"Viability of Anisotropic Conductive Film (ACF) as a Flip Chip Interconnection Technology" by K.M. Kim, J.O. Kim, S.G. Kim, K.H. Lee of ChipPAC Korea Co., Ltd. and A.S. Chen, N.Ahmad, N. Dugbartey, M. Karnezos, S.Tam, Y.D. Kweon, R. Pendse of ChipPAC, Inc. of 2000 Electronic Components and Technology Conference		2000	Kim

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
N/A	"Investigation of Thermal Enhancement on Flip Chip Plastic BGA Packages Using CFD Tool" by Tien-Yu (Tom) Lee, Associate Member, IEEE, from IEEE Transactions On Components And Packaging Technologies, Vol. 23, No. 3, September 2000		September 2000	Lee
N/A	"New Approach to Using Anisotropically Conductive Adhesives for Flip Chip Assembly," by Alan M. Lyons, Elizabeth E. Hall, Yiu-Hum Wong, and Gregory Adams of AT&T Bell Laboratories, a 1995 IEEE Publication		1995	Lyons
N/A	"High Frequency, High Power Miniature DC to DC Power Supply utilizing MCM-L Technology" by Greg Miller of Harris Semiconductor, Intelligent Power Products and Matt Salatino, of Harris Semiconductor Melbourne, Florida Advanced Packaging Technology		February 1996	Miller

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
N/A	"High Density Packaging for Mobile Terminals," by Seppo K. Pienimaa of Nokia Mobile Phones and Nigel I. Martin of Nokia Mobile Display Appliances, from 2001 Electronic Components and Technology Conference		2001	Pienimaa
N/A	"High-Density Packaging for Mobile Terminals" by Seppo K. Pienimaa and Nigel I. Martin, from IEEE Transactions On Advanced Packaging, Vol. 27, No. 3, August 2004		August 2004	Pienimaa
N/A	"A Numerical Study of the Thermal Performance of an Impingement Heat Sink—Fin Shape Optimization," byAmit Shah, Bahgat G. Sammakia, Hari Srihari, and Koneru Ramakrishna, Member, IEEE from from IEEE Transactions On Advanced Packaging, Vol. 27, No. 3, August 2004		August 2004	Shah
N/A	"Thermomechanical Reliability Assessment of Large		1998	Sylvester

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
	Organic Flip-Chip Ball Grid Array Packages," by Mark F. Sylvester, Donald R. Banks, Richard L. Kem, and Ronald G. Pofahl of W. L. Gore & Associates, Inc. from 1998 Electronic Components and Technology Conference			
N/A	"System-In-Package (SIP): Challenges and Opportunities" by King L. Tai of Bell Laboratories, a 2000 IEEE Publication		2000	Tai
N/A	"Performance Of Metal Ball Grid Array(Meta1 BGA) Package" by Hirofbmi Tanaka, Junsuke Tanaka, Moritsugu Morita and Hiroshi Waki of Mitsui Chemicals, Inc., of 1998 IEMT/IMC Proceeding		1998	Tanaka
N/A	"Chip-scale packaging," an August 1997 IEEE Spectrum publication		1997	Thompson II
I14	"Reliability Assessment of a Thin (Flex) BGA Using a Polyimide Tape Substrate," by Trent Thompson, Armando Carrasco and		1999	Thompson

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
	Andrew Mawer, of Motorola Semiconductor Products Sector, from 1999 IEEE/CPMT Int'l Electronics Manufacturing Technology Symposium			
N/A	"Parametric Studies of the Thermal Performance of Back-to-Back Tape Ball Grid Array (TBGA) Packages," by Sandeep S. Tonapi, Sanjeev B. Sathe, Bahgat G. Sammakia, K. Srihari1, of the Thomas J. Watson School of Engineering and Applied Science, State University of New York at Binghamton and the IBM Microelectronics Division, from the 2001 Electronic Components and Technology Conference		2001	Tonapi
N/A	"A Novel IMB Technology for Integrating Active and Passive Components," by R. Tuominen and J. K. Kivilahti, by 2000 IEEE		2000	Tuominen

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
I14	"Tape Ball Grid Array Package Analysis," by Y.P. Wang, and T.D. Her of Siliconware Precision Industries Co. Ltd., from 2000 Electronic Components and Technology Conference		2000	Wang
N/A	"Performance Enhanced Copper Core BGA," by Paul Wu, Kevin Chen, L.H. Ho of ProLinx Labs Corporation, and Manoj Nachnani of Enabling Solutions, Inc., from 1998 IEEE/CPMT Int'l Electronics Manufacturing Technology Symposium		1998	Wu
N/A	"A Transparent, High Barrier, and High Heat Substrate for Organic Electronics," by Min Yan, Tae Won Kim, Ahmet Gün Erlat, Matthew Pellow, Donald F. Foust, Jie Liu, Marc Schaepkens, Christian M. Heller, Paul A. Mcconnelee, Thomas P. Feist, And Anil R. Duggal, from Proceedings Of The IEEE, Vol. 93, No. 8, August 2005		August 2005	Yan

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
N/A	"Qualification of an Enhanced Ball Grid Array Package Using Build-up Layers on a Metal Heat Spreader," by LiG (Steve) Yang, Carl King and Ralph Doe of the Advanced Development Group, Intel Corporation, from the 2004 Electronic Component and Technology Conference		2004	Yang
N/A	"Optimizing Cost and Thermal Performance: Rapid Prototyping of a High Pin Count Cavity-Up Enhanced Plastic Ball Grid Array (EPBGA) Package," by Bret A. Zahn from ChipPAC Inc., from the Fifteenth SEMI-THERM Symposium		1999	Zahn
I14	"Frontmatter," *The Electronic Packaging Handbook*, edited by Blackwell, G.W., CRC Press LLC		2000	Blackwell
I14	"Technology Drivers," *Microelectronics Packaging Handbook*, Part 1, Second Edition, Edited by Rao R.		1997	Tummala

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
	Tummala, Eugene J. Rymaszewski, Alan G. Klopfenstein, Spring Science Business Media, B.V.			
I14	US 5,909,057	September 23, 1997	June 1, 1999	McCormick
I14	US 6,703,704	September 25, 2002	March 9, 2004	Alcoe
N/A	US 7,271,479	November 3, 2004	September 18, 2007	Zhao II
I14	US 6,284,569	May 10, 1999	September 4, 2001	Sheppard
I14	US 2005/0280139	June 21, 2004	December 22, 2005	Zhao III

b. Prior Art Systems/Services To The Asserted Claims of the '170 Patent.

Exhibit #	System/Service	Relevant Dates	Persons/Entities Involved in Prior Use, Sale, or Offers for Sale	Short Cite
I10	NVIDIA NV30, NV35, and NV38 based products, including at least the GeoForce FX 5800 (based on NV30)	Released on or around January 27, 2003	NVIDIA, its employees, and its customers	NVIDIA Cap Prior Art Products
I11	NVIDIA NV40, NV41, and NV45 based products, including at least the GeForce 6800 GT (PCIe) (based on NV45)	Released on or around April 24, 2004	NVIDIA, its employees, and its customers	NVIDIA Ring Prior Art Products
I12	ATI Radeon 8000 & 9000 series, including at least the ATI Radeon 9000 Pro	Released on or around August 1, 2002	ATI (which was subsequently acquired by AMD), its employees, and its customers	ATI Cap Prior Art Products

Exhibit #	System/Service	Relevant Dates	Persons/Entities Involved in Prior Use, Sale, or Offers for Sale	Short Cite
I13	ATI Radeon R300 series, including at least the ATI Radeon 9800 Pro	Released on or around March 1, 2003	ATI (which was subsequently acquired by AMD), its employees, and its customers	ATI Ring Prior Art Products

2. Obviousness Combinations

In *KSR International Co. v. Teleflex Inc.*, 550 U.S. 398 (2007), the United States Supreme Court clarified the standard for what types of inventions are patentable. The Supreme Court emphasized that inventions arising from ordinary innovation, ordinary skill, or common sense are not patentable. *Id.* at 415-27. In that regard, a patent claim may be obvious if the combination of elements was obvious to try or there existed at the time of the invention a known problem for which there was an obvious solution encompassed by the patent's claims. *Id*. at 417. In addition, when work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. *Id*. The Supreme Court recognized that if a person of ordinary skill can implement a predictable variation, Section 103 likely bars its patentability. *Id*.

All of the following rationales recognized in *KSR* support a finding of obviousness:

1. Combining prior art elements according to known methods to yield predictable results;
2. Simple substitution of one known element for another to obtain predictable results;
3. Use of known technique to improve similar devices (methods, or products) in the same way;
4. Applying a known technique to a known device (method, or product) ready for improvement to yield predictable results;

5. "Obvious to try"—choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;

6. Known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations would have been predictable to one of ordinary skill in the art; and

7. Some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

Certain of these rationales are discussed more specifically below. That others are not discussed more specifically should not be interpreted as an admission or concession that it does not apply. To the contrary, the discussion below simply provides more explanation of these specific rationales. Defendant may also rely on contemporaneous textbooks, treatises, and/or publications and/or on the testimony of fact and expert witnesses that bear on these rationales and on the reasons to combine the prior art.

Because the '170 Patent simply arranges old elements, with each performing the same function it had been known to perform and yields no more than what one would expect from such an arrangement, the combinations of these old elements are obvious. Further, in the prior art there were well recognized design needs and market pressures to develop the alleged invention claimed in the '170 Patent.

Those of ordinary skill in the art would have been (and indeed were) motivated to combine known prior art solutions in the manner claimed in the '170 Patent. Design needs and market pressures provided ample reason to combine prior art elements in the manner recited in the claims. Moreover, since there were a finite number of predictable solutions, a person of ordinary skill in

the art had good reason to pursue the known options. The prior art used those familiar elements for their primary or well-known purposes in a manner well within the ordinary level of skill in the art. A person of ordinary skill in the art would thus have had a reasonable expectation that the combination would succeed in producing the invention as claimed.

To the extent that any one of the anticipation references is found not to disclose a limitation recited in the asserted claims from the '170 Patent, it would have been obvious to one of ordinary skill in the art at the time of the alleged invention of the '170 Patent either (i) to modify the reference to include this limitation and any remaining limitations of this claim and any claim(s) from which this claim depends and/or (ii) to combine said reference with any other of the references in Exhibits I1-I14 and/or with a POSITA's general knowledge. Generally, motivation to combine any of these references with others exists within the references themselves, as well as within the knowledge of those of ordinary skill in the art at the relevant time. A person having ordinary skill in the art would have been motivated to combine any of the references described in attached Exhibits I1-I14, including for the reasons described below. A person having ordinary skill in the art at the time of filing of the asserted patents would also have understood the references listed above, alone or in combination, to contain explicit and/or implicit teaching, suggestion, and/or rationales to combine them, including as further described below.

The alleged invention of the '170 Patent relates to integrated circuit ("IC") package with substrate, chip, passive components (including specifically a "capacitor," as recited in claim 13), and stiffener. This configuration for an IC package was well known in the prior art before the alleged priority date of the '170 Patent. By definition, the purpose of an IC package is to package an IC. Thus, at a minimum an IC package must include the IC—*i.e.*, a chip—and a "substrate" on which to place the chip. Moreover, a person of ordinary skill would recognize the benefit of

including passive electronic components, such as decoupling capacitors, in the IC package. *See e.g.*, Dalmia et al., Design and Optimization of High-Q RF Passives on SOP-Based Organic Substrates, 2002 Electronic Components and Technology Conference, 495; Blackwell et al., The Electronic Packaging Handbook, 2000. Decoupling capacitors ensure the IC receives a steady voltage, which is key to proper IC operation. Blackwell et al., The Electronic Packaging Handbook, 2000 ("Large decoupling capacitors are also added between the power and ground planes for increased voltage stability."); *id.* ("Decoupling is also required to provide sufficient dynamic voltage and current level for proper operation of components during clock or at transitions when all component signal pins switch simultaneously under maximum capacitive load … Optimal implementation is achieved using a capacitor for a specific application: bulk, bypass, and decoupling."); *id.* ("Decoupling provides a localized point source charge, since finite inductance exists within the power supply network. By keeping the voltage level at a stable reference point, false logic switching is prevented."); Tummala et al., "Microelectornics Packaging Handbook," 2d ed., 1997 ("Electronic packages contain many electrical circuit components-up to several millions or even tens of millions-mainly transistors assembled in integrated circuit (IC) chips, but also resistors, diodes, capacitors, and other components."); *id*. ("One way to reduce this problem for off-chip paths is to use decoupling capacitors on card, board, module, and/or chip. … For on-chip circuits, the impact of decoupling capacitors is even more dramatic than for off-chip paths. Because the internal circuits are in parallel with either an on-chip or an on-module decoupling capacitor (or both, if they are present), there is an alternate source of local charge for the operation of these circuits and the instantaneous current does not have to flow through the Lerr of the package."). Decoupling capacitors store charge and will absorb additional charge in response to voltage increases and will provide charge in response to voltage decreases. Blackwell et al., The

Electronic Packaging Handbook, 2000 ("Decoupling capacitors ideally should be able to supply all the current necessary during a state transition of a logic device … The response of a decoupling capacitor is based on a sudden change in demand for current."). Thus, decoupling capacitors average out voltage from the IC's perspective, ensuring a more consistent voltage supply to the IC, and for at least that reason a person of ordinary skill would have been motivated to include them in any IC package, regardless of its design.

Including a stiffener with an IC was similarly well known prior to the '170 Patent. To make manufacturing more efficient and/or cheaper, one of ordinary skill would have been motivated to use thinner substrates with less material, which in turn are more prone to warping, and flexible substrates were also well known. '170 patent at 2:29-41 ("Background" section observing: "One advantage of thinner substrates is the ability to use smaller drill heads to perforate the substrate. The drilling of smaller holes means that less conductive material is needed to cover the interior of the hole and reduces undesirable impedance, saves manufacturing time, reduces waste, and is more cost effective. These advantages must be weighed against undesirable secondary effects such as warping of the surface of the substrate, difficulty of obtaining a stable surface, and weakening of the substrate during manufacturing operations. Thinner boards have lowered mechanical strength and impede the large scale industrialization of film-chip assemblies in a strip, matrix or array format."). Warping is a problem because it, e.g. negatively affects the connection of the IC to the substrate and in turn to the main board. Blackwell et al., The Electronic Packaging Handbook, 2000 ("Circuit board warpage is a fact of life that must be minimized for successful implementation of newer part packages. … [N]ewer large-area devices such as BGAs[] are extremely non-tolerant to board warp."); *id.* (identifying "[w]arped substrate" as one of the "[c]auses of solder bridges"). Adding a stiffener, such as a thin metal ring or cap, was a well-

known mechanism for addressing the well-known warping issue before the '170 Patent. Blackwell et al., The Electronic Packaging Handbook, 2000 ("Flexible Printed Board. A printed board using a flexible base material only. May be partially provided with electrically nonfunctional stiffeners and/or cover lay.").

Implementing the entire package as a flip-chip, ball-grid array was also well-known configuration. First of all, using flip-chip bonding, is one of only a limited set of options for connecting a chip or package to a substrate or board, was well known, and was understood to be the preferred approach for chips/packages that require many connections and/or where real estate is at a premium. Blackwell et al., The Electronic Packaging Handbook, 2000 ("Packaged components occupy a large percentage of real estate due to the fanout of the leadframe from the die bond pads to the solder bond pads. Direct attachment of bare die to a hybrid assembly saves space and is accomplished by wire bonding, TAB, and flip chip processes. … The ideal method for attaching bare die without giving up real estate to fan-out is by flip chip bonding."); *see also id.* (section titled "Flip Chip Benefits"). A designer would then similarly have to choose between the well-known options of connecting the chip or substrate using a ball-grid or pins, and either with an array or peripherals, all of which were well-known approaches, and one of ordinary skill would have known and understood the benefits of using a ball-grid array. Blackwell et al., The Electronic Packaging Handbook, 2000 ("More recently, ball grid array (BGA) packages and chip scale packages (CSP) have addressed the needs for higher I/O counts and higher-density hybrid circuits. The primary advantage of arrays over peripheral leads is the larger number of I/O per unit area."); Sathe at 3:1-9 ("While the following detailed description will describe example embodiments of the stiffener arrangements applied to thin-core substrates and coreless substrates in the context of an example flip chip (FC) pin grid array (PGA) arrangement (FC-PGA), practice

of the present invention is not limited to such context, i.e., practice of the present invention may have uses with other types of chips and with other types of mounting and packaging technologies, e.g., flip chip ball grid array (FC-BGA).").

Indeed, given these well-known issues and solutions, before 2006, companies (including NVIDIA, ATI, and Intel) were using the same IC package design claimed by the '170 Patent in publicly available, commercial products. For example, each of the following prior art systems and patents includes the limitations required by at least claim 1 of the '170 patent in at least the same configuration that Ocean is alleging falls within the scope of this claims in its preliminary infringement contentions: NVIDIA Ring Prior Art, NVIDIA Cap Prior Art, ATI Ring Prior Art, ATI Cap Prior Art, Chuang, Akai, Ogawa, Baba, Jimarez, Sathe, Xie, and Fosberry. The details of the disclosures are provided in the accompanying invalidity claim charts.

The types of substrates used in connection with IC packages, including use of "a polyimide tape substrate," as recited in claim 8, were well-known design choices. For example, as described in at least Thompson II, Ogawa, Jimarez, Fosberry, Thompson, Tummala, Blackwell, and Wang, various substrates for use in IC design and processing had well-known benefits and drawbacks, and one of ordinary skill would know to weigh these benefits and drawbacks when deciding what substrate to use. *See e.g.*, Thompson at 38 ("A flexible film, such as liquid-crystal polymer, unreinforced bismaleimaide triazine (BT) resin, or polyimide, serves as the package substrate."); Ogawa at [0047] ("First, an epoxy resin paste mixed with BaTiO3 powder is applied to the surface (upper surface in the figure) RFS of the resin film RF made of polyimide"); Jimarez at 2:2-5 ("The substrate 10 can be made of any conventional dielectric material, such as FR4, polyimide, polytetrafluoroethylene or other dielectric materials"); Fosberry at 5:34-39 ("semiconductor chip package assembly, generally designated as 10, includes a semiconductor chip 12 and a chip carrier

14. The chip carrier 14 is made up of a dielectric layer 16 (which may be flexible or rigid and is preferably made from a thin sheet of material such as polyimide)"); Tummala et al., "Microelectornics Packaging Handbook," 2d ed., 1997 (comparing various substrates ("carrier[s]"), and explaining that "[t]he flexible carrier … consists of two surface layers of thin-film copper wiring on each side of polymide or other polymeric film"); Blackwell et al., The Electronic Packaging Handbook, 2000 ("Glass reinforced polyimide is the next most used multilayer substrate material due to its excellent handling strength and its higher temperature cycling capability"). For example, at least the following prior art references disclose using a "polyimide tape substrate": Thompson et al., "Reliability Assessment of a Thin (Flex) BGA Using a Polyimide Tape Substrate," 1999 IEEE/CPMT Int'l Electronics Manufacturing Tech. Symposium at Abstract ("The fleXBGAm package is a thin package that uses polyimide tape as a substrate to reduce the overall package profile to 1.10 mm.");Ogawa at [0047] ("First, an epoxy resin paste mixed with BaTiO3 powder is applied to the surface (upper surface in the figure) RFS of the resin film RF made of polyimide"); Jimarez at 2:2-5 ("The substrate 10 can be made of any conventional dielectric material, such as FR4, polyimide, polytetrafluoroethylene or other dielectric materials"); Fosberry at 5:34-39 ("semiconductor chip package assembly, generally designated as 10, includes a semiconductor chip 12 and a chip carrier 14. The chip carrier 14 is made up of a dielectric layer 16 (which may be flexible or rigid and is preferably made from a thin sheet of material such as polyimide)"); Tummala et al., "Microelectornics Packaging Handbook," 2d ed., 1997 (comparing various substrates ("carrier[s]"), and explaining that "[t]he flexible carrier … consists of two surface layers of thin-film copper wiring on each side of polymide or other polymeric film"); Blackwell et al., The Electronic Packaging Handbook, 2000 ("Glass reinforced polyimide is the next most used multilayer substrate material due to its excellent handling strength

and its higher temperature cycling capability"); Wang at 1 ("This paper describes how high performance polyimide (PI) tape based materials are being utilized to increase routing density and improve the electrical and thermal performance.").

The specific stiffener thickness claimed, including a stiffener between 500 and 1000 microns thick (0.5 - 1 mm) and thinner than the chip, as recited in claims 10-11, was another design choice known in the art. *See e.g.*, Ogawa at [0050] ("The stiffener body 221 is formed of a substantially square-shaped copper plate having a thickness of 0.7 mm"); Sathe at 4:40-42 ("the die 120 may be, for example, in a thickness range of 0.6-0.9 mm, and typically may be 0.8 mm"). A person of ordinary skill would understand that there is no unexpected result from using a particular stiffener thickness, e.g., using 0.45 or 1.05 vs. 0.5-1 mm. At most, a person of ordinary skill would understand that the stiffener should not protrude beyond the height of the IC because doing so may waste space and decrease the thermal contact between the IC and a heat sink. This was all known well before the '170 Patent. For example, at least the NVIDIA Ring Prior Art, Ogawa, and Sathe disclose using a stiffener with the thickness required by claims 10-11.

Including "a heat sink is attached to a top side of the packaged integrated chip," as recited in claim 12, was another well-known component of IC packages or used in connection with the same. *See e.g.*, Chuang ("Fig. 1a and Fig. 1b show a typical fcBGA package 100. The package 100 comprises a chip 30, a substrate 40, a heat sink 10, a stiffener ring 20, and a plurality of passive components 80."); Akai at [0020] ("The semiconductor device 1 is a semiconductor device having a single chip, Ball Grid Array (BGA) structure, and generally includes a semiconductor chip 2, a circuit board 3, a heat radiating fin 4, bumps 5 for external connection, supporting members 6 that are the main part of the present invention, and other components."); Jimarez at 1:12-19 ("In the packaging of I/C chips, there has developed a need for a chip package that includes a cover plate

for the assembly, which cover plate is thermally conducting for heat transfer, and also electrically conducting for grounding the substrate, while preventing the chip itself from being electrically grounded to the cover plate, so that the cover plate can act as both a heat sink for the chip and also an electrical ground for the substrate."). A person of ordinary skill would understand that temperature control / ensuring for adequate cooling is an important design consideration in the semiconductor industry and including a heat sink (potentially along with a fan) is a well-known solution for achieving that result. Tellingly, at least the NVIDIA Ring Prior Art, NVIDIA Cap Prior Art, ATI Ring Prior Art, ATI Cap Prior Art, Akai, Chuang, Jimarez, Sathe, Xie, and Fosberry all disclose the use of a heat sink with an IC.

In sum, by the time the '170 Patent was filed, it was well known to design ICs as claimed at least because all the above was well known in the art before the '170 Patent, and persons of skill in the art would have known that any and/or all these above techniques could be combined to create an IC package with a substrate, chip, passive components, and stiffener. This is especially true here because all of the references disclose various aspects of IC designs, but may not disclose every aspect of an IC design to create a fully formed and functioning IC. As such, a person of skill in the art would have logically and predictably consulted all of the references together to design a complete IC. Furthermore, the general background knowledge described above and below would have provided the basis for combining any number of known IC package designs to create different IC packages. Because all of these techniques were already known in the art for use in IC package design, a person of skill in the art would have understood that combining any/all of these techniques would have yielded predictable results, would have been a simple substitution of one known technique for another to obtain predictable results, would have used known techniques to improve similar techniques in the same way, would have applied a known technique to a known

method that was ready for improvement to yield predictable results, would have been obvious to try because the techniques were all known and there was reasonable expectation of success in combining them, would have been obvious to try to improve IC package design, and would have been obvious because all techniques were already known and combined in various fashions before. With respect to the prior art references in Exhibits I1-I14, a person of ordinary skill in the art would have been motivated to combine any of the references identified as prior art to the '170 Patent for these reasons provided above, and the additional reasons provided below.

First, the prior art references identified above and the accompanying invalidity claim charts teach similar IC package designs (and within relevant timeframes), and thus the teachings of any one reference are applicable to other references in that same field. *See e.g.*, Sathe at 1:7-9 ("The present invention relates to arrangements to provide mechanical stiffening elements to a thin-core or coreless substrate."); Jimarez at 1:4-10 ("This invention relates generally to I/C chip mounting structures which include a substrate and an electrically and thermally conducting cover plate and a method of manufacturing the same. In even more particular aspects, this invention relates to an I/C chip assembly which electrically insulates the chip from the cover plate but provides grounding of the substrate to the cover plate."); Fosberry at 1:24-26 ("The present invention relates generally to a method of packaging a semiconductor chip or an array of such semiconductor chips."); Akai at [0001] ("The present invention relates to a semiconductor device, and more particularly to a semiconductor device in which a semiconductor chip is mounted on a substrate by using flip chip bonding technology."); Ogawa at [0001] ("The present invention relates to a wiring board and a stiffener provided with a stiffener and a capacitor, and a method for manufacturing the same, and more particularly to a wiring board and a stiffener having high rigidity, and a method for manufacturing the same."); Baba at 1:6-14 ("The present invention relates generally to a

semiconductor device in which one or more semiconductor chips and chip components are mounted on a substrate and a method of manufacturing the semiconductor device. More particularly, the present invention relates to a semiconductor device in which one or more semiconductor chips and chip components are mounted on a substrate and in which electrical short and coming away of the chip components from the substrate are avoided, and a method of manufacturing such semiconductor device."); Akai at [0001] ("The present invention relates to a semiconductor device, and more particularly to a semiconductor device in which a semiconductor chip is mounted on a substrate by using flip chip bonding technology"); Xie at 2:64-3:5 ("While the following detailed description will describe example embodiments of the IHS/IS arrangements applied to thin-core substrates and coreless substrates in the context of an example FC-PGA arrangement, practice of embodiments of the present invention is not limited to such context, i.e. practice of embodiments of the present invention may have uses with other types of chips and with other types of mounting and packaging technologies, e.g. flip chip ball grid array (FC-BGA) packages, interposers, etc."); Chuang at 1 ("The present disclosure relates to a flip-chip package module, and more particularly relates to a stiffener ring with an uneven contact surface and a heat sink. As the demand for lighter and more complex electronic devices increases, the speed and complexity of chips also increase accordingly. Semiconductor chips must provide more leads accordingly for the input and output of signals. Flip-Chip Ball Grid Array (fcBGA) Package is a known and advanced package."); Thompson et al., "Reliability Assessment of a Thin (Flex) BGA Using a Polyimide Tape Substrate," 1999 IEEE/CPMT Int'l Electronics Manufacturing Tech. Symposium at Abstract ("Wireless communication customers require thinner, smaller footprint packaging to allow for reductions in phone and paging product sizes. Currently, the thin MAP (Mold Array Process) BGA (Ball Grid Array) package is in production which converted from glob-

top BGA to reduce the overall package profile from 1.60 to 1.30 mm"). Given these similarities, a person of ordinary skill in the art would have recognized the compatibility between the teachings of the prior art references. As explained above, it was common to assemble IC packages in the semiconductor industry, and a person of ordinary skill in the art would have regarded the combination of teachings from different references as typical in the field.

Second, a person of ordinary skill in the art would have been motivated and found it obvious to apply references teaching certain specific techniques, e.g., use of capacitors as passive electronic components, use of polyimide tape substrate, use of specific stiffener thickness, and use of a heat sink to other references that relate to IC packages generally because all references teach IC package designs, and it would have been a trivial exercise to consult the references that taught more specific IC designs to fill in less specific disclosures in other references. *See e.g.*, Sathe at 1:7-9; Jimarez at 1:4-10; Fosberry at 1:24-26; Akai at [0001]; Ogawa at [0001]; Baba at 1:6-14 ("The present invention relates generally to a semiconductor device in which one or more semiconductor chips and chip components are mounted on a substrate and a method of manufacturing the semiconductor device. More particularly, the present invention relates to a semiconductor device in which one or more semiconductor chips and chip components are mounted on a substrate and in which electrical short and coming away of the chip components from the substrate are avoided, and a method of manufacturing such semiconductor device."); Akai at [0001]; Xie at 2:64-3:5; Chuang at 1; Thompson et al., "Reliability Assessment of a Thin (Flex) BGA Using a Polyimide Tape Substrate," 1999 IEEE/CPMT Int'l Electronics Manufacturing Tech. Symposium at Abstract. A person of ordinary skill in the art would have also been motivated and found it obvious to replace and/or combine a reference's exact set of materials, components, or configurations in a particular IC package with the teachings regarding other materials,

components, and configurations used in other IC packages for all the reasons provided above and below. These modifications would have been a simple substitution of one known element for another, which would have obtained predictable results because it was already well known in the art that multiple techniques of IC package design. The substitution of one component, material, or configuration for another would not have changed the principle of operation for either reference in any combination because the references all use similar mechanisms for a similar purpose: designing an IC package. This is thus a combination of prior art elements (e.g., passive components, substrate material, stiffener thickness, or use of a heat sink) according to known methods (a person of ordinary skill would understand that these are all available design choices) to yield predictable results (a person of ordinary skill would understand the benefits and drawbacks of each design choice, and there are no unexpected results from any particular combination). A person of ordinary skill in the art would have been motivated to combine these teachings, and to make these replacements, because all of these IC package components, materials, and configurations techniques were widely-used techniques. Accordingly, a person of ordinary skill in the art would have had a reasonable expectation of success given considerations discussed above, the similarities in the teachings and systems, and given that all the claimed IC package components, materials, and configurations were all well-known at the time. Implementing the combination and any necessary modifications would have been routine and within the scope of the prior art references' teachings.

As one example, to the extent that ATI Ring Prior Art, ATI Cap Prior Art, NVIDIA Ring Prior Art, Chuang, Baba, Sathe, or Xie does not disclose the "polyimide tape substrate" limitation of claim 8, it would have been obvious to combine any of these references with, e.g., Ogawa, Jimarez, Fosberry, or Thompson to arrive at said limitation because those references disclose such

limitation, and a person of ordinary skill would have been motived to consult references that disclose known options for substrate materials. Thompson at 38 ("A flexible film, such as liquid-crystal polymer, unreinforced bismaleimaide triazine (BT) resin, or polyimide, serves as the package substrate."); Ogawa at [0047] ("First, an epoxy resin paste mixed with BaTiO3 powder is applied to the surface (upper surface in the figure) RFS of the resin film RF made of polyimide"); Jimarez at 2:2-5 ("The substrate 10 can be made of any conventional dielectric material, such as FR4, polyimide, polytetrafluoroethylene or other dielectric materials"); Fosberry at 5:34-39 ("semiconductor chip package assembly, generally designated as 10, includes a semiconductor chip 12 and a chip carrier 14. The chip carrier 14 is made up of a dielectric layer 16 (which may be flexible or rigid and is preferably made from a thin sheet of material such as polyimide)"). It would have been obvious to use a "polyimide tape substrate" because this was a well-known material for use as a substrate (as shown by the foregoing references), and using this particular substrate would have been an obvious design choice that led to predictable results. Moreover, all of these references relate to IC package design, and thus a person of ordinary skill would have been motivated to look at Ogawa, Jimarez, Fosberry, or Thompson for substrate material design choices such as "polyimide tape substrate."

As another example, to the extent that ATI Ring Prior Art, ATI Cap Prior Art, Chuang or Fosberry do not disclose including a capacitor or other type of passive electronic component in an IC package, NVIDIA Ring Prior Art, NVIDIA Cap Prior Art, Akai, Ogawa, Baba, Jimarez, Sathe, and Xie disclose this limitation. *See, e.g.*, Exhibit J14; NVIDIA_OS_00003229 (showing "CHIP-CAP"); Akai at [0040] ("The electronic elements 18 are, for example, … chip capacitors … ."); Ogawa at [0004] ("chip capacitors CC are mounted by solder"); Baba at 6:47-67 (disclosing "chip components 7, such as … chip capacitors"); Jimarez at 2:40-51 (disclosing "capacitors 36"); Sathe

at 3:25-30 (disclosindie side components (DSCs) 140" such as "decoupling capacitors or resistors"); Xie at 3:10-33 (same); *see also* Blackwell et al., The Electronic Packaging Handbook, 2000 ("Large decoupling capacitors are also added between the power and ground planes for increased voltage stability."). For the same reasons one would include passive electronic components/capacitors in their IC packages (discussed above), one of ordinary skill would be motivated to also include passive components/capacitors in the ATI Ring Prior Art, ATI Cap Prior Art, Chuang or Fosberry, and including such components would have been a well-known design choice with predicable results because (as discussed above) it was common to include passive components in IC packages well before the '170 Patent at least because it was known to be desirable to use decoupling capacitors in IC packages.

Additional obviousness combinations of the references identified here are possible, and Defendant may rely on such combination(s) in this litigation. In particular, Defendant is currently unaware of Ocean's allegations with respect to the level of skill in the art and the qualifications of the typical person of ordinary skill in the art. Defendant is also unaware of the extent, if any, to which Ocean may contend that limitations of the claims at issue are not disclosed in the prior art identified by defendants as anticipatory, and the extent to which Ocean will contend that elements not disclosed in the asserted patent specifications would have been known to persons of skill in the art. And Defendant does not yet know how the Court will construe terms in the asserted claims. Defendant is also continuing its investigation of the large universe of prior art to identify potential prior art systems, publications related to those systems, and third parties that may have information about those systems. Ocean may also be in possession of prior art that Defendant may receive after discovery opens in this case. Defendant reserves the right to amend and supplement these contentions to identify other prior art and combinations rendering the asserted claims obvious.

j. The ’383 Patent

1. Identification of Prior Art

The tables below list prior art that anticipates and/or renders obvious one or more of the asserted claims. The attached claim charts in Exhibits J1-J17 demonstrate where each limitation of the claims is found in certain of the references listed below, either expressly or inherently in the larger context of the passage, as understood by a person having ordinary skill in the art. The following patents, publications, products and/or services are prior art under at least 35 U.S.C. §§ 102(a), (b), or (e).

a. Prior Art Patents, Patent Publications, and Non-Patent Publications To The Asserted Claims of the ’383 Patent.

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
J1	TWI 233679 B	May 20, 2003	June 1, 2005	Chuang
J2	JP9-293808	April 25, 1996	November 11, 1997	Akai
J3	JP2000-232260	February 9, 1999	August 22, 2000	Ogawa
J4	US 6,313,521 B1	November 3, 1999	November 6, 2001	Baba
J5	US 6,407,334 B1	November 30, 2000	June 18, 2002	Jimarez
J6	US 6,903,278 B2	June 29, 2001	June 7, 2005	Sathe
J7	US 7,045,890	September 28, 2001	May 16, 2006	Xie
J8	US 6,214,640 B1	August 3, 1999	April 10, 2001	Fosberry
J9	JP2002-329839	September 14, 2001	November 15, 2002	Maruyama
J10	JP2004-328505	April 25, 2003	November 18, 2004	Horie
J11	US 2003/0104652 A1	December 3, 2001	June 5, 2003	LaBonheur
J12	US Pub. No. 2004/0105241 A1	December 3, 2002	June 3, 2004	Ranade

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
N/A	JP8-306820	April 28, 1995	November 22, 1996	Haga
N/A	JP2001-274628	March 23, 2000	October 5, 2001	Hirano
N/A	JP2004-072649	August 9, 2002	March 4, 2004	Harima 649
N/A	JP2004-088533	August 28, 2002	March 18, 2004	Harima 333
N/A	JP2005-217673	January 28, 2004	August 11, 2005	Miura 673
N/A	JP2005-217729	January 29, 2004	August 11, 2005	Miura 729
N/A	JP2006-147652	November 16, 2004	June 8, 2006	Aoki
N/A	US 5,471,027	July 22, 1994	November 28, 1995	Call
N/A	US 6,011,304	May 5, 1997	January 4, 2000	Metrol
J17	US 6,906,414	October 31, 2002	June 14, 2005	Zhao
N/A	US 7,443,016	October 13, 2005	December 28, 2008	Tsai
N/A	US 7,489,021	February 17, 2004	February 10, 2009	Juskey
N/A	US 7,566,591	October 31, 2005	July 28, 2009	Zhao
N/A	US 2002/0038913 A1	December 10, 2001	April 4, 2002	Farquhar
N/A	US 2002/0149027 A1	March 19, 1998	October 17, 2002	Takahashi
N/A	US 2002/016797 A1	March 12, 2002	November 14, 2002	DiStefano
N/A	US 2004/40174682 A1	May 19, 2003	September 9, 2004	Lin
N/A	US 2006/0087033 A1	February 3, 2004	April 27, 2006	Goh
N/A	US 4,748,495	August 8, 1985	May 31, 1988	Kucharek
N/A	US 5,050,039	June 26, 1990	September 17, 1991	Edfors
N/A	US 5,182,632	December 2, 1991	January 26, 1993	Bechtel
N/A	US 5,250,843	September 8, 1992	October 5, 1993	Eichelberger
N/A	US 5,471,366	August 19, 1993	November 28, 1995	Ozawa

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
N/A	US 5,589,711	December 29, 1993	December 31, 1996	Sano
N/A	US 5,717,245	March 24, 1995	February 10, 1998	Pedder
N/A	US 5,966,290	September 2, 1997	October 12, 1999	Sammakia
N/A	US 6,002,171	September 22, 1997	December 14, 1999	Desai
N/A	US 6,229,216	January 11, 1999	May 8, 2001	Ma
N/A	US 6,292,369	August 7, 2000	September 18, 2001	Daves
N/A	US 6,326,686	August 31, 1998	December 4, 2001	Back
N/A	US 6,653,730	December 14, 2000	November 25, 20003	Chrysler
N/A	US 6,680,532	October 7, 2002	January 20, 2004	Miller
N/A	US 6,706,562	December 21, 2001	March 16, 2004	Mahajan
N/A	US 7,042,084	January 2, 2002	May 9, 2006	Takeuchi
N/A	US 5,909,056	June 3, 1997	June 1, 1999	Mertol
N/A	US 7,002,246 B2	July 2, 2004	February 21, 2006	Ho
N/A	US 7,166,9717 B2	January 5, 2005	January 23, 2007	Yang
N/A	US 2002/0171144 A1	May 7, 2001	November 21, 2002	Zhang
N/A	"Development of Very Thin (0.5 mmt) Transfer-molded TAB Packages" by Seung-Ho Ahn of Semiconductor Business, Samsung Electronics Co. and Yoshikatsu Maeda of Toray Industries Co.		December 1995	Ahn
N/A	"Development of Chip Scale Packages (CSP) for Center Pad Devices" by Masazumi Amagai, Hiroyuki Sano, Takayuki Maeda, Takahiro Imura, and		May 1997	Amagai

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
	Tadashi Saitohof the New Package Development (NDP) Dept., Texas Instruments Japan			
N/A	"TBGA Package Technology" by Frank E. Andros and Richard B. Hammer, from IEEE Transactions on Components, Packaging, and Manufacturing Technology, Part B, Vol. 17, No. 4		November 1994	Andros
N/A	"Thermal Characterization of Cavity-Down TBGA Package with Flotherm Simulation" by Eric Cho of Flotrend Co, Eric Tan of Taiwan Semiconductor Technology Co., Yu-Tsai Lin, Associate Professor of the Mechanical Engineering Department at Yuan-Ze Yniversity, Taiwan, from the Sixteenth IEEE Semi-Therm Symposium		March 2000	Cho
N/A	"TBGA Substrate for Lead-Free and Halogen-Free Applications" by C Q Cui and Kelvin Pun of Compass		September 2004	Cui

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
	Technology Co., Ltd., from the 2004 International IEEE Conference on Asian Green Electronics			
N/A	"Design and Optimization of High-Q RF Passives on SOP-Based Organic Substrates," by Sidharth Dalmia, Joseph Martin Hobbs, Venky Sundaram, Madhavan Swaminathan, Seock Hee Lee, Farrokh Ayazi, George White and Swapan Bhattacharya, affiliated with the School of Electrical and Computer Engineering, Packaging Research Center, Georgia Institute of Technology and the Oelphi Automotive Systems Fellow, Delphi Packard Electric Systems, from the 2002 Electronic Components and Technology Conference		May 2002	Dalmia
N/A	"Thermal Performance of Tape Based Ball Grid Array Over Molded Packages," by Darvin Edwards and Paul		March 1998	Edwards

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
	Hundt of Texas Instruments, Inc. from the Fourteenth IEEE SEMI-THERM Symposium			
N/A	"High-Performance Package Tape," by L. Fox, C. Davidson, and S. Hansen of the Manufacturing Design and Technology and K. Brown and A. Oscilowski of Semiconductor Operations of the Digital Equipment Corpoation, from 1992 IEEE Publication		1992	Fox
N/A	"Development of a 4-Layer Low Cost Flip Chip Packaging Technology" by Anand Govind, and Farshad Ghahghahi of LSI Logi Corp from the 2003 Electronic Components and Technology Conference		May 2003	Govind
N/A	"Development of Organic Flip Chip Packaging Technology for Nanometer Silicon Incorporating Copper Metallization and Low-k Dielectric" by Anand Govind, and Farshad Ghahghahi		2004	Govind

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
	of LSI Logi Corp from the 2004 Electronic Components and Technology Conference			
N/A	"Comparative Analysis of two heat spreader desims for a Wire Bond TBGA Package" by Satish C. Guttikonda', Bahgat G. Sammakia, Dept. of Mechanical Engineering, T.J.Watson School of Engineering, State University of New York at Binghamton, from the 2002 Inter Society Conference on Thermal Phenomena		2002	Guttikonda
N/A	"Thermal & Electrical Performance and Reliability Results for Cavity-Up Enhanced BGAs," by Terry F. Hayden, Paul M. Harvey, Randy D. Schueller, and William J. Clatanoff of the 3M Electronic Products Division Laboratory from the 1999 Electronics Components and Technology Conference		1999	Hayden

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
N/A	"High Density BGA Substrates Fabricated by Laser Technologies" by Tadashi Hirakawa" and Fumitaka Sato of Fuji Machinery Mfg & Electronics CO , Ltd.		1997	Hirakawa
N/A	"Moisture Resistance Of Epoxy Resin Used For Extremely Low Profile Ic Modules" by Hiroki Hirayama, Norio Totsuka and Seigo Nambu of Production Engineering Center, OK1 Electric Industry Co., Ltd. from the IEEE/CHMT '89 Japan IEMT Symposium		1989	Hirayama
N/A	"Understanding the Strength of Epoxy-Polyimide Interfaces for Flip-Chip Packages" by Pat Hoontrakul, Les H. Sperling, and Raymond A. Pearson from IEEE Transactions On Device And Materials Reliability, Vol. 3, No. 4, December 2003		December 2003	Hoontrakul
J17	"Viability of Anisotropic Conductive Film (ACF) as a Flip Chip		2000	Kim

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
	Interconnection Technology" by K.M. Kim, J.O. Kim, S.G. Kim, K.H. Lee of ChipPAC Korea Co., Ltd. and A.S. Chen, N.Ahmad, N. Dugbartey, M. Karnezos, S.Tam, Y.D. Kweon, R. Pendse of ChipPAC, Inc. of 2000 Electronic Components and Technology Conference			
N/A	"Investigation of Thermal Enhancement on Flip Chip Plastic BGA Packages Using CFD Tool" by Tien-Yu (Tom) Lee, Associate Member, IEEE, from IEEE Transactions On Components And Packaging Technologies, Vol. 23, No. 3, September 2000		September 2000	Lee
N/A	"New Approach to Using Anisotropically Conductive Adhesives for Flip Chip Assembly," by Alan M. Lyons, Elizabeth E. Hall, Yiu-Hum Wong, and Gregory Adams of AT&T Bell		1995	Lyons

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
	Laboratories, a 1995 IEEE Publication			
N/A	"High Frequency, High Power Miniature DC to DC Power Supply utilizing MCM-L Technology" by Greg Miller of Harris Semiconductor, Intelligent Power Products and Matt Salatino, of Harris Semiconductor Melbourne, Florida Advanced Packaging Technology		February 1996	Miller
N/A	"High Density Packaging for Mobile Terminals," by Seppo K. Pienimaa of Nokia Mobile Phones and Nigel I. Martin of Nokia Mobile Display Appliances, from 2001 Electronic Components and Technology Conference		2001	Pienimaa
N/A	"High-Density Packaging for Mobile Terminals" by Seppo K. Pienimaa and Nigel I. Martin, from IEEE Transactions On Advanced Packaging, Vol. 27, No. 3, August 2004		August 2004	Pienimaa
N/A	"A Numerical Study of the Thermal Performance of an Impingement Heat		August 2004	Shah

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
	Sink—Fin Shape Optimization," byAmit Shah, Bahgat G. Sammakia, Hari Srihari, and Koneru Ramakrishna, Member, IEEE from from IEEE Transactions On Advanced Packaging, Vol. 27, No. 3, August 2004			
N/A	"Thermomechanical Reliability Assessment of Large Organic Flip-Chip Ball Grid Array Packages," by Mark F. Sylvester, Donald R. Banks, Richard L. Kem, and Ronald G. Pofahl of W. L. Gore & Associates, Inc. from 1998 Electronic Components and Technology Conference		1998	Sylvester
N/A	"System-In-Package (SIP): Challenges and Opportunities" by King L. Tai of Bell Laboratories, a 2000 IEEE Publication		2000	Tai
N/A	"Performance Of Metal Ball Grid Array(Meta1 BGA) Package" by Hirofbmi Tanaka, Junsuke Tanaka, Moritsugu Morita and Hiroshi Waki of Mitsui Chemicals,		1998	Tanaka

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
	Inc., of 1998 IEMT/IMC Proceeding			
N/A	"Chip-scale packaging," an August 1997 IEEE Spectrum publication		1997	Thompson II
J17	"Reliability Assessment of a Thin (Flex) BGA Using a Polyimide Tape Substrate," by Trent Thompson, Armando Carrasco and Andrew Mawer, of Motorola Semiconductor Products Sector, from 1999 IEEE/CPMT Int'l Electronics Manufacturing Technology Symposium		1999	Thompson
N/A	"Parametric Studies of the Thermal Performance of Back-to-Back Tape Ball Grid Array (TBGA) Packages," by Sandeep S. Tonapi, Sanjeev B. Sathe, Bahgat G. Sammakia, K. Srihari1, of the Thomas J. Watson School of Engineering and Applied Science, State University of New York at Binghamton and the IBM Microelectronics		2001	Tonapi

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
	Division, from the 2001 Electronic Components and Technology Conference			
N/A	"A Novel IMB Technology for Integrating Active and Passive Components," by R. Tuominen and J. K. Kivilahti, by 2000 IEEE		2000	Tuominen
J17	"Tape Ball Grid Array Package Analysis," by Y.P. Wang, and T.D. Her of Siliconware Precision Industries Co. Ltd., from 2000 Electronic Components and Technology Conference		2000	Wang
N/A	"Performance Enhanced Copper Core BGA," by Paul Wu, Kevin Chen, L.H. Ho of ProLinx Labs Corporation, and Manoj Nachnani of Enabling Solutions, Inc., from 1998 IEEE/CPMT Int'l Electronics Manufacturing Technology Symposium		1998	Wu
N/A	"A Transparent, High Barrier, and High Heat Substrate for Organic Electronics,"		August 2005	Yan

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
	by Min Yan, Tae Won Kim, Ahmet Gün Erlat, Matthew Pellow, Donald F. Foust, Jie Liu, Marc Schaepkens, Christian M. Heller, Paul A. Mcconnelee, Thomas P. Feist, And Anil R. Duggal, from Proceedings Of The IEEE, Vol. 93, No. 8, August 2005			
N/A	"Qualification of an Enhanced Ball Grid Array Package Using Build-up Layers on a Metal Heat Spreader," by LiG (Steve) Yang, Carl King and Ralph Doe of the Advanced Development Group, Intel Corporation, from the 2004 Electronic Component and Technology Conference		2004	Yang
N/A	"Optimizing Cost and Thermal Performance: Rapid Prototyping of a High Pin Count Cavity-Up Enhanced Plastic Ball Grid Array (EPBGA) Package," by Bret A. Zahn from ChipPAC Inc., from the Fifteenth SEMI-THERM Symposium		1999	Zahn

Exhibit	Reference	Filing / Priority Date	Date of Issue or Publication	Short Cite
J17	"Frontmatter," *The Electronic Packaging Handbook*, edited by Blackwell, G.W., CRC Press LLC		2000	Blackwell
J17	"Technology Drivers," *Microelectronics Packaging Handbook*, Part 1, Second Edition, Edited by Rao R. Tummala, Eugene J. Rymaszewski, Alan G. Klopfenstein, Spring Science Business Media, B.V.		1997	Tummala
J17	US 5,909,057	September 23, 1997	June 1, 1999	McCormick
J17	US 6,703,704	September 25, 2002	March 9, 2004	Alcoe
N/A	US 7,271,479	November 3, 2004	September 18, 2007	Zhao II
J17	US 6,284,569	May 10, 1999	September 4, 2001	Sheppard
J17	US 2005/0280139	June 21, 2004	December 22, 2005	Zhao III

b. Prior Art Systems/Services To The Asserted Claims of the '383 Patent.

Exhibit #	System/Service	Relevant Dates	Persons/Entities Involved in Prior Use, Sale, or Offers for Sale	Short Cite
J13	NVIDIA NV30, NV35, and NV38 based products, including at least the GeoForce FX 5800 (based on NV30)	Released on or around January 27, 2003	NVIDIA, its employees, and its customers	NVIDIA Cap Prior Art Products

J14	NVIDIA NV40, NV41, and NV45 based products, including at least the GeForce 6800 GT (PCIe) (based on NV45)	Released on or around April 24, 2004	NVIDIA, its employees, and its customers	NVIDIA Ring Prior Art Products
J15	ATI Radeon 8000 & 9000 series, including at least the ATI Radeon 9000 Pro	Released on or around August 1, 2002	ATI (which was subsequently acquired by AMD), its employees, and its customers	ATI Cap Prior Art Products
J16	ATI Radeon R300 series, including at least the ATI Radeon 9800 Pro	Released on or around March 1, 2003	ATI (which was subsequently acquired by AMD), its employees, and its customers	ATI Ring Prior Art Products

2. Obviousness Combinations

In *KSR International Co. v. Teleflex Inc.*, 550 U.S. 398 (2007), the United States Supreme Court clarified the standard for what types of inventions are patentable. The Supreme Court emphasized that inventions arising from ordinary innovation, ordinary skill, or common sense are not patentable. *Id.* at 415-27. In that regard, a patent claim may be obvious if the combination of elements was obvious to try or there existed at the time of the invention a known problem for which there was an obvious solution encompassed by the patent's claims. *Id*. at 417. In addition, when work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. *Id*. The Supreme Court recognized that if a person of ordinary skill can implement a predictable variation, Section 103 likely bars its patentability. *Id*.

All of the following rationales recognized in *KSR* support a finding of obviousness:

1. Combining prior art elements according to known methods to yield predictable results;

2. Simple substitution of one known element for another to obtain predictable results;

3. Use of known technique to improve similar devices (methods, or products) in the same way;

4. Applying a known technique to a known device (method, or product) ready for improvement to yield predictable results;

5. "Obvious to try"—choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;

6. Known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations would have been predictable to one of ordinary skill in the art; and

7. Some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

Certain of these rationales are discussed more specifically below. That others are not discussed more specifically should not be interpreted as an admission or concession that it does not apply. To the contrary, the discussion below simply provides more explanation of these specific rationales. Defendant may also rely on contemporaneous textbooks, treatises, and/or publications and/or on the testimony of fact and expert witnesses that bear on these rationales and on the reasons to combine the prior art.

Because the '383 Patent simply arranges old elements, with each performing the same function it had been known to perform and yields no more than what one would expect from such an arrangement, the combinations of these old elements are obvious. Further, in the prior art there were well recognized design needs and market pressures to develop the alleged invention claimed in the '383 Patent.

Those of ordinary skill in the art would have been (and indeed were) motivated to combine known prior art solutions in the manner claimed in the ’383 Patent. Design needs and market pressures provided ample reason to combine prior art elements in the manner recited in the claims. Moreover, since there were a finite number of predictable solutions, a person of ordinary skill in the art had good reason to pursue the known options. The prior art used those familiar elements for their primary or well-known purposes in a manner well within the ordinary level of skill in the art. A person of ordinary skill in the art would thus have had a reasonable expectation that the combination would succeed in producing the invention as claimed.

To the extent that any one of the anticipatory references is found not to disclose a limitation recited in the asserted claims from the ’383Patent, it would have been obvious to one of ordinary skill in the art at the time of the alleged invention of the ’383 Patent either (i) to modify the reference to include this limitation and any remaining limitations of this claim and any claim(s) from which this claim depends and/or (ii) to combine said reference with any other of the references in Exhibits J1-J17 and/or with a POSITA’s general knowledge. Generally, motivation to combine any of these references with others exists within the references themselves, as well as within the knowledge of those of ordinary skill in the art at the relevant time. A person having ordinary skill in the art would have been motivated to combine any of the references described in attached Exhibits J1-J17, including for the reasons described below. A person having ordinary skill in the art at the time of filing of the asserted patents would also have understood the references listed above, alone or in combination, to contain explicit and/or implicit teaching, suggestion, and/or rationales to combine them, including as further described below.

The alleged invention of the ’383 Patent relates to integrated circuit (“IC”) package with substrate, chip, passive components (including specifically a “capacitor,” as recited in claim 13),

and stiffener. This configuration for an IC package was well known in the prior art before the alleged priority date of the '383 Patent. By definition, the purpose of an IC package is to package an IC. Thus, at a minimum an IC package must include the IC—*i.e.*, a chip—and a "substrate" on which to place the chip. Moreover, a person of ordinary skill would recognize the benefit of including passive electronic components, such as decoupling capacitors, in the IC package. *See e.g.*, Dalmia et al., Design and Optimization of High-Q RF Passives on SOP-Based Organic Substrates, 2002 Electronic Components and Technology Conference, 495; Blackwell et al., The Electronic Packaging Handbook, 2000. Decoupling capacitors ensure the IC receives a steady voltage, which is key to proper IC operation. Blackwell et al., The Electronic Packaging Handbook, 2000 ("Large decoupling capacitors are also added between the power and ground planes for increased voltage stability."); *id.* ("Decoupling is also required to provide sufficient dynamic voltage and current level for proper operation of components during clock or at transitions when all component signal pins switch simultaneously under maximum capacitive load … Optimal implementation is achieved using a capacitor for a specific application: bulk, bypass, and decoupling."); *id.* ("Decoupling provides a localized point source charge, since finite inductance exists within the power supply network. By keeping the voltage level at a stable reference point, false logic switching is prevented."). Decoupling capacitors store charge and will absorb additional charge in response to voltage increases and will provide charge in response to voltage decreases. Blackwell et al., The Electronic Packaging Handbook, 2000 ("Decoupling capacitors ideally should be able to supply all the current necessary during a state transition of a logic device … The response of a decoupling capacitor is based on a sudden change in demand for current."). Thus, decoupling capacitors average out voltage from the IC's perspective, ensuring a more

consistent voltage supply to the IC, and for at least that reason a person of ordinary skill would have been motivated to include them in any IC package, regardless of its design.

Including a stiffener with an IC was similarly well known prior to the '383 Patent. *See e.g.*, Sathe. To make manufacturing more efficient and/or cheaper, one of ordinary skill would have been motivated to use thinner substrates with less material, which in turn are more prone to warping, and flexible substrates were also well known. '383 patent at 2:29-41 ("Background" section observing: "One advantage of thinner substrates is the ability to use smaller drill heads to perforate the substrate. The drilling of smaller holes means that less conductive material is needed to cover the interior of the hole and reduces undesirable impedance, saves manufacturing time, reduces waste, and is more cost effective. These advantages must be weighed against undesirable secondary effects such as warping of the surface of the substrate, difficulty of obtaining a stable surface, and weakening of the substrate during manufacturing operations. Thinner boards have lowered mechanical strength and impede the large scale industrialization of film-chip assemblies in a strip, matrix or array format."). Warping is a problem because it, e.g. negatively affects the connection of the IC to the substrate and in turn to the main board. Blackwell et al., The Electronic Packaging Handbook, 2000 ("Circuit board warpage is a fact of life that must be minimized for successful implementation of newer part packages. … [N]ewer large-area devices such as BGAs[] are extremely non-tolerant to board warp."); *id.* (identifying "[w]arped substrate" as one of the "[c]auses of solder bridges"). Adding a stiffener, such as a thin metal ring or cap, was a well-known mechanism for addressing the well-known warping issue before the '383 Patent. Blackwell et al., The Electronic Packaging Handbook, 2000 ("Flexible Printed Board. A printed board using a flexible base material only. May be partially provided with electrically nonfunctional stiffeners and/or cover lay.").

Indeed, give these well-known issues and solutions, before 2006, companies (including NVIDIA, ATI, and Intel) were using the same IC package design claimed by the '383 Patent publicly available, commercial products. For example, each of the following prior art systems and patents includes all components required by at least claim 1 of the '383 patent in at least the same configuration that Ocean is alleging falls within the scope of this claims in its preliminary infringement contentions: NVIDIA Ring Prior Art, NVIDIA Cap Prior Art, ATI Ring Prior Art, ATI Cap Prior Art, Chuang, Akai, Ogawa, Baba, Jimarez, Sathe, and Xie. The details of the disclosures are provided in the accompanying invalidity claim charts.

The types of substrates used in connection with IC packages, including use of "a polyimide tape substrate," as recited in claim 8, were well-known design choices. For example, as described in at least Thompson II, Ogawa, Jimarez, Fosberry, Thompson, Tummala, Blackwell, and Wang, various substrates for use in IC design and processing had well-known benefits and drawbacks, and one of ordinary skill would know to weigh these benefits and drawbacks when deciding what substrate to use. *See e.g.*, Thompson at 38 ("A flexible film, such as liquid-crystal polymer, unreinforced bismaleimaide triazine (BT) resin, or polyimide, serves as the package substrate."); Ogawa at [0047] ("First, an epoxy resin paste mixed with BaTiO3 powder is applied to the surface (upper surface in the figure) RFS of the resin film RF made of polyimide"); Jimarez at 2:2-5 ("The substrate 10 can be made of any conventional dielectric material, such as FR4, polyimide, polytetrafluoroethylene or other dielectric materials"); Fosberry at 5:34-39 ("semiconductor chip package assembly, generally designated as 10, includes a semiconductor chip 12 and a chip carrier 14. The chip carrier 14 is made up of a dielectric layer 16 (which may be flexible or rigid and is preferably made from a thin sheet of material such as polyimide)"); Tummala et al., "Microelectornics Packaging Handbook," 2d ed., 1997 (comparing various substrates

("carrier[s]"), and explaining that "[t]he flexible carrier … consists of two surface layers of thin-film copper wiring on each side of polymide or other polymeric film"); Blackwell et al., The Electronic Packaging Handbook, 2000 ("Glass reinforced polyimide is the next most used multilayer substrate material due to its excellent handling strength and its higher temperature cycling capability"). For example, at least the following prior art references disclose using a "polyimide tape substrate": Thompson et al., "Reliability Assessment of a Thin (Flex) BGA Using a Polyimide Tape Substrate," 1999 IEEE/CPMT Int'l Electronics Manufacturing Tech. Symposium at Abstract ("The fleXBGAm package is a thin package that uses polyimide tape as a substrate to reduce the overall package profile to 1.10 mm.");Ogawa at [0047] ("First, an epoxy resin paste mixed with BaTiO3 powder is applied to the surface (upper surface in the figure) RFS of the resin film RF made of polyimide"); Jimarez at 2:2-5 ("The substrate 10 can be made of any conventional dielectric material, such as FR4, polyimide, polytetrafluoroethylene or other dielectric materials"); Fosberry at 5:34-39 ("semiconductor chip package assembly, generally designated as 10, includes a semiconductor chip 12 and a chip carrier 14. The chip carrier 14 is made up of a dielectric layer 16 (which may be flexible or rigid and is preferably made from a thin sheet of material such as polyimide)"); Tummala et al., "Microelectornics Packaging Handbook," 2d ed., 1997 (comparing various substrates ("carrier[s]"), and explaining that "[t]he flexible carrier … consists of two surface layers of thin-film copper wiring on each side of polymide or other polymeric film"); Blackwell et al., The Electronic Packaging Handbook, 2000 ("Glass reinforced polyimide is the next most used multilayer substrate material due to its excellent handling strength and its higher temperature cycling capability"); Wang at 1 ("This paper describes how high performance polyimide (PI) tape based materials are being utilized to increase routing density and improve the electrical and thermal performance.").

The specific stiffener thickness claimed, including a stiffener between 500 and 1000 microns thick (0.5 - 1 mm), as recited in claim 9, was another design choice known in the art. *See e.g.*, Ogawa at [0050] ("The stiffener body 221 is formed of a substantially square-shaped copper plate having a thickness of 0.7 mm"); Sathe at 4:40-42 ("the die 120 may be, for example, in a thickness range of 0.6-0.9 mm, and typically may be 0.8 mm"); NVIDIA_OS_00003427; NVIDIA_OS_00033460. A person of ordinary skill would understand that there is no unexpected result from using a particular stiffener thickness, e.g., using 0.45 or 1.05 vs. 0.5-1 mm. At most, a person of ordinary skill would understand that the stiffener should not protrude beyond the height of the IC because doing so may waste space and decrease the thermal contact between the IC and a heat sink. This was all known well before the '383 Patent. For example, at least the NVIDIA Ring Prior Art, NVIDIA Cap Prior Art, Ogawa, and Sathe disclose using a stiffener with the thickness required by claim 9.

Given that all of the above was well known in the art before the '383 patent, a person of skill in the art would have known that any and/or all of these above techniques could be combined to create an IC package with a substrate, chip, passive components, and stiffener. Furthermore, this general background knowledge would have provided the basis for combining any number of known IC package designs to create different IC packages. Because all of these techniques were already known in the art for use in IC package design, a person of skill in the art would have understood that combining these techniques would have yielded predictable results, would have been a simple substitution of one known technique for another to obtain predictable results, would have used known techniques to improve similar techniques in the same way, would have applied a known technique to a known method that was ready for improvement to yield predictable results, would have been obvious to try because the techniques were all known and there was reasonable

expectation of success in combining them, would have been obvious to try to improve IC package design, and would have been obvious because all techniques were already known and combined in various fashions before. With respect to the prior art references in Exhibits J1-J17, a person of ordinary skill in the art would have been motivated to combine any of the references identified as prior art to the '383 Patent for these reasons provided above, and the additional reasons provided below.

First, all of the prior art references identified as prior art to the '383 Patent teach similar IC package designs, and thus the teachings of any one reference are applicable to other references in that same field. *See e.g.*, Sathe at 1:7-9 ("The present invention relates to arrangements to provide mechanical stiffening elements to a thin-core or coreless substrate."); Jimarez at 1:4-10 ("This invention relates generally to I/C chip mounting structures which include a substrate and an electrically and thermally conducting cover plate and a method of manufacturing the same. In even more particular aspects, this invention relates to an I/C chip assembly which electrically insulates the chip from the cover plate but provides grounding of the substrate to the cover plate."); Fosberry at 1:24-26 ("The present invention relates generally to a method of packaging a semiconductor chip or an array of such semiconductor chips."); Akai at [0001] ("The present invention relates to a semiconductor device, and more particularly to a semiconductor device in which a semiconductor chip is mounted on a substrate by using flip chip bonding technology."); Ogawa at [0001] ("The present invention relates to a wiring board and a stiffener provided with a stiffener and a capacitor, and a method for manufacturing the same, and more particularly to a wiring board and a stiffener having high rigidity, and a method for manufacturing the same."); Baba at 1:6-14 ("The present invention relates generally to a semiconductor device in which one or more semiconductor chips and chip components are mounted on a substrate and a method of

manufacturing the semiconductor device. More particularly, the present invention relates to a semiconductor device in which one or more semiconductor chips and chip components are mounted on a substrate and in which electrical short and coming away of the chip components from the substrate are avoided, and a method of manufacturing such semiconductor device."); Akai at [0001] ("The present invention relates to a semiconductor device, and more particularly to a semiconductor device in which a semiconductor chip is mounted on a substrate by using flip chip bonding technology"); Xie at 2:64-3:5 ("While the following detailed description will describe example embodiments of the IHS/IS arrangements applied to thin-core substrates and coreless substrates in the context of an example FC-PGA arrangement, practice of embodiments of the present invention is not limited to such context, i.e. practice of embodiments of the present invention may have uses with other types of chips and with other types of mounting and packaging technologies, e.g. flip chip ball grid array (FC-BGA) packages, interposers, etc."); Chuang at 1 ("The present disclosure relates to a flip-chip package module, and more particularly relates to a stiffener ring with an uneven contact surface and a heat sink. As the demand for lighter and more complex electronic devices increases, the speed and complexity of chips also increase accordingly. Semiconductor chips must provide more leads accordingly for the input and output of signals. Flip-Chip Ball Grid Array (fcBGA) Package is a known and advanced package."); Thompson et al., "Reliability Assessment of a Thin (Flex) BGA Using a Polyimide Tape Substrate," 1999 IEEE/CPMT Int'l Electronics Manufacturing Tech. Symposium at Abstract ("Wireless communication customers require thinner, smaller footprint packaging to allow for reductions in phone and paging product sizes. Currently, the thin MAP (Mold Array Process) BGA (Ball Grid Array) package is in production which converted from glob-top BGA to reduce the overall package profile from 1.60 to 1.30 mm"). Given these similarities, a person of ordinary skill in the art would

have recognized the compatibility between the teachings of the prior art references. As explained above, it was common to assemble IC packages in the semiconductor industry, and a person of ordinary skill in the art would have regarded the combination of teachings from different references as typical in the field.

Second, a person of ordinary skill in the art would have been motivated and found it obvious to apply references teaching certain specific techniques, e.g., use of capacitors as passive electronic components, use of polyimide tape substrate, use of specific stiffener thickness, and use of a heat sink to other references that relate to IC packages generally because all references teach IC package designs, and it would have been a trivial exercise to consult the references that taught more specific IC designs to fill in less specific disclosures in other references. *See e.g.*, Sathe at 1:7-9; Jimarez at 1:4-10; Fosberry at 1:24-26; Akai at [0001]; Ogawa at [0001]; Baba at 1:6-14 ("The present invention relates generally to a semiconductor device in which one or more semiconductor chips and chip components are mounted on a substrate and a method of manufacturing the semiconductor device. More particularly, the present invention relates to a semiconductor device in which one or more semiconductor chips and chip components are mounted on a substrate and in which electrical short and coming away of the chip components from the substrate are avoided, and a method of manufacturing such semiconductor device."); Akai at [0001]; Xie at 2:64-3:5; Chuang at 1; Thompson et al., "Reliability Assessment of a Thin (Flex) BGA Using a Polyimide Tape Substrate," 1999 IEEE/CPMT Int'l Electronics Manufacturing Tech. Symposium at Abstract. A person of ordinary skill in the art would have also been motivated and found it obvious to replace and/or combine a reference's exact set of materials, components, or configurations in a particular IC package with the teachings regarding other materials, components, and configurations used in other IC packages for all the reasons provided above and

below. For example, these modifications would have only required a simple substitution of one known element for another (one material for another, one size for another), which would have obtained predictable results because it was already well known in the art that there were many techniques, designs, and processes for IC packaging. The substitution of one component, material, or configuration for another would not have changed the principle of operation for either reference in any combination because the references all use similar mechanisms for a similar purpose: designing an IC package. This is thus a combination of prior art elements (e.g., passive components, substrate material, stiffener thickness, or use of a heat sink) according to known methods (a person of ordinary skill would understand that these are all available design choices) to yield predictable results (a person of ordinary skill would understand the benefits and drawbacks of each design choice, and there are no unexpected results from any particular combination). A person of ordinary skill in the art would have been motivated to combine these teachings, and to make these replacements, because all of these IC package components, materials, and configurations were widely-used techniques. Accordingly, a person of ordinary skill in the art would have had a reasonable expectation of success given considerations discussed above, the similarities in the teachings and systems, and given that all the claimed IC package components, materials, and configurations were all well-known at the time. Implementing the combination and any necessary modifications would have been routine and within the scope of the prior art references' teachings.

As one example, to the extent that ATI Ring Prior Art, ATI Cap Prior Art, NVIDIA Ring Prior Art, Chuang, Baba, Sathe, or Xie does not disclose the "polyimide tape substrate" limitation of claim 8, it would have been obvious to combine any of these references with (e.g.) Ogawa, Jimarez, Fosberry, or Thompson to arrive at said limitation. Thompson at 38 ("A flexible film,

such as liquid-crystal polymer, unreinforced bismaleimaide triazine (BT) resin, or polyimide, serves as the package substrate.");Ogawa at [0047] ("First, an epoxy resin paste mixed with BaTiO3 powder is applied to the surface (upper surface in the figure) RFS of the resin film RF made of polyimide"); Jimarez at 2:2-5 ("The substrate 10 can be made of any conventional dielectric material, such as FR4, polyimide, polytetrafluoroethylene or other dielectric materials"); Fosberry at 5:34-39 ("semiconductor chip package assembly, generally designated as 10, includes a semiconductor chip 12 and a chip carrier 14. The chip carrier 14 is made up of a dielectric layer 16 (which may be flexible or rigid and is preferably made from a thin sheet of material such as polyimide)"). It would have been obvious to use a "polyimide tape substrate" disclosed in, e.g., Ogawa, Jimarez, Fosberry, or Thompson with, e.g., ATI Ring Prior Art, ATI Cap Prior Art, NVIDIA Ring Prior Art, Chuang, Baba, Sathe, or Xie because this was a well-known material for use as a substrate, and using this particular substrate would thus have been an obvious design choice that would be used with predictable results. Moreover, all of these references relate to IC package design, and a person of ordinary skill would have been motivated to look at Ogawa, Jimarez, Fosberry, or Thompson for specfic substrate materials.

As another example, to the extent that ATI Ring Prior Art, ATI Cap Prior Art, Chuang or Fosberry do not disclose including a capacitor or other type of passive electronic component in an IC package, NVIDIA Ring Prior Art, NVIDIA Cap Prior Art, Akai, Ogawa, Baba, Jimarez, Sathe, and Xie disclose this limitation. *See, e.g.,* Exhibit J14; NVIDIA_OS_00003229 (showing "CHIP-CAP"); Akai at [0040] ("The electronic elements 18 are, for example, … chip capacitors … ."); Ogawa at [0004] ("chip capacitors CC are mounted by solder"); Baba at 6:47-67 (disclosing "chip components 7, such as … chip capacitors"); Jimarez at 2:40-51 (disclosing "capacitors 36"); Sathe at 3:25-30 (disclosing "die side components (DSCs) 140" such as "decoupling capacitors or

resistors"); Xie at 3:10-33 (same); *see also* Blackwell et al., The Electronic Packaging Handbook, 2000 ("Large decoupling capacitors are also added between the power and ground planes for increased voltage stability."). For the same reasons one would include passive electronic components/capacitors in their IC packages (discussed above), one of ordinary skill would be motivated to also include passive components/capacitors in the ATI Ring Prior Art, ATI Cap Prior Art, Chuang or Fosberry, and including such components would have been a well-known design choice with predicable results because (as discussed above) it was common to include passive components in IC packages well before the '383 Patent at least because it was known to be desirable to use decoupling capacitors in IC packages.

Further, claim 1 of the '383 patent can be effectively separated into two requirements. The first requirement of claim 1 specifies how an IC package is manufactured using a "strip." Numerous references disclose manufacturing IC packages as part of a strip, including at least Maruyama, Horie, Fosberry, and LeBonheur (together, "manufacturing prior art"). *See, e.g.*, Maruyama at [0016] ("[A]s is well known in the art, when a IC mounting package is made of ceramic, or the like, a large area ceramic sheet having a plurality of package pieces connected longitudinally and horizontally is manufactured beforehand, and after a required process such as a component mounting, or the like, is applied on each piece, the process of dividing into individual pieces is carried out."); Horie at [0045] ("Here, in the method of manufacturing piezoelectric oscillators having the structures described in the first to fourth embodiments of the present invention, the method of cutting a sheet wiring substrate arranged with a plurality of wiring substrates for a plurality of oscillators from the viewpoint of mass productivity into individual oscillators after adjusting respective oscillators is employed."); Fosberry at 10:48-50 ("The embodiment shown in FIG. 11 can be produced one at a time. Preferably, however, it is produced

using a panel process, as described above, such that many chips 12 can be packaged simultaneously"); *id.* at 7:45-50 ("Added manufacturing efficiency can be reached by encapsulating a plurality of such packages within the same frame ... ."); *id.* at 16:22-29 ("Although only two chips are pictured in FIGS. 17A-17I and many of the other figures herein, the methods of the present invention are preferably practiced by simultaneously packaging more than two chips on a single chip carrier. The optimum number of chips that can be simultaneously packaged on a single chip carrier will be determined by the respective sizes of the chip carrier and chips."); LeBonheur at [0024] ("[A]n array of seminconductor chip packages 28 can be manufactured in a molded matrix type of package (MMAP) … After manufacture, substrate 30 is cut to provide the separate semiconductor chips."). It was also well known that strips could have any number of dimensions, which are limited as a practical matter only by substrate space and/or manufacturing device capabilities, and rows of three packages (as recited in claim 2) was a well-known option. *See, e.g.,* Fosberry at Fig. 13A (showing rows of 3 chips, continuing indefinitely); *id.* at 16:16-22-29 ("Although only two chips are pictured in FIGS 17A-17I and many of the other figures herein, the methods of the present invention are preferably practiced by simultaneously packaging more than two chips on a single chip carrier. The optimum number of chips that can be simultaneously packaged on a single chip carrier will be determined by the respective sizes of the chip carrier and chips."); LeBonheur at Fig. 3 (showing rows of 3 chips).

The second requirement of claim 1 specifies the configuration of an individual IC package—including a specific configuration of "stiffener" and "passive electronic components," as discussed above. Numerous references disclose this specific configuration, including at least NVIDIA Ring Prior Art, ATI Ring Prior Art, NVIDIA Cap Prior Art, ATI Cap Prior Art, Chuang, Akai, Ogawa, Baba, Jimarez, Sathe, and Xie (together, "configuration prior art"). *See e.g.*, Sathe

at 1:7-9 ("The present invention relates to arrangements to provide mechanical stiffening elements to a thin-core or coreless substrate."); Jimarez at 1:4-10 ("This invention relates generally to I/C chip mounting structures which include a substrate and an electrically and thermally conducting cover plate and a method of manufacturing the same. In even more particular aspects, this invention relates to an I/C chip assembly which electrically insulates the chip from the cover plate but provides grounding of the substrate to the cover plate."); Fosberry at 1:24-26 ("The present invention relates generally to a method of packaging a semiconductor chip or an array of such semiconductor chips."); Akai at [0001] ("The present invention relates to a semiconductor device, and more particularly to a semiconductor device in which a semiconductor chip is mounted on a substrate by using flip chip bonding technology."); Ogawa at [0001] ("The present invention relates to a wiring board and a stiffener provided with a stiffener and a capacitor, and a method for manufacturing the same, and more particularly to a wiring board and a stiffener having high rigidity, and a method for manufacturing the same."); Baba at 1:6-14 ("The present invention relates generally to a semiconductor device in which one or more semiconductor chips and chip components are mounted on a substrate and a method of manufacturing the semiconductor device. More particularly, the present invention relates to a semiconductor device in which one or more semiconductor chips and chip components are mounted on a substrate and in which electrical short and coming away of the chip components from the substrate are avoided, and a method of manufacturing such semiconductor device."); Akai at [0001] ("The present invention relates to a semiconductor device, and more particularly to a semiconductor device in which a semiconductor chip is mounted on a substrate by using flip chip bonding technology"); Xie at 2:64-3:5 ("While the following detailed description will describe example embodiments of the IHS/IS arrangements applied to thin-core substrates and coreless substrates in the context of an example FC-PGA

arrangement, practice of embodiments of the present invention is not limited to such context, i.e. practice of embodiments of the present invention may have uses with other types of chips and with other types of mounting and packaging technologies, e.g. flip chip ball grid array (FC-BGA) packages, interposers, etc."); Chuang at 1 ("The present disclosure relates to a flip-chip package module, and more particularly relates to a stiffener ring with an uneven contact surface and a heat sink. As the demand for lighter and more complex electronic devices increases, the speed and complexity of chips also increase accordingly. Semiconductor chips must provide more leads accordingly for the input and output of signals. Flip-Chip Ball Grid Array (fcBGA) Package is a known and advanced package.").

One of ordinary skill would have been motivated and found it obvious to combine any manufacturing prior art with any configuration prior art to arrive at the '383 patent claims. The claims of the '383 patent simply include well known elements of IC design with well known elements of IC manufacturing. As explained above, one of ordinary skill would look to the configuration prior art to improve the components, material, or configuration of an individual IC package. Then, one of ordinary skill would look to the manufacturing prior art for disclosure on how to efficiently manufacture the IC packages. As one of ordinary skill would have understood, not only do ICs need to be designed, they then need to be manufactured. Therefore, one of skill in the art would have readily looked to prior art disclosing IC manufacturing processes to combine with prior art disclosing IC design to actually create and make a fully functional IC design. This would have been entirely obvious and routine. Indeed, at a high level, there are two options for manufacturing packages—manufacture part or all of a package as part of a strip using a single substrate, and then singulate; or first singulate substrate and then assemble individual packages—and a person of ordinary skill would have considered either obvious and been motivated to use the

"strip" approach to improve manufacturing efficiency and speed (e.g., by assembling multiple packages at the same time). Moreover, a number of the configuration prior art references do not include much disclosure on manufacturing, revealing that a person of ordinary skill would understand that configuration prior art was focused on what components, materials, and configurations to use in the final product, but that person of ordinary skill would look to other references (such as the manufacturing prior art) to learn how to manufacture the final product. And when the configuration prior art did address manufacturing, it readily recognized the importance of efficient, cost-effective manufacture, and that this may be achieved by manufacturing components in strips and only performing singulation after part or all of the package has been assembled. *See, e.g.,* Sathe at 1:11-27 (noting significance of "lower manufacturing costs"); *id.* at 8:51-56 ("[I]t may be more advantageous to receive thin-core or coreless substrates from manufacturers having the stiffeners pre-attached thereto."). Any such combination would use each disclosure without substantial modification and arrive at expected results—IC packages as disclosed by the configuration prior art, but manufactured in accordance with the manufacturing prior art. In fact, this would have been so obvious to try because without the manufacturing prior art, the IC designs in the configuration prior art could not actually be made.

Additional obviousness combinations of the references identified here are possible, and Defendant may rely on such combination(s) in this litigation. In particular, Defendant is currently unaware of Ocean's allegations with respect to the level of skill in the art and the qualifications of the typical person of ordinary skill in the art. Defendant is also unaware of the extent, if any, to which Ocean may contend that limitations of the claims at issue are not disclosed in the prior art identified by defendants as anticipatory, and the extent to which Ocean will contend that elements not disclosed in the asserted patent specifications would have been known to persons of skill in

the art. And Defendant does not yet know how the Court will construe terms in the asserted claims. Defendant is also continuing its investigation of the large universe of prior art to identify potential prior art systems, publications related to those systems, and third parties that may have information about those systems. Ocean may also be in possession of prior art that Defendant may receive after discovery opens in this case. Defendant reserves the right to amend and supplement these contentions to identify other prior art and combinations rendering the asserted claims obvious.

D. INVALIDITY BASED ON 35 U.S.C. § 112 FOR INDEFINITENESS, LACK OF WRITTEN DESCRIPTION AND ENABLEMENT

The specifications of certain Asserted Patents do not provide adequate written description to support the scope of the claims asserted by Ocean in furtherance of its infringement theories or any reasonably understood scope of the claims.[14] 35 U.S.C. § 112 ¶ 1[15] requires the specification to contain "a written description of the invention." To fulfill the written description requirement, the specification "must clearly allow persons of ordinary skill in the art to recognize that the inventor invented what is claimed." *Ariad Pharm., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010) (citation omitted). To satisfy the written description requirement, "the applicant must 'convey with reasonable clarity to those skilled in the art that, as of the filing date sought, he or she was in possession of the invention,' and demonstrate that by disclosure in the specification of the patent." *Carnegie Mellon Univ. v. Hoffmann-La Roche Inc.*, 541 F.3d 1115, 1122 (Fed. Cir.

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[14] This is also true of the original application(s) that gave rise to the Asserted Patents.

[15] Because Ocean contends that the Asserted Claims are entitled to a priority date before September 16, 2012, Defendant applies pre-AIA 35 U.S.C. § 112 here. However, to the extent that any other form of the patent statute (e.g., post-AIA) regarding invalidity for indefiniteness, non-enablement, or lack of written description applies, Defendant's contentions and analysis apply just the same.

2008) (quoting *Vas-Cath Inc. v. Mahurkar*, 935 F.2d 1555, 1563-64 (Fed. Cir. 1991)). Certain of the Asserted Patents do not meet that requirement for the reasons described below. Defendant reserves the right to amend this list.

Additionally, certain of the Asserted Patents do not enable the claim scope reflected in Ocean's Infringement Contentions and interpretation of the Asserted Claims.[16] Title 35 U.S.C. § 112 ¶ 1 requires the specification to describe "the manner and process of making and using [the invention], in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains … to make and use the [invention]." The enablement requirement is separate from and in addition to the written description requirement. *Ariad*, 598 F.3d at 1344. This "requirement is satisfied when one skilled in the art, after reading the specification, could practice the claimed invention without undue experimentation." *AK Steel Corp. v. Sollac & Ugine*, 344 F.3d 1234, 1244 (Fed. Cir. 2003) (citation omitted); *see Wyeth & Cordis Corp. v. Abbott Laboratories*, 720 F.3d 1380 (Fed. Cir. 2013). Certain of the Asserted Patents do not meet that requirement for the reasons described below. Defendant reserves the right to amend this list.

Certain of the Asserted Claims of certain of the Asserted Patents are invalid for failing to comply with the definiteness requirement of 35 U.S.C. § 112. Defendant notes that its charting of a prior art reference for a claim or limitation that Defendant contends is invalid for lack of definiteness in no way represents an admission or concession that the scope of the claim or limitation is definite or ascertainable. Title 35 U.S.C. § 112 ¶ 2 requires that a patent claim "particularly point[] out and distinctly claim[] the subject matter which the applicant regards as his invention." Claim terms that fail to inform those skilled in the art "with reasonable certainty . . .

[16] This is also true of the original application(s) that gave rise to the Asserted Patents.

about the scope of the invention" fail the definiteness requirement of § 112 ¶ 2. *Nautilus, Inc. v. Biosig Instruments, Inc.*, 134 S. Ct. 2120, 2124 (2014). The patent laws of the United States prohibit claiming an invention through functional terms as way to capture every way of performing a function. Claim terms that recite an invention using functional terms are invalid as indefinite, except for those adequately claimed and supported in accordance with 35 U.S.C. § 112 ¶ 6. Under 35 U.S.C. § 112 ¶ 6, an element in a claim may be expressed as a "means or step for performing a specified function without the recital of structure, material, or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof." "The standard [for determining whether § 112(6) applies] is whether the words of the claim are understood by persons of ordinary skill in the art to have a sufficiently definite meaning as the name for structure." *Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1349 (Fed. Cir. 2015). Although use of the word "means" in a claim creates a "presumption that § 112, ¶ 6 applies," "[w]hen a claim term lacks the word 'means,' the presumption can be overcome and § 112, para. 6 will apply if the challenger demonstrates that the claim term fails to recite sufficiently definite structure or else recites function without reciting sufficient structure for performing that function." *Id.* (internal quotations omitted). Certain of the Asserted Claims are indefinite for at least the reasons described below; the arguments below apply to both the listed claims and claims depending therefrom. Defendant reserves the right to amend this list.

a. The '651 Patent

Claim Element	Patent (Claim)	§ 112 Grounds
"said processed wafers"	'651 patent, claims 31, 35	Indefinite (§ 112 ¶ 2)
"said process chamber"	'651 patent, claim 31	Indefinite (§ 112 ¶ 2)

Claim Element	Patent (Claim)	§ 112 Grounds
"a process operation"	'651 patent, claims 19, 31, 72, 77	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)

b. The '538 patent

Claim Element	Patent (Claim)	§ 112 Grounds
A said computer	'538 patent, claim 1	Indefinite (§ 112 ¶ 2)
"determining in said computer an importance of a parameter"	'538 patent, claim 4	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
"a significant fault"	'538 patent, claim 5	Indefinite (§ 112 ¶ 2)
"determining in said computer whether said parameter is a significant factor"	'538 patent, claim 7	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
"requiring…a smaller/larger fluctuation of said parameter…to determine that a fault…has occurred."	'538 patent, claims 15, 16	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)

c. The '402 patent

Claim Element	Patent (Claim)	§ 112 Grounds
"the manufacture"	'402 patent, claim 1	Indefinite (§ 112 ¶ 2)
"determining if a fault condition exists"	'402 patent, claim 1	Indefinite (§ 112 ¶ 2)
"sending a signal by the framework to the first interface reflective of the predetermined action"	'402 patent, claim 1	Lack of enablement, written description, and/or indefinite (§ 112 ¶¶ 1, 2)
"providing that a faulty condition exists"	'402 patent, claim 2	Indefinite (§ 112 ¶ 2)
"a first communications protocol used by the sensor"	'402 patent, claim 4	Indefinite (§ 112 ¶ 2)
"a second communications protocol used by the fault detection unit"	'402 patent, claim 4	Indefinite (§ 112 ¶2)
"comparing the state data received at the first interface"	'402 patent, claims 5	Lack of enablement, written description, and/or indefinite (§ 112 ¶¶ 1, 2)

"comparing the state data received"	'402 patent, claims 6	Lack of enablement, written description, and/or indefinite (§ 112 ¶¶ 1, 2)
"other similar-type wafers"	'402 patent, claim 6	Lack of enablement and/or indefinite (§ 112 ¶¶ 1, 2)
"sending the accumulated state data from the data collection unit to the fault detection unit"	'402 patent, claim 7	Lack of enablement, written description, and/or indefinite (§ 112 ¶¶ 1, 2)
"a processing piece"	'402 patent, claim 7	Indefinite (§ 112 ¶2)

d. The '330 patent

Claim Element	Patent (Claim)	§ 112 Grounds
"Determining if one or more of the critical dimensions are outside of acceptable tolerances;" "acceptable tolerances"	'330 patent, claim 19	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
"determining whether an overlay error is occurring"	'330 patent, claim 19	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
"when at least one of an overlay error is occurring and one or more of the critical dimensions fall outside of acceptable tolerances"	'330 patent, claim 19	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)

e. The '305 patent

Claim Element	Patent (Claim)	§ 112 Grounds
"further comprising proactively scheduling an appointment with which the predetermined event is associated"	'305 patent, claim 10	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
"wherein proactively scheduling the appointment includes proactively scheduling the appointment from the software scheduling agent"	'305 patent, claim 11	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)

"…an appointment nearing completion, an appointment completing…"	'305 patent, claim 7	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
"an alarm event"	'305 patent, claims 3, 5, 7, 9	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)

f. The '691 patent

Claim Element	Patent (Claim)	§ 112 Grounds
"related to the processing of workpieces in a plurality of tools"	'691 patent, claim 1	Indefinite (§ 112 ¶ 2)
"generating context data for the metrology data"	'691 patent, claim 1	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
"conducting a process control activity related to one of the tools based on the filtered metrology data"	'691 patent, claim 1	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
"generating identification data associated with the metrology data"	'691 patent, claim 2	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
"generating collection purpose data"	'691 patent, claim 3	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)

g. The '248 patent

Claim Element	Patent (Claim)	§ 112 Grounds
"further comprising proactively scheduling an appointment with which the predetermined event is associated"	'248 patent, claim 8	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
"wherein proactively scheduling the appointment includes proactively scheduling the appointment from the software scheduling agent"	'248 patent, claim 9	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
"…an appointment nearing completion, an appointment completing…"	'248 patent, claim 5	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)

Claim Element	Patent (Claim)	§ 112 Grounds
"an alarm event"	'248 patent, claims 5 and 7	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)

h. The '097 patent

Claim Element	Patent (Claim)	§ 112 Grounds
"forming circuit structures having linewidths which are smaller than what is achievable by conventional UV lithographic techniques"	'097 patent, claims 1	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
"ultra-thin resist layer[s]"	'097 patent, claims 1	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
"width substantially equal to the final linewidth"	'097 patent, claims 1	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
"exposing the resist layer to a UV bake prior to the step of isotropic over-etching so as to enhance selectivity to the hardmask layer"	'097 patent, claim 10	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
"curing the resist layer by an electron beam prior to the step of isotropic over-etching so as to enhance selectivity to the hardmask layer"	'097 patent, claim 11	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
wherein the resist mask used in the isotropic etching step is maintained on top of the hardmask during the anisotropic etching step of the device layer.	'097 patent, claim 17	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)

i. The ’170 patent

Claim Element	Patent (Claim)	§ 112 Grounds
“the bottom surface coupled to the substrate and having a space at least partly surrounding at least one passive electronic component coupled to a substrate”	’170 patent, claim 1	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
“a polyimide tape substrate”	’170 patent, claim 8	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
“a thickness of about 500 to 1000 microns”	’170 patent, claim 10	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
“the packaged integrated chip has a thickness greater than the thickness of the stiffener”	’170 patent, claim 11	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)

j. The ’383 patent

Claim Element	Patent (Claim)	§ 112 Grounds
“at least one integrated circuit package in the strip has four lateral sections that surround a stiffener and where the integrated circuit package shares at least two of the four lateral sections with different integrated circuit packages along the strip”	’383 patent, claim 1	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
“the bottom surface coupled to the substrate and having a space at least partly surrounding at least one passive electronic component coupled to a substrate”	’383 patent, claim 1	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
“the strip is comprised of an array of 3-by-10 integrated circuit packages”	’383 patent, claim 2	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
“a polyimide tape substrate”	’383 patent, claim 8	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)

Claim Element	Patent (Claim)	§ 112 Grounds
"a thickness of about 500 to 1000 microns"	'383 patent, claim 9	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)

E. PATENT-INELIGIBLE SUBJECT MATTER UNDER 35 U.S.C. § 101

Defendant's asserted bases for invalidity under 35 U.S.C. § 101 are based on Defendant's investigation thus far. Defendant reserves the right to amend or otherwise modify its asserted bases for invalidity under 35 U.S.C. § 101 based on its review of additional documents and evidence, including, without limitation, additional information concerning the state of the art and level of one of ordinary skill in the art at the relevant time. Further, Defendant reserves the right to assert additional arguments of invalidity under 35 U.S.C. § 101 based on the claim construction process, Ocean's proposed claim constructions, any supplement to Ocean's infringement contentions, Ocean's expert reports, or other positions taken by Ocean. A more detailed basis for § 101 defenses will be set forth in Defendant's expert reports and/ or in pleadings. Additionally, Defendant incorporates by reference, as if stated fully herein, the 35 U.S.C. § 101 arguments put forth in the following memoranda in support of motions to dismiss from pending cases with common asserted patents: Memorandum of Law by Analog Devices, Inc. in Support of Motion to Dismiss for Failure to State a Claim, *Ocean Semiconductor, LLC v. Analog Devices, Inc.*, No. 1:20-cv-12310-PBS (D. Mass. April 26, 2021), Dkt. 18; Defendants Infineon Technologies AG and Infineon Technologies Americas Corp.'s Memorandum of Law in Support of Its Motion to Dismiss for Failure to State a Claim, *Ocean Semiconductor LLC v. Infineon Techs. AG*, No. 1:20-cv-12311-PBS (D. Mass. April 26, 2021), Dkt. 18; and Renesas's Rule 12(b)(6) Motion to Dismiss, *Ocean Semiconductor LLC v. Renesas Elecs. Corp.*, No. 6:20-cv-01213-ADA (W.D. Tex. April 26, 2021), Dkt. 15.

Certain Asserted Claims are not patent eligible under 35 U.S.C. § 101 because they are directed to abstract and well-known ideas that do not constitute patentable subject matter. *See Alice Corp. Pty. v. CLS Bank Int'l*, 134 S. Ct. 2347, 2355 (2014). In particular, the asserted claims of the '305 and '248 patents ("the Automation Patents") are directed to the mere automation of human activity. The common specification of the Automation Patents details how the claimed invention is a "software scheduling agent" that automatically schedules in reaction to events in the manufacturing process. However, the specification also explains that the exact same functions were traditionally performed by humans—namely wafer fabrication technicians. Such automation has repeatedly been held abstract. *See, e.g.*, *Credit Acceptance Corp. v. Westlake Servs*., 859 F.3d 1044, 1055 (Fed. Cir. 2017) ("[M]ere automation of manual processes using generic computers does not constitute a patentable improvement in computer technology."); *Univ. of Fla. Rsch. Found., Inc. v. Gen. Elec. Co*., 916 F.3d 1363, 1367 (Fed. Cir. 2019) ("[The patent] seeks to automate 'pen and paper methodologies' to conserve human resources and minimize errors. This is a quintessential 'do it on a computer' patent [that is invalid]."). In addition, the asserted claims of the '538, '402, and '691 patents ("Data Manipulation Patents") are directed to the abstract idea of data collection, analysis and manipulation. Such claims have consistently been found abstract. *Elec. Power Grp., LLC v. Alstom S.A*., 830 F.3d 1350, 1353-54 (Fed. Cir. 2016) (holding that collecting and analyzing information are abstract ideas) (collecting cases); *Braemar Mfg., LLC v. ScottCare Corp*., 816 F. App'x 465, 470 (Fed. Cir. 2020) (holding claims directed to "abstract idea of classification and filtering of data" ineligible).

These Asserted Claims also lack an "inventive step" because they apply the abstract idea using generic computer components and do not identify any advancements in the functioning of the computer equipment itself. In particular, the Automation Patents' purported advancement is

the reactive scheduling of events by a software scheduling agent. However, as this is the abstract idea itself, it cannot supply the inventive concept. *BSG Tech LLC v. Buyseasons, Inc*., 899 F.3d 1281, 1290 (Fed. Cir. 2018) ("[A] claimed invention's use of the ineligible concept to which it is directed cannot supply the inventive concept . . . ."). The bare recitation of a "software scheduling agent" in the claims also fails to provide an inventive concept where, "[s]ignificantly [it fails to] provide details to any non-conventional software for enhancing" reactive scheduling in a manufacturing process. *Credit Acceptance*, 859 F.3d at 1057; *Mortg. Application Techs., LLC v. MeridianLink, Inc*., 839 F. App'x 520, 526 (Fed. Cir. 2021) ("[C]laims that do not define the particular features used to achieve the alleged advantage cannot be said to pass step two of the Alice analysis."). Similarly, the claims of the Data Manipulation Patents fail to recite an inventive concept because they do not "require[] anything other than off-the-shelf, conventional computer, network and display technology for gathering, sending, and presenting the desired information." *Elec. Power*¸ 830 F.3d at 1355; *FairWarning IP, LLC v. Iatric Sys., Inc*., 839 F.3d 1089, 1095 (2016) ("While the claimed system and method certainly purport to accelerate the process . . . the speed increase comes from the capabilities of a general-purpose computer . . . .").

The '330 patent also is directed to the abstract idea of collecting, analyzing, and sending data relating to a process. Claim 19 recites mapping data, taking measurements, analyzing those measurements to determine if there are errors, and then passing along information depending on the outcome of the measurements to adjust the process. These steps can be done by a human. Dependent claims 21 and 22 fare no better, as they merely are directed to the addition of elements used in the measuring process. *See, e.g.*, *Elec. Power Grp., LLC v. Alstom S.A.*, 830 F.3d 1350 (Fed. Cir. 2016) (finding invalid claims that were directed to the abstract idea of "collecting information, analyzing it, and displaying certain results of the collection and analysis"); *Two-Way*

Media Ltd. v. Comcast Cable Communications, LLC, 874 F.3d 1329 (Fed. Cir. 2017) (finding invalid claims that were directed to the abstract idea of sending information, directing the sent information, monitoring receipt of the sent information, and accumulating records about receipt of the sent information); *Hewlett-Packard Co. v. Servicenow, Inc.*, No. 14-cv- 00570, Slip Op. at 6-16 (N.D. Cal. Mar. 10, 2015) (granting summary judgment of ineligibility of claims relating to, for example, the abstract ideas of monitoring deadlines and providing alerts and categorizing information); *Neochloris, Inc. v. Emerson Process Mgm't Power & Water Solutions, Inc.*, No. 1:14-cv- 09680, Op. at 9, 16 (N.D. Ill. Oct. 13, 2015) (granting motion for summary judgment on the basis of ineligibility of water treatment patent claims, holding that the claims were directed to the abstract idea of "observing, analyzing, monitoring, and altering"); *Joao Control & Monitoring Sys., LLC v. Telular Corp.*, No. 1:14- cv-09852, Op. at 11-12, 18 (N.D. Ill. Mar. 23, 2016) (holding that the claims were directed to the abstract idea of "monitoring and controlling property and communicating this information through generic computer functions"). There also is nothing unconventional or transformational about the claimed processes under *Alice* Step Two. Nor do the claims invent new ways of collecting, analyzing, and sending data. The only purported "invention" is doing two measurements at the same time, but the claims do not recite a transformational or new way of collecting that data at the same time, they merely state the measurements are performed "concurrently" without any further information. Thus, no new machine, device, or measuring methodology is claimed—the patent and claims only recite known SEM or scatterometry systems that can be used to perform the claimed steps, including the claimed "concurrent" measurements (*i.e.*, data collection). *Elec. Power*, 830 F.3d at 1355; *FairWarning*, 839 F.3d at 1095.

Similarly, the ’651 patent is directed to the abstract idea of adjusting the position of a wafer stage within a process tool by raising, lowering, or varying a tilt of the wafer stage on which a wafer is positioned for processing. In other words, the asserted claims of the ’651 patent purport to claim the abstract and conventional steps of changing the position of the wafer on the wafer stage relative to the process tool to affect subsequent processing of a wafer. All of the wafer processing steps claimed are conventional and do not save the asserted claims from unpatentability. Some of the asserted claims includes a step for measuring variations across a wafer to determine how the wafer stage position should be adjusted, but this step is merely part of long-used, conventional human activity related to wafer fabrication. Likewise, the generic “process operation” performed on the wafer positioned on the wafer stage recited in each of the asserted claims is a well-known and conventional step of the prior art that does not confer patent eligibility to any of the asserted claims. Thus, at bottom the asserted claims of the ’651 Patent claim the mere automation of human activity, which has been repeatedly held to be patent ineligible.

More specifically, the asserted claims of the ’651 patent are abstract because they attempt to claim the fundamental concept of adjusting the *position* of a wafer stage within a process tool in order to affect processing of the wafer positioned on the wafer stage. The U.S. Supreme Court has long recognized that § 101 “contains an important implicit exception: Laws of nature, natural phenomena, and abstract ideas are not patentable.” *Ass’n for Molecular Pathology v. Myriad Genetics, Inc.*, 569 U.S. 576, 589 (2013). Applying force to an object to alter the position of the object is perhaps the most fundamental law of nature. Thus, the ’651 Patent claims are not patent eligible for the same reason the Federal Circuit found claims directed to the application of Hooke’s Law to attenuate vibration in driveline propeller shafts (propshafts) invalid for attempting to claim natural laws. *Am. Axle & Mfg. v. Neapco Holdings LLC*, 967 F.3d 1285, 1295-96 (Fed. Cir. 2020)

("Claiming a result that involves application of a natural law without limiting the claim to particular methods of achieving the result runs headlong into the very problem repeatedly identified by the Supreme Court in its cases shaping eligibility analysis."). It is difficult to conceive of a natural law more fundamental than changing the position of a surface relative to another object through motion imparted to that surface. Each of the '651 Patent's asserted claims "is directed to a natural law because it clearly invokes a natural law, and nothing more, to accomplish a desired result." *Id*. at 1297. For example, independent claim 19 recites the step "*adjusting* said surface of said wafer stage by *actuating* at least one of a plurality of pneumatic cylinders that are operatively coupled to said wafer stage to accomplish at least one of *raising, lowering and varying a tilt of said surface* of said wafer stage." '651 patent at 12:62-66 (emphasis added). Thus, this step merely claims adjusting the position of the wafer stage by *actuating* at least one of a plurality of pneumatic cylinders to impart force on the wafer stage. The "adjusting" step in the other asserted independent claims are broader than claim 19. For example, claim 31 recites "*adjusting*, based upon said measured across-wafer variations, a *plane of a surface* of an adjustable wafer stage." *Id*. at 13:56-58 (emphasis added). According to the Summary of the Invention, adjusting the position of the wafer stage is the entire point of alleged novelty of the '651 Patent. *See id*. at 3:7-67; *supra*, §C.b.1. Accordingly, the asserted claims are abstract under *Mayo/Alice* step 1 for merely claiming the result of applying a natural law.

As to step 2 of the *Mayo/Alice* framework, nothing in the asserted claims qualifies as an "inventive concept" to transform them into patent-eligible subject matter. Although the '651 patent specification discloses "a controller for adjusting a plane of the surface of the wafer stage based upon the determined across-wafer variations produced by the tool" (*id.* at 3:62-64) none of the asserted claims recites a controller or any steps performed by a controller. *See id*. at 12:59-13:19;

13:50-67; 14:7-28; 17:17-40; 17:46-18:21. "We have repeatedly held that features that are not claimed are irrelevant as to step 1 or step 2 of the *Mayo/Alice* analysis." *Am. Axle*, 967 F.3d at 1293. Moreover, the result of applying the natural law of applying force to an object to change its position cannot serve as the "inventive concept" in step 2. "'A claimed invention's use of the ineligible concept to which it is directed cannot supply the inventive concept' required to cross the line into eligibility." *Id*. at 1299 (citing *BSG Tech*, 899 F.3d at 1290). The other steps in asserted independent claims 19, 31, 72 and 77 recite "previously known, conventional and routine" steps such as "providing a process chamber comprised of a wafer stage," "positioning a wafer on said wafer stage," and "performing a process operation on said wafer positioned on said wafer stage." The Background of the Invention of the '651 patent acknowledges that all of these steps were well-known and conventional in the prior art. *See* '651 patent at 1:8-3:3; *supra*, §C (discussing the '651 patent). Indeed, as discussed above in Section C with respect to the '651 patent, the '651 patent admits that the various claimed processing tool components on which the claimed methods are performed are well-known and conventional and intended to be used for their ordinary purposes (*e.g.*, a processing tool with a process chamber containing an adjustable wafer stage that may be adjusted by using conventional actuators such as pneumatic cylinders with ball and socket connections connecting the cylinders to the stage).

Similarly, none of the dependent claims provides an "inventive concept" sufficient to make them patent-eligible. For example, dependent claim 20 limits the "process chamber" of claim 19 to "at least one of a dependent chamber and an etching chamber," which were known and conventional. Dependent claims 21 and 22 limit positioning the wafer on the wafer stage to either after or before the wafer stage is adjusted, respectively. Dependent claim 23 limits the "process operation" in claim 19 to "at least one of a deposition process and an etching process in said process

chamber," again, known and conventional process operations. Dependent claim 24 limits the pneumatic cylinders of claim 19 to ball and socket connections to the wafer stage. Other dependent claims, such as claims 35 and 36, relate to measurement of across-wafer variations in a plurality of wafers, which the '651 Patent admits are conventional and routine. All of the limitations in dependent claims 20-24, 32, 34-37, 73-75, and 78-81 recite limitations that were well-known, conventional and routine and therefore do not provide an "inventive concept" that makes any of these claims patent-eligible. *See supra*, §C.b.1. Accordingly, all asserted claims of the '651 Patent are invalid because they claim ineligible subject matter.

Accordingly, the Asserted Claims of the '305, '248, '330, '651, '402, '538, and '691 patents identified above (*See supra* page 1) are invalid under 35 U.S.C. § 101 for claiming ineligible subject matter.

F. DOCUMENT PRODUCTION

Pursuant to the Court's Order Governing Proceedings and concurrent with service of these Preliminary Invalidity Contentions: Defendant NVIDIA Corporation is producing documents related to these Preliminary Contentions with the following Bates numbers: NVIDIA_OS_00000001 - NVIDIA_OS_00049881, and reserves the right to supplement by producing additional documents. NVIDIA also is making available for inspection physical samples of prior art devices/systems, including one PNY GeForce FX 5900 (NVIDIA_OS_P_000001), one BFG GeForce 6800 GT (PCIe) (NVIDIA_OS_P_000002), one NVIDIA GeForce 6800 (NVIDIA_OS_P_000003), four NVIDIA GeForce 6800 IC packages (NVIDIA_OS_P_000004-07), six NVIDIA GeForce FX 5900 ZT packages (NVIDIA_OS_P_000008-13), one ATI Radeon 9000 Pro (NVIDIA_OS_P_000014), and three ATI Radeon 9800 Pro (NVIDIA_OS_P_0000015-17). NVIDIA reserves the right to acquire and make available for inspection additional physical samples of prior art devices/systems.

Defendant NXP USA, Inc. is producing documents related to these Preliminary Contentions with the following Bates numbers: NXP0000001-0004296.

Defendants Renesas Electronics Corporation and Renesas Electronics America, Inc. are producing documents related to these Preliminary Contentions with the following Bates numbers: REN0000001– REN0000514.

Defendant Silicon Laboratories Inc. is producing documents related to these Preliminary Contentions with the following Bates numbers: SILABS-OCEAN-00000001 – 00000002.

Defendant STMicroelectronics, Inc. is producing documents related to these Preliminary Contentions with the following Bates numbers: STM0000001-STM0003173.

Defendant WDT is producing documents related to these Preliminary Contentions and will provide the Bates number under separate cover.

Defendant MediaTek is producing documents related to these Preliminary Contentions with the following Bates numbers: MTK-00000001 – MTK-00000002.

Defendant Silicon Labs also is producing prior art and other documents related to these Preliminary Invalidity Contentions on behalf of all Defendants. Those documents have the following Bates numbers: OCEAN-DEF-PA00000001 – OCEAN-DEF-PA00018209.

Copies of all these documents will be sent under separate cover.

Dated: August 27, 2021

Respectfully submitted,

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CERTIFICATE OF SERVICE

Pursuant to the Federal Rules of Civil Procedure and Local Rule CV-5, I hereby certify that, on August 27, 2021, all counsel of record who have appeared in the above-captioned cases are being served with a copy of the foregoing by email.

/s/ Eric C. Green