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Paper 129
Entered: June 13, 2023

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

PATENT QUALITY ASSURANCE, LLC, and
INTEL CORPORATION,
Petitioner,

v.

VLSI TECHNOLOGY LLC,
Patent Owner.

IPR2021-01229*
Patent 7,523,373 B2

Before THOMAS L. GIANNETTI, BRIAN J. MCNAMARA, and JASON W. MELVIN, *Administrative Patent Judges*.

MELVIN, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

* Intel Corporation, which filed a petition in IPR2022-00479, has been joined as a party to this proceeding.

I. INTRODUCTION

Patent Quality Assurance, LLC ("PQA") filed a Petition (Paper 1, "Pet.") requesting institution of *inter partes* review of claims 1–16 (all claims, or "the challenged claims") of U.S. Patent No. 7,523,373 B2 (Ex. 1001, "the '373 patent"), owned by VLSI Technology LLC ("Patent Owner").

After preliminary briefing, we instituted review. Paper 10 ("Institution Decision" or "Inst."). Following institution, Intel Corporation filed a petition for *inter partes* review and a Motion for Joinder in IPR2022-00479, requesting that Intel be joined as a petitioner to this proceeding. IPR2022-00479, Papers 3, 4. We instituted trial in IPR2022-00479, granted the Motion for Joinder, and added Intel as a petitioner here. *Id.*, Paper 13. A copy of that decision was entered into the record of this proceeding. Paper 30. Thus, PQA and Intel are, collectively, "Petitioner" here.

Patent Owner filed a Response (Paper 28 ("PO Resp.")), Petitioner filed a Reply (Paper 45 ("Pet. Reply")), and Patent Owner filed a Sur-Reply (Paper 89 ("PO Sur-Reply")). We held oral argument on October 26, 2022. Paper 126 ("Tr.").

We have jurisdiction under 35 U.S.C. § 6(b). This is a Final Written Decision under 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons set forth below, we find Petitioner has demonstrated by a preponderance of evidence that the challenged claims are unpatentable.

A. RELATED MATTERS

The parties both identify the following matters related to the '373 patent: *VLSI Technology LLC v. Intel Corporation*, No. 1:19-cv-00254-ADA (consolidated as 1:19-cv-00977) (W.D. Tex.) (trial concluded with jury

verdict); and *OpenSky Industries, LLC v. VLSI Tech. LLC*, IPR2021-01056. Pet. 75; Paper 4.

Patent Owner identifies the following additional matters: *VLSI Tech. LLC v. Intel Corp.*, No. 6:21-cv-00057 (W.D. Tex.); *VLSI Tech. LLC v. Intel Corp.*, No. 6:21-cv-00299 (W.D. Tex.); and *Intel Corp. v. VLSI Tech. LLC*, IPR2020-00158 (PTAB) (on appeal to Federal Circuit, No. 21-1616). Paper 4.

B. Real Parties in Interest

Petitioner PQA identifies only itself as the real party in interest. Pet. 75. Petitioner Intel also identifies only itself as the real party in interest. IPR2022-00479, Paper 3, 1. Patent Owner identifies VLSI Technology LLC and CF VLSI Holdings LLC as real parties in interest. Paper 4.

C. The '373 Patent

The '373 patent is titled Minimum Memory Operating Voltage Technique. Ex. 1001, code (54). It describes a method of determining the minimum operating voltage for integrated-circuit memory, storing the value of that voltage in nonvolatile memory, and using the value to determine when an alternative power-supply voltage may be switched to the memory or ensuring that the minimum operating voltage is otherwise met. *Id.*, code (57).

The '373 patent's Figure 1 is reproduced below. *Id.*, Fig. 1.

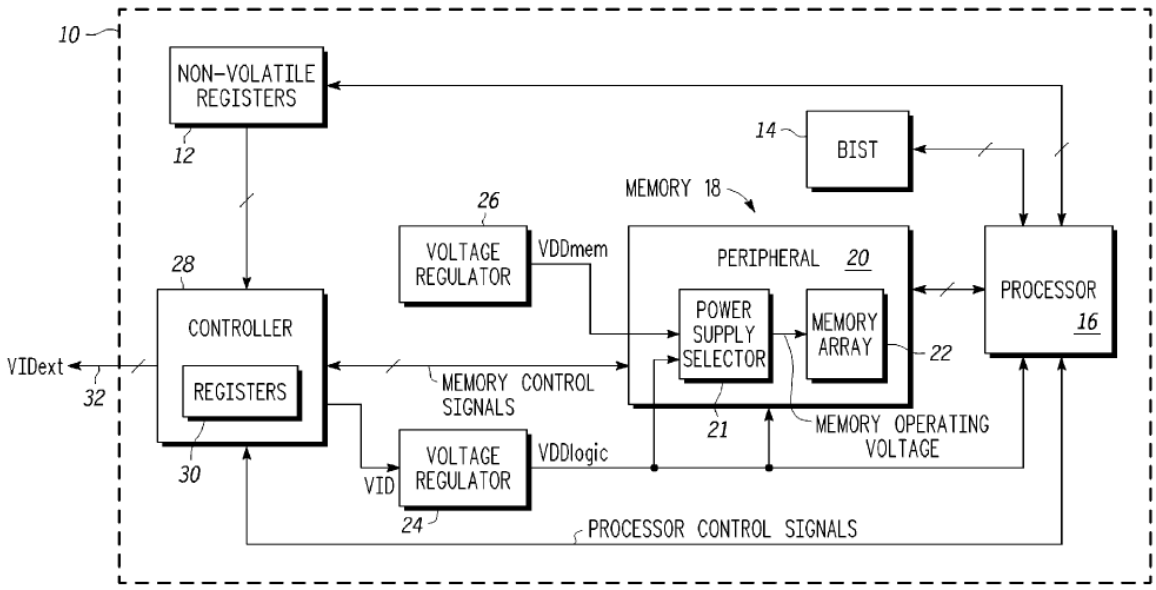

FIG. 1

Figure 1 depicts data processing system 10 including processor 16, voltage regulators 24 and 26, and memory 18 that includes power supply selector 21. *Id.* at 2:38–57. The system may adjust voltage regulator 24 such that "VDDlogic is scalable." *Id.* at 3:23–27; *see also id.* at 5:61–67 ("VDDmem may also be scalable"). Power supply selector 21 "selects one of VDDmem and VDDlogic and provides one of these to memory array 22 as the memory operating voltage." *Id.* at 2:52–55.

The '373 patent describes that various thresholds may be used for switching the memory's operating voltage from VDDlogic to VDDmem and that additional voltages may be provided to the memory using an additional voltage regulator. *Id.* at 3:54–67. For example, power supply selector 21 may switch the memory's power supply based on the minimum memory operating voltage required for reads, the minimum operating voltage required for writes, the minimum data retention voltage, or variations of those that depend on the memory's operating condition. *Id.* at 3:30–5:40.

The patent describes built-in test (BIST) circuitry 14, which may be used to determine the various minimum operating voltages, which are then stored in nonvolatile memory. *Id.* at 2:40–41, 6:22–46; *see also id.* at 6:47–8:15.

D. Challenged Claims

Challenged claim 1 is reproduced below:

1. A method, comprising:

[a] providing an integrated circuit with a memory;

[b] operating the memory with an operating voltage;

[c] determining a value of a minimum operating voltage of the memory;

[d.1] providing a non-volatile memory (NVM) location;

[d.2] storing the value of the minimum operating voltage of the memory in the NVM location;

[e] providing a functional circuit on the integrated circuit exclusive of the memory;

[f] providing a first regulated voltage to the functional circuit;

[g] providing a second regulated voltage, the second regulated voltage is greater than the first regulated voltage;

[h] providing the first regulated voltage as the operating voltage of the memory when the first regulated voltage is at least the value of the minimum operating voltage; and

[i] providing the second regulated voltage as the operating voltage of the memory when the first regulated voltage is less than the value of the minimum operating voltage,

[j] wherein while the second regulated voltage is provided as the operating voltage of the memory, the first regulated voltage is provided to the functional circuit.

Ex. 1001, 13:7–28.[1] Claims 9 and 16 are independent and recite limitations similar to claim 1's. *Id.* at 13:59–14:15, 14:40–62. Claims 2–8 each depend from claim 1; claims 10–15 depend, directly or indirectly, from claim 9. *Id.* at 13:29–14:39.

E. PRIOR ART AND ASSERTED GROUNDS

Petitioner asserts the following grounds of unpatentability:

Claim(s) Challenged	35 U.S.C. §	References/Basis
1–7, 9–11, 13–16	103	Harris,[2] Abadeer,[3] Zhang[4]
2, 11, 12	103	Harris, Abadeer, Zhang, Cornwell[5]
8	103	Harris, Abadeer, Zhang, Bilak[6]

Pet. 2. Petitioner relies also on the Declarations of Adit Singh, Ph.D. (Ex. 1002; Ex. 1040) and the Declaration of Sylvia D. Hall-Ellis, Ph.D. (Ex. 1027).

II. ANALYSIS

A. CLAIM CONSTRUCTION

Petitioner contends that no claim requires construction other than claim 14, which recites a "means for providing the operating voltage to the memory at a value at least as great as the minimum operating voltage in response to the operating value selected by the processor being below the

[1] Our bracketed designations for limitations largely follow those used by the parties. *See* Pet. 25–46.
[2] US 5,867,719, issued Feb. 2, 1999 (Ex. 1003).
[3] US 2006/0259840 A1, published Nov. 16, 2006 (Ex. 1004).
[4] US 2003/0122429 A1, published July 3, 2003 (Ex. 1005).
[5] US 7,702,935 B2, issued Apr. 20, 2010 (Ex. 1006).
[6] US 2005/0188230 A1, published Aug. 25, 2005 (Ex. 1007).

minimum operating voltage." Pet. 24, 64; Ex. 1001, 14:31–37. Petitioner points out that a district court construed the term as a means-plus-function term under 35 U.S.C. § 112, sixth paragraph, with the claimed function and a corresponding structure of the "power supply selector." *Id.* at 64 (quoting Ex. 1028, 2). Patent Owner does not challenge or otherwise address that construction, and we apply it in this decision.

B. UNPATENTABILITY OVER HARRIS, ABADEER, AND ZHANG

Petitioner submits that claim 1 would have been obvious over Harris, Abadeer, and Zhang. Pet. 25–46. Petitioner relies on Harris for a system with switchable voltages provided to memory and other systems in an integrated circuit. *Id.*

Harris discloses a system for permitting "soft defect detection testing (SDDT)" of a memory array in a data processor. Ex. 1003, code (57). Harris's Figure 1 is reproduced below. *Id.*, Fig. 1.

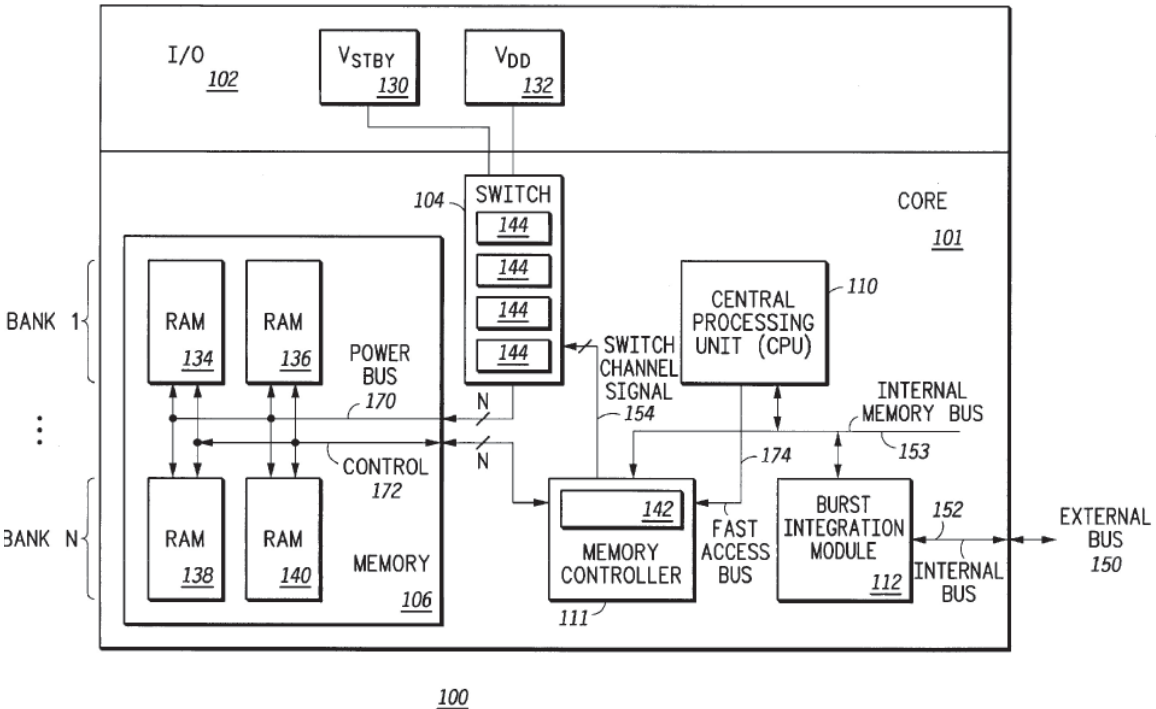

FIG.1

Figure 1 depicts data processor 100 with core 101 including memory portion 106 and switch circuit 104 with a plurality of switches 144 that couple two power-supply terminals in I/O section 102, Vstby 130 and VDD 132, to power bus 170 providing power to memory portion 106. *Id.* at 2:27–67.

Harris states that, "[i]n a normal mode of operation, the core 101 would be powered by a supply voltage applied to VDD terminal 132." *Id.* at 3:1–2. It then describes the SDDT operation, in which CPU 110 writes to register 142 in memory controller 111, causing switch 104 to power a portion of memory 106 from the Vstby terminal rather than the VDD terminal. *Id.* at 3:10–36. When so powered, an external circuit that applies power to the Vstby terminal may measure the current drawn by the portion

of memory powered by Vstby, detecting whether that portion has a defect. *Id.* at 3:36–49.

Harris describes that "the Vstby pin has a hardware controlled function as well," which is "the normal standby voltage function of the Vstby pin." *Id.* at 3:50–54. The parties refer to this as Harris's failure mode. For the failure-mode function, "the voltage level on the terminal VDD 132 is monitored to ensure that a functional voltage is provided." *Id.* at 3:54–56. "When this VDD voltage level drops below a set level or threshold, the voltage on the Vstby terminal 132 is switched to power the memory 106 to sustain memory contents when either main or VDD power is failing." *Id.* at 3:57–60. Thus, the memory contents are preserved by switching the memory to a power supply of sufficient voltage (Vstby) when the main supply (VDD) drops below the threshold level.

Harris further describes a low-power feature:

> [T]he test mode of the data processor . . . taught herein may be used as a low power feature wherein the second power supply voltage (Vstby or Vdd) is provided to the at least one memory array while the first power supply voltage (Vdd or Vstby) which is being supplied to the CPU is lowered so that lower power is consumed in the data processor while data within the at least one memory array is maintained.

Id. at 4:64–5:4.

Petitioner asserts that Abadeer discloses determining a memory's minimum operating voltage and storing that voltage's value in nonvolatile memory. Pet. 15–19, 27–30. Abadeer discloses "[a] solution for determining minimum operating voltages due to performance/power requirements." Ex. 1004, code (57). It states that its method applies to determining a minimum operating voltage for a "voltage island," in an integrated circuit,

such as a memory array. *Id.* ¶ 12. By that method, Abadeer aims to reduce power consumption in semiconductor circuits. *Id.* ¶ 13. Once a minimum operating voltage is determined in Abadeer, it is stored in nonvolatile memory. *Id.* ¶¶ 44–45.

Petitioner submits that skilled artisans had reason to use those teachings from Abadeer with Harris's system because (1) Harris teaches memory loss may occur below a threshold voltage and switching power supplies to prevent such losses, but does not teach how to determine that threshold; (2) Abadeer teaches a method for determining a memory's minimum operating threshold; (3) both Harris and Abadeer teach reducing a circuit's power consumption while maintaining a threshold voltage for memory in the circuit; and (4) Harris's and Abadeer's teachings are compatible, and Abadeer's technique would have predictably applied to Harris's system. *Id.* at 30–33.

Petitioner asserts that Zhang discloses voltage regulators applicable to Harris's system. Pet. 19–21, 36. Zhang discloses a system including "one or more integrated voltage regulators powered by an external voltage regulator and generating one or more local supply voltages for [a] processor." Ex. 1005, code (57); *see also id.* ¶¶ 18–31.

Petitioner submits that skilled artisans would have had reason to use Zhang's voltage regulators to supply the voltages for Harris's circuit. Pet. 35–40. Petitioner asserts that skilled artisans would have done so to (1) provide stable, precise supply voltages to Harris's system; (2) decrease power consumption when implementing Harris's low-power feature by making the supply voltages adjustable; and (3) predictably gain Zhang's benefits of adjustable supply voltages in Harris's system. *Id.* at 37–39.

1. Harris's three operational modes are compatible with Abadeer

Patent Owner contends that Harris describes a circuit that could not accommodate Abadeer's "minimum operating voltage" as a threshold for switching power supplies. PO Resp. 3–14. Patent Owner argues that the Institution Decision established that Harris's "'low power feature' must be compatible with the 'failure mode.'" *Id.* at 11 (citing Inst. 21); *accord id.* at 3–4. That misinterprets the Institution Decision, which stated that Harris's "three operating modes (SDDT, power failure, and low power) all arise from and relate to the same underlying hardware system." Inst. 21. That statement does not require all three modes be available in a particular implementation, only that all three use the same hardware system.

This distinction is particularly significant because Harris describes that its low-power feature is realized by using "the test mode." Ex. 1003, 4:64–65. The test mode uses a software-selected switch that allows the CPU to write to a register to control which power supply is provided to the memory. *Id.* at 3:9–18, 3:50–51. Thus, Harris describes that the low-power feature uses a software-defined switching threshold, and nothing about that threshold requires that it be the same as the threshold used for the failure mode. The failure mode, in contrast, is "a hardware controlled function" that monitors the voltage on the VDD terminal, and when that voltage "drops below a set level or threshold, the voltage on the Vstby terminal 132 is switched to power the memory 105 to sustain memory contents when either main or VDD power is failing." *Id.* at 3:52–60.

Accordingly, we do not agree with Patent Owner that "Harris's system cannot use a threshold [for its low-power feature] lower than the power-failure detection threshold." PO Resp. 11–12 (emphasis omitted). The

two aspects use different mechanisms to control which power supply is provided to the memory. Relatedly, Patent Owner asserts that Petitioner fails to justify "why a POSITA would have been motivated to abandon the 'failure mode' in favor of pursuing the specific 'low power feature.'" *Id.* at 14. Because Harris's failure mode and low-power feature are distinct aspects of Harris's operation, however, there would have been no need for skilled artisans to abandon one in favor of the other. In that regard, we credit Dr. Singh's testimony that because Harris's circuitry can be used for multiple functions, skilled artisans would have understood "how the operation of the circuitry would have been configured differently for those different functions or operations." Ex. 1040 ¶ 9.

Patent Owner argues additionally that, even if the low-power feature is distinct from the failure mode, Petitioner has not justified using the failure mode's "set level or threshold" with a different threshold for the low-power feature. PO Resp. 13–14. But that argument ignores that the low-power feature uses software to control the switch, rather than the hardware-controlled failure mode, as described above. Because the low-power feature and failure mode are based on different controlling mechanisms, Harris already describes using different thresholds for switching the memory's power supply in the two instances. And as Dr. Singh testifies, achieving the desired power savings or low-power operating parameters would have motivated skilled artisans to select a specific minimum operating voltage for the low-power feature. Ex. 1040 ¶ 9.

2. A failing voltage is not "regulated"

Patent Owner argues that, when Harris's failure mode is triggered such that the system switches the memory's power supply from VDD to

Vstby, the system would no longer provide the first regulated voltage (VDD) to the functional circuit (i.e., Harris's CPU) while providing Vstby to the memory. PO Resp. 14–17. We agree and do not rely on Harris's failure mode for unpatentability.

3. Harris's use of "while" is consistent with the claim language requiring switching "when" voltage drops

The claim language requires providing the memory with the first regulated voltage when it is at least the memory's minimum operating voltage, and providing the memory with the second regulated voltage when the first voltage is less than the memory's minimum operating voltage. Patent Owner summarizes that as "the voltage received by the memory is dictated by" the first regulated voltage. PO Resp. 17. Patent Owner argues that Harris's low-power feature does not follow that relationship because it discloses providing the memory with the second voltage "while the first power supply voltage . . . is lowered." *Id.* at 18 (quoting Ex. 1003, 4:65–5:4); *accord id.* ("Harris's memory is already receiving the second voltage '***while***' the first voltage is being lowered.").

We do not agree. Primarily, Harris's description of the low-power feature does not restrict the feature to a particular timing for switching the memory's power supply. Instead, Harris uses "while" as a term of contrast—the memory receives the second power supply voltage, in contrast to the CPU, which receives the first power supply voltage. Ex. 1003, 4:66–5:2. Although Harris does not limit the low-power feature's switching methodology, Petitioner explains that because Harris separately describes threshold-based voltage switching (in connection with the failure mode), implementing the claimed threshold-based switching in connection with the

low-power mode would have involved using that known technique to achieve a predictable result (avoiding memory data loss). Pet. 32–33 (citing Ex. 1002 ¶ 76).

We agree, and find that skilled artisans would have had reason to and would have known how to implement Harris's low-power feature with the threshold-based switching described in Harris's failure mode.

4. Skilled artisans had reason to add Zhang's voltage regulators to Harris's voltage supplies

The claim language requires providing a first regulated voltage to the functional circuit (i.e., the CPU), and providing a second regulated voltage that is greater than the first regulated voltage. That second regulated voltage is provided to the memory when the first regulated voltage is less than the memory's minimum operating voltage.

Petitioner reasons that because Harris discloses lowering the voltage provided to its CPU, skilled artisans would have understood that Harris's circuit implemented voltage scaling—an adjustable voltage—using a voltage regulator with a controllable output. Pet. 35–36 (citing Ex. 1002 ¶ 81). Petitioner further reasons that skilled artisans would have incorporated Zhang's teachings for providing a regulated voltage to a functional circuit. *Id.* at 36–40. For the same reasons, Petitioner submits skilled artisans would have been motivated to add Zhang's voltage regulator to Harris's Vstby input also. Pet. 42–43.

Petitioner submits that skilled artisans would have incorporated Zhang's voltage regulators on Harris's VDD and Vstby inputs "to provide a stable voltage" (Pet. 37 (citing Ex. 1002 ¶ 84)) and "to permit independent voltage control and to manage power in low power operation" (*id.* at 39

(citing Ex. 1002 ¶ 85)). As to managing power in low-power operation, Petitioner points out that Harris discloses that either voltage (VDD or Vstby) may be lowered. *Id.* at 38 (citing Ex. 1003, 4:63–5:4). Petitioner further reasons that using Zhang's regulators for Harris's VDD and Vstby inputs would have been nothing more than using Zhang's known elements in Harris's known system according to Zhang's known methods, with predictable results. *Id.* at 39.

Patent Owner challenges whether skilled artisans would have had reason to regulate Harris's Vstby power supply voltage. PO Resp. 19–32. First, Patent Owner argues that because Zhang discloses adjustable regulators, there would have been no need to use Harris's switching mechanism to switch power supplies rather than "simply adopting Zhang's solution" to adjust independent power supplies. *Id.* at 21–24. That argument is inapposite because existence of an alternative approach does not undermine Petitioner's combination. *Intel Corp. v. Qualcomm Inc.*, No. 2020-2092, 2022 WL 880681, at *4 (Fed. Cir. Mar. 24, 2022) (holding a petitioner is "required to show only that 'there is something in the prior art as a whole to suggest the *desirability* . . . of making the combination, not whether there is something in the prior art as a whole to suggest that the combination is the *most desirable* combination available.'" (quoting *In re Fulton*, 391 F.3d 1195, 1200 (Fed. Cir. 2004) (internal quotation omitted)).

Next, Patent Owner argues that Harris's battery-powered Vstby supply has no need for regulation because a battery already provides a sufficiently stable voltage source. *Id.* at 24–26. Harris states that "[n]ormally, Vstby will be powered from a battery back-up source."

Ex. 1003, 3:60–61.[7] While Patent Owner contends we should interpret Harris's statement to mean Vstby is powered from a battery when not used for Harris's soft-defect-test functionality (PO Sur-Reply 4), we do not agree. In our view, Harris's statement supports Petitioner's view that a battery need not be used in all scenarios, and Vstby could be powered from a non-battery source. *See* Pet. Reply 12 (citing Ex. 1040 ¶ 14). Nothing about Harris's statement indicates it is drawing a contrast with the test functionality. Further, the sentence continues that Vstby "may or may not be a voltage equal to that supplied by VDD." Ex. 1003, 3:61–62. That nonlimiting disclosure regarding voltage supports that Vstby could be provided by a source other than a battery. And in such a case, adding a regulator would benefit the power supply's stability as Petitioner asserts. *See* Pet. 37.

The parties dispute also whether Harris discloses adjusting the voltage of Vstby in addition to VDD. Petitioner relies on Harris's description of its "low power feature wherein the second power supply voltage (Vstby or Vdd) is provided to the at least one memory array while the first power supply voltage (Vdd or Vstby) which is being supplied to the CPU is lowered." Ex. 1003, 4:65–5:2. That description indicates that either supply may be provided to the CPU, and either may be provided to the memory. If the system provides power from Vstby to the CPU, then lowering the

[7] Patent Owner relies also on Dr. Singh's testimony that Harris's "standby voltage will be designed to be as robust as possible, including battery backup." Ex. 2053, 123:4–15. We do not agree that testimony establishes that Harris requires a battery in all implementations. Rather, Harris's nonlimiting language discussed above is more persuasive that Harris's battery is a preferred embodiment.

voltage provided to the CPU requires a way to adjust the Vstby voltage. Petitioner reasons that this need for voltage scaling would have motivated skilled artisans to include Zhang's adjustable voltage regulator in Harris's circuit for *both* VDD and Vstby. Pet. 35–36, 38–39, 42; Pet. Reply 10–11, 12, 14. Patent Owner disputes this, arguing that Harris never discloses providing Vstby to the CPU and therefore does not support a need for voltage scaling on Vstby. PO Sur-Reply 5; Tr. 43:8–46:4. Although Patent Owner recognizes that Harris discloses the interchangeability of its power supplies when lowering the CPU's voltage, Patent Owner contends that is a mistake "because the hardware of Harris is not designed for Vstby to power the CPU." Tr. 45:17–46:4.

Harris twice discloses the interchangeability of its power-supply inputs when discussing the low-power feature. Ex. 1003, 4:66–5:2. And that ability is consistent with Harris's description that "switch control signal 154 is software controlled or software programmable and is used to set a configuration of the switches 144 to control power supply distribution in the data processor 100." *Id.* at 2:47–52. That description indicates that switch 104 (which contains switches 144) controls power supply distribution in data processor 100 as a whole, not just for memory 106. Harris, however, does not depict the power supply connection from switch 104 to CPU 110, and Figure 2 shows a detailed view of switch 104 that does not include any output for CPU 100. *Id.*, Fig. 2. We read Harris's disclosure of its low-power feature as indicating a flexibility in the design that is consistent with the earlier description that switch 104 controls power supply distribution generally. Because Harris's core functionality does not require power supply interchangeability, there was no need for Harris to detail circuitry capable of

that. But that does not mean Harris's description of the interchangeability was a mistake.[8] While the issue is not determinative because we rely on Petitioner's other arguments that skilled artisans would have included Zhang's regulator on Vstby, we determine the record supports Petitioner's view that skilled artisans had reason to make Vstby scalable.

Additionally, Petitioner's contention that skilled artisans had reason to add Zhang's regulator to Harris's Vstby input does not depend on a non-battery Vstby supply. As the Petition contended, using a voltage regulator would provide a stable voltage. Pet. 37. Although Patent Owner argues that a battery already provides a stable voltage (PO Resp. 24–25), a voltage regulator would stabilize the battery's voltage as it neared discharge. *See* Pet. Reply 12. Dr. Singh's testimony supports that view, recognizing that Harris's reference to "a battery back-up source" indicates accompanying circuitry to condition and regulate the battery's voltage. Ex. 1040 ¶ 13. Stated otherwise, a battery alone does not necessarily provide an optimum power supply, and adding Zhang's voltage regulator as Petitioner asserts would offer a benefit to Harris's circuit.

Thus, we agree that skilled artisans had reason to add a voltage regulator to Harris's Vstby input to ensure a stable voltage for the memory during low-power operation. Patent Owner argues that including such a regulator would cost more in power dissipation than it would extend the battery life (PO Resp. 31–32), but we credit Dr. Singh's testimony that even

[8] Harris claims embodiments in which the first power supply voltage (claim 6) and the second power supply voltage (claim 7) may be lowered, supporting that Harris desires voltage scaling for both of its power supplies. Ex. 1003, 5:58–6:5.

with a voltage regulator's non-zero resistance, including the regulator would extend the usable battery life, particularly because the regulator would have been able to boost the battery's voltage at the end of its life. Ex. 1040 ¶ 16.

Patent Owner argues also that using a voltage regulator on Harris's Vstby input would compromise Harris's primary SDDT functionality. PO Resp. 27–30. Petitioner disputes that argument, submitting that the added voltage regulation would still permit detection of elevated current draws. Pet. Reply 12. We credit Dr. Singh's testimony that any higher current draw by the memory would result in higher current draw by the voltage regulator, permitting the testing as Harris intends. Ex. 1040 ¶ 15. Thus, although the added regulator may have an effect on SDDT, the record supports that the regulator would provide a benefit to low-power functionality without undermining SDDT.

Patent Owner argues also that using Zhang's regulators would undermine Harris's principle of operation by requiring design iterations to calibrate the on-chip regulators. PO Resp. 33–34. Harris sought to reduce iterations required during a circuit's design cycle by eliminating on-board test circuitry and providing a way for the circuit to use external test circuitry. Ex. 1003, 1:36–52. Dr. Singh agreed that present approaches to circuit design often require two or three iterations. Ex. 2053, 80:22–24. Patent Owner asserts that testimony shows that adding Zhang's regulators to Harris would undermine the goal of reducing design iterations, but Dr. Singh noted that "power supply specifications" implicating a voltage regulator are only one possible reason for design iterations and that "there are lots of other issues going on." *Id.* at 80:24–25; *see id.* at 79:17–80:25. We conclude that the record does not show that adding Zhang's voltage regulators would

interfere with Harris's principle of operation. As discussed above, the regulators would not prevent Harris's primary SDDT functionality. Harris's goal of reducing design iterations does not implicate its principle of operation, and even if adding Zhang's regulators would have added rather than reduced design iterations, we do not view it as rising to a level that would undermine the combination. *See Medichem S.A. v. Rolabo S.L.,* 437 F.3d 1157, 1165 (Fed. Cir. 2006) ("The fact that the motivating benefit comes at the expense of another benefit, however, should not nullify its use as a basis to modify the disclosure of one reference with the teachings of another. Instead, the benefits, both lost and gained, should be weighed against one another." (quoting *Winner Int'l Royalty Corp. v. Wang*, 202 F.3d 1340, 1349 n.8 (Fed. Cir. 2000))).

Finally, Patent Owner contends that Zhang's regulators require a stable reference to themselves regulate a voltage. PO Resp. 34–35. Thus, reasons Patent Owner, Harris's circuit would still need a stable, external voltage, eliminating any benefit from adding Zhang's regulators. *Id.* That argument, however, ignores Harris's desire for adjustable voltages. As discussed above, at least Harris's VDD (and in our view Vstby also) must be adjustable for the low-power feature, and Zhang's adjustable regulators provide that functionality.

For the reasons discussed, the record supports that adding Zhang's regulator to Harris's Vstby would provide a benefit, whether or not using a battery for Vstby and whether or not Harris supports scaling Vstby, and that skilled artisans therefore had reason to make the asserted combination, notwithstanding some potential drawbacks.

5. Using Abadeer's nonvolatile storage would not have undermined Harris's principle of operation

Abadeer discloses a "Built-In-Self-Test (BIST) circuit . . . used to determine the correct supply voltage for all elements in a design." Ex. 1004 ¶ 14. Once Abadeer's circuit uses BIST to determine the minimum operating voltages, those values are "stored in a non-volatile memory (such as fuses)." *Id.* ¶ 45. Petitioner reasons that, in the combination, skilled artisans would have incorporated Abadeer's nonvolatile memory to store minimum operating voltages to reduce the need to run the self-test and speed startup after a power cycle. Pet. 34 (citing Ex. 1002 ¶ 78).

Patent Owner contends that including nonvolatile memory would have disrupted Harris's principle of operation. PO Resp. 36–39. Because Harris uses SRAM, which was a type of memory that was a common alternative to nonvolatile memory, Patent Owner contends Harris "was designed to avoid such [nonvolatile] memory." *Id.* at 37. In Patent Owner's view, using Abadeer's BIST to determine the minimum operating voltage during each power cycle "would have been preferable." *Id.* But there is no requirement that an asserted "combination is the *best* option, only that it be a *suitable* option." *Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1380 (Fed. Cir. 2023). We do not agree with Patent Owner that Harris's principle of operation included avoiding nonvolatile memory. Petitioner provides a persuasive reason that skilled artisans would have used Abadeer's approach for storing determined minimum operating voltages in nonvolatile memory added to Harris's system.

6. Objective indicia of nonobviousness

Despite Patent Owner not asserting objective indicia of nonobviousness in the Response, Petitioner asserts that the jury verdict of infringement by Intel does not weigh against obviousness. Pet. Reply 23–25. Patent Owner disputes that and contends the jury's infringement verdict shows commercial success. PO Sur-Reply 19–20; *see* Ex. 1031, 2, 6.

As an initial matter, we determine that Patent Owner waived reliance on secondary considerations by failing to raise them in the Response. *See* Paper 15, 9 ("Patent Owner is cautioned that any arguments not raised in the response may be deemed waived."); *In re NuVasive, Inc.*, 842 F.3d 1376, 1380–81 (Fed. Cir. 2016); Consolidated Trial Practice Guide 52 (Nov. 2019), *available at* https://www.uspto.gov/TrialPracticeGuideConsolidated. Even considering Patent Owner's purported reliance, however, it is not persuasive.

To establish a nexus between Patent Owner's alleged commercial success and the '373 patent's claims, Patent Owner asserts that the jury was "charged with determining damages based upon the value of the technology captured by the claims." PO Sur-Reply 20 n.2 (citing Ex. 2021, 1545:13–1546:9).

When the evidence shows that a product includes "the invention disclosed and claimed in the patent," we presume that any commercial success of the product is due to the patented invention. *PPC Broadband v. Corning Optical Commc'ns,* 815 F. 3d 734, 746–747 (Fed. Cir. 2016). Such a presumed nexus requires not only that a commercial product embodies the claims, but also that it is coextensive with them. *See Fox Factory, Inc. v. SRAM, LLC*, 944 F.3d 1366, 1373 (Fed. Cir. 2019) ("[P]resuming nexus is

appropriate 'when the patentee shows that the asserted objective evidence is tied to a specific product and that product embodies the claimed features, and is coextensive with them.'" (quoting *Polaris Indus., Inc. v. Arctic Cat, Inc.*, 882 F.3d 1056, 1072 (Fed. Cir. 2018))).

Petitioner notes that the jury infringement verdict is on appeal. Pet. Reply 23. According to Petitioner, Patent Owner fails to show the verdict demonstrates commercial success with a nexus to the challenged claims. *Id.* at 24. Petitioner argues that the challenged claims were not the basis for customer demand of the accused products. *Id.* (citing Ex. 1044, 811:13–812:24 (Intel employee Adam King testifying that Intel's customers care about numerous technical attributes, including graphics performance for video editing, camera quality for video conferencing and power efficiency for laptops)). Petitioner notes that Patent Owner accused only the "C6 SRAM multiplexer" feature of infringing the '373 patent (Ex. 1042, 453:20–25; Ex. 1044, 815:16–816:21) and that Patent Owner's damages expert, Dr. Sullivan, "conceded that many of the thousands of other features 'have nothing to do with what [Patent Owner] accuses.'" Pet. Reply 24 (quoting Ex. 1043, 690:19–691:24).

The record before us does not show that Intel's product or products underlying the infringement verdict are coextensive with "the invention disclosed and claimed." *See Fox Factory*, 944 F.3d at 1373, 1377; *Facebook, Inc. v. Express Mobile Inc.*, IPR2021-01457, Paper 38 at 76–80 (PTAB Mar. 14, 2023) (concluding an infringement verdict was insufficient to establish nexus). Rather, the record shows that the accused products contained many features beyond those claimed in the '373 patent. Ex. 1043, 690:19–691:24; Ex. 1044, 815:16–816:21. That evidence persuades us that,

regardless of a presumed nexus, the commercial success does not have a nexus with the challenged claims.

Additionally, other than the jury verdict, Patent Owner has not provided financial information that would allow us to weigh the extent of Intel's infringing sales in the market. In particular, the record does not reflect whether the infringing devices represented an increase in market share over prior, noninfringing devices or any other aspect that would allow us to place the verdict's amount in context. *See, e.g.*, *In re Applied Materials, Inc.*, 692 F.3d 1289, 1300 (Fed. Cir. 2012) ("An important component of the commercial success inquiry in the present case is determining whether Applied had a significant market share."). On this record, even considering the waived issue, we find the evidence of commercial success is weak evidence of non-obviousness.

7. Harris is available as prior art

Patent Owner argues that Harris is nonanalogous art to the '373 patent and therefore cannot be used in an obviousness combination. PO Resp. 39–52. To be analogous art, Harris must be in the same field of endeavor as the '373 patent or be reasonably pertinent to the problem addressed by the '373 patent. *In re Clay*, 966 F.2d 656, 658–59 (Fed. Cir. 1992).

Patent Owner contends that the '373 patent's field of endeavor is a "minimum memory operating voltage technique." PO Resp. 40–41 (citing Ex. 2052 ¶¶ 155–156). With that contention, Patent Owner contrasts Harris's field, which Patent Owner asserts as "soft-defect testing on-chip memory." *Id.* at 43 (citing Ex. 2052 ¶ 157).

Petitioner submits that Patent Owner improperly constrains the '373 patent's field of endeavor. Pet. Reply 16–17. According to Petitioner,

the '373 patent's field is "the design and operation of memories, including voltage supplies to those memories." Pet. Reply 16 (citing Ex. 1040 ¶ 22). Petitioner points out that the '373 patent describes related art as that making "tradeoffs between performance and power" by operating processors "at maximum voltage and frequency when peak performance is required" and "at low voltage and frequency to reduce power consumption" at other times. Pet. Reply 16 (quoting Ex. 1001, 1:12–25). Petitioner compares that to Harris, which "teach[es] circuit design and operation for processors and/or memory to manage power by adjusting voltage levels to components of an IC." Pet. 39–40 (citing Ex. 1003, 4:63–5:4); Pet. Reply 17.

We agree with Petitioner. Both Harris and the '373 patent are in the field of memory power supply. While Harris describes a voltage-supply system allowing for a particular testing approach, its field is not limited to its primary purpose of soft-defect testing on-chip memory. Rather, Harris also describes that its system allows other features such as failure protection and a low-power feature. Ex. 1003, 3:50–67, 5:59–5:4. Thus, we find that Harris's field is memory power supply, and more specifically, switchable memory power supplies.

As discussed, the '373 patent describes its related art as making tradeoffs between performance and power when choosing voltage and frequency for processors and memory. Ex. 1001, 1:12–25. While the '373 patent describes determining the minimum operating voltage for each part and storing that determined value (*id.* at 2:3–37, 6:22–8:15), its disclosures are considerably broader in scope. The patent describes selecting memory voltage based on multiple considerations, such as using the logic voltage when it is higher than the memory minimum operating voltage, or a

variety of minimum voltages depending on operating circumstances. *Id.* at 3:30–5:41. As to the system controlling a memory's power supply, the '373 patent describes mechanisms that may be used to control a memory's power supply, such as power supply selector 21. *Id.* at 2:52–59, 5:42–58. It details operation of the power supply controller 28 and selector 21. *Id.* at 8:33–9:4. The '373 patent describes alternatively that memory may be permanently coupled to a particular voltage bus that is scaled to provide the desired power. *Id.* at 2:59–61, 5:61–67.

The disclosures regarding mechanisms for controlling the memory power supply show that the '373 patent's field is broader than just determining the minimum operating voltage. We find that the '373 patent's field includes switchable memory power supplies, supporting that Harris is from the same field as the '373 patent.

As to whether Harris is reasonably pertinent to the problem addressed by the '373 patent, Petitioner contends that the '373 patent addresses "lowering power consumption in integrated circuits, considering that 'different types of circuitry within a data processing system may have different ranges of allowable operating voltages' and that 'the processor may be able to operate at a lower voltage than is possible for the memory.'" Pet. Reply 19 (quoting Ex. 1001, 1:12–25, 2:5–7). Petitioner contends that Harris addresses the same problem with its circuit to "ensure the memory is provided with sufficient voltage to avoid data loss." Pet. 14–15 (citing Ex. 1003, 3:54–56, 3:64–67 (Harris's disclosure of switching memory power supply "to avoid memory data loss")).

Patent Owner's expert agrees that the '373 patent addresses "the problem of providing different voltages to different parts of the circuit" to

accommodate different "allowable operating voltages." PO Resp. 49 (quoting Ex. 2052 ¶ 159). As discussed above, Harris discloses a mechanism for providing different voltages to different parts of its circuit, whether for testing or low-power operation. Ex. 1003, 3:50–67, 5:59–5:4. We find that Harris is reasonably pertinent to the problem of providing different voltages to different parts of the circuit. While the '373 patent addresses other problems also, that does not undermine the problem to which Harris is reasonably pertinent. *See Ethicon LLC v. Intuitive Surgical, Inc.*, No. 2021-1601, 2022 WL 1576779, at *4 (Fed. Cir. May 19, 2022) (nonprecedential) (holding that the patent owner's identification of an additional problem beyond that supporting analogous art was irrelevant); *Donner Tech., LLC v. Pro Stage Gear, LLC*, 979 F.3d 1353, 1361 (Fed. Cir. 2020) (noting the analysis considers "one or more problems to which the claimed invention relates").

Accordingly, Harris is analogous art to the '373 patent because it is both from the same field of endeavor and reasonably pertinent to a problem confronting the inventor of the '373 patent.

8. Abadeer is available as prior art

Patent Owner contends that Abadeer is not available as prior art in an *inter partes* review because section 311(b) of 35 U.S.C. limits *inter partes* reviews to "patents or printed publications," whereas Abadeer was neither as of the '373 patent's filing date. PO Resp. 53–58. In Patent Owner's view, an *inter partes* review may not consider a reference that, like Abadeer, was published after the challenged patent's filing date, notwithstanding 35 U.S.C. § 102(e). *Id.* at 55.

Section 311(b) provides that an *inter partes* review may assert "a ground that could be raised under section 102 or 103 and only on the basis of prior art consisting of patents or printed publications." 35 U.S.C. § 311(b). Pre-AIA section 102(e) provides for unpatentability based on "an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for" the challenged patent. 35 U.S.C. § 102(e)(1) (2006). Petitioner argues that section 311(b) thus applies to art, like Abadeer, that is a printed publication that can be raised under section 102(e). Pet. Reply 19–20.

We agree with Petitioner. The Federal Circuit held in *Purdue Pharma L.P. v. Iancu* that an asserted patent application published on December 12, 2002, *after* the August 6, 2002, effective priority date of a challenged patent, but filed on August 30, 2001, *before* the challenged patent's effective priority date, nonetheless qualified as prior art that could be used in an *inter partes* review based on its pre-AIA section 102(e) application filing date . *Purdue Pharma*, 767 F. App'x 918, 925 (Fed. Cir. 2019) (nonprecedential). While the court did not consider the specific argument raised here—that *inter partes* reviews categorically may not rely on patent applications published after the challenged patent's priority date—*Purdue Pharma* signals an endorsement of the ability to use such publications as section 102(e) art in *inter partes* reviews.

According published applications an effective date as of their filing, as defined by section 102(e)(1), is consistent with according patents an effective date as of their filing, as defined by section 102(e)(2). In *Becton, Dickinson & Co. v. Baxter Corp. Englewood*, 998 F.3d 1337 (Fed. Cir. 2021), the Federal Circuit held that section 102(e)(2) applied to a patent

that had been later canceled, making that former patent available as prior art in an *inter partes* review. *Becton, Dickinson*, 998 F.3d at 1345. In its decision, the Federal Circuit noted and rejected the patent owner's argument that a 102(e)(2) patent could not be considered a prior-art patent before the date it was actually made public, i.e., the date it issued. *Id.* at 1345 n.7. We do not agree with Patent Owner that *Becton, Dickinson* is irrelevant because it concerned an issued patent (PO Sur-Reply 23 n.5). Rather, it supports that *inter partes* reviews properly consider prior-art references with effective dates prior to their actual publication dates.

While Patent Owner argues that section 311's "patents or printed publications" does not encompass a published patent application that is prior art under section 102(e)(1), we do not agree. *See* PO Resp. 53–57. Patent Owner relies on case law holding that a "printed publication" under sections 102(a) and (b) must be publicly available as of the challenged patent's priority date, but as noted, Petitioner relies on Abadeer being a printed publication having an effective date determined by its filing date under section 102(e)(1) rather than its publication date. In our view, section 311's reference generally to section 102 indicates that applicable "printed publications" include published applications under section 102(e)(1).

9. Conclusion regarding claim 1

We have considered the full record, including evidence and arguments presented by Petitioner and Patent Owner on whether Harris, Abadeer, and Zhang teach or suggest claim 1's limitations, whether there was a reason that skilled artisans at the time would have combined Harris, Abadeer, and Zhang as asserted, and whether objective indicia indicate the claims would

not have been obvious. Based on the full record, we conclude that Petitioner has shown by a preponderance of the evidence that claim 1 would have been obvious over Harris, Abadeer, and Zhang.

10. Additional claims

Petitioner provides contentions for claims 2–7, 9–11, and 13–16, generally relying on its contentions for claim 1, addressing differences in the language of independent claims 9 and 16, and identifying disclosures teaching the limitations of the dependent claims. Pet. 47–67. Other than as discussed above regarding claim 1, Patent Owner does not dispute Petitioner's contentions. We have reviewed the record, including Patent Owner's asserted objective indicia of nonobviousness, and determine that Petitioner has shown claims 2–7, 9–11, and 13–16 would have been obvious over Harris, Abadeer, and Zhang for the reasons discussed above, and because Petitioner has shown that the combination teaches all the limitations recited in claims 2–7, 9–11, and 13–16.

C. UNPATENTABILITY OVER HARRIS, ABADEER, ZHANG, AND CORNWELL

For claims 2, 11, and 12, which depend from claim 1 or claim 9, Petitioner relies on its contentions for claims 1 and 9, and further points to Cornwell's disclosures relevant to the limitations in claims 2, 11, and 12. Pet. 67–72. Other than as discussed above, Patent Owner does not challenge those contentions. We have reviewed Petitioner's contentions and determine Petitioner has shown claims 2, 11, and 12 would have been obvious over Harris, Abadeer, Zhang, and Cornwell for the reasons discussed above, and because Petitioner has shown that the combination teaches all the limitations recited in claims 2, 11, and 12 and has provided reasoning with a rational

underpinning to explain why a person having ordinary skill in the art at the time of the invention would have combined the references as asserted.

D. Unpatentability over Harris, Abadeer, Zhang, and Bilak

For claim 8, which depends from claim 1, Petitioner relies on its contentions for claim 1, and further points to Bilak's disclosures relevant to claim 8's limitations. Pet. 72–74. Other than its arguments for the patentability of claim 1, Patent Owner does not challenge Petitioner's contentions for claim 8 or introduce secondary considerations evidence specific to claim 8. We have reviewed Petitioner's contentions and determine Petitioner has shown claim 8 would have been obvious over Harris, Abadeer, Zhang, and Bilak for the reasons discussed above, and because Petitioner has shown that the combination teaches all the limitations recited in claim 8 and has provided reasoning with a rational underpinning to explain why a person having ordinary skill in the art at the time of the invention would have combined the references as asserted.

E. Constitutional Standing

Patent Owner argues that an *inter partes* review where the petitioner lacks constitutional injury-in-fact is unconstitutional. PO Resp. 58–62. We agree with Petitioner that Patent Owner's argument contradicts precedent. Pet. Reply 25; *Cuozzo Speed Techs., LLC v. Lee*, 579 U.S. 261, 279 (2016) ("Parties that initiate the proceeding need not have a concrete stake in the outcome; indeed, they may lack constitutional standing."); *Consumer Watchdog v. Wisconsin Alumni Rsch. Found.*, 753 F.3d 1258, 1261 (Fed. Cir. 2014) ("Article III standing is not necessarily a requirement to appear before an administrative agency . . . ."). We further agree that, because Intel

has been joined as a Petitioner, Patent Owner's argument does not apply to this proceeding. Pet. Reply 26.

III. CONCLUSION[9]

For the reasons discussed and based on the entire record, Petitioner has shown by a preponderance of the evidence that claims 1–16 are unpatentable.

In summary:

Claim(s)	35 U.S.C. §	Reference(s)/Basis	Claim(s) Shown Unpatentable	Claim(s) Not Shown Unpatentable
1–7, 9–11, 13–16	103	Harris, Abadeer, Zhang	1–7, 9–11, 13–16	
2, 11, 12	103	Harris, Abadeer, Zhang, Cornwell	2, 11, 12	
8	103	Harris, Abadeer, Zhang, Bilak	8	
Overall Outcome			1–16	

IV. ORDER

In consideration of the foregoing, it is hereby:

[9] Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. *See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. §§ 42.8(a)(3), (b)(2).

ORDERED that Petitioner has shown by a preponderance of the evidence that claims 1–16 of the '373 patent are unpatentable;

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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