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NEW CONTINUATION/DIVISIONAL PATENT APPLICATION TRANSMITTAL UNDER 37 C.F.R. §1.53(b)

This is a request for filing a continuation application under 37 C.F.R. §1.53(b) of pending Patent Application No. **12/077,503** filed on **March 18, 2008**, entitled **MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNDIRECTIONAL SERIAL BIT CHANNELS**, by the following named inventor(s):

(a) Full Name: **William W. Y. Chu**

1. Enclosed are:

and including:
[X] (55) pages of description (before the claims);
[X] (11) pages of claims ((43) total claims; (13) independent claims);
[X] One (1) Sheet of Abstract;
[X] (24) sheets of drawing(s) including Figures 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 19b, 20, 21, 22 and 23 .

1. Also enclosed are:
[X] Executed Declaration
[X] Power by Assignee and Statement Under 37 C.F.R. §3.73(b)

2. Applicant Claims Entitlement to Small Entity Status. The filing fee has been calculated as follows [] and in accordance with the enclosed preliminary amendment:

	NO. OF CLAIMS		EXTRA CLAIMS	RATE	FEE
Basic Application Fee – (EFS Filing Fee not reduced for small entity of $82.00, search fee of $270, examination fee of $110)					$462.00
Total Claims	43	- 20 =	23	x $26.00	598.00
Independent Claims	13	- 3 =	10	x $110.00	1,100.00
If multiple dependent claims are presented, add $195.00					
Total Application Fee					2,160.00
Other fees: (specify)					
TOTAL FEE DUE					**$2,160.00**

Intel Corporation v. ACQIS LLC
Intel Corp.'s Exhibit 1042
Ex. 1042, Page 1

[X] Please charge $2,160.00 to Deposit Account No. 50-1283 for the total fee.

[X] The Director is hereby authorized to charge any appropriate fees under 37 C.F.R. §§1.16, 1.17, and 1.21 that may be required by this paper, and to credit any overpayment, to Deposit Account No. 50-1283.

3. Please direct all correspondence concerning this application to:

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MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNDIRECTIONAL SERIAL BIT CHANNELS

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of U.S. Application No. 12/077,503 filed March 18, 2008, which is a continuation of U.S. nonprovisional Application No. 11/166,656, filed June 24, 2005 (Now U.S. Patent No. 7,376,779), which is a continuation of U.S. nonprovisional Application No. 11/097,694, filed March 31, 2005 (Now U.S. Patent No. 7,363,415), which is a continuation of U.S. nonprovisional Application No. 10/772,214, filed February 3, 2004 (Now U.S. Patent No. 7,099,981), which is a continuation of U.S. nonprovisional Application No. 09/569,758, filed May 12, 2000 (Now U.S. patent no. 6,718,415), and which claimed priority to U.S. Provisional Application No. 60/134,122 filed May 14, 1999. These applications are hereby incorporated by reference in their entirety.

BACKGROUND OF THE INVENTION

[0002] The present invention relates to computing devices. More particularly, the present invention provides a system including a plurality of computer modules that can independently operate to provide backup capability, dual processing, and the like. Merely by way of example, the present invention is applied to a modular computing environment for desk top computers, but it will be recognized that the invention has a much wider range of applicability. It can be applied to a server as well as other portable or modular computing applications.

[0003] Many desktop or personal computers, which are commonly termed PCs, have been around and used for over ten years. The PCs often come with state-of-art microprocessors such as the Intel PentiumTM microprocessor chips. They also include a hard or fixed disk drive such as memory in the giga-bit range. Additionally, the PCs often include a random access memory integrated circuit device such as a dynamic random access memory device, which is commonly termed DRAM. The DRAM devices now provide up to millions of memory cells (i.e., mega-bit) on a single slice of silicon. PCs also include a high resolution display such as cathode ray tubes or CRTs. In most cases,

the CRTs are at least 15 inches or 17 inches or 20 inches in diameter. High resolution flat panel displays are also used with PCs.

[0004] Many external or peripheral devices can be used with the PCs. Among others, these peripheral devices include mass storage devices such as a ZipTM Drive product sold by Iomega Corporation of Utah. Other storage devices include external hard drives, tape drives, and others. Additional devices include communication devices such as a modem, which can be used to link the PC to a wide area network of computers such as the Internet. Furthermore, the PC can include output devices such as a printer and other output means. Moreover, the PC can include special audio output devices such as speakers the like.

[0005] PCs also have easy to use keyboards, mouse input devices, and the like. The keyboard is generally configured similar to a typewriter format. The keyboard also has the length and width for easily inputting information by way of keys to the computer. The mouse also has a sufficient size and shape to easily move a curser on the display from one location to another location.

[0006] Other types of computing devices include portable computing devices such as "laptop" computers and the like. Although somewhat successful, laptop computers have many limitations. These computing devices have poor display technology. In fact, these devices often have a smaller flat panel display that has poor viewing characteristics. Additionally, these devices also have poor input devices such as smaller keyboards and the like. Furthermore. these devices have limited common platforms to transfer information to and from these devices and other devices such as PCs.

[0007] Up to now, there has been little common ground between these platforms including the PCs and laptops in terms of upgrading, ease-of-use, cost, performance, and the like. Many differences between these platforms, probably somewhat intentional, has benefited computer manufacturers at the cost of consumers. A drawback to having two separate computers is that the user must often purchase both the desktop and laptop to have "total" computing power, where the desktop serves as a "regular" computer and the laptop serves as a "portable" computer. Purchasing both computers is often costly and runs "thousands" of dollars. The user also wastes a significant amount of time transferring software and data between the two types of computers. For example, the user must often couple the portable computer to a local area network (i.e., LAN), to a serial

port with a modem and then manually transfer over files and data between the desktop and the portable computer. Alternatively, the user often must use floppy disks to "zip" up files and programs that exceed the storage capacity of conventional floppy disks, and transfer the floppy disk data manually.

[0008] Another drawback with the current model of separate portable and desktop computer is that the user has to spend money to buy components and peripherals the are duplicated in at least one of these computers. For example, both the desktop and portable computers typically include hard disk drives, floppy drives, CD-ROMs, computer memory, host processors, graphics accelerators, and the like. Because program software and supporting programs generally must be installed upon both hard drives in order for the user to operate programs on the road and in the office, hard disk space is often wasted.

[0009] One approach to reduce some of these drawbacks has been the use of a docking station with a portable computer. Here, the user has the portable computer for "on the road" use and a docking station that houses the portable computer for office use.

[0010] Similar to separate desktop and portable computers, there is no commonality between two desktop computers. To date, most personal computers are constructed with a single motherboard that provides connection for CPU and other components in the computer. Dual CPU systems have been available through Intel's slot 1 architecture. For example, two Pentium II cartridges can be plugged into two "slot 1" card slots on a motherboard to form a Dual-processor system. The two CPU's share a common host bus that connects to the rest of the system, e.g. main memory, hard disk drive, graphics subsystem, and others. Dual CPU systems have the advantage of increased CPU performance for the whole system. Adding a CPU cartridge requires no change in operating systems and application software. However, dual CPU systems may suffer limited performance improvement if memory or disk drive bandwidth becomes the limiting factor. Also, dual CPU systems have to time-share the processing unit in running multiple applications. CPU performance improvement efficiency also depends on software coding structure. Dual CPU systems provide no hardware redundancy to help fault tolerance. In running multiple applications, memory and disk drive data throughput will become the limiting factor in improving performance with multi-processor systems.

[0011] The present invention generally relates to computer interfaces. More specifically, the present invention relates to an interface channel that interfaces two computer interface buses that operate under protocols that are different from that used by the interface channel.

[0012] Interfaces coupling two independent computer buses are well known in the art. A block diagram of a computer system utilizing such a prior art interface is shown in Fig. 5. In Fig. 5, a primary peripheral component interconnect (PCI) bus 505 of a notebook PC 500 is coupled to a secondary PCI bus 555 in a docking system 550 (also referred to as docking station 550) through high pin count connectors 501 and 502, which are normally mating connectors. The high pin count connectors 501 and 502 contain a sufficiently large number of pins so as to carry PCI bus signals between the two PCI buses without any translation. The main purpose for interfacing the two independent PCI buses is to allow transactions to occur between a master on one PCI bus and a target on the other PCI bus. The interface between these two independent PCI buses additionally includes an optional PCI to PCI bridge 560, located in the docking station 550, to expand the add on capability in docking station 550. The bridge 560 creates a new bus number for devices behind the bridge 560 so that they are not on the same bus number as other devices in the system thus increasing the add on capability in the docking station 550.

[0013] An interface such as that shown in Fig. 5 provides an adequate interface between the primary and secondary PCI buses. However, the interface is limited in a number of ways. The interface transfers signals between the primary and secondary PCI buses using the protocols of a PCI bus. Consequently, the interface is subject to the limitations under which PCI buses operate. One such limitation is the fact that PCI buses are not cable friendly. The cable friendliness of the interface was not a major concern in the prior art. However, in the context of the computer system of the present invention, which is described in the present inventor's (William W.Y. Chu's) application for "Personal Computer Peripheral Console With Attached Computer Module" filed concurrently with the present application on Sep. 8, 1998 and incorporated herein by reference, a cable friendly interface is desired for interfacing an attached computer module (ACM) and a peripheral console of the present invention. Furthermore, as a result of operating by PCI protocols, the prior art interface includes a very large number of signal channels with a corresponding large number of conductive lines (and a similarly large number of pins in

the connectors of the interface) that are commensurate in number with the number of signal lines in the PCI buses which it interfaces. One disadvantage of an interface having a relatively large number of conductive lines and pins is that it costs more than one that uses a fewer number of conductive lines and pins. Additionally, an interface having a large number of conductive lines is bulkier and more cumbersome to handle. Finally, a relatively large number of signal channels in the interface renders the option of using differential voltage signals less viable because a differential voltage signal method would require duplicating a large number of signal lines. It is desirable to use a low voltage differential signal (LVDS) channel in the computer system of the present invention because an LVDS channel is more cable friendly, faster, consumes less power, and generates less noise, including electromagnetic interferences (EMI), than a PCI channel. The term LVDS is herein used to generically refer to low voltage differential signals and is not intended to be limited to any particular type of LVDS technology.

[0014] Thus, what is needed are computer systems that can have multiple computer modules. Each computer module has dedicated memory and disk drive, and can operate independently.

BRIEF SUMMARY OF THE INVENTION

[0015] According to the present invention, a technique including a method and device for multi-module computing is provided. In an exemplary embodiment, the present invention provides a system including a plurality of computer modules that can independently operate to provide backup capability, dual processing, and the like.

[0016] In a specific embodiment, the present invention provides a computer system for multi-processing purposes. The computer system has a console comprising a first coupling site and a second coupling site, e.g., computer module bay. Each coupling site comprises a connector. The console is an enclosure that is capable of housing each coupling site. The system also has a plurality of computer modules, where each of the computer modules is coupled to one of the connectors. Each of the computer modules has a processing unit, a main memory coupled to the processing unit, a graphics controller coupled to the processing unit, and a mass storage device coupled to the processing unit. Each of the computer modules is substantially similar in design to each other to provide independent processing of each of the computer modules in the computer system.

[0017] In an alternative specific embodiment, the present invention provides a multi-processing computer system. The system has a console comprising a first coupling site and a second coupling site. Each coupling site comprises a connector. The console is an enclosure that is capable of housing each coupling site. The system also has a plurality of computer modules, where each of the computer modules is coupled to one of the connectors. Each of the computer modules has a processing unit, a main memory coupled to the processing unit, a graphics controller coupled to the processing unit, a mass storage device coupled to the processing unit, and a video output coupled to the processing unit. Each of the computer modules is substantially similar in design to each other to provide independent processing of each of the computer modules in the computer system. A video switch circuit is coupled to each of the computer modules through the video output. The video switch is configured to switch a video signal from any one of the computer modules to a display.

[0018] Numerous benefits are achieved using the present invention over previously existing techniques. In one embodiment, the invention provides improved processing and maintenance features. The invention can also provide increased CPU performance for the whole system. The invention also can be implemented without changes in operating system and application software. The present invention is also implemented using conventional technologies that can be provided in the present computer system in an easy and efficient manner.

[0019] In another embodiment, the invention provides at least two users to share the same modular desktop system. Each user operates on a different computer module. The other peripheral devices, i.e. CDROM, printer, DSL connection, etc. can be shared. This provides lower system cost, less desktop space and more efficiency. Depending upon the embodiment, one or more of these benefits can be available. These and other advantages or benefits are described throughout the present specification and are described more particularly below.

[0020] In still further embodiments, the present invention provides methods of using multiple computer modules.

[0021] The present invention encompasses an apparatus for bridging a first computer interface bus and a second computer interface bus. where each of the first and second

computer interface buses have a number of parallel multiplexed address/data bus lines and operate at a clock speed in a predetermined clock speed range having a minimum clock speed and a maximum clock speed. The apparatus comprises an interface channel having a clock line and a plurality of bit lines for transmitting bits; a first interface controller coupled to the first computer interface bus and to the interface channel to encode first control signals from the first computer interface bus into first control bits to be transmitted on the interface channel and to decode second control bits received from the interface channel into second control signals to be transmitted to the first computer interface bus; and a second interface controller coupled to the interface channel and the second computer interface bus to decode the first control bits from the interface channel into third control signals to be transmitted on the second computer interface bus and to encode fourth control signals from the second computer interface bus into the second control bits to be transmitted on the interface channel.

[0022] In one embodiment, the first and second interface controllers comprise a host interface controller (HIC) and a peripheral interface controller (PIC), respectively, the first and second computer interface buses comprise a primary PCI and a secondary PCI bus, respectively, and the interface channel comprises an LVDS channel.

[0023] The present invention overcomes the aforementioned disadvantages of the prior art by interfacing two PCI or PCI-like buses using a non-PCI or non-PCI-like channel. In the present invention, PCI control signals are encoded into control bits and the control bits, rather than the control signals that they represent, are transmitted on the interface channel. At the receiving end, the control bits representing control signals are decoded back into PCI control signals prior to being transmitted to the intended PCI bus.

[0024] The fact that control bits rather than control signals are transmitted on the interface channel allows using a smaller number of signal channels and a correspondingly small number of conductive lines in the interface channel than would otherwise be possible. This is because the control bits can be more easily multiplexed at one end of the interface channel and recovered at the other end than control signals. This relatively small number of signal channels used in the interface channel allows using LVDS channels for the interface. As mentioned above, an LVDS channel is more cable friendly, faster, consumes less power, and generates less noise than a PCI bus channel, which is used in the prior art to interface two PCI buses. Therefore, the present invention advantageously

uses an LVDS channel for the hereto unused purpose of interfacing PCI or PCI-like buses. The relatively smaller number of signal channels in the interface also allows using connectors having smaller pins counts. As mentioned above an interface having a smaller number of signal channels and, therefore, a smaller number of conductive lines is less bulky and less expensive than one having a larger number of signal channels. Similarly, connectors having a smaller number of pins are also less expensive and less bulky than connectors having a larger number of pins.

[0025] In one embodiment, the present invention encompasses an apparatus for bridging a first computer interface bus and a second computer interface bus, in a microprocessor based computer system where each of the first and second computer interface buses have a number of parallel multiplexed address/data bus lines and operate at a clock speed in a predetermined clock speed range having a minimum clock speed and a maximum clock speed. The apparatus comprises an interface channel having a clock channel and a plurality of bit channels for transmitting bits; a first interface controller coupled to the first computer interface bus and to the interface channel to encode first control signals from the first computer interface bus into first control bits to be transmitted on the interface channel and to decode second control bits received from the interface channel into second control signals to be transmitted to the first computer interface bus; and a second interface controller coupled to the interface channel and the second computer interface bus to decode the first control bits from the interface channel into third control signals to be transmitted on the second computer interface bus and to encode fourth control signals from the second computer interface bus into the second control bits to be transmitted on the interface channel.

[0026] In one embodiment, the first and second interface controllers comprise a host interface controller (HIC) and a peripheral interface controller (PIC), respectively, the first and second computer interface buses comprise a primary PCI and a secondary PCI bus, respectively, and the interface channel comprises an LVDS channel.

[0027] In a preferred embodiment, the interface channel has a plurality of serial bit channels numbering fewer than the number of parallel bus lines in each of the PCI buses and operates at a clock speed higher than the clock speed at which any of the bus lines operates. More specifically, the interface channel includes two sets of unidirectional serial bit channels which transmit data in opposite directions such that one set of bit

channels transmits serial bits from the HIC to the PIC while the other set transmits serial bits from the PIC to the HIC. For each cycle of the PCI clock, each bit channel of the interface channel transmits a packet of serial bits.

[0028] The HIC and PIC each include a bus controller to interface with the first and second computer interface buses, respectively, and to manage transactions that occur therewith. The HIC and PIC also include a translator coupled to the bus controller to encode control signals from the first and second computer interface buses, respectively, into control bits and to decode control bits from the interface channel into control signals. Additionally, the HIC and PIC each include a transmitter and a receiver coupled to the translator. The transmitter converts parallel bits into serial bits and transmits the serial bits to the interface channel. The receiver receives serial bits from the interface channel and converts them into parallel bits.

[0029] According to the present invention, a technique including a method and device for securing a computer module using a password in a computer system is provided. In an exemplary embodiment, the present invention provides a security system for an attached computer module ("ACM"). In an embodiment, the ACM inserts into a Computer Module Bay (CMB) within a peripheral console to form a functional computer.

[0030] In a specific embodiment, the present invention provides a computer module. The computer module has an enclosure that is insertable into a console. The module also has a central processing unit (i.e., integrated circuit chip) in the enclosure. The module has a hard disk drive in the enclosure, where the hard disk drive is coupled to the central processing unit. The module further has a programmable memory device in the enclosure, where the programmable memory device can be configurable to store a password for preventing a possibility of unauthorized use of the hard disk drive and/or other module elements. The stored password can be any suitable key strokes that a user can change from time to time. In a further embodiment, the present invention provides a permanent password or user identification code stored in flash memory, which also can be in the processing unit, or other integrated circuit element. The permanent password or user identification code is designed to provide a permanent "finger print" on the attached computer module.

[0031] In a specific embodiment, the present invention provides a variety of methods. In one embodiment, the present invention provides a method for operating a computer system such as a modular computer system and others. The method includes inserting an attached computer module ("ACM") into a bay of a modular computer system. The ACM has a microprocessor unit (e.g.. microcontroller, microprocessor) coupled to a mass memory storage device (e.g., hard disk). The method also includes applying power to the computer system and the ACM to execute a security program, which is stored in the mass memory storage device. The method also includes prompting for a user password from a user on a display (e.g., fiat panel, CRT). In a further embodiment, the present method includes a step of reading a permanent password or user identification code stored in flash memory, or other integrated circuit element. The permanent password or user identification code provides a permanent finger print on the attached computer module. The present invention includes a variety of these methods that can be implemented in computer codes, for example, as well as hardware.

[0032] Numerous benefits are achieved using the present invention over previously existing techniques. The present invention provides mechanical and electrical security systems to prevent theft or unauthorized use of the computer system in a specific embodiment. Additionally, the present invention substantially prevents accidental removal of the ACM from the console. In some embodiments, the present invention prevents illegal or unauthorized use during transit. The present invention is also implemented using conventional technologies that can be provided in the present computer system in an easy and efficient manner. Depending upon the embodiment, one or more of these benefits can be available. These and other advantages or benefits are described throughout the present specification and are described more particularly below.

[0033] These and other embodiments of the present invention, as well as its advantages and features, are described in more detail in conjunction with the text below and attached Figs.

BRIEF DESCRIPTION OF THE DRAWINGS

[0034] Fig. 1 is a simplified diagram of a computer system according to an embodiment of the present invention;

[0035] Fig. 2 is a simplified block diagram of a computer system according to an alternative embodiment of the present invention;

[0036] Fig. 3 is a simplified block diagram of a compeer system according to a further alternative embodiment of the present invention, and

[0037] Fig. 4 is a simplified flow diagram of a method according to an embodiment of the present invention.

[0038] Fig. 5 is a block diagram of a computer system using a prior art interface between a primary and a secondary PCI bus.

[0039] Fig. 6 is a block diagram of one embodiment of a computer system using the interface of the present invention.

[0040] Fig. 7 is a partial block diagram of a computer system using the interface of the present invention as a bridge between the north and south bridges of the computer system.

[0041] Fig. 8 is a partial block diagram of a computer system in which the north and south bridges are integrated with the host and peripheral interface controllers, respectively.

[0042] Fig. 9 is a block diagram of one embodiment of the host interface controller and the peripheral interface controller of the present invention.

[0043] Fig. 10 is a detailed block diagram of one embodiment of the host interface controller of the present invention.

[0044] Fig. 11 is a detailed block diagram of one embodiment of the PIC of the present invention.

[0045] Fig. 12 is a table showing the symbols, signals, data rate and description of signals in a first embodiment of the XPBus.

[0046] Fig. 13 is a table showing the information transmitted on the XPBus during two clock cycles of the XPBus in one embodiment of the present invention where 10 data bits transmitted in each clock cycle of the XPBus.

[0047] Fig. 14 is a table showing information transmitted on the XPBus during four clock cycles of the XPBus in another embodiment of the present invention where 10 data bits are transmitted in each clock cycle of the XPBus.

[0048] Fig. 15 is a schematic diagram of the signal lines PCK, PD0 to PD3, and PCN.

[0049] Fig. 16 is a table showing the names, types, number of pins dedicated to, and the description of the primary bus PCI signals.

[0050] FIG. 17 is a block diagram of one embodiment of a computer system employing the present invention.

[0051] FIG. 18 is a block diagram of an attached computing module (ACM).

[0052] FIG. 19 illustrates an external view of one embodiment of an ACM.

[0053] FIG. 19b illustrates one possible embodiment of a computer bay.

[0054] FIG. 20 illustrates the internal component layout for one embodiment of an ACM.

[0055] FIG. 21 is a block diagram of a peripheral console (PCON).

[0056] FIG. 22 is a simplified layout diagram of a security system for a computer system according to an embodiment of the present invention; and

[0057] FIG. 23 is a simplified block diagram of a security system for a computer module according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0058] According to the present invention, a technique including a method and device for multi-module computing is provided. In an exemplary embodiment, the present invention provides a system including a plurality of computer modules that can independently operate to provide backup capability, dual processing, and the like.

[0059] Fig. 1 is a simplified diagram of a computer system 100 according to an embodiment of the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. The computer system 100 includes an

attached computer module (i.e., ACM) 113, a desktop console 101, among other elements. The computer system also has another ACM module 117. Each ACM module has a respective slot 121, 119, which mechanically houses and electrically couples each ACM to the computer console. Also shown is a display 111, which connects to the console. Additionally, keyboard 109 and mouse 115 are also shown. A second display 102, keyboard 105, and mouse 107 can be coupled to the console in some optional embodiments to allow more than one user to operate the computer system. The computer system is modular and has a variety of components that are removable. Some of these components (or modules) can be used in different computers, workstations, computerized television sets, and portable or laptop units.

[0060] In the present embodiment, each ACM 113 includes computer components. as will be described below, including a central processing unit ("CPU"). IDE controller, hard disk drive, computer memory, and the like. The computer module bay (i.e., CMB) 121 is an opening or slot in the desktop console. The CMB houses the ACM and provides communication to and from the ACM. The CMB also provides mechanical protection and support to the ACM. The CMB has a mechanical alignment mechanism for mating a portion of the ACM to the console. The CMB further has thermal heat dissipation sinks, electrical connection mechanisms, and the like. Some details of the ACM can be found in co-pending Patent Application Nos. 09/149,882 and 09/149,548 filed 9/8/98, commonly assigned, and hereby incorporated by reference for all purposes.

[0061] In a specific embodiment, the present multiple computer module system has a peripheral console that has two or more computer bays that can receive a removable computer module or ACM. Multiple computer module system can function as a personal computer with only one ACM and the peripheral console. The second and additional ACM can be added later to increase overall system performance and reliability. The ACM operates independently as self-contained computer, communicates with each other through a high-speed serial communication and share most peripheral devices within the peripheral console. Each ACM controls its independent graphics subsystem and drives separate video output signals. A practical implementation is a dual ACM system. In a dual ACM system, two monitors can be used to display the two ACMs' graphics outputs at the same time. For a single monitor, a RGB switch is used to switch between the video outputs of the two ACMs and can be controlled by a command from the user. Similarly,

input devices (i.e. keyboard and mouse) are switched between the two computer systems with a command from the user. Command from the user can be in the form of either a dedicated key on the keyboard or a special icon on the screen that the mouse can click on.

[0062] In most embodiments, the ACM includes an enclosure such as the one described with the following components, which should not be limiting:

1) A CPU with cache memory;
2) Core logic device or means;
3) Main memory;
4) A single primary Hard Disk Drive ("HDD") that has a security program;
5) Flash memory with system BIOS and programmable user password;
6) Operating System, application software, data files on primary HDD;
7) An interface device and connectors to peripheral console;
8) A software controllable mechanical lock, lock control means, and other accessories.

[0063] The ACM connects to a peripheral console with power supply, a display device, an input device, and other elements. Some details of these elements with the present system are described in more detail below. In a dual ACM system, the primary ACM can connect directly to the peripheral board in the peripheral console. The second ACM can connect either directly or indirectly to the peripheral board. For indirect connection, a receptacle board is added to allow a cable connection to the peripheral board. This is to facilitate the mechanical positioning of the second ACM inside the computer chassis. The receptacle board approach can even be used for the primary ACM if a high bandwidth peripheral bus, e.g. PCI Bus, is not connected from the primary ACM to the peripheral board.

[0064] The shared peripheral console has a chassis and a motherboard that connects the following devices:

1) Input means, e.g. keyboard and mouse,
2) Display means, e.g. RGB monitor,
3) Add-on means, e.g. PCI add-on slots,
4) Two Computer Module Bays (CMB) with connectors to two ACMs,

5) A serial communication Hub controller that interfaces to serial communication controller of both ACMs,

6) Shared storage subsystem, e.g. Floppy drive, CDROM drive, DVD drive, or 2nd Hard Drive,

7) Communication device, e.g. modem,

8) Power supply, and others.

[0065] The computer bay is an opening in the peripheral console that receives an ACM. CMB provides mechanical protection to ACM, mechanical alignment for connector mating, mechanical locking system to prevent theft and accidental removal, and connectors at the end of the opening for connecting to ACM. The interface bus between ACM and the peripheral console has a video bus, peripheral connections, serial communication connection, control signals and power connection. Video bus includes video output of graphics devices, i.e. analog RGB and control signals for monitor. Power connection supplies the power for ACM.

[0066] An implementation of peripheral sharing is the use of Ethernet controllers to bridge the communication between the two ACMs. Some of the peripheral devices residing in the peripheral console are shown in the simplified diagram of Fig. 2. As shown, the diagram is merely an illustration which should not limit the scope of the claims herein. One of ordinary skill in the art would recognize many other variations, alternatives, and modifications. As shown, a primary ACM 203 is connected to PCI peripheral devices in the peripheral console through the PCI bus 225 that passes through the connection between primary ACM 203 and peripheral console 201. As shown, ACM has a CPU module 207 coupled to the PCI bus through a North Bridge 211.

[0067] The CPU module can use a suitable microprocessing unit, microcontroller, digital signal processor, and the like. In a specific embodiment, the CPU module uses, for example, a 400 MHz Pentium II microprocessor module from Intel Corporation and like microprocessors from AMD Corporation, Cyrix Corporation (now National Semiconductor Corporation), and others. In other aspects, the microprocessor can be one such as the Compaq Computer Corporation Alpha Chip, Apple Computer Corporation PowerPC G3 processor, and the like. Further, higher speed processors are contemplated in other embodiments as technology increases in the future.

[0068] In the CPU module, peripheral controller 213 is coupled to BIOS/flash memory 217. Additionally, the peripheral controller is coupled to a clock control logic, a configuration signal, and a peripheral bus. The ACM has the hard drive module 215. Among other elements, the ACM includes north bridge 215, graphics subsystem 223 (e.g., graphics accelerator, graphics memory), an IDE controller, and other components. Adjacent to and in parallel alignment with the hard drive module 215 is the PCI bus. In a specific embodiment, North Bridge unit 211 often couples to a computer memory 209, to the graphics subsystem, and to the peripheral controller via the PCI bus. Graphics subsystem typically couples to a graphics memory, and other elements. IDE controller generally supports and provides timing signals necessary for the IDE bus. In the present embodiment, the IDE controller is embodied as part of a P114XE controller from Intel, for example. Other types of buses than IDE are contemplated, for example EIDE, SCSI, 1394, and the like in alternative embodiments of the present invention.

[0069] The hard drive module or mass storage unit 215 typically includes a computer operating system, application software program files, data files, and the like. In a specific embodiment, the computer operating system may be the Windows98 operating system from Microsoft Corporation of Redmond Washington. Other operating systems, such as WindowsNT, MacOS8, Unix, and the like are also contemplated in alternative embodiments of the present invention. Further, some typical application software programs can include Office98 by Microsoft Corporation, Corel Perfect Suite by Corel, and others. Hard disk module 215 includes a hard disk drive. The hard disk drive, however, can also be replaced by removable hard disk drives, read/write CD ROMs, flash memory, floppy disk drives, and the like. A small form factor, for example 2.5", is currently contemplated, however, other form factors, such as PC card, and the like are also contemplated. Mass storage unit 240 may also support other interfaces than IDE.

[0070] Among other features, the computer system includes an ACM with security protection.

[0071] The ACM also has a network controller, which can be an Ethernet controller 219, which is coupled to the North Bridge through the PCI bus. The North Bridge is coupled to the CPU. The Ethernet controller can be a 10/100 Base, such as Intel's 82559 or the like. Other types of network connection devices can also be used. For example, the

invention can use Gbit Ethernet 1394, and USB 2.0. The network controller couples to a hub 233 in the console, which includes shared peripheral system 201.

[0072] Also shown is the second ACM 205. The second ACM has the same or similar components as the first ACM. Here, like reference numerals have been used for easy cross-referencing, but is not intended to be limiting. In some embodiments, the secondary ACM is not connected to the PCI bus in the peripheral console directly. The secondary ACM 219 accesses peripheral devices controlled by the primary ACM through the Ethernet connection to the primary ACM, e.g. CD-ROM, or PCI modem. The implementation is not restricted to Ethernet serial communication and can use other high-speed serial communication such as USB 2.0, and 1394. The Ethernet hub is coupled to an external output port 235, which connects to an external network.

[0073] The primary hard disk drive in each ACM can be accessed by the other ACM as sharable hard drive through the Ethernet connection. This allows the easy sharing of files between the two independent computer modules. The Ethernet Hub Controller provides the high-speed communication function between the two computer modules. Ethernet data bandwidth of 100 Mbit/sec allows fast data communication between the two computer modules. The secondary ACM access peripheral devices of the primary ACM through the network connection provided by Ethernet link. The operating system, e.g. Windows98, provides the sharing of resources between the two ACMs. In some embodiments, critical data in one ACM can be backup into the other ACM.

[0074] The Ethernet hub also couples to PCI bus 239, which connects to PCI devices 241, 243, e.g., modem, SCSI controller. A flash memory 242 can also be coupled to the PCI bus. The flash memory can store passwords and security information, such as those implementations described in U.S. Serial No. 09/183,493, which is commonly owned, and hereby incorporated by reference. The hub 233 also couples to an I/O control 237, which connects to keyboard/mouse switch 245, which couples to keyboard/mouse 247. Optionally, the keyboard/mouse switch also couples to a second keyboard/house 259 via PS2 or USB signal line 251. The keyboard/mouse switch has at least a first state and a second state, which allow operation of respectively multiple keyboards or a single keyboard. The switch also couples to each I/O controller 221 in each ACM via lines 253, 255. The I/O control 237 also couples to an RGB switch 257, which allows video signals to pass to the first monitor 259. Alternatively, the RGB switch couples to a second

monitor 261. The RGB switch includes analog video switches such as MAXIM's MAX4545.

[0075] The peripheral system 201 also has an independent power supply 231 for each ACM. Each power supply provides power to each ACM. As merely an example, the power supply is a MICRO ATX 150W made by ENLIGHT, but can be others. The power supply is connected or coupled to each ACM through a separate line, for example. The independent power supply allows for independent operation of each ACM in some embodiments.

[0076] The above embodiments are described generally in terms of hardware and software. It will be recognized, however, that the functionality of the hardware can be further combined or even separated. The functionality of the software can also be further combined or even separated. Hardware can be replaced, at times, with software. Software can be replaced, at times, with hardware. Accordingly, the present embodiments should not be construed as limiting the scope of the claims here. One of ordinary skill in the art would recognize other variations, modifications, and alternatives.

[0077] Fig. 3 is a simplified block diagram 300 of a computer system according to an alternative embodiment of the present invention. This diagram is merely an example which should not limit the scope of the claims herein. One of ordinary skill in the art would recognizes many other variations, modifications, and alternatives. Like reference numerals are used in this Fig. as the previous Figs. for easy referencing, but are not intended to be limiting. As shown, each ACM includes common elements as the previous Fig. A primary ACM 203 is connected to PCI peripheral devices in the peripheral console through the PCI bus 225 that passes through the connection between primary ACM 203 and peripheral console 201. As shown, ACM has a CPU module 207 coupled to the PCI bus through a North Bridge 211.

[0078] The CPU module can use a suitable microprocessing unit, microcontroller, digital signal processor, and the like. In a specific embodiment, the CPU module uses, for example, a 400 MHz Pentium II microprocessor module from Intel Corporation and like microprocessors from AMD Corporation, Cyrix Corporation (now National Semiconductor Corporation), and others. In other aspects, the microprocessor can be one such as the Compaq Computer Corporation Alpha Chip, Apple Computer Corporation

PowerPC G3 processor, and the like. Further, higher speed processors are contemplated in other embodiments as technology increases in the future.

[0079] In the CPU module, peripheral controller 213 is coupled to BIOS/flash memory 217. Additionally, the peripheral controller is coupled to a clock control logic, a configuration signal, and a peripheral bus. The ACM has the hard drive module 215. Among other elements, the ACM includes north bridge 215, graphics subsystem 223 (e.g., graphics accelerator, graphics memory), an IDE controller, and other components. Adjacent to and in parallel alignment with the hard drive module 215 is the PCI bus. In a specific embodiment, North Bridge unit 211 often couples to a computer memory 209, to the graphics subsystem, and to the peripheral controller via the PCI bus. Graphics subsystem typically couples to a graphics memory, and other elements. IDE controller generally supports and provides timing signals necessary for the IDE bus. In the present embodiment, the IDE controller is embodied as part of a P114XE controller from Intel, for example. Other types of buses than IDE are contemplated, for example EIDE, SCSI, 1394, and the like in alternative embodiments of the present invention.

[0080] The hard drive module or mass storage unit 215 typically includes a computer operating system, application software program files, data files, and the like. In a specific embodiment, the computer operating system may be the Windows98 operating system from Microsoft Corporation of Redmond Washington. Other operating systems, such as WindowsNT, MacOS8, Unix, and the like are also contemplated in alternative embodiments of the present invention. Further, some typical application software programs can include Office98 by Microsoft Corporation, Corel Perfect Suite by Corel, and others. Hard disk module 215 includes a hard disk drive. The hard disk drive, however, can also be replaced by removable hard disk drives, read/write CD ROMs, flash memory, floppy disk drives, and the like. A small form factor, for example 2.5", is currently contemplated, however, other form factors, such as PC card, and the like are also contemplated. Mass storage unit 240 may also support other interfaces than IDE.

[0081] Among other features, the computer system includes an ACM with security protection.

[0082] The ACM also has a network controller, which can be coupled to a serial port 302, which is coupled to the PCI bus in the ACM. The serial port is coupled to the

peripheral console through a serial controller 301 in the serial console. The serial controller is connected to PCI bus 239. The serial controller is also coupled to a serial hub controller 303, which is coupled to the PCI bus and a second ACM. In a specific embodiment, a receptacle board 310 is added to connect to the second ACM. The purpose of the receptacle board is to allow a cable connection 307 to the peripheral board 300. The cable connection is possible because the signals needed to connect to the peripheral board can be limited to video, I/O, serial communication, and power. The serial communication controller can be placed on the receptacle board and not in the ACM. As shown, the serial bus controller couples to the PCI bus. The receptacle board also couples to power, graphics subsystem, I/O controller, and other elements, which may be on a common bus. The overall operation of the present configuration is similar to the previous one except it operates in serial communication mode.

[0083] The Dual ACM system can support different usage models:

[0084] 1. One user using both ACMs concurrently with 1 or 2 monitors, and a common keyboard/mouse.

[0085] 2. Two users using the two separate ACMs at the same time with separate monitors and keyboard/mouse. The 2 users share peripherals, e.g., printer, CDROM, and others. The two users share external networking.

[0086] To support 1 monitor for both ACMs, a video switch in the peripheral console is used to switch between the video outputs of the two ACMs. The system can be set to support either 1 monitor or 2-monitor mode. The user presses a special key on the keyboard or a special icon on the screen to switch the screen display from one ACM to the other. This same action causes the keyboard and mouse connections to switch from one ACM to the other ACM.

[0087] A dual ACM system can save space, wiring, and cost for a 2-person PC setup, with the added benefit that both PC systems can be accessed from one user site for increased system performance if the other user is not using the system. Files can be copied between the primary drive of both system and provides protection against a single ACM failure. Software needs to be developed to manage the concurrent use of two PC subsystems, the automatic sharing of selected files between the two systems, and fault tolerance.

[0088] The design with more than two computer modules can be implemented with the use of multi-port, serial communication hub controller and multi-port I/O switches. In one embodiment, a peripheral console has four computer bays for four separate computer modules. The computer modules communicate through a four port Ethernet hub. The video, keyboard, and mouse switch will cycle through the connection from each computer module to the external monitor, keyboard, and mouse with a push button sequentially. This embodiment is useful for a server that performs different functions concurrently, e.g. email, application hosting, web hosting , firewall, etc.

[0089] The above embodiments are described generally in terms of hardware and software. It will be recognized, however, that the functionality of the hardware can be further combined or even separated. The functionality of the software can also be further combined or even separated. Hardware can be replaced, at times, with software. Software can be replaced, at times, with hardware. Accordingly, the present embodiments should not be construed as limiting the scope of the claims here. One of ordinary skill in the an would recognize other variations, modifications, and alternatives.

[0090] Fig. 4 is a simplified diagram of a method according to an embodiment of the present invention. This diagram is merely an example which should not limit the scope of the claims herein. One of ordinary skill in the art would recognize many other variations, modifications, and alternatives. The present diagram illustrates an automatic file backup procedure from one computer module to the other. As shown, a user selects (step 401) a certain file in one of the computer module for automatic backup. Next, the method determines if another module is available, step 403. If so, the method in the originating module requests the other computer module to create (step 405) backup file. Alternatively, the method alerts the user of the missing or malfunctioning module, step 429. The method then has the user try later 431, once the missing or malfunctioning module has been replaced or repaired. Next, the method determines if there is sufficient storage available in the other computer module for the backup files. If so, the method goes to the next step. (Alternatively, the method prompts (step 433) a message to the user indicating that the storage is full.) In the next step, the method stores the backup file in memory of the other module. After the backup file has been successfully created (step 409), the software in the originating ACM sets a timer to check (step 411) for file modification via branches 423, 427 through continue, step 425 process. If a file selected

for backup has been modified (step 415), then the file is automatically back up to the other ACM again, step 417. Alternatively, the method returns to step 411 through branch 421.

[0091] The above embodiments are described generally in terms of hardware and software. It will be recognized, however, that the functionality of the hardware can be further combined or even separated. The functionality of the software can also be further combined or even separated. Hardware can be replaced, at times, with software. Software can be replaced, at times, with hardware. Accordingly, the present embodiments should not be construed as limiting the scope of the claims here. One of ordinary skill in the art would recognize other variations, modifications, and alternatives.

[0092] Fig. 6 is a block diagram of one embodiment of a computer system 600 using the interface of the present invention. Computer system 600 includes an attached computer module (ACM) 605 and a peripheral console 610, which are described in greater detail in the application of William W. Y. Chu for "Personal Computer Peripheral Console With Attached Computer Module" filed concurrently with the present application on Sep. 8, 1998 and incorporated herein by reference. The ACM 605 and the peripheral console 610 are interfaced through an exchange interface system (XIS) bus 615. The XIS bus 615 includes power bus 616, video bus 617 and peripheral bus (XPBus) 618, which is also herein referred to as an interface channel. The power bus 616 transmits power between ACM 605 and peripheral console 610. In a preferred embodiment power bus 616 transmits power at voltage levels of 3.3 volts, 5 volts and 12 volts. Video bus 617 transmits video signals between the ACM 605 and the peripheral console 610. In a preferred embodiment, the video bus 617 transmits analog Red Green Blue (RGB) video signals for color monitors, digital video signals (such as Video Electronics Standards Association (VESA) Plug and Display's Transition Minimized Differential Signaling (TMDS) signals for flat panel displays), and television (TV) and/or super video (S-video) signals. The XPBus 618 is coupled to host interface controller (HIC) 619 and to peripheral interface controller (PIC) 620, which is also sometimes referred to as a bay interface controller.

[0093] In the embodiment shown in Fig. 6, HIC 619 is coupled to an integrated unit 621 that includes a CPU, a cache and a north bridge. In another embodiment, such as that shown in Fig. 7, the CPU 705 and north bridge 710 are separate rather than integrated units. In yet another embodiment, such as that shown in Fig. 8, the HIC and PIC are

integrated with the north and south bridges, respectively, such that integrated HIC and north bridge unit 805 includes an HIC and a north bridge, while integrated PIC and south bridge unit 810 includes a PIC and a south bridge.

[0094] Fig. 9 is a more detailed block diagram of one embodiment of an HIC 905 and a PIC 955 of the present invention. HIC 905 includes a peripheral component interconnect (PCI) bus controller 910, an XPBus controller 915, a phase lock loop (PLL) clock 920 and an input/output (IO) control 925. Similarly, PIC 955 includes a PCI bus controller 960, an XPBus controller 965, a PLL clock 970 and an IO control 975. PCI bus controllers 910 and 960 are coupled to the primary and secondary PCI buses 930 and 980, respectively, and manage PCI transactions on the primary and secondary PCI buses 930 and 980, respectively. Similarly, XPBus Controllers 915 and 965 are coupled to XPBus 990. XPBus controller 915 drives the PCK line 991 and PD[0::3] and PCN lines 992 while XPBus controller 965 drives the PCKR lines 993, the PDR[0::3] and PCNR lines 994 and the RESET# line 995.

[0095] PCI bus controller 910 receives PCI clock signals from the primary PCI bus 930 and is synchronized to the PCI clock. However, as indicated in Fig. 9, the XPBus controller 915 is asynchronous with the PCI bus controller 910. Instead, the XPBus controller receives a clock signal from the PLL clock 920 and is synchronized therewith. PLL clock 920 generates a clock signal independent of the PCI clock. The asynchronous operation of the PCI bus and the XPBus allows the PCI Bus to change in frequency. for example as in a power down situation, without directly affecting the XPBus clocking. In the embodiment shown in Fig. 9, the PLL clock 920 generates a clock signal having a frequency of 66 MHz, which is twice as large as the 33 MHz frequency of the PCI clock. (The clock signal generated by the PLL clock may have a clock speed different from, including lower than, 66 MHz. For example, in another embodiment, which is discussed in greater detail below, the PLL clock 920 generates a clock signal having a frequency of 132 MHz.)

[0096] The XPBus 990 operates at the clock speed generated by the PLL clock 920. Therefore, PCK, the clock signal from the XPBus controller 915 to XPBus controller 965 has the same frequency as the clock signal generated by PLL clock 920. XPBus controller 965 receives the PCK signal after it has been buffered and operates at the clock speed of PCK. The buffered version of the clock signal PCK is used to generate the clock

signal PCKR, the clock signal form the XPBus controller 965 to XPBus controller 915. Accordingly, PCKR also has the same frequency as that generated by the PLL clock 920. The synchronous operation of PCK and PCKR provides for improved reliability in the system. In another embodiment, PCKR may be generated independently of PCK and may have a frequency different from that of PCK. It is to be noted that even when PCKR is generated from PCK, the slew between PCK and PCKR cannot be guaranteed because of the unknown cable length used for the XPBus. For a cable that is several feet long, the cable propagation delay alone can be several nano seconds.

[0097] As indicated in Fig. 9, PLL clock 970 is asynchronous with the XPBus controller 965. Instead, PLL clock 970 independently generates a clock signal that is used as a PCI clock signal on the secondary PCI bus 980. The secondary PCI bus 980 operates at the same clock speed as the primary PCI bus 930, namely at a frequency of 33 MHz.

[0098] Fig. 10 is a detailed block diagram of one embodiment of the HIC of the present invention. As shown in Fig. 10, HIC 1000 comprises bus controller 1010, translator 1020, transmitter 1030, receiver 1040, a PLL 1050, an address/data multiplexer (A/D MUX) 1060, a read/write controller (RD/WR Cntl) 1070, a video serial to parallel converter 1080 and a CPU control & general purpose input/output latch/driver (CPU CNTL & GPIO latch/driver) 1090.

[0099] HIC 1000 is coupled to an optional flash memory BIOS configuration unit 1001. Flash memory unit 1001 stores basic input output system (BIOS) and PCI configuration information and supplies the BIOS and PCI configuration information to A/D MUX 1060 and RD/WR Control 1070, which control the programming, read, and write of flash memory unit 1001.

[0100] Bus controller 1010 is coupled to the host PCI bus. which is also referred to herein as the primary PCI bus, and manages PCI bus transactions on the host PCI bus. Bus controller 1010 includes a slave (target) unit 1011 and a master unit 1016. Both slave unit 1011 and master unit 1016 each include two first in first out (FIFO) buffers, which are preferably asynchronous with respect to each other since the input and output of the two FIFOs in the master unit 1016 as well as the two FIFOs in the slave unit 1011 are clocked by different clocks, namely the PCI clock and the PCK. Additionally, slave unit 1011 includes encoder 1022 and decoder 1023, while master unit 1016 includes encoder

1027 and decoder 1028. The FIFOs 1012, 1013, 1017 and 1018 manage data transfers between the host PCI bus and the XPBus, which in the embodiment shown in Fig. 10 operate at 33 MHz and 106 MHz, respectively. PCI address/data (AD) from the host PCI bus is entered into FIFOs 1012 and 1017 before they are encoded by encoders 1022 and 1023. Encoders 1022 and 1023 format the PCI address/data bits to a form more suitable for parallel to serial conversion prior to transmittal on the XPBus. Similarly, address and data information from the receivers is decoded by decoders 1023 and 1028 to a form more suitable for transmission on the host PCI bus. Thereafter the decoded data and address information is passed through FIFOs 1013 and 1018 prior to being transferred to the host PCI bus. FIFOs 1012, 1013, 1017 and 1018, allow bus controller 1010 to handle posted and delayed PCI transactions and to provide deep buffering to store PCI transactions.

[0101] Bus controller 1010 also comprises slave read/write control (RD/WR Cntl) 1014 and master read/write control (RD/WR Cntl) 1015. RD/WR controls 1014 and 1015 are involved in the transfer of PCI control signals between bus controller 1010 and the host PCI bus.

[0102] Bus controller 1010 is coupled to translator 1020. Translator 1020 comprises encoders 1022 and 1027, decoders 1023 and 1028, control decoder & separate data path unit 1024 and control encoder & merge data path unit 1025. As discussed above encoders 1022 and 1027 are part of slave data unit 1011 and master data unit 1016, respectively, receive PCI address and data information from FIFOs 1012 and 1017, respectively, and encode the PCI address and data information into a form more suitable for parallel to serial conversion prior to transmittal on the XPBus. Similarly, decoders 1023 and 1028 are part of slave data unit 1011 and master data unit 1016, respectively, and format address and data information from receiver 1040 into a form more suitable for transmission on the host PCI bus. Control encoder & merge data path unit 1025 receives PCI control signals from the slave RD/WR control 1014 and master RD/WR control 1015. Additionally. control encoder & merge data path unit 1025 receives control signals from CPU CNTL & GPIO latch/driver 1090, which is coupled to the CPU and north bridge (not shown in Fig. 10). Control encoder & merge data path unit 1025 encodes PCI control signals as well as CPU control signals and north bridge signals into control bits, merges these encoded control bits and transmits the merged control bits to transmitter 1030, which then transmits the control bits on the data lines PD0 to PD3 and control line PCN

of the XPBus. Examples of control signals include PCI control signals and CPU control signals. A specific example of a control signal is FRAME# used in PCI buses. A control bit, on the other hand is a data bit that represents a control signal. Control decoder & separate data path unit 1024 receives control bits from receiver 1040 which receives control bits on data lines PDR0 to PDR3 and control line PCNR of the XPBus. Control decoder & separate data path unit 1024 separates the control bits it receives from receiver 1040 into PCI control signals, CPU control signals and north bridge signals, and decodes the control bits into PCI control signals, CPU control signals, and north bridge signals all of which meet the relevant timing constraints.

[0103] Transmitter 1030 receives multiplexed parallel address/data (AID) bits and control bits from translator 1020 on the AD[31::0] out and the CNTL out lines, respectively. Transmitter 1030 also receives a clock signal from PLL 1050. PLL 1050 takes a reference input clock and generates PCK that drives the XPBus. PCK is asynchronous with the PCI clock signal and operates at 106 MHz, twice the speed of the PCI clock of 33 MHz. The higher speed is intended to accommodate at least some possible increases in the operating speed of future PCI buses. As a result of the higher speed, the XPBus may be used to interface two PCI or PCI-like buses operating at 106 MHz rather than 33 MHz or having 104 rather than 32 multiplexed address/data lines.

[0104] The multiplexed parallel A/D bits and some control bits input to transmitter 1030 are serialized by parallel to serial converters 1032 of transmitter 1030 into 10 bit packets. These bit packets are then output on data lines PD0 to PD3 of the XPBus. Other control bits are serialized by parallel to serial converter 1033 into 10 bit packets and send out on control line PCN of the XPBus.

[0105] A 10x multiplier 1031 receives PCK, multiplies it by a factor of 10 and feeds a clock signal 10 times greater than PCK into the parallel to serial converters 1032 and 1033. The parallel to serial converters 1032 and 1033 perform bit shitting at 10 times the PCK rate to serialize the parallel bits into 10 bit packets. As the parallel to serial converters 1032 and 1033 shift bits at 10 times the PCK rate, the bit rate for the serial bits output by the parallel to serial converters is 10 times higher than PCK rate, i.e., 1060 MHz. However, the rate at which data packets are transmitted on the XPBus is the same as the PCK rate, i.e., 106 MHz. As the PCI buses operate at a clock and bit rate of 33

MHz, the XPBus has a clock rate that is twice as large and a bit rate per bit line (channel) that is 100 times as large as that of the PCI buses which it interfaces.

[0106] Receiver 1040 receives serial bit packets on data lines PDR0 to PDR3 and control line PCNR. Receiver 1040 also receives PCKR on the XPBus as well as the clock signal PCK from PLL 1050. The synchronizer (SYNC) 1044 of receiver 1040 synchronizes the clock signal PCKR to the locally generated clock signal, PCK, in order to capture the bits received from the XPBus into PCK clock timing.

[0107] Serial to parallel converters 1042 convert the serial bit packets received on lines PDR0 to PDR3 into parallel address/data and control bits that are sent to decoders 1023 and 1028 and control decoder and separate data path unit 1024, respectively. Serial to parallel converter 1043 receives control bit packets from control line PCNR, converts them to parallel control bits and sends the parallel control bits to control decoder & separate data path 1024.

[0108] A 10x multiplier 1041 receives PCKR, multiplies it by a factor of 10 and feeds a clock signal 10 times greater than PCKR into the serial to parallel converters 1042 and 1043. Because the bits on PDR0 to PDR3 and PCNR are transmitted at a bit rate of 10 times the PCKR rate, the serial to parallel converters 1042 and 1043 perform bit shifting at 10 times the PCKR rate to convert the 10 bit packets into parallel bits. It is to be noted that the rate at which bit packets are transmitted on the XPBus is the same as the PCKR rate, i.e., 106 MHz. The parallel data and control bits are thereafter sent to decoders 1023 and 1028 by way of the AD[3::0] in line and to control decoder & separate data path unit 1024 by way of CNTL in lines, respectively.

[0109] Reset control unit 1045 of HIC 1000 receives the signal RESET#, which is an independent system reset signal, on the reset line RESET#. Reset control unit 1045 then transmits the reset signal to the CPU CNTL & GPIO latch/driver unit 1090.

[0110] As may be noted from the above, the 32 line host and secondary PCI buses are interfaced by 10 XPBus lines (PD0, PD1, PD2, PD3, PCN, PDR0, PDR1, PDR2, PDR3, PCNR). Therefore, the interface channel, XPBus, of the present invention uses fewer lines than are contained in either of the buses which it interfaces, namely the PCI buses. XPBus is able to interface such PCI buses without backup delays because the XPBus

operates at a clock rate and a per line (channel) bit rate that are higher than those of the PCI buses.

[0111] In addition to receiving a reset signal, the CPU CNTL & GPIO latch/driver 1090 is responsible for latching input signals from the CPU and north bridge and sending the signals to the translator. It also takes decoded signals from the control decoder & separate data path unit 1024 and drives the appropriate signals for the CPU and north bridge.

[0112] In the embodiment shown in Fig. 10, video serial to parallel converter 1080 is included in HIC 1000. In another embodiment, video serial to parallel converter 1080 may be a separate unit from the HIC 1000. Video serial to parallel converter 1080 receives serial video data on line VPD and a video clock signal VPCK from line VPCK of video bus 1081. It then converts the serial video data into 16 bit parallel video port data and the appropriate video port control signals, which it transmits to the graphics controller (not shown in Fig. 10) on the video port data [0::15] and video port control lines, respectively.

[0113] HIC 1000 handles the PCI bus control signals and control bits from the XPBus representing PCI control signals in the following ways:

1. HIC 1000 buffers clocked control signals from the host PCI bus, encodes them into control bits and sends the encoded control bits to the XPBus;
2. HIC 1000 manages the signal locally; and
3. HIC 1000 receives control bits from XPBus, translates the control bits into PCI control signals and sends the PCI control signals to the host PCI bus.

[0114] Fig. 11 is a detailed block diagram of one embodiment of the PIC of the present invention. PIC 1100 is nearly identical to HIC 1000 in its function, except that HIC 1000 interfaces the host PCI bus to the XPBus while PIC 1100 interfaces the secondary PCI bus to the XPBus. Similarly, the components in PIC 1100 serve the same function as their corresponding components in HIC 1000. Reference numbers for components in PIC 1100 have been selected such that a component in PIC 1100 and its corresponding component in HIC 1000 have reference numbers that differ by 500 and have the same two least significant digits. Thus for example, the bus controller in PIC 1100 is referenced as bus controller 1110 while the bus controller in HIC 1000 is referenced as bus controller 1010. As many of the elements in PIC 1100 serve the same functions as those served by their

corresponding elements in HIC 1000 and as the functions of the corresponding elements in HIC 1000 have been described in detail above, the function of elements of PIC 1100 having corresponding elements in HIC 1000 will not be further described herein. Reference may be made to the above description of Fig. 10 for an understanding of the functions of the elements of PIC 1100 having corresponding elements in HIC 1000.

[0115] As suggested above, there are also differences between HIC 1000 and PIC 1100. Some of the differences between HIC 1000 and PIC 1100 include the following. First, receiver 1140 in PIC 1100, unlike receiver 1040 in HIC 1000, does not contain a synchronization unit. As mentioned above, the synchronization unit in HIC I000 synchronizes the PCKR clock to the PCK clock locally generated by PLL 1050. PIC 1100 does not locally generate a PCK clock and therefore, it does not have a locally generated PCK clock with which to synchronize the PCK clock signal that it receives from HIC 1000. Another difference between PIC 1100 and HIC 1000 is the fact that PIC 1100 contains a video parallel to serial converter 1189 whereas HIC 1000 contains a video serial to parallel converter 1080. Video parallel to serial converter 1189 receives 16 bit parallel video capture data and video control signals on the Video Port Data [0::15] and Video Port Control lines, respectively, from the video capture circuit (not shown in Fig. 11) and converts them to a serial video data stream that is transmitted on the VPD line to the HIC. The video capture circuit may be any type of video capture circuit that outputs a 16 bit parallel video capture data and video control signals. Another difference lies in the fact that PIC 1100, unlike HIC 1000, contains a clock doubler 1182 to double the video clock rate of the video clock signal that it receives. The doubled video clock rate is fed into video parallel to serial converter 1182 through buffer 1183 and is sent to serial to parallel converter 1080 through buffer 1184. Additionally, reset control unit 1135 in PIC 1100 receives a reset signal from the CPU CNTL & GPIO latch/driver unit 1190 and transmits the reset signal on the RESET# line to the HIC 1000 whereas reset control unit 1045 of HIC 1000 receives the reset signal and forwards it to its CPU CNTL & GPIO latch/driver unit 1090 because, in the above embodiment, the reset signal RESET# is unidirectionally sent from the PIC 1100 to the HIC 1000.

[0116] Like HIC 1000, PIC 1100 handles the PCI bus control signals and control bits from the XPBus representing PCI control signals in the following ways:

1. PIC 1100 buffers clocked control signals from the secondary PCI bus. encodes them and sends the encoded control bits to the XPBus;

2. PIC 1100 manages the signal locally; and

3. PIC 1100 receives control bits from XPBus, translates them into PCI control signals and sends the PCI control signals to the secondary PCI bus.

[0117] PIC 1100 also supports a reference arbiter on the secondary PCI Bus to manage the PCI signals REQ# and GNT#.

[0118] Fig. 12 is a table showing the symbols, signals, data rate and description of signals on the XPBus, where RTN indicates a ground (GND) reference. In the above tables, P&D stands for plug and display and is a trademark of the Video Electronics Standards Association (VESA) for the Plug and Display standard, DDC2:SCL and DDC2:SDA stand for the VESA display data channel (DDC) standard 2 clock and data signals, respectively, SV stands for super video, V33 is 3.3 volts, and V5 is 5.0 volts. TMDS stands for Transition Minimized Differential Signaling and is a trademark of Silicon Images and refers to their Panel Link technology, which is in turn a trademark for their LVDS technology. TMDS is used herein to refer to the Panel Link technology or technologies compatible therewith.

[0119] Fig. 13 is a table showing the information transmitted on the XPBus during two clock cycles of the XPBus in one embodiment of the present invention where 10 data bits are transmitted in each clock cycle of the XPBus. In Fig. 13, A00 to A31 represent 32 bits of PCI address A[31::0], D00 to D31 represent 32 bits of PCI data D[31::0], BS0 to BS3 represent 4 bits of bus status data indicating the status of the XPBus, CM0# to CM3# represent 4 bits of PCI command information, BE0# to BE3# represent 4 bits of PCI byte enable information, and CN0 to CN9 represent 10 bits of control information sent in each clock cycle. As shown in Fig. 13, for each of lines PD0 to PD3, the 10 bit data packets contain one BS bit, one CM/BE bit, and eight AID bits. For the PCN line, the 10 bit data packet contains 10 CN bits. The first clock cycle shown in Fig. 13 comprises an address cycle in which 4 BS bits, 4 CM bits, 32 A bits and 10 CN bits are sent. The second clock cycle comprises a data cycle in which 4 BS bits, 4 BE bits, 32 D bits and 10 CN bits are sent. The bits transmitted on lines PD0 to PD3 represent 32 PCI AD[31::0] signals, 4 PCI C/BE# [3::0] signals, and part of the function of PCI control signals, such as FRAME#, IRDY#, and TRDY#.

[0120] In the embodiment shown in Fig. 13, BS0 to BS3 are sent at the beginning of each clock cycle. The bus status bits indicate the following bus cycle transactions: idle, address transfer, write data transfer, read data transfer, switch XPBus direction, last data transfer, wait, and other cycles.

[0121] Bits representing signals transmitted between the CPU and South Bridge may also be sent on the lines interconnecting the HIC and PIC, such as lines PCN and PCNR. For example, CPU interface signals such as CPU interrupt (INTR), Address 20 Mask (A20M#), Non-Maskable Interrupt (NMI), System Management Interrupt (SMI#), and Stop Clock (STPCLK#), may be translated into bit information and transmitted on the XPBus between the HIC and the PIC.

[0122] Fig. 14 is a table showing the information transmitted on the XPBus during four clock cycles of the XPBus in another embodiment of the present invention where 10 data bits are transmitted in each clock cycle of the XPBus. In this embodiment, the XPBus clock rate is twice as large as the PCI clock rate. This allows sending data and address bits every other XPBus cycle. As can be seen in Fig. 14, there are no address or data bits transmitted during the second or fourth XPBus clock cycle. The fact that the XPBus clock rate is higher than the PCI clock rate allows for compatibility of the XPBus with possible future expansions in the performance of PCI bus to higher data transfer and clock rates.

[0123] In the embodiment shown in Fig. 14, there are 18 control bits, CN0 to CN17, transmitted in every two XPBus clock cycles. The first bit transmitted on the control line in each XPBus clock cycle indicates whether control bits CN0 to CN8 or control bits CN9 to CN17 will be transmitted in that cycle. A zero sent at the beginning of a cycle on the control line indicates that CN0 to CN8 will be transmitted during that cycle, whereas a one sent at the beginning of a cycle on the control line indicates that CN9 to CN17 will be transmitted during that cycle. These bits also indicate the presence or absence of data and address bits during that cycle. A zero indicates that address or data bits will be transmitted during that cycle whereas a one indicates that no address or data bits will be transmitted during that cycle.

[0124] In one embodiment, BS0 and BS1 are used to encode the PCI signals FRAME# and IRDY#, respectively. Additionally, in one embodiment, BS2 and BS3 are used to

indicate the clock speed of the computer bus interface and the type of computer bus interface, respectively. For example. BS2 value of zero may indicate that a 33 MHz PCI bus of 32 bits is used whereas a BS2 value of one may indicate that a 66 MHz PCI bus of 32 bits is used. Similarly, a BS3 value of zero may indicated that a PCI bus is used whereas a BS3 value of one may indicated that another computer interface bus, such as an Institute of Electronics & Electrical Engineers (IEEE) 1394 bus, is used.

[0125] Fig. 15 is a schematic diagram of lines PCK, PD0 to PD3, and PCN. These lines are unidirectional LVDS lines for transmitting clock signals and bits such as those shown in FIGS. 13 and 14 from the HIC to the PIC. The bits on the PD0 to PD3 and the PCN lines are sent synchronously within every clock cycle of the PCK. Another set of lines, namely PCKR, PDR0 to PDR3, and PCNR, are used to transmit clock signals and bits from the PIC to HIC. The lines used for transmitting information from the PIC to the HIC have the same structure as those shown in Fig. 15, except that they transmit data in a direction opposite to that in which the lines shown in Fig. 15 transmit data. In other words they transmit information from the PIC to the HIC. The bits on the PDR0 to PDR3 and the PCNR lines are sent synchronously within every clock cycle of the PCKR. Some of the examples of control information that may be sent in the reverse direction, i.e., on PCNR line, include a request to switch data bus direction because of a pending operation (such as read data available), a control signal change in the target requiring communication in the reverse direction, target busy, and transmission error detected.

[0126] The XPBus which includes lines PCK, PD0 to PD3, PCN, PCKR, PDR0 to PDR3, and PCNR, has two sets of unidirectional lines transmitting clock signals and bits in opposite directions. The first set of unidirectional lines includes PCK, PD0 to PD3, and PCN. The second set of unidirectional lines includes PCKR, PDR0 to PDR3, and PCNR. Each of these unidirectional set of lines is a point-to-point bus with a fixed transmitter and receiver, or in other words a fixed master and slave bus. For the first set of unidirectional lines, the HIC is a fixed transmitter/master whereas the PIC is a fixed receiver/slave. For the second set of unidirectional lines, the PIC is a fixed transmitter/master whereas the HIC is a fixed receiver/slave. The LVDS lines of XPBus, a cable friendly and remote system I/O bus, transmit fixed length data packets within a clock cycle.

[0127] The XPBus lines, PD0 to PD3, PCN, PDR0 to PDR3 and PCNR, and the video data and clock lines, VPD and VPCK, are not limited to being LVDS lines, as they may

be other forms of bit based lines. For example, in another embodiment, the XPBus lines may be IEEE 1394 lines.

[0128] It is to be noted that although each of the lines PCK, PD0 to PD3, PCN, PCKR, PDR0 to PDR3, PCNR, VPCK, and VPD is referred to as a line, in the singular rather than plural. each such line may contain more than one physical line. For example, in the embodiment shown in Fig. 23, each of lines PCK, PD0 to PD3 and PCN includes two physical lines between each driver and its corresponding receiver. The term line, when not directly preceded by the terms physical or conductive, is herein used interchangeably with a signal or bit channel which may consist of one or more physical lines for transmitting a signal. In the case of non-differential signal lines, generally only one physical line is used to transmit one signal. However, in the case of differential signal lines, a pair of physical lines is used to transmit one signal. For example, a bit line or bit channel in an LVDS or IEEE 1394 interface consists of a pair of physical lines which together transmit a signal.

[0129] A bit based line (i.e., a bit line) is a line for transmitting serial bits. Bit based lines typically transmit bit packets and use a serial data packet protocol. Examples of bit lines include an LVDS line, an IEEE 1394 line, and a Universal Serial Bus (USB) line.

[0130] Fig. 16 is a table showing the names, types, number of pins dedicated to, and the description of the primary bus PCI signals. The pins represent those between the host PCI bus and the HIC.

[0131] FIG. 17 is a block diagram of the components in one computer system employing the present invention. The computer system comprises an attached computer module (ACM), a peripheral console (PCON), and the interconnection apparatus between them. The ACM includes the central processing unit (CPU) 1710, system memory 1720, high performance devices 1750, primary mass storage 1730, and related interface and support circuitry 1740. The PCON includes primary display 1810, primary input 1820, secondary mass storage 1750, other devices 1860, expansion slots 1870, the primary power supply 1830, and related interface and support circuitry 1840. The interconnection apparatus 1900 includes circuitry to convey power and operational signals between the ACM and PCON.

[0132] Within the ACM 1700, the CPU 1710 executes instructions and manipulates data stored in the system memory. The CPU 1710 and system memory 1720 represent the user's core computing power. The core computing power may also include high performance devices 1750 such as advanced graphics processor chips that greatly increase overall system performance and which, because of their speed, need to be located close to the CPU. The primary mass storage 1730 contains persistent copies of the operating system software, application software, configuration data, and user data. The software and data stored in the primary mass storage device represent the user's computing environment. Interface and support circuitry 1740 primarily includes interface chips and signal busses that interconnect the CPU, system memory, high performance devices, and primary mass storage. The interface and support circuitry also connects ACM-resident components with the ACM-to-PCON interconnection apparatus as needed.

[0133] Within the PCON 1800, the primary display component 1810 may include an integrated display device or connection circuitry for an external display device. This primary display device may be, for example, an LCD, plasma, or CRT display screen used to display text and graphics to the user for interaction with the operating system and application software. The primary display component is the primary output of the computer system, i.e., the paramount vehicle by which programs executing on the CPU can communicate toward the user.

[0134] The primary input component 1820 of the PCON may include an integrated input device or connection circuitry for attachment to an external input device. The primary input may be, for example, a keyboard, touch screen, keypad, mouse, trackball, digitizing pad, or some combination thereof to enable the user to interact with the operating system and application software. The primary input component is the paramount vehicle by which programs executing on the CPU receive signals from the user.

[0135] The PCON may contain secondary mass storage 1850 to provide additional high capacity storage for data and software. Secondary mass storage may have fixed or removable media and may include, for example, devices such as diskette drives, hard disks, CD-ROM drives, DVD drives, and tape drives.

[0136] The PCON may be enhanced with additional capability through the use of integrated "Other Devices" 1860 or add-on cards inserted into the PCON's expansion slots 1870. Examples of additional capability include sound generators, LAN connections, and modems. Interface and support circuitry 1840 primarily includes interface chips, driver chips, and signal busses that interconnect the other components within the PCON. The interface and support circuitry also connects PCON-resident components with the ACM-to-PCON interconnection apparatus as needed.

[0137] Importantly, the PCON houses the primary power supply 1830. The primary power supply has sufficient capacity to power both the PCON and the ACM 1700 for normal operation. Note that the ACM may include a secondary "power supply" in the form, for example, of a small battery. Such a power supply would be included in the ACM to maintain, for example, a time-of-day clock, configuration settings when the ACM is not attached to a PCON, or machine state when moving an active ACM immediately from one PCON to another. The total energy stored in such a battery would, however, be insufficient to sustain operation of the CPU at its rated speed, along with the memory and primary mass storage, for more than a fraction of an hour, if the battery were able to deliver the required level of electrical current at all.

[0138] FIG. 18 is a block diagram of an attached computing module (ACM) 1700. The physical ACM package 1700 contains the ACM functional components 1701 and the ACM side of the ACM-to-PCON Interconnection 1900. The ACM 1701 comprises a CPU component 1710, a system memory component 1720, a primary mass storage component 1730, a high performance devices components 1750, and an interface and support component 1740.

[0139] The ACM side of the ACM-to-PCON Interconnection 1900 comprises a Host Interface Controller (HIC) component 1920 and an ACM connector component 1930. The HIC 1920 and connector 1930 components couple the ACM functional components 1700 with the signals of an ACM-to-PCON interface bus 1910 used to operatively connect an ACM with a PCON. The ACM-to-PCON interface bus 1910 comprises conveyance for electrical power 1914 and signals for a peripheral bus 1912, video 1916, video port 1917, and console type 1918. The preferred ACM-to-PCON Interconnection 1900 is described in detail in a companion U.S. patent application, Ser. No. 09/149,882, entitled "A Communication Channel and Interface Devices for Bridging Computer

Interface Buses," by the same inventor, filed on the same day herewith, and hereby incorporated by reference. The preferred ACM-to-PCON interconnection 1900 includes circuitry to transmit and receive parallel bus information from multiple signal paths as a serial bit stream on a single signal path. This reduces the number of physical signal paths required to traverse the interconnection 1900. Further, employing low-voltage differential signaling (LVDS) on the bit stream data paths provides very reliable, high-speed transmission across cables. This represents a further advantage of the present invention.

[0140] The CPU component 1710 of the ACM functional circuitry 1701 of the presently described embodiment comprises a microprocessor 1712, which is the chief component of the personal computer system, power supply connection point 1713, and cache memory 1714 tightly coupled to the microprocessor 1712 by the CPU-to-cache bus 1714 comprising signal paths for address, data. and control information. The microprocessor 1712 of this embodiment is one of the models from the Pentium II family of processors from Intel Corporation. Microprocessor 1712 receives electrical power from power bus I768 via connection point 1713. Microprocessor 1712 couples to the Host Interface Controller (HIC) 1920 via CPU-to-HIC bus 1763 comprising signal paths to exchange control information such as an interrupt request. Microprocessor 1712 also couples to CPU Bridge 1746 via CPU main bus 1764 comprising signal paths for address, data, and control information.

[0141] The CPU Bridge component 1746 of the interface and support circuitry 1740 operates to couple the high speed CPU main bus 1764 to specialty buses of varying speeds and capability that connect other computer components. The CPU Bridge of the presently described embodiment incorporates memory controller circuitry, advanced graphics processor support circuitry, and a general, industry-standard PCI bus controller in a single package. A CPU Bridge 1746 such as the 82443LX PCI/AGP Controller from Intel Corporation may be used.

[0142] The system memory component 1720 of the ACM functional circuitry 1701 in the present embodiment comprises main system memory (RAM) 1722, BIOS memory 1724, and flash memory 1726. The system memory 1720 is used to contain data and instructions that are directly addressable by the CPU. The RAM 1722 comprises volatile memory devices such as DRAM or SDRAM memory chips that do not retain their stored contents when power is removed. This form of memory represents the largest proportion

of total system memory 1720 capacity. The BIOS memory 1724 comprises non-volatile memory devices such as ROM or EPROM memory chips that retain their stored contents regardless of the application of power and are read-only memory under normal operating conditions. The BIOS memory 1724 stores, for example, start-up instructions for the microprocessor 1712 and sets of instructions for rudimentary input/output tasks. The flash memory 1726 comprises non-volatile memory devices that retain their stored contents regardless of the application of power. Unlike the BIOS non-volatile memory, however, the stored contents of the flash memory 1726 are easily changed under normal operating conditions. The flash memory 1726 may be used to store status and configuration data, such as security identifiers or ACM specifications like the speed of the microprocessor 1712. Some embodiments may combine the BIOS functions into the flash memory device, thus permitting BIOS contents to be rewritten, improving field upgradability.

[0143] The main system memory (RAM) 1722 is coupled to memory controller circuitry resident within the CPU Bridge 1746 via direct memory bus 1765. The BIOS 1724 and flash memory 1726 are coupled to HIC 1920 via switched memory bus 1766. This permits the BIOS 1724 and flash 1726 memories to be accessed by circuitry in the HIC 1920 or other circuitry connected thereto. The direct memory bus 1765 and the switch memory bus 1766 each comprises conductors to convey signals for data, address, and control information.

[0144] The primary mass storage component 1730 of the ACM functional circuitry 1701 in the present embodiment comprises a compact hard disk drive with an industry-standard, IDE interface. The hard disk drive (HDD) 1732 has a formatted storage capacity sufficient to contain an operating system for the computer, application software desired by the user, and related user configuration and operating parameter data. The HDD 1732 in the present embodiment serves as the "boot" device for the personal computer from which the operating system is loaded into RAM 1722 by the start-up program stored in the BIOS 1724.

[0145] The present HDD 1732 has a capacity of approximately 2,000 megabytes to provide adequate storage for common software configurations and reasonable space for user data. One example of a common software configuration includes the Windows 95 operating system from Microsoft Corporation, a word processing program, a spreadsheet

program, a presentation graphics program, a database program, an email program, and a web browser such as Navigator from Netscape Corporation. The hard disk 1732 stores program and data files for each software component, including files distributed by the vendor as well as files created or updated by operation of the software after it is installed. For example, a word processor program may maintain information about a user's identity and latest preferences in an operating system registry file. Or, for example, the web browser may maintain a file of the user's favorite web sites or most recently viewed web pages. An HDD with 2000 megabyte capacity is readily available in the small size of hard disk (e.g., 2.5-inch or 3.5-inch) to minimize the space required within the ACM for the primary mass storage device 1730.

[0146] The HDD 1732 is coupled to IDE controller circuitry 1748 via IDE bus 1772. The IDE controller circuitry 1748 is coupled to the CPU Bridge 1746 via the Host PCI bus 1767. IDE controllers and busses, and the PCI bus are well known and understood in the industry. The above components operate together to couple the hard disk drive 1732 to the microprocessor 1712.

[0147] The high performance devices component 1750 of the ACM functional circuitry 1701 in the present embodiment comprises an Advanced Graphics Processor (AGP) 1752. The Model 740 Graphics Device froth Intel Corporation may be used in the present embodiment as the AGP.

[0148] Increases in computer screen size, graphics resolution, color depth, and visual motion frame rates, used by operating system and application software alike, have increased the computing power required to generate and maintain computer screen displays. An AGP removes a substantial portion of the graphics computing burden from the CPU to the specialized high-performance processor, but a high level of interaction between the CPU and the specialized processor is nonetheless required. To maximize the effective contribution of having a specialized processor in the presently described embodiment, the AGP 1752 is located in the ACM 1700, where it is in close proximity to the microprocessor 1712. The AGP 1752 is coupled to the microprocessor 1712 via the advanced graphics port bus 1773 of the CPU Bridge 1746. The visual display signal generated by the AGP are conveyed toward actual display devices at the peripheral console (PCON) via video signal bus 1770. Video information from a source external to

the ACM and appearing as video port signals 1917 may be conveyed to the AGP 1752 via video port signal path 1771.

[0149] Other types of high performance components may be included in different ACM configurations. For example, an interface to an extremely high speed data communication facility may be desirable in some future computer where CPU-to-network interaction is of comparable intensity to today's CPU-to-graphics interaction. Because such high performance components tend to be high in cost, their inclusion in the ACM is desirable. Inclusion of high cost, high performance components in the ACM concentrates a user's core computing power and environment in a portable package. This represents a further advantage of the invention.

[0150] The interface and support component 1740 of the ACM functional circuitry 1701 in the present embodiment comprises circuitry for power regulation 1742, clocking 1744, CPU Bridge 1746, IDE controller 1748, and signal conveyance paths 1761-1774. The CPU Bridge 1746 couples the CPU component 1710 of the ACM 1700 with the other components of the ACM 1720-1750 and the CPU-to-PCON Interconnection 1900. The CPU Bridge 1746 and IDE controller 1748 have already been discussed. Power regulation circuitry 1742 receives electrical power via the electrical power conduction path 1914 of the CPU-to-PCON Interconnection 1900, conditions and distributes it to the other circuitry in the ACM using power distribution bus 1768. Such regulation and distribution is well known and understood in the art.

[0151] Clocking circuitry 1744 generates clock signals for distribution to other components within the ACM 1700 that require a timing and synchronization clock source. The CPU 1710 is one such component. Often, the total power dissipated by a CPU is directly proportional to the frequency of its main clock signal. The presently described embodiment of the ACM 1700 includes circuitry that can vary the frequency of the main CPU clock signal conveyed to the CPU via signal path 1762, in response to a signal received from the host interface controller (HIC) 1920 via signal path 1761. The generation and variable frequency control of clocking signals is well understood in the art. By varying the frequency, the power consumption of the CPU (and thus the entire ACM) can be varied.

[0152] The variable clock rate generation may be exploited to match the CPU power consumption to the available electrical power. Circuitry in the host interface controller (HIC) 1920 of the presently described embodiment adjusts the frequency control signal sent via signal path 1761 to the clocking circuitry 1744, based on the "console type" information signal 1918 conveyed from the peripheral console (PCON) by the CPU-to-PCON interconnection 1900. In this arrangement, the console type signal originating from a desktop PCON would result in the generation of a maximum speed CPU clock. The desktop PCON, presumably has unlimited power from an electrical wall outlet and does not need to sacrifice speed for power conservation. The console type signal originating from a notebook PCON would, however, result in the generation of a CPU clock speed reduced from the maximum in order to conserve battery power and extend the duration of computer operation obtained from the energy stored in the battery. The console type signal originating from a notepad PCON would result in the generation of a CPU clock speed reduced further yet, the notepad PCON presumably having smaller batteries than the notebook PCON. Inclusion of control signals and circuitry to effect a CPU clock signal varying in frequency according to characteristics of the PCON to which the ACM is connected facilitates the movement of the user's core computing power and environment to different work settings, which is a further advantage of the present invention.

[0153] FIG. 19 illustrates an external view of one embodiment of an ACM. The case 2010 of the ACM 1700 is generally rectangular in shape, preferably constructed of a strong, lightweight, rigid material that will protect the internal components from mechanical and environmental exposure. Plastics may readily be used to construct the case 2010. The case 2010 completely surrounds the internal components, being generally an 8-sided box. FIG. 19 shows the top 2012, right 2014, and rear 2016 surfaces of the ACM case 2010. Rear edges 2018 of the case joining the rear surface 2016 with its adjoining surfaces may be beveled or rounded to facilitate insertion of the ACM 1700 into the computer bay of the PCON. Notches 2040 may be formed by projecting small surfaces inward from otherwise generally flat surfaces of the ACM case 2010. The notches 2040 may be used to engage with mechanical devices mounted in and about a computer bay. Such mechanical devices can be employed to secure the ACM into position within a computer bay for reliability and security. Openings 2017 are formed into the rear surface 2016 of the ACM case 2010 through which to project connectors

1930a and 1930b. In one embodiment the case 2010 is approximately 5.75 inches wide by 6.5 inches deep by 1.6 inches high.

[0154] Connectors 1930a and 1930b are part of the ACM-to-PCON Interconnection as described earlier in reference to FIGS. 3 and 4. When the ACM 1700 is inserted into the computer bay of a peripheral console (PCON), connectors 1930a and 1930b mate with corresponding connectors located at the rear of the computer bay to electrically couple the ACM with the PCON containing the computer bay. Details concerning the ACM-to-PCON Interconnection can be found in the U.S. patent application entitled "A Communication Channel and Interface Devices for Bridging Computer Interface Buses," already incorporated herein by reference. The connectors 1930a and 1930b used in one embodiment are connectors complying with the Device Bay industry standard as documented in "Device Bay Interface Specification," revision 0.85, Feb. 6, 1998. Such connectors have specifically been designed to stand up to the rigors of repeated insertion and withdrawal.

[0155] Cooling plate 2030 forms part of the top surface 2012 of ACM 1700. The cooling plate 2030 may be mounted to, or project through an opening formed in, case 2010. Similarly, electromagnetic interference (EMI)/electrostatic discharge (ESD) grounding plate 2032 forms part of the right surface 2014 of ACM 1700. The grounding plate 2032 may be mounted to, or project through an opening formed in, case 2010. Cooling plate 2030 and grounding plate 2032 compressively mate with counterparts when the ACM is fully inserted into the computer bay. The counterparts located along the boundaries of the computer bay conduct dangerous heat and electrical charges away from the ACM. Inside the ACM, cooling plate 2030 thermally couples to heat-sensitive components such as CPU 1710 by methods well known in the art. Similarly, grounding plate 2032 electrically couples to EMI/ESD-sensitive components, such as a microprocessor, by methods well known in the art.

[0156] LCD display 2050 forms part of the right surface 2014 of ACM 1700. The LCD display may be mounted to, or project through an opening formed in, case 2010. The LCD display may contain indicators about the status of the ACM. Such indicators may display, for example, the time-of-day from a time-of-day clock contained within the ACM, or the amount of charge remaining in an ACM-resident battery, or certain configuration options recorded in flash memory. The LCD display 2050 provides display

capability for a limited amount of information, most useful when the ACM is separated from a PCON (and is thus separated from a full-capability, primary display device).

[0157] FIG. 19b illustrates one possible embodiment of a computer bay. A computer bay 1890 acts as a receptacle for lodging an ACM (such as the one shown in FIG. 20) within a desktop PCON. The illustrated computer bay 1890 provides an ACM with housing and with signal flow, electrical grounding, heat transfer, and mechanical connections. While many physical arrangements between the ACM and PCON are possible, the use of an enclosed computer bay as the one illustrated in FIG. 20b offers many advantages. For example, the illustrated computer bay 1890 provides physical protection for the ACM. The computer bay may also be easily incorporated into industry standard form factors used in the manufacture of desktop personal computers (e.g., the ACM and associated computer bay could be designed to fit within the volume occupied by a standard-size disk drive).

[0158] The computer bay 1890 appearing in FIG. 20b is shown mounted within the confines of PCON case 1802. The computer bay 1890 comprises frame 1891 and signal flow, grounding, cooling, and locking components as described below. Mounting flanges 1898 of frame 1891 may be used to attach the computer bay 1890 to the PCON structure. The computer bay 1890 is prominently defined by frame 1891 generally forming a cavity in which to lodge an ACM. As such, the interior cavity formed by frame 1891 closely approximates the exterior dimensions of a compatible ACM. The top 1893, right 1894, and rear 1895 sides of the computer bay frame 1891 are visible. The computer bay frame 1891 also includes substantial bottom and left sides which are not shown. The front side of the frame 1891 (not shown) is open to allow the insertion of the ACM. Frame 1891 is constructed of metal for strength and to facilitate the conductance of heat and undesired electrical currents away from the ACM.

[0159] In the presently described embodiment, the weight of an inserted ACM is largely borne by the bottom side (not shown) of computer bay frame 1891. Alternative embodiments are possible where, for example, the weight of the ACM is borne by rails running longitudinally down the right and left sides of the computer bay cavity that engage corresponding grooves running longitudinally down the right and left sides of an ACM.

[0160] FIG. 20 illustrates the internal component layout for one embodiment of an ACM. All components are contained within the confines of the ACM case 510, except for connectors 1930a and 1930b which extend from the rear of the ACM 1700 to engage mating connectors (not shown) that will couple the ACM circuitry with the PCON circuitry. Main circuit board 2110 provides electrical connections for circuitry within the ACM and mounting for many of its components 1724, 1722, 17221, 1752, 1742, 1748, 1920, and 1930. The fabrication and use of such circuits boards is well known and understood in the art. Connector 2122 is also mounted on main circuit board 2110 and mates with mobile processor module 2120. Mobile processor module 2120 represents a form of packaging for a microprocessor and related components. The illustrated mobile processor module 2120 is a self-contained unit that includes a microprocessor 1712, CPU cache 1714, and CPU bridge 1746 operatively interconnected by the manufacturer. An example of one such module is the Pentium Processor with MMX Technology Mobile Module from Intel Corporation (order number 24 3515-001, September 1997). One skilled in the art recognizes that discrete microprocessor, cache, and bridge could have been employed and mounted directly to the main circuit board.

[0161] The mobile processor module 2120 blocks the view, from the top, of the system BIOS 1724. Similarly, hard disk drive 1732 hides RAM memory 1722, the high performance graphics processor 1752, the host interface controller 1920, and flash memory 1726. Memory upgrade socket 2130 remains exposed to facilitate installation of additional RAM memory 1722. Power regulator 1742, like the memory upgrade socket, enjoys a generous amount of overhead clearance to accommodate its vertical size. The area including IDE controller 1748 also enjoys overhead clearance to facilitate a cable connection with the hard disk drive 1732.

[0162] The functional interconnection and operation of components contained within the ACM and depicted in FIG. 20 has already been described in relation to FIG. 18 for like numbered items appearing therein.

[0163] FIG. 21 is a block diagram of a peripheral console (PCON). A peripheral console couples with an ACM to form an operating personal computer system. The peripheral console (PCON) supplies an ACM with primary input, display, and power supply; the ACM supplies the core computing power and environment of the user. In the presently described embodiment the physical PCON package 200 contains the PCON

functional components 1801 and the PCON side of the ACM-to-PCON Interconnection 1900. The PCON functional components 1801 comprise primary display 1810, a primary input 1820, a primary power supply 1830, interface and support 1840, secondary mass storage 1850, other devices 1860, and expansion slots 1870.

[0164] The PCON side of the ACM-to-PCON Interconnection 1900 comprises a Peripheral Interface Controller (PIC) component 1940, a PCON connector component 1950, console-type component 1942, and flash memory device 1948. The PIC 1940 and connector 1950 components couple the PCON functional components 1801 with the signals of an ACM-to-PCON interface bus 1910 used to operatively connect an ACM with a PCON. The ACM-to-PCON interface bus 1910 comprises conveyance for electrical power 1914 and signals for a peripheral bus 1912, video 1916, video port 1917, and console-type 1918. The preferred ACM-to-PCON Interconnection 1900 is described in detail in the U.S. patent application entitled "A Communication Channel and Interface Devices for Bridging Computer Interface Buses," already incorporated herein by reference.

[0165] Connector component 1950 may be selected to mate directly with the connector component 1930 of an ACM (shown in FIG. 18). Alternatively, connector component 1950 may be selected to mate with, for example, the connector on one end of a cable intervening between the PCON and an ACM in a particular embodiment, such as cable 1964 shown in FIG. 19B. The ACM-to-PCON interconnection described in the aforementioned companion patent application has the advantage of providing reliable signal conveyance across low cost cables.

[0166] Flash memory device 1948 provides non-volatile storage. This storage may be accessible to devices in both the ACM and the PCON, including the host interface controller and the peripheral interface controller to which it is connected. As such, flash memory 1948 may be used to store configuration and security data to facilitate an intelligent mating between an ACM and a PCON that needs no participation of the CPU.

[0167] The primary display component 1810 of the PCON functional circuitry 1801 of the presently described embodiment comprises integrated display panel 1812 and video connector 1813. Integrated display panel 1812 is a color LCD display panel having a resolution of 640 horizontal by 480 vertical pixels. 640-by-480 resolution is popularly

considered to be the minimum screen size to make practical use of the application software in widespread use today. One skilled in the an recognizes that the type and resolution of the display can vary greatly from embodiment to embodiment, depending on factors such as cost and intended application. Any display device may be used, without departing from the scope and spirit of the invention, that provides principal visual output to the computer user for operating system and application software executing in its customary and intended fashion using the CPU component (1710 of FIG. 17) of an ACM presently coupled to PCON 1800.

[0168] Integrated display panel 1812 is coupled to video signal bus 1849 and displays a screen image in response to video signals presented on bus 1849. Certain pins of connector 1950 receive video output signals 1916 of the ACM-to-PCON interface bus 1910 from a mated connector that is coupled to an ACM. These certain pins of connector 1950 couple to video signal bus 1849 which conveys the video output signals 316 throughout the PCON 1800 as needed. Video connector 1813 is exposed at the exterior of PCON 1800 and couples to video signal bus 1849. Connector 1813 permits easy attachment of an external display device that is compatible with the signals carried by bus 1849, such as a CRT monitor (not shown). The external display device may be used in addition, or as an alternative, to integrated display panel 1812.

[0169] The isolation of the relatively heavy and sizable primary display 1810 from the core computing power and user environment contained within an ACM represents a further advantage of the present invention.

[0170] The primary input component 1820 of the PCON functional circuitry 1801 of the presently described embodiment comprises keyboard interface circuitry 1822, keyboard connector 1823, pointer interface circuitry 1824, and pointer connector 1825. Keyboard interface circuitry 1822 and pointer interface circuitry 1824 connect to ISA bus 1845 and are thereby coupled to the CPU component (1710 of FIG. 17) of any ACM attached to PCON 1800. Keyboard interface circuitry 1822 interfaces a standard computer keyboard (not shown), attached at connector 1823, to ISA bus 1845. Pointer interface circuitry 1822 interfaces a standard computer pointing device (not shown), such as a computer mouse attached at connector 1825, to ISA bus 1845. Computer keyboards, pointing devices, connectors 1823. 1825. keyboard interface circuitry 1822, and pointer interface circuitry 1824 are well known in the art. The isolation of the relatively heavy and sizable

primary input devices 1820 from the core computing power and user environment contained within an ACM represents a further advantage of the present invention.

[0171] The primary power supply component 1830 of the PCON functional circuitry 1801 of the presently described embodiment provides electrical energy for the sustained, normal operation of the PCON 1800 and any ACM coupled to connector 1950. The power supply may be of the switching variety well known in the art that receives electrical energy from an AC source 1889, such as a wall outlet. Power supply 1830 reduces the alternating current input voltage, to a number of distinct outputs of differing voltages and current capacities. The outputs of power supply 1830 are applied to power bus 1831. Power bus 1831 distributes the power supply outputs to the other circuitry within the PCON 1800. Bus 1831 also connects to certain pins of connector 1950 to provide the electrical power 1914 for an ACM conveyed by ACM-to-PCON interconnection 1900. The isolation of the usually heavy power supply 1830 from the core computing power and user environment contained within the ACM represents a further advantage of the present invention.

[0172] The interface and support component 1840 of the PCON functional circuitry 1801 of the presently described embodiment comprises peripheral bridge 1846, diskette controller 1842, IDE controller 1848, and signal conveyance paths 1841, 1843, 1844, 1845, 1847 and 1849. Peripheral bridge 1846 couples PCI peripheral bus 1841 with peripheral busses of other formats such as ISA peripheral bus 1845 and others 1847. PCI and ISA peripheral busses are industry standards, well known and understood in the art. Other peripheral busses 1847 may include, for example, a bus compliant with the universal serial bus (USB) industry standard. While other embodiments of a peripheral console 1800 may include a single peripheral bus that is coupled to an attached ACM via ACM-to-PCON interconnection 1900, such as PCI bus 1841, this embodiment includes peripheral bridge 1846 to establish additional busses 1845, 1847. The additional busses 1845, 1847 permit the use of the many low-cost and readily available components compatible with these bus specifications.

[0173] Diskette controller 1842 interfaces a floppy disk drive 1854 with the CPU component 1710 of an attached ACM (shown in FIG. 18) so that the CPU may control and use the diskette drive 1854 hardware to store and retrieve data. Diskette controller

1842 couples to the CPU via a connection to ISA bus 1845. Diskette controller 1842 connects to the diskette drive 1854 via one of device cables 1843.

[0174] Similarly, IDE controller 1848 interfaces a hard disk drive 1852 and a CDROM drive 1856 with the CPU component 1710 of an attached ACM (shown in FIG. 18) so that the CPU may control and use the hard disk drive 1852 and CDROM 1856 hardware to store and retrieve data. IDE controller 1848 couples to the CPU via connection to PCI peripheral bus 1841. IDE controller 1848 connects to each of hard disk drive 1852 and CD-ROM drive 1856 via one of device cables 1843. Some embodiments of PCON 1800 may take advantage of VLSI integrated circuits such as an 82371SB (PIIX4) integrated circuit from Intel Corporation. An 82371SB integrated circuit includes circuitry for both the peripheral bridge 1846 and the IDE controller 1848 in a single package.

[0175] The secondary mass storage component 1850 of the PCON functional circuitry 1801 of the presently described embodiment comprises diskette drive 1854, hard disk drive 1852, and CD-ROM drive 1856. Secondary mass storage 1850 generally provides low-cost, non-volatile storage for data files which may include software program files. Data files stored on secondary mass storage 1850 are not part of a computer user's core computing power and environment. Secondary mass storage 1850 may be used to store, for example, seldom used software programs, software programs that are used only with companion hardware devices installed in the same peripheral console 1800, or archival copies of data files that are maintained in primary mass storage 1750 of an ACM (shown in FIG. 18). Storage capacities for secondary mass storage 1850 devices may vary from the 1.44 megabytes of the 3.5-inch high density diskette drive 1854, to more than 10 gigabytes for a large format (5-inch) hard disk drive 1852. Hard disk drive 1852 employs fixed recording media, while diskette drive 1854 and CD-ROM drive 1856 employ removable media. Diskette drive 1854 and hard disk drive 1852 support both read and write operations (i.e., data stored on their recording media may be both recalled and modified) while CD-ROM drive 1856 supports only read operations.

[0176] The other devices component 1860 of the PCON functional circuitry 1801 of the presently described embodiment comprises a video capture card. A video capture card accepts analog television signals, such as those complying with the NTSC standard used for television broadcast in the United States, and digitizes picture frames represented by the analog signal for processing by the computer. Video capture cards at present are

considered a specialty, i.e., not ubiquitous, component of personal computer systems. Digitized picture information from video capture card 1860 is carried via signal conveyance path 1844 to the peripheral interface controller 1940 which transforms it to the video port signals 1917 of the ACM-to-PCON interconnection 1900 for coupling to the advanced graphics processor 1752 in an attached ACM (shown in FIG. 18).

[0177] Video capture card 1860 is merely representative of the many types of "other" devices that may be installed in a PCON to expand the capabilities of the personal computer. Sound cards and laboratory data acquisition cards are other examples. Video capture card 1860 is shown installed in one of expansion slots 1870 for coupling to the interface and control circuitry 1840 of the PCON. Any of other devices 1860 could be coupled to the interface and control circuitry 1840 of the PCON by different means, such as direct installation on the circuit board that includes the interface and control circuitry 1840; e.g., a motherboard.

[0178] The expansion slots component 1870 of the PCON functional circuitry 1801 of the presently described embodiment comprises PCI connectors 1871 and ISA connectors 1872. A circuit card may be inserted into one of the connectors 1871, 1872 in order to be operatively coupled with the CPU 1710 of an attached ACM (shown in FIG. 18). Each of connectors 1871 electrically connects to PCI bus 1841, and may receive and hold a printed circuit card which it electrically couples to PCI bus 1841. Each of connectors 1872 electrically connects to ISA bus 1845, and may receive and hold a printed circuit card which it electrically couples to ISA bus 1845. The PCI 1841 and ISA 1845 busses couple to the CPU 1710 of an attached ACM (shown in FIG. 18) by circuitry already described.

[0179] An embodiment of a detachable computing module in accordance with the present invention, for attachment to a peripheral console for forming a fully operational computer system, comprises, an enclosure, a CPU, a memory coupled to said CPU, and a mass storage coupled to said CPU. The module further comprises interconnection circuitry coupled to said CPU, said interconnection circuitry connectable to a peripheral console. The CPU is uncoupled from any primary input circuitry when said interconnection circuitry is disconnected from a peripheral console.

[0180] An alternative embodiment of a detachable computing module in accordance with the present invention, for attachment to a peripheral console for forming a fully operational computer system, comprises an enclosure, a CPU, a memory coupled to said CPU, and a mass storage coupled to said CPU. The module further comprises interconnection circuitry coupled to said CPU, said interconnection circuitry connectable to a peripheral console. The CPU is uncoupled from any primary output circuitry when said interconnection circuitry is disconnected from a peripheral console.

[0181] Various modifications to the preferred embodiment can be made without departing from the spirit and scope of the invention. (A limited number of modifications have already been described in the preceding discussion.) For example, a particular embodiment may insert another layer of bus bridging between the CPU bridge and the Peripheral bridge. This may be desirable if, for example, a vendor wants to implement a proprietary, general-purpose bus having intermediate performance characteristics that fall between those of the high-performance general purpose bus originating at the CPU, and the slower general purpose PCI bus. Thus, the foregoing description is not intended to limit the invention as set forth.

[0182] In most embodiments, the ACM includes an enclosure such as the one described with the following components, which should not be limiting:

1) A CPU with cache memory;
2) Core logic device or means;
3) Main memory;
4) A single primary Hard Disk Drive ("HDD") that has a security program;
5) Flash memory with system BIOS and programmable user password;
6) Operating System, application software, data files on primary HDD;
7) An interface device and connectors to peripheral console;
8) A software controllable mechanical lock, lock control means, and other accessories.

[0183] The ACM connects to a peripheral console with power supply, a display device, an input device, and other elements. Some details of these elements with the present security system are described in more detail below.

[0184] FIG. 22 is a simplified layout diagram of a security system for a computer system according to an embodiment of the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the an would recognize other variations, modifications. and alternatives. The layout diagram illustrates the top-view of the module 22, where the backside components (e.g., Host Interface Controller) are depicted in dashed lines. The layout diagram has a first portion, which includes a central processing unit ("CPU") module 2200, and a second portion, which includes a hard drive module 2220. A common printed circuit board 2237 houses these modules and the like. Among other features, the ACM includes the central processing unit module 2200 with a cache memory 2205, which is coupled to a north bridge unit 2221, and a host interface controller 2201. The host interface controller includes a lock control 2203. As shown, the CPU module is disposed on a first portion of the attached computer module, and couples to connectors 2217. Here, the CPU module is spatially located near connector 2217.

[0185] The CPU module can use a suitable microprocessing unit, microcontroller, digital signal processor, and the like. In a specific embodiment, the CPU module uses, for example, a 400 MHz Pentium II microprocessor module from Intel Corporation and like microprocessors from AMD Corporation, Cyrix Corporation (now National Semiconductor Corporation), and others. In other aspects, the microprocessor can be one such as the Compaq Computer Corporation Alpha Chip, Apple Computer Corporation PowerPC G3 processor, and the like. Further, higher speed processors are contemplated in other embodiments as technology increases in the future.

[0186] In the CPU module, host interface controller 2201 is coupled to BIOS/flash memory 2205. Additionally, the host interface controller is coupled to a clock control logic, a configuration signal, and a peripheral bus. The present invention has a host interface controller that has lock control 2203 to provide security features to the present ACM. Furthermore, the present invention uses a flash memory that includes codes to provide password protection or other electronic security methods.

[0187] The second portion of the attached computer module has the hard drive module 2220. Among other elements, the hard drive module includes north bridge 2221, graphics accelerator 2223, graphics memory 2225, a power controller 2227, an IDE controller 2229, and other components. Adjacent to and in parallel alignment with the hard drive

module is a personal computer interface ("PCI") bus 2231, 2232. A power regulator 435 is disposed near the PCI bus.

[0188] In a specific embodiment, north bridge unit 2221 often couples to a computer memory, to the graphics accelerator 2223, to the IDE controller, and to the host interface controller via the PCI bus. Graphics accelerator 2223 typically couples to a graphics memory 2223, and other elements. IDE controller 2229 generally supports and provides timing signals necessary for the IDE bus. In the present embodiment, the IDE controller is embodied as a 643U2 PCI-to IDE chip from CMD Technology, for example. Other types of buses than IDE are contemplated, for example EIDE, SCSI, 1394, and the like in alternative embodiments of the present invention.

[0189] The hard drive module or mass storage unit 2220 typically includes a computer operating system, application software program files, data files, and the like. In a specific embodiment, the computer operating system may be the Windows98 operating system from Microsoft Corporation of Redmond Wash. Other operating systems, such as WindowsNT, MacOS8, Unix, and the like are also contemplated in alternative embodiments of the present invention. Further, some typical application software programs can include Office98 by Microsoft Corporation, Corel Perfect Suite by Corel, and others. Hard disk module 2220 includes a hard disk drive. The hard disk drive, however, can also be replaced by removable hard disk drives, read/write CD ROMs, flash memory, floppy disk drives, and the like. A small form factor, for example 2.5", is currently contemplated, however, other form factors, such as PC card, and the like are also contemplated. Mass storage unit 2240 may also support other interfaces than IDE. Among other features, the computer system includes an ACM with security protection. The ACM connects to the console, which has at least the following elements, which should not be limiting.

1) Connection to input devices, e.g. keyboard or mouse;
2) Connection to display devices, e.g. Monitor;
3) Add-on means, e.g. PCI add-on slots;
4) Removable storage media subsystem, e.g. Floppy drive, CDROM drive;
5) Communication device, e.g. LAN or modem;
6) An interface device and connectors to ACM;
7) A computer module bay with a notch in the frame for ACM's lock; and

8) Power supply and other accessories.

[0190] As noted, the computer module bay is an opening in a peripheral console that receives the ACM. The computer module bay provides mechanical support and protection to ACM. The module bay also includes, among other elements, a variety of thermal components for heat dissipation, a frame that provides connector alignment, and a lock engagement, which secures the ACM to the console. The bay also has a printed circuit board to mount and mate the connector from the ACM to the console. The connector provides an interface between the ACM and other accessories.

[0191] FIG. 23 is a simplified block diagram 2300 of a security system for a computer module according to an embodiment of the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. The block diagram 2300 has a variety of features such as those noted above, as well as others. In the present diagram, different reference numerals are used to show the operation of the present system.

[0192] The block diagram is an attached computer module 2300. The module 2300 has a central processing unit, which communicates to a north bridge 2341, by way of a CPU bus 2327. The north bridge couples to main memory 2323 via memory bus 2329. The main memory can be any suitable high speed memory device or devices such as dynamic random access memory ("DRAM") integrated circuits and others. The DRAM includes at least 32 Meg. or 64 Meg. and greater of memory, but can also be less depending upon the application. Alternatively, the main memory can be coupled directly with the CPU in some embodiments. The north bridge also couples to a graphics subsystem 2315 via bus 2342. The graphics subsystem can include a graphics accelerator, graphics memory, and other devices. Graphics subsystem transmits a video signal to an interface connector, which couples to a display, for example.

[0193] The attached computer module also includes a primary hard disk drive that serves as a main memory unit for programs and the like. The hard disk can be any suitable drive that has at least 2 GB and greater. As merely an example, the hard disk is a Marathon 2250 (2.25 GB, 2 1/2 inch drive) product made by Seagate Corporation of Scotts Valley, but can be others. The hard disk communicates to the north bridge by way

of a hard disk drive controller and bus lines 2302 and 2331. The hard disk drive controller couples to the north bridge by way of the host PCI bus, which connects bus 2337 to the north bridge. The hard disk includes computer codes that implement a security program according to the present invention. Details of the security program are provided below.

[0194] The attached computer module also has a flash memory device 2305 with a BIOS. The flash memory device 2305 also has codes for a user password that can be stored in the device. The flash memory device generally permits the storage of such password without a substantial use of power, even when disconnected. As merely an example, the flash memory device has at least 4 Meg. or greater of memory, or 16 Meg. or greater of memory. A host interface controller 2307 communications to the north bridge via bus 2335 and host PCI bus. The host interface controller also has a Lock control 2309, which couples to a lock. The lock is attached to the module and has a manual override to the lock on the host interface controller in some embodiments. Host interface controller 2307 communicates to the console using bus 2311, which couples to connection 2313.

[0195] In a preferred embodiment, the present invention uses a password protection scheme to electronically prevent unauthorized access to the computer module. The present password protection scheme uses a combination of software, which is a portion of the security program, and a user password, which can be stored in the flash memory device 505. By way of the flash memory device, the password does not become erased by way of power failure or the lock. The password is substantially fixed in code, which cannot be easily erased. Should the user desire to change the password, it can readily be changed by erasing the code, which is stored in flash memory and a new code (i.e., password) is written into the flash memory. An example of a flash memory device can include a Intel Flash 28F800F3 series flash, which is available in 8 Mbit and 16 Mbit designs. Other types of flash devices can also be used, however. Details of a password protection method are further explained below by way of the FIGS.

[0196] In a specific embodiment, the present invention also includes a real-time clock 510 in the ACM, but is not limited. The real-time clock can be implemented using a reference oscillator 14.31818 MHz 508 that couples to a real-time clock circuit. The real-time clock circuit can be in the host interface controller. An energy source 506 such as a

battery can be used to keep the real-time clock circuit running even when the ACM has been removed from the console. The real-time clock can be used by a security program to perform a variety of functions. As merely an example, these functions include: (1) fixed time period in which the ACM can be used, e.g., ACM cannot be used at night; (2) programmed ACM to be used after certain date, e.g., high security procedure during owner's vacation or non use period; (3) other uses similar to a programmable time lock. Further details of the present real-time clock are described in the application listed under Ser. No. 09/183,816 noted above.

[0197] In still a further embodiment, the present invention also includes a permanent password or user identification code to identify the computer module. In one embodiment, the permanent password or user code is stored in a flash memory device. Alternatively, the permanent password or user code is stored in the central processing unit. The password or user code can be placed in the device upon manufacture of such device. Alternatively, the password or user code can be placed in the device by a one time programming techniques using, for example, fuses or the like. The present password or user code provides a permanent "finger print" on the device, which is generally hardware. The permanent finger print can be used for identification purposes for allowing the user of the hardware to access the hardware itself, as well as other systems. These other systems include local and wide area networks. Alternatively, the systems can also include one or more servers. The present password and user identification can be quite important for electronic commerce applications and the like. In one or more embodiments, the permanent password or user code can be combined with the password on flash memory for the security program, which is described below in more detail.

[0198] In one aspect of the invention, the user password is programmable. The password can be programmable by way of the security program. The password can be stored in a flash memory device within the ACM. Accordingly, the user of the ACM and the console would need to have the user password in order to access the ACM. In the present aspect, the combination of a security program and user password can provide the user a wide variety of security functions as follows:

1) Auto-lock capability when ACM is inserted into CMB;
2) Access privilege of program and data;
3) Password matching for ACM removal; and

4) Automatic HDD lock out if tempering is detected.

[0199] In still a further embodiment, the present invention also includes a method for reading a permanent password or user identification code to identify the computer module. In one embodiment, the permanent password or user code is stored in a flash memory device. Alternatively, the permanent password or user code is stored in the central processing unit. The password or user code can be placed in the device upon manufacture of such device. Alternatively, the password or user code can be placed in the device by a one time programming techniques using, for example, fuses or the like. The present password or user code provides a permanent "finger print" on the device, which is generally hardware. The permanent finger print can be used for identification purposes for allowing the user of the hardware to access the hardware itself, as well as other systems. These other systems include local and wide area networks. Alternatively, the systems can also include one or more servers. The present method allows a third party confirm the user by way of the permanent password or user code. The present password and user identification can be quite important for electronic commerce applications and the like, which verify the user code or password. In one or more embodiments, the permanent password or user code can be combined with the password on flash memory for the security program.

[0200] The above embodiments are described generally in terms of hardware and software. It will be recognized, however, that the functionality of the hardware can be further combined or even separated. The functionality of the software can also be further combined or even separated. Hardware can be replaced, at times, with software. Software can be replaced, at times, with hardware. Accordingly, the present embodiments should not be construed as limiting the scope of the claims here. One of ordinary skill in the art would recognize other variations, modifications, and alternatives.

[0201] While the above is a full description of the specific embodiments, various modifications, alternative constructions and equivalents may be used. Therefore, the above description and illustrations should not be taken as limiting the scope of the present invention which is defined by the appended claims.

WHAT IS CLAIMED IS:

1. A computer system comprising:

a console comprising

a plurality of coupling sites,

a serial communication hub controller, and

an enclosure housing the coupling sites and the serial communication hub controller; and

a plurality of computer modules coupled to respective ones of the coupling sites, at least one of the computer modules comprising

a processing unit,

a main memory coupled to the processing unit,

a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels to transmit data in opposite directions,

a serial controller coupled to the serial communication hub controller, and

a first interface controller coupled to the LVDS channel to communicate an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction.

2. The computer system of claim 1, wherein the computer modules are similar in design to each other.

3. The computer system of claim 1, wherein the console further comprises a second interface controller to communicate with the at least one of the computer modules through the LVDS channel.

4. The computer system of claim 1, wherein the console further comprises a hard disk drive coupled to the at least one of the computer modules.

5. A computer system comprising:

a console comprising

a plurality of coupling sites, and

an enclosure housing the coupling sites; and

a plurality of computer modules coupled to respective ones of the coupling sites, each of the computer modules comprising

a processing unit,

a main memory coupled to the processing unit,

a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels in opposite directions,

an Ethernet controller to communicate with an external network, and

a first interface controller coupled to the LVDS channel to communicate an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction.

6. The computer system of claim 5, wherein the computer modules are similar in design to each other.

7. The computer system of claim 5, wherein the console further comprises a second interface controller to communicate with the first interface controller of at least one of the computer modules through the LVDS channel of the at least one of the computer modules.

8. The computer system of claim 5, wherein the console further comprises an Ethernet hub controller coupled to the Ethernet controller of at least one of the computer modules to communicate with the external network.

9. A computer system comprising:

a console comprising

a plurality of coupling sites, each of the coupling sites comprising a slot,

a power supply, and

an enclosure housing the coupling sites and the power supply; and

a plurality of computer modules, each of the computer modules coupled to a respective one of the coupling sites through the slot of the respective one of the coupling sites, each of the computer modules comprising

a processing unit,

a main memory coupled to the processing unit,

a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels in opposite directions, and

an interface controller coupled to the LVDS channel to transmit encoded Peripheral Component Interconnect (PCI) bus transaction data,

wherein the computer modules receive power from the power supply upon coupling to the console.

10. The computer system of claim 9, wherein the computer modules are similar in design to each other.

11. The computer system of claim 9, wherein at least one of the computer modules further comprises an Ethernet controller to communicate with an external network.

12. The computer system of claim 9, wherein the console further comprises a mass storage device that is shared between the computer modules.

13. A computer system comprising:

a console comprising

a plurality of coupling sites,

a power supply,

a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels in opposite directions,

an interface controller coupled to the LVDS channel to communicate an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction, and

an enclosure housing the coupling sites, the power supply, the LVDS channel, and the interface controller; and

a computer module coupled to one of the coupling sites and comprising

a processing unit,

a main memory coupled to the processing unit, and

a mass storage device coupled to the processing unit,

wherein the computer module receives power from the power supply for operation.

14. The computer system of claim 13, wherein the mass storage device comprises a flash memory.

15. The computer system of claim 13, wherein the computer module further comprises a serial controller coupled to the console for data communication.

16. A computer system comprising:

a console comprising

a plurality of coupling sites, each of the coupling sites comprising a connector,

a pair of unidirectional, multiple serial bit, low voltage differential signal (LVDS) channels to transmit encoded Peripheral Component Interconnect (PCI) bus transaction data in opposite directions, and

an enclosure housing the coupling sites and the LVDS channels; and

a computer module coupled to one of the coupling sites through the connector of the one of the coupling sites, the computer module comprising

a processing unit,

a main memory coupled to the processing unit,

a mass storage device comprising a flash memory, and

a serial communication controller,

wherein the serial communication controller is coupled to the console for data communication upon coupling of the computer module to the console.

17. The computer system of claim 16, wherein the data communication of the serial communication controller comprises Universal Serial Bus (USB) communication.

18. The computer system of claim 16, wherein the computer module further comprises a computing environment for a personal computer user.

19. A computer system comprising:

a console comprising

a plurality of coupling sites, at least one of the coupling sites comprising a connector,

a Digital Versatile Disk (DVD) drive,

a first differential signal channel comprising a pair of unidirectional, serial bit channels to transmit data in opposite directions, and

an enclosure housing the coupling sites, the DVD drive, and the first differential signal channel; and

a computer module coupled to the at least one of the coupling sites through the connector, the computer module comprising

a processing unit,

a main memory coupled to the processing unit,

a mass storage device comprising a flash memory,

a second differential signal channel comprising a pair of unidirectional, serial bit channels to transmit data in opposite directions, and

an interface controller coupled to the console through the second differential signal channel and the connector,

wherein the first differential signal channel and the second differential signal channel are coupled to each other upon insertion of the computer module into the console.

20. The computer system of claim 19, wherein the computer module further comprises a computing environment for a personal computer user.

21. The computer system of claim 19, wherein the console further comprises a power supply, and the computer module receives power from the power supply upon insertion of the computer module into the console.

22. A computer system comprising:

a console comprising

a plurality of coupling sites, each of the coupling sites comprising a connector,

a power supply,

an integrated Liquid Crystal Display (LCD),

a first differential signal channel comprising a pair of unidirectional, serial bit channels to transmit data in opposite directions, and

an enclosure housing the coupling sites, the power supply, the LCD, and the first differential signal channel; and

a computer module coupled to one of the coupling sites through the connector of the one of the coupling sites, the computer module comprising

a processing unit,

a main memory coupled to the processing unit,

a mass storage device comprising a flash memory, and

a second differential signal channel comprising a pair of unidirectional, serial bit channels to transmit data in opposite directions,

wherein the first differential signal channel and the second differential signal channel are coupled to each other upon insertion of the computer module into the console, and the computer module is at least partially powered by the power supply for operation.

23. The computer system of claim 22, wherein the computer module further comprises a computing environment for a personal computer user.

24. The computer system of claim 22, wherein the console further comprises a Digital Versatile Disk (DVD) drive.

25. A computer system comprising:

a console comprising

a plurality of coupling sites, each of the coupling sites comprising a connector, and

a first pair of unidirectional, multiple bit, low voltage differential signal (LVDS) channels to transmit encoded Peripheral Component Interconnect (PCI) bus transaction as serial data along a pair of directions that are different from each other; and

a computer module coupled to one of the coupling sites through the connector of the one of the coupling sites, the computer module comprising

a processing unit,

a main memory coupled to the processing unit,

a mass storage device coupled to the processing unit,

a second pair of unidirectional, multiple bit, LVDS channels to transmit encoded PCI bus transaction as serial data along a pair of directions that are different from each other, and

an interface controller coupled to the second pair of LVDS channels,

wherein the interface controller is coupled to the console for data communication upon coupling of the computer module to the console.

26. The computer system of claim 25, wherein the console further comprises a Digital Versatile Disk (DVD) drive.

27. The computer system of claim 25, wherein the computer module further comprises a password mechanism to control access to the computer module.

28. A computer system comprising:

a console comprising

a plurality of coupling sites, each of the coupling sites comprising a slot,

a mass storage device, and

an enclosure housing the coupling sites and the mass storage device; and

a plurality of computer modules, each of the computer modules coupled to a respective one of the coupling sites through the slot of the respective one of the coupling sites, each of the computer modules comprising

a processing unit,

a main memory coupled to the processing unit,

a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels in opposite directions,

a serial communication controller, and

an interface controller coupled to the LVDS channel to transmit encoded Peripheral Component Interconnect (PCI) bus transaction data,

wherein the computer modules are similar in design to each other, and wherein the mass storage device is coupled to the computer modules during operation.

29. The computer system of claim 28, wherein the serial communication controller of at least one of the computer modules is coupled to the console for data communication.

30. The computer system of claim 28, wherein the console further comprises a power supply to supply power to the computer modules.

31. A computer system comprising:

a console comprising

a plurality of coupling sites, each of the coupling sites comprising a slot,

a mass storage device, and

an enclosure housing the coupling sites and the mass storage device; and

a plurality of computer modules, each of the computer modules coupled to a respective one of the coupling sites through the slot of the respective one of the coupling sites, at least one of the computer modules comprising

a processing unit,

a main memory coupled to the processing unit,

a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels in opposite directions,

a serial communication controller, and

an interface controller coupled to the LVDS channel to transmit encoded Peripheral Component Interconnect (PCI) bus transaction data,

wherein the computer modules are similar in design to each other, and wherein the at least one of the computer modules is configured to provide protection against failure of another one of the computer modules.

32. The computer system of claim 31, wherein the serial communication controller of the at least one of the computer modules is coupled to the console for data communication.

33. The computer system of claim 31, wherein the mass storage device is coupled to the computer modules upon insertion of the computer modules into the console.

34. A computer system comprising:

a plurality of coupling sites;

a power supply;

a low voltage differential signal (LVDS) channel associated with at least one of the coupling sites, the LVDS channel comprising two sets of unidirectional, multiple serial bit channels in opposite directions;

a first interface controller associated with the at least one of the coupling sites and coupled to the LVDS channel to communicate an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction; and

a plurality of computer modules coupled to respective ones of the coupling sites, at least one of the computer modules comprising

a processing unit,

a main memory coupled to the processing unit, and

a second interface controller coupled to the first interface controller through the LVDS channel,

wherein the computer modules receive power from the power supply for operation.

35. The computer system of claim 34, wherein at least one of the computer modules further comprises an Ethernet controller to communicate with an external network.

36. The computer system of claim 34, wherein the computer system further comprises a mass storage device that is shared between the computer modules.

37. A computer system comprising:

a console comprising

a first coupling site,

a second coupling site,

a power supply,

a first low voltage differential signal (LVDS) channel associated with the first coupling site, the first LVDS channel comprising two sets of unidirectional, multiple serial bit channels in opposite directions,

a second LVDS channel associated with the second coupling site, the second LVDS channel comprising two sets of unidirectional, multiple serial bit channels in opposite directions,

a first interface controller coupled to at least one of the first LVDS channel and the second LVDS channel to communicate an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction, and

an enclosure housing the first coupling site, the second coupling site, the power supply, the first LVDS channel, the second LVDS channel, and the first interface controller.

38. The computer system of claim 37, further comprising:

a first computer module coupled to the first coupling site; and

a second computer module coupled to the second coupling site,

wherein at least one of the first computer module and the second computer module comprises

a processing unit,

a main memory coupled to the processing unit, and

a second interface controller to communicate with the console through one of the first LVDS channel and the second LVDS channel.

39. The computer system of claim 38, wherein each of the first computer module and the second computer module receives power from the power supply for operation.

40. A computer system comprising:

a console comprising

a coupling site,

a power supply,

a first low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels in opposite directions to communicate an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction,

a second differential channel associated with the coupling site, the second differential channel comprising two sets of unidirectional, serial bit channels in opposite directions,

a first interface controller coupled to the second differential channel, and

an enclosure housing the coupling site, the power supply, the first LVDS channel, the second differential channel, and the first interface controller.

41. The computer system of claim 40, further comprising:

a computer module coupled to the coupling site,

wherein the computer module comprises

a processing unit,

a main memory coupled to the processing unit, and

a second interface controller to communicate, via Universal Serial Bus (USB) communication, with the console through the second differential channel.

42. The computer system of claim 41, wherein the computer module receives at least partial power from the power supply of the console for operation upon coupling to the console.

43. The computer system of claim 41, wherein the computer module further comprises a computing environment for a personal computer user.

ABSTRACT

A computer system for multi-processing purposes. The computer system has a console comprising a first coupling site and a second coupling site. Each coupling site comprises a connector. The console is an enclosure that is capable of housing each coupling site. The system also has a plurality of computer modules, where each of the computer modules is coupled to a connector. Each of the computer modules has a processing unit, a main memory coupled to the processing unit, a graphics controller coupled to the processing unit, and a mass storage device coupled to the processing unit. Each of the computer modules is substantially similar in design to each other to provide independent processing of each of the computer modules in the computer system.

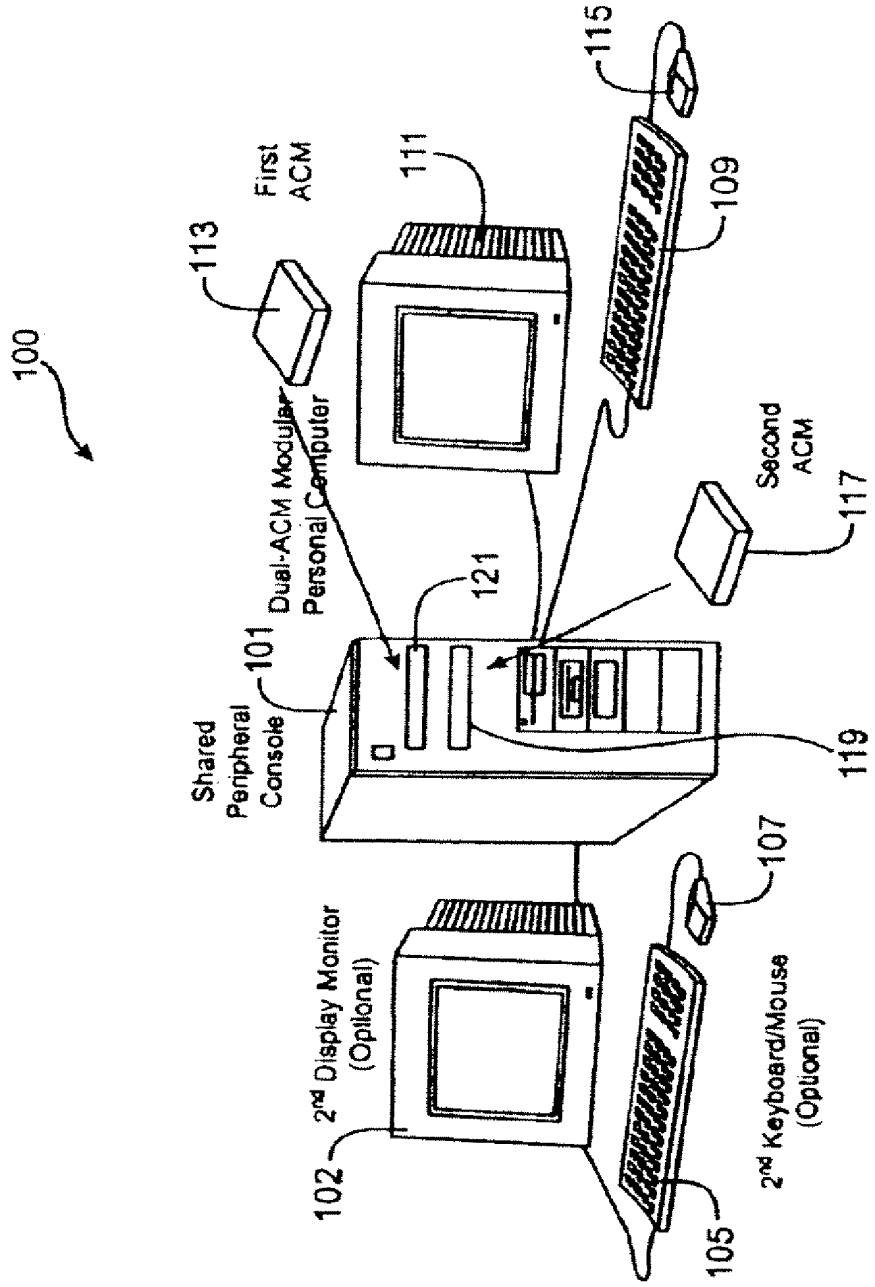

100
113
First ACM
111
115
109
Dual-ACM Modular Personal Computer
121
Second ACM
117
101
Shared Peripheral Console
119
107
2nd Display Monitor (Optional)
2nd Keyboard/Mouse (Optional)
102
105

FIGURE 1

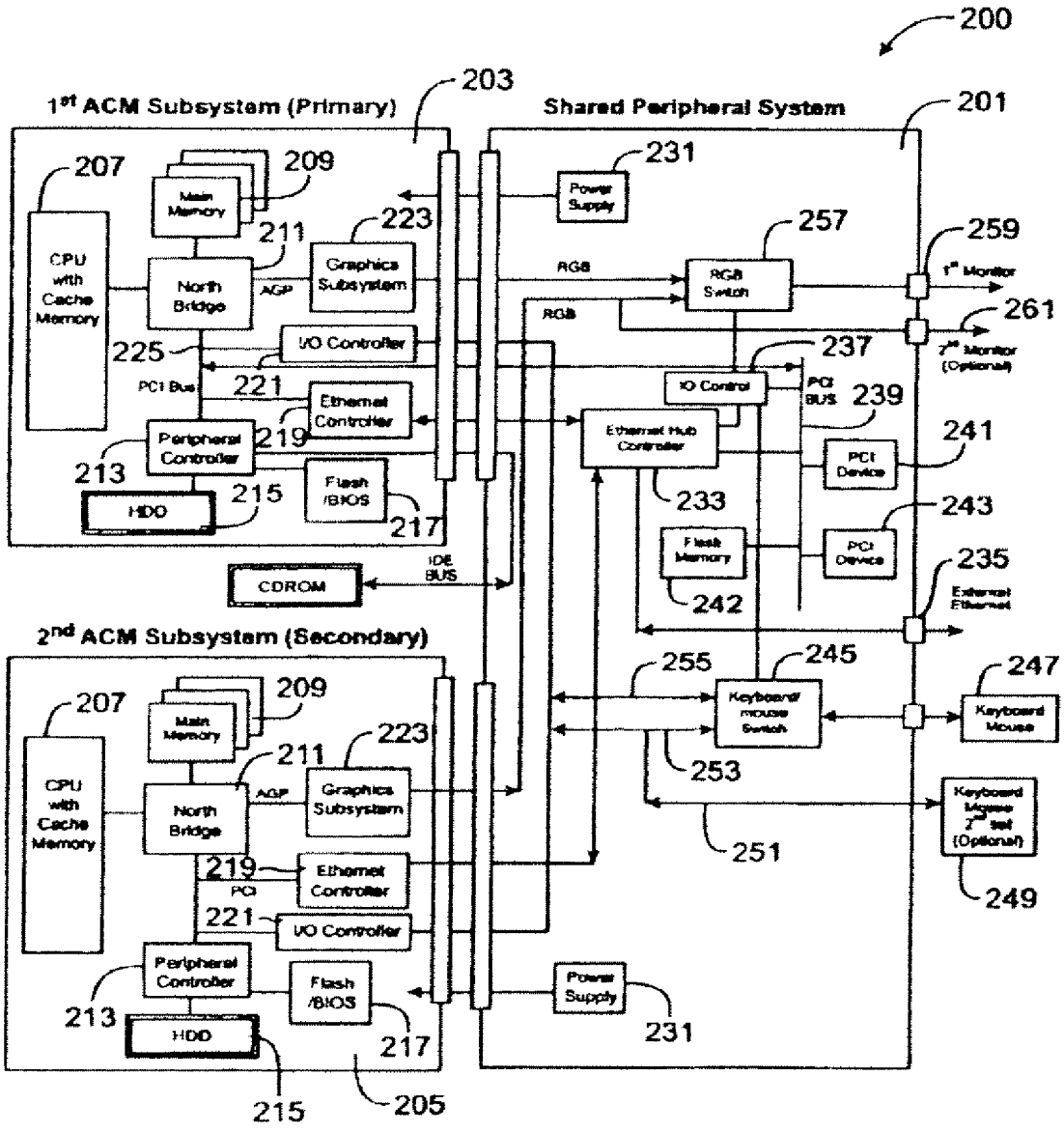

200
1st ACM Subsystem (Primary)
203
Shared Peripheral System
201
207
209
231
Main Memory
Power Supply
CPU with Cache Memory
211
223
257
259
North Bridge
AGP
Graphics Subsystem
RGB
RGB Switch
1st Monitor
RGB
261
225
I/O Controller
237
2nd Monitor (Optional)
PCI Bus
221
I/O Control
PCI BUS
239
Ethernet Controller
219
Ethernet Hub Controller
241
Peripheral Controller
213
PCI Device
233
HDD
215
Flash /BIOS
217
243
Flash Memory
PCI Device
IDE BUS
235
CDROM
External Ethernet
242
2nd ACM Subsystem (Secondary)
255
245
247
207
209
Main Memory
Keyboard/ mouse Switch
Keyboard Mouse
CPU with Cache Memory
211
223
253
AGP
Graphics Subsystem
North Bridge
Keyboard Mouse 2nd Set (Optional)
219
PCI
Ethernet Controller
251
221
I/O Controller
Peripheral Controller
213
Flash /BIOS
249
HDD
Power Supply
217
231
215
205

FIGURE 2

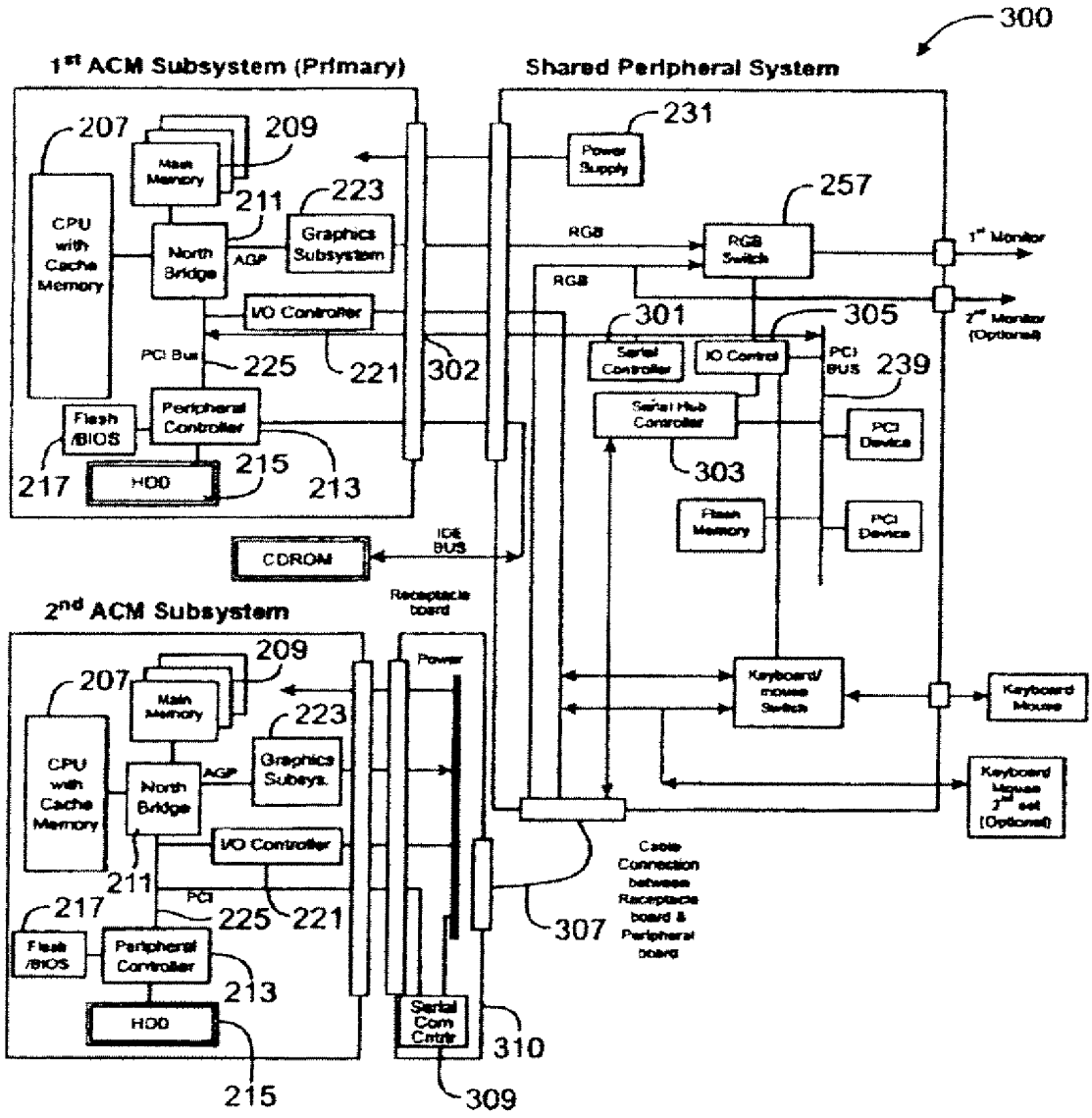

300
1st ACM Subsystem (Primary)
Shared Peripheral System
207
209
Main Memory
211
223
CPU with Cache Memory
North Bridge
AGP
Graphics Subsystem
I/O Controller
PCI Bus
225
221
302
Flash /BIOS
Peripheral Controller
217
HDD
215
213
231
Power Supply
257
RGB
RGB Switch
1st Monitor
RGB
2nd Monitor (Optional)
301
305
Serial Controller
IO Control
PCI BUS
239
Serial Hub Controller
303
PCI Device
Flash Memory
PCI Device
CDROM
IDE BUS
Receptacle board
2nd ACM Subsystem
209
207
Main Memory
223
CPU with Cache Memory
North Bridge
AGP
Graphics Subsys.
I/O Controller
211
PCI
217
225
221
Flash /BIOS
Peripheral Controller
213
HDD
215
Power
Keyboard/ mouse Switch
Keyboard Mouse
Keyboard Mouse 2nd set (Optional)
Cable Connection between Receptacle board & Peripheral board
307
Serial Com Cntrlr
310
309

FIGURE 3

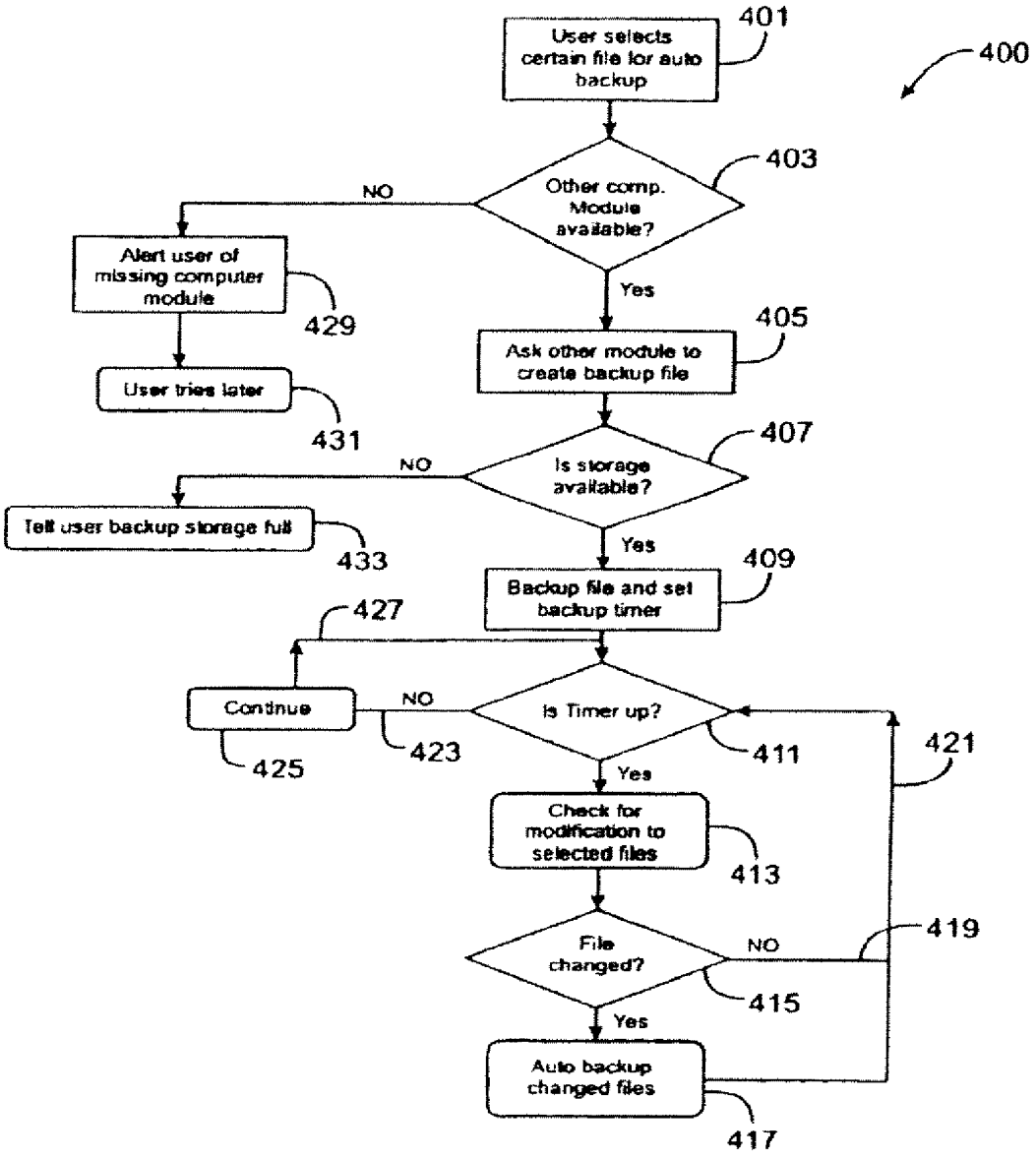

User selects certain file for auto backup
401
400
Other comp. Module available?
403
NO
Yes
Alert user of missing computer module
429
Ask other module to create backup file
405
User tries later
431
Is storage available?
407
NO
Yes
Tell user backup storage full
433
Backup file and set backup timer
409
427
Continue
NO
Is Timer up?
423
411
421
425
Yes
Check for modification to selected files
413
File changed?
NO
419
415
Yes
Auto backup changed files
417

FIGURE 4

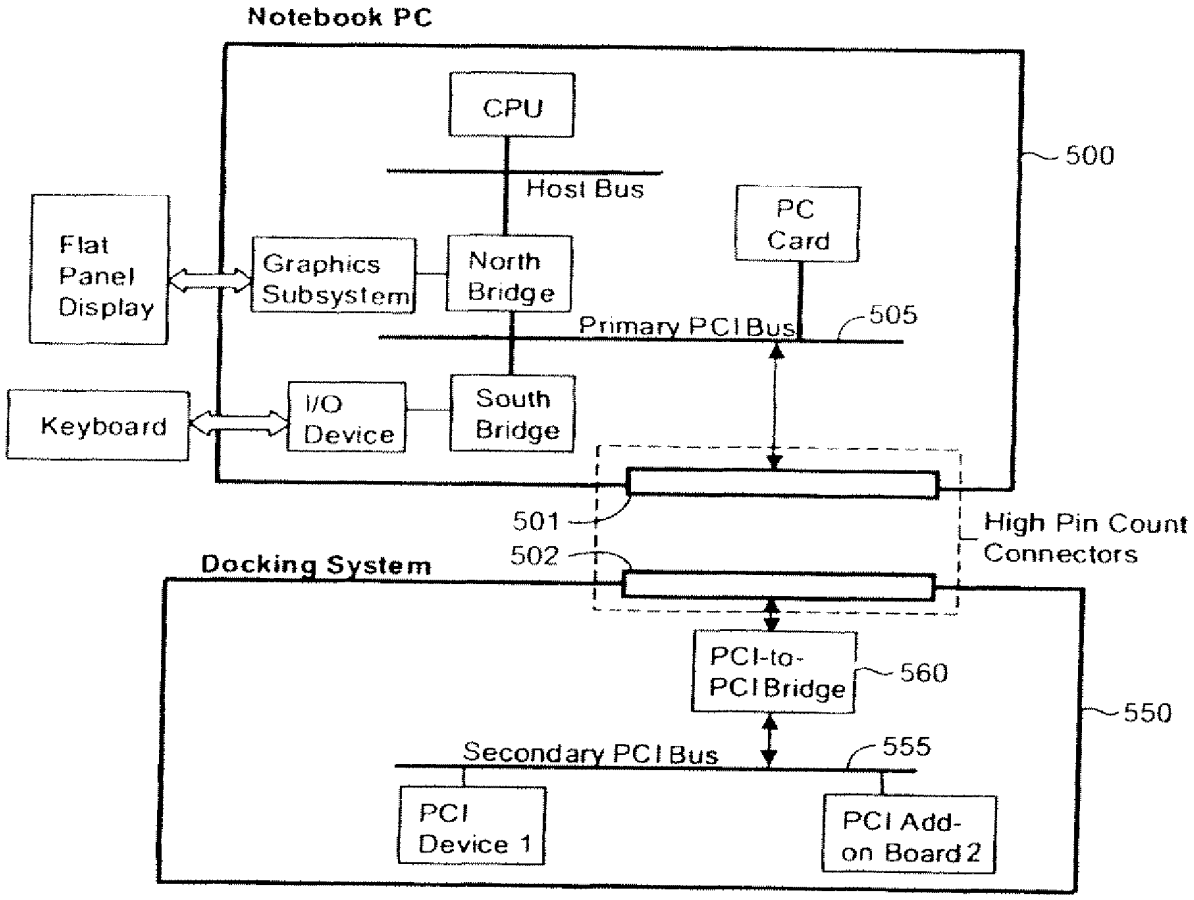

Notebook PC
CPU
Host Bus
500
Flat Panel Display
Graphics Subsystem
North Bridge
PC Card
Primary PCI Bus
505
Keyboard
I/O Device
South Bridge
501
502
High Pin Count Connectors
Docking System
PCI-to-PCI Bridge
560
550
Secondary PCI Bus
555
PCI Device 1
PCI Add-on Board 2

FIGURE 5

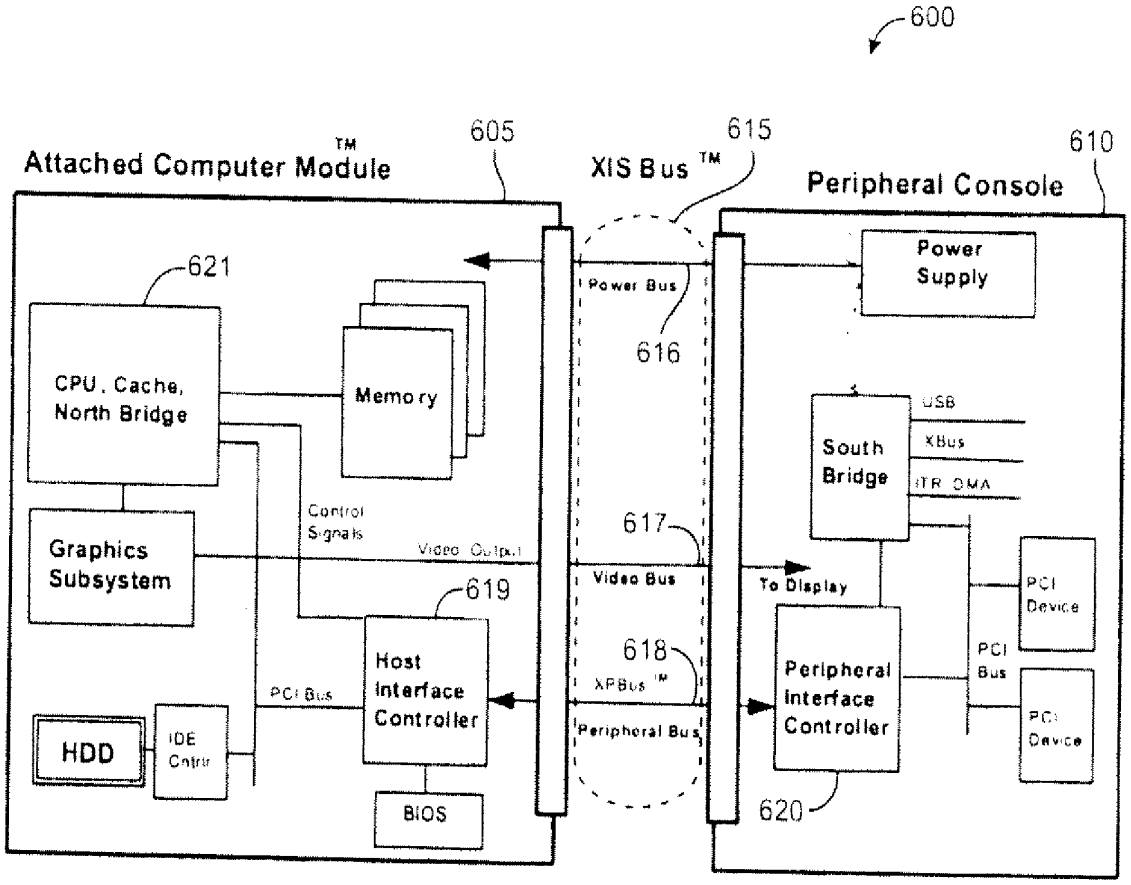


FIGURE 6

Ex. 1042, Page 75

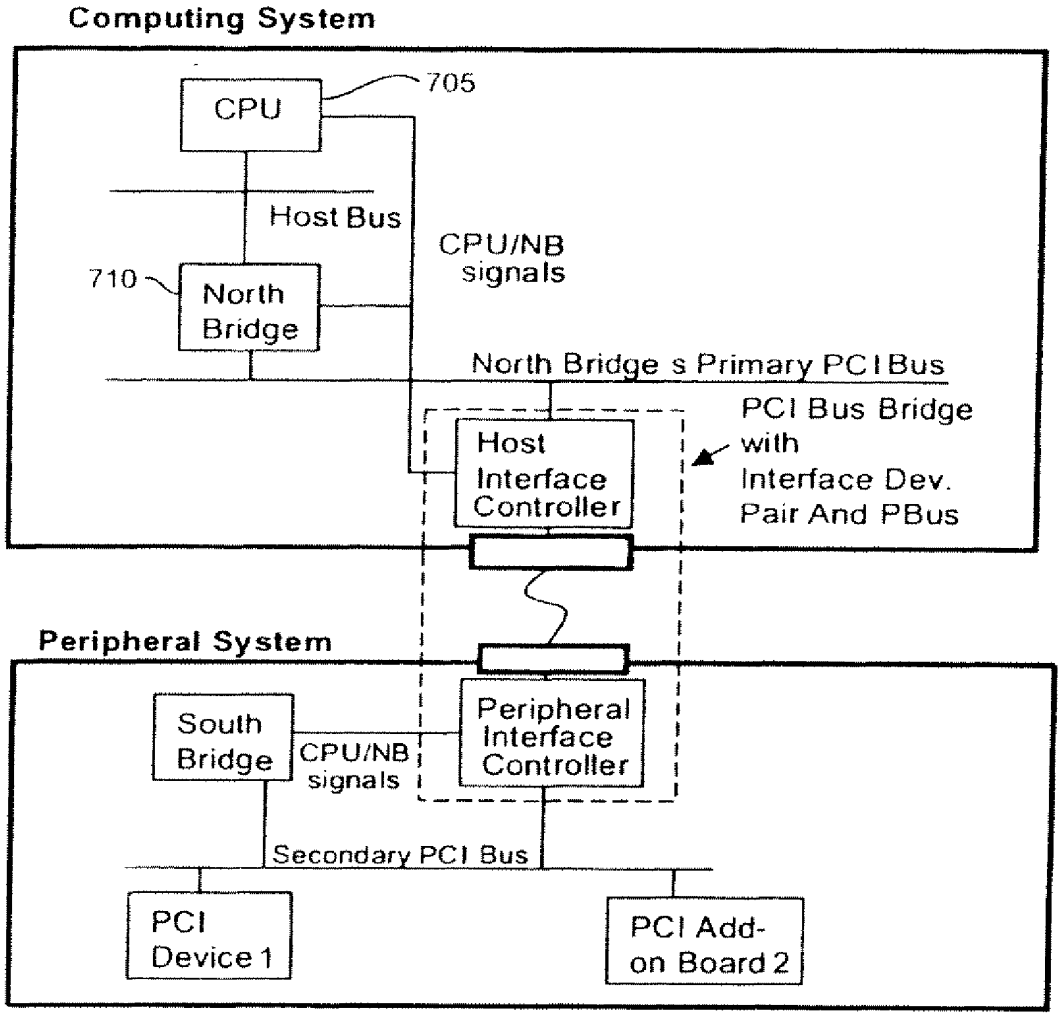

Computing System
CPU
705
Host Bus
CPU/NB
signals
710
North
Bridge
North Bridge s Primary PCI Bus
PCI Bus Bridge
with
Interface Dev.
Pair And PBus
Host
Interface
Controller
Peripheral System
South
Bridge
CPU/NB
signals
Peripheral
Interface
Controller
Secondary PCI Bus
PCI
Device 1
PCI Add-
on Board 2

FIGURE 7

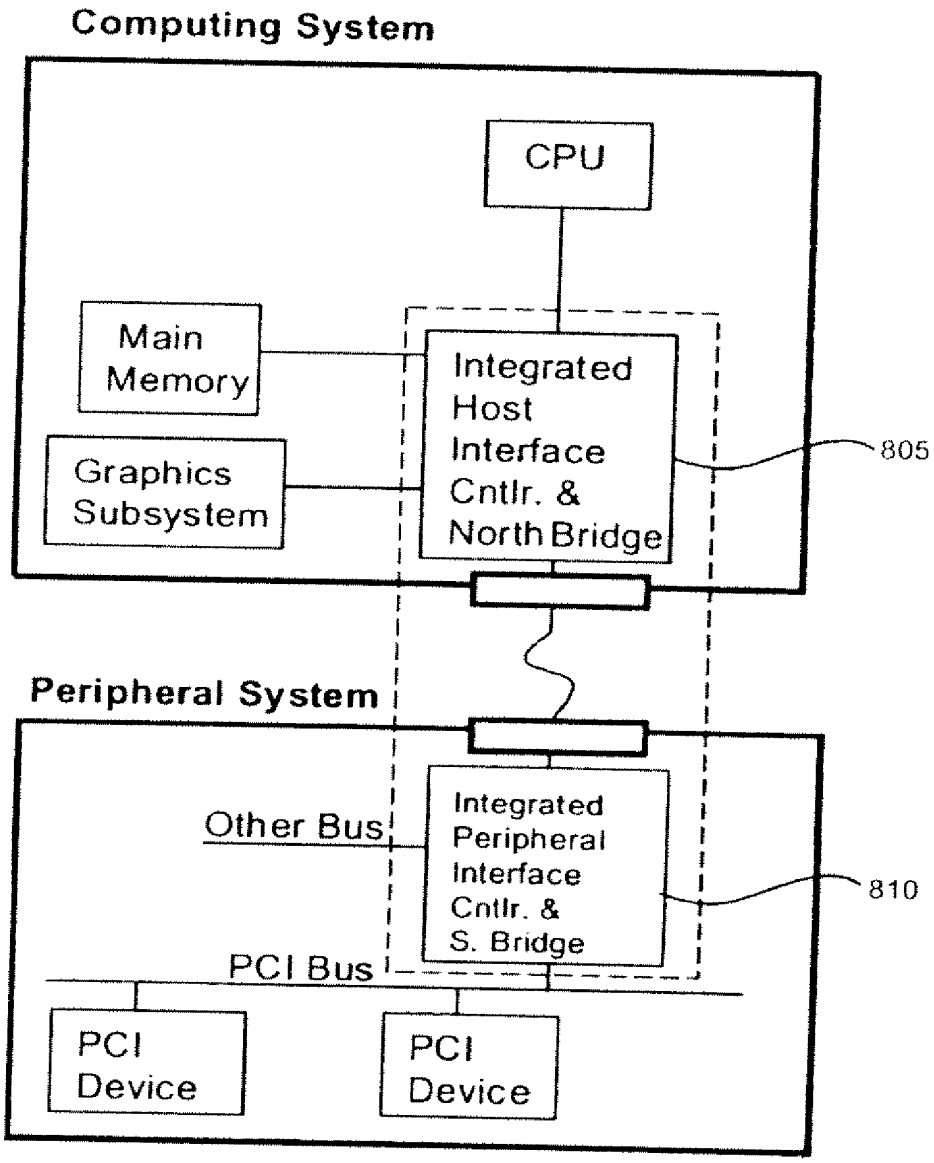

Computing System
CPU
Main Memory
Graphics Subsystem
Integrated Host Interface Cntlr. & North Bridge
805
Peripheral System
Other Bus
Integrated Peripheral Interface Cntlr. & S. Bridge
810
PCI Bus
PCI Device
PCI Device

FIGURE 8

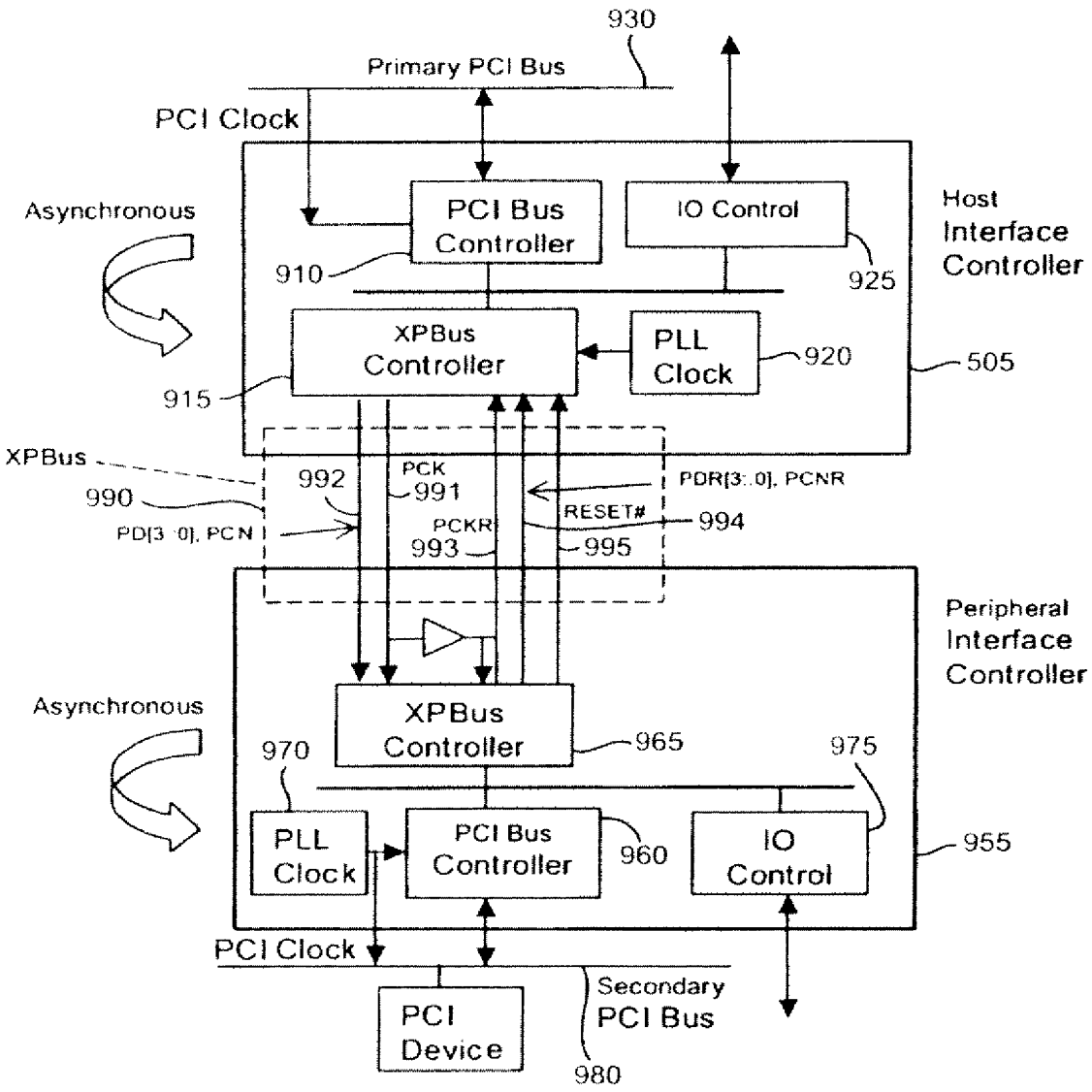

930
Primary PCI Bus
PCI Clock
Asynchronous
PCI Bus Controller
IO Control
Host Interface Controller
910
925
XPBus Controller
PLL Clock
920
505
915
XPBus
990
992
PCK
991
PDR[3:0], PCNR
PD[3:0], PCN
PCKR
993
RESET#
994
995
Peripheral Interface Controller
Asynchronous
XPBus Controller
965
970
975
PLL Clock
PCI Bus Controller
960
IO Control
955
PCI Clock
Secondary PCI Bus
PCI Device
980

FIGURE 9

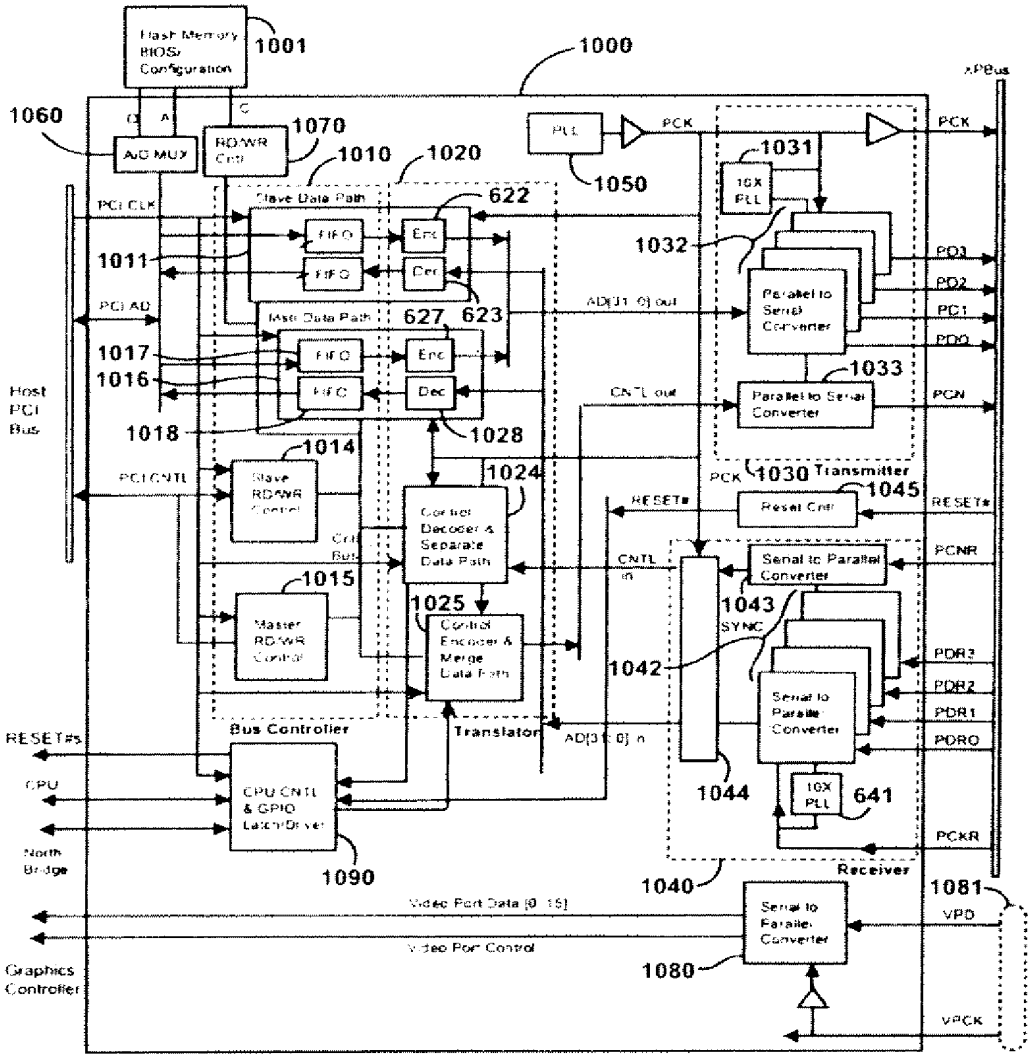

Flash Memory BIOS/ Configuration
1001
1000
1060
A/D MUX
RD/WR Ctrl
1070
1010
1020
PLL
1050
PCK
xPBus
1031
10X PLL
1032
PCI CLK
Slave Data Path
622
FIFO
Enc
Dec
1011
PCI AD
Mast Data Path
627
623
AD[31..0] out
Parallel to Serial Converter
PD3
PD2
PC1
PD0
1017
1016
1033
CNTL out
PCN
Host PCI Bus
1018
1028
1014
PCI CNTL
Slave R/D/WR Control
1024
Control Decoder & Separate Data Path
PCK
1030 Transmitter
RESET#
Reset Cntl
1045
RESET#
CNTL
PCNR
Serial to Parallel Converter
1015
1025
1043
SYNC
Master R/D/WR Control
Control Encoder & Merge Data Path
1042
PDR3
PDR2
PDR1
PDR0
Serial to Parallel Converter
Bus Controller
Translator
AD[31..0] n
RESET#s
CPU
CPU CNTL & GPIO Latch/Driver
1044
10X PLL
641
PCKR
North Bridge
1090
1040
Receiver
1081
Video Port Data [0..15]
VPD
Serial to Parallel Converter
Video Port Control
1080
Graphics Controller
VPCK

FIGURE 10

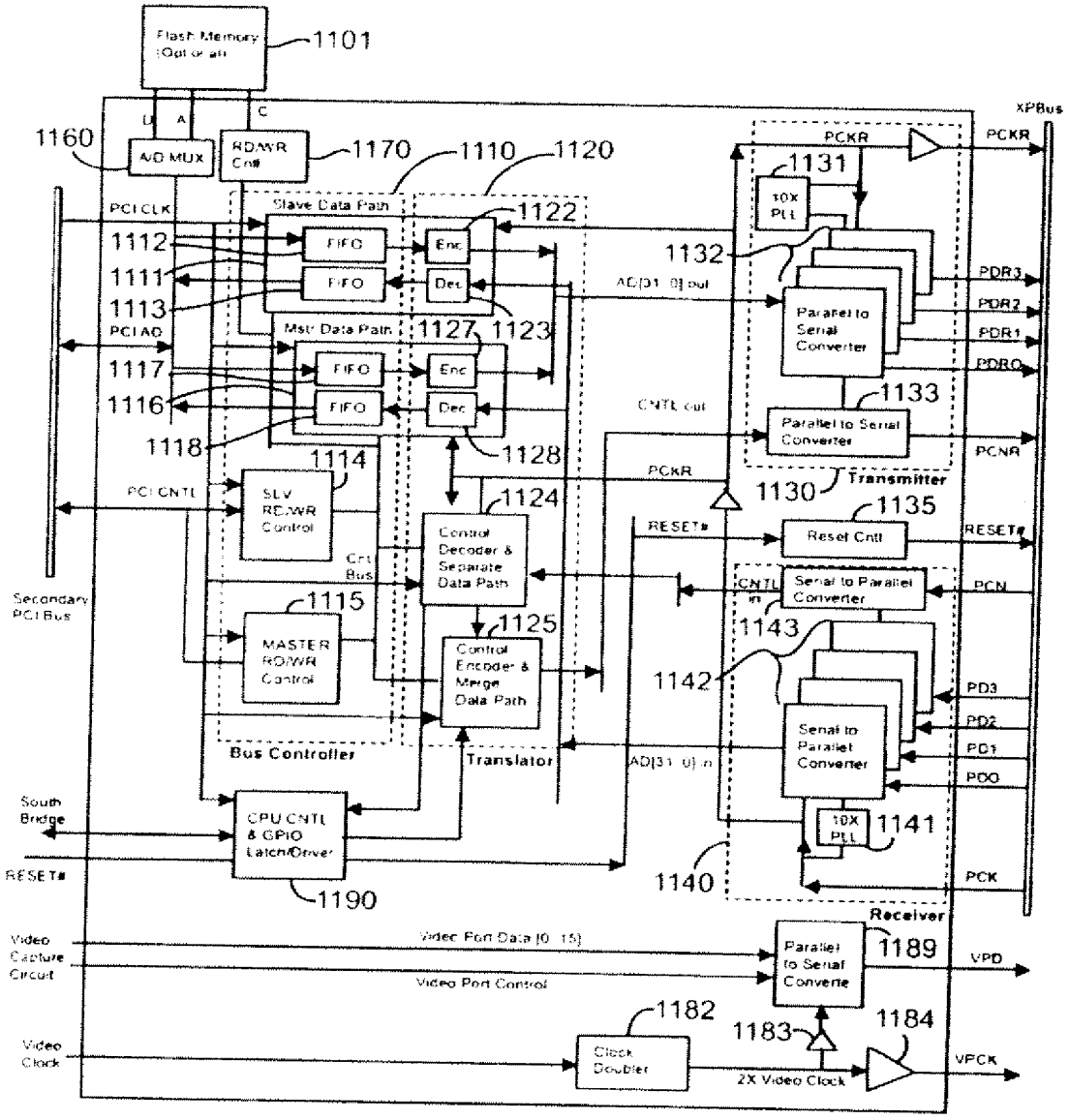

Flash Memory (Optional)
1101
A/D MUX
RD/WR Cntl
1160
1170
1110
1120
Slave Data Path
1122
FIFO
Enc
Dec
1112
1111
1113
PCI CLK
PCI AD
Mstr Data Path
1127
1123
1117
1116
1118
1114
PCI CNTL
SLV RD/WR Control
1124
Control Decoder & Separate Data Path
Cntl Bus
1115
MASTER RD/WR Control
1125
Control Encoder & Merge Data Path
Bus Controller
Translator
Secondary PCI Bus
South Bridge
RESET#
CPU CNTL & GPIO Latch/Driver
1190
1128
PCKR
1131
10X PLL
1132
AD[31..0] out
Parallel to Serial Converter
1133
CNTL out
Transmitter
1130
1135
Reset Cntl
CNTL in
Serial to Parallel Converter
1143
1142
Serial to Parallel Converter
1141
1140
Receiver
XPBus
PDR3
PDR2
PDR1
PDR0
PCNR
RESET#
PCN
PD3
PD2
PD1
PD0
PCK
AD[31..0] in
Video Capture Circuit
Video Port Data [0..15]
Video Port Control
1189
Parallel to Serial Converte
VPD
Video Clock
1182
Clock Doubler
1183
1184
2X Video Clock
VPCK

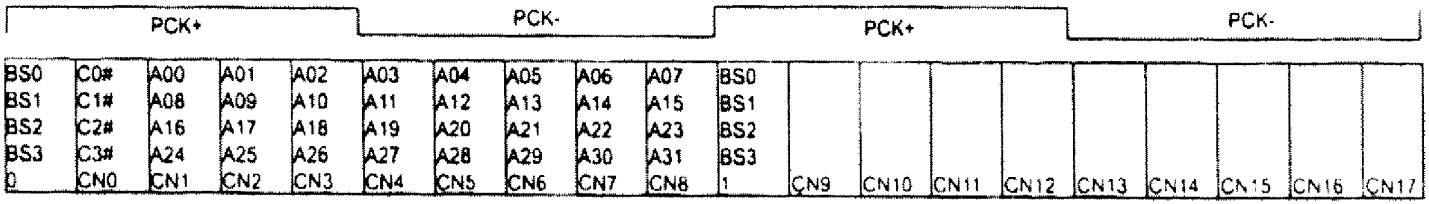
FIGURE 11

	Symbol	Signal	Data Rate	Description
1	PD0 RTN			GND
2	PD0 +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 0 +
3	PD0 -			Computer to Peripheral LVDS Data 0 -
4	PD1 RTN			GND
5	PD1 +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 1 +
6	PD1 -			Computer to Peripheral LVDS Data 1 -
7	PD2 RTN			GND
8	PD2 +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 2 +
9	PD2 -			Computer to Peripheral LVDS Data 2 -
10	PD3 RTN			GND
11	PD3 +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 3 +
12	PD3 -			Computer to Peripheral LVDS Data 3 -
13	PCK RTN			GND
14	PCK +	Clock	Clock rate	Computer to Peripheral LVDS Clock +
15	PCK -			Computer to Peripheral LVDS Clock -
16	PCN RTN			GND
17	PCN +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Control +
18	PCN -			Computer to Peripheral LVDS Control -
19	PDR0 RTN			GND
20	PDR0 +	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 0 +
21	PDR0 -			Peripheral to Computer LVDS Data 0 -
22	PDR1 RTN			GND
23	PDR1 +	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 1 +
24	PDR1 -			Peripheral to Computer LVDS Data 1 -
25	PDR2 RTN			GND
26	PDR2 +	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 2 +
27	PDR2 -			Peripheral to Computer LVDS Data 2 -
28	PDR3 RTN			GND
29	PDR3 +	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 3 +
30	PDR3 -			Peripheral to Computer LVDS Data 3 -
31	PCKR RTN			GND
32	PCKR +	Reverse Dir. Clock	Clock rate	Peripheral to Computer LVDS Clock +
33	PCKR -			Peripheral to Computer LVDS Clock -
34	PCNR RTN			GND
35	PCNR +	Synch. To PCKR	10 x Clock rate	Peripheral to Computer LVDS Control +
36	PCNR -			Peripheral to Computer LVDS Control -
37	RESET#		Asynchronous	Reset

FIGURE 12

PCK	CK+	CK+	CK+	CK+	CK+	CK-	CK-	CK-	CK-	CK-	CK+	CK+	CK+	CK+	CK+	CK-	CK-	CK-	CK-	CK-
PD0	BS0	CM0#	A00	A01	A02	A03	A04	A05	A06	A07	BS0	BE0#	D00	D01	D02	D03	D04	D05	D06	D07
PD1	BS1	CM1#	A08	A09	A10	A11	A12	A13	A14	A15	BS1	BE1#	D08	D09	D10	D11	D12	D13	D14	D15
PD2	BS2	CM2#	A16	A17	A18	A19	A20	A21	A22	A23	BS2	BE2#	D16	D17	D18	D19	D20	D21	D22	D23
PD3	BS3	CM3#	A24	A25	A26	A27	A28	A29	A30	A31	BS3	BE3#	D24	D25	D26	D27	D28	D29	D30	D31
PCN	CN0	CN1	CN2	CN3	CN4	CN5	CN6	CN7	CN8	CN9	CN0	CN1	CN2	CN3	CN4	CN5	CN6	CN7	CN8	CN9

FIGURE 13


PCK+
PCK-
PCK+
PCK-
BS0 C0# A00 A01 A02 A03 A04 A05 A06 A07 BS0
BS1 C1# A08 A09 A10 A11 A12 A13 A14 A15 BS1
BS2 C2# A16 A17 A18 A19 A20 A21 A22 A23 BS2
BS3 C3# A24 A25 A26 A27 A28 A29 A30 A31 BS3
0 CN0 CN1 CN2 CN3 CN4 CN5 CN6 CN7 CN8 1 CN9 CN10 CN11 CN12 CN13 CN14 CN15 CN16 CN17

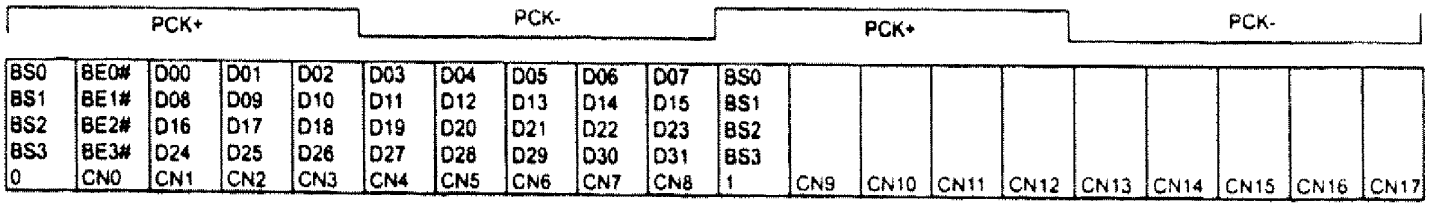

PCK+
PCK-
PCK+
PCK-
BS0 BE0# D00 D01 D02 D03 D04 D05 D06 D07 BS0
BS1 BE1# D08 D09 D10 D11 D12 D13 D14 D15 BS1
BS2 BE2# D16 D17 D18 D19 D20 D21 D22 D23 BS2
BS3 BE3# D24 D25 D26 D27 D28 D29 D30 D31 BS3
0 CN0 CN1 CN2 CN3 CN4 CN5 CN6 CN7 CN8 1 CN9 CN10 CN11 CN12 CN13 CN14 CN15 CN16 CN17

FIGURE 14

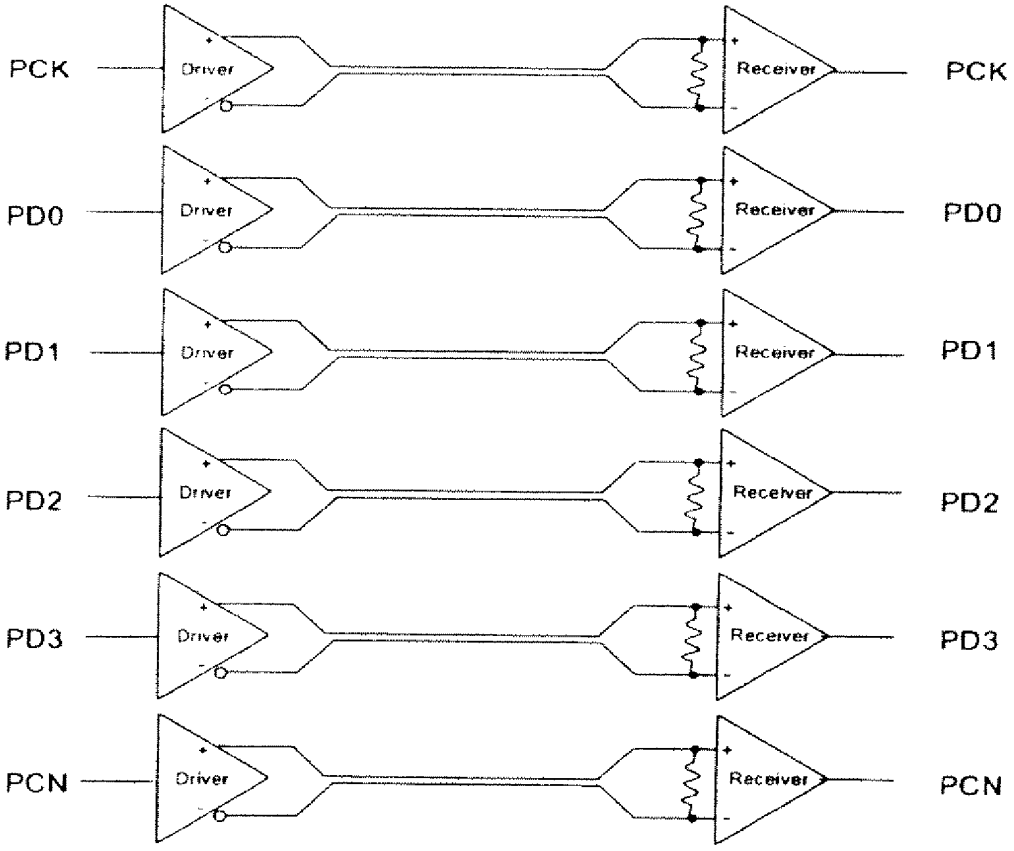

PCK
Driver
Receiver
PCK
PD0
Driver
Receiver
PD0
PD1
Driver
Receiver
PD1
PD2
Driver
Receiver
PD2
PD3
Driver
Receiver
PD3
PCN
Driver
Receiver
PCN

FIGURE 15

Name	Type	Pins	Description
AD[31::0]	TS	32	Multiplexed Address/Data. AD is driven to a valid state when GNT# is asserted.
C/BE[3::0]#	TS	4	Multiplexed Command/Byte Enables. For a two-address transaction, 1st address phase carries the command, and the 2nd address phase carries the transaction type. C/BE is driven to a valid state when GNT# is asserted.
FRAME#	STS	1	Indicates beginning and duration of a PCI transaction. When the bus is idle, FRAME# is driven to High for 1 cycle. A pull-up resistor sustains STS signal.
IRDY#	STS	1	Initiator Ready. IRDY# is driven High for 1 cycle if bus is idle, and the state is sustained by a pull-up resistor.
TRDY#	STS	1	Target Ready. When bus is idle, TRDY# is driven High for 1 cycle if bus is idle. An external pull-up resistor sustains STS signal.
DEVSEL#	STS	1	Device Select. DEVSEL# is asserted by target to indicate it is ready to accept the transaction. HIC decodes address of a transaction to decide the need to assert DEVSEL#. As an initiator, HIC waits for 5 cycles to detect assertion of DEVSEL# by the target; otherwise HIC terminates with a master abort. DEVSEL# is driven High for 1 cycle when bus is idle, and the state is sustained by a pull-up resistor.
STOP#	STS	1	Target request to stop transaction. There are 3 cases: STOP#, TRDY# & DEVSEL# asserted: disconnect with data transfer Only STOP# & DEVSEL# asserted: request initiator to retry later Only STOP# asserted: target abort STOP# is driven High for 1 cycle when bus is idle, and the state is sustained by a pull-up resistor.
PAR	TS	1	Even parity for 36 bits of AD & C/BE#. PAR is sent one cycle after address or data is valid. In write transaction, initiator sends PAR one cycle after write data is valid. In read transaction, target sends PAR one cycle after read data is valid.
LOCK#	Input	1	Initiator request lock on target downstream. LOCK# is asserted 1 clock cycle after address phase by an initiator wanting to perform an atomic operation that take more than one transaction to complete. HIC passes the LOCK# request to the secondary PCI bus. HIC does not drive LOCK# or propagate LOCK# upstream.
IDSEL#	Input	1	Chip Select for Type 0 configuration access. During a Type 0 configuration transaction, the initiator asserts IDSEL# during the address phase to select HIC. HIC responds by asserting DEVSEL#.
PERR#	STS	1	Data Parity Error on all transactions except Special Cycle. PERR# is driven one clock cycle after PAR. PERR# is asserted by target during write transactions, and by initiator during read transactions.
SERR#	OD	1	System Error. HIC asserts SERR# under the following conditions: Address parity error, Secondary bus SERR# asserted, Posted write transaction: data parity error on target bus, Posted write transaction discarded, Master abort, Target abort Delayed read or write transaction discarded, and Delayed transaction master timeout.
REQ#	TS	1	Request for bus. If a target retry or disconnect is received in response to initiating a transaction, HIC deasserts REQ# for at least 2 cycles before asserting it again.
GNT#	Input	1	Bus is granted to HIC. HIC can initiate transaction if GNT# is asserted and the bus is idle. When HIC is not requesting bus and GNT# is asserted, HIC must drive AD, C/BE, and PAR to valid logic levels.
CLKRUN#	I/OD	1	Input indicating clock status. HIC can request the central clock resource to start, speed up or maintain the PCI clock. There are 3 clocking states:
PCICK	Input	1	Clock running, Clock about to stop/slow down, and Clock stopped/slowed. PCI Clock. All inputs are sampled on the rising edge of PCICK. Frequency

FIGURE 16

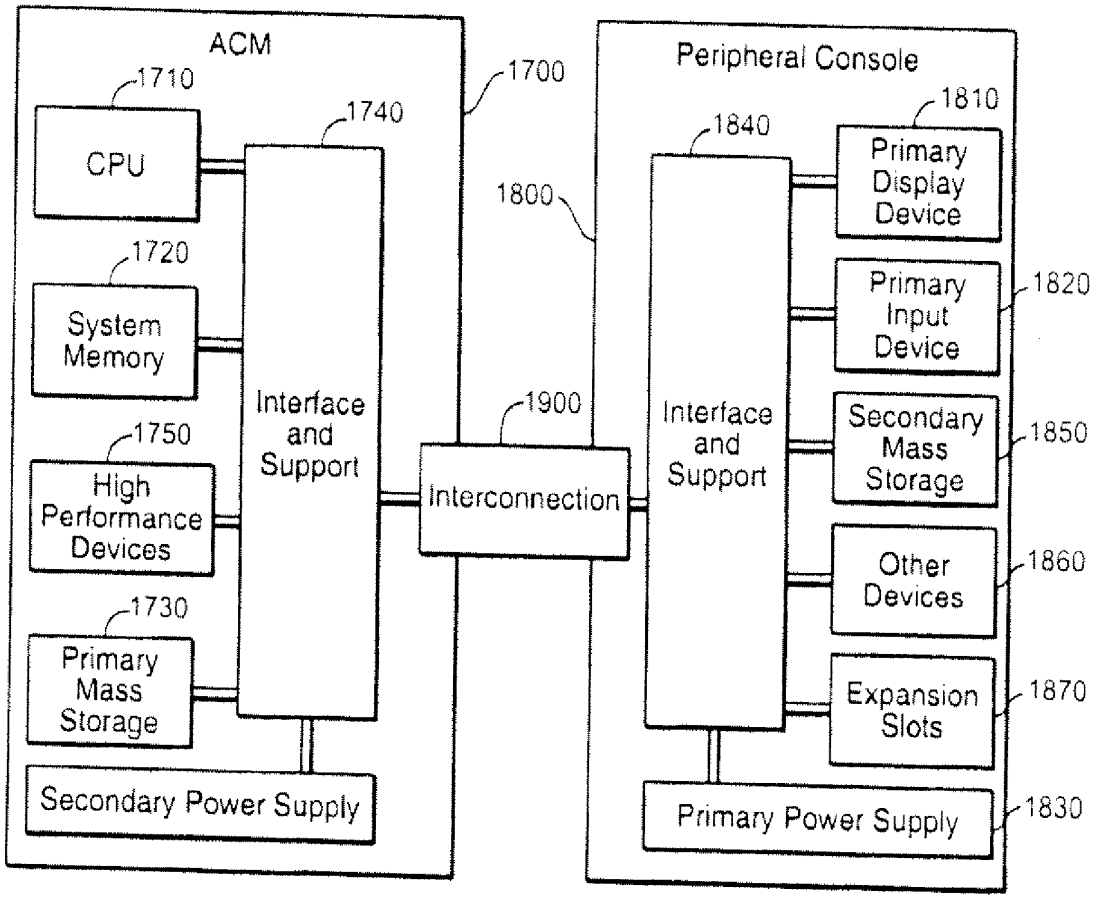


FIGURE 17

Ex. 1042, Page 86

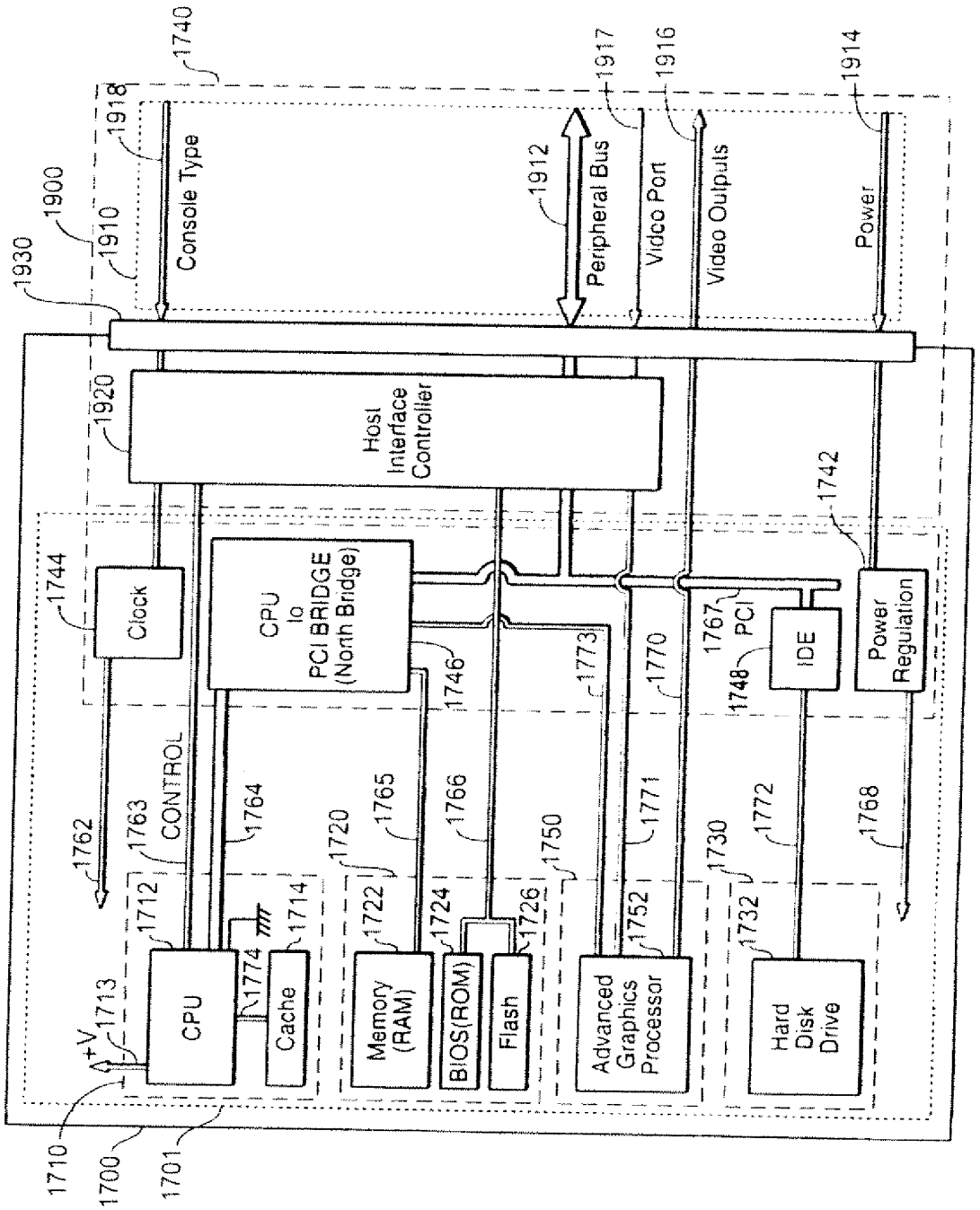

1740
1917
1916
1914
1918
1900
1910
1912
1930
Console Type
Peripheral Bus
Video Port
Video Outputs
Power
1920
Host Interface Controller
1742
1744
Clock
CPU to PCI BRIDGE (North Bridge)
1746
1773
1770
1767
PCI
1748
IDE
Power Regulation
1762
1763
CONTROL
1764
1765
1766
1720
1750
1771
1772
1730
1768
1712
1722
1724
1726
1752
1732
1713
+V
1774
1714
CPU
Cache
Memory (RAM)
BIOS(ROM)
Flash
Advanced Graphics Processor
Hard Disk Drive
1710
1700
1701

FIGURE 18

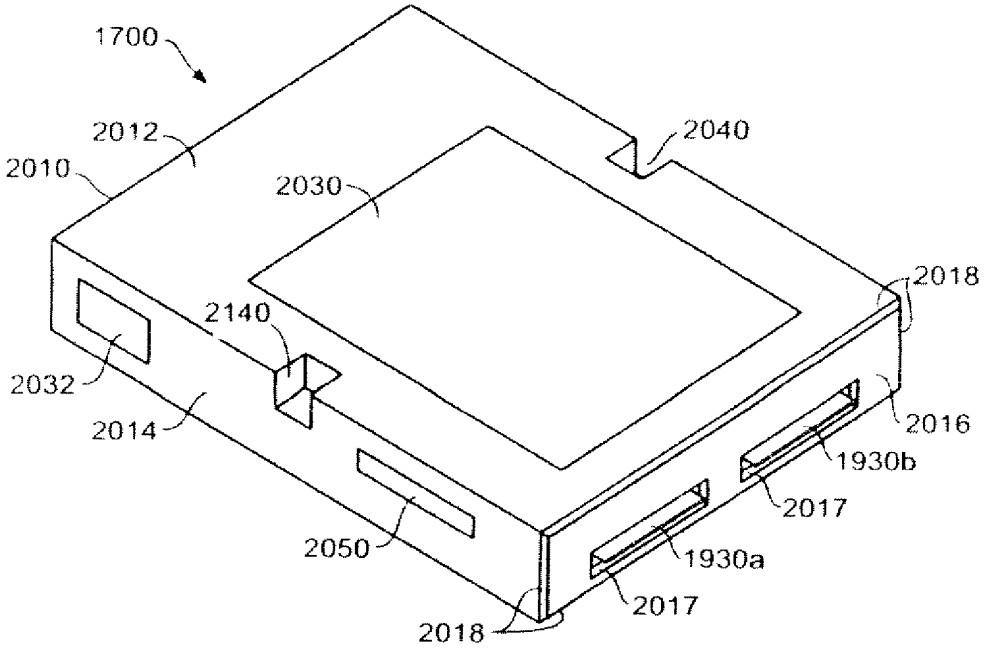

1700
2012
2010
2040
2030
2018
2140
2032
2014
2016
1930b
2017
2050
1930a
2017
2018

FIGURE 19

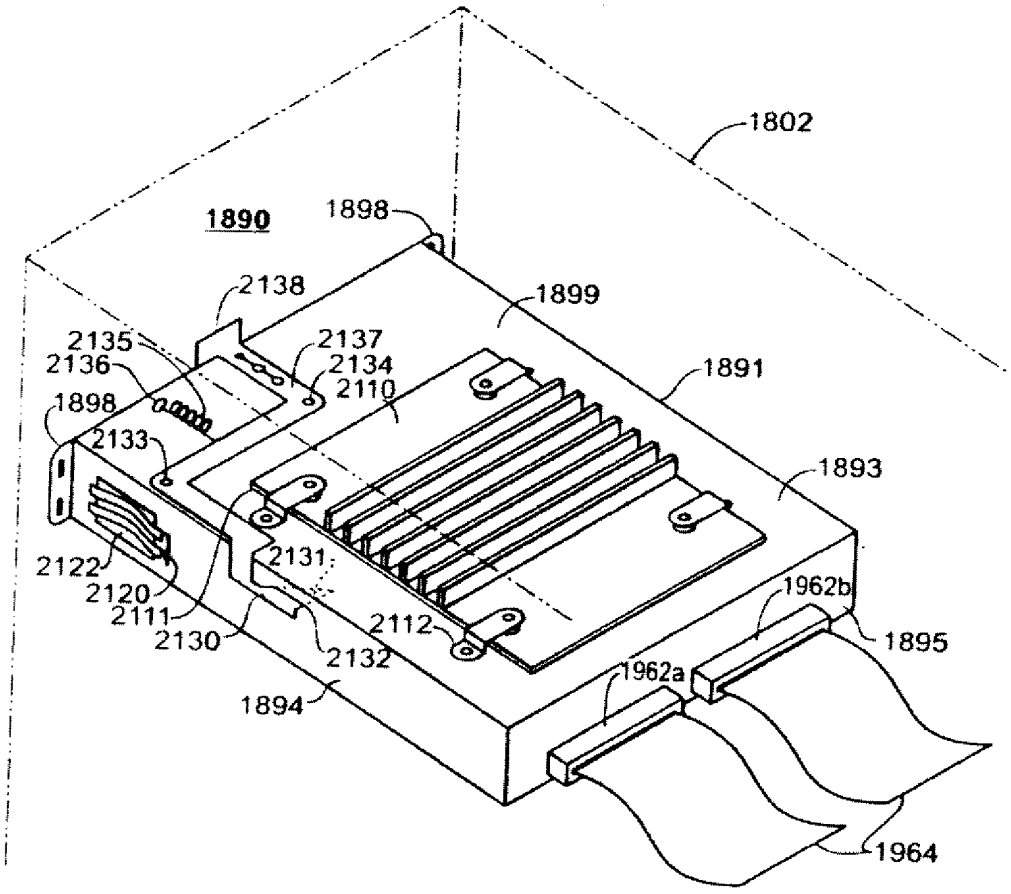

1802
1890
1898
2138
1899
2135
2137
2136
2134
2110
1891
1898
2133
1893
2122
2131
2120
2111
2130
2112
1962b
1895
2132
1962a
1894
1964

FIGURE 19B

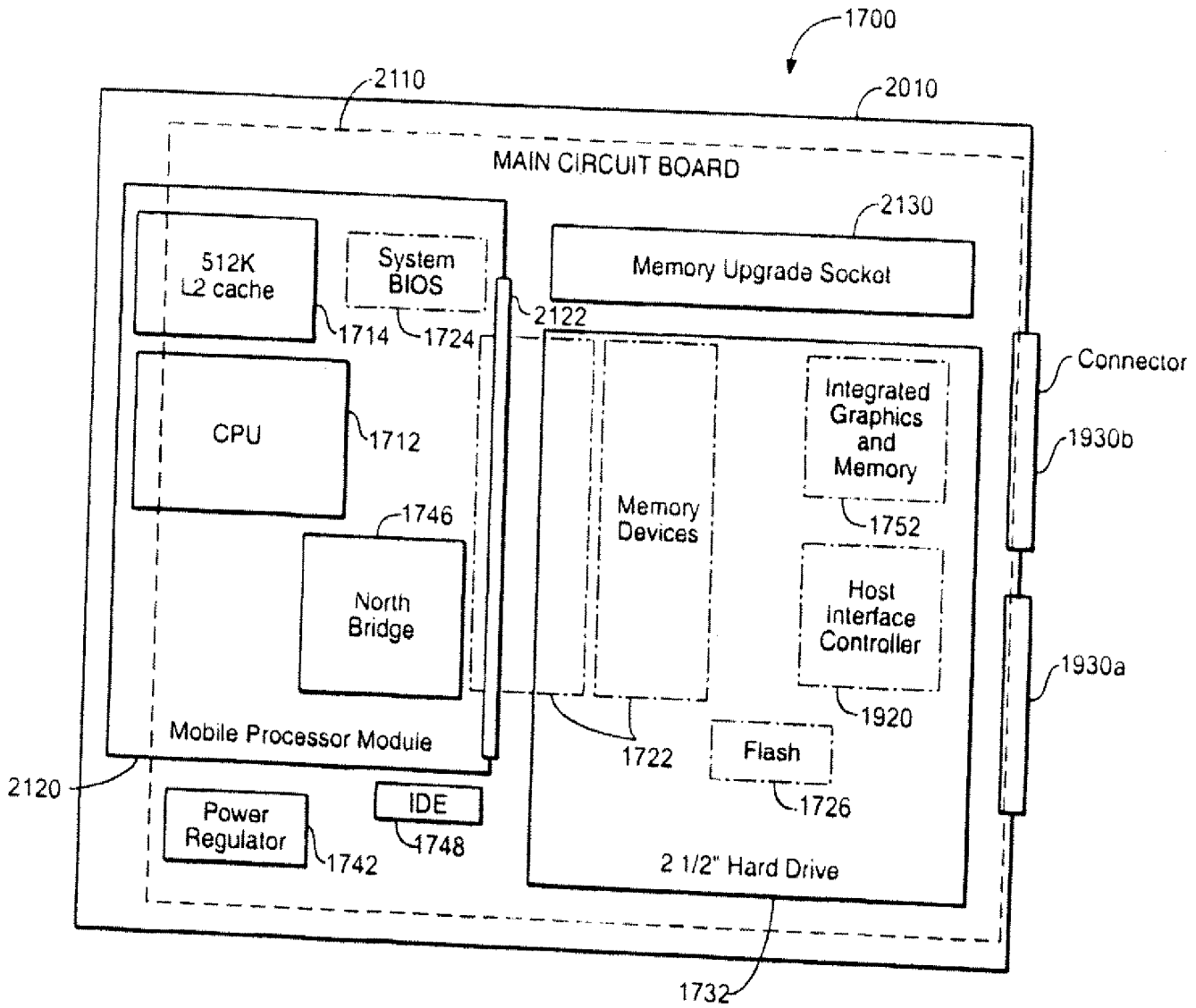


FIGURE 20

Ex. 1042, Page 90

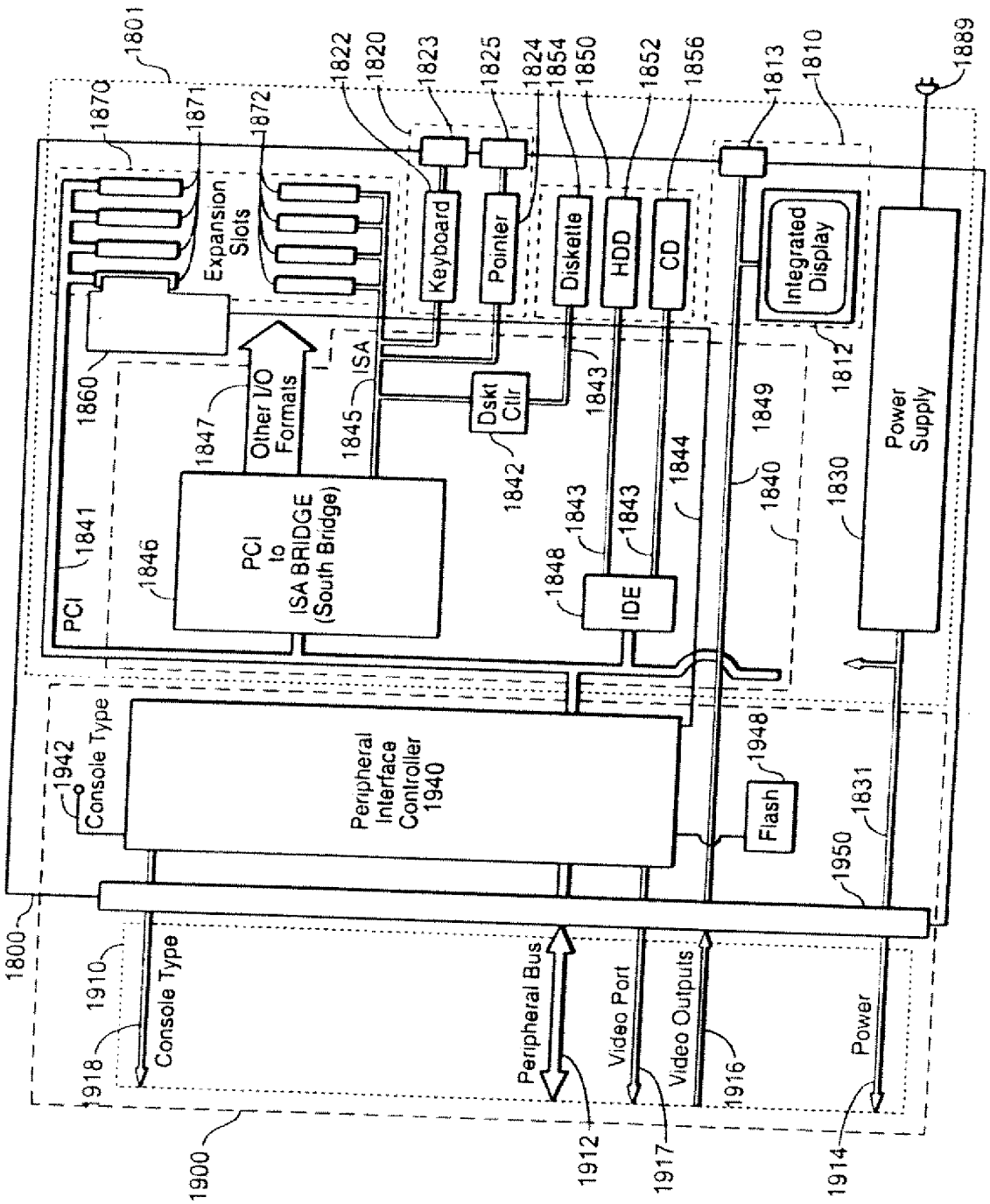

1801
1870
1871
1872
1822
1820
1823
1825
1824
1854
1850
1852
1856
1813
1810
1889
Expansion Slots
Keyboard
Pointer
Diskette
HDD
CD
Integrated Display
1860
1847
Other I/O Formats
ISA
1845
Dskt Ctlr
1842
1843
1849
1812
Power Supply
PCI
1841
1846
PCI to ISA BRIDGE (South Bridge)
1840
1844
1830
1848
IDE
1942
Console Type
Peripheral Interface Controller 1940
1948
Flash
1831
1950
1800
1910
Console Type
Peripheral Bus
Video Port
Video Outputs
Power
1918
1916
1900
1912
1917
1914

FIGURE 21

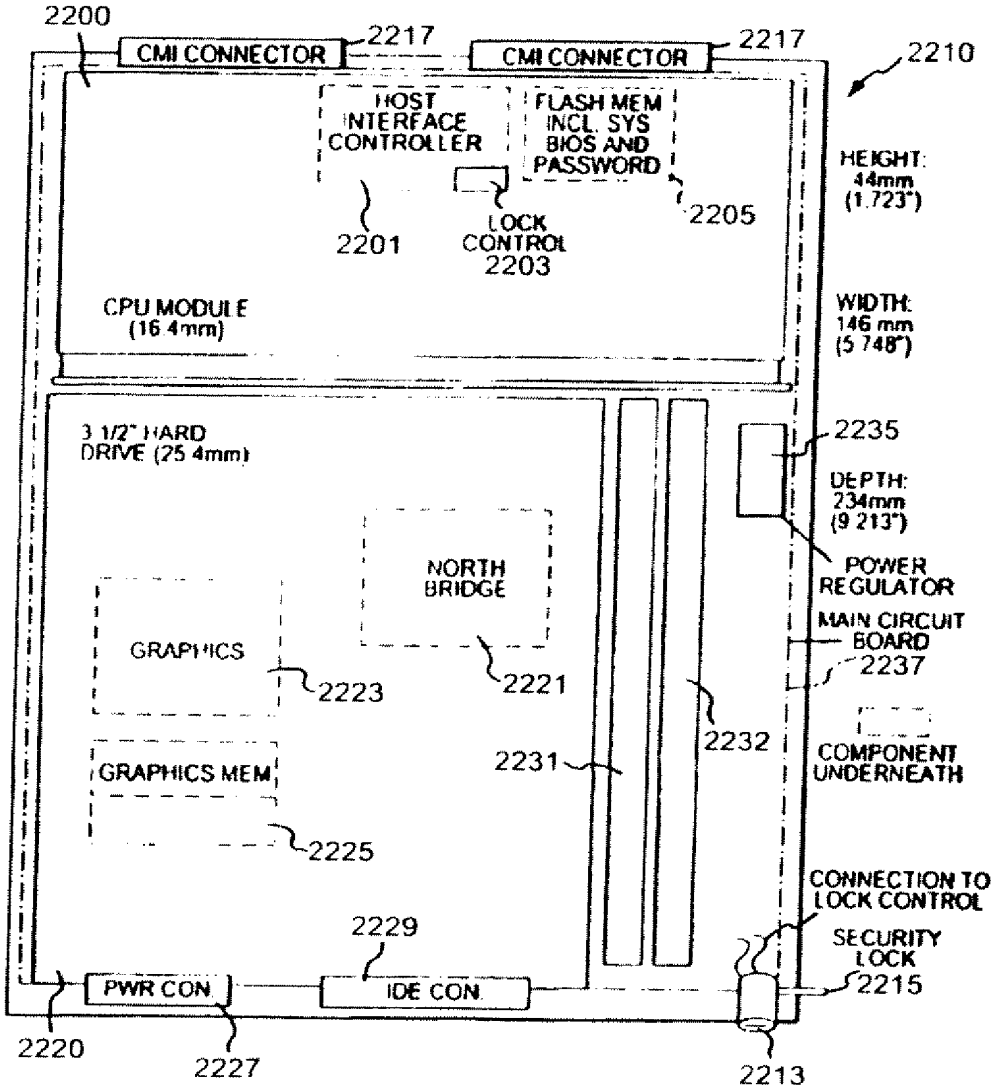

2200
CMI CONNECTOR
2217
CMI CONNECTOR
2217
2210
HOST INTERFACE CONTROLLER
FLASH MEM INCL. SYS BIOS AND PASSWORD
2205
2201
LOCK CONTROL 2203
HEIGHT: 44mm (1.723")
CPU MODULE (16.4mm)
WIDTH: 146 mm (5.748")
3 1/2" HARD DRIVE (25.4mm)
2235
DEPTH: 234mm (9.213")
NORTH BRIDGE
POWER REGULATOR
MAIN CIRCUIT BOARD
2237
GRAPHICS
2223
2221
2232
2231
COMPONENT UNDERNEATH
GRAPHICS MEM
2225
CONNECTION TO LOCK CONTROL
2229
SECURITY LOCK
2215
PWR CON
IDE CON
2220
2227
2213

FIGURE 22

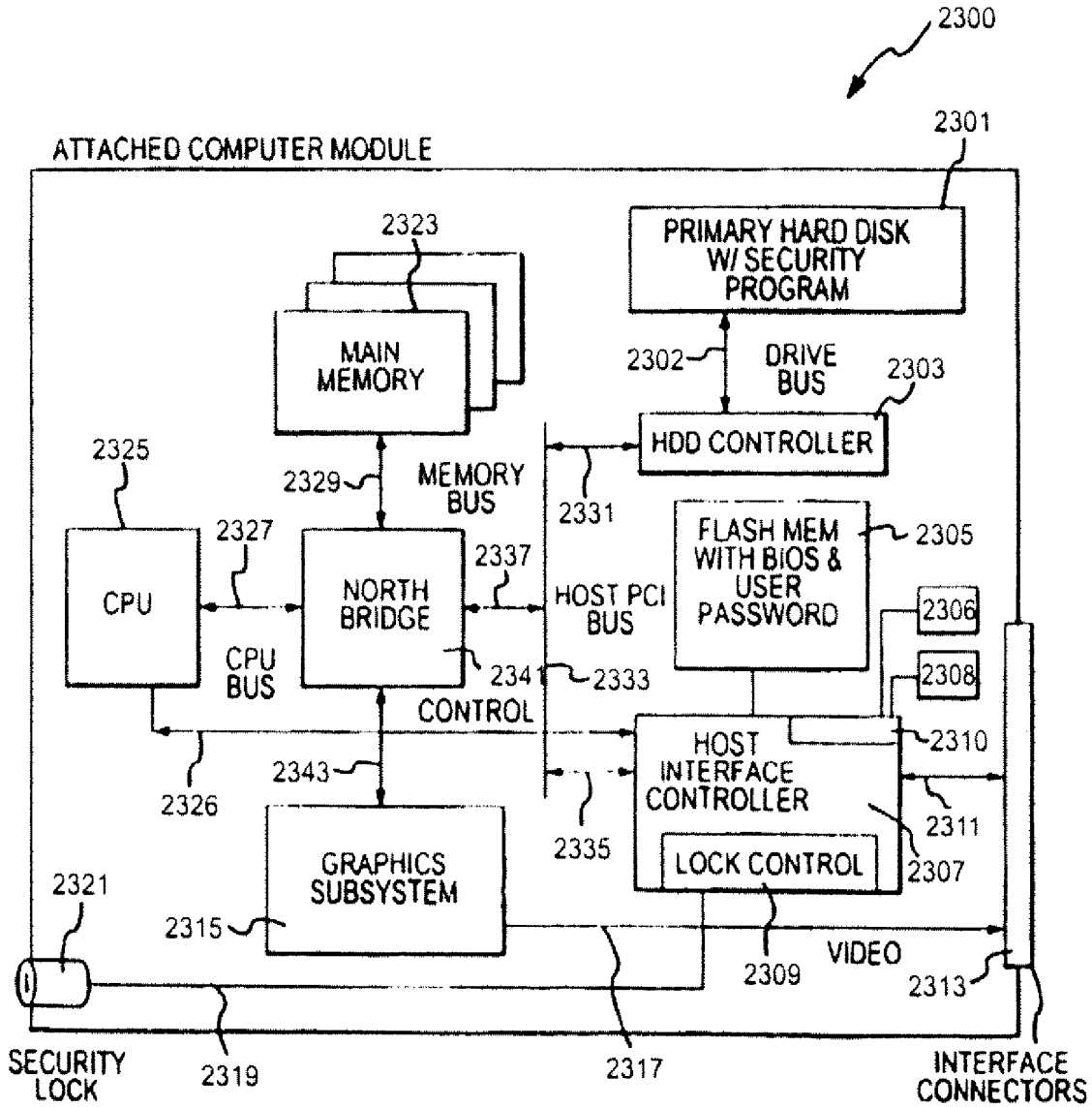


FIGURE 23

Ex. 1042, Page 93

DECLARATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated next to my name;

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNDIRECTIONAL SERIAL BIT CHANNELS

the specification of which:

(check one)

[X] is attached hereto:

[] was filed as United States Application Serial No. ____ on ____, and was amended on (if applicable);

[] was filed as PCT International Application No. ___ on ___ and was amended under PCT Article 19 or Article 34 on ___ (if applicable);

I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above;

I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information which is known to me to be material to the patentability of said invention in accordance with 37 C.F.R. §1.56;

I hereby claim foreign priority benefits under 35 U.S.C. §119 and/or §365 of any foreign application(s) for patent, any foreign application(s) for inventor's certificate, or any PCT international application(s) designating at least one country other than the United States of America listed below; I have also identified below any foreign application(s) for patent, any foreign application(s) for inventor's certificate, or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

Prior Foreign Application(s)

COUNTRY/INTERNATIONAL	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY CLAIMED
			[] YES [] NO
			[] YES [] NO

I hereby claim the benefit under 35 U.S.C. §119(e) of any United States provisional application(s) listed below:

60/134,122 (Application Number) 14/05/1999 (Filing Date) (day, month, year)

(Application Number) (Filing Date) (day, month, year)

I hereby claim the benefit under 35 U.S.C. §120 and/or §365 of any United States application(s) or of any international application(s) designating the United States of America that is/are listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior application(s) in the manner provided by the first paragraph of 35 U.S.C. §112, I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to patentability as defined in 37 C.F.R. §1.56 which became available between the filing date(s) of the prior application(s) and the national or PCT international filing date of this application:

Prior U.S. Application(s) or PCT International Applications Designating the U.S. for benefit under 35 U.S.C. §120

U.S. APPLICATIONS		STATUS (*check one*)		
U.S. APPLICATION NO.	U.S. FILING DATE (day, month, year)	Pending	Patented	Abandoned
12/077,503	18/03/2008	[X]	[]	[]
11/166,656	24/06/2005	[]	[X]	[]
11/097,694	31/03/2005	[]	[X]	[]
10/772,214	03/02/2004	[]	[X]	[]
09/569,758	12/05/2000	[]	[X]	[]
PCT APPLICATIONS DESIGNATING THE U.S.				
PCT APPLICATION NO.	PCT FILING DATE (day, month, year)	U.S. APPLICATION NOS. (if any)		
			[]	[] []
			[]	[] []

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States

Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of first inventor:

Inventor's signature William W. Y. Chu Date 7/16/2009
Residence: **William W. Y. Chu**
Citizen of: **United States**
Post Office Address: **1320 Miravalle Avenue, Los Altos, CA 94024**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:	William W. Y. Chu	Confirmation No.:	Not Yet Assigned
Serial No.:	Not Yet Assigned	Group Art Unit:	Not Yet Assigned
Filed:	July 16, 2009	Examiner:	Not Yet Assigned

FOR: MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNDIRECTIONAL SERIAL BIT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

POWER BY ASSIGNEE AND STATEMENT UNDER 37 C.F.R. §3.73(b)

The Assignee of the entire right, title, and interest in the above-identified application hereby grants the registered practitioners of Cooley Godward Kronish LLP included in the Customer Number provided below power to act, prosecute, and transact all business in the U.S. Patent and Trademark Office in connection with this application, any applications claiming priority to this application, and any patents issuing therefrom.

The Assignee certifies that to the best of its knowledge and belief it is the owner of the entire right, title, and interest in and to the above-identified application as evidenced by:

[] An assignment document, a copy of which is enclosed herewith;

[X] An assignment previously recorded in the U.S. Patent and Trademark Office at Reel **022460**, Frame **0848**; and Reel **022461**, Frame **0702**.

Please direct all telephone calls and correspondence to:

CUSTOMER NUMBER: **58249**

COOLEY GODWARD KRONISH LLP
ATTN: Patent Group
777 6th Street NW, Suite 1100
Washington, DC 20001
Tel: (650) 843-5852
Fax: (202) 842-7899

The undersigned (whose title is supplied below) is empowered to sign this statement on behalf of the Assignee.

Date: 7/16/2009

Signature: William W. Y. Chu
Name: William W. Y. Chu
Title: President
Company: ACQI LLC

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNDIRECTIONAL SERIAL BIT CHANNELS
First Named Inventor/Applicant Name:	William W. Y. Chu
Filer:	Cliff Z. Liu/Gina Luna
Attorney Docket Number:	ACQI-010/10US 310578-2052

Filed as Small Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility filing Fee (Electronic filing)	4011	1	82	82
Utility Search Fee	2111	1	270	270
Utility Examination Fee	2311	1	110	110
Pages:				
Claims:				
Claims in excess of 20	2202	23	26	598
Independent claims in excess of 3	2201	10	110	1100
Miscellaneous-Filing:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**2160**

Electronic Acknowledgement Receipt

EFS ID:	5719067
Application Number:	12504534
International Application Number:	
Confirmation Number:	1286
Title of Invention:	MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNDIRECTIONAL SERIAL BIT CHANNELS
First Named Inventor/Applicant Name:	William W. Y. Chu
Customer Number:	58249
Filer:	Cliff Z. Liu/Gina Luna
Filer Authorized By:	Cliff Z. Liu
Attorney Docket Number:	ACQI-010/10US 310578-2052
Receipt Date:	16-JUL-2009
Filing Date:	
Time Stamp:	18:39:35
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal of New Application	ACQI_010_10US_Application_Transmittal.pdf	63652 63f9261aeda09f27fe919bffd38ba1664ea2479a	no	2

Warnings:	
Information:	

2		ACQI_010_01US_Specification_Drawings.pdf	3697606 06f5b979325199e29a934d2ec81123f3b285f6d0	yes	91

Multipart Description/PDF files in .zip description		
Document Description	**Start**	**End**
Specification	1	55
Claims	56	66
Abstract	67	67
Drawings-only black and white line drawings	68	91

Warnings:					
Information:					
3	Oath or Declaration filed	ACQI_010_10US_Declaration.pdf	116147 82c8d8114576a6209ec34c95362aa6172c3a9ccc	no	3
Warnings:					
Information:					
4	Power of Attorney	ACQI_010_10US_Power.pdf	49256 1a6ed0634f3853b997c33e16c605eb9be63029b0	no	2
Warnings:					
Information:					
5	Fee Worksheet (PTO-875)	fee-info.pdf	38546 14bea63ce501f53b60647086e26bad946135cafd	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	3965207		

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronic Patent Application Fee Transmittal

Application Number:	12504534
Filing Date:	
Title of Invention:	MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNDIRECTIONAL SERIAL BIT CHANNELS
First Named Inventor/Applicant Name:	William W. Y. Chu
Filer:	Cliff Z. Liu/Gina Luna
Attorney Docket Number:	ACQI-010/10US 310578-2052

Filed as Small Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility filing Fee (Electronic filing)	4011	1	82	82
Utility Search Fee	2111	1	270	270
Utility Examination Fee	2311	1	110	110
Pages:				
Claims:				
Claims in excess of 20	2202	23	26	598
Independent claims in excess of 3	2201	10	110	1100
Miscellaneous-Filing:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**2160**

Electronic Acknowledgement Receipt

EFS ID:	5719191
Application Number:	12504534
International Application Number:	
Confirmation Number:	1286
Title of Invention:	MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNDIRECTIONAL SERIAL BIT CHANNELS
First Named Inventor/Applicant Name:	William W. Y. Chu
Customer Number:	58249
Filer:	Cliff Z. Liu/Gina Luna
Filer Authorized By:	Cliff Z. Liu
Attorney Docket Number:	ACQI-010/10US 310578-2052
Receipt Date:	16-JUL-2009
Filing Date:	
Time Stamp:	18:53:36
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$2160
RAM confirmation Number	4785
Deposit Account	501283
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Fee Worksheet (PTO-875)	fee-info.pdf	38669 d5cbe285fe62dd592d32ddac793da4611f2bfa31	no	2

Warnings:

Information:

Total Files Size (in bytes):	38669

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Filing Date: 07/16/09

Approved for use through 7/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 12/504,534

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	82		N/A	
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	270		N/A	
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	110		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	43 minus 20 =	23	x$26	598	OR	x$52	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	13 minus 3 =	* 10	x$110	1100		x$220	
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $270 ($135 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))			195			390	
			TOTAL	2160		TOTAL	

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED – PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					N/A		OR	N/A	
						TOTAL ADD'T FEE		OR	TOTAL ADD'T FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)	OR	RATE ($)	ADDITIONAL FEE ($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					N/A		OR	N/A	
						TOTAL ADD'T FEE		OR	TOTAL ADD'T FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/504,534	07/16/2009	William W. Y. Chu	ACQI-010/10US 310578-2052

CONFIRMATION NO. 1286

58249
COOLEY GODWARD KRONISH LLP
ATTN: Patent Group
Suite 1100
777 - 6th Street, NW
WASHINGTON, DC 20001

FORMALITIES LETTER

OC000000037099178

Date Mailed: 07/30/2009

NOTICE TO FILE CORRECTED APPLICATION PAPERS

Filing Date Granted

An application number and filing date have been accorded to this application. The application is informal since it does not comply with the regulations for the reason(s) indicated below. Applicant is given TWO MONTHS from the date of this Notice within which to correct the informalities indicated below. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

The required item(s) identified below must be timely submitted to avoid abandonment:

- Replacement drawings in compliance with 37 CFR 1.84 and 37 CFR 1.121(d) are required. The drawings submitted are not acceptable because:
  - Numbers, letters, and reference characters on the drawings must measure at least 0.32 cm (1/8 inch) in height. See Figure(s) 2-4, 6, 10-16.
  - The drawings submitted to the Office are not electronically reproducible because portions of figures 1-4, 6, 9-16, 22 are missing and/or blurry.

Applicant is cautioned that correction of the above items may cause the specification and drawings page count to exceed 100 pages. If the specification and drawings exceed 100 pages, applicant will need to submit the required application size fee.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
12/504,534	07/16/2009	2111	2160	ACQI-010/10US 310578-2052	43	13

CONFIRMATION NO. 1286

58249
COOLEY GODWARD KRONISH LLP
ATTN: Patent Group
Suite 1100
777 - 6th Street, NW
WASHINGTON, DC 20001

FILING RECEIPT



Date Mailed: 07/30/2009

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

William W. Y. Chu, Los Altos, CA;

Power of Attorney: The patent practitioners associated with Customer Number 58249

Domestic Priority data as claimed by applicant

This application is a CON of 12/077,503 03/18/2008
which is a CON of 11/166,656 06/24/2005 PAT 7,376,779
which is a CON of 11/097,694 03/31/2005 PAT 7,363,415
which is a CON of 10/772,214 02/03/2004 PAT 7,099,981
which is a CON of 09/569,758 05/12/2000 PAT 6,718,415
which claims benefit of 60/134,122 05/14/1999

Foreign Applications

If Required, Foreign Filing License Granted: 07/27/2009

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/504,534**

Projected Publication Date: To Be Determined - pending completion of Corrected Papers

Non-Publication Request: No

Early Publication Request: No
**** SMALL ENTITY ****

Title

MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNDIRECTIONAL SERIAL BIT CHANNELS

Preliminary Class

710

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/504,534	07/16/2009	William W. Y. Chu	ACQI-010/10US 310578-2052

CONFIRMATION NO. 1286

58249
COOLEY GODWARD KRONISH LLP
ATTN: Patent Group
Suite 1100
777 - 6th Street, NW
WASHINGTON, DC 20001

POA ACCEPTANCE LETTER



Date Mailed: 07/30/2009

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 07/16/2009.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/rsantos/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

Substitute for form 1449A/PTO		*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Application Number	12/504,534
		Filing Date	July 16, 2009
		First Named Inventor	William W.Y. Chu
		Group Art Unit	2111
(*use as many sheets as necessary*)		Examiner Name	Unassigned
Sheet	1 of 6	Attorney Docket Number	ACQI-010/10US 310578-2052

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1.	US-3,996,585	12-07-1976	Hogan	
	2.	US-4,623,964	11-18-1986	Getz et al.	
	3.	US-4,700,362	10-13-1987	Todd et al.	
	4.	US-4,769,764	09-06-1988	Levanon	
	5.	US-4,872,091	10-03-1989	Maniwa et al.	
	6.	US-4,890,282	12-26-1989	Lambert et al.	
	7.	US-4,918,572	04-17-1990	Tarver et al.	
	8.	US-4,939,735	07-03-1990	Fredericks et al.	
	9.	US-5,056,141	10-08-1991	Dyke	
	10.	US-5,086,499	02-04-1992	Mutone	
	11.	US-5,251,097	10-05-1993	Simmons et al.	
	12.	US-5,278,509	01-11-1994	Haynes et al.	
	13.	US-5,278,730	01-11-1994	Kikinis	
	14.	US-5,293,497	03-08-1994	Free	
	15.	US-5,311,397	05-10-1994	Harshberger et al.	
	16.	US-5,317,477	05-31-1994	Gillett	
	17.	US-5,319,771	06-07-1994	Takeda	
	18.	US-5,331,509	07-19-1994	Kikinis	
	19.	US-5,355,391	10-11-1994	Horowitz et al.	
	20.	US-5,428,806	06-27-1995	Pocrass	
	21.	US-5,436,857	07-25-1995	Nelson et al.	
	22.	US-5,463,742	10-31-1995	Kobayashi	
	23.	US-5,539,616	07-23-1996	Kikinis	
	24.	US-5,550,710	08-27-1996	Rahamim et al.	
	25.	US-5,550,861	08-27-1996	Chan et al.	
	26.	US-5,578,940	11-26-1996	Dillon	
	27.	US-5,600,800	02-04-1997	Kikinis et al.	
	28.	US-5,603,044	02-11-1997	Annapareddy et al.	
	29.	US-5,606,717	02-25-1997	Farmwald et al.	
	30.	US-5,608,608	03-04-1997	Flint et al.	
	31.	US-5,630,057	05-13-1997	Hait	
	32.	US-5,638,521	06-10-1997	Buchala et al.	
	33.	US-5,640,302	06-17-1997	Kikinis	
	34.	US-5,659,773	08-19-1997	Huynh et al.	
	35.	US-5,663,661	09-02-1997	Dillon et al.	
	36.	US-5,673,174	09-30-1997	Hamirani	
	37.	US-5,680,126	10-21-1997	Kikinis	
	38.	US-5,689,654	11-18-1997	Kikinis	
	39.	US-5,774,704	06-30-1998	Williams	
	40.	US-5,721,837	02-24-1998	Kikinis	
	41.	US-5,721,842	02-24-1998	Beasley et al.	
	42.	US-5,745,733	04-28-1998	Robinson	
	43.	US-5,752,080	05-12-1998	Ryan	
	44.	US-5,764,924	06-09-1998	Hong	
	45.	US-5,795,228	08-18-1998	Trumbull	
	46.	US-5,809,538	09-15-1998	Pollmann	
	47.	US-5,815,681	09-29-1998	Kikinis	
	48.	US-5,819,050	10-06-1998	Boehling et al.	
	49.	US-5,826,048	10-20-1998	Dempsey et al.	
	50.	US-5,848,249	12-08-1998	Garbus	
	51.	US-5,859,669	01-12-1999	Prentice	

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PTO/SB/08A (07-05)
Approved for use through 07/31/2006. OMB 0651-0031

Substitute for form 1449A/PTO		*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Application Number	12/504,534
		Filing Date	July 16, 2009
		First Named Inventor	William W.Y. Chu
(use as many sheets as necessary)		Group Art Unit	2111
		Examiner Name	Unassigned
Sheet	2 of 6	Attorney Docket No.	ACQI-010/10US 310578-2052

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	52.	US-5,907,566	05-25-1999	Benson et al.	
	53.	US-5,941,965	08-24-1999	Moroz	
	54.	US-5,948,047	09-07-1999	Jenkins et al.	
	55.	US-5,960,213	08-28-1999	Wilson	
	56.	US-5,968,144	10-19-1999	Walker et al.	
	57.	US-5,971,804	10-26-1999	Gallagher et al.	
	58.	US-5,977,989	11-02-1999	Lee et al.	
	59.	US-5,982,363	11-09-1999	Naift	
	60.	US-5,991,163	11-23-1999	Marconi et al.	
	61.	US-5,991,844	12-23-1999	Khosrowpour	
	62.	US-5,999,952	12-07-1999	Jenkins et al.	
	63.	US-6,002,442	12-14-1999	Li et al.	
	64.	US-6,003,105	12-14-1999	Vicard et al.	
	65.	US-6,011,546	01-04-2000	Bertram	
	66.	US-6,016,252	01-18-2000	Pignolet et al.	
	67.	US-6,028,643	02-22-2000	Jordan et al.	
	68.	US-6,029,183	02-22-2000	Jenkins et al.	
	69.	US-6,038,621	03-14-2000	Gale et al.	
	70.	US-6,040,792	03-21-2000	Watson et al.	
	71.	US-6,052,513	04-18-2000	McLaren	
	72.	US-6,069,615	05-30-2000	Abraham et al.	
	73.	US-6,088,224	07-11-2000	Gallagher et al.	
	74.	US-6,088,752	07-11-2000	Ahern	
	75.	US-6,157,534	12-05-2000	Gallagher et al.	
	76.	US-6,163,464	12-19-2000	Ishibashi et al.	
	77.	US-6,175,490	01-16-2001	Papa et al.	
	78.	US-6,202,169	03-13-2001	Razzaghe-Ashrafi et al.	
	79.	US-6,208,522	03-27-2001	Manweiler et al.	
	80.	US-6,216,185	04-10-2001	Chu	
	81.	US-6,260,155	07-10-2001	Dellacona	
	82.	US-6,289,376	09-11-2001	Taylor et al.	
	83.	US-6,304,895	10-16-2001	Schneider et al.	
	84.	US-6,311,268	10-30-2001	Chu	
	85.	US-6,314,522	11-06-2001	Chu et al.	
	86.	US-6,317,329	11-13-2001	Dowdy et al.	
	87.	US-6,321,335	11-20-2001	Chu	
	88.	US-6,332,180	12-18-2001	Kauffman et al.	
	89.	US-6,345,330	02-05-2002	Chu	
	90.	US-6,366,951	04-02-2002	Schmidt	
	91.	US-6,378,009	04-23-2002	Pinkston, II et al.	
	92.	US-6,381,602	04-30-2002	Shoroff et al.	
	93.	US-6,393,561	05-21-2002	Hagiwara et al.	
	94.	US-6,401,124	06-04-2002	Yang et al.	
	95.	US-6,425,033	07-23-2002	Conway et al.	
	96.	US-6,452,789	09-17-2002	Pallotti et al.	
	97.	US-6,452,790	09-17-2002	Chu et al.	
	98.	US-6,453,344	09-17-2002	Ellsworth	
	99.	US-6,496,361	12-17-2003	Kim et al.	
	100.	US-6,549,966	04-15-2003	Dickens et al.	
	101.	US-6,564,274	05-13-2003	Heath et al.	

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PTO/SB/08A (07-05)
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Substitute for form 1449A/PTO		*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Application Number	12/504,534
		Filing Date	July 16, 2009
		First Named Inventor	William W.Y. Chu
		Group Art Unit	2111
(use as many sheets as necessary)		Examiner Name	Unassigned
Sheet	3 of 6	Attorney Docket No.	ACQI-010/10US 310578-2052

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	102.	US-6,643,777	11-04-2003	Chu	
	103.	US-6,718,415	04-06-2004	Chu	
	104.	US-6,725,317	04-20-2004	Bouchier et al.	
	105.	US-6,324,605 B1	11-27-2001	Rafferty et al.	
	106.	US-2009/0157939	06/18/2009	Chu	
	107.	US-5,978,919	11-1999	Doi et al.	
	108.	US-6,009,488	12-28-1999	Kavipurapu	
	109.	US-6,025,989	02-15-2000	Ayd et al.	
	110.	US-6,070,214	05-30-2000	Ahern	
	111.	US-7,099,981 B2	08-29-2006	Chu	
	112.	US-7,416,446 B2	12-05-2006	Chu	
	113.	US-7,328,297 B2	02-05-2008	Chu	
	114.	US-7,363,415 B2	04-22-2008	Chu	
	115.	US-7,363,416 B2	04-22-2008	Chu	
	116.	US-7,376,779 B2	05-20-2008	Chu	
	117.	US-6,161,524	12-19-2000	Akbarian et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	1.	WO 92/18924	10-29-1992			
	2.	WO 94/00097	01-06-1994			
	3.	WO 95/13640	05-18-1995			
	4.	EP 722138A1	07-17-1996			
	5.	JP 6-289953	10-18-1994			

OTHER – NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[6]
	1.	Agerwala, T. et al., "SP2 System Architecture", IBM Systems Journal, Vol. 34, No. 2 (1995)	
	2.	Bernal, Carlos, product brochure entitled: "PowerSMP Series 4000", (March 1998) <<http://www/winnetmag.com/Windows/Article/ArticleID/3095//3095.html, downloaded from web on June 22, 2004, 2 pgs.	
	3.	Cragle, Jonathan, "Density System 1100", (May 1999) <<http://www.winnetmag.com/Windows/Article/ArtideID/5199/5199.html>>, downloaded from web on June 21, 2004, 4 pgs.	
	4.	Feldman, Jonathan, "Rack Steady: The Four Rack-Mounted Servers That Rocked Our Network", <<http://www.networkcomputing.com/shared/printArtide.jhtml?article=/910/910r3sidel .htm...>> June 23, 2004, 3 pgs.	
	5.	Fetters, Dave, "Cubix High-Density Server Leads the Way With Standout Management Software", (February 8. 1999) <<http://www. nwc. com/shared/printArticle.jhtml?article=/1003/1003r3full.html&pub=nwc>>, downloaded from web on June 23, 2004, 5 pgs.	
	6.	Gardner, Michael and Null, Christopher, "A Server Condominium", <<http://www.lantimes.com/testing/98jun/806a042a.html>>, June 23, 2004, 3 pgs.	
	7.	Harrison, Dave, "VME in the Military: The M1A2 Main Battle Tank Upgrade Relies on COTS VME"	

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Approved for use through 07/31/2006. OMB 0651-0031

Substitute for form 1449A/PTO		*Complete if Known*	
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		Filing Date	July 16, 2009
		First Named Inventor	William W.Y. Chu
		Group Art Unit	2111
(use as many sheets as necessary)		Examiner Name	Unassigned
Sheet	4 of 6	Attorney Docket No.	ACQI-010/10US 310578-2052

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Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[6]
		<<http://www.dv4.com>>, (February 9, 1998), pgs. 1-34.	
	8.	Williams, Dennis, "Consolidated Servers", (February 17, 1997) <<http://www.lantimes.com/testing/97compare/pcconsol.html>> downloaded from web on June 23, 2004, 2 pgs.	
	9.	Williams, Dennis, "Executive Summary: Consolidate Now", (February 17, 1997) <<http://www.lantimes.com/testing/97feb/702b064a.html>> downloaded from web on June 23, 2004, 2 pgs.	
	10.	Williams, Dennis, "Top "Scores for Useability and Openness", (February 17, 1997) <<http://www.lantimes.com/testing/97feb/702b064a.html>> downloaded from web on June 23, 2004, 2 pgs.	
	11.	Williams, Dennis, "ChatCom Inc. Chatterbox", (February 17, 1997) <<http://www.lantimes.com/testing/97feb/702b066a.html>> downloaded from web on June 23, 2004, 3 pgs.	
	12.	Williams, Dennis, "EVERSYS Corp. System 8000", (February 17, 1997) <<http://www.lantimes.com/testing/97feb/702b070b.html>> downloaded from web on June 22, 2004, 4 pgs.	
	13.	Williams, Dennis, "Cubix Corp. ERS/FT II", (February 17, 1997) <<http://www.lantimes.com/testing/97feb/702b068b.html>> downloaded from web on June 23, 2004, 4 pgs.	
	14.	Crystal Advertisement for "Rackmount Computers", (©2000-2004) <<http://www.crystalpc.com/products/roservers.asp>>, downloaded from web on June 17, 2004, 8 pgs.	
	15.	Crystal Advertisement for "QuickConnect® Cable Management", (©2000-2004) <<http://www.crystalpc.com/products/quickconnect.asp>> downloaded from web on June 17, 2004, 4 pgs.	
	16.	Cubix Product Brochure entitled, "Density System", (©2000) <<http://64.173.211.7/support/techinfo/system/density/densityl0.htm>> downloaded from web on June 22, 2004, 3 pgs.	
	17.	Cubix Product Brochure entitled, "Density System, Technical Specifications", (©2000) <<http://64.173.211.7/support/techinfo/system/density/info/spec.htm>> downloaded from web on June 22, 2004, 2 pgs.	
	18.	Cubix Product Manual entitled, "Density System", Chapter 1-Introduction, (©2000) <<http://64.173.211.7/support/techinfo/manuals/density/Chap-1.htm>> downloaded from web on June 22, 2004, 5 pgs.	
	19.	Cubix, "Click on the front panel that matches your system", (©2000) <<http://64.173.211.7/support/techinfo/system/density/densiry.htm>>, downloaded from web on June 22, 2004, 1 pg.	
	20.	Cubix Product Manual entitled, "Density System", Chapter 2-Installation, (©2000) <<http://64.173.211.7/support/techinfo/manuals/density/Chap-2.htm>> downloaded from web on June 22, 2004, 9 pgs.	
	21.	Cubix Product Manual entitled, "Density System", Chapter 3-Operation, (©2000) <<http://64.173.211.7/support/techinfo/manuals/density/Chap-3.htm>> downloaded from web on June 22, 2004, 4 pgs.	
	22.	Cubix Product Manual entitled, "Density System", Chapter 4-Maintenance and Repair, (©2000) <<http://64.173.211.7/support/techinfo/manuals/density/Chap-4.htm>> downloaded from web on June 22, 2004, 5 pgs.	
	23.	Cubix, "What are Groups?", (©2000) <<http://64.173.211.7/support/techinfo/system/density/info/groups.htm>>, downloaded from web on June 22, 2004, 3 pgs.	
	24.	Cubix, "SP 5200XS Series Plug-in Computers", (©2000) <<http://64.173.211.7/support/techinfo/bc/sp5200xs/intro.htm>>, downloaded from web on June 22, 2004, 2 pgs.	
	25.	Cubix, "SP 5200XS Series Technical Specifications", (©2000) <<http://64.173.211.7/support/techinfo/bc/sp5200xs/spec.htm>>, downloaded from web on June 22, 2004, 2 pgs.	

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Substitute for form 1449A/PTO		*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Application Number	12/504,534
		Filing Date	July 16, 2009
		First Named Inventor	William W.Y. Chu
		Group Art Unit	2111
(*use as many sheets as necessary*)		Examiner Name	Unassigned
Sheet	5 of 6	Attorney Docket No.	ACQI-010/10US 310578-2052

OTHER – NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[6]
	26.	Cubix, "SP 5200 Series" Chapter 1-Introduction, (©2000) <<http://64.173.211.7/support/techinfo/manuals/sp5200/chap-1.htm>>, downloaded from web on June 22, 2004, 3 pgs.	
	27.	Cubix, "SP 5200 Series" Chapter 2-Switches & Jumpers, (©2000) <<http://64.173.211.7/support/techinfo/manuals/sp5200/chap-2.htm>>, downloaded from web on June 22, 2004, 3 pgs.	
	28.	Cubix, "SP 5200 Series" Chapter 3-Installation, (©2000) <<http//64.173.211.7/support/techinfo/manuals/sp5200/chap-3.htm>>, downloaded from web on June 22, 2004, 4 pgs.	
	29.	Cubix, "SP 5200 Series" Chapter 4-Technical Reference, (©2000) <<http://64.173.211.7/support/techinfo/manuals/sp5200/chap-4.htm>>, downloaded from web on June 22, 2004, 3 pgs.	
	30.	Cubix, "DP 6200 'D' Series Plug-in Computers" <<http://64.173.211.7/support/techinfo/bc/dp/6200d/intro.htm">>, downloaded from web on June 22, 2004, 3 pgs.	
	31.	Cubix, "Installing DP or SP Series Boards" (©2000) <<http://64.173.211.7/support/techinfo/bc/dp/6200d/intro.htm">>, downloaded from web on June 22, 2004, 2 pgs.	
	32.	Cubix, "Powering On/Off or Resetting Plug-in Computers in an Density System", (©2000) <<http://64.173.211.7/support/techinfo/system/density/info/power.htm>>, downloaded from web on June 22, 2004, 2 pgs.	
	33.	Cubix, "Multiplexing Video, Keyboard & Mouse with Multiple Density Systems", (©2000) <<http://64.173.211.7/support/techinfo/system/density/info/vkm-mux.htm>>, downloaded from web on June 22, 2004, 2 pgs.	
	34.	eBay Advertisement for "Total IT Group Network Engines", <<http://cgi.ebay.com/ws/eBayISAPI.dll?ViewItem&item=5706388046&sspagename=STRK%3AMDBI%3AMEBI3AIT&rd=1>>, (downloaded from web on June 25, 200), 1 pg.	
	35.	"Features Chart", (February 1, 1997) <<http://www.lantimes.com/testing/97feb/702b072a.html>>, (downloaded from web on June 23, 2004), 3 pgs.	
	36.	Internet Telephone Roundup, "Industrial Computers", <<http://www.tmcnet.com/articles/itmag/0499/0499roundup.htm>>, (downloaded from web on June 23, 2004), 5 pgs.	
	37.	Press Release: Hiawatha, Iowa, (March 1, 1997) entitled "Crystal Group Products Offer Industrial PC's with Built-in Flexibility", <<http://www.crystalpc.com/news/pressreleases/prodpr.asp>>, (downloaded from web on May 14, 2004), 2 pgs.	
	38.	Press Release: Kanata, Ontario, Canada, (April 1998) entitled "Enhanced COTS SBC from DY 4 Systems features 166MHz Pentium™ Processor" <<http://www.realtime-info.be/VPR/layout/display/pr.asp?/pr.asp?PRID=363>>, 2 pgs.	
	39.	Product Brochure entitled "SVME/DM-192 Pentium®II Single Board Computer" (June 1999) pgs. 1-9.	
	40.	Product Brochure entitled "System 8000", <<http://www.bomara.com/Eversys/briefDefault.htm>>, (downloaded from web on June 22, 2004), 4 pgs.	
	41.	Product Brochure entitled: "ERS/FT II System", (©2000) <<http://64.173.211.7/support/techinfo/system/ersft2/ersft2.htm>>, downloaded from web on June 22, 2004, 4 pgs.	
	42.	Product Manual entitled: "ERS II and ERS/ FT II", Chap. 3, System Components, <<http://64.173.211.7/support/techinfo/manuals/ers2/ers2-c3.htm>>, (downloaded from web on June 22, 2004), 21 pgs.	
	43.	Product Manual entitled: "ERS II and ERS/FT II", Chap. 6, Component Installation, <<http://64.173.211.7/support/techinfo/manuals/ers2/ers2-c6.htm>>, (downloaded from web on June 22, 2004), 18 pgs.	
	44.	Windows Magazine, "Cubix PowerSMP Series 4000", (Nov. 1997), <http://<www.techweb.com/winmag/library/1997/1101/ntent008.htm>> downloaded from the web on June 22, 2004, pg. NT07.	
	45.	CETIA Brochure "CETIA Powerengine CVME 603e" pp. 1-6 downloaded from the internet @ http://www.cetia.com/Products Addons/wp-47-01.pdf. on 2/15/2006.	

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Substitute for form 1449A/PTO **INFORMATION DISCLOSURE STATEMENT BY APPLICANT** (*use as many sheets as necessary*)		***Complete if Known***	
		Application Number	12/504,534
		Filing Date	July 16, 2009
		First Named Inventor	William W.Y. Chu
		Group Art Unit	2111
		Examiner Name	Unassigned
Sheet	6 of 6	Attorney Docket No.	ACQI-010/10US 310578-2052

OTHER – NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[6]
	46.	MPL Brochure, "The First Rugged All in One Industrial 486FDX-133 Mhz PC", (1998), pages 53.	
	47.	MPL Brochure "IPM 486 Brochure/IPM5 User Manual", pp. 1-9, downloaded from the internet @ http://www.mpl ch/DOCS./u48600xd.pdf on 2/15/2006.	
	48.	Synder, Joel, "Better Management Through Consolidation," (Aug. 18, 1997), pp. 1-6 downloaded from the internet @ http://www.opus1.com/www/jms/nw-con-0818rev.html.,	
	49.	Eversys Corporation, "Eversys System 8000 Consolidated Network Server Market and Product Overview," Slide presentation, downlaoded from <http://eversys.com>, (Product to be Released March 1, 2007), 20 pages.	
	50.	"SQL Server and NT Cluster Manager Availability Demo, "Microsoft Server Programmer Developers Conference, November 1996, 15 pages.	
	51.	Microsoft Cluster Service Center, MSCS Basics," downloaded from <<http://www.networks.com/mscsbasics.htm.., February 7, 2005, 6 pages.	
	52.	Complaint For Patent Infringement, Case 6:09-cv-00148, filed April 2, 2009.	
	53.	Answer to 2nd Amended and Counterclaims by Fujitsu America, Inc., Case 6:09-cv-00148-LED, dated August 10, 2009, 34 pages.	

Examiner Signature		Date Considered	

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This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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EFS ID:	6167960
Application Number:	12504534
International Application Number:	
Confirmation Number:	1286
Title of Invention:	MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNDIRECTIONAL SERIAL BIT CHANNELS
First Named Inventor/Applicant Name:	William W. Y. Chu
Customer Number:	58249
Filer:	Cliff Z. Liu/Donna Hengst
Filer Authorized By:	Cliff Z. Liu
Attorney Docket Number:	ACQI-010/10US 310578-2052
Receipt Date:	29-SEP-2009
Filing Date:	16-JUL-2009
Time Stamp:	16:04:55
Application Type:	Utility under 35 USC 111(a)

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1	Miscellaneous Incoming Letter	ACQI-010-10US-Letter.pdf	33976 e9e4a9ceed51756f973035db12d136d5ffa42d1f	no	1

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2	Drawings-only black and white line drawings	ACQI-010-10US-Drawings.pdf	736748 536166f71817289e46a117ee69f49a7abe645952	no	24
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3	Transmittal Letter	ACQI-010-10US-IDS-Letter.pdf	73496 56f0f24f40761284196ee8e97dff3d4d8c046063	no	2
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National Stage of an International Application under 35 U.S.C. 371

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Attorney Docket No. ACQI-010/10US 310578-2052 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:	CHU, William W. Y.	Confirmation No.:	1286
Serial No.:	12/504,534	Group Art Unit:	2111
Filed:	July 16, 2009	Examiner:	Unassigned

FOR: **MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNDIRECTIONAL SERIAL BIT CHANNELS**

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RESPONSE TO NOTICE TO FILE CORRECTED APPLICATION PAPERS

In response to the Notice to File Corrected Application Papers under 37 C.F.R. § 1.36(e) mailed July 30, 2009 enclosed are:

[**X**] (24) Sheets of Replacement Drawings, containing Figures 1 to 23.

The Commissioner is hereby authorized to charge any appropriate fees under 37 C.F.R. §§1.16, 1.17, and 1.21 that may be required by this paper, and to credit any overpayment, to Deposit Account No. 50-1283.

Dated: 9/29/2009

Respectfully submitted,
COOLEY GODWARD KRONISH LLP

By: _____
Cliff Z. Liu
Reg. No. 50,834

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ATTN: Patent Group
777 6th Street NW, Suite 1100
Washington, DC 20001
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Fax: (202) 842-7899

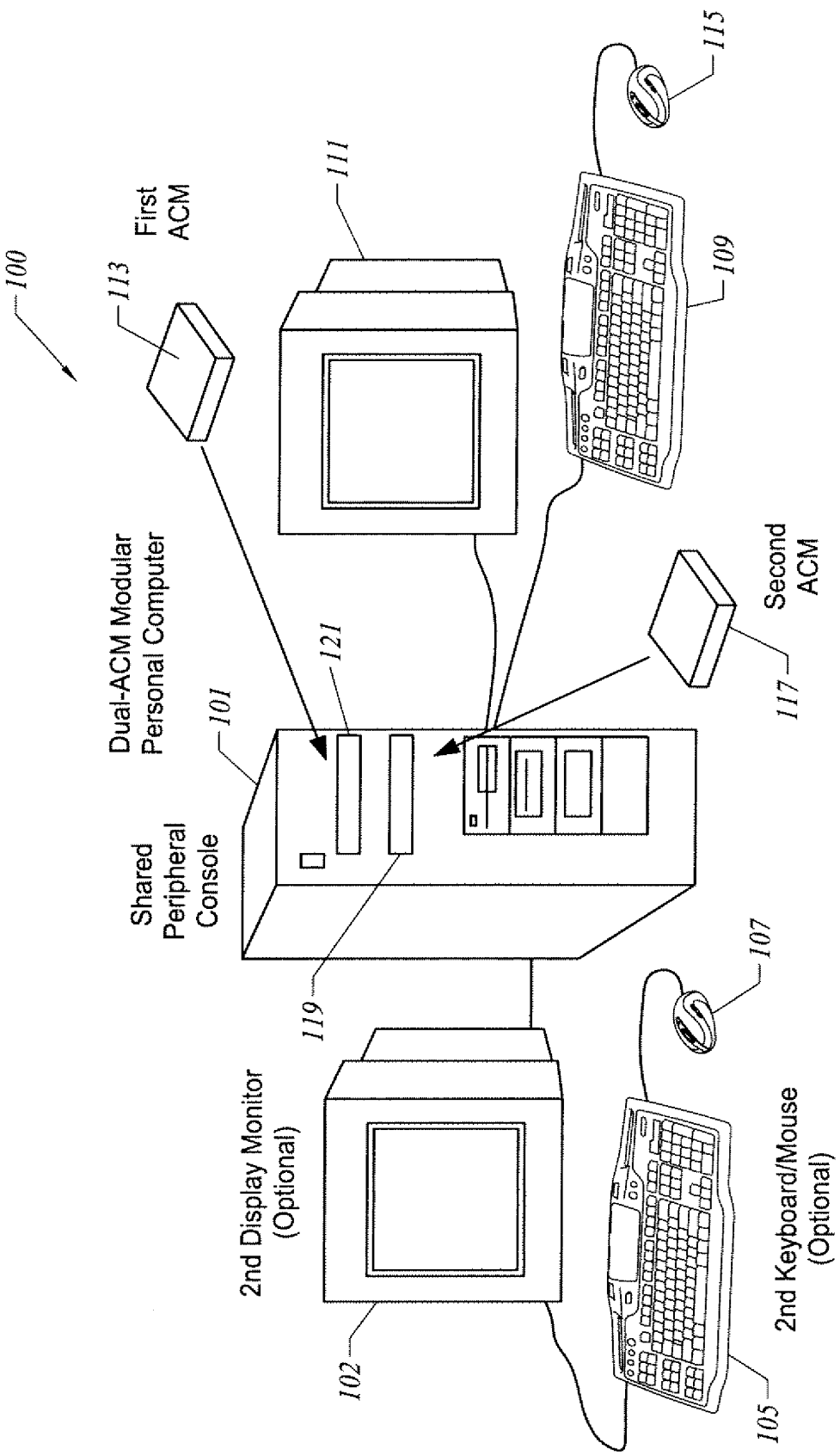

100
113
First ACM
111
115
109
Dual-ACM Modular Personal Computer
121
101
Second ACM
117
Shared Peripheral Console
119
107
2nd Display Monitor (Optional)
102
2nd Keyboard/Mouse (Optional)
105

FIGURE 1

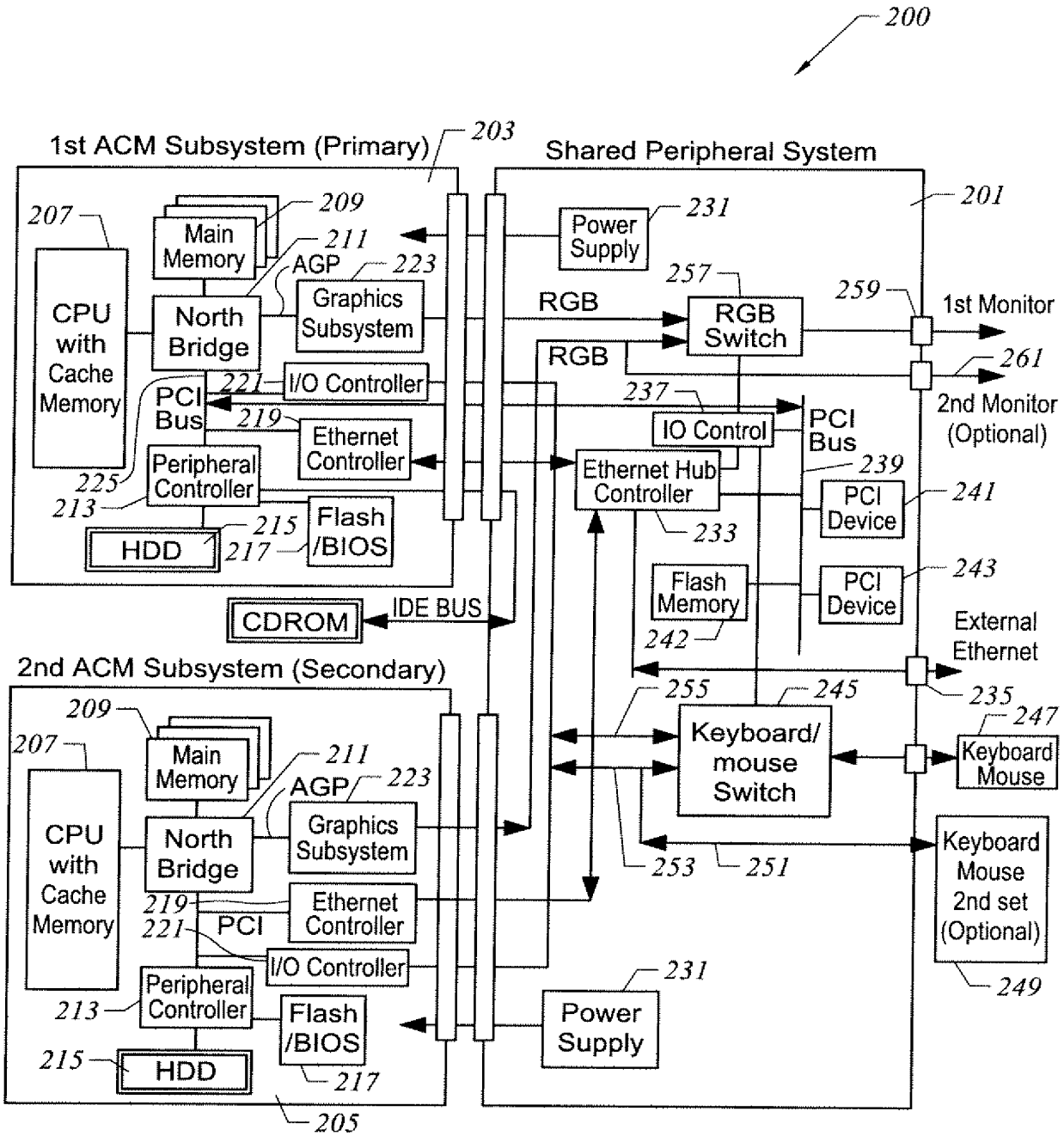

200
1st ACM Subsystem (Primary)
203
Shared Peripheral System
201
207
209
Main Memory
211
AGP
223
Graphics Subsystem
CPU with Cache Memory
North Bridge
221
I/O Controller
PCI Bus
219
Ethernet Controller
225
Peripheral Controller
213
215
HDD
217
Flash /BIOS
CDROM
IDE BUS
Power Supply
231
257
RGB
RGB Switch
259
1st Monitor
RGB
261
2nd Monitor (Optional)
237
IO Control
PCI Bus
239
Ethernet Hub Controller
233
PCI Device
241
Flash Memory
242
PCI Device
243
External Ethernet
235
255
245
247
Keyboard/ mouse Switch
Keyboard Mouse
253
251
Keyboard Mouse 2nd set (Optional)
249
2nd ACM Subsystem (Secondary)
209
207
Main Memory
211
AGP
223
Graphics Subsystem
CPU with Cache Memory
North Bridge
219
Ethernet Controller
221
PCI
I/O Controller
Peripheral Controller
213
Flash /BIOS
215
HDD
217
231
Power Supply
205

FIGURE 2

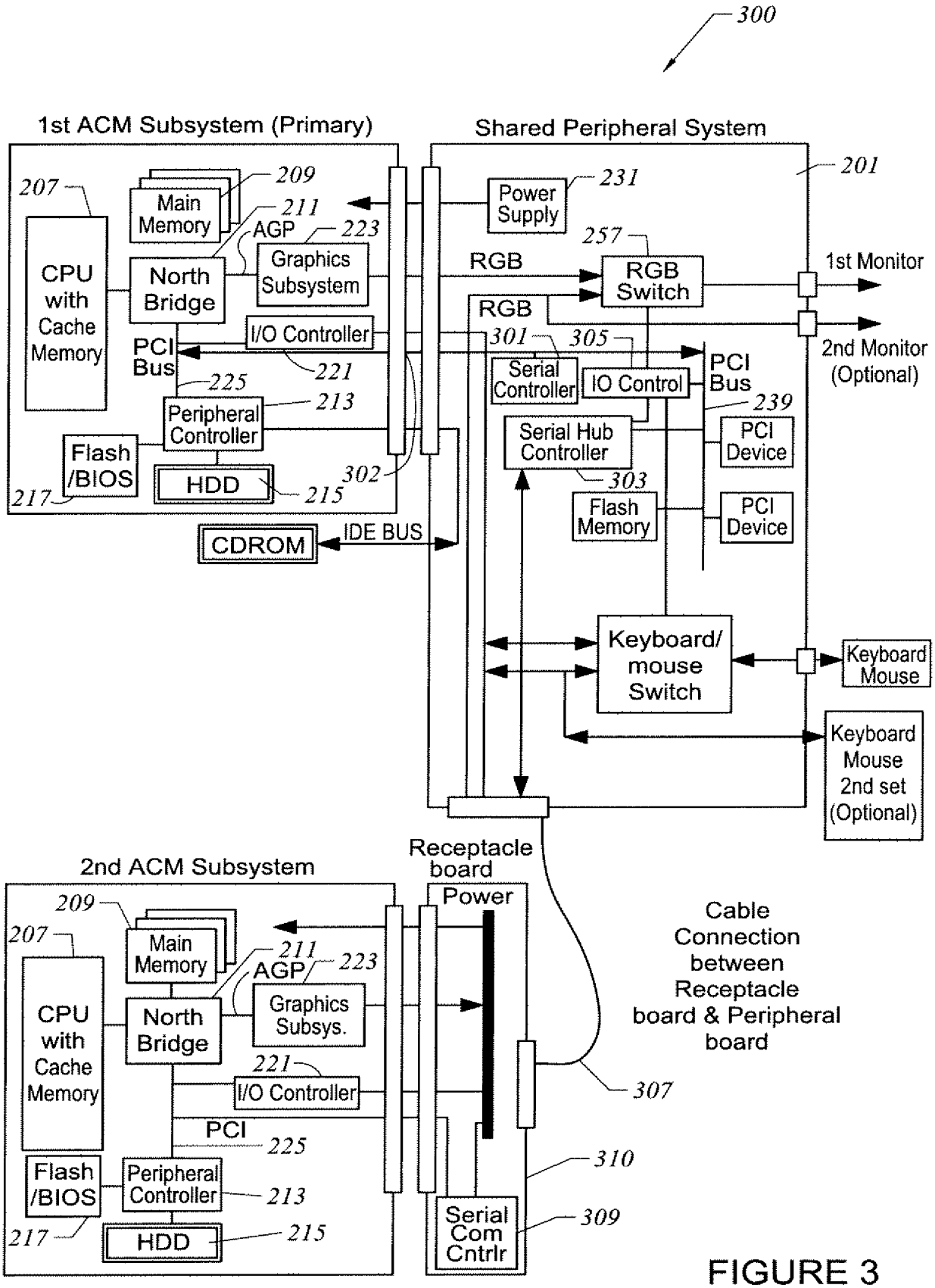

300
1st ACM Subsystem (Primary)
Shared Peripheral System
201
207
CPU with Cache Memory
Main Memory
209
211
AGP
223
Graphics Subsystem
North Bridge
I/O Controller
PCI Bus
225
221
Peripheral Controller
213
Flash /BIOS
217
HDD
215
302
CDROM
IDE BUS
Power Supply
231
257
RGB
RGB Switch
1st Monitor
RGB
2nd Monitor (Optional)
301
305
Serial Controller
IO Control
PCI Bus
239
Serial Hub Controller
303
PCI Device
Flash Memory
PCI Device
Keyboard/ mouse Switch
Keyboard Mouse
Keyboard Mouse 2nd set (Optional)
Receptacle board
Power
2nd ACM Subsystem
209
207
Main Memory
211
AGP
223
CPU with Cache Memory
North Bridge
Graphics Subsys.
221
I/O Controller
PCI
225
Flash /BIOS
Peripheral Controller
213
217
HDD
215
Cable Connection between Receptacle board & Peripheral board
307
310
Serial Com Cntrlr
309

FIGURE 3

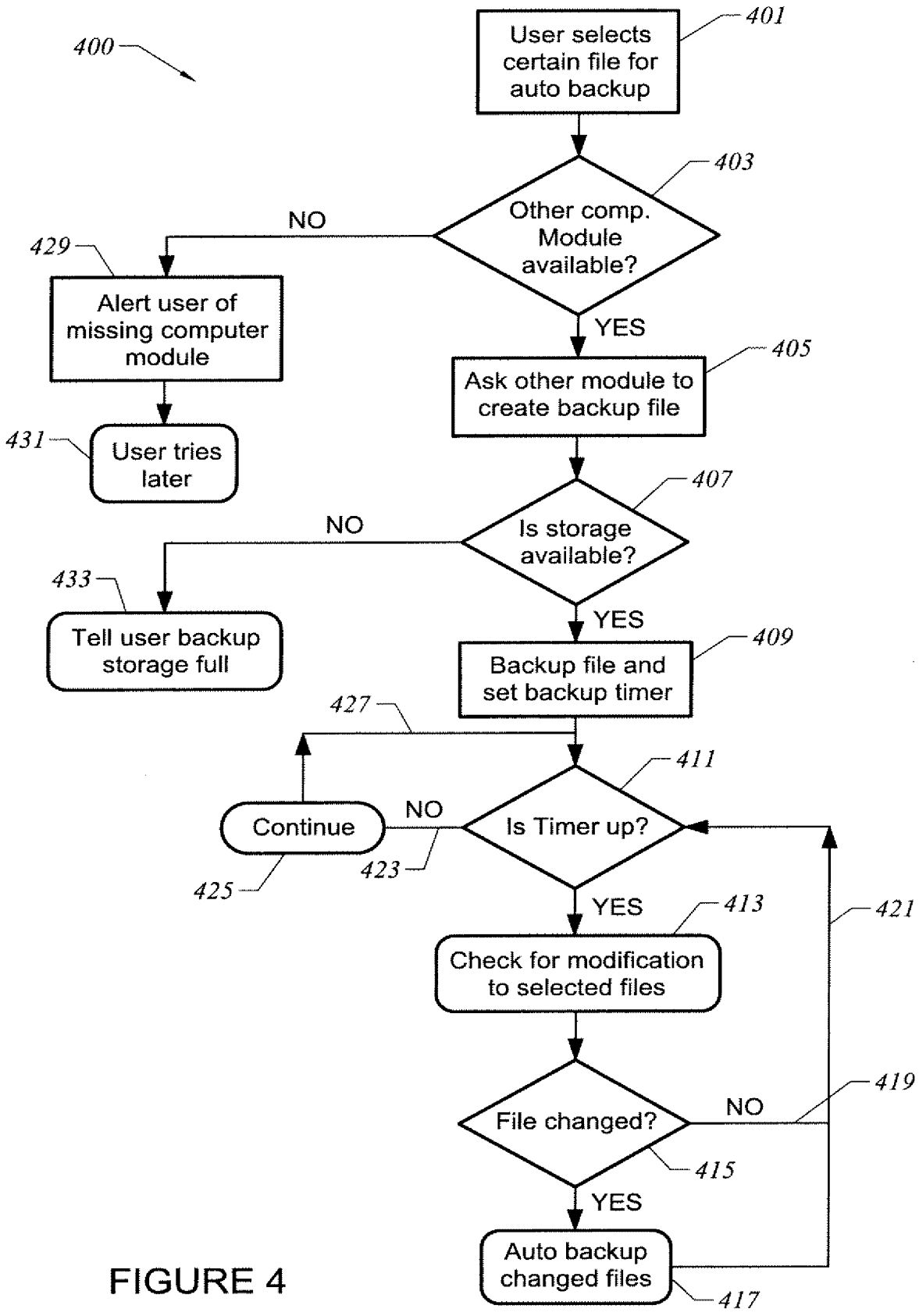

400
User selects certain file for auto backup
401
Other comp. Module available?
403
NO
YES
429
Alert user of missing computer module
431
User tries later
Ask other module to create backup file
405
Is storage available?
407
NO
YES
433
Tell user backup storage full
Backup file and set backup timer
409
427
411
Continue
NO
Is Timer up?
423
425
YES
413
421
Check for modification to selected files
File changed?
419
NO
415
YES
Auto backup changed files
417

FIGURE 4

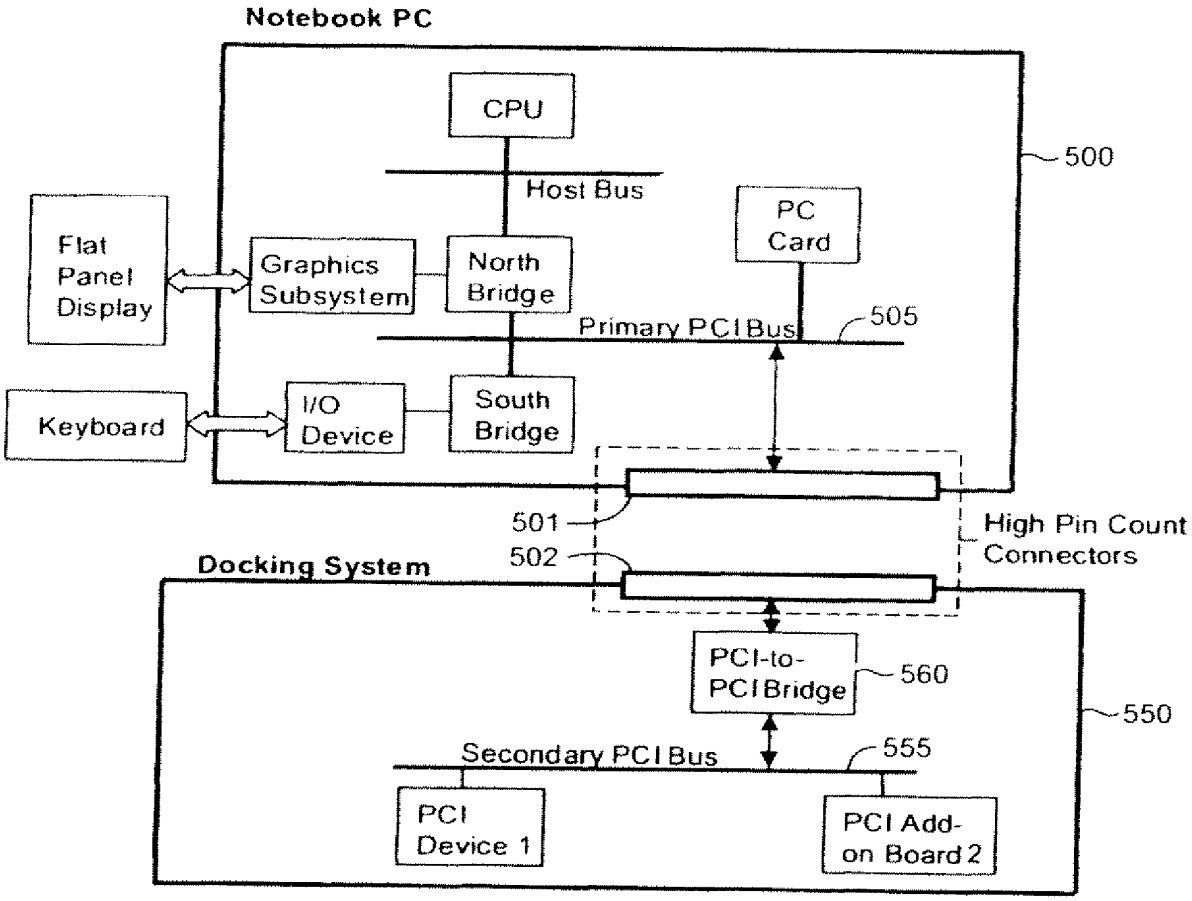

Notebook PC
CPU
Host Bus
500
PC Card
Flat Panel Display
Graphics Subsystem
North Bridge
Primary PCI Bus
505
Keyboard
I/O Device
South Bridge
501
High Pin Count Connectors
Docking System
502
PCI-to-PCI Bridge
560
550
Secondary PCI Bus
555
PCI Device 1
PCI Add-on Board 2

FIGURE 5

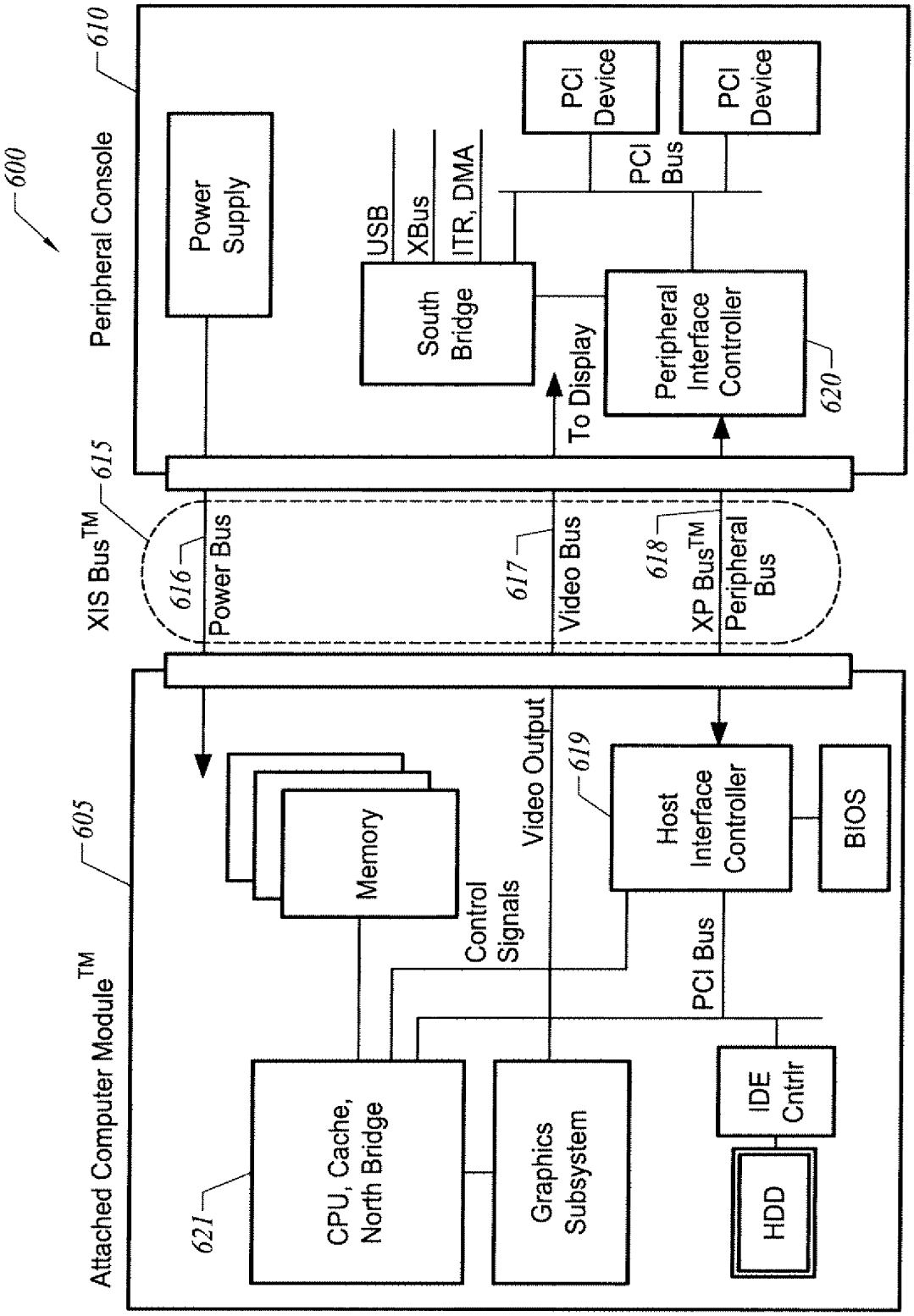

600
610
Peripheral Console
Power Supply
USB
XBus
ITR, DMA
South Bridge
PCI Device
PCI Device
PCI Bus
To Display
Peripheral Interface Controller
620
615
XIS Bus™
616
Power Bus
617
Video Bus
618
XP Bus™ Peripheral Bus
605
Attached Computer Module™
Memory
Control Signals
Video Output
619
Host Interface Controller
BIOS
PCI Bus
621
CPU, Cache, North Bridge
Graphics Subsystem
IDE Cntrlr
HDD

FIGURE 6

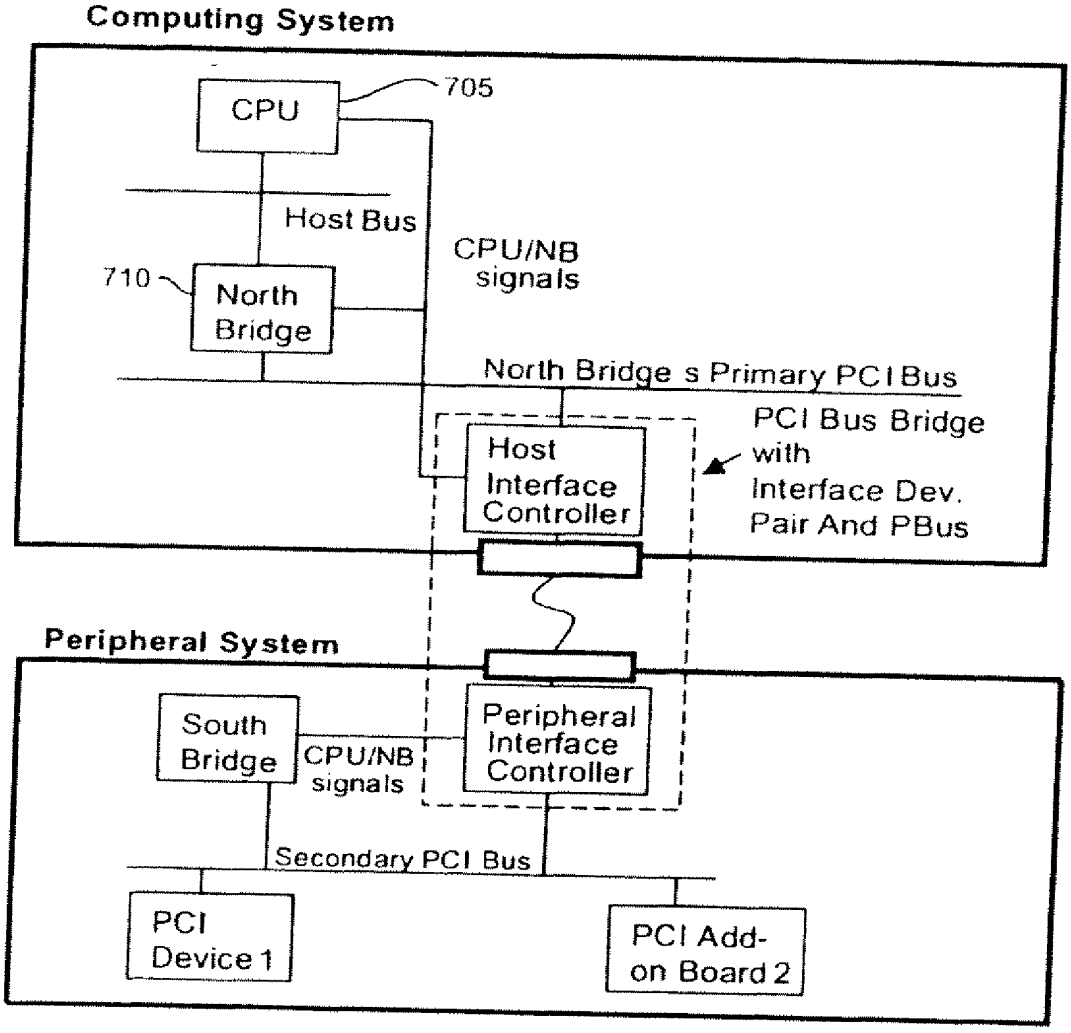

Computing System
CPU
705
Host Bus
CPU/NB
signals
710
North
Bridge
North Bridge s Primary PCI Bus
PCI Bus Bridge
with
Interface Dev.
Pair And PBus
Host
Interface
Controller
Peripheral System
South
Bridge
CPU/NB
signals
Peripheral
Interface
Controller
Secondary PCI Bus
PCI
Device 1
PCI Add-
on Board 2

FIGURE 7

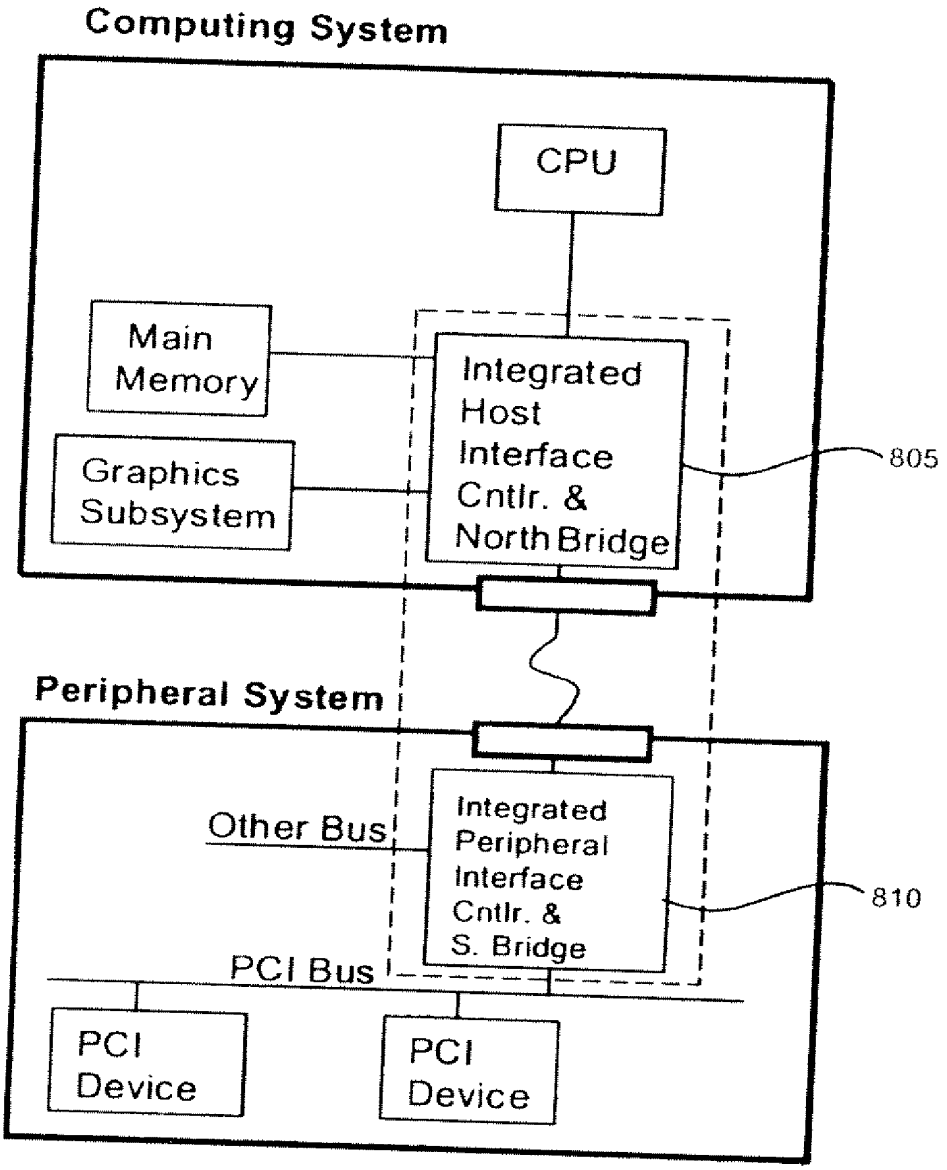

Computing System
CPU
Main Memory
Graphics Subsystem
Integrated Host Interface Cntlr. & North Bridge
805
Peripheral System
Other Bus
Integrated Peripheral Interface Cntlr. & S. Bridge
810
PCI Bus
PCI Device
PCI Device

FIGURE 8

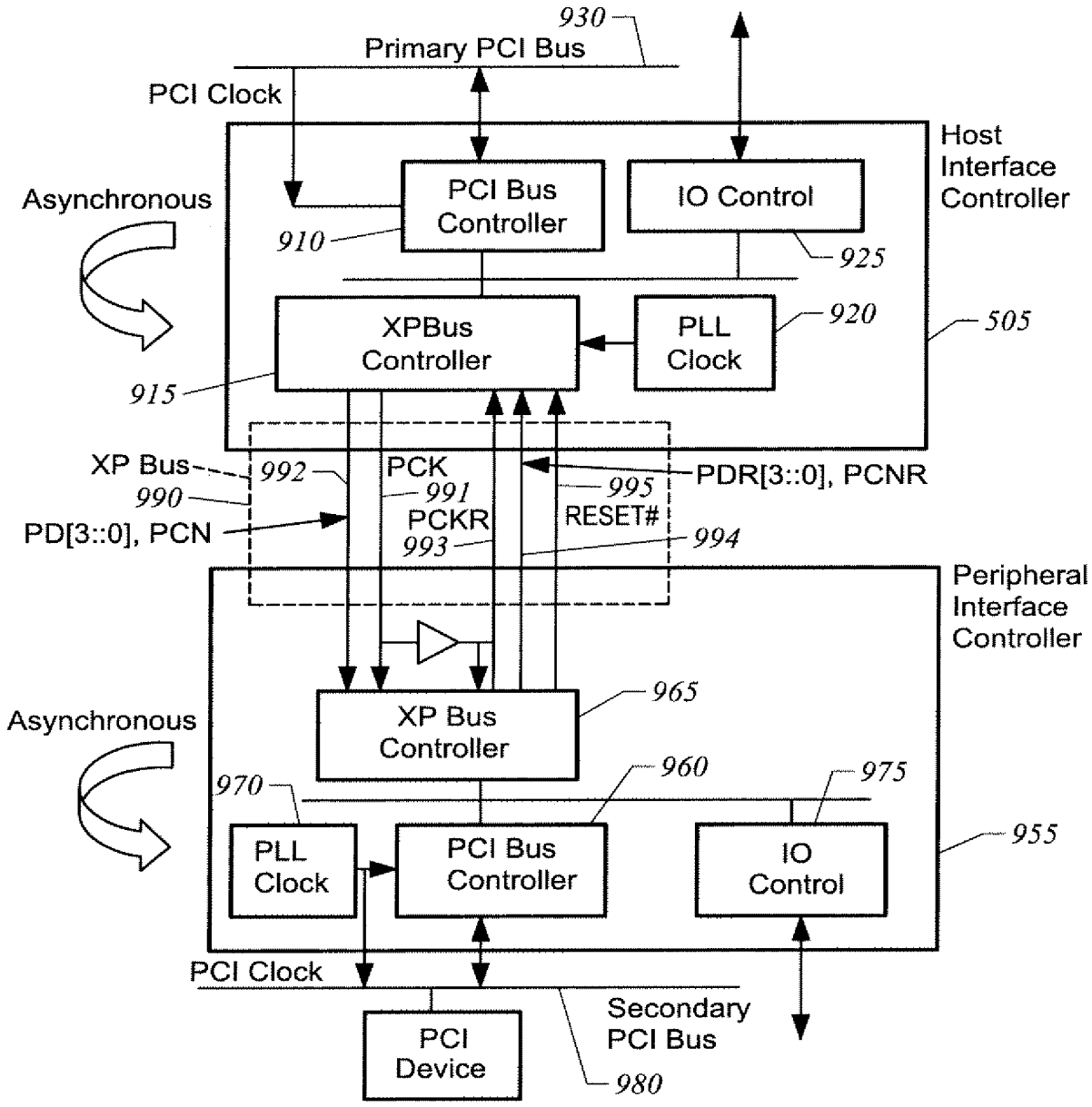

930
Primary PCI Bus
PCI Clock
Host
Interface
Controller
Asynchronous
PCI Bus
Controller
910
IO Control
925
XPBus
Controller
PLL
Clock
920
505
915
XP Bus
990
PD[3::0], PCN
992
PCK
991
PCKR
993
995
RESET#
PDR[3::0], PCNR
994
Peripheral
Interface
Controller
965
XP Bus
Controller
Asynchronous
970
960
975
PLL
Clock
PCI Bus
Controller
IO
Control
955
PCI Clock
Secondary
PCI Bus
PCI
Device
980

FIGURE 9

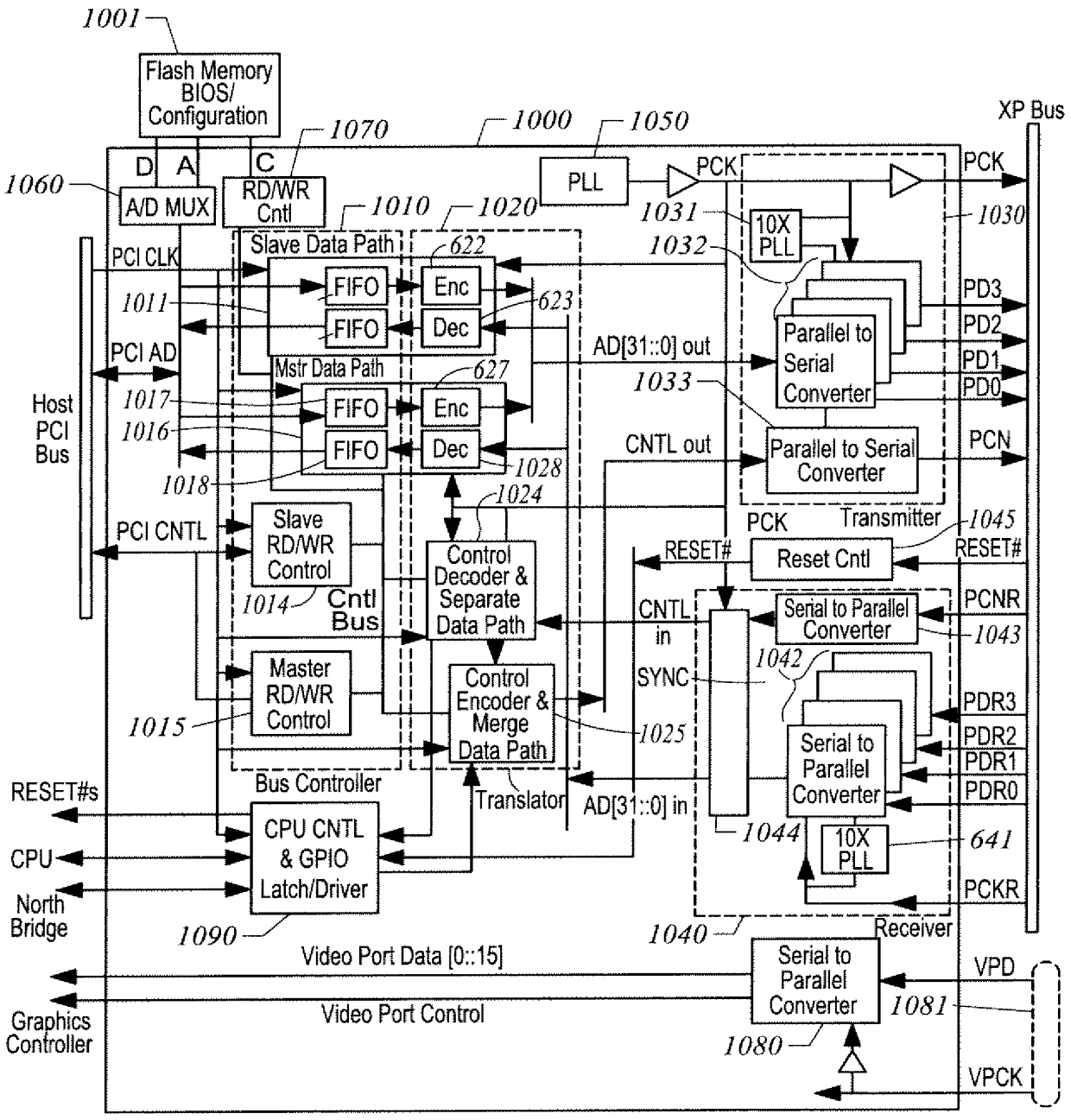

1001
Flash Memory BIOS/ Configuration
1070
1000
1050
XP Bus
D
A
C
1060
A/D MUX
RD/WR Cntl
1010
1020
PLL
PCK
PCK
1031
10X PLL
1030
Slave Data Path
622
1032
PCI CLK
FIFO
Enc
1011
623
FIFO
Dec
PD3
PD2
PCI AD
AD[31::0] out
Parallel to Serial Converter
PD1
Mstr Data Path
627
1033
PD0
Host PCI Bus
1017
FIFO
Enc
1016
FIFO
Dec
CNTL out
Parallel to Serial Converter
PCN
1028
1018
1024
PCK
Transmitter
1045
PCI CNTL
Slave RD/WR Control
Control Decoder & Separate Data Path
RESET#
Reset Cntl
RESET#
1014
Cntl Bus
CNTL in
Serial to Parallel Converter
PCNR
1043
1042
Master RD/WR Control
Control Encoder & Merge Data Path
SYNC
PDR3
1015
1025
Serial to Parallel Converter
PDR2
PDR1
Bus Controller
Translator
AD[31::0] in
PDR0
RESET#s
1044
10X PLL
641
CPU CNTL & GPIO Latch/Driver
CPU
PCKR
North Bridge
1090
1040
Receiver
Video Port Data [0::15]
Serial to Parallel Converter
VPD
Graphics Controller
Video Port Control
1081
1080
VPCK

FIGURE 10

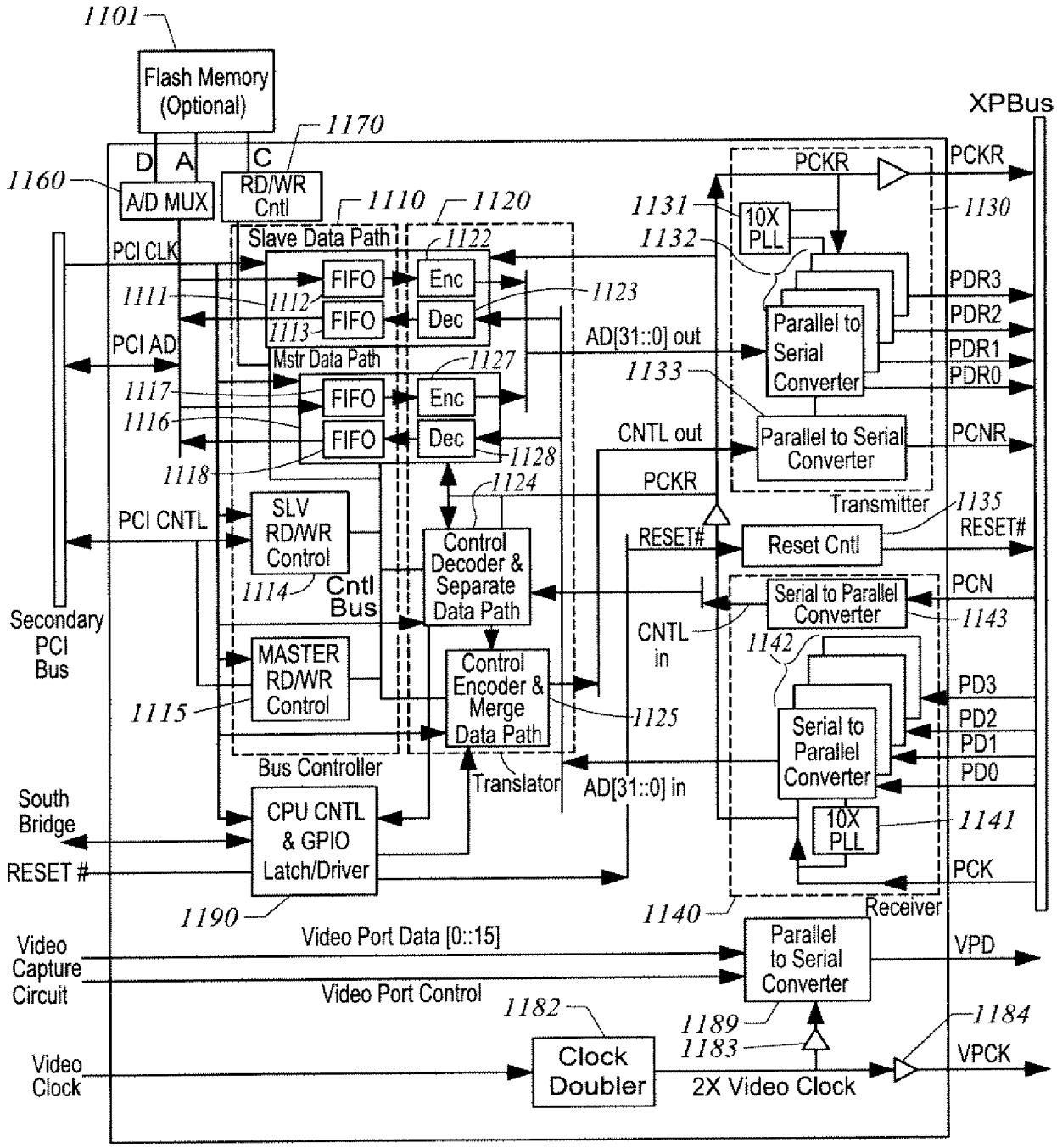
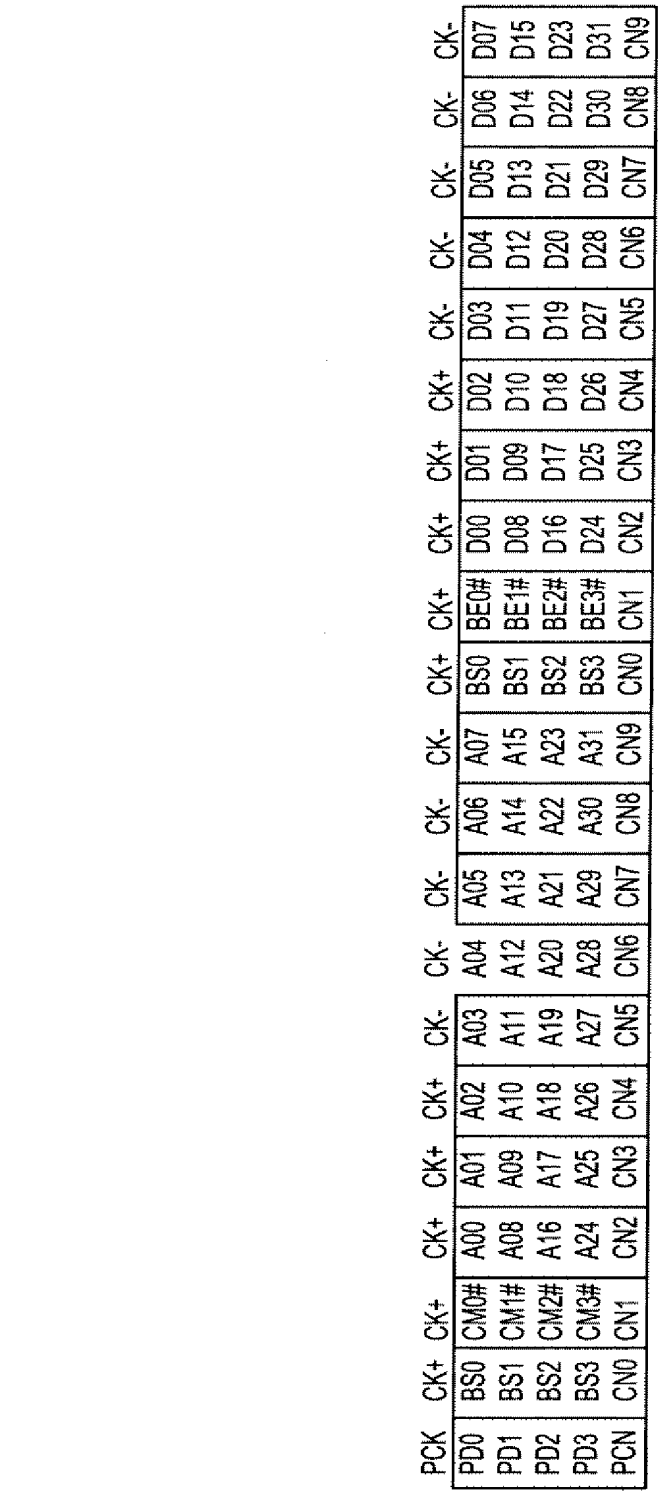

1101
Flash Memory (Optional)
XPBus
1170
D
A
C
1160
A/D MUX
RD/WR Cntl
1110
1120
Slave Data Path
1122
PCI CLK
FIFO
Enc
1111
1112
1123
FIFO
Dec
1113
PCI AD
Mstr Data Path
1127
1117
FIFO
Enc
1116
FIFO
Dec
1128
1118
1124
PCI CNTL
SLV RD/WR Control
1114
Cntl Bus
Control Decoder & Separate Data Path
Secondary PCI Bus
MASTER RD/WR Control
1115
Control Encoder & Merge Data Path
1125
Bus Controller
Translator
South Bridge
CPU CNTL & GPIO Latch/Driver
RESET #
1190
Video Capture Circuit
Video Port Data [0::15]
Video Port Control
Video Clock
1182
Clock Doubler
1189
1183
2X Video Clock
1184
VPCK
AD[31::0] out
AD[31::0] in
CNTL out
CNTL in
PCKR
RESET#
1131
10X PLL
1132
1130
PCKR
PDR3
PDR2
PDR1
PDR0
Parallel to Serial Converter
1133
PCNR
Parallel to Serial Converter
Transmitter
1135
RESET#
Reset Cntl
PCN
Serial to Parallel Converter
1143
1142
PD3
PD2
PD1
PD0
Serial to Parallel Converter
10X PLL
1141
PCK
Receiver
1140
Parallel to Serial Converter
VPD

FIGURE 11

	Symbol	Signal	Data Rate	Description
1	PD0 RTN			GND
2	PD0+	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 0+
3	PD0-			Computer to Peripheral LVDS Data 0-
4	PD1 RTN			GND
5	PD1+	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 1+
6	PD1-			Computer to Peripheral LVDS Data 1-
7	PD2 RTN			GND
8	PD2+	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 2+
9	PD2-			Computer to Peripheral LVDS Data 2-
10	PD3 RTN			GND
11	PD3+	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 3+
12	PD3-			Computer to Peripheral LVDS Data 3-
13	PCK RTN			GND
14	PCK+	Clock	Clock rate	Computer to Peripheral LVDS Clock +
15	PCK-			Computer to Peripheral LVDS Clock -
16	PCN RTN			GND
17	PCN+	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Control +
18	PCN-			Computer to Peripheral LVDS Control -
19	PDR0 RTN			GND
20	PDR0+	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 0+
21	PDR0-			Peripheral to Computer LVDS Data 0-
22	PDR1 RTN			GND
23	PDR1+	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 1+
24	PDR1-			Peripheral to Computer LVDS Data 1-
25	PDR2 RTN			GND
26	PDR2+	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 2+
27	PDR2-			Peripheral to Computer LVDS Data 2-
28	PDR3 RTN			GND
29	PDR3+	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 3+
30	PDR3-			Peripheral to Computer LVDS Data 3-
31	PCKR RTN			GND
32	PCKR+	Reverse Dir Clock	Clock rate	Peripheral to Computer LVDS Clock +
33	PCKR-			Peripheral to Computer LVDS Clock -
34	PCNR RTN			GND
35	PCNR+	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Control +
36	PCNR-			Peripheral to Computer LVDS Control -
37	RESET#		Asynchronous	Reset

FIGURE 12



PCK	CK+	CK+	CK+	CK+	CK+	CK-	CK-	CK-	CK-	CK+	CK+	CK+	CK+	CK+	CK-	CK-	CK-	CK-	CK-
PD0	BS0	CM0#	A00	A01	A02	A03	A04	A05	A06	A07	BS0	BE0#	D00	D01	D02	D03	D04	D05	D06	D07
PD1	BS1	CM1#	A08	A09	A10	A11	A12	A13	A14	A15	BS1	BE1#	D08	D09	D10	D11	D12	D13	D14	D15
PD2	BS2	CM2#	A16	A17	A18	A19	A20	A21	A22	A23	BS2	BE2#	D16	D17	D18	D19	D20	D21	D22	D23
PD3	BS3	CM3#	A24	A25	A26	A27	A28	A29	A30	A31	BS3	BE3#	D24	D25	D26	D27	D28	D29	D30	D31
PCN	CN0	CN1	CN2	CN3	CN4	CN5	CN6	CN7	CN8	CN9	CN0	CN1	CN2	CN3	CN4	CN5	CN6	CN7	CN8	CN9

FIGURE 13


PCK+
PCK-
PCK+
PCK-
BS0 C0# A00 A01 A02 A03 A04 A05 A06 A07 BS0
BS1 C1# A08 A09 A10 A11 A12 A13 A14 A15 BS1
BS2 C2# A16 A17 A18 A19 A20 A21 A22 A23 BS2
BS3 C3# A24 A25 A26 A27 A28 A29 A30 A31 BS3
0 CN0 CN1 CN2 CN3 CN4 CN5 CN6 CN7 CN8 1 CN9 CN10 CN11 CN12 CN13 CN14 CN15 CN16 CN17
PCK+
PCK-
PCK+
PCK-
BS0 BE0# D00 D01 D02 D03 D04 D05 D06 D07 BS0
BS1 BE1# D08 D09 D10 D11 D12 D13 D14 D15 BS1
BS2 BE2# D16 D17 D18 D19 D20 D21 D22 D23 BS2
BS3 BE3# D24 D25 D26 D27 D28 D29 D30 D31 BS3
0 CN0 CN1 CN2 CN3 CN4 CN5 CN6 CN7 CN8 1 CN9 CN10 CN11 CN12 CN13 CN14 CN15 CN16 CN17

FIGURE 14

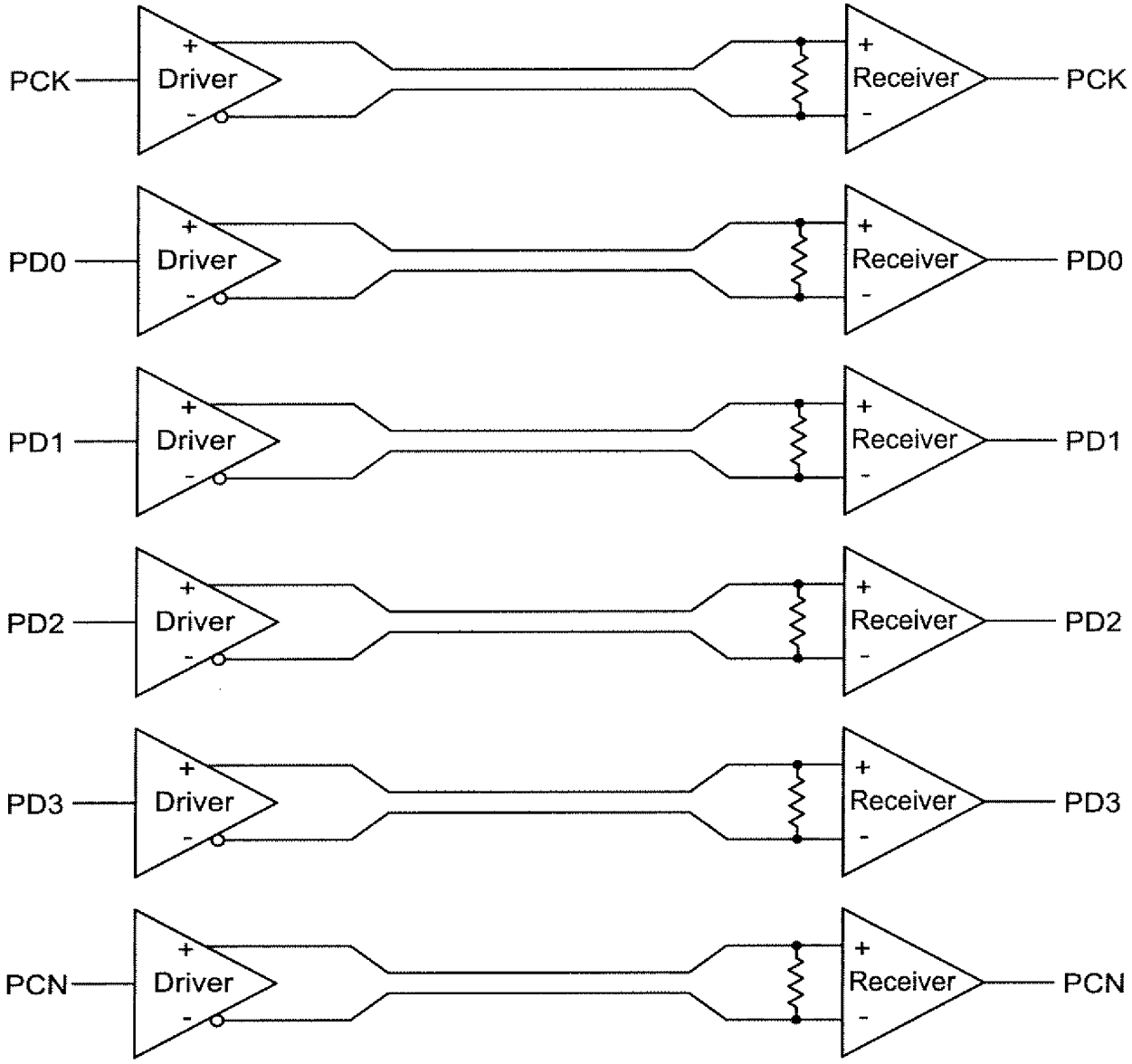

PCK
Driver
+
-
Receiver
PCK
PD0
Driver
Receiver
PD0
PD1
Driver
Receiver
PD1
PD2
Driver
Receiver
PD2
PD3
Driver
Receiver
PD3
PCN
Driver
Receiver
PCN

FIGURE 15

Name	Type	Pins	Description
AD[31::0]	TS	32	Multiplexed Address/Data. AD is driven to a valid state when GNT# is asserted.
C/BE[3::0]#	TS	4	Multiplexed Command/Byte Enables. For a two-address transaction, 1st address phase carries the command, and the 2nd address phase carries the transaction type C/BE is driven to a valid state when GNT# is asserted.
FRAME#	STS	1	Indicates beginning and duration of a PCI transaction. When the bus is idle. FRAME# is driven to High for 1 cycle. A pull-up resistor sustains STS signal.
IRDY#	STS	1	Initiator Ready. IRDY# is driven High for 1 cycle if bus is idle, and the state is sustained by a pull-up resistor.
TRDY#	STS	1	Target Ready. When bus is idle, TRDY# is driven High for 1 cycle if bus is idle. An external pull-up resistor sustains STS signal.
DEVSEL#	STS	1	Device Select. DEVSEL# is asserted by target to indicate it is ready to accept the transaction. HIC decodes address of a transaction to decide the need to assert DEVSEL#. As an initiator, HIC waits for 5 cycles to detect assertion of DEVSEL# by the target; otherwise HIC terminates with a master abort. DEVSEL# is driven High for 1 cycle when bus is idle, and the state is sustained by a pull-up resistor.
STOP#	STS	1	Target request to stop transaction. There are 3 cases: STOP#, TRDY# & DEVSEL# asserted: disconnect with data transfer Only STOP# & DEVSEL# asserted: request initiator to retry later Only STOP# asserted: target abort STOP# is driven High for 1 cycle when bus is idle, and the state is sustained by a pull-up resistor.
PAR	TS	1	Even parity for 36 bits of AD & C/BE#. PAR is sent one cycle after address or data is valid. In write transaction, initiator sends PAR one cycle after write data is valid. In read transaction, target sends PAR one cycle after read data is valid.
LOCK#	Input	1	Initiator request lock on target downstream. LOCK# is asserted 1 clock cycle after address phase by an initiator wanting to perform an atomic operation that take more than one transaction to complete. HIC passes the LOCK# request to the secondary PCI bus. HIC does not drive LOCK# or propagate LOCK# upstream.
IDSEL#	Input	1	Chip Select for Type 0 configuration access. During a Type 0 configuration transaction, the initiator asserts IDSEL# during the address phase to select HIC. HIC responds by asserting DEVSEL#.
PERR#	STS	1	Data Parity Error on all transactions except Special Cycle. PERR# is driven one clock cycle after PAR. PERR# is asserted by target during write transactions, and by initiator during read transactions.
SERR#	OD	1	System Error. HIC asserts SERR# under the following conditions: Address parity error. Secondary bus SERR# asserted. Posted write transaction: data parity error on target bus. Posted write transaction discarded. Master abort. Target abort Delayed read or write transaction discarded, and Delayed transaction master timeout.
REQ#	TS	1	Request for bus. If a target retry or disconnect is received in response to initiating a transaction, HIC deasserts REQ# for at least 2 cycles before asserting it again.
GNT#	Input	1	Bus is granted to HIC. HIC can initiate transaction if GNT# is asserted and the bus is idle. When HIC is not requesting bus and GNT# is asserted, HIC must drive AD, C/BE, and PAR to valid logic levels.
CLKRUN#	I/OD	1	Input indicating clock status. HIC can request the central clock resource to start, speed up or maintain the PCI clock. There are 3 clocking states: Clock running, Clock about to stop/slow down, and Clock stopped/slowed.
PCICK	Input	1	PCI Clock. All inputs are sampled on the rising edge of PCICK. Frequency

FIGURE 16

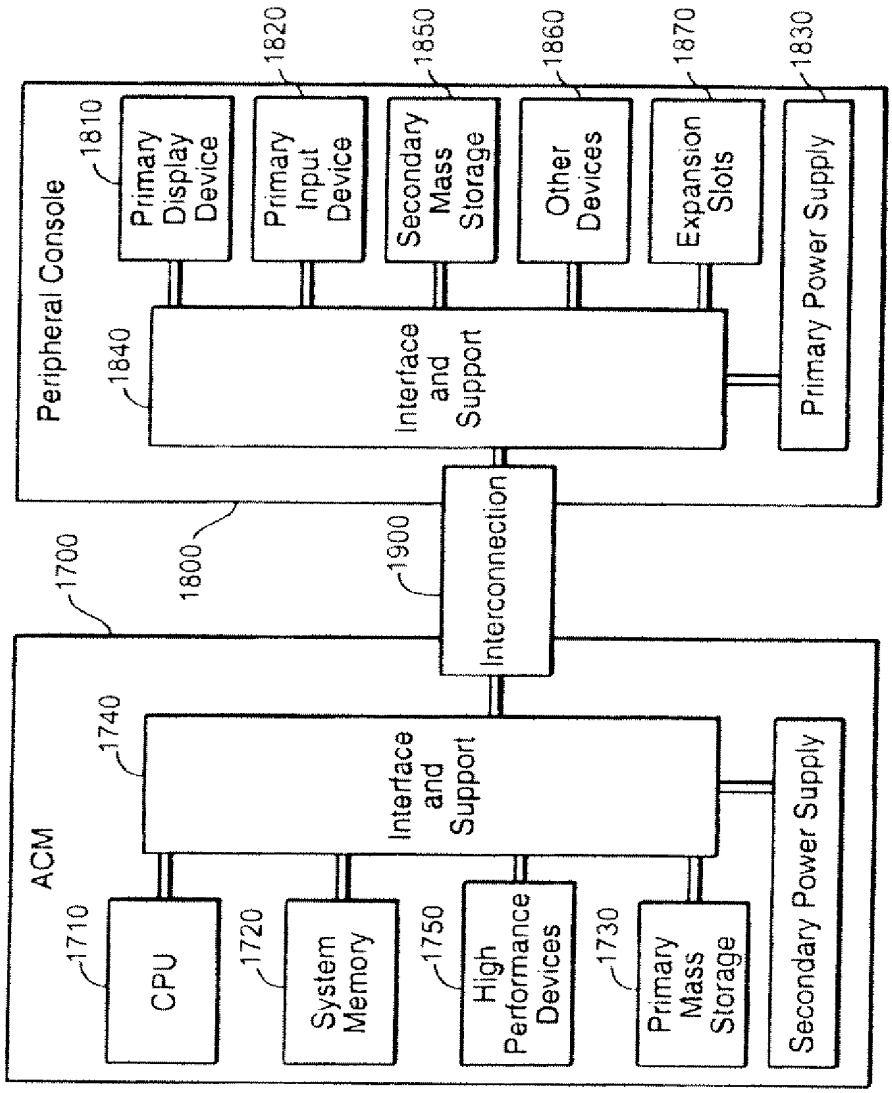

Peripheral Console
1810
Primary Display Device
1820
Primary Input Device
1850
Secondary Mass Storage
1860
Other Devices
1870
Expansion Slots
1830
Primary Power Supply
1840
Interface and Support
1800
1900
Interconnection
1700
ACM
1740
Interface and Support
1710
CPU
1720
System Memory
1750
High Performance Devices
1730
Primary Mass Storage
Secondary Power Supply

FIGURE 17

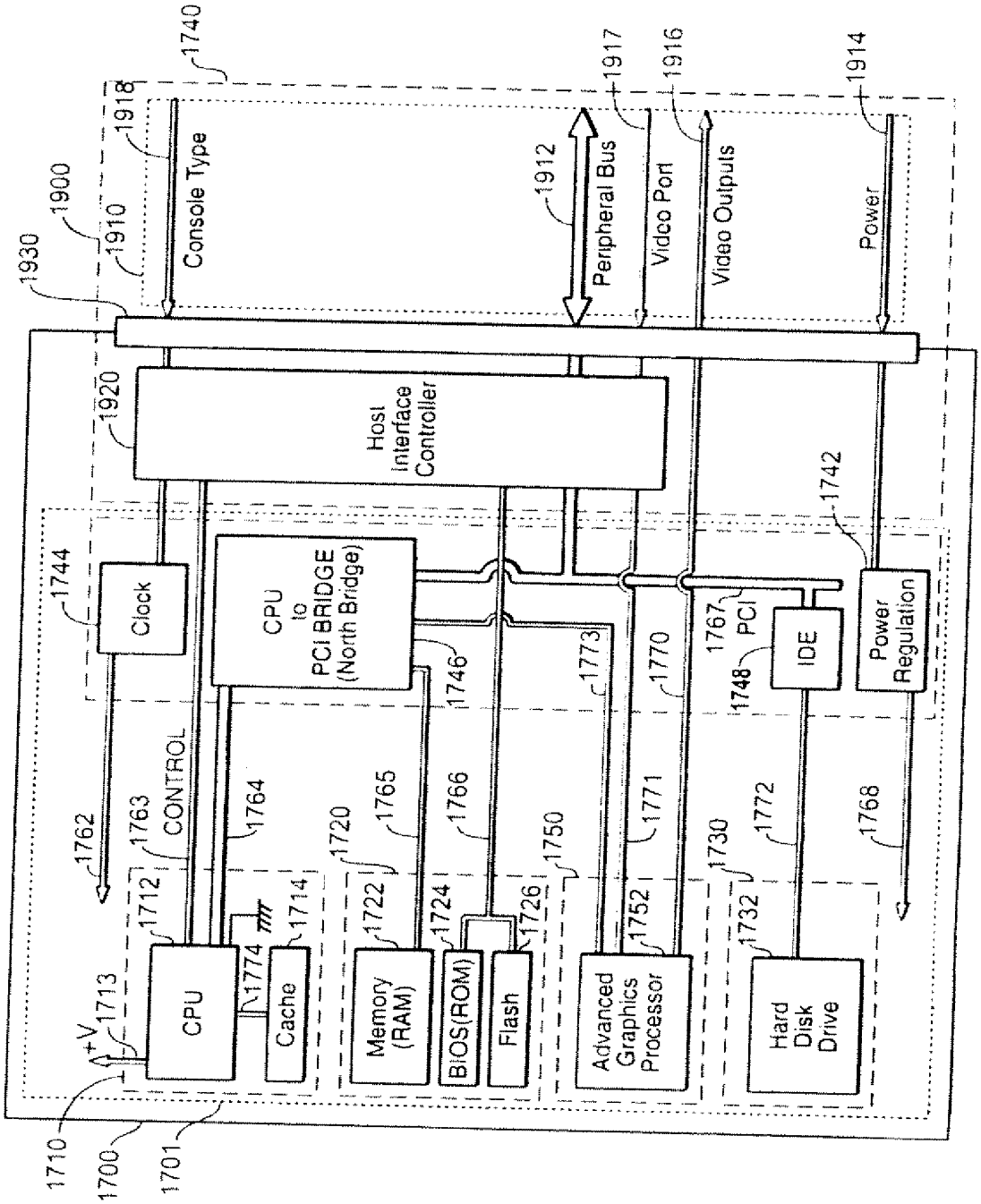

1740
1917
1916
1914
1918
1900
1910
1912
1930
Console Type
Peripheral Bus
Video Port
Video Outputs
Power
1920
Host Interface Controller
1742
1744
Clock
CPU to PCI BRIDGE (North Bridge)
1746
1773
1770
1767
PCI
1748
IDE
Power Regulation
1762
1763
CONTROL
1764
1765
1766
1720
1750
1771
1772
1730
1768
1712
1722
1724
1726
1752
1732
1713
1774
1714
CPU
Cache
Memory (RAM)
BIOS(ROM)
Flash
Advanced Graphics Processor
Hard Disk Drive
+V
1710
1700
1701

FIGURE 18

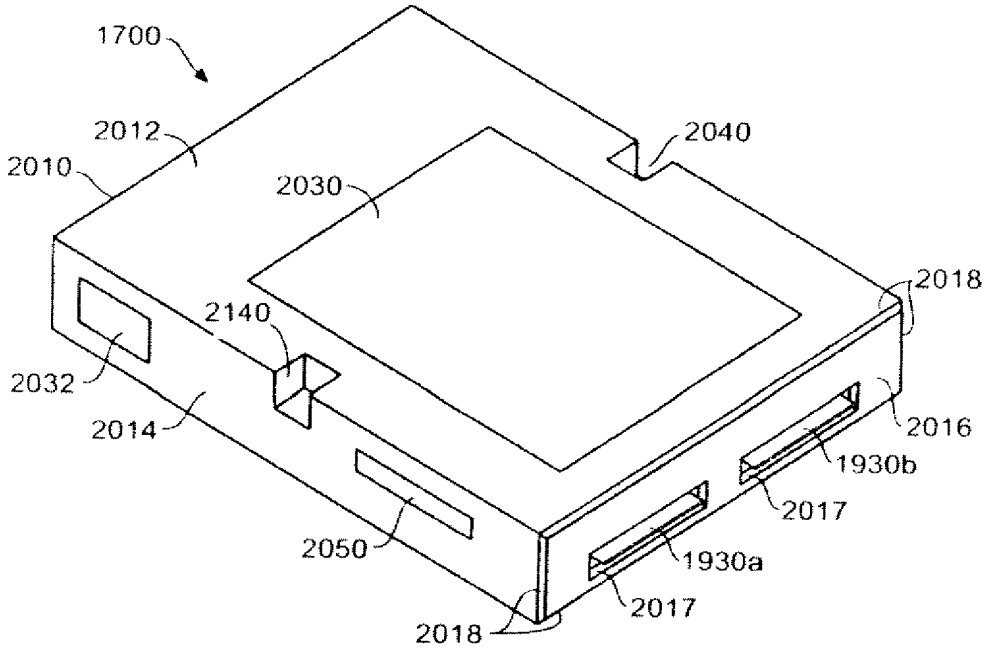

1700
2012
2010
2040
2030
2018
2140
2032
2014
2016
1930b
2017
2050
1930a
2017
2018

FIGURE 19

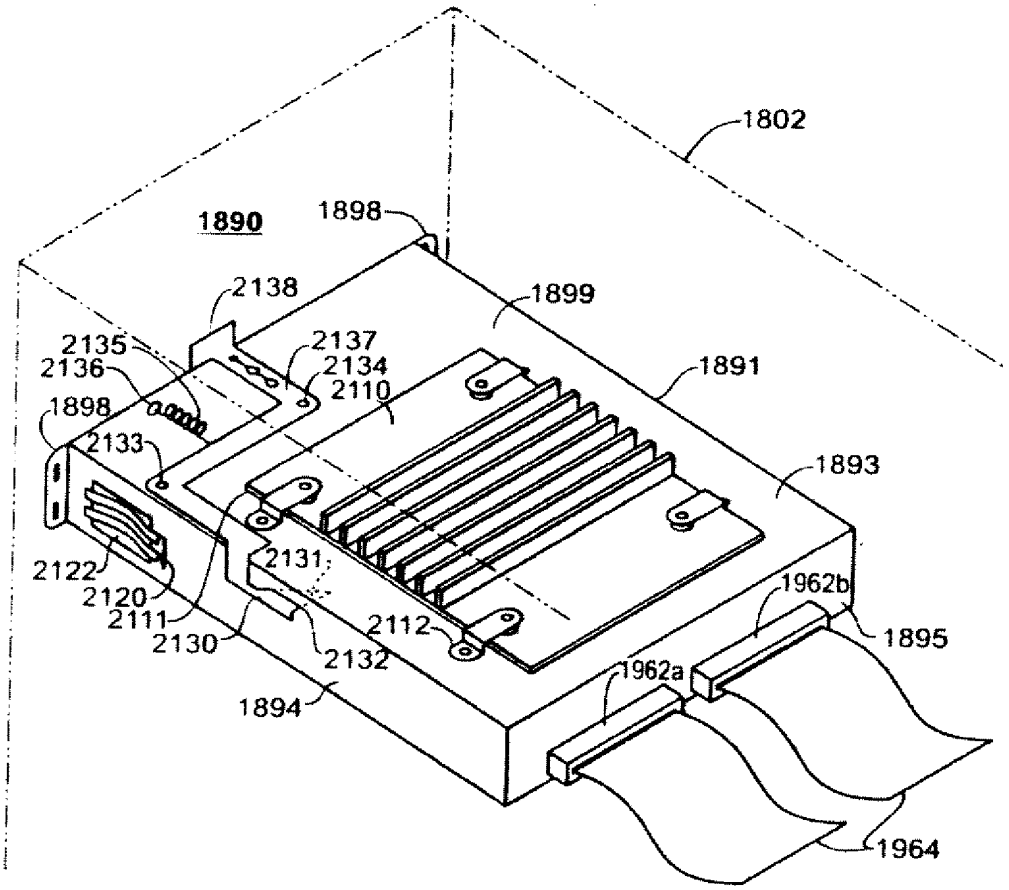

1802
1890
1898
2138
1899
2135
2136
2137
2134
2110
1891
1898
2133
1893
2122
2120
2111
2131
2130
2132
2112
1962b
1895
1894
1962a
1964

FIGURE 19B

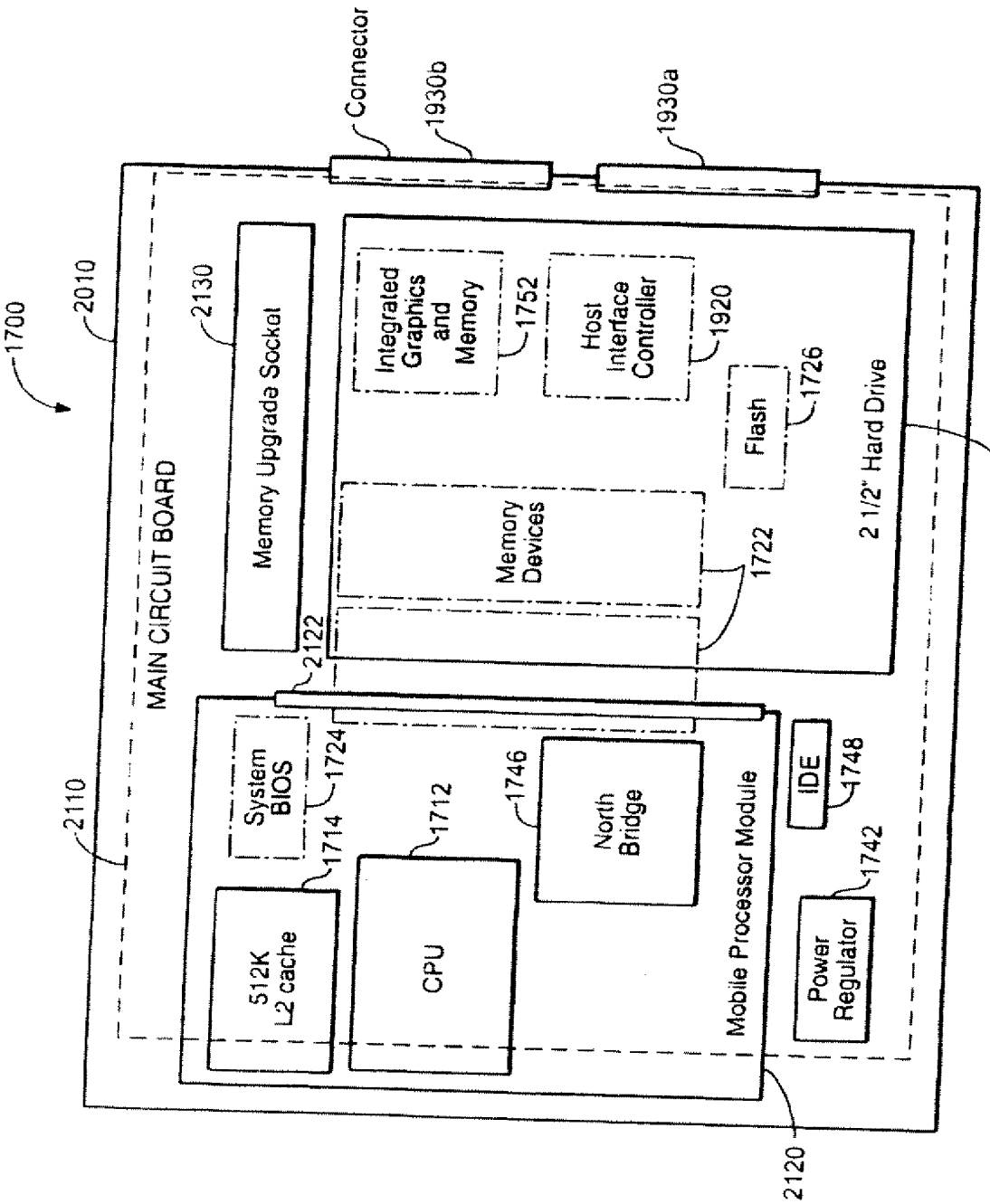

1700
2010
MAIN CIRCUIT BOARD
2130
Memory Upgrade Socket
Connector
1930b
1930a
Integrated Graphics and Memory
1752
Host Interface Controller
1920
Flash
1726
2 1/2" Hard Drive
1732
Memory Devices
1722
2122
2110
System BIOS
1724
1714
512K L2 cache
1712
CPU
1746
North Bridge
Mobile Processor Module
IDE
1748
Power Regulator
1742
2120

FIGURE 20

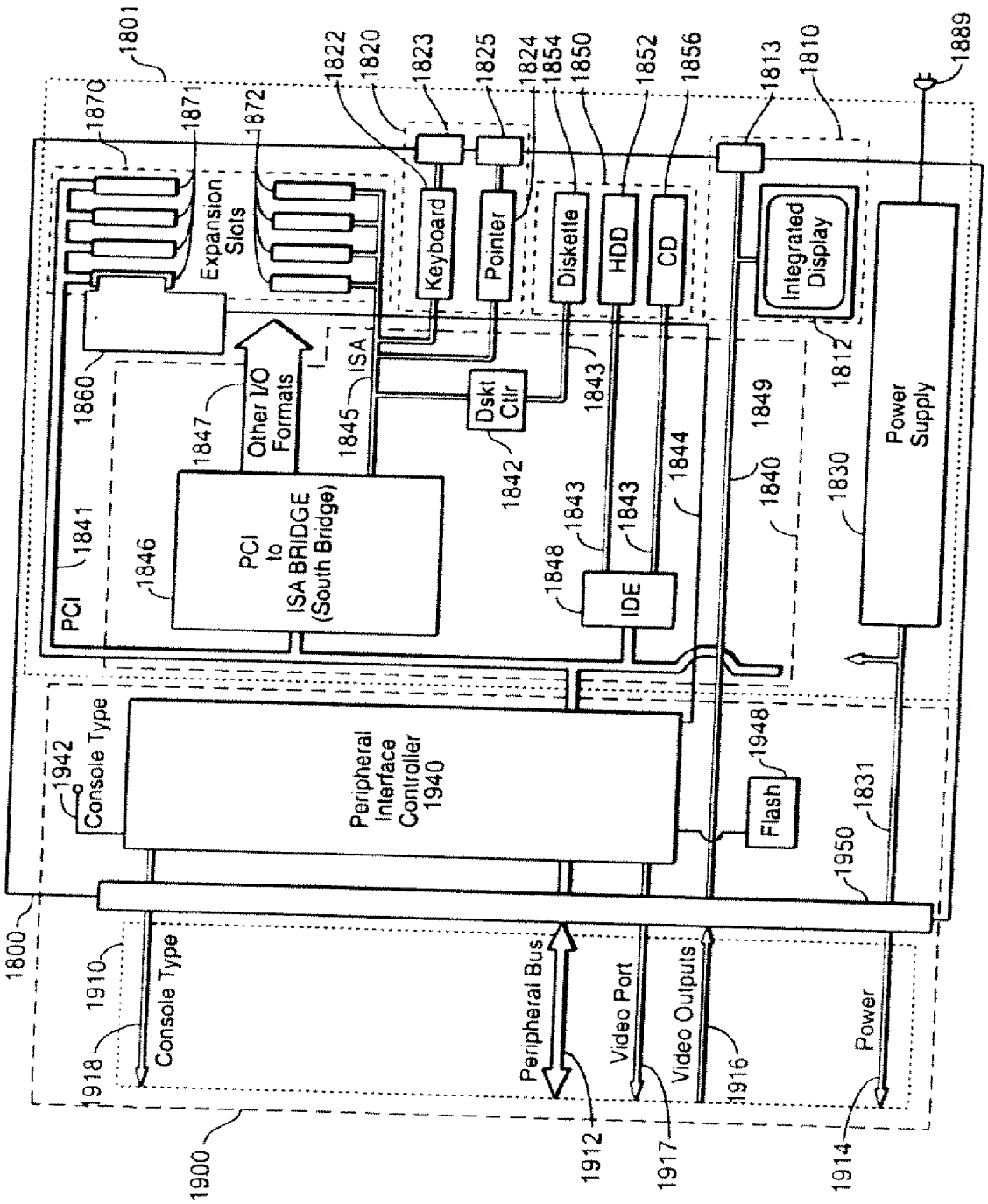

1801
1870
1871
1872
1822
1820
1823
1825
1824
1854
1850
1852
1856
1813
1810
1889
Expansion Slots
Keyboard
Pointer
Diskette
HDD
CD
Integrated Display
Power Supply
1860
1847
Other I/O Formats
ISA
1845
Dskt Cltr
1842
1843
1849
1812
1841
PCI
1846
PCI to ISA BRIDGE (South Bridge)
1848
IDE
1844
1840
1830
1942
Console Type
Peripheral Interface Controller 1940
1948
Flash
1831
1950
1800
1910
1918
Console Type
Peripheral Bus
Video Port
Video Outputs
1916
Power
1900
1912
1917
1914

FIGURE 21

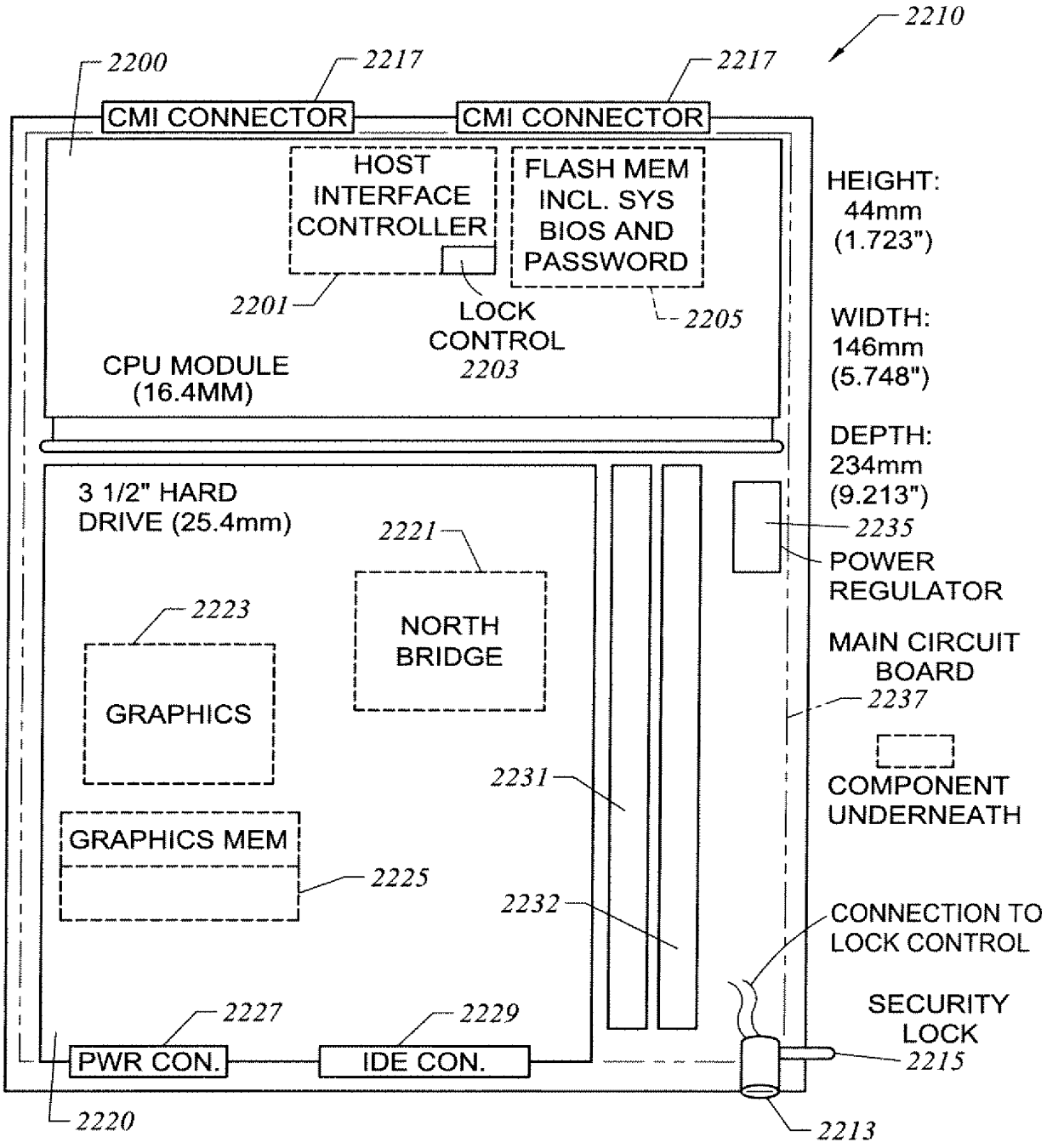

2210
2200
2217
2217
CMI CONNECTOR
CMI CONNECTOR
HOST INTERFACE CONTROLLER
FLASH MEM INCL. SYS BIOS AND PASSWORD
HEIGHT: 44mm (1.723")
2201
LOCK CONTROL 2203
2205
WIDTH: 146mm (5.748")
CPU MODULE (16.4MM)
DEPTH: 234mm (9.213")
3 1/2" HARD DRIVE (25.4mm)
2221
2235
POWER REGULATOR
2223
NORTH BRIDGE
MAIN CIRCUIT BOARD
2237
GRAPHICS
2231
COMPONENT UNDERNEATH
GRAPHICS MEM
2225
2232
CONNECTION TO LOCK CONTROL
2227
2229
SECURITY LOCK
PWR CON.
IDE CON.
2215
2220
2213

FIGURE 22

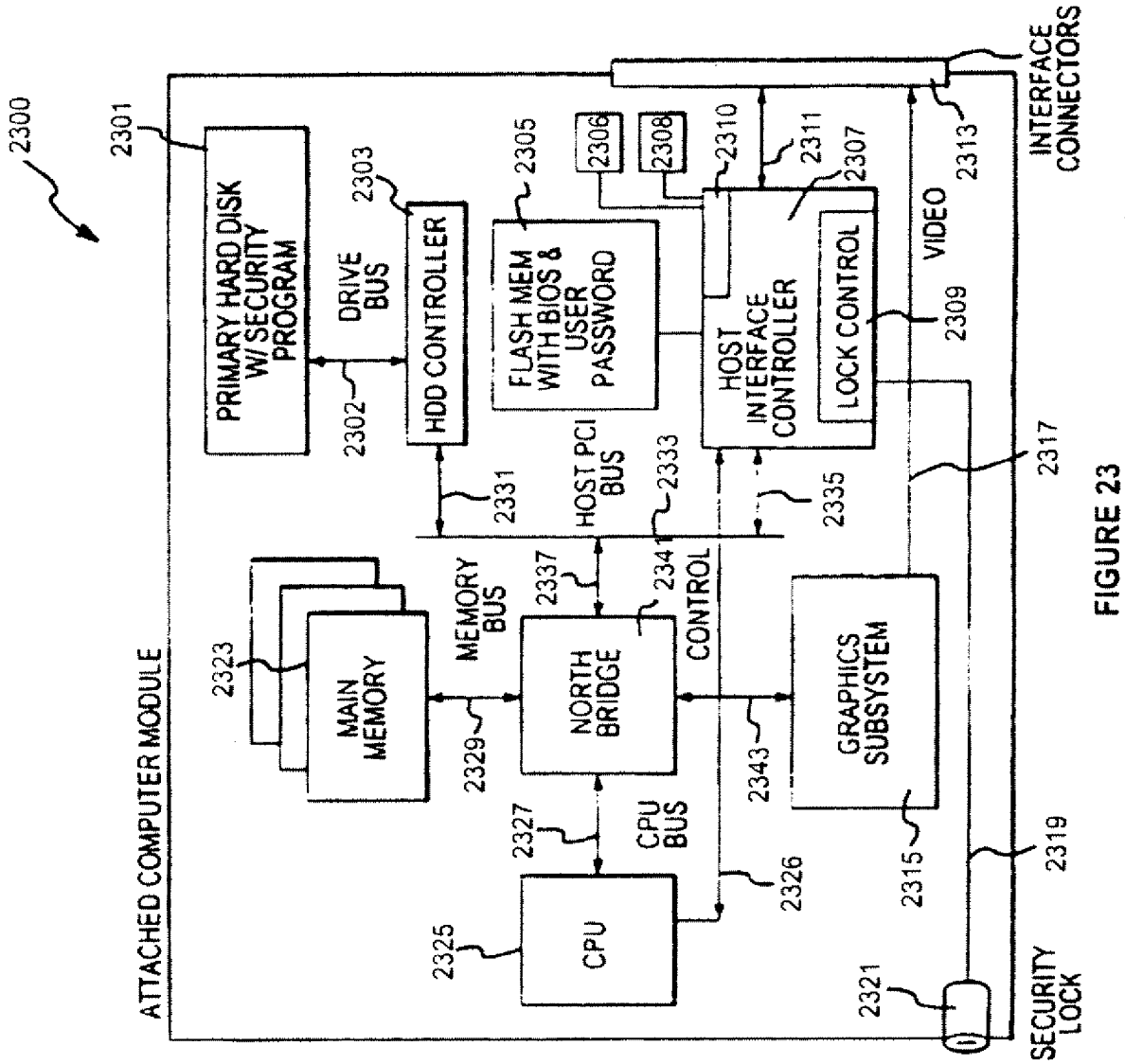

2300
2301
ATTACHED COMPUTER MODULE
PRIMARY HARD DISK W/SECURITY PROGRAM
2302
DRIVE BUS
2303
HDD CONTROLLER
2305
FLASH MEM WITH BIOS & USER PASSWORD
2306
2308
2310
2311
2307
HOST INTERFACE CONTROLLER
LOCK CONTROL
VIDEO
2309
2313
INTERFACE CONNECTORS
2331
HOST PCI BUS
2333
2335
2317
2323
MAIN MEMORY
MEMORY BUS
2329
2337
NORTH BRIDGE
234
CONTROL
2343
GRAPHICS SUBSYSTEM
2315
2319
2327
CPU BUS
2326
2325
CPU
2321
SECURITY LOCK

FIGURE 23

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:	CHU, William W. Y.	Confirmation No.:	1286
Serial No.:	12/504,534	Group Art Unit:	2111
Filed:	July 16, 2009	Examiner:	Unassigned

FOR: **MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNDIRECTIONAL SERIAL BIT CHANNELS**

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. §1.97(b)

In accordance with the duty of disclosure set forth in 37 C.F.R. §1.56, Applicant(s) hereby submits the following information in conformance with 37 C.F.R. §§1.97 and 1.98.

[] Pursuant to 37 C.F.R. §1.98, a copy of each non-US patent document cited in the attached Form PTO/SB/08 is enclosed.

[X] No copies of the publications (Citation Nos. 1-52) as listed on the attached Form PTO/SB/08 is being provided pursuant to 37 C.F.R. §1.98(d) because the publications were previously cited by, or submitted to the Office in prior Application Serial No. 12/077,503 to which the above-identified application claims priority under 35 U.S.C. §120.

[X] No copies of any U.S. patents or U.S. patent application publications listed on the attached Form PTO/SB/08 are being provided pursuant to 37 C.F.R. §1.98.

[] Publication(s) _____ listed on the attached Form PTO/SB/08 were cited in a foreign search or examination report corresponding to _____ application serial no. _____ and mailed on _____.

Attorney Docket No. ACQI-010/10 310578-2052

[] Enclosed is a copy of a non-English publication(s) _____ Pursuant to §609 of the M.P.E.P., Applicant submits the attached foreign search or examination report, which cites such non-English language publication(s).

[] Enclosed is a copy of a non-English publication(s) _____ English language publication _____ (copy enclosed) claims priority from this non-English publication.

[] Enclosed is an explanation of non-English publication(s) _____ for which an English translation is not available.

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This Information Disclosure Statement is filed within any one of the following time periods:

[] within three months from the filing date of this national application other than a CPA under 37 C.F.R. § 1.53(d);

[] within three months from the date of entry of the national stage as set forth in 37 C.F.R. §1.491 in this international application;

[x] before the mailing date of a first office action on the merits; or

[] before the mailing of a first office action after the filing of a request for continued examination under 37 C.F.R. § 1.114.

It is respectfully requested that the Examiner consider the above-noted information and return an initialed copy of the attached Form PTO/SB/08 to the undersigned.

Dated: 9/29/2009

Respectfully submitted,
COOLEY GODWARD KRONISH LLP

COOLEY GODWARD KRONISH LLP
ATTN: Patent Group
777 6th Street NW, Suite 1100
Washington, DC 20001

Tel: (650) 843-5852
Fax: (202) 842-7899

By: _____
Cliff Z. Liu
Reg. No. 50,834

PTO/SB/08a (07-09)
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(Not for submission under 37 CFR 1.99)

Application Number	12504534
Filing Date	2009-07-16
First Named Inventor	William W.Y. Chu
Art Unit	
Examiner Name	
Attorney Docket Number	ACQI-010/10US 310578-2052

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	6742068	B2	2004-05-25	Gallagher et al.	

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	Application Number	12504534
	Filing Date	2009-07-16
	First Named Inventor	William W.Y. Chu
	Art Unit	
	Examiner Name	
	Attorney Docket Number	ACQI-010/10US 310578-2052

	1	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Exhibit B, US Patent No. 6,718,415 File History, 159 pages	☐
	2	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Exhibit C, Patent Owner's Asserted Claim Construction against Hewlett-Packard Company, 15 pages	☐
	3	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Exhibit D, Patent Owner's Asserted Claim Construction against International Business Machines Corporation, 11 pages	☐
	4	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Exhibit E, QuantumNet.com [1997-10-11], [online], [retrieved on 2009-11-16] Retrieved from the Internet Archive (archive.org) using Internet, 16 pages	☐
	5	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Exhibit F, jlChatCom.com {1997-1-4], [online], [retrieved on 2009-12-2] Retrieved from the Internet Archive (archive.org) using Internet, 15 pages	☐
	6	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Exhibit G, Eversys.com [1996-11-4], [online], [retrieved on 2009-11-16] Retrieved from the Internet Archive (archive.org) using Internet, 17 pages	☐
	7	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Exhibit H, Origin2000 Rackmount Owner's Guide [1998-6-15], [online], [retrieved on 2009-11-16] Retrieved from Silicon Graphics, Inc. using Internet <URL:http://techpubs.sgi.com/library/manuals/3000/007-3415-003/pdf/007-3415-003.pdf>, 149 pages	☐
	8	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Exhibit K, Novell Netware 4.11 documentation [1996], [online], [retreived on 2009-11-16] Retreived from Novell Inc. using Internet ,URL:http://www.novell.com/documentation/nw4/docui/>, 14 pages	☐
	9	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Exhibit L, Origin and Onyx2 Theory of Operations Manual [1998-6-15], [online], [retrieved on 2009-11-16] Retrieved from Silicon Graphics, Inc. using Internet <URL:http://techpubs.sgi.com/library/manuals/3000/007-3439-002/pdf/007-3439-002.pdf>, 127 pages	☐
	10	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Exhibit M (Part 1), IRIS Failsafe Administrator's Guide {1997-4-6], [online], [retrieved on 2009-11-16] Retrieved from Silicon Graphics Inc. using Internet <URL:http://techpubs.sgi.com/librarymanuals/3000/007-3109-003/pdf/007-3109-003.pdf>, 115 pages	☐
	11	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Exhibit M (Part 2), IRIS Failsafe Administrator's Guide {1997-4-6], [online], [retrieved on 2009-11-16] Retrieved from Silicon Graphics Inc. using Internet <URL:http://techpubs.sgi.com/librarymanuals/3000/007-3109-003/pdf/007-3109-003.pdf>, 101 pages	☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	12504534
	Filing Date	2009-07-16
	First Named Inventor	William W.Y. Chu
	Art Unit	
	Examiner Name	
	Attorney Docket Number	ACQI-010/10US 310578-2052

	12	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Exhibit N, CAPserver Product Guide, 1995, pp.1-16, 19 pages	☐
	13	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Exhibit O, Declaration Under 37 CFR 1.132 of Vincent P. Conroy, 11-24-2009, 3 pages	☐
	14	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Exhibit AA, Claim Charts with respect to QuantumNet for Anticipation and Obviousness, 60 pages	☐
	15	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Exhibit BB, Claim Charts with respect to Chatcom for Anticipation and Obviousness, 51 pages	☐
	16	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Exhibit CC, Claim Charts with respect to Eversys for Anticipation and Obviousness, 51 pages	☐
	17	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Exhibit DD, Claim Chart with respect to the Origin2000 Manual for Obviousness, 36 pages	☐
	18	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Exhibit EE, Claim Chart with respect to Gallagher for Anticipation and Obviousness, 59 pages	☐
	19	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Request for Inter Partes Reexamination, 44 pages	☐

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[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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	Application Number	12504534
	Filing Date	2009-07-16
	First Named Inventor	William W.Y. Chu
	Art Unit	
	Examiner Name	
	Attorney Docket Number	ACQI-010/10US 310578-2052

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

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☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Cliff Z. Liu/	Date (YYYY-MM-DD)	2010-01-05
Name/Print	Cliff Z. Liu	Registration Number	50834

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

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EFS ID:	6754791
Application Number:	12504534
International Application Number:	
Confirmation Number:	1286
Title of Invention:	MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNDIRECTIONAL SERIAL BIT CHANNELS
First Named Inventor/Applicant Name:	William W. Y. Chu
Customer Number:	58249
Filer:	Cliff Z. Liu/Bobbie Jutras
Filer Authorized By:	Cliff Z. Liu
Attorney Docket Number:	ACQI-010/10US 310578-2052
Receipt Date:	05-JAN-2010
Filing Date:	16-JUL-2009
Time Stamp:	18:47:02
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Filed (SB/08)	ACQI-010-10US_01-05-10_IDS_Form_SB08a.pdf	609159 42e7e3936b786d387a150cfc39a71e05016e675e	no	5

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2	NPL Documents	USP6718415_FileHistory.pdf	8152832 85955f123921d575bf592815d6b67f277e9e93fb	no	159
Warnings:					
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3	NPL Documents	USP_6718415_IPReexam_Acquis_Asserted_Claim_Construction_against_HP.pdf	1818595 54782f726b99a16571b5607df0612c27727d6de1	no	15
Warnings:					
Information:					
4	NPL Documents	USP_6718415_IPReexam_Acquis_Asserted_Claim_Construction_against_IBM.pdf	1283424 8e575a1901051bfd48d65235fa64ea2a15ad4d84	no	11
Warnings:					
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5	NPL Documents	Quantumnet.pdf	998472 85fe4b2cb7dc0ad7f63741d8885b11059946a54a	no	16
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6	NPL Documents	JLChatcom.pdf	668328 e76418b0d6cd385972747ec5ceaf7c233f3e8ec0	no	15
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7	NPL Documents	Eversys.pdf	1077867 7adb4cc8861441f8005548680a14d14e52156656	no	17
Warnings:					
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8	NPL Documents	SGI_Rackmount_Guide.pdf	8028523 d4f21792ffb7134e87b10f42a2ab6a3c4d628b0c	no	149
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9	NPL Documents	NovellNetware_411.pdf	420785 fd554cd29ab9fa54636d2a9d2e9dd908b3b91017	no	14
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10	NPL Documents	SGI_OriginOnyx2TheoryOperations_Manual.pdf	4360664 62ae5c0a2c19faae5e05c3cb9dab576de012a0c4	no	127
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11	NPL Documents	SGI_IRIS_Failsafe_Administrators_Guide-Part1.pdf	3887879 50243982ad7eb4eb2f322faa95788b98ac3d7079	no	115
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Warnings:					
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13	NPL Documents	Evergreen_Systems_CAPserver_Guide.pdf	2027841 ac28240d052fb046ff339f3f67cad33aa8d0820a	no	19
Warnings:					
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14	NPL Documents	Conroy_Declaration.pdf	84601 0b1f8a22a605bc80538127adc9af00b9e3789830	no	3
Warnings:					
Information:					
15	NPL Documents	USP_6718415_IPReexam_QuantumNet_Claim_Charts.pdf	4750417 ec5cd7c81965b9b4fdd85ccd57fae9203e690ff6	no	60
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Information:					
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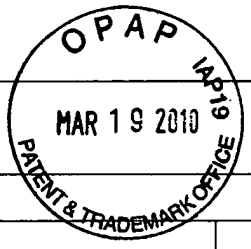
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	12504534
Filing Date	2009-07-16
First Named Inventor	William W. Y. Chu
Art Unit	
Examiner Name	
Attorney Docket Number	ACQI-010/10US 310578-2052



U.S.PATENTS

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	Examiner Name	
	Attorney Docket Number	ACQI-010/10US 310578-2052

	1	Ziatech Corporation-Ketris9000 Product Manual (2000) (159 pp.) (No. 18.pdf)	☐
	2	Ziatech Corp. ZT 8907 Product Description (1998) (4 pp) (No. 19b.pdf)	☐
	3	Ziatech Corp. ZT 8908 Product Description (1998)+A249 (6 pp) (No. 19c.pdf)	☐
	4	Ziatech Corp. System Designer's Guide: Hot Swap Capability on STD 32 Computers (Jan. 1996) (6 pp) (No. 19e.pdf)	☐
	5	Ziatech Corp. Press Release (Feb. 1996) (2 pp.) (No. 19i.pdf)	☐
	6	Ziatech Corp. Industrial BIOS for CompacktPCI and STD 32 Systems Software Manual (July 1998) (134 pp) No. 19h.pdf)	☐
	7	Ziatech Corp.System Designers Guide: Expanding STD Bus Performance Through Multiprocessing. (Apr. 1996) (6 pp.) (No. 19d.pdf)	☐
	8	Ziatech, STD 32 Star System Product Description(6 pp) (No. 19a.pdf)	☐
	9	Ziatech Corp. zVID2 Local Bus Super VGA/FPD Adapter Product Description (2 pp) (Apr. 1996) (No. 19f.pdf)	☐

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	Attorney Docket Number	ACQI-010/10US 310578-2052

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☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Cliff Z. Liu/	Date (YYYY-MM-DD)	2010-03-19
Name/Print	Cliff Z. Liu	Registration Number	50,834

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OPAP IAP19 MAR 19 2010 PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:	CHU, William W. Y.	Confirmation No.:	1286
Serial No.:	12/504,534	Group Art Unit:	Not yet assigned
Filed:	July 16, 2009	Examiner:	Not yet assigned

FOR: **Multiple Module Computer System and Method Including Differential Signal Channel Comprising Unidirectional Serial Bit Channels**

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Date of Deposit: March 19, 2010

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Date: March 19, 2010 By: Kathleen M. Smith

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INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. §1.97(b)

In accordance with the duty of disclosure set forth in 37 C.F.R. §1.56, Applicant(s) hereby submits the following information in conformance with 37 C.F.R. §§1.97 and 1.98.

[X] Pursuant to 37 C.F.R. §1.98, a copy of each non-US patent document cited in the attached Form PTO/SB/08 is is on the enclosed Compact Disk.

[] No copies of the publications listed on the attached Form PTO/SB/08 are being provided pursuant to 37 C.F.R. §1.98(d) because the publications were previously cited by or submitted to the Office in prior Application Serial No. _____ to which the above-identified application claims priority under 35 U.S.C. §120.

[X] No copies of any U.S. patents or U.S. patent application publications listed on the attached Form PTO/SB/08 are being provided pursuant to 37 C.F.R. §1.98.

[] Publication(s) _____ listed on the attached Form PTO/SB/08 were cited in a foreign search or examination report corresponding to _____ application serial no. _____ and mailed on _____.

[] Enclosed is a copy of a non-English publication(s) _____ Pursuant to §609 of the M.P.E.P., Applicant submits the attached foreign search or examination report, which cites such non-English language publication(s).

[] Enclosed is a copy of a non-English publication(s) _____ English language publication _____ (copy enclosed) claims priority from this non-English publication.

[] Enclosed is an explanation of non-English publication(s) _____ for which an English translation is not available.

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[] Enclosed is a copy of pending patent Application Serial No. _____.

This Information Disclosure Statement is filed within any one of the following time periods:

[] within three months from the filing date of this national application other than a CPA under 37 C.F.R. § 1.53(d);

[] within three months from the date of entry of the national stage as set forth in 37 C.F.R. §1.491 in this international application;

[X] before the mailing date of a first office action on the merits; or

[] before the mailing of a first office action after the filing of a request for continued examination under 37 C.F.R. § 1.114.

It is respectfully requested that the Examiner consider the above-noted information and return an initialed copy of the attached Form PTO/SB/08 to the undersigned.

Dated: March 19, 2010

Respectfully submitted,
COOLEY GODWARD KRONISH LLP

By: _____
Cliff Z. Liu
Reg. No. 50,834

CUSTOMER NO. 58249
COOLEY GODWARD KRONISH LLP
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Washington, DC 20001

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PTO/SB/08a (01-10)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

OPAP IAP19 MAR 19 2010 PATENT & TRADEMARK OFFICE

Application Number	12504534
Filing Date	2009-07-16
First Named Inventor	William W. Y. Chu
Art Unit	
Examiner Name	
Attorney Docket Number	ACQI-010/10US 310578-2052

U.S.PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	4228496		1980-10-14	Katzman et al.	
	2	4453215		1984-06-05	Reid	
	3	4680674		1987-07-14	Moore	
	4	4760276		1988-07-26	Lethellier	
	5	4791524		1988-12-13	Teigen et al.	
	6	5187645		1993-02-16	Spalding et al.	
	7	5282247		1994-01-25	McLean et al.	
	8	5325517		1994-06-28	Baker et al.	

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	9	5339408		1994-08-16	Bruckert et al.	
	10	5577205		1996-11-19	Hwang et al.	
	11	5430607		1995-07-04	Smith	
	12	5432939		1995-07-11	Blackledge Jr. et al.	
	13	5436902		1995-07-25	McNamara et al.	
	14	5533125		1996-07-02	Bensimon et al.	
	15	5537544		1996-07-16	Morisawa et al.	
	16	5552776		1996-09-03	Wade et al.	
	17	5588850		1996-12-31	Pan et al.	
	18	5673172		1997-09-30	Hastings et al.	
	19	5680536		1997-10-21	Tyuluman	

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	20	5708840		1998-01-13	Kikinis et al.	
	21	5724591		1998-03-03	Hara et al.	
	22	5737194		1998-04-07	Hopkins et al.	
	23	5774703		1998-06-30	Weiss et al.	
	24	5802391		1998-09-01	Hwang	
	25	5805903		1998-09-08	Elkhoury	
	26	5809262		1998-09-15	Potter	
	27	5884053		1999-03-16	Clouser et al.	
	28	5978821		1999-11-02	Freeny	
	29	5982614		1999-11-09	Reid	
	30	6049823		2000-04-11	Hwang	

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	31	6070211		2000-05-30	Neal et al.	
	32	6078503		2000-06-20	Gallagher et al.	
	33	6091737		2000-07-18	Hong et al.	
	34	6145085		2000-11-07	Tran et al.	
	35	6188602		2001-02-13	Alexander et al.	
	36	6256691		2001-07-03	Moroz et al.	
	37	6297955		2001-10-02	Frank Jr. et al.	
	38	6311287		2001-10-30	Dischler et al.	
	39	6325636		2001-12-04	Hipp et al.	
	40	6411506		2002-06-25	Hipp et al.	
	41	6567877		2003-05-20	Lewis et al.	

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	42	6581125		2003-06-17	Lange et al.	
	43	6715100		2004-03-30	Hwang	
	44	6747878		2004-06-08	Hipp et al.	
	45	6948047		2005-09-20	Maruska et al.	
	46	6985967		2006-01-10	Hipp	
	47	7017001		2006-03-21	Hill et al.	
	48	7020735		2006-03-28	Kikinis	
	49	7339786		2008-03-04	Bottom et al.	

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U.S.PATENT APPLICATION PUBLICATIONS

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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	Attorney Docket Number	ACQI-010/10US 310578-2052

FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	JP 7-04672			1995-03-10	Toshiba Corp.		☐
	2	JP 7-084675			1995-03-31	Hitachi Ltd.		☐
	3	JP 6-289956			1994-10-18	Hitachi Ltd.		☐
	4	WO 97/05618			1997-02-13	Memory Corporation		☐

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NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	Acqis -v- Appro International, USDC-Eastern District of Texas (Tyler Div) Case No. 6:09-cv-148-LED Defendants' Amended Invalidity Contentions (March 1, 2010)	☐
	2	Acqis -v- Appro International, USDC-Eastern District of Texas (Tyler Div) Case No. 6:09-cv-148-LED EXHIBIT B-Defendants' Amended Invalidity Contentions (March 1, 2010)	☐
	3	Acqis -v- Appro International, USDC-Eastern District of Texas (Tyler Div) Case No. 6:09-cv-148-LED EXHIBIT C-Defendants' Amended Invalidity Contentions (March 1, 2010)	☐
	4	Acqis -v- Appro International, USDC-Eastern District of Texas (Tyler Div) Case No. 6:09-cv-148-LED EXHIBIT D-Defendants' Amended Invalidity Contentions (March 1, 2010)	☐

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	Attorney Docket Number	ACQI-010/10US 310578-2052

	5	Acqis -v- Appro International, USDC-Eastern District of Texas (Tyler Div) Case No. 6:09-cv-148-LED EXHIBIT E-Defendants' Amended Invalidity Contentions (March 1, 2010)	☐
	6	Acqis -v- Appro International, USDC-Eastern District of Texas (Tyler Div) Case No. 6:09-cv-148-LED EXHIBIT F-Defendants' Amended Invalidity Contentions (March 1, 2010)	☐
	7	Acqis -v- Appro International, USDC-Eastern District of Texas (Tyler Div) Case No. 6:09-cv-148-LED APPENDIX 1-Defendants' Amended Invalidity Contentions (March 1, 2010)	☐
	8	Acqis -v- Appro International, USDC-Eastern District of Texas (Tyler Div) Case No. 6:09-cv-148-LED Defendants' Notice of Errata Re Invalidity Contentions (March 1, 2010)	☐
	9	ACCTON, Gigabit Ethernet PCI Adapter (1999) (2 pp) (No. 122.pdf)	☐
	10	AMD-K6-III Processor Data Sheet (1999) (326 pp) (No. 114.pdf)	☐
	11	Black Box Network Services "Welcome to the ServSwitch Family" (Jul. 1998) (52 pp) (No. 115.pdf)	☐
	12	Cisco AS5800 Universal Access Server Dial Shelf Controller Card Installation & Replacement (1997/1999) (28 pp) (No. 116.pdf)	☐
	13	CUBIX White paper: Benefits of High Density Servers (Jul. 2009) (6 pp) (Cubix-1.pdf)	☐
	14	Digital AlphaServer 4000 and 4100 Systems (1998) (4 pp) (No. 117.pdf)	☐
	15	EIA-422A - Standard (Superseded), Electrical Characteristics of Balanced Voltage Digital Interface Circuits (Dec. 1978) (20 pp) (No. 118a.pdf)	☐

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	16	Grow et al. (XLNT Designs), "Gigabit Media Independent Interface Proposal," IEEE 802.z Vancouver (11 Nov 1996) (22 pp) (No. 124.pdf)	☐
	17	HP: HDMP-1636, Gigabit Ethernet Transceiver Chip, Preliminary Technical Data (May 1997) (No. 123.pdf)	☐
	18	Huq et al. "An Overview of LVDS Technology" National Semiconductor Corp. (Jul. 1998) (6 pp.) (No. 118d.pdf)	☐
	19	IBM 8260 ATM Product Architecture (Sept. 1997) (220 pp.) (No. 1.pdf)	☐
	20	IBM 8265 Nways ATM Switch Product Description (1994 / 1998) (144 pp.) (No. 2.pdf)	☐
	21	Intel Pentium II Processor Datasheet (Aug. 1998) (84 pp.) (No. 129.pdf)	☐
	22	Intel, 82559 Fast Ethernet Multifunction PCI/Cardbus Controller (Jan. 1999) (56 pp.) (No. 128.pdf)	☐
	23	Intel, 21143 PCI/CardBus 10/100Mb/s Ethernet LAN Controller, Product Datasheet (Oct. 1998) (8 pp.) (No. 127.pdf)	☐
	24	KTI Networks, Installation Guide 10/100 Dual-speed Fast Ethernet PCI Adapters (1999) (24 pp.) (No. 126.pdf).	☐
	25	Micronet SP2500R Series Etherfast 10/100 MBPS Adapter, User's Guide (1999) (10 pp.) (No. 136.pdf)	☐
	26	Miastkowski, Stan "A Whale of a System," Byte (Aug. 1991) pp. 39-40 (No. 35.pdf)	☐

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	27	NEC Computer Systems: Server HX4500 User's Guide (Dec. 1998) (160 pp.) (No. 132.pdf)	☐
	28	Khan, Fasil "Ethernet Switch Card Design-Layout Specification, Rev. 2.00) (Aug 2001) (63 pp) (No. 26j.pdf)	☐
	29	PCI Local Bus Specification (Rev. 2.2, Dec. 1998) (322 pp.) (No. 135.pdf)	☐
	30	Sun Microsystems, Sun Enterprise 250 Server Owner's Guide (Jun. 1998) (324 pp.) (No. 137.pdf)	☐
	31	Sun Microsystems, UltraSPARC-II CPU Module Datasheet (Jul. 1999) (28 pp.) (No. 138.pdf)	☐
	32	Sun Microsystems, Netra ft 1800 White Paper (Apr. 1999) (50 pp.) (No. 139.pdf)	☐
	33	TIA/EIA (644) Standard Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits (Mar. 1996) (42 pp) (No. 118c.pdf)	☐
	34	Network Engines: P6000EXP Fault-Tolerant Load-Balanced Cluster Server (NEI00095) (1997) (4 pp.) (No. 22a.pdf)	☐
	35	Network Engines ClusterDirector User's Manual (Jun. 1998) (32 pp.) (No. 22b.pdf)	☐
	36	Freakes, Louise "Disk Connector Card Functional Requirement / Layout Specifications" (Jan. 1998) (9 pp.) (No. 26d.pdf)	☐
	37	Phillips, 9800 Processor Card Layout & Design Specifications (July 1997) (142 pp) (No. 26o.pdf)	☐

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	Attorney Docket Number	ACQI-010/10US 310578-2052

	38	Eversys, CAPserver Product Brief (Nov. 2009) (No. 119.pdf)	☐
	39	Burrow, "Whitecross Data Exploration: A Technical Overview of the WXDES/98000 (Mar. 1999 Rev. 2.00) (90 pp) (No. 26f.pdf)	☐
	40	Burrow, "Whitecross Data Exploration: A Technical Overview of the WXDES/98000 (Apr. 1999) (222 pp) (No. 26i.pdf)	☐
	41	USB Compaq, Intel, Microsoft, NEC - (Rev. Apr. 2000) (650 pp.) (No. 141.pdf)	☐
	42	USB Compaq, Intel, Microsoft, NEC - Rev. (Sep. 1998) (327 pp.) No. 140.pdf	☐
	43	Whitecross Data Exploration Configuration and Maintenance Manual. Draft. (Jul 2000) (699 pp.) (No. 26e.pdf)	☐
	44	Whitecross WX-DES Hardware Maintenance (2000) (284 pp) (No. 26g.pdf)	☐
	45	Whitecross WX-DES Technical Overview (2000) (211 pp) (No. 26h.pdf)	☐
	46	Smith, Brendon "Processor Backplane Functional Requirement Specification" (Jul. 1997) (45 pp) (No. 26k.pdf)	☐

If you wish to add additional non-patent literature document citation information please click the Add button

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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	Attorney Docket Number	ACQI-010/10US 310578-2052

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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	Examiner Name	
	Attorney Docket Number	ACQI-010/10US 310578-2052

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Cliff Z. Liu/	Date (YYYY-MM-DD)	2010-03-19
Name/Print	Cliff Z. Liu	Registration Number	50,834

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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March 8, 2004

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Attorney Docket No. ACQI-010/10US 310578-2052 **PATENT**

OPAP IAP19 MAR 19 2010 PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:	CHU, William W. Y.	Confirmation No.:	1286
Serial No.:	12/504,534	Group Art Unit:	Not yet assigned
Filed:	July 16, 2009	Examiner:	Not yet assigned

FOR: **Multiple Module Computer System and Method Including Differential Signal Channel Comprising Unidirectional Serial Bit Channels**

Express Mail Label Number: EQ285618171US
Date of Deposit: March 19, 2010

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to the Director of Patents, PO Box 1450, Alexandria, VA 22318-1450

Date: March 19, 2010 By: Kathleen M. Smith
Kathleen M. Smith

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. §1.97(b)

In accordance with the duty of disclosure set forth in 37 C.F.R. §1.56, Applicant(s) hereby submits the following information in conformance with 37 C.F.R. §§1.97 and 1.98.

[X] Pursuant to 37 C.F.R. §1.98, a copy of each non-US patent document cited in the attached Form PTO/SB/08 is on the enclosed Compact Disk. .

[] No copies of the publications listed on the attached Form PTO/SB/08 are being provided pursuant to 37 C.F.R. §1.98(d) because the publications were previously cited by or submitted to the Office in prior Application Serial No. _____ to which the above-identified application claims priority under 35 U.S.C. §120.

[X] No copies of any U.S. patents or U.S. patent application publications listed on the attached Form PTO/SB/08 are being provided pursuant to 37 C.F.R. §1.98.

[] Publication(s) _____ listed on the attached Form PTO/SB/08 were cited in a foreign search or examination report corresponding to _____ application serial no. _____ and mailed on _____.

[] Enclosed is a copy of a non-English publication(s) _____ Pursuant to §609 of the M.P.E.P., Applicant submits the attached foreign search or examination report, which cites such non-English language publication(s).

[] Enclosed is a copy of a non-English publication(s) _____ English language publication _____ (copy enclosed) claims priority from this non-English publication.

[] Enclosed is an explanation of non-English publication(s) _____ for which an English translation is not available.

[] Enclosed is an English translation of non-English publication(s) _____ cited in the attached Form PTO/SB/08.

[] Enclosed is a copy of pending patent Application Serial No. _____.

This Information Disclosure Statement is filed within any one of the following time periods:

[] within three months from the filing date of this national application other than a CPA under 37 C.F.R. § 1.53(d);

[] within three months from the date of entry of the national stage as set forth in 37 C.F.R. §1.491 in this international application;

[X] before the mailing date of a first office action on the merits; or

[] before the mailing of a first office action after the filing of a request for continued examination under 37 C.F.R. § 1.114.

It is respectfully requested that the Examiner consider the above-noted information and return an initialed copy of the attached Form PTO/SB/08 to the undersigned.

Dated: March 19, 2010

Respectfully submitted,
COOLEY GODWARD KRONISH LLP

By: _____
Cliff Z. Liu
Reg. No. 50,834

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777 6th Street NW, Suite 1100
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:	CHU, William W.Y.	Confirmation No.:	1286
Serial No.:	12/504,534	Group Art Unit:	Unassigned
Filed:	July 16, 2009	Examiner:	Unassigned

FOR: **MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNIDIRECTIONAL SERIAL BIT CHANNELS**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST FOR UPDATED FILING RECEIPT

Please issue an Updated Filing Receipt for this patent application.

Applicant filed a Response to the Notice To File Corrected Application Papers on September 29, 2009.

Dated: March 24, 2010

Respectfully submitted,
COOLEY GODWARD KRONISH LLP

By: _____
Cliff Z. Liu
Reg. No. 50,834

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777 6th Street NW, Suite 1100
Washington, DC 20001

Tel: (650) 843-5852
Fax: (202) 842-7899

Electronic Acknowledgement Receipt

EFS ID:	7279845
Application Number:	12504534
International Application Number:	
Confirmation Number:	1286
Title of Invention:	MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNDIRECTIONAL SERIAL BIT CHANNELS
First Named Inventor/Applicant Name:	William W. Y. Chu
Customer Number:	58249
Filer:	Cliff Z. Liu/Kathleen Smith
Filer Authorized By:	Cliff Z. Liu
Attorney Docket Number:	ACQI-010/10US 310578-2052
Receipt Date:	24-MAR-2010
Filing Date:	16-JUL-2009
Time Stamp:	18:56:25
Application Type:	Utility under 35 USC 111(a)

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Corrected Filing Receipt	12504534ReqUpdatedFR.pdf	46518 fad27a97c91d8923125e4b6022b2fb84835e7bae	no	1

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
12/504,534	07/16/2009	2111	2160	ACQI-010/10US 310578-2052	43	13

CONFIRMATION NO. 1286

UPDATED FILING RECEIPT

58249
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Applicant(s)

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Power of Attorney: The patent practitioners associated with Customer Number 58249

Domestic Priority data as claimed by applicant

This application is a CON of 12/077,503 03/18/2008 PAT 7,676,624
which is a CON of 11/166,656 06/24/2005 PAT 7,376,779
which is a CON of 11/097,694 03/31/2005 PAT 7,363,415
which is a CON of 10/772,214 02/03/2004 PAT 7,099,981
which is a CON of 09/569,758 05/12/2000 PAT 6,718,415
which claims benefit of 60/134,122 05/14/1999

Foreign Applications

If Required, Foreign Filing License Granted: 07/27/2009

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/504,534**

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Early Publication Request: No
** **SMALL ENTITY** **

Title

MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNDIRECTIONAL SERIAL BIT CHANNELS

Preliminary Class

710

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Title 37, Code of Federal Regulations, 5.11 & 5.15

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/504,534	07/16/2009	William W. Y. Chu	ACQI-010/10US 310578-2052

CONFIRMATION NO. 1286

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PUBLICATION NOTICE

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Title:MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNDIRECTIONAL SERIAL BIT CHANNELS

Publication No.US-2010-0174844-A1
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NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:	CHU, William W. Y.	Confirmation No.:	1286
Serial No.:	12/504,534	Group Art Unit:	2111
Filed:	July 16, 2009	Examiner:	Unassigned

For: MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNIDIRECTIONAL SERIAL BIT CHANNELS

Mail Stop: Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRELIMINARY AMENDMENT

Prior to examination of the above-identified application, please amend the subject application as follows:

Amendments to the Claims are reflected in the listing of the claims which begins on page 2 of this paper.

Remarks begin on page 20 of this paper.

The Director is hereby authorized to charge any appropriate fees under 37 C.F.R. §§1.16, 1.17, and 1.21 that may be required by this paper, and to credit any overpayment, to Deposit Account No. 50-1283.

IN THE CLAIMS

1. (Original) A computer system comprising:

a console comprising

a plurality of coupling sites,

a serial communication hub controller, and

an enclosure housing the coupling sites and the serial communication hub controller; and

a plurality of computer modules coupled to respective ones of the coupling sites, at least one of the computer modules comprising

a processing unit,

a main memory coupled to the processing unit,

a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels to transmit data in opposite directions,

a serial controller coupled to the serial communication hub controller, and

a first interface controller coupled to the LVDS channel to communicate an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction.

2. (Original) The computer system of claim 1, wherein the computer modules are similar in design to each other.

3. (Original) The computer system of claim 1, wherein the console further comprises a second interface controller to communicate with the at least one of the computer modules through the LVDS channel.

4. (Original) The computer system of claim 1, wherein the console further comprises a hard disk drive coupled to the at least one of the computer modules.

5. (Original) A computer system comprising:

a console comprising

a plurality of coupling sites, and

an enclosure housing the coupling sites; and

a plurality of computer modules coupled to respective ones of the coupling sites, each of the computer modules comprising

a processing unit,

a main memory coupled to the processing unit,

a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels in opposite directions,

an Ethernet controller to communicate with an external network, and

a first interface controller coupled to the LVDS channel to communicate an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction.

6. (Original) The computer system of claim 5, wherein the computer modules are similar in design to each other.

7. (Original) The computer system of claim 5, wherein the console further comprises a second interface controller to communicate with the first interface controller of at least one of the computer modules through the LVDS channel of the at least one of the computer modules.

8. (Original) The computer system of claim 5, wherein the console further comprises an Ethernet hub controller coupled to the Ethernet controller of at least one of the computer modules to communicate with the external network.

9. (Original) A computer system comprising:

a console comprising

a plurality of coupling sites, each of the coupling sites comprising a slot,

a power supply, and

an enclosure housing the coupling sites and the power supply; and

a plurality of computer modules, each of the computer modules coupled to a respective one of the coupling sites through the slot of the respective one of the coupling sites, each of the computer modules comprising

a processing unit,

a main memory coupled to the processing unit,

a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels in opposite directions, and

an interface controller coupled to the LVDS channel to transmit encoded Peripheral Component Interconnect (PCI) bus transaction data,

wherein the computer modules receive power from the power supply upon coupling to the console.

10. (Original) The computer system of claim 9, wherein the computer modules are similar in design to each other.

11. (Original) The computer system of claim 9, wherein at least one of the computer modules further comprises an Ethernet controller to communicate with an external network.

12. (Original) The computer system of claim 9, wherein the console further comprises a mass storage device that is shared between the computer modules.

13. (Original) A computer system comprising:

a console comprising

a plurality of coupling sites,

a power supply,

a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels in opposite directions,

an interface controller coupled to the LVDS channel to communicate an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction, and

an enclosure housing the coupling sites, the power supply, the LVDS channel, and the interface controller; and

a computer module coupled to one of the coupling sites and comprising

a processing unit,

a main memory coupled to the processing unit, and

a mass storage device coupled to the processing unit,

wherein the computer module receives power from the power supply for operation.

14. (Original) The computer system of claim 13, wherein the mass storage device comprises a flash memory.

15. (Original) The computer system of claim 13, wherein the computer module further comprises a serial controller coupled to the console for data communication.

16. (Original) A computer system comprising:

a console comprising

a plurality of coupling sites, each of the coupling sites comprising a connector,

a pair of unidirectional, multiple serial bit, low voltage differential signal (LVDS) channels to transmit encoded Peripheral Component Interconnect (PCI) bus transaction data in opposite directions, and

an enclosure housing the coupling sites and the LVDS channels; and

a computer module coupled to one of the coupling sites through the connector of the one of the coupling sites, the computer module comprising

a processing unit,

a main memory coupled to the processing unit,

a mass storage device comprising a flash memory, and

a serial communication controller,

wherein the serial communication controller is coupled to the console for data communication upon coupling of the computer module to the console.

17. (Original) The computer system of claim 16, wherein the data communication of the serial communication controller comprises Universal Serial Bus (USB) communication.

18. (Original) The computer system of claim 16, wherein the computer module further comprises a computing environment for a personal computer user.

19. (Original) A computer system comprising:

a console comprising

a plurality of coupling sites, at least one of the coupling sites comprising a connector,

a Digital Versatile Disk (DVD) drive,

a first differential signal channel comprising a pair of unidirectional, serial bit channels to transmit data in opposite directions, and

an enclosure housing the coupling sites, the DVD drive, and the first differential signal channel; and

a computer module coupled to the at least one of the coupling sites through the connector, the computer module comprising

a processing unit,

a main memory coupled to the processing unit,

a mass storage device comprising a flash memory,

a second differential signal channel comprising a pair of unidirectional, serial bit channels to transmit data in opposite directions, and

an interface controller coupled to the console through the second differential signal channel and the connector,

wherein the first differential signal channel and the second differential signal channel are coupled to each other upon insertion of the computer module into the console.

20. (Original) The computer system of claim 19, wherein the computer module further comprises a computing environment for a personal computer user.

21. (Original) The computer system of claim 19, wherein the console further comprises a power supply, and the computer module receives power from the power supply upon insertion of the computer module into the console.

22. (Original) A computer system comprising:

a console comprising

a plurality of coupling sites, each of the coupling sites comprising a connector,

a power supply,

an integrated Liquid Crystal Display (LCD),

a first differential signal channel comprising a pair of unidirectional, serial bit channels to transmit data in opposite directions, and

an enclosure housing the coupling sites, the power supply, the LCD, and the first differential signal channel; and

a computer module coupled to one of the coupling sites through the connector of the one of the coupling sites, the computer module comprising

a processing unit,

a main memory coupled to the processing unit,

a mass storage device comprising a flash memory, and

a second differential signal channel comprising a pair of unidirectional, serial bit channels to transmit data in opposite directions,

wherein the first differential signal channel and the second differential signal channel are coupled to each other upon insertion of the computer module into the console, and the computer module is at least partially powered by the power supply for operation.

23. (Original) The computer system of claim 22, wherein the computer module further comprises a computing environment for a personal computer user.

24. (Original) The computer system of claim 22, wherein the console further comprises a Digital Versatile Disk (DVD) drive.

25. (Original) A computer system comprising:

a console comprising

a plurality of coupling sites, each of the coupling sites comprising a connector, and

a first pair of unidirectional, multiple bit, low voltage differential signal (LVDS) channels to transmit encoded Peripheral Component Interconnect (PCI) bus transaction as serial data along a pair of directions that are different from each other; and

a computer module coupled to one of the coupling sites through the connector of the one of the coupling sites, the computer module comprising

a processing unit,

a main memory coupled to the processing unit,

a mass storage device coupled to the processing unit,

a second pair of unidirectional, multiple bit, LVDS channels to transmit encoded PCI bus transaction as serial data along a pair of directions that are different from each other, and

an interface controller coupled to the second pair of LVDS channels,

wherein the interface controller is coupled to the console for data communication upon coupling of the computer module to the console.

26. (Original) The computer system of claim 25, wherein the console further comprises a Digital Versatile Disk (DVD) drive.

27. (Original) The computer system of claim 25, wherein the computer module further comprises a password mechanism to control access to the computer module.

28. (Original) A computer system comprising:

a console comprising

a plurality of coupling sites, each of the coupling sites comprising a slot,

a mass storage device, and

an enclosure housing the coupling sites and the mass storage device; and

a plurality of computer modules, each of the computer modules coupled to a respective one of the coupling sites through the slot of the respective one of the coupling sites, each of the computer modules comprising

a processing unit,

a main memory coupled to the processing unit,

a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels in opposite directions,

a serial communication controller, and

an interface controller coupled to the LVDS channel to transmit encoded Peripheral Component Interconnect (PCI) bus transaction data,

wherein the computer modules are similar in design to each other, and wherein the mass storage device is coupled to the computer modules during operation.

29. (Original) The computer system of claim 28, wherein the serial communication controller of at least one of the computer modules is coupled to the console for data communication.

30. (Original) The computer system of claim 28, wherein the console further comprises a power supply to supply power to the computer modules.

31. (Original) A computer system comprising:

a console comprising

a plurality of coupling sites, each of the coupling sites comprising a slot,

a mass storage device, and

an enclosure housing the coupling sites and the mass storage device; and

a plurality of computer modules, each of the computer modules coupled to a respective one of the coupling sites through the slot of the respective one of the coupling sites, at least one of the computer modules comprising

a processing unit,

a main memory coupled to the processing unit,

a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels in opposite directions,

a serial communication controller, and

an interface controller coupled to the LVDS channel to transmit encoded Peripheral Component Interconnect (PCI) bus transaction data,

wherein the computer modules are similar in design to each other, and wherein the at least one of the computer modules is configured to provide protection against failure of another one of the computer modules.

32. (Original) The computer system of claim 31, wherein the serial communication controller of the at least one of the computer modules is coupled to the console for data communication.

33. (Original) The computer system of claim 31, wherein the mass storage device is coupled to the computer modules upon insertion of the computer modules into the console.

34. (Original) A computer system comprising:

a plurality of coupling sites;

a power supply;

a low voltage differential signal (LVDS) channel associated with at least one of the coupling sites, the LVDS channel comprising two sets of unidirectional, multiple serial bit channels in opposite directions;

a first interface controller associated with the at least one of the coupling sites and coupled to the LVDS channel to communicate an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction; and

a plurality of computer modules coupled to respective ones of the coupling sites, at least one of the computer modules comprising

a processing unit,

a main memory coupled to the processing unit, and

a second interface controller coupled to the first interface controller through the LVDS channel,

wherein the computer modules receive power from the power supply for operation.

35. (Original) The computer system of claim 34, wherein at least one of the computer modules further comprises an Ethernet controller to communicate with an external network.

36. (Original) The computer system of claim 34, wherein the computer system further comprises a mass storage device that is shared between the computer modules.

37. (Original) A computer system comprising:

a console comprising

a first coupling site,

a second coupling site,

a power supply,

a first low voltage differential signal (LVDS) channel associated with the first coupling site, the first LVDS channel comprising two sets of unidirectional, multiple serial bit channels in opposite directions,

a second LVDS channel associated with the second coupling site, the second LVDS channel comprising two sets of unidirectional, multiple serial bit channels in opposite directions,

a first interface controller coupled to at least one of the first LVDS channel and the second LVDS channel to communicate an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction, and

an enclosure housing the first coupling site, the second coupling site, the power supply, the first LVDS channel, the second LVDS channel, and the first interface controller.

38. (Original) The computer system of claim 37, further comprising:

a first computer module coupled to the first coupling site; and

a second computer module coupled to the second coupling site,

wherein at least one of the first computer module and the second computer module comprises

a processing unit,

a main memory coupled to the processing unit, and

a second interface controller to communicate with the console through one of the first LVDS channel and the second LVDS channel.

39. (Original) The computer system of claim 38, wherein each of the first computer module and the second computer module receives power from the power supply for operation.

40. (Original) A computer system comprising:

a console comprising

a coupling site,

a power supply,

a first low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels in opposite directions to communicate an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction,

a second differential channel associated with the coupling site, the second differential channel comprising two sets of unidirectional, serial bit channels in opposite directions,

a first interface controller coupled to the second differential channel, and

an enclosure housing the coupling site, the power supply, the first LVDS channel, the second differential channel, and the first interface controller.

41. (Original) The computer system of claim 40, further comprising:

a computer module coupled to the coupling site,

wherein the computer module comprises

a processing unit,

a main memory coupled to the processing unit, and

a second interface controller to communicate, via Universal Serial Bus (USB) communication, with the console through the second differential channel.

42. (Original) The computer system of claim 41, wherein the computer module receives at least partial power from the power supply of the console for operation upon coupling to the console.

43. (Original) The computer system of claim 41, wherein the computer module further comprises a computing environment for a personal computer user.

44. (New) A computer module insertable into a coupling site of a console for data communication, comprising:

a main circuit board;

a processing unit coupled to the main circuit board;

a main memory coupled to the processing unit;

a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels to transmit data in opposite directions for communicating an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction; and

an interface controller coupled to the LVDS channel.

45. (New) The computer module of claim 44, further comprising a removable hard disk drive.

46. (New) The computer module of claim 44, further comprising a serial communication controller to couple to the console for data communication.

47. (New) The computer module of claim 46, wherein the data communication of the serial communication controller comprises Ethernet communication.

48. (New) The computer module of claim 46, wherein the data communication of the serial communication controller comprises Universal Serial Bus (USB) communication.

49. (New) The computer module of claim 44, wherein the computer module is configured to operate upon receiving power from the console.

50. (New) The computer module of claim 44, further comprising an enclosure housing the main circuit board, the processing unit, the main memory, the LVDS channel, and the interface controller, and the enclosure is insertable into the coupling site of the console.

51. (New) The computer module of claim 44, further comprising a connector distinct from the main circuit board, and the connector is configured to couple to the coupling site of the console for data communication.

52. (New) The computer module of claim 51, wherein the interface controller is configured to communicate the encoded serial bit stream of PCI bus transaction through the LVDS channel and the connector.

53. (New) A computer module comprising:

an enclosure insertable into a slot of a console for guidance to a first connector of the console for operation;

a processing unit housed in the enclosure;

a main memory coupled to the processing unit and housed in the enclosure;

an Ethernet controller coupled to the processing unit and housed in the enclosure;

a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels to transmit data in opposite directions;

a second connector configured to couple to the first connector of the console; and

an interface controller housed in the enclosure and coupled to the second connector through the LVDS channel for communicating an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction.

54. (New) The computer module of claim 53, wherein the Ethernet controller is configured to couple to the first connector of the console for data communication.

55. (New) The computer module of claim 54, wherein the Ethernet controller is coupled to the second connector.

56. (New) The computer module of claim 54, wherein the Ethernet controller is configured to communicate with an external network through the console.

57. (New) The computer module of claim 53, wherein the computer module is configured to operate only upon receiving power from the console.

58. (New) The computer module of claim 53, wherein the enclosure defines a set of grooves to engage a corresponding set of rails of the slot of the console.

59. (New) A computer module comprising:

a main circuit board;

a first connector distinct from the main circuit board;

a processing unit coupled to the main circuit board;

a main memory coupled to the processing unit;

a hard disk drive coupled to the processing unit;

a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels to transmit data in opposite directions; and

an interface controller coupled to the LVDS channel and the first connector for communicating an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction,

wherein the computer module is configured to engage rails on opposite sides of a slot of a console for guidance towards a second connector of the console.

60. (New) The computer module of claim 59, wherein the LVDS channel is configured to couple to the console.

61. (New) The computer module of claim 59, wherein the first connector of the computer module is configured to mate with the second connector of the console upon the computer module being inserted into the console for operation.

62. (New) The computer module of claim 61, wherein the LVDS channel is configured to couple to the console through the first connector of the computer module and the second connector of the console.

63. (New) A computer module comprising:

a processing unit;

a main memory coupled to the processing unit;

a mass storage device coupled to the processing unit;

a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels to transmit data in opposite directions for communicating an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction; and

a serial communication controller configured to couple to a console,

wherein the computer module is insertable into a slot of the console for guidance to a connector of the console for serial data communication.

64. (New) The computer module of claim 63, wherein the mass storage device comprises a SCSI hard disk drive.

65. (New) The computer module of claim 63, wherein the computer module is configured to operate only upon receiving power from the console.

66. (New) The computer module of claim 63, wherein the serial communication controller comprises an Ethernet controller to communicate with an external network through the console.

67. (New) A console to couple to a plurality of computer modules to form a server system, comprising:

a first coupling site to couple to a first computer module;

a second coupling site to couple to a second computer module;

a power supply coupled to at least one of the first coupling site and the second coupling site;

a printed circuit board;

a first low voltage differential signal (LVDS) channel coupled to the printed circuit board and comprising two sets of unidirectional, multiple serial bit channels in opposite directions;

a second LVDS channel coupled to the printed circuit board and comprising two sets of unidirectional, multiple serial bit channels in opposite directions; and

an enclosure housing the first coupling site, the second coupling site, the power supply, the first LVDS channel, the second LVDS channel, and the printed circuit board.

68. (New) The console of claim 67, further comprising a first interface controller coupled to at least one of the first LVDS channel and the second LVDS channel to communicate an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction.

69. (New) The console of claim 68, wherein at least one of the first computer module and the second computer module comprises a second interface controller, and the first interface controller is configured to couple to the second interface controller.

70. (New) The console of claim 67, wherein the power supply is configured to provide power to each of the first computer module and the second computer module for operation.

71. (New) The console of claim 67, further comprising a hard disk drive configured to couple to at least one of the first computer module and the second computer module.

72. (New) The console of claim 67, further comprising an Ethernet hub controller configured to couple to at least one of the first computer module and the second computer module for communication with an external network.

73. (New) A console to couple to a plurality of computer modules to form a server system, comprising:

a first coupling site to couple to a first computer module;

a second coupling site to couple to a second computer module;

a power supply;

a printed circuit board coupled to the first coupling site and the second coupling site;

a serial communication hub controller coupled to the printed circuit board;

a low voltage differential signal (LVDS) channel associated with at least one of the first coupling site and the second coupling site, the LVDS channel comprising two sets of unidirectional, multiple serial bit channels in opposite directions for communicating an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction; and

an enclosure housing the first coupling site, the second coupling site, the power supply, the printed circuit board, the serial communication hub controller, and the LVDS channel.

74. (New) The console of claim 73, wherein each of the first coupling site and the second coupling site comprises a slot and a connector.

75. (New) The console of claim 73, further comprising an interface controller housed in the enclosure and coupled to the LVDS channel to communicate the encoded serial bit stream of PCI bus transaction.

76. (New) The console of claim 73, further comprising an integrated display device.

77. (New) The console of claim 73, wherein the serial communication hub controller comprises a multi-port, serial communication hub controller to support communication between the first computer module and the second computer module and with an external network.

78. (New) The console of claim 73, further comprising a storage subsystem housed in the enclosure and shared by the first computer module and the second computer module.

79. (New) The console of claim 73, wherein the power supply is configured to provide power to each of the first computer module and the second computer module for operation.

80. (New) A server comprising:

a processing unit;

a main memory coupled to the processing unit;

a mass storage device coupled to the processing unit;

a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels to transmit data in opposite directions for communicating an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction; and

an interface controller coupled to the LVDS channel;

wherein the processing unit is configured to couple to an external network through the LVDS channel.

81. (New) The server of claim 80, further comprising an Ethernet controller coupled to the LVDS channel.

82. (New) A server comprising:

a processing unit;

a main memory coupled to the processing unit;

a SCSI hard disk drive coupled to the processing unit;

a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels to transmit data in opposite directions for communicating an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction; and

an interface controller coupled to the LVDS channel;

wherein the processing unit is coupled to the interface controller for data communication with an external Ethernet network.

83. (New) The server of claim 82, further comprising an Ethernet controller coupled to the LVDS channel.

REMARKS

Claims 1-43 were pending in the subject application. New claims 44-83 are added by this preliminary amendment. Support for the new claims can be found in figures and text of the subject application as filed. No new matter has been added.

Entry of the foregoing amendments is respectfully requested.

Date: 8/13/10

Respectfully submitted,
COOLEY LLP

By: _____
Cliff Z. Liu
Reg. No. 50,834

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Electronic Patent Application Fee Transmittal

Application Number:	12504534
Filing Date:	16-Jul-2009
Title of Invention:	MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNDIRECTIONAL SERIAL BIT CHANNELS
First Named Inventor/Applicant Name:	William W. Y. Chu
Filer:	Cliff Z. Liu/Kathleen Smith
Attorney Docket Number:	ACQI-010/10US 310578-2052

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Claims in excess of 20	1202	40	52	2080
Independent claims in excess of 3	1201	8	220	1760
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**3840**

Electronic Acknowledgement Receipt

EFS ID:	8220505
Application Number:	12504534
International Application Number:	
Confirmation Number:	1286
Title of Invention:	MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNDIRECTIONAL SERIAL BIT CHANNELS
First Named Inventor/Applicant Name:	William W. Y. Chu
Customer Number:	58249
Filer:	Cliff Z. Liu/Kathleen Smith
Filer Authorized By:	Cliff Z. Liu
Attorney Docket Number:	ACQI-010/10US 310578-2052
Receipt Date:	13-AUG-2010
Filing Date:	16-JUL-2009
Time Stamp:	20:03:27
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$3840
RAM confirmation Number	4937
Deposit Account	501283
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		12504534PreliminaryAmd13Aug10.pdf	1035974 80cfbd8b1a51056cbbc002b74ebb97aaf7345b3b	yes	20

Multipart Description/PDF files in .zip description		
Document Description	**Start**	**End**
Preliminary Amendment	1	1
Claims	2	19
Applicant Arguments/Remarks Made in an Amendment	20	20

Warnings:

Information:

2	Fee Worksheet (PTO-875)	fee-info.pdf	32488 90de707dab37a7e956b82569ce14c121d4ee1fd6	no	2

Warnings:

Information:

Total Files Size (in bytes):	1068462

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
12/504,534	07/16/2009	

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY ☒ RATE ($)	SMALL ENTITY ☒ FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT 08/13/2010	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 83	Minus	** 43	= 40	X $26 =	1040	OR	X $ =	
Independent (37 CFR 1.16(h))	* 21	Minus	***13	= 8	X $110 =	880	OR	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE	1920	OR	TOTAL ADD'L FEE	

AMENDMENT	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)	OR	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/MARY PEOPLES/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/504,534	07/16/2009	William W. Y. Chu	ACQI-010/10US 310578-2052	1286

58249 7590 10/28/2010

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EXAMINER	
PHAN, RAYMOND NGAN	
ART UNIT	**PAPER NUMBER**
2111	

MAIL DATE	DELIVERY MODE
10/28/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	12/504,534	CHU, WILLIAM W. Y.	
	Examiner	Art Unit	
	RAYMOND N. PHAN	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-83* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *19-27,34-43 and 67-72* is/are allowed.

6)☒ Claim(s) *1-18,28-33,44-66 and 73-83* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *092909/010510/031910/031910*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Part III DETAILED ACTION

Notice to Applicant(s)

1. This application has been examined. Claims 1-83 are pending.

2. The Group and/or Art Unit location of your application in the PTO has changed. To aid in correlating any papers for this application, all further correspondence regarding this application should be directed to Group Art Unit 2111.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321© may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 1, 5, 28 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 39 in Patent

No. 7,818,487. Although the conflicting claims are not identical, they are not patentably distinct from each other because the omission/different of wordings,

multiple serial bit channel,

serial communication hub controller,

wherein each of the computer module can operate fully independent of each other,

in claims 1, 5, 28 are obvious expedients since elements of claims 1, 5, 28 of the present application still perform the same functions,

A computer system comprising: a console comprising a first coupling site, and a second coupling site, each coupling site comprising a connector, the console being an enclosure housing each coupling site, a hard disk drive and a low voltage differential signal (LVDS) channel comprises two sets of unidirectional serial bit channels which transmit data in opposite directions; and a plurality of computer modules, each computer module coupled to one of the coupling site through the connector, comprising

a processing unit,

a main memory coupled to the processing unit, and

an Ethemet controller coupled to the connector of the coupling site for communication to an external network through the console,

as claim 39 of the patent. In re Karlson, 136 USPQ 189 (ccPA 1963).

6. Claims 9 and 13 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 6 in Patent No. 7,818,487. Although the conflicting claims are not identical, they are not patentably distinct from each other because the omission/different of wordings,

multiple serial bit channel,

wherein the computer modules receive power from the power supply upon coupling to the console,

in claims 9, 13 are obvious expedients since elements of claims 9, 13 of the present application still perform the same functions,

A computer system comprising: a console comprising a power supply, a first coupling site and a second coupling site, each coupling site comprising a connector, the console being a first enclosure housing the coupling sites, the power supply and a low voltage differential signal channel (LVDS) comprises two sets of unidirectional, serial bit channels which transmit encoded PCI bus transaction data in opposite directions; a computer module coupled to one of the coupling sitessite through the connector, comprising a second enclosure, a processing unit, a serial communication controller coupled to the connector of the coupling site for communication to the console, and a flash memory storage device coupled to the processing unit; wherein the power supply supplies power to the computer module,

as claim 6 of the patent. In re Karlson, 136 USPQ 189 (ccPA 1963).

7. Claims 31 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 26 in Patent No. 7,818,487. Although the conflicting claims are not identical, they are not patentably distinct from each other because the omission/different of wordings,

multiple serial bit channel,

an Ethernet controller coupled to the processing unit and coupling site for communication to the external network through the console,

in claims 31, are obvious expedients since elements of claims 31, of the present application still perform the same functions,

A computer system comprising: a console comprising a first coupling site, and a second coupling site, each coupling site comprising a connector, the console being an enclosure housing each coupling site, a hard disk drive and a low voltage differential signal (LVDS) channel comprises two sets of unidirectional serial bit channels which transmit data in opposite directions; and a plurality of computer modules, each computer module coupled to one of the coupling site through the connector, comprising a processing unit, a main memory coupled to the processing unit, and an Ethernet controller coupled to the connector of the coupling site for communication to an external network through the console; and wherein each of the computer modules is similar in design to each other and operates fully independent of each other,

as claim 26 of the patent. In re Karlson, 136 USPQ 189 (ccPA 1963).

8. Claims 44, 73, 80, 82 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 36 in Patent No. 7,818,487. Although the conflicting claims are not identical, they are not patentably distinct from each other because the omission/different of wordings,

multiple serial bit channel,

wherein each of the computer modules is similar in design to each other and operates fully independent of each other,

in claims 44, 73, 80, 82 are obvious expedients since elements of claims 44, 73, 80, 82 of the present application still perform the same functions,

> A computer system comprising: a console comprising a first coupling site and a second coupling site, each coupling site comprising a connector; the console being an enclosure housing each coupling site, and a low voltage differential signal (LVDS) channel comprises two sets of unidirectional multiple serial bit channels which can transmit encoded Peripheral Component Interconnect (PCI) bus transaction data in opposite directions; a plurality of computer modules, each computer module coupled to one of the coupling sites through the connector, and comprising
> a processing unit, and
> a main memrory coupled to the processing unit,
> wherein one of the computer modulesmodute couples to the LVDS channel for data communication,

as claim 36 of the patent. In re Karlson, 136 USPQ 189 (ccPA 1963).

9. Claims 53 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 26 in Patent No. 7,676,624. Although the conflicting claims are not identical, they are not patentably distinct from each other because the omission/different of wordings,

> multiple serial bit channel,
> a second connector configured to couple to the first connector of the console, coupled to the second connector,
> wherein each of the computer modules is similar in design to each other and operates fully independent of each other,

in claims 53, are obvious expedients since elements of claims 53, of the present application still perform the same functions,

> A computer system comprising: a console comprising a first coupling site and a second coupling site, each coupling site comprising a connector and a slot, the console being an enclosure housing the coupling sites; a plurality of computer modules, each computer module coupled to one of the coupling sites through the connector and the slot, comprising a processing unit, a main memory coupled to the processing unit, a low voltage differential signal (LVDS) channel comprising two sets of unidirectional multiple serial bit channels which transmit data in opposite directions, an Ethernet controller coupled to the connector of the coupling site for communication to an external network through the console, and a first interface controller coupled the LVDS channel for communicating anencoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction,

as claim 26 of the patent. In re Karlson, 136 USPQ 189 (ccPA 1963).

10. Claims 59 and 63 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 53 in Patent No. 7,818,487. Although the conflicting claims are not identical, they are not patentably distinct from each other because the omission/different of wordings,

> a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels to transmit data in opposite directions, and

an interface controller coupled to the LVDS channel and the first connector for communicating an encoded serial bit stream Peripheral Component Interconnect bus transaction,

wherein each of the computer modules is similar in design to each other and operates fully independent of each other,

in claims 59 and 63 are obvious expedients since elements of claims 59 and 63 of the present application still perform the same functions,

A computer system comprising: a console comprising a power supply, a plurality of coupling sites, and an Ethemet hub controller configured to couple to an external network, each of the coupling sites comprising a connector and a slot, the coupling sites comprising a first coupling site and a second coupling site, the console being an enclosure comprising internal power and data connections to each of the coupling sites, the enclosure housing the power supply, the coupling sites, and the Ethernet hub controller; and a plurality of computer modules configured to couple to respective ones of the coupling sites, each of the computer modules being an assembly comprising a main circuit board and a connector that is distinct from the main circuit board and that is configured to couple to a respective one of the connectors of the coupling sites for power and data communication, each of the computer modules comprising

a processing unit,

a main memory coupled to the processing unit, and

an Ethernet controller configured to couple to the Ethernet hub controller through a respective one of the connectors of the coupling sites for data communication between the computer modules and to the external network,

wherein the computer modules comprise a first computer module, configured to couple to the first coupling site, and a second computer module, configured to couple to the second coupling site, the slot of the first coupling site configured to receive the first computer module and to guide the first computer module to the connector of the first coupling site, the slot of the second coupling site configured to receive the second computer module and to guide the second computer module to the connector of the second coupling site,

as claim 53 of the patent. In re Karlson, 136 USPQ 189 (ccPA 1963).

Allowable Subject Matter

11. Claims 19-27, 34-43, 67-72 are allowable over the prior of records.

12. The following is an Examiner's statement of reasons for the indication of allowable subject matter: Claim 1 is allowable over the prior art of record because the prior arts, cited in its entirety, or in combination, do not teach first a first differential signal channel comprising a pair of unidirectional, serial bit channels to transmit data in opposite directions, second differential signal channel comprising a pair of unidirectional, serial bit channels to transmit data in opposite directions, and wherein the first differential signal channel and the second differential signal channel are coupled to each other upon insertion of the computer module into the console (claims 19, 34. 37, 40, 67);

first a first differential signal channel comprising a pair of unidirectional, serial bit channels to transmit data in opposite directions, second differential signal channel comprising a pair of unidirectional, serial bit channels to transmit data in opposite directions, and wherein the first differential signal channel and the second differential signal channel are coupled to each other upon insertion of the computer

module into the console and the computer module is at least partially powered by the power supply for operation (claim 22);

a first pair of unidirectional, multiple bit, low voltage differential signal (LVDS) channels to transmit encoded Peripheral Component Interconnect (PCI) bus transaction as serial data along a pair of directions that are different from each other; a second pair of unidirectional, multiple bit, LVDS channels to transmit encoded PCI bus transaction as serial data along a pair of directions that are different from each other (claim 25).

Conclusion

13. Claims 1-18, 28-33, 44-66, 73-83 are rejected. Claims 19-27, 34-43, 67-72 are allowed.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Raymond Phan, whose telephone number is (571) 272-3630. The examiner can normally be reached on Monday-Friday from 6:30AM- 4:00PM. The Group Fax No (571) 273-8300.

Communications via Internet e-mail regarding this application, other than those under 35 U.S.C. 132 or which otherwise require a signature, may be used by the applicant and should be addressed to [**raymond.phan@uspto.gov**].

All Internet e-mail communications will be made of record in the application file. PTO employees do not engage in Internet communications where there exists a possibility that sensitive information could be identified or exchanged unless the record includes a properly signed express waiver of the confidentiality requirements of 35 U.S.C. 122. This is more clearly set forth in the Interim Internet Usage Policy published in the Official Gazette of the Patent and Trademark on February 25, 1997 at 1195 OG 89.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 central telephone number is (571) 272-2100.

/RAYMOND N PHAN/
Primary Examiner, Art Unit 2111

Notice of References Cited	Application/Control No. 12/504,534	Applicant(s)/Patent Under Reexamination CHU, WILLIAM W. Y.	
	Examiner RAYMOND N. PHAN	Art Unit 2111	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-7,818,487	10-2010	Chu, William W. Y.	710/313
*	B	US-7,676,624	03-2010	Chu, William W. Y.	710/313
	C	US-			
	D	US-			
	E	US-			
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FOREIGN PATENT DOCUMENTS

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CONFIRMATION NO. 1286

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
12/504,534	07/16/2009	710	2111	ACQI-010/10US 310578-2052

APPLICANTS

William W. Y. Chu, Los Altos, CA;

**** CONTINUING DATA ***************************

This application is a CON of 12/077,503 03/18/2008 PAT 7,676,624
which is a CON of 11/166,656 06/24/2005 PAT 7,376,779
which is a CON of 11/097,694 03/31/2005 PAT 7,363,415
which is a CON of 10/772,214 02/03/2004 PAT 7,099,981
which is a CON of 09/569,758 05/12/2000 PAT 6,718,415
which claims benefit of 60/134,122 05/14/1999

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED **** ** SMALL ENTITY **
07/27/2009

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /Raymond Ngan Phan/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		CA	24	43	13

ADDRESS

COOLEY LLP
ATTN: Patent Group
Suite 1100
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WASHINGTON, DC 20001
UNITED STATES

TITLE

MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNDIRECTIONAL SERIAL BIT CHANNELS

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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12504534	CHU, WILLIAM W. Y.
	Examiner	Art Unit
	RAYMOND N PHAN	2111

SEARCHED

Class	Subclass	Date	Examiner
710	300-317,62-64,72-74	1021/10	RP
709	214-219,226-227	10/21/10	RP
714	43-44, 11, 13	10/21/10	RP

SEARCH NOTES

Search Notes	Date	Examiner
EAST Search	10/22/10	RP

INTERFERENCE SEARCH

Class	Subclass	Date	Examiner

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /R.P./

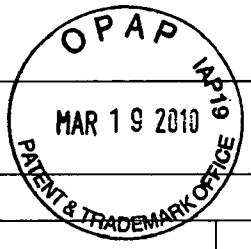
Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

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U.S.PATENTS

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FOREIGN PATENT DOCUMENTS

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	Attorney Docket Number	ACQI-010/10US 310578-2052

	1	Ziatech Corporation-Ketris9000 Product Manual (2000) (159 pp.) (No. 18.pdf)	☐
	2	Ziatech Corp. ZT 8907 Product Description (1998) (4 pp) (No. 19b.pdf)	☐
	3	Ziatech Corp. ZT 8908 Product Description (1998)+A249 (6 pp) (No. 19c.pdf)	☐
	4	Ziatech Corp. System Designer's Guide: Hot Swap Capability on STD 32 Computers (Jan. 1996) (6 pp) (No. 19e.pdf)	☐
	5	Ziatech Corp. Press Release (Feb. 1996) (2 pp.) (No. 19i.pdf)	☐
	6	Ziatech Corp. Industrial BIOS for CompacktPCI and STD 32 Systems Software Manual (July 1998) (134 pp) No. 19h.pdf)	☐
	7	Ziatech Corp.System Designers Guide: Expanding STD Bus Performance Through Multiprocessing. (Apr. 1996) (6 pp.) (No. 19d.pdf)	☐
	8	Ziatech, STD 32 Star System Product Description(6 pp) (No. 19a.pdf)	☐
	9	Ziatech Corp. zVID2 Local Bus Super VGA/FPD Adapter Product Description (2 pp) (Apr. 1996) (No. 19f.pdf)	☐

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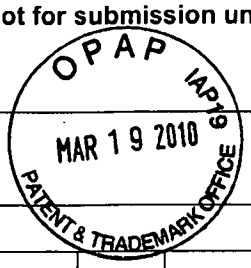
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Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
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U.S.PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	4228496		1980-10-14	Katzman et al.	
	2	4453215		1984-06-05	Reid	
	3	4680674		1987-07-14	Moore	
	4	4760276		1988-07-26	Lethellier	
	5	4791524		1988-12-13	Teigen et al.	
	6	5187645		1993-02-16	Spalding et al.	
	7	5282247		1994-01-25	McLean et al.	
	8	5325517		1994-06-28	Baker et al.	

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	Attorney Docket Number	ACQI-010/10US 310578-2052

	9	5339408		1994-08-16	Bruckert et al.	
	10	5577205		1996-11-19	Hwang et al.	
	11	5430607		1995-07-04	Smith	
	12	5432939		1995-07-11	Blackledge Jr. et al.	
	13	5436902		1995-07-25	McNamara et al.	
	14	5533125		1996-07-02	Bensimon et al.	
	15	5537544		1996-07-16	Morisawa et al.	
	16	5552776		1996-09-03	Wade et al.	
	17	5588850		1996-12-31	Pan et al.	
	18	5673172		1997-09-30	Hastings et al.	
	19	5680536		1997-10-21	Tyuluman	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /R.P./

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	20	5708840		1998-01-13	Kikinis et al.	
	21	5724591		1998-03-03	Hara et al.	
	22	5737194		1998-04-07	Hopkins et al.	
	23	5774703		1998-06-30	Weiss et al.	
	24	5802391		1998-09-01	Hwang	
	25	5805903		1998-09-08	Elkhoury	
	26	5809262		1998-09-15	Potter	
	27	5884053		1999-03-16	Clouser et al.	
	28	5978821		1999-11-02	Freeny	
	29	5982614		1999-11-09	Reid	
	30	6049823		2000-04-11	Hwang	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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	Attorney Docket Number	ACQI-010/10US 310578-2052

	31	6070211		2000-05-30	Neal et al.	
	32	6078503		2000-06-20	Gallagher et al.	
	33	6091737		2000-07-18	Hong et al.	
	34	6145085		2000-11-07	Tran et al.	
	35	6188602		2001-02-13	Alexander et al.	
	36	6256691		2001-07-03	Moroz et al.	
	37	6297955		2001-10-02	Frank Jr. et al.	
	38	6311287		2001-10-30	Dischler et al.	
	39	6325636		2001-12-04	Hipp et al.	
	40	6411506		2002-06-25	Hipp et al.	
	41	6567877		2003-05-20	Lewis et al.	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /R.P./

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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	Examiner Name	
	Attorney Docket Number	ACQI-010/10US 310578-2052

	42	6581125		2003-06-17	Lange et al.	
	43	6715100		2004-03-30	Hwang	
	44	6747878		2004-06-08	Hipp et al.	
	45	6948047		2005-09-20	Maruska et al.	
	46	6985967		2006-01-10	Hipp	
	47	7017001		2006-03-21	Hill et al.	
	48	7020735		2006-03-28	Kikinis	
	49	7339786		2008-03-04	Bottom et al.	

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U.S.PATENT APPLICATION PUBLICATIONS

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FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	JP 7-04672			1995-03-10	Toshiba Corp.		☐
	2	JP 7-084675			1995-03-31	Hitachi Ltd.		☐
	3	JP 6-289956			1994-10-18	Hitachi Ltd.		☐
	4	WO 97/05618			1997-02-13	Memory Corporation		☐

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NON-PATENT LITERATURE DOCUMENTS

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	1	Acqis -v- Appro International, USDC-Eastern District of Texas (Tyler Div) Case No. 6:09-cv-148-LED Defendants' Amended Invalidity Contentions (March 1, 2010)	☐
	2	Acqis -v- Appro International, USDC-Eastern District of Texas (Tyler Div) Case No. 6:09-cv-148-LED EXHIBIT B-Defendants' Amended Invalidity Contentions (March 1, 2010)	☐
	3	Acqis -v- Appro International, USDC-Eastern District of Texas (Tyler Div) Case No. 6:09-cv-148-LED EXHIBIT C-Defendants' Amended Invalidity Contentions (March 1, 2010)	☐
	4	Acqis -v- Appro International, USDC-Eastern District of Texas (Tyler Div) Case No. 6:09-cv-148-LED EXHIBIT D-Defendants' Amended Invalidity Contentions (March 1, 2010)	☐

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	5	Acqis -v- Appro International, USDC-Eastern District of Texas (Tyler Div) Case No. 6:09-cv-148-LED EXHIBIT E-Defendants' Amended Invalidity Contentions (March 1, 2010)	☐
	6	Acqis -v- Appro International, USDC-Eastern District of Texas (Tyler Div) Case No. 6:09-cv-148-LED EXHIBIT F-Defendants' Amended Invalidity Contentions (March 1, 2010)	☐
	7	Acqis -v- Appro International, USDC-Eastern District of Texas (Tyler Div) Case No. 6:09-cv-148-LED APPENDIX 1-Defendants' Amended Invalidity Contentions (March 1, 2010)	☐
	8	Acqis -v- Appro International, USDC-Eastern District of Texas (Tyler Div) Case No. 6:09-cv-148-LED Defendants' Notice of Errata Re Invalidity Contentions (March 1, 2010)	☐
	9	ACCTON, Gigabit Ethernet PCI Adapter (1999) (2 pp) (No. 122.pdf)	☐
	10	AMD-K6-III Processor Data Sheet (1999) (326 pp) (No. 114.pdf)	☐
	11	Black Box Network Services "Welcome to the ServSwitch Family" (Jul. 1998) (52 pp) (No. 115.pdf)	☐
	12	Cisco AS5800 Universal Access Server Dial Shelf Controller Card Installation & Replacement (1997/1999) (28 pp) (No. 116.pdf)	☐
	13	CUBIX White paper: Benefits of High Density Servers (Jul. 2009) (6 pp) (Cubix-1.pdf)	☐
	14	Digital AlphaServer 4000 and 4100 Systems (1998) (4 pp) (No. 117.pdf)	☐
	15	EIA-422A - Standard (Superseded), Electrical Characteristics of Balanced Voltage Digital Interface Circuits (Dec. 1978) (20 pp) (No. 118a.pdf)	☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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	Examiner Name	
	Attorney Docket Number	ACQI-010/10US 310578-2052

	16	Grow et al. (XLNT Designs), "Gigabit Media Independent Interface Proposal," IEEE 802.z Vancouver (11 Nov 1996) (22 pp) (No. 124.pdf)	☐
	17	HP: HDMP-1636, Gigabit Ethernet Transceiver Chip, Preliminary Technical Data (May 1997) (No. 123.pdf)	☐
	18	Huq et al. "An Overview of LVDS Technology" National Semiconductor Corp. (Jul. 1998) (6 pp.) (No. 118d.pdf)	☐
	19	IBM 8260 ATM Product Architecture (Sept. 1997) (220 pp.) (No. 1.pdf)	☐
	20	IBM 8265 Nways ATM Switch Product Description (1994 / 1998) (144 pp.) (No. 2.pdf)	☐
	21	Intel Pentium II Processor Datasheet (Aug. 1998) (84 pp.) (No. 129.pdf)	☐
	22	Intel, 82559 Fast Ethernet Multifunction PCI/Cardbus Controller (Jan. 1999) (56 pp.) (No. 128.pdf)	☐
	23	Intel, 21143 PCI/CardBus 10/100Mb/s Ethernet LAN Controller, Product Datasheet (Oct. 1998) (8 pp.) (No. 127.pdf)	☐
	24	KTI Networks, Installation Guide 10/100 Dual-speed Fast Ethernet PCI Adapters (1999) (24 pp.) (No. 126.pdf).	☐
	25	Micronet SP2500R Series Etherfast 10/100 MBPS Adapter, User's Guide (1999) (10 pp.) (No. 136.pdf)	☐
	26	Miastkowski, Stan "A Whale of a System," Byte (Aug. 1991) pp. 39-40 (No. 35.pdf)	☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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	Examiner Name	
	Attorney Docket Number	ACQI-010/10US 310578-2052

	27	NEC Computer Systems: Server HX4500 User's Guide (Dec. 1998) (160 pp.) (No. 132.pdf)	☐
	28	Khan, Fasil "Ethernet Switch Card Design-Layout Specification, Rev. 2.00) (Aug 2001) (63 pp) (No. 26j.pdf)	☐
	29	PCI Local Bus Specification (Rev. 2.2, Dec. 1998) (322 pp.) (No. 135.pdf)	☐
	30	Sun Microsystems, Sun Enterprise 250 Server Owner's Guide (Jun. 1998) (324 pp.) (No. 137.pdf)	☐
	31	Sun Microsystems, UltraSPARC-II CPU Module Datasheet (Jul. 1999) (28 pp.) (No. 138.pdf)	☐
	32	Sun Microsystems, Netra ft 1800 White Paper (Apr. 1999) (50 pp.) (No. 139.pdf)	☐
	33	TIA/EIA (644) Standard Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits (Mar. 1996) (42 pp) (No. 118c.pdf)	☐
	34	Network Engines: P6000EXP Fault-Tolerant Load-Balanced Cluster Server (NEI00095) (1997) (4 pp.) (No. 22a.pdf)	☐
	35	Network Engines ClusterDirector User's Manual (Jun. 1998) (32 pp.) (No. 22b.pdf)	☐
	36	Freakes, Louise "Disk Connector Card Functional Requirement / Layout Specifications" (Jan. 1998) (9 pp.) (No. 26d.pdf)	☐
	37	Phillips, 9800 Processor Card Layout & Design Specifications (July 1997) (142 pp) (No. 26o.pdf)	☐

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	Examiner Name	
	Attorney Docket Number	ACQI-010/10US 310578-2052

	38	Eversys, CAPserver Product Brief (Nov. 2009) (No. 119.pdf)	☐
	39	Burrow, "Whitecross Data Exploration: A Technical Overview of the WXDES/98000 (Mar. 1999 Rev. 2.00) (90 pp) (No. 26f.pdf)	☐
	40	Burrow, "Whitecross Data Exploration: A Technical Overview of the WXDES/98000 (Apr. 1999) (222 pp) (No. 26i.pdf)	☐
	41	USB Compaq, Intel, Microsoft, NEC - (Rev. Apr. 2000) (650 pp.) (No. 141.pdf)	☐
	42	USB Compaq, Intel, Microsoft, NEC - Rev. (Sep. 1998) (327 pp.) No. 140.pdf	☐
	43	Whitecross Data Exploration Configuration and Maintenance Manual. Draft. (Jul 2000) (699 pp.) (No. 26e.pdf)	☐
	44	Whitecross WX-DES Hardware Maintenance (2000) (284 pp) (No. 26g.pdf)	☐
	45	Whitecross WX-DES Technical Overview (2000) (211 pp) (No. 26h.pdf)	☐
	46	Smith, Brendon "Processor Backplane Functional Requirement Specification" (Jul. 1997) (45 pp) (No. 26k.pdf)	☐

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U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	6742068	B2	2004-05-25	Gallagher et al.	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	12504534
	Filing Date	2009-07-16
	First Named Inventor	William W.Y. Chu
	Art Unit	
	Examiner Name	
	Attorney Docket Number	ACQI-010/10US 310578-2052

	1	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Exhibit B, US Patent No. 6,718,415 File History, 159 pages	☐
	2	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Exhibit C, Patent Owner's Asserted Claim Construction against Hewlett-Packard Company, 15 pages	☐
	3	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Exhibit D, Patent Owner's Asserted Claim Construction against International Business Machines Corporation, 11 pages	☐
	4	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Exhibit E, QuantumNet.com [1997-10-11], [online], [retrieved on 2009-11-16] Retrieved from the Internet Archive (archive.org) using Internet, 16 pages	☐
	5	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Exhibit F, jlChatCom.com {1997-1-4], [online], [retrieved on 2009-12-2] Retrieved from the Internet Archive (archive.org) using Internet, 15 pages	☐
	6	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Exhibit G, Eversys.com [1996-11-4], [online], [retrieved on 2009-11-16] Retrieved from the Internet Archive (archive.org) using Internet, 17 pages	☐
	7	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Exhibit H, Origin2000 Rackmount Owner's Guide [1998-6-15], [online], [retrieved on 2009-11-16] Retrieved from Silicon Graphics, Inc. using Internet <URL:http://techpubs.sgi.com/library/manuals/3000/007-3415-003/pdf/007-3415-003.pdf>, 149 pages	☐
	8	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Exhibit K, Novell Netware 4.11 documentation [1996], [online], [retreived on 2009-11-16] Retreived from Novell Inc. using Internet ,URL:http://www.novell.com/documentation/nw4/docui/>, 14 pages	☐
	9	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Exhibit L, Origin and Onyx2 Theory of Operations Manual [1998-6-15], [online], [retrieved on 2009-11-16] Retrieved from Silicon Graphics, Inc. using Internet <URL:http://techpubs.sgi.com/library/manuals/3000/007-3439-002/pdf/007-3439-002.pdf>, 127 pages	☐
	10	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Exhibit M (Part 1), IRIS Failsafe Administrator's Guide {1997-4-6], [online], [retrieved on 2009-11-16] Retrieved from Silicon Graphics Inc. using Internet <URL:http://techpubs.sgi.com/librarymanuals/3000/007-3109-003/pdf/007-3109-003.pdf>, 115 pages	☐
	11	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Exhibit M (Part 2), IRIS Failsafe Administrator's Guide {1997-4-6], [online], [retrieved on 2009-11-16] Retrieved from Silicon Graphics Inc. using Internet <URL:http://techpubs.sgi.com/librarymanuals/3000/007-3109-003/pdf/007-3109-003.pdf>, 101 pages	☐

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /R.P./

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	Application Number	12504534
	Filing Date	2009-07-16
	First Named Inventor	William W.Y. Chu
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	Attorney Docket Number	ACQI-010/10US 310578-2052

	12	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Exhibit N, CAPserver Product Guide, 1995, pp.1-16, 19 pages	☐
	13	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Exhibit O, Declaration Under 37 CFR 1.132 of Vincent P. Conroy, 11-24-2009, 3 pages	☐
	14	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Exhibit AA, Claim Charts with respect to QuantumNet for Anticipation and Obviousness, 60 pages	☐
	15	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Exhibit BB, Claim Charts with respect to Chatcom for Anticipation and Obviousness, 51 pages	☐
	16	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Exhibit CC, Claim Charts with respect to Eversys for Anticipation and Obviousness, 51 pages	☐
	17	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Exhibit DD, Claim Chart with respect to the Origin2000 Manual for Obviousness, 36 pages	☐
	18	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Exhibit EE, Claim Chart with respect to Gallagher for Anticipation and Obviousness, 59 pages	☐
	19	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Request for Inter Partes Reexamination, 44 pages	☐

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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12504534	CHU, WILLIAM W. Y.
	Examiner	Art Unit
	RAYMOND N PHAN	2111

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	10/22/2010								
	1	✓								
	2	✓								
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	4	✓								
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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
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	Examiner	Art Unit
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Final	Original	10/22/2010								
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	74	✓								
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	80	✓								
	81	✓								
	82	✓								
	83	✓								

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	17	blade same lvds	US-PGPUB; USPAT; USOCR; EPO; DERWENT	OR	ON	2010/10/25 07:59
L2	994	processor same (voltage adj2 differential)	US-PGPUB; USPAT; USOCR; EPO; DERWENT	OR	ON	2010/10/25 08:00
L3	118	processor same (voltage adj2 differential) same (blade or board or replacement)	US-PGPUB; USPAT; USOCR; EPO; DERWENT	OR	ON	2010/10/25 08:00
L4	52	pocrass.inv.	US-PGPUB; USPAT; USOCR; EPO; DERWENT	OR	ON	2010/10/25 08:02
L5	42	pocrass.inv. and connector	US-PGPUB; USPAT; USOCR; EPO; DERWENT	OR	ON	2010/10/25 08:03
L6	1	lvds same comput$3 same rack	US-PGPUB; USPAT; USOCR; EPO; DERWENT	OR	ON	2010/10/25 08:05
L7	64	lvds and (comput$3 same rack)	US-PGPUB; USPAT; USOCR; EPO; DERWENT	OR	ON	2010/10/25 08:07
L8	335	lvds same pci	US-PGPUB; USPAT; USOCR; EPO; DERWENT	OR	ON	2010/10/25 08:09
L9	51	lvds same pci same channel	US-PGPUB; USPAT; USOCR; EPO; DERWENT	OR	ON	2010/10/25 08:09
L10	1	power.clm. and "7818487".pn.	US-PGPUB; USPAT; USOCR; EPO; DERWENT	OR	ON	2010/10/25 09:55

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /R.P./

Substitute for form 1449A/PTO		*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Application Number	12/504,534
		Filing Date	July 16, 2009
		First Named Inventor	William W.Y. Chu
		Group Art Unit	2111
(*use as many sheets as necessary*)		Examiner Name	Unassigned
Sheet	1 of 6	Attorney Docket Number	ACQI-010/10US 310578-2052

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1.	US-3,996,585	12-07-1976	Hogan	
	2.	US-4,623,964	11-18-1986	Getz et al.	
	3.	US-4,700,362	10-13-1987	Todd et al.	
	4.	US-4,769,764	09-06-1988	Levanon	
	5.	US-4,872,091	10-03-1989	Maniwa et al.	
	6.	US-4,890,282	12-26-1989	Lambert et al.	
	7.	US-4,918,572	04-17-1990	Tarver et al.	
	8.	US-4,939,735	07-03-1990	Fredericks et al.	
	9.	US-5,056,141	10-08-1991	Dyke	
	10.	US-5,086,499	02-04-1992	Mutone	
	11.	US-5,251,097	10-05-1993	Simmons et al.	
	12.	US-5,278,509	01-11-1994	Haynes et al.	
	13.	US-5,278,730	01-11-1994	Kikinis	
	14.	US-5,293,497	03-08-1994	Free	
	15.	US-5,311,397	05-10-1994	Harshberger et al.	
	16.	US-5,317,477	05-31-1994	Gillett	
	17.	US-5,319,771	06-07-1994	Takeda	
	18.	US-5,331,509	07-19-1994	Kikinis	
	19.	US-5,355,391	10-11-1994	Horowitz et al.	
	20.	US-5,428,806	06-27-1995	Pocrass	
	21.	US-5,436,857	07-25-1995	Nelson et al.	
	22.	US-5,463,742	10-31-1995	Kobayashi	
	23.	US-5,539,616	07-23-1996	Kikinis	
	24.	US-5,550,710	08-27-1996	Rahamim et al.	
	25.	US-5,550,861	08-27-1996	Chan et al.	
	26.	US-5,578,940	11-26-1996	Dillon	
	27.	US-5,600,800	02-04-1997	Kikinis et al.	
	28.	US-5,603,044	02-11-1997	Annapareddy et al.	
	29.	US-5,606,717	02-25-1997	Farmwald et al.	
	30.	US-5,608,608	03-04-1997	Flint et al.	
	31.	US-5,630,057	05-13-1997	Hait	
	32.	US-5,638,521	06-10-1997	Buchala et al.	
	33.	US-5,640,302	06-17-1997	Kikinis	
	34.	US-5,659,773	08-19-1997	Huynh et al.	
	35.	US-5,663,661	09-02-1997	Dillon et al.	
	36.	US-5,673,174	09-30-1997	Hamirani	
	37.	US-5,680,126	10-21-1997	Kikinis	
	38.	US-5,689,654	11-18-1997	Kikinis	
	39.	US-5,774,704	06-30-1998	Williams	
	40.	US-5,721,837	02-24-1998	Kikinis	
	41.	US-5,721,842	02-24-1998	Beasley et al.	
	42.	US-5,745,733	04-28-1998	Robinson	
	43.	US-5,752,080	05-12-1998	Ryan	
	44.	US-5,764,924	06-09-1998	Hong	
	45.	US-5,795,228	08-18-1998	Trumbull	
	46.	US-5,809,538	09-15-1998	Pollmann	
	47.	US-5,815,681	09-29-1998	Kikinis	
	48.	US-5,819,050	10-06-1998	Boehling et al.	
	49.	US-5,826,048	10-20-1998	Dempsey et al.	
	50.	US-5,848,249	12-08-1998	Garbus	
	51.	US-5,859,669	01-12-1999	Prentice	

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Substitute for form 1449A/PTO		*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Application Number	12/504,534
		Filing Date	July 16, 2009
		First Named Inventor	William W.Y. Chu
(use as many sheets as necessary)		Group Art Unit	2111
		Examiner Name	Unassigned
Sheet	2 of 6	Attorney Docket No.	ACQI-010/10US 310578-2052

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	52.	US-5,907,566	05-25-1999	Benson et al.	
	53.	US-5,941,965	08-24-1999	Moroz	
	54.	US-5,948,047	09-07-1999	Jenkins et al.	
	55.	US-5,960,213	08-28-1999	Wilson	
	56.	US-5,968,144	10-19-1999	Walker et al.	
	57.	US-5,971,804	10-26-1999	Gallagher et al.	
	58.	US-5,977,989	11-02-1999	Lee et al.	
	59.	US-5,982,363	11-09-1999	Naift	
	60.	US-5,991,163	11-23-1999	Marconi et al.	
	61.	US-5,991,844	12-23-1999	Khosrowpour	
	62.	US-5,999,952	12-07-1999	Jenkins et al.	
	63.	US-6,002,442	12-14-1999	Li et al.	
	64.	US-6,003,105	12-14-1999	Vicard et al.	
	65.	US-6,011,546	01-04-2000	Bertram	
	66.	US-6,016,252	01-18-2000	Pignolet et al.	
	67.	US-6,028,643	02-22-2000	Jordan et al.	
	68.	US-6,029,183	02-22-2000	Jenkins et al.	
	69.	US-6,038,621	03-14-2000	Gale et al.	
	70.	US-6,040,792	03-21-2000	Watson et al.	
	71.	US-6,052,513	04-18-2000	McLaren	
	72.	US-6,069,615	05-30-2000	Abraham et al.	
	73.	US-6,088,224	07-11-2000	Gallagher et al.	
	74.	US-6,088,752	07-11-2000	Ahern	
	75.	US-6,157,534	12-05-2000	Gallagher et al.	
	76.	US-6,163,464	12-19-2000	Ishibashi et al.	
	77.	US-6,175,490	01-16-2001	Papa et al.	
	78.	US-6,202,169	03-13-2001	Razzaghe-Ashrafi et al.	
	79.	US-6,208,522	03-27-2001	Manweiler et al.	
	80.	US-6,216,185	04-10-2001	Chu	
	81.	US-6,260,155	07-10-2001	Dellacona	
	82.	US-6,289,376	09-11-2001	Taylor et al.	
	83.	US-6,304,895	10-16-2001	Schneider et al.	
	84.	US-6,311,268	10-30-2001	Chu	
	85.	US-6,314,522	11-06-2001	Chu et al.	
	86.	US-6,317,329	11-13-2001	Dowdy et al.	
	87.	US-6,321,335	11-20-2001	Chu	
	88.	US-6,332,180	12-18-2001	Kauffman et al.	
	89.	US-6,345,330	02-05-2002	Chu	
	90.	US-6,366,951	04-02-2002	Schmidt	
	91.	US-6,378,009	04-23-2002	Pinkston, II et al.	
	92.	US-6,381,602	04-30-2002	Shoroff et al.	
	93.	US-6,393,561	05-21-2002	Hagiwara et al.	
	94.	US-6,401,124	06-04-2002	Yang et al.	
	95.	US-6,425,033	07-23-2002	Conway et al.	
	96.	US-6,452,789	09-17-2002	Pallotti et al.	
	97.	US-6,452,790	09-17-2002	Chu et al.	
	98.	US-6,453,344	09-17-2002	Ellsworth	
	99.	US-6,496,361	12-17-2003	Kim et al.	
	100.	US-6,549,966	04-15-2003	Dickens et al.	
	101.	US-6,564,274	05-13-2003	Heath et al.	

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	102.	US-6,643,777	11-04-2003	Chu	
	103.	US-6,718,415	04-06-2004	Chu	
	104.	US-6,725,317	04-20-2004	Bouchier et al.	
	105.	US-6,324,605 B1	11-27-2001	Rafferty et al.	
	106.	US-2009/0157939	06/18/2009	Chu	
	107.	US-5,978,919	11-1999	Doi et al.	
	108.	US-6,009,488	12-28-1999	Kavipurapu	
	109.	US-6,025,989	02-15-2000	Ayd et al.	
	110.	US-6,070,214	05-30-2000	Ahern	
	111.	US-7,099,981 B2	08-29-2006	Chu	
	112.	US-7,416,446 B2	12-05-2006	Chu	
	113.	US-7,328,297 B2	02-05-2008	Chu	
	114.	US-7,363,415 B2	04-22-2008	Chu	
	115.	US-7,363,416 B2	04-22-2008	Chu	
	116.	US-7,376,779 B2	05-20-2008	Chu	
	117.	US-6,161,524	12-19-2000	Akbarian et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	1.	WO 92/18924	10-29-1992			
	2.	WO 94/00097	01-06-1994			
	3.	WO 95/13640	05-18-1995			
	4.	EP 722138A1	07-17-1996			
	5.	JP 6-289953	10-18-1994			

OTHER – NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[6]
	1.	Agerwala, T. et al., "SP2 System Architecture", IBM Systems Journal, Vol. 34, No. 2 (1995)	
	2.	Bernal, Carlos, product brochure entitled: "PowerSMP Series 4000", (March 1998) <<http://www/winnetmag.com/Windows/Article/ArticleID/3095//3095.html, downloaded from web on June 22, 2004, 2 pgs.	
	3.	Cragle, Jonathan, "Density System 1100", (May 1999) <<http://www.winnetmag.com/Windows/Article/ArtideID/5199/5199.html>>, downloaded from web on June 21, 2004, 4 pgs.	
	4.	Feldman, Jonathan, "Rack Steady: The Four Rack-Mounted Servers That Rocked Our Network", <<http://www.networkcomputing.com/shared/printArtide.jhtml?article=/910/910r3sidel .htm...>> June 23, 2004, 3 pgs.	
	5.	Fetters, Dave, "Cubix High-Density Server Leads the Way With Standout Management Software", (February 8. 1999) <<http://www. nwc. com/shared/printArticle.jhtml?article=/1003/1003r3full.html&pub=nwc>>, downloaded from web on June 23, 2004, 5 pgs.	
	6.	Gardner, Michael and Null, Christopher, "A Server Condominium", <<http://www.lantimes.com/testing/98jun/806a042a.html>>, June 23, 2004, 3 pgs.	
	7.	Harrison, Dave, "VME in the Military: The M1A2 Main Battle Tank Upgrade Relies on COTS VME"	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Application Number	12/504,534
		Filing Date	July 16, 2009
		First Named Inventor	William W.Y. Chu
		Group Art Unit	2111
(use as many sheets as necessary)		Examiner Name	Unassigned
Sheet	4 of 6	Attorney Docket No.	ACQI-010/10US 310578-2052

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		<<http://www.dv4.com>>, (February 9, 1998), pgs. 1-34.	
	8.	Williams, Dennis, "Consolidated Servers", (February 17, 1997) <<http://www.lantimes.com/testing/97compare/pcconsol.html>> downloaded from web on June 23, 2004, 2 pgs.	
	9.	Williams, Dennis, "Executive Summary: Consolidate Now", (February 17, 1997) <<http://www.lantimes.com/testing/97feb/702b064a.html>> downloaded from web on June 23, 2004, 2 pgs.	
	10.	Williams, Dennis, "Top "Scores for Useability and Openness", (February 17, 1997) <<http://www.lantimes.com/testing/97feb/702b064a.html>> downloaded from web on June 23, 2004, 2 pgs.	
	11.	Williams, Dennis, "ChatCom Inc. Chatterbox", (February 17, 1997) <<http://www.lantimes.com/testing/97feb/702b066a.html>> downloaded from web on June 23, 2004, 3 pgs.	
	12.	Williams, Dennis, "EVERSYS Corp. System 8000", (February 17, 1997) <<http://www.lantimes.com/testing/97feb/702b070b.html>> downloaded from web on June 22, 2004, 4 pgs.	
	13.	Williams, Dennis, "Cubix Corp. ERS/FT II", (February 17, 1997) <<http://www.lantimes.com/testing/97feb/702b068b.html>> downloaded from web on June 23, 2004, 4 pgs.	
	14.	Crystal Advertisement for "Rackmount Computers", (©2000-2004) <<http://www.crystalpc.com/products/roservers.asp>>, downloaded from web on June 17, 2004, 8 pgs.	
	15.	Crystal Advertisement for "QuickConnect® Cable Management", (©2000-2004) <<http://www.crystalpc.com/products/quickconnect.asp>> downloaded from web on June 17, 2004, 4 pgs.	
	16.	Cubix Product Brochure entitled, "Density System", (©2000) <<http://64.173.211.7/support/techinfo/system/density/densityl0.htm>> downloaded from web on June 22, 2004, 3 pgs.	
	17.	Cubix Product Brochure entitled, "Density System, Technical Specifications", (©2000) <<http://64.173.211.7/support/techinfo/system/density/info/spec.htm>> downloaded from web on June 22, 2004, 2 pgs.	
	18.	Cubix Product Manual entitled, "Density System", Chapter 1-Introduction, (©2000) <<http://64.173.211.7/support/techinfo/manuals/density/Chap-1.htm>> downloaded from web on June 22, 2004, 5 pgs.	
	19.	Cubix, "Click on the front panel that matches your system", (©2000) <<http://64.173.211.7/support/techinfo/system/density/densiry.htm>>, downloaded from web on June 22, 2004, 1 pg.	
	20.	Cubix Product Manual entitled, "Density System", Chapter 2-Installation, (©2000) <<http://64.173.211.7/support/techinfo/manuals/density/Chap-2.htm>> downloaded from web on June 22, 2004, 9 pgs.	
	21.	Cubix Product Manual entitled, "Density System", Chapter 3-Operation, (©2000) <<http://64.173.211.7/support/techinfo/manuals/density/Chap-3.htm>> downloaded from web on June 22, 2004, 4 pgs.	
	22.	Cubix Product Manual entitled, "Density System", Chapter 4-Maintenance and Repair, (©2000) <<http://64.173.211.7/support/techinfo/manuals/density/Chap-4.htm>> downloaded from web on June 22, 2004, 5 pgs.	
	23.	Cubix, "What are Groups?", (©2000) <<http://64.173.211.7/support/techinfo/system/density/info/groups.htm>>, downloaded from web on June 22, 2004, 3 pgs.	
	24.	Cubix, "SP 5200XS Series Plug-in Computers", (©2000) <<http://64.173.211.7/support/techinfo/bc/sp5200xs/intro.htm>>, downloaded from web on June 22, 2004, 2 pgs.	
	25.	Cubix, "SP 5200XS Series Technical Specifications", (©2000) <<http://64.173.211.7/support/techinfo/bc/sp5200xs/spec.htm>>, downloaded from web on June 22, 2004, 2 pgs.	

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Substitute for form 1449A/PTO		*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Application Number	12/504,534
		Filing Date	July 16, 2009
		First Named Inventor	William W.Y. Chu
		Group Art Unit	2111
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Sheet	5 of 6	Attorney Docket No.	ACQI-010/10US 310578-2052

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	26.	Cubix, "SP 5200 Series" Chapter 1-Introduction, (©2000) <<http://64.173.211.7/support/techinfo/manuals/sp5200/chap-1.htm>>, downloaded from web on June 22, 2004, 3 pgs.	
	27.	Cubix, "SP 5200 Series" Chapter 2-Switches & Jumpers, (©2000) <<http://64.173.211.7/support/techinfo/manuals/sp5200/chap-2.htm>>, downloaded from web on June 22, 2004, 3 pgs.	
	28.	Cubix, "SP 5200 Series" Chapter 3-Installation, (©2000) <<http//64.173.211.7/support/techinfo/manuals/sp5200/chap-3.htm>>, downloaded from web on June 22, 2004, 4 pgs.	
	29.	Cubix, "SP 5200 Series" Chapter 4-Technical Reference, (©2000) <<http://64.173.211.7/support/techinfo/manuals/sp5200/chap-4.htm>>, downloaded from web on June 22, 2004, 3 pgs.	
	30.	Cubix, "DP 6200 'D' Series Plug-in Computers" <<http://64.173.211.7/support/techinfo/bc/dp/6200d/intro.htm">>, downloaded from web on June 22, 2004, 3 pgs.	
	31.	Cubix, "Installing DP or SP Series Boards" (©2000) <<http://64.173.211.7/support/techinfo/bc/dp/6200d/intro.htm">>, downloaded from web on June 22, 2004, 2 pgs.	
	32.	Cubix, "Powering On/Off or Resetting Plug-in Computers in an Density System", (©2000) <<http://64.173.211.7/support/techinfo/system/density/info/power.htm>>, downloaded from web on June 22, 2004, 2 pgs.	
	33.	Cubix, "Multiplexing Video, Keyboard & Mouse with Multiple Density Systems", (©2000) <<http://64.173.211.7/support/techinfo/system/density/info/vkm-mux.htm>>, downloaded from web on June 22, 2004, 2 pgs.	
	34.	eBay Advertisement for "Total IT Group Network Engines", <<http://cgi.ebay.com/ws/eBayISAPI.dll?ViewItem&item=5706388046&sspagename=STRK%3AMDBI%3AMEBI3AIT&rd=1>>, (downloaded from web on June 25, 200), 1 pg.	
	35.	"Features Chart", (February 1, 1997) <<http://www.lantimes.com/testing/97feb/702b072a.html>>, (downloaded from web on June 23, 2004), 3 pgs.	
	36.	Internet Telephone Roundup, "Industrial Computers", <<http://www.tmcnet.com/articles/itmag/0499/0499roundup.htm>>, (downloaded from web on June 23, 2004), 5 pgs.	
	37.	Press Release: Hiawatha, Iowa, (March 1, 1997) entitled "Crystal Group Products Offer Industrial PC's with Built-in Flexibility", <<http://www.crystalpc.com/news/pressreleases/prodpr.asp>>, (downloaded from web on May 14, 2004), 2 pgs.	
	38.	Press Release: Kanata, Ontario, Canada, (April 1998) entitled "Enhanced COTS SBC from DY 4 Systems features 166MHz Pentium™ Processor" <<http://www.realtime-info.be/VPR/layout/display/pr.asp?/pr.asp?PRID=363>>, 2 pgs.	
	39.	Product Brochure entitled "SVME/DM-192 Pentium®II Single Board Computer" (June 1999) pgs. 1-9.	
	40.	Product Brochure entitled "System 8000", <<http://www.bomara.com/Eversys/briefDefault.htm>>, (downloaded from web on June 22, 2004), 4 pgs.	
	41.	Product Brochure entitled: "ERS/FT II System", (©2000) <<http://64.173.211.7/support/techinfo/system/ersft2/ersft2.htm>>, downloaded from web on June 22, 2004, 4 pgs.	
	42.	Product Manual entitled: "ERS II and ERS/ FT II", Chap. 3, System Components, <<http://64.173.211.7/support/techinfo/manuals/ers2/ers2-c3.htm>>, (downloaded from web on June 22, 2004), 21 pgs.	
	43.	Product Manual entitled: "ERS II and ERS/FT II", Chap. 6, Component Installation, <<http://64.173.211.7/support/techinfo/manuals/ers2/ers2-c6.htm>>, (downloaded from web on June 22, 2004), 18 pgs.	
	44.	Windows Magazine, "Cubix PowerSMP Series 4000", (Nov. 1997), <http://<www.techweb.com/winmag/library/1997/1101/ntent008.htm>> downloaded from the web on June 22, 2004, pg. NT07.	
	45.	CETIA Brochure "CETIA Powerengine CVME 603e" pp. 1-6 downloaded from the internet @ http://www.cetia.com/Products Addons/wp-47-01.pdf. on 2/15/2006.	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Application Number	12/504,534
		Filing Date	July 16, 2009
		First Named Inventor	William W.Y. Chu
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	46.	MPL Brochure, "The First Rugged All in One Industrial 486FDX-133 Mhz PC", (1998), pages 53.	
	47.	MPL Brochure "IPM 486 Brochure/IPM5 User Manual", pp. 1-9, downloaded from the internet @ http://www.mpl ch/DOCS./u48600xd.pdf on 2/15/2006.	
	48.	Synder, Joel, "Better Management Through Consolidation," (Aug. 18, 1997), pp. 1-6 downloaded from the internet @ http://www.opus1.com/www/jms/nw-con-0818rev.html.,	
	49.	Eversys Corporation, "Eversys System 8000 Consolidated Network Server Market and Product Overview," Slide presentation, downlaoded from <http://eversys.com>, (Product to be Released March 1, 2007), 20 pages.	
	50.	"SQL Server and NT Cluster Manager Availability Demo, "Microsoft Server Programmer Developers Conference, November 1996, 15 pages.	
	51.	Microsoft Cluster Service Center, MSCS Basics," downloaded from <<http://www.networks.com/mscsbasics.htm.., February 7, 2005, 6 pages.	
	52.	Complaint For Patent Infringement, Case 6:09-cv-00148, filed April 2, 2009.	
	53.	Answer to 2nd Amended and Counterclaims by Fujitsu America, Inc., Case 6:09-cv-00148-LED, dated August 10, 2009, 34 pages.	

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Application Number	12504534
Filing Date	2009-07-16
First Named Inventor	William Chu
Art Unit	2111
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	First Named Inventor	William Chu
	Art Unit	2111
	Examiner Name	Raymond Ngan Phan
	Attorney Docket Number	ACQI-010/10US 310578-2052

	1	PC MAGAZINE, "Think Modular" (06-10-1997)	☐
	2	LIQUORMAN, "Convergent Technologies Had This Idea" (12/05/1997)	☐
	3	BERST, "Hope For The Modular PCs We all Really Want" (12/05/1997)	☐
	4	BOYD-MERRITT, "Upgradable-PC Effort Takes Divergent Paths" (EE Times 1997) http://techweb.cmp/com/eet/news/97/949news/effort.html	☐
	5	FAEGRE, et al., "Unisys' Best-Kept Secret Is An Operating System Built For Distributed Business Applications." BYTE (12/1994)	☐
	6	SPANG, "Component House: Design Technology For 'PCs in a snap' -- NeoSystems Offers Building Blocks" TECHWEB (04/21/1997:732)	☐

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	First Named Inventor	William Chu
	Art Unit	2111
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(71) Applicant *(for all designated States except US)*: INTEL CORPORATION [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95052 (US).

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(74) Agents: HYMAN, Eric, S. et al.; Blakely, Sokoloff, Taylor & Zafman, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025-1026 (US).

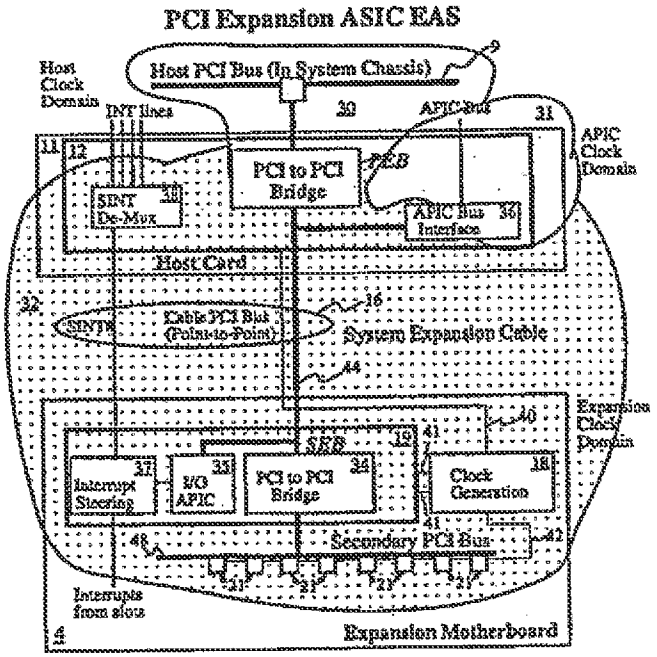
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(54) Title: AN APPARATUS AND METHOD FOR PROVIDING REMOTE PCI SLOT EXPANSION

(57) Abstract

An apparatus and method for providing PCI slot expansion (21). An asynchronous PCI to PCI bridge (34) for insertion into a host PCI slot (10) is coupled via a cabled PCI bus (16) to an expansion module (4). The bridge establishes two distinct time domains. An expansion clock signal (18) is generated and its timing matched for consistent arrival throughout the expansion clock domain. An expanded number of PCI slots are thereby available to the host system.



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AN APPARATUS AND METHOD FOR PROVIDING REMOTE PCI SLOT EXPANSION

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention relates to bussing in a computer system. More specifically, the invention relates to using PCI as a cable bus to expand the number of PCI slots available in a system.

2. Related Art

The peripheral component interconnect (PCI) bus is a high performance low latency I/O bus architected to minimize system cost. PCI has quickly gained wide acceptance in the computer industry. The PCI bus standard provides for a high bandwidth and a flexibility that is independent of new processor technologies and increased processor speed. At this time, computer system architects are primarily designing speed sensitive peripherals such as graphics accelerators and SCSI disk drive controllers to be utilized with the PCI bus.

The PCI specification is well defined. See particularly, PCI Local Bus Specification, rev. 2.0, April 30, 1993. The specification reflects that PCI is capable of running at any frequency up to 33 MHz. This high level of possible throughput makes PCI an ideal choice for volume servers. Unfortunately, at such speed, the PCI bus can only support 3 - 4 slots along a single bus segment. This number of slots is unacceptably low for a practical application in the volume server market. Some prior systems have addressed this problem by cascading PCI buses on the host mother board. Unfortunately, such cascading increases the cost of the basic system and still fails to provide a level of slot expansion necessary in volume servers. Moreover, such single chassis systems are not readily expandable as the user's needs change.

The possibility of bussing between multiple modular chassis implicates some unique problem in the context of PCI. Specifically, using available PCI to PCI bridges, it is necessary to synchronize the clock system wide. Because PCI does not require a standard host clock signal, phase lock loops cannot be employed to synchronize both sides of the bridge. The shear physical dimension of a multi-chassis system makes such synchronization of a single clock domain

even more problematic. These problems necessitated custom design for circuits to provide out of chassis slot expansion.

Additionally, the PCI bus specification requires four active low, level sensitive interrupt pins for all slots supported and defines these interrupts' use as hardware shareable. That means that multiple PCI devices can drive the same interrupt line or that multiple PCI interrupt lines can be driven by different devices but may result in a single interrupt being generated to the system interrupt controller to be serviced by a shared interrupt driver. Thus, as the number of slots amongst which the interrupts must be shared increases, the resources and overhead required to resolve the source of the interrupt also increases as the number of sharing slots increases.

It is therefore desirable to provide an apparatus which allows PCI slot expansion without unnecessarily increasing the cost of the host system. Such apparatus should be forward and backward compatible, without requiring customization to each specific system. The performance of an expanded slot must be maintained at an acceptably high level, and the system should be readily expandable to meet the demands of increasing processor power. It is also desirable to develop a way to simplify the interrupts generated by such an expanded system.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shoes a block diagram of a host and expansion module of the invention.

Figure 1A is a table of the signals and required pins in the cabled bus of the invention.

Figure 2 is a block diagram of the module interfaces of the instant invention.

Figure 3 is a diagram of the clock generation circuit for the expansion module of the invention.

Figure 4 is a table listing specifications of cables suitable for the instant invention.

Figure 4A is a table showing timing budgets of two possible operating point for the invention.

SUMMARY OF THE INVENTION

The instant invention provides an apparatus and method for expanding the number of PCI slots available to a host system. By employing an asynchronous PCI to PCI bridge, host and expansion time domains are segregated. A cabled PCI bus responsive to a clock signal generated and controlled in the expansion module is used to carry the signals between independent host and expansion chassis. Because the expansion system is not dependent on the host clock or the functionalities of the host system, it is suitable for integration into existing system, and it will not increase the cost of a base host system. Thus, the invention provides ready expandability as needs change.

In one embodiment, the invention provides interrupt expansion in addition to slot expansion. This is accomplished by providing a means for connecting to the host APIC bus on the expansion card and a means of encoding the PCI interrupts generated by the expansion PCI slot into APIC on the expansion mother board. This expansion will reduce the overhead associated with servicing interrupts shared by the expanded slots.

DETAILED DESCRIPTION OF THE INVENTION

The present invention provides a method and apparatus for using a cabled PCI bus to provide an expansion of the number of PCI slots available to a host system. For the purpose of explanation, specific details are set forth to provide a thorough understanding of the present invention. However, it will be understood by one skilled in the art, from reading this disclosure, that the invention may be practiced without these details. Moreover, well known elements devices, process steps and the like are not set forth in order to avoid obscuring the invention.

Figure 1 shows a block diagram of a system incorporating the instant invention. The host system resides within a host chassis 1 and includes a host mother board 3. The host mother board has a CPU 5 connected to a memory 6 by a system bus 7. A bridge 8 is provided on the mother board to bridge between the system bus 7 and a host PCI bus 9. At 33 MHz, the PCI specification only permits 3 - 4 slots 10 along a single bus segment. By installing an expansion card

11 in at least one of the slots 10 on the host PCI bus 9, it is possible to expand the number of slots of the system as a whole.

The expansion card 11 has a primary expansion bridge (PEB) 12 described more fully with reference to Figure 2 below, and a cable connector 15, an exemplary embodiment employs a 100 pin cable connector. The expansion card also provides an optional APIC connector 14 to allow the card 11 to be connected to the APIC bus not shown on the host mother board 3. This allows for sufficient signal conductors to accommodate parallel transmission of all PCI required signals and adequate grounding. Figure 1A is a table of the relevant PCI signals. The cable 16 is selected based on propagation speed down the cable 16 and cable skewing. It is desirable to choose a cable 16 with minimal skewing with maximum propagation speed. The cable 16 functions as a point to point PCI bus between the expansion side of the PEB 12 and the secondary expansion bridge (SEB) 19 which is described more fully below. The cable 16 should be well terminated at either end with impedances approximately equal to the characteristic impedance in the cable. In an exemplary embodiment, a six foot HIPPI cable with a characteristic impedance of 88 ± 5 ohms is used. HIPPI cable meets ANSI standards and includes 50 twisted pairs, thereby providing an adequate number of signal lines. It would be possible to use a smaller cable and lower pin count connector but such would limit possible functionality somewhat.

The expansion chassis 2 contains an expansion mother board 4 to which the cable 16 connects via connector 17. A PCI bus runs from the connector to the SEB 19. The clocking in the expansion system is provided by a clock generator 18 which is asynchronous with and independent of the host clock (not shown). The number of slots 21 available on the secondary PCI bus (SPB) 20 is determined by the speed of the clock signal generated. At 25 MHz, 8 - 12 slots are available, while at 33 MHz, only 3 - 4 slots would be available.

It is possible and contemplated as within the scope of this invention that multiple expansion modules could be coupled to a single host (one card per available PCI slot). It is also within the scope of the invention to cascade an expansion module off an expansion module.

Figure 2 more clearly sets forth the relationship between the PEB 12, Cable 16, and SEB 19. Figure 2 is divided into three clock domains. The host clock domain 30, the expansion clock domain 32, and an optional APIC clock

domain 31. The instant invention employs an asynchronous bridge 33 between the host and expansion module. A PCI to PCI bridge comprises a primary bus interface and a secondary bus interface. In the case of an asynchronous bridge the primary interface is responsive to the host clock while the secondary interface is responsive to the expansion clock, thereby creating an asynchronous boundary 13 between the host clock domain 30 and expansion clock domain 32. At the most basic level this could be implemented with a pair of D flip flops for each relevant signal. As a practical matter to ensure data validity where clock rates vary it is desirable to provide some storage between the two interfaces. Inbound and outbound queues of 4x16 bytes have been found adequate. For further detail see PCI to PCI Bridge Spec. Revision 1.0, April 15, 1994.

In one exemplary embodiment, the host PCI bus is connected to an asynchronous PCI to PCI bridge 33 contained in PEB 12 on the expansion card. The host side of the bridge 33 operates in the host clock domain 30 while the expansion side is synchronous with the expansion clock domain 32. The PEB 12 also contains a demultiplexer 38 to demultiplex the 4 PCI supported interrupts coming from the expansion system. An optional APIC bus interface 36 can also be provided within the PEB 12, thereby expanding the interrupts available to the expansion system. Such interface must be asynchronous operating partially in the APIC clock domain 31 and partially in the expansion clock domain 32. Significantly, this option does not comply with PCI specification. Intelligent I/O units like those described in co-pending application, Architecture for I/O Processor that Integrates a PCI-to-PCI Bridge, Serial No. _____ supports these functionalities. Accordingly, one embodiment envisioned in the instant invention employs such an intelligent I/O unit as the PEB 12.

The expansion end of the asynchronous bridge 33 is coupled through a cabled PCI bus 16 to the SEB 19 on the expansion mother board 41. The cable 16 contains the PCI bus signals 44, the expansion domain clock signal 40, an SINT# 39. SINT #39 is not a standard PCI line. Rather, it is a line carrying the serialization of the standard PCI interrupts. One way to serialize this is to continuously synchronize the four standard PCI interrupt signals to the PCI clock and send the information across the interface on SINT# whenever a change occurs using a protocol of one start bit (low), INTA#, INTB#, INTC#, INTD#, odd parity and one stop bit (high) as shown in Figure 5. If an interrupt is unmasked in

the I/O APIC, then that INT# line should not be serialized on the SINT# signal (i.e. it should be interpreted as inactive). In such case, the I/O APIC will handle distributing the interrupt to the host. The SINT# protocol will be driven continuously (with all interrupts inactive) during reset. The interrupt serializer will also send a new message after 16 clocks of inactivity.

SINT# is used by the PEB to decode the current value of INTA#, INTB#, INTC#, INTD#. Whenever the interrupt demux block sees SINT# go low, it will capture the data for the next four clocks and if the parity (5th cloth after Start) is good, use the data to update its current value for the four interrupt outputs. If bad parity is detected, the data will be ignored. This interrupt serialization process causes a worst case delay of 9 clocks for each level of expansion subsystem (2 for synchronization and 7 to send) which is 360 ns at 25 MHz. This is merely one simple way to serialize interrupts. Other serialization schemes will occur to one of ordinary skill in the art, such schemes are contemplated for use with the instant invention.

At the expansion end of cable 16, the SEB 19 contains a PCI to PCI bridge 34 which may be synchronous or asynchronous. SEB 19 also optionally contains an I/O APIC 35 which expands the number of interrupts available for use by the expansion system, and reduces or eliminates the polling which would be required if all PCI slots in the combined host and expansion system shared only the four PCI provided interrupts. Finally, an interrupt steering device 37 is provided to either steer the PCI supported interrupts across the cable 16 to the demultiplexer 38, or if provided, steers slot interrupt into the I/O APIC 35 which in turn buses the interrupt along the cable 16 to the APIC bus interface 36. Again, it is contemplated that an intelligent I/O unit as described in co-pending application Serial No. _____ could be used to implement SEB 19. Also, on the expansion mother board 4 are the clock generation device 18 and the secondary PCI bus 45.

In Figure 2, eight slots 21 are shown on the secondary PCI bus 45. PCI does not define a maximum number of slots, rather it has rigidly defined electrical characteristics. Specifically, PCI defines that clock skew + clock to out at master + setup at target + settling time ≤ clock period. In the clock generation scheme described below the time allotted for settling is used as flight time down the cable 16 thereby reducing the latency in the transaction between host and expansion modules. Since the introduction of each slot 21 increases the capacitance of the

system thereby negatively affecting the transition speed between states, i.e., the settling time, a slower clock increases the time available for settling and accordingly increase the number of loads (slots) the system can handle. If operation is at 25 MHz, it is contemplated that 8 - 12 slots could be provided.

Figure 3 shows the clock generation of the instant invention, an oscillator 50 generates a clock signal of a desired frequency up to 33 MHz. It will be recognized that an oscillator need not be employed to generate the clock signal, any conventional method of generating a signal of the desired frequency can be employed. In an exemplary embodiment, the oscillator 50 generates a 25 MHz clock signal.

The present application requires multiple copies of the clock be generated from a single source. Figure 3 shows the clock signal going to the cable 16 and ten other lines 58. This is adequate for right slots 21 and the SEB 19. It is necessary that the clock used at the host interface end of the cable 15 and expansion chassis interfaces 58 arrive within the clock skew timing specifications. To this end, low skew clock drivers 51 are employed along each line to minimize skew along the different lines, and a delay element 52 is introduced between the local lines and the remote interface 15. By matching the propagation delay in the cable 16 to the host (remote) interface 15 with a delay element 52, it is possible to achieve the desired synchronization of the clocks at the respective interfaces 15 and 58. To select an appropriate delay line 52 value two options exist, one can either delay the local lines by the propagation delay in the cable or delay the signal to the cable by the period of its clock signal minus the propagation delay. Figure 3 depicts the delay element 52 introduced along the local lines. It is contemplated that either a passive delay line or suitable high speed buffer might be employed to accomplish the desired delay. The maximum clock skew between slots 21 on the expansion mother board 4 and the SEB 19 is 2 ns. Figure 4 reflects possible selections which will satisfy the PCI specifications. Significantly, each clock signal line should be matched as closely as possible. Thus, the same number of buffer drivers 51 are employed along each line. Impedances 56 should be matched with the characteristic impedance of the clock traces on expansion motherboard 4. Moreover, the lengths of printed circuit board traces from the buffers 51 to their destinations should be as closely matched as possible, including the trace from the buffer driving the cable connection. This can be done by increasing the length of

all traces to match which ever trace has the longest length naturally. The most critical length match is between the clock going to the SEB 19 and the one driving the PEB 12 through the cable 16. Appropriately selecting delay 52 line value will improve this match.

The electrical connection scheme uses the bridge chips (i.e., PEB and SEB) to connect to the cable using series termination. This termination is external. The series termination value is equal to the impedance of the cable minus the impedance of the driver. The source end of the cable is driving with a 1/2 voltage incident waveform which doubles to a full voltage waveform due to the reflection coefficient of 1 it encounters at the destination end of the cable. When driving the cable the series termination forms a half wave incident waveform which encounters a reflection coefficient of one. In an embodiment employing a 6 foot cable, the characteristic impedance of such cable is 88 ± 5 ohms. Accordingly appropriate termination impedances can be selected with reference to the impedance of the selected driver.

It would also be possible to place the clock generator 18 on the expansions card 11. While the same rules discussed above would apply to such placement, maintaining the required coordination of the signals becomes more problematic as the number of remote signals to be coordinated increases. Nevertheless, such placement is within the scope and contemplation of the invention.

In the foregoing specification, the invention has been described with reference to specific embodiments thereof. It will however be evident that various modifications and changes made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims. The specification and drawings are accordingly, to be regarded in an illustrative rather than a restrictive sense. Therefore, the scope of the invention should be limited only by the appended claims.

CLAIMS

What is claimed is:

1. An apparatus for providing PCI slot expansion comprising:

an expansion card having disposed thereon an asynchronous PCI to PCI bridge with a host side and an expansion side for coupling to a host motherboard;

an expansion motherboard having a plurality of PCI slots;

a cabled PCI bus for coupling the expansion card to the expansion motherboard;

a clock generator for providing a clock signal to the expansion motherboard and the expansion side of the asynchronous PCI to PCI bridge.

2. The apparatus of claim 1 wherein the clock generator is disposed on the expansion mother board.

3. The apparatus of claim 2 wherein the clock generator generates a 25 MHz signal.

4. The apparatus of claim 2

wherein the expansion mother board further comprises a secondary expansion bridge; and

coupling the cabled signals to an expansion PCI bus having a plurality of slots.

5. The apparatus of claim 4

wherein the secondary expansion bridge further comprises an interrupt steering circuit and an I/O APIC; and

the expansion card further comprises an APIC interface.

6. The apparatus of claim 1 wherein the asynchronous bridge is an intelligent I/O unit.

7. The apparatus of claim 4 wherein the secondary expansion bridge is an intelligent I/O unit.

8. A modular computer system providing an expanded number of PCI slots comprising:

a host module having a host motherboard with a CPU disposed thereon;

a PCI bus disposed on the host motherboard responsive to a host clock and having a plurality of host PCI slots;

an expansion card for coupling to one of the plurality of host PCI slots;

an expansion module having an expansion motherboard, the expansion motherboard having an expansion PCI bus with a plurality of expansion PCI slots responsive to an expansion clock signal; and

a cabled PCI bus for connecting the host and expansion modules.

9. The modular computer system of claim 8

further comprising a primary expansion bridge for providing an interface between the cabled bus and the host PCI bus;

a secondary expansion bridge for providing an interface between the cabled bus and the expansion PCI bus;

a clock generator disposed within the expansion module for generation of the expansion clock signal.

10. The modular computer system of claim 9

wherein the primary expansion bridge comprises an asynchronous PCI to PCI bridge and a demultiplexor; and

the secondary expansion bridge comprises a PCI to PCI bridge and an interrupt steering unit.

11. The modular computer system of claim 9 wherein the expansion clock signal is 25 MHz.

12. The modular computer system of claim 9 wherein the cabled bus comprises a 100 conductor cable with a 100 pin connector at each end.

13. The modular computer system of claim 9 wherein the primary expansion bridge is an intelligent I/O unit.

14. The modular computer system of claim 10 wherein the primary expansion bridge further comprises:

an APIC interface unit; and

the secondary expansion bridge further comprises an I/O APIC unit.

15. A method of providing modular expansion of PCI slots in a computer system comprising the steps of:

installing an expansion card in a PCI slot of a host module;

connecting the expansion card to an expansion module by a cable;

generating an expansion clock signal independent of a host clock signal;

segregating the host and expansion clock signals at the expansion card; and

cabling PCI transmissions between the modules along the cable.

16. The method of claim 15 wherein the segregating step is performed by an asynchronous PCI to PCI bridge.

17. The method of claim 15 wherein the step of generating further comprises the step of coordinating arrival of the expansion clock signal at a plurality of local and remote interfaces.

18. The method of claim 15 wherein the cable is terminated and operates as a point to point PCI bus.

19. The method of claim 17 further comprising

providing an APIC bus interface on the expansion card;

disposing an I/O APIC unit within the expansion module;

passing interrupts generated in the expansion module to a host APIC bus.

20. The method of claim 15 wherein an intelligent I/O unit performs the segregating step.

21. An apparatus for providing PCI slot expansion comprising:

means for segregating a host and an expansion time domain for installing in a host system PCI slot;

means for transmitting PCI signals over a predetermined distance;

means for generating a clock signal for the expansion time domain;

an expansion PCI bus responsive to the clock of the expansion time domain, said expansion bus having a plurality of PCI slots;

wherein the means for transmitting more PCI signals from the expansion bus to the means for segregating, and the means for segregating passes the signals between the time domains.

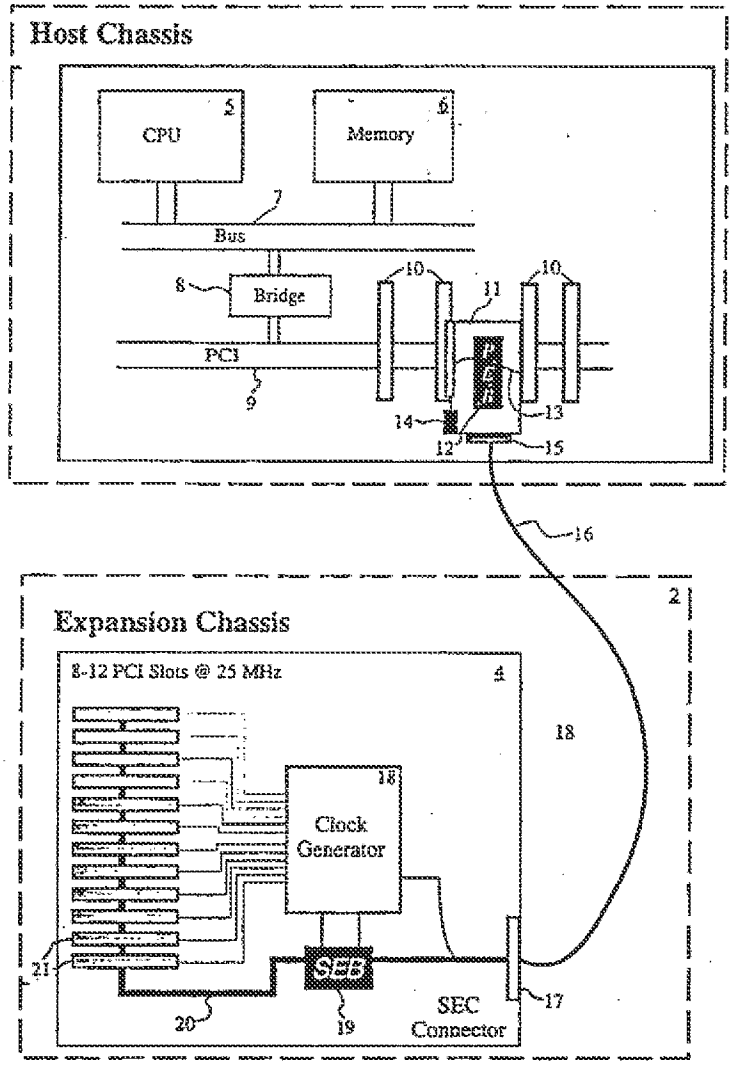

Host Chassis
CPU
5
Memory
6
7
Bus
8
Bridge
10
10
11
PCI
9
14
13
12
15
16
2
Expansion Chassis
8-12 PCI Slots @ 25 MHz
4
18
18
Clock Generator
21
SEC
20
19
SEC Connector
17

FIGURE 1

SIGNALS	PINS	DESCRIPTION
AD[0:31]	32	Standard PCI multiplexed address/data lines
C/BE[0:3]#	4	Standard PCI multiplexed command/byte enable lines
FRAME#	1	Standard PCI FRAME# line
IRDY#	1	Standard PCI IRDY# line
TRDY#	1	Standard PCI TRDY# line
DEVSEL#	1	Standard PCI DEVSEL# line
STOP#	1	Standard PCI STOP# line
LOCK#	1	Standard PCI LOCK# line
PERR#	1	Standard PCI PERR# line
SERR#	1	Standard PCI SERR# line
RESET #	1	Standard PCI RESET# line
PAR	1	Standard PCI PAR line
REQ#	1	*SEB* request to *PEB* for use of the *SEC*.
GNT#	1	*PEB* grant to *SEB* use of the *SEC*.
SINT#	1	Serialized interrupt line (Not Standard PCI)
CLK	1	*SEB* generated clock to *PEB* for use of the with the interface to *SEC*.
total	50	

FIGURE 1A

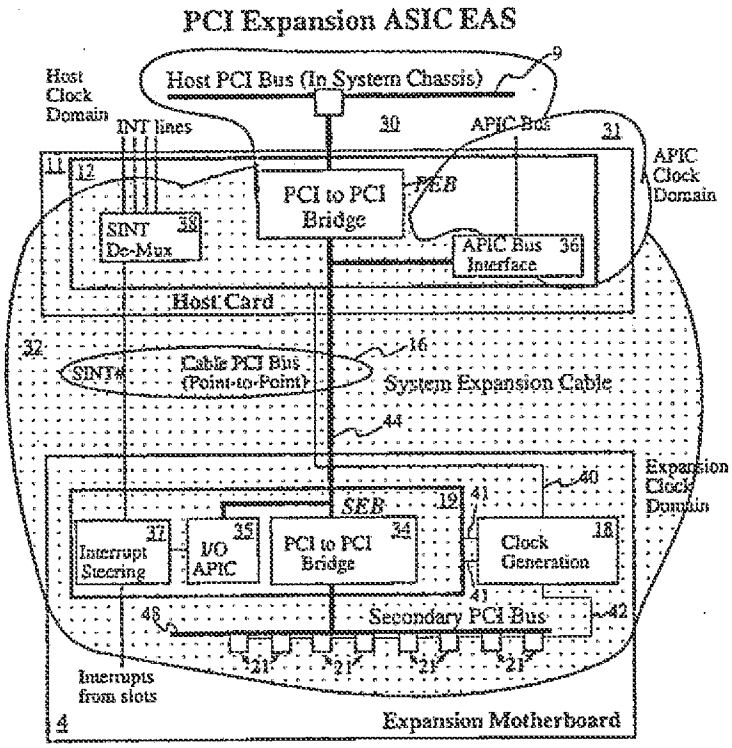

PCI Expansion ASIC EAS
Host Clock Domain
Host PCI Bus (In System Chassis)
9
INT lines
30
APIC Bus
31
APIC Clock Domain
11
12
PCI to PCI Bridge
SEB
SINT De-Mux
38
APIC Bus Interface
36
Host Card
32
SINTs
Cable PCI Bus (Point-to-Point)
16
System Expansion Cable
44
Expansion Clock Domain
40
SEB
41
Interrupt Steering
37
I/O APIC
35
PCI to PCI Bridge
34
Clock Generation
18
43
48
Secondary PCI Bus
42
21
Interrupts from slots
4
Expansion Motherboard

FIGURE 2

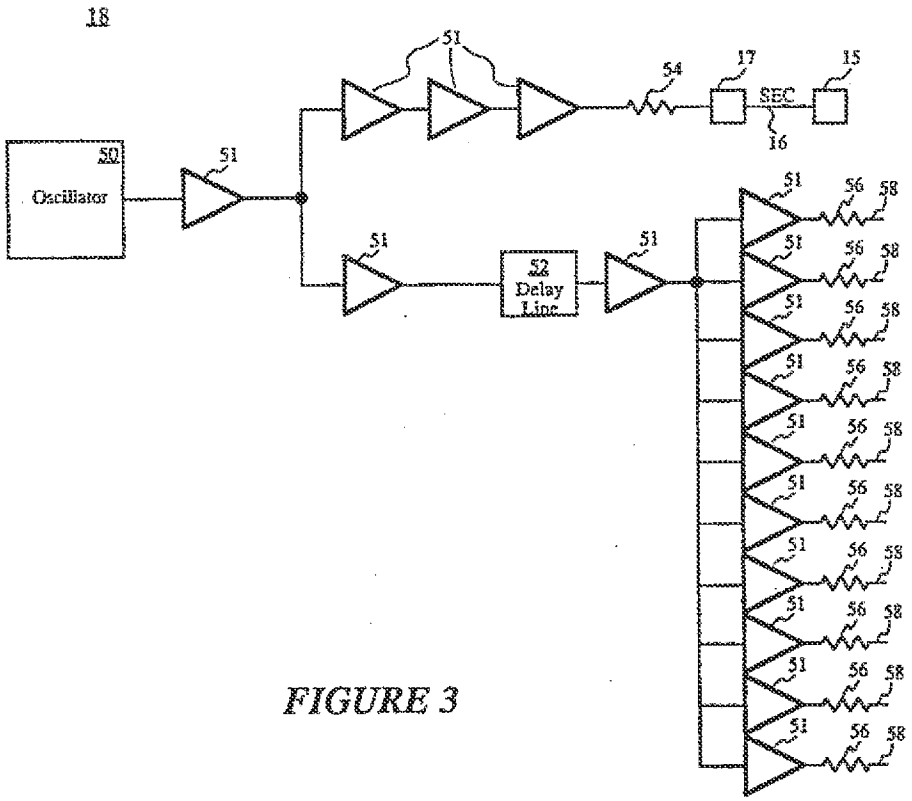


FIGURE 3

		Total Buffer	Delay Line		Cable	
Option	Clock Period	Skew	Delay	Skew	Length	Skew
1	30ns	840ps	10ns	250ps	10ns	910ps
2	40ns	10840ps	10ns	250ps	10ns	910ps
3	40ns	1500ps	19ns	250ps	19ns	1250ps
4	30ns	20840ps	10ns	250ps	10ns	910ps
5	50ns	11500ps	19ns	250ps	19ns	1250ps
6	60ns	21500ps	19ns	250ps	19ns	2150ps

FIGURE 4: Clock Skew

	33 MHz	25 MHz
Clock Skew (PCI)	2 ns	6 ns
Clock to Out at Master (PCI)	11 ns	11 ns
Cable delay at 6 feet +/- 2 in.	9.5 ns	9.5 ns
Cable Skew	0.5 ns	0.5 ns
Setup at Target (PCI)	7 ns	7 ns
Margin	0 ns	6 ns
Total Period	30 ns	40 ns

FIGURE 4A

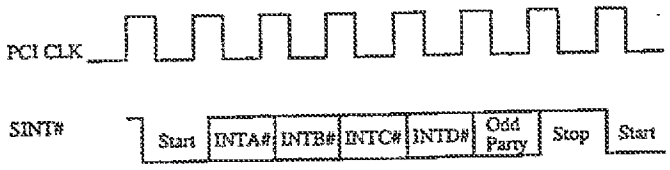


FIGURE 5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US96/10460

A. CLASSIFICATION OF SUBJECT MATTER
IPC(6) :G06F 13/00
US CL : 395/822
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 395/822, 828, 306; 364/231, 240

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS, IEEE

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US, A, 4,882,702 (STRUGER ET AL) 21 NOVEMBER 1989, column 4, lines 33-50, column 15, lines 66 - column 16, lines 18, and FIG. 1	1, 4-5, 8, 12, 14-15, 18-19, 21.
Y	US, A, 5,191,657 (LUDWIG ET AL) 02 MARCH 1993, column 3, lines 62-68, column 4, lines 47-51, column 7, lines 30-32, and column 22, lines 30-37.	1-3, 6-7, 9-11, 13, 15-17, 20, 21.

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
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INTERNATIONAL SEARCH REPORT

International application No.
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C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant t
Y,P	PC SYSTEM ARCHITECHTURE SERIES, NOVEMBER 1995, SHANLEY ET AL, "PCI SYSTEM ARCHITECHTURE", PAGES 381-387 (THE INFORMATION ON THE PAGES ARE FROM REVISION 1.0 PCI to PCI BRIDGE ARCHITECHTURE SPECIFICATION DATED APRIL 5, 1994).	1, 8, 15,

Form PCT/ISA/210 (continuation of second sheet)(July 1992)*

Electronic Patent Application Fee Transmittal

Application Number:	12504534
Filing Date:	16-Jul-2009
Title of Invention:	MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNDIRECTIONAL SERIAL BIT CHANNELS
First Named Inventor/Applicant Name:	William W. Y. Chu
Filer:	Cliff Z. Liu/Kathleen Smith
Attorney Docket Number:	ACQI-010/10US 310578-2052

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
		Total in USD ($)		**180**

Electronic Acknowledgement Receipt

EFS ID:	9053225
Application Number:	12504534
International Application Number:	
Confirmation Number:	1286
Title of Invention:	MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNDIRECTIONAL SERIAL BIT CHANNELS
First Named Inventor/Applicant Name:	William W. Y. Chu
Customer Number:	58249
Filer:	Cliff Z. Liu/Kathleen Smith
Filer Authorized By:	Cliff Z. Liu
Attorney Docket Number:	ACQI-010/10US 310578-2052
Receipt Date:	16-DEC-2010
Filing Date:	16-JUL-2009
Time Stamp:	15:33:15
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$180
RAM confirmation Number	2100
Deposit Account	501283
Authorized User	
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Filed (SB/08)	ACQI_010_10US_SB08_16Dec10.pdf	612648 d21fd3be32fc0e0bbaa3fcafff94d43de5956e3c	no	4
Warnings:					
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2	Foreign Reference	FOR.pdf	1112991 649617f624d0df70a12badd8cbd88d2be437f4de	no	22
Warnings:					
Information:					
3	NPL Documents	NPL.pdf	1489117 c2e087dfe0a8988de63ff7c4a7e7f3d049d5cbf6	no	16
Warnings:					
Information:					
4	Fee Worksheet (PTO-875)	fee-info.pdf	30859 d9b9877d17f228dd08097f79aa08aeeff3021264	no	2
Warnings:					
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		Total Files Size (in bytes):	3245615		

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National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT

Docket Number (Optional): ACQI-010/10US 310578-2052

In re Application of: William W.Y. Chu

Application No.: 12/504,534

Filed: July 16, 2009

For: MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNDIRECTIONAL SERIAL BIT CHANNELS

The owner*, Acqis LLC, of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term **prior patent** No. 7,676,624 as the term of said prior patent is defined in 35 U.S.C. 154 and 173, and as the term of said **prior patent** is presently shortened by any terminal disclaimer. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the prior patent are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the owner does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term as defined in 35 U.S.C. 154 and 173 of the **prior patent**, "as the term of said **prior patent** is presently shortened by any terminal disclaimer," in the event that said **prior patent** later:

- expires for failure to pay a maintenance fee;
- is held unenforceable;
- is found invalid by a court of competent jurisdiction;
- is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
- has all claims canceled by a reexamination certificate;
- is reissued; or
- is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

Check either box 1 or 2 below, if appropriate.

1. ☐ For submissions on behalf of a business/organization (e.g., corporation, partnership, university, government agency, etc.), the undersigned is empowered to act on behalf of the business/organization.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

2. ☒ The undersigned is an attorney or agent of record. Reg. No. 50,834



Signature — January 28, 2011 (Date)

Cliff Z. Liu
Typed or printed name

650 843-5852
Telephone Number

☒ Terminal disclaimer fee under 37 CFR 1.20(d) included.

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*Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner). Form PTO/SB/96 may be used for making this certification. See MPEP § 324.

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Docket Number (Optional)
ACQI-010/10US 310578-2052

In re Application of: William W.Y. Chu

Application No.: 12/504,534

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The owner*, Acqis LLC, of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term **prior patent** No. 7,818,487 as the term of said prior patent is defined in 35 U.S.C. 154 and 173, and as the term of said **prior patent** is presently shortened by any terminal disclaimer. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the prior patent are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

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expires for failure to pay a maintenance fee;
is held unenforceable;
is found invalid by a court of competent jurisdiction;
is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
has all claims canceled by a reexamination certificate;
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is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

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1. ☐ For submissions on behalf of a business/organization (e.g., corporation, partnership, university, government agency, etc.), the undersigned is empowered to act on behalf of the business/organization.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

2. ☒ The undersigned is an attorney or agent of record. Reg. No. 50,834

Signature — January 28, 2011 (Date)

Cliff Z. Liu
Typed or printed name

650 843-5852
Telephone Number

☒ Terminal disclaimer fee under 37 CFR 1.20(d) included.

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Attorney Docket No. ACQI-010/10US 310578-2052 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	William W.Y. Chu	Confirmation No.:	1286
Serial No.:	12/504,534	Group Art Unit:	2111
Filed:	July 16, 2009	Examiner:	Phan, Raymond Ngan

For: MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNDIRECTIONAL SERIAL BIT CHANNELS

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Date of Deposit: January 28, 2011

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Date: January 28, 2011 By: Bobbie Jutras
Bobbie Jutras

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Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. §1.97(c)

In accordance with the duty of disclosure set forth in 37 C.F.R. §1.56, Applicant(s) hereby submits the following information in conformance with 37 C.F.R. §§1.97 and 1.98.

☒ Pursuant to 37 C.F.R. §1.98, a copy of each non-US patent document cited in the attached Form PTO/SB/08 is enclosed in electronic form on a compact disc (CD).

☐ No copies of the publications listed on the attached Form PTO/SB/08 are being provided pursuant to 37 C.F.R. §1.98(d) because the publications were previously cited by or submitted to the Office in prior Application Serial No. _____ to which the above-identified application claims priority under 35 U.S.C. §120.

☐ No copies of any U.S. patents or U.S. patent application publications listed on the attached Form PTO/SB/08 are being provided pursuant to 37 C.F.R. §1.98.

☐ Publications listed on the attached Form PTO/SB/08 were cited in a foreign search or examination report corresponding to application serial no. _____ and mailed on _____

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☐ Enclosed is a copy of a non-English publication(s) _____. Pursuant to §609 of the M.P.E.P., Applicant submits the attached foreign search or examination report, which cites such non-English language publication(s).

☐ Enclosed is a copy of a non-English publication(s) _____ English language publication _____ (copy enclosed) claims priority from this non-English publication.

☐ Enclosed is an explanation of non-English publication(s) _____ for which an English translation is not available.

☐ Enclosed is an English translation of non-English publication(s) _____ cited in the attached Form PTO/SB/08.

☐ Enclosed is a copy of pending patent Application Serial No. _____

This Information Disclosure Statement is filed after the period specified in 37 C.F.R. § 1.97(b), but before the mailing of any of the following:

☒ a final action under 37 C.F.R. §1.113;

☒ a notice of allowance under 37 C.F.R. §1.311; or

☒ an action that otherwise closes prosecution in this application.

In accordance with 37 C.F.R. §1.97(c) also enclosed is:

☒ Fee under 37 C.F.R. §1.17(p) in the amount of $180.00; or

☐ Statement as specified in 37 C.F.R. §1.97(e):

☐ Each item of information contained in the Information Disclosure Statement cited herein was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing date of the Information Disclosure Statement; or

☐ No item of information contained in the Information Disclosure Statement submitted herewith was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the undersigned, having made a reasonable inquiry, no item of information contained in the Information Disclosure Statement was known to any individual designated in 37 C.F.R. §1.56(c) more than three months prior to the filing date of the Information Disclosure Statement.

It is respectfully requested that the Examiner consider the above-noted information and return an initialed copy of the attached Form PTO/SB/08 to the undersigned.

Respectfully submitted,
COOLEY LLP

Date: January 28, 2011

By: _____

Cliff Z. Liu
Reg. No. 50,834

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COOLEY LLP
777 6th Street NW, Suite 1100
Washington, DC 20001

Tel: (650) 843-5852
Fax: (202) 842-7899

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 26

Complete if Known	
Application Number	12/504,534
Filing Date	July 16, 2009
First Named Inventor	William W.Y. Chu
Art Unit	2111
Examiner Name	Phan, Raymond Ngan
Attorney Docket Number	ACQI-010/10US 310578-2052

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	A105	4,141,068	02-20-1979	Mager et al.	
	A104	4,670,837	06-02-1987	Sheets	
	AU002	4,799,258	01-17-1989	Davies	
	AO003	5,103,446	04-07-1992	Fischer	
	AO004	5,191,581	03-02-1993	Woodbury et al.	
	AK002	5,293,487	03-08-1994	Russo et al.	
		5,293,497	03-08-1994	Free	
	AO005	5,519,843	05-21-1996	Moran et al.	
	AU003	5,546,463	08-13-1996	Caputo et al.	
	AO006	5,572,441	11-05-1996	Boie	
	AR001	5,590,377	12-31-1996	Smith	
	AP002	5,623,637	04-22-1997	Jones et al.	
	AO007	5,648,762	07-15-1997	Ichimura et al.	
	A107	5,737,524	04-07-1998	Cohen et al.	
	AO008	5,751,711	05-12-1998	Sakaue	
	AO009	5,838,932	11-17-1998	Alzien	
	A103	5,862,350	01-19-1999	Coulson	
	AO002	5,862,381	01-19-1999	Advani et al.	
	AW001	5,878,211	03-02-1999	Delagrange et al.	
	AR002	5,884,049	03-16-1999	Atkinson	
	AM002	5,930,110	07-27-1999	Nishigaki et al.	
	AO010	5,933,609	08-03-1999	Walker et al.	
	A102	5,965,957	10-12-1999	Bourgeois	
	AR003	5,974,486	10-26-1999	Siddappa	
	AO011	6,006,243	12-21-1999	Karidis	
	AO012	6,012,145	01-04-2000	Mathers et al.	
	AO013	6,046,571	04-04-2000	Bovio et al.	

Examiner Signature		Date Considered	

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Sheet 2 of 26

Complete if Known	
Application Number	12/504,534
Filing Date	July 16, 2009
First Named Inventor	William W.Y. Chu
Art Unit	2111
Examiner Name	Phan, Raymond Ngan
Attorney Docket Number	ACQI-010/10US 310578-2052

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	AM001	6,088,620	07-11-2000	Ninomiya et al.	
	AO014	6,104,921	08-15-2000	Cosley et al.	
	AO015	6,256,689	07-03-2001	Khosrowpour	
	AO016	6,266,539	07-24-2001	Pardo	
	AR004	6,301,637	10-09-2001	Krull et al.	
	AC038	6,498,361 B1	12-24-2002	Osann, Jr.	
	A094	6,578,103 B1	06-10-2003	Hill et al.	
	A106	6,606,253 B2	08-12-2003	Jackson et al.	
	A096	6,664,377 B1	12-16-2003	Xu	
	A012	6,757,748 B1	06-29-2004	Hipp	
	AH001	7,676,624 B2	03-09-2010	Chu	
	AI001	7,818,487 B2	10-19-2010	Chu	
	AQ001	RE41,076 E	01-12-2010	Chu	
	AU001	RE41,092	01-26-2010	Chu	
	AP001	RE41,294 E	04-27-2010	Chu	
	AO001	RE41,961	11-23-2010	Chu	
		2001/0011312 A1	08-02-2001	Chu	
	AG002	2005/0182882 A1	08-18-2005	Chu	
	AJ001	2010/0174844 A1	07-08-2010	Chu	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] "Number[4] "Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	B004	JP 6-289953	10-18-1994	Hitachi, Ltd.		
	BN001	WO 97/00481	01-03-1997	Intel Corporation		

Examiner Signature		Date Considered	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 3 of 26

Complete if Known	
Application Number	12/504,534
Filing Date	July 16, 2009
First Named Inventor	William W.Y. Chu
Art Unit	2111
Examiner Name	Phan, Raymond Ngan
Attorney Docket Number	ACQI-010/10US 310578-2052

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	C004	QuantumNet, Inc., QuantumNet Product Overview [online], 1996 [retrieved on November 16, 2009], Retrieved from the Internet: <URL: http://web.archive.org/web/19971011194003/www.quantumnet.com/products.htm>, 1 page.	
	C005	QuantumNet, Inc., QuantumNet: The Next Generation Computing and Networking Environment [online], 1996 [retrieved on November 16, 2009], Retrieved from the Internet: <URL: http://web.archive.org/web/19971011194123/www.quantumnet.com/qnetovw.htm>, 7 pages.	
	C006	QuantumNet, Inc., QuantumNet 6500 Processor Modules [online], 1996 [retrieved on November 16, 2009], Retrieved from the Internet: <URL:http://web.archive.org/web/19971011194317/www.quantumnet.com/ds6500.htm>, 4 pages.	
	C007	QuantumNet, Inc., QuantumServer Chassis [online], 1996 [retrieved on November 16, 2009], Retrieved from the Internet: <URL: http://web.archive.org/web/19971011194309/www.quantumnet.com/dsq6000.htm>, 3 pages.	
	C009	Cubix Corporation, Datasheet: Single-Board Computers with Pentium Processors [online], 1997 [retrieved on July 31, 2009], Retrieved from the Internet: <URL: http://web.archive.org/web/19970716204717/www.cubix.com/corporate/data/bcp5t.htm>, 5 pages.	
	C010	Cubix Corporation, Datasheet: ERS/FT II Server Chassis [online], 1997 [retrieved on July 31, 2009], Retrieved from the Internet: <URL: http://web.archive.org/web/19970716204623/www.cubix.com/corporate/data/ersft2.htm>, 3 pages.	
	C011	Cubix Corporation, Cubix ERS/FT II Systems [online], 1997 [retrieved on July 31, 2009], Retrieved from the Internet: <URL: http://web.archive.org/web/19980124213320/www.cubix.com/support/steps/ers-ft2/intro.htm>, 5 pages.	
	C012	Cubix Corporation, Cubix Product Catalog, Summer 1995, 56 pages.	
	C013	Cubix Corporation, BC Series, Processor Boards Installation Guide, DOC 800A, August 1994, 149 pages.	
	C014	Cubix Corporation, ERS/FT II - Enhanced Resource Subsystem/Fault Tolerant II, November 1994, 4 pages.	

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Sheet 4 of 26

Complete if Known	
Application Number	12/504,534
Filing Date	July 16, 2009
First Named Inventor	William W.Y. Chu
Art Unit	2111
Examiner Name	Phan, Raymond Ngan
Attorney Docket Number	ACQI-010/10US 310578-2052

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	C015	Cubix Corporation, Density Series Plug-In Servers, Plug-In Computers for Managed Server Farms, September 15, 1998, 2 pages.	
	C016	Cubix Corporation, Cubix Pentium II Plug-In Computers for Density Series Systems, September 15, 1998, 1 page.	
	C017	Cubix Corporation, Density Series Multi-Server Systems, September 10, 1999, 4 pages.	
	C018	Compaq Computer Corporation, White Paper, "Order and Configuration Guide for Compaq ProLiant Cluster Series F Model 100," September 1998, pages 1-8.	
	C019	Compaq Computer Corporation, QuickSpecs, Compaq ProLiant Cluster Series F Model 100, (undated), pages 8-36 to 8-37.	
	C020	Compaq Computer Corporation, Compaq Performance Brief, ProLiant 1600 ServerBench Performance Summary, August 1998, pages 1-7.	
	C021	Compaq Computer Corporation, Compaq ActiveAnswers Installation Guide, Installation and Configuration Guide for Linux and Apache Web Server on Compaq Prosignia and ProLiant Servers, May 1999, pages 1-40.	
	C022	Compaq Computer Corporation, Compaq White Paper, "Microsoft Internet Information Server 4.0 on the Compaq ProLiant 6500," August 1998, pages 1-14.	
	C023	Compaq Computer Corporation, Compaq White Paper, "Accelerating Financial Spreadsheet Simulations with Workstation Clusters," October 1998, pages 1-14.	
	C024	Compaq Computer Corporation, ProLiant 6500-PDC/O1000 C/S with 4 ProLiant 1850R, TPC-C Rev. 3.4, Report Date: Dec. 22, 1998, pages 1-3.	
	C026	Compaq Computer Corporation, Compaq White Paper, "ServerNet - A High Bandwith, Low Latency Cluster Interconnection," September 1998, pages 1-9.	
	C027	JL ChatCom, Inc. - Web Site, JL ChatCom, Inc., ChatterBox Communications and Server Solutions [online], 1996 [retrieved on December 2, 2009], Retrieved from the Internet: <URL: http://web.archive.org/web/19970104221841/http://www.jlchatcom.com/>, 1 page.	
	C028	JL ChatCom, Inc. - Scaleable Application and Communication Servers, "ChatCom, Inc. Announces Complete Line of Scaleable Application and Communication Servers," August 30, 1996 [retrieved on December 2, 2009], JL ChatCom, Inc., ChatterBox Communications and Server Solutions [online], Retrieved from the Internet: <URL: http://web.archive.org/web/19970104221932/www.jlchatcom.com/cpofrel.htm>, 4 pages.	

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Sheet 5 of 26

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First Named Inventor	William W.Y. Chu
Art Unit	2111
Examiner Name	Phan, Raymond Ngan
Attorney Docket Number	ACQI-010/10US 310578-2052

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	C029	JL ChatCom, Inc. - Highly Adaptable Intranet and Web Servers, "ChatCom, Inc. Announces Highly Adaptable Intranet and Web Servers," September 3, 1996 [retrieved on December 2, 2009], JL ChatCom, Inc., ChatterBox Communications and Server Solutions [online], Retrieved from the Internet: <URL: http://web.archive.org/web/19970104221941/www.jlchatcom.com/chat4int.htm>, 2 pages.	
	C030	JL ChatCom, Inc., "ChatPower Plus," 1996 [retrieved on December 2, 2009], JL ChatCom, Inc., ChatterBox Communications and Server Solutions [online], Retrieved from the Internet: <URL: http://web.archive.org/web/19970104222122/www.jlchatcom.com/chatplus.htm>, 3 pages.	
	C031	JL ChatCom, Inc., "ChatterBox ChatPower Plus," (undated) [retrieved on December 2, 2009], JL ChatCom, Inc., ChatterBox Communications and Server Solutions [online], Retrieved from the Internet: <URL: http://web.archive.org/web/19970104222556/www.jlchatcom.com/cpp1.gif>, 1 page.	
	C032	JL ChatCom, Inc., "ChatExpress PB5 Series P166 Pentium PCI/ISA CPU Card," 1996 [retrieved on December 2, 2009], JL ChatCom, Inc., ChatterBox Communications and Server Solutions [online], Retrieved from the Internet: <URL: http://web.archive.org/web/19970104222157/www.jlchatcom.com/chatp599.htm>, 2 pages.	
	C033	JL ChatCom, Inc., "ChatExpress - 2 Slot," [retrieved on December 2, 2009], JL ChatCom, Inc., ChatterBox Communications and Server Solutions [online], Retrieved from the Internet: <URL: http://web.archive.org/web/19970104222644/www.jlchatcom.com/exp2ill.gif>, 1 page.	
	C034	Ziatech Corporation, Ketris 9000, August 1, 2000, 4 pages.	
	C035	Ziatech Corporation, Ketris 9000 System Hardware Manual, 2000, 46 pages.	
	C036	Ziatech Corporation, Ketris Server Blade Hardware Manual, 2000, pages 1-60.	
	C037	Ziatech Corporation, Ketris Media Blade Hardware Manual, 2000, pages 1-17.	
	C038	Ziatech Corporation, Ketris Manager Software Manual, 2000, pages 1-28.	
	C039	Ziatech Corporation, Ketris System Management Overview, June 22, 2000, 4 pages.	
	C041	Ziatech Corporation, STD 32 Star System Multiprocessing Computer System, 1998, 6 pages.	
	C042	Ziatech Corporation, ZT 8907 Single Board Computer with IntelDX4 Microprocessor, 1998, 4 pages.	
	C043	Ziatech Corporation, ZT 8908 Single Board Computer with Pentium Processor or AMD-K6, 1998, 6 pages.	

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Sheet 6 of 26

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Filing Date	July 16, 2009
First Named Inventor	William W.Y. Chu
Art Unit	2111
Examiner Name	Phan, Raymond Ngan
Attorney Docket Number	ACQI-010/10US 310578-2052

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	C044	Ziatech Corporation, System Designer's Guide, Expanding STD Bus Performance Through Multiprocessing, April 1996, 6 pages.	
	C045	Ziatech Corporation, System Designer's Guide, Hot Swap Capability on STD 32 Computers, January 1996, 6 pages.	
	C046	Ziatech Corporation, STD 32 zVID2 Local Bus Super VGA/FPD Adapter, April 1996, 2 pages.	
	C047	Wolfpack or Microsoft Cluster Services on STAR System, (undated), 3 pages.	
	C048	Ziatech Corporation, Ziatech Industrial BIOS for CompactPCI and STD 32 Systems, Software Manual for Industrial BIOS Version 4.7, July 27, 1998, 134 pages.	
	C049	Ziatech Corporation, "New STD 32 Fault Tolerant Computer Provides Modular Platform for 'Non-Stop' Applications," February 5, 1996, 2 pages.	
	C052	Eversys Corporation, System 8000 Consolidated Network Server Product Brief, (undated), 2 pages.	
	C053	Eversys Corporation, System 8000 Consolidated Server, (undated), [retrieved on November 9, 2009], Retrieved from C: drive <path: file://C:\Documents and Settings\Daniel\M Documents\Eversys\Eversys Web Site Master...>, 6 pages.	
	C054	Eversys Corporation, System 8000 Consolidated Server Presentation, (undated), 23 pages.	
	C055	Eversys Corporation, System 8000 Consolidated Network Server, Pentium II Processor Module User's Guide for Module version P2D-BXT, January 1998, 49 pages.	
	C056	Eversys Corporation, EVERSYS System 8000 Peripheral Sharing Switch (PSS) User's Guide, 1st Edition-June 1997, 2nd Edition-January 1998, 17 pages.	
	C057	Eversys Corporation, WebView 8000 version 1.1 User's Guide, Web-Based Management Software fo the EVERSYS System 8000 Consolidated Server, Revision A-November 1998, Revision B-December 1998, 56 pages.	
	C058	Eversys Corporation, S8000 Single Module Body Assemby, October 9, 1998, 9 pages.	
	C059	Eversys CAPserver Product Brief [online], (undated), [retrieved on November 16, 2009], Retrieved from the Internet: <URL: http://web.archive.org/web/19961104093115/www.eversys.com/CAPbrief.htm>, 10 pages.	
	C060	Eversys CAPcard 9500/sa Product Brief [online], (undated), [retrieved on November 16, 2009], Retrieved from the Internet: <URL: http://web.archive.org/web/19961104093144/www.eversys.com/cc95sa_Brief.htm>, 3 pages.	

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Application Number	12/504,534
Filing Date	July 16, 2009
First Named Inventor	William W.Y. Chu
Art Unit	2111
Examiner Name	Phan, Raymond Ngan
Attorney Docket Number	ACQI-010/10US 310578-2052

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	C062	PHILLIPS, J., "9800 Disk Card Design Specification," May 26, 1998, White Cross Systems Limited, pages 1-44.	
	C063	PHILLIPS, J., "9800 Disk Card Layout Specification," April 6, 1998, White Cross Systems Limited, pages 1-22.	
	C064	FEAKES, L., "Disk Connector Card Functional Requirement Specification," January 14, 1998, White Cross Systems Limited, pages 1-4.	
	C065	FEAKES, L., "Disk Connector Card Layout Specification," January 14, 1998, White Cross Systems Limited, pages 1-6.	
	C066	White Cross Systems Limited, WhiteCross Data Exploration Configuration and Maintenance Manual, July 2000, 354 pages.	
	C067	White Cross Systems Limited, WhiteCross Data Exploration, White Paper: R&D 99Q3-01, "WXDES-Technical Information," September 3, 1999, pages 1-38.	
	C068	White Cross Systems Limited, WhiteCross Configuration & Maintenance Manual, November 2002, Version 5.2, 305 pages.	
	C069	BURROW, M., WhiteCross Data Exploration, "A Technical Overview of the WXDES/9800," March 2, 1999, Revision 2.00, White Cross Systems Limited, pages 1-90.	
	C070	White Cross Systems Limited, WhiteCross WX/DES Hardware Maintenance, 2000, pages 1-72.	
	C073	KHAN, M. F., "Ethernet Switch Card Design Specification," March 8, 2001, White Cross Systems Limited, pages 1-32.	
	C074	KHAN, M. F., "Ethernet Switch Card Layout Specifications," March 8, 2001, pages 1-31.	
	C075	SMITH, B., Processor Backplane Functional Requirement Specification, July 31, 1997, White Cross Systems Limited, pages 1- 11.	
	C076	SMITH, B., "Processor Backplane Design Specification," February 3, 1998, White Cross Systems Limited, pages 1-16.	
	C077	SMITH, B., "Processor Backplane Layout Specification," November 12, 1997, White Cross Systems Limited, pages 1-7.	
	C078	PHILLIPS, J., "9800 Processor Card Design Specification," February 25, 1998, White Cross Systems Limited, pages 1-41.	
	C079	PHILLIPS, J., "9800 Processor Card Layout Specification," September 29, 1997, White Cross Systems Limited, pages 1-13.	

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	C080	MIASTKOWSKI, S. (Editor), "A Whale of a System," BYTE, August 1991, 4 pages, Vol. 16, No. 8.	
	C081	Advanced Micro Devices, Inc., "AMD-K6-III Processor Data Sheet," 21918B/0, October 1999, 326 pages.	
	C084	Digital Equipment Corporation, "DIGITAL AlphaServer 4000 and 4100 systems," [Brochure], 1998, 4 pages.	
	C089	EVERSYS, "CAPserver Product Brief" [online], [retrieved on 11-16-2009], Retrieved from the Internet: <URL: http://web.archieve.org/web/19961104093115/www.eversys.com/CAPbrief.htm>, 10 pages.	
	C090	EVERSYS, "CAPcard 9500/sa Product Brief," [online], [retrieved on 11-16-2009], Retrieved from the Internet: <URL: http://web.archieve.org/web/19961104093144/www.eversys.com/cc95sa_Brief.htm>, 3 pages.	
	C100	ELLIS, S., "IRIS FailSafe™ Administrator's Guide," Document Number 007-3109-003, April 6, 1997, 212 pages.	
	C101	Microsoft Cluster Service Center, "MSCS Basics," [online], [retrieved on 02-07-2005]. Retrieved from the Internet at <URL: http://www.nwnetworks.com/mscsbasics.htm>, 6 pages.	
	C103	Novell, Inc., "Novell's NetWare 4.1 Momentum Continues - NetWare 4 Now World's Best-Selling Network Operating System," [online], March 21, 1996, [retrieved on November 16, 2009]. Retrieved from the Internet: <URL: http://www.novell.com/news/press/archive/1996/03/pr96056.html>, 2 pages.	
	C104	Chapter 7: Maintaining the NetWare Server, "Supervising the Network," (undated), pages 514-517.	
	C105	Chapter 7: Designing a Data Protection Plan, (undated), pages 170-171.	
	C106	Concepts, Disk Driver and Disk Duplexing, (undated), pages 82-83.	
	C107	Network Engines, "P6000EXP Fault-tolerant Load-balanced Clustered Server," 1997, 3 pages.	
	C110	Sun Microsystems Computer Company, "Sun™ Enterprise™ 250 Server Owner's Guide," June 1998, Part No. 805-5160-10, Revision A, 324 pages.	
	C111	Sun Microsystems, Inc., "UltraSPARC™ -II CPU Module, Datasheet 400 MHz CPU, 2.0 MP E-Cache," July 1999, 28 pages.	

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	C113	Compaq Computer Corporation, et al., "Universal Serial Bus Specification," September 23, 1998, Revision 1.1, 327 pages.	
	C114	Compaq Computer Corporation, et al., "Universal Serial Bus Specification," April 27, 2000, Revision 2.0, 650 pages.	
	C115	Silicon Graphics International, "Additional Information for: IRIS FailSafe Administrator's Guide (IRIX 6.4)," [online], Document Number: 007-3109-003, Published April 6, 1997, [retrieved on November 5, 2009], Retrieved from the Internet: <URL: http://techpubs.sgi.com/library/tpl/cgi-bin/summary.cgi?coll=0640&db=bks&docnumber=...>, 2 pages.	
	C116	Origin and Onyx Theory of Operations Manual, Document Number 007-3439-002, 1997, Silicon Graphics, Inc., 124 pages.	
	C117	QuantumNet, Inc., QuantumNet 6000 Sharing Modules [online], 1996 [retrieved on November 16, 2009], Retrieved from the Internet: <URL: http://web.archive.org/web/19971011194326/www.quantumnet.com/dsq60xx.htm>, 3 pages.	
	C118	JL ChatCom, Inc., "ChatTwin," [retrieved on December 2, 2009], JL ChatCom, Inc., ChatterBox Communications and Server Solutions [online], Retrieved from the Internet: <URL: http://web.archive.org/web/19970104222644/www.jlchatcom.com/chattwin.htm>, 2 pages.	
	C119	EVERSYS, "Welcome to EverSys" [online], [retrieved on 11-16-2009], Retrieved from the Internet: <URL: http://web.archieve.org/web/19961104092834/www.eversys.com/index2.htm>, 1 page.	
	C120	EVERSYS, "Products" [online], [retrieved on 11-16-2009], Retrieved from the Internet: <URL: http://web.archieve.org/web/19961104093103/www.eversys.com/prodinfo.htm>, 2 pages.	
	C121	"Microsoft Press Computer Dictionary, Third Edition," Microsoft Press, 1997, pages 199 and 332, Kim Fryer ed.	
	C122	Excerpt from "Microsoft Computer Dictionary, 5th Edition", Microsoft Press, 2002, pages 96 and 547	
	C123	Excerpt from IEEE 100: The Authoritative Dictionary of IEEE Standards Terms (7th Ed., 2000), pages 78, 79 and 128	

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Sheet 10 of 26

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First Named Inventor	William W.Y. Chu
Art Unit	2111
Examiner Name	Phan, Raymond Ngan
Attorney Docket Number	ACQI-010/10US 310578-2052

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	C124	ANDERSON, C.R. et al., "IEEE 1355 HS-Links: Present Status and Future Prospects," [online], 1998, [retrieved on 08-11-2010], Retrieved from the Internet: <URL: http://www94.web.cern.ch/HIS/dshs/publications/wotug21/hslink/pdf/hslinkpaper.pdf>, 14 pages.	
	C125	MAMAKOS, L. et al., "Request for Comments 2516 - A method for Transmitting PPP Over Ethernet (PPPoE)," [online], 1999, [retrieved on 08-18-2010], Retrieved from the Internet: <URL: http://ttols.ietf.org/html/rfc2516>, 35 pages.	
	C126	HAAS, S., "The IEEE 1355 Standard: Developments, Performance and Application in High Energy Physics," Thesis for degree of Doctor of Philosophy, University of Liverpool, December 1998, 138 pages.	
	C127	"IEEE Std 1355-1995 Standard for Heterogeneous InterConnect (HIC)," Open Micro-processor systems Initiative (OMI), [online], October 30, 1998, [retrieved on 08-06-2010], Retrieved from the Internet: <URL: http://grouper.ieee.org/groups/1355/index.html>, 6 pages.	
	C128	GALLES, M., "Spider: A Hide-Speed Network Interconnect," IEEE Micro, 1997, pp. 34-39. (6 pages)	
	C129	Excerpt from "Microsoft Computer Dictionary, 4th Edition", Microsoft Press, 1999, pages 184-85, 241, 432 (7 pages)	
	C130	Excerpt from "Microsoft Computer Dictionary, 4th Edition", Microsoft Press, 1999, pages 40, 241, 432 (6 pages)	
	C131	Excerpt from IEEE 100: The Authoritative Dictionary of IEEE Standards Terms (7th Ed., 2000), pages 181,304 and 771.	
	C132	"Family of VME Technology Specifications," [online], date unknown, [retrieved on 12-29-2010], Retrieved from the Internet: <URL: http://www.vita.com/specifications.html>, 1 page.	
	CB001	"SQL Server and NT Cluster Manager Availability Demo," Microsoft WindowsNT Server, Microsoft Server Programmer Developers Conference, Nov. 4-6, 1996, 15 pages.	
	CB004	MPL Brochure, "The First Rugged All-in-One Industrial 486FDX-133 MHz PC," MPL [online], [retrieved on February 16, 2006]. Retrieved from the Internet at <URL: http://www.mpl.ch/DOCs/ds48600.pdf>, 2 pages.	
	CB006	SNYDER, J., "Better Management Through Consolidation," August 18, 1997, Network World [online], [retrieved on June 22, 2004]. Retrieved from the Internet at <URL: http://www.opus1.com/www.jms/nw-con-0818rev.html.>, pp. 1-6.	

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	CB041	GALITZINE, G., "Industrial Computers," April 1999, Internet Telephony Roundup [online], [retrieved on June 23, 2004]. Retrieved from the Internet at <URL: http://www.tmcnet.com/articles/itmag/0499/0499roundup.htm>, 5 pages.	
	CB042	CRYSTAL Group Press Release, "Crystal Group Products Offer Industrial PCs With Built-In Flexibility," March 1, 1997, Crystal Group Inc. [online], [retrieved on May 14, 2004]. Retrieved from the Internet at <URL: http://www.crystalpc.com/news/pressreleases/prodpr.asp>, 2 pages.	
	CB043	DY 4 Systems, Inc. Press Release, "Enhanced COTS SBC from DY 4 Systems Features 166MHz Pentium (TM) Processor," April 8, 1998, [online]. Retrieved from the Internet at <URL: http://www.realtime-info.be/VPR/layout/display/pr.asp?/PRID=363>, 2 pages.	
	CB044	DY 4 Systems, Inc. Product Brochure, "SVME/DMV-192 Pentium® II Single Board Computer," Revision D June 1999, pp. 1-9.	
	CB045	EVERSYS Corporation Web Product Brief, "System 8000," Bomara Associates [online], [retrieved on June 22, 2004]. Retrieved from the Internet at <URL: http://www.bomara.com/Eversys/brief/Default.htm>, 4 pages.	
	CB046	CUBIX Product Brochure, "ERS/FT II System (includes PowerSMP and RemoteServ/IS)," ©2000, Cubix [online], [retrieved on June 22, 2004]. Retrieved from the Internet at <URL: http://64.173.211.7/support/techinfo/system/ersft2/ersft2.htm>, 4 pages.	
	CB047	CUBIX Product Manual, "ERS II and ERS/FT II," Chapter 3, System Components, ©1997, Cubix [online], [retrieved on June 22, 2004]. Retrieved from the Internet at <URL: http://64.173.211.7/support/techinfo/manuals/ers2/ers2-c3.htm>, 21 pages.	
	CB048	CUBIX Product Manual, "ERS II and ERS/FT II," Chapter 6, Component Installation, ©1997, Cubix [online], [retrieved on June 22, 2004]. Retrieved from the Internet at <URL: http://64.173.211.7/support/techinfo/manuals/ers2/ers2-c6.htm>, 18 pages.	
	CB049	NT Enterprise, NT Product Pipeline - Hardware, "Cubix PowerSMP Series 4000," November 1997, Windows Magazine [online], [retrieved on June 22, 2004]. Retrieved from the Internet at <URL: http://www.techweb.com/winmag/library/1997/1101/ntent008.htm>, p. NT07, 1 page.	
	CB050	EVERSYS Corporation Slide Presentation, "Eversys System 8000 Consolidated Network Server, Market and Product Overview," Product to be Released March 1, 2007, [online]. Retrieved from the Internet at <URL: http://eversys.com>, 20 pages.	

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	CB051	CUBIX Customer Service Support System, "Click on the Front Panel That Matches Your System," ©2000, Cubix [online], [retrieved on June 22, 2004]. Retrieved from the Internet at <URL: http://64.173.211.7/support/techinfo/density/density.htm>, 1 page.	
	CC001	MPL Brochure, "The First Rugged All-in-One Industrial 486FDX-133 MHz PC," IMP486/IPM5 User Manual, 1998, 15 pages.	
	CK001	International Search Report for International Patent Application No. PCT/US99/09369, report mailed November 16, 1999, 7 pages.	
	CK002	International Preliminary Examination Report for International Patent Application No. PCT/US99/09369, report completed July 5, 2000, 4 pages.	
	CK003	IBM Corporation, "Grounding Spring for Peripheral Device and Bezel Bracket," IBM Technical Disclosure Bulletin, November 1, 1993, Vol. 36, No. 11, 2 pages.	
	CL001	DIGITAL SEMICONDUCTOR Product Brief, "21152 PCI-to-PCI Bridge," February 1996, 6 pages.	
	CL002	INTEL CORPORATION Architectural Overview, "Intel 430TX PCISET: 82439TX System Controller (MTXC)," February 1997, 4 pages.	
	CL003	INTEL CORPORATION Architectural Overview, "Intel 82371AB PCI-to-ISA/IDE XCELERATOR (PIIX4)," April 1997, 3 pages.	
	CL004	INTEL CORPORATION Advance Information, "Intel 440LX AGPSET: 82443LX PCI A.G.P. Controller (PAC)," August 1997, 4 pages.	
	CL005	NATIONAL SEMICONDUCTOR, "DS90CR215/DS90CR216 +3.3V Rising Edge Data Strobe LVDS 21-Bit Channel Link-66 MHz, July 1997, 2 pages.	
	CL006	NATIONAL SEMICONDUCTOR Product Folder, "DS90CR215 Plus-3.3V Rising Edge Data Strobe LVDS 21-Bit Channel and Link - 66 MHz," National Semiconductor Corporation [online], [retrieved on October 30, 1997]. Retrieved from the Internet at <URL: http://www.national.com/search/search.cgi/design?keywords=DS90CR215>, 2 pages.	
	CL007	VIDEO ELECTRONICS Standards Association (VESA), Plug and Display (P&D) Standard, P&D and Digital Transition Minimized Differential Signaling (TMDS) Video Transmission Overview, 1997, Version 1, Revision 0, pp. 13 & 31-34.	
	CN001	LIQUORMAN, M., "Convergent Technologies Had This Idea," December 5, 1997, Jesse Berst's Anchor Desk [online], [retrieved on July 10, 1998]. Retrieved from the Internet at: <URL: http://www.zdnet.com/anchordesk/talkback/talkback_56555.html>, 1 page.	

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	CN002	BERST, J., "Hope For The Modular PCs We All Really Want," December 5, 1997, Jesse Berst's Anchor Desk [online], [retrieved on July 10, 1998]. Retrieved from the Internet at: <URL: http://www.zdnet.com/anchordesk/story/story_1504.html>, 3 pages.	
	CN003	BOYD-MERRITT, R., "Upgradable-PC Effort Takes Divergent Paths," EE Times - Headline News [online], [retrieved on July 31, 1998]. Retrieved from the Internet at : <URL: http://techweb.cmp.com/eet/news/97/949news/effort.html>, 3 pages.	
	CN004	FAEGRE, D. S. et al., "CTOS Revealed - Unisys' Best-Kept Secret Is An Operating System Built For Distributed Business Applications," December 1994, Core Technologies, BYTE [online], [retrieved on July 10, 1998]. Retrieved from the Internet at: <URL: http://www.byte.com/art/9412/sec13/art2.htm>, 6 pages.	
	CN005	SPANG, K., "Component House: Design Technology for 'PCs in a Snap' - NeoSystems Offers Building Blocks," Computer Reseller News, April 21, 1997, Issue: 732, Section: Channel Assembly, TechWeb [online], [retrieved on July 31, 1998]. Retrieved from the Internet at: <URL: http://www.techweb.com/se/directlink.cgi?CRN19970421S0054>, 2 pages.	
	CN006	"Think Modular," June 10, 1997, PC Magazine [online], [retrieved on July 31, 1998]. Retrieved from the Internet at: <URL: wysiwyg://60/http://homezdnet.com/pcmag/issues/1611/pcmg0072.htm>, 1 page.	
	DA001	Office Action for U.S. Patent No. 6,718,415, mailed October 10, 2002, 7 pages.	
	DA002	Response for U.S. Patent No. 6,718,415, filed November 7, 2002, 9 pages.	
	DA003	Office Action for U.S. Patent No. 6,718,415, mailed January 29, 2003, 7 pages.	
	DA004	Response for U.S. Patent No. 6,718,415, filed March 6, 2003, 8 pages.	
	DA005	Office Action for U.S. Patent No. 6,718,415, mailed June 4, 2003, 8 pages.	
	DA006	Response for U.S. Patent No. 6,718,415, filed September 4, 2003, 10 pages.	
	DB001	Amendment Submitted With RCE for U.S. Patent No. 7,099,981, filed March 1, 2006, 23 pages.	
	DC001	Office Action for U.S. Patent No. 7,363,415, mailed on April 12, 2007, 23 pages.	
	DC002	Response for U.S. Patent No. 7,363,415, filed on April 24, 2007, 25 pages.	
	DD001	Office Action for U.S. Patent No. 7,328,297, mailed February 8, 2007, 5 pages.	
	DD002	Response for U.S. Patent No. 7,328,297, filed April 19, 2007, 32 pages.	
	DD003	Office Action for U.S. Patent No. 7,328,297, mailed July 12, 2007, 13 pages.	
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	DG002	Response for U.S. Patent No. 7,376,779, filed October 16, 2007, 23 pages.	
	DH001	Office Action for U.S. Patent No. 7,676,624, mailed December 1, 2008, 8 pages.	
	DH002	Response for U.S. Patent No. 7,676,624, filed January 13, 2009, 14 pages.	
	DH003	Supplemental Response for U.S. Patent No. 7,676,624, filed on February 6, 2009, 13 pages.	
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	DK002	Response for U.S. Patent No. 6,216,185, filed August 3, 2000, 15 pages.	
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	DL002	Amendment for U.S. Patent No. 6,345,330, filed September 12, 2000, 5 pages.	
	DL003	Restriction Requirement for U.S. Patent No. 6,345,330, mailed December 19, 2000, 5 pages.	
	DL004	Amendment filed with Continued Prosecution Application for U.S. Patent No. 6,345,330, filed January 17, 2001, 5 pages.	
	DL005	Office Action for U.S. Patent No. 6,345,330, mailed March 23, 2001, 6 pages.	
	DL006	Response to Office Action for U.S. Patent No. 6,345,330, filed July 19, 2001, 5 pages.	
	DM001	Office Action for U.S. Patent Application No. 09/642,628, mailed April 5, 2001, 9 pages.	
	DO001	Office Action for U.S. Application No. 10/963,825, mailed October 27, 2005, 25 pages.	
	DO002	Response for U.S. Application No. 10/963,825, filed January 9, 2006, 22 pages.	
	DO003	Office Action for U.S. Application No. 10/963,825, mailed May 31, 2006, 29 pages.	
	DO004	Amendment Submitted with RCE for U.S. Application No. 10/963,825, filed July 27, 2006, 29 pages.	
	DO005	Office Action for U.S. Application No. 10/963,825, mailed October 20, 2006, 28 pages.	

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Sheet 15 of 26

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First Named Inventor	William W.Y. Chu
Art Unit	2111
Examiner Name	Phan, Raymond Ngan
Attorney Docket Number	ACQI-010/10US 310578-2052

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	DO006	Appellants' Brief for U.S. Application No. 10/963,825, filed January 8, 2007, 31 pages.	
	DO007	Revised Appellants' Brief for U.S. Application No. 10/963,825, filed April 20, 2007, 34 pages.	
	DO008	Examiner's Answer for U.S. Application No. 10/963,825, mailed August 8, 2007, 30 pages.	
	DO009	Reply Brief for U.S. Application No. 10/963,825, filed September 4, 2007, 4 pages.	
	DO010	Decision on Appeal for U.S. Application No. 10/963,825, mailed February 4, 2009, 13 pages.	
	DO011	Amendment Submitted with RCE for U.S. Application No. 10/963,825, filed February 20, 2009, 24 pages.	
	DO012	Office Action for U.S. Application No. 10/963,825, mailed May 14, 2009, 5 pages.	
	DO013	Response for U.S. Application No. 10/963,825, filed May 22, 2009, 2 pages.	
	DO014	Office Action for U.S. Application No. 10/963,825, mailed September 15, 2009, 14 pages.	
	DO015	Response for U.S. Application No. 10/963,825, filed October 1, 2009, 7 pages.	
	DP001	Office Action for RE 41,294, mailed November 16, 2007, 10 pages.	
	DP002	Response for RE 41,294, filed December 20, 2007, 21 pages.	
	DP003	Office Action for RE 41,294, mailed April 15, 2008, 10 pages.	
	DP004	Amendment Submitted with RCE for RE 41,294, filed May 27, 2008, 14 pages.	
	DP005	Supplemental Amendment Submitted with RCE for RE 41,294, filed July 8, 2008, 12 pages.	
	DP006	Office Action for RE 41,294, mailed September 16, 2008, 11 pages.	
	DP007	Response for RE 41,294, filed October 30, 2008, 14 pages.	
	DP008	Supplemental Response for RE 41,294, filed February 20, 2009, 13 pages.	
	DP009	Supplemental Response for RE 41,294, filed August 17, 2009, 3 pages.	
	DP010	Examiner Interview Summary Record, mailed January 15, 2009, 1 page.	
	DQ001	Office Action for RE 41,076, mailed July 13, 2007, 38 pages.	
	DQ002	Response for RE 41,076, filed September 26, 2007, 18 pages.	
	DQ003	Office Action for RE 41,076, mailed October 17, 2007, 55 pages.	
	DQ004	Amendment Submitted with RCE for RE 41,076, filed November 5, 2007, 19 pages.	
	DQ005	Office Action for RE 41,076, mailed February 11, 2008, 62 pages.	
	DQ006	Response for RE 41,076, filed April 7, 2008, 18 pages.	
	DQ007	Office Action for RE 41,076, mailed June 9, 2008, 25 pages.	
	DQ008	Amendment Submitted with RCE for RE 41,076, filed December 8, 2008, 44 pages.	
	DQ009	Office Action for RE 41,076, mailed December 30, 2008, 8 pages.	
	DQ010	Response for RE 41,076, filed January 16, 2009, 14 pages.	

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Art Unit	2111
Examiner Name	Phan, Raymond Ngan
Attorney Docket Number	ACQI-010/10US 310578-2052

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	DQ011	Amendment Submitted with RCE for RE 41,076, filed August 4, 2009, 2 pages.	
	DQ012	Examiner Interview Summary Record, mailed February 24, 2009, 4 pages.	
	DQ013	Applicant Summary of Interview, filed March 24, 2009, 1 page.	
	DQ014	Examiner Interview Summary Record, mailed September 22, 2009, 5 pages.	
	DR001	Office Action for U.S. Application No. 12/322,858, mailed March 4, 2010, 24 pages.	
	DR002	Response for U.S. Application No. 12/322,858, filed June 4, 2010, 15 pages.	
	DR003	Office Action for U.S. Application No. 12/322,858, mailed June 25, 2010, 22 pages.	
	DR004	Response for U.S. Application No. 12/322,858, filed October 25, 2010, 12 pages.	
	DS001	Office Action for U.S. Application No. 12/577,074, mailed April 13, 2010, 7 pages.	
	DS002	Response for U.S. Application No. 12/577,074, filed July 13, 2010, 3 pages.	
	DS003	Office Action for U.S. Application No. 12/577,074, mailed November 10, 2010, 6 pages.	
	DT001	Office Action for U.S. Application No. 09/312,199, mailed March 26, 2003, 5 pages.	
	DT002	Response for U.S. Application No. 09/312,199, filed June 11, 2003, 5 pages.	
	DU001	Office Action for RE 41,092, mailed September 17, 2008, 8 pages.	
	DU002	Response for RE 41,092, filed October 27, 2008, 27 pages.	
	DU003	Examiner's Amendment for RE 41,092, mailed November 4, 2009, 4 pages.	
	DV001	Office Action for U.S. Application No. 11/545,056, mailed March 12, 2010, 26 pages.	
	DV002	Response for U.S. Application No. 11/545,056, filed June 14, 2010, 18 pages.	
	DW001	Office Action for U.S. Application No. 12/561,138, mailed September 29, 2010, 4 pages.	
	EA001	Request for Ex Parte Reexamination of US Patent No. 6,216,185, Control No. 90/010,816, filed January 8, 2010, 39 pages.	
	EA002	Request for Ex Parte Reexamination of US Patent No. 6,216,185, Control No. 90/010,816, filed January 8, 2010, Exhibit AA to Request Claim Charts with respect to the Hitachi '953 for Anticipation and Obviousness, 136 pages	
	EA003	Request for Ex Parte Reexamination of US Patent No. 6,216,185, Control No. 90/010,816, filed January 8, 2010, Exhibit BB Claim Charts with respect to Kobayashi for Anticipation and Obviousness, 128 pages	
	EA004	Request for Ex Parte Reexamination of US Patent No. 6,216,185, Control No. 90/010,816, filed January 8, 2010, Exhibit CC Claim Charts with respect to Byte for Anticipation and Obviousness, 122 pages	

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Application Number	12/504,534
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First Named Inventor	William W.Y. Chu
Art Unit	2111
Examiner Name	Phan, Raymond Ngan
Attorney Docket Number	ACQI-010/10US 310578-2052

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	EA005	Request for Ex Parte Reexamination of US Patent No. 6,216,185, Control No. 90/010,816, filed January 8, 2010, Exhibit DD Claim Charts with respect to the Hitachi '675 for Anticipation and Obviousness, 119 pages	
	EA006	Office Action in Ex Parte Reexamination of US Patent No. 6,216,185, Control No. 90/010,816, mailed July 27, 2010, 103 pages	
	EA007	Patent Owner's Response to Office Action in Ex Parte Reexamination of US Patent No. 6,216,185, Control No. 90/010,816, filed September 27, 2010, 55 pages	
	EB001	Request for Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, filed December 2, 2009, 44 pages.	
	EB002	Request for Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, filed December 2, 2009, Exhibit O, Declaration Under 37 CFR 1.132 of Vincent P. Conroy, 11-24-2009, 3 pages.	
	EB003	Request for Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, Replacement Exhibit AA, Claim Charts with respect to QuantumNet for Anticipation and Obviousness, filed January 5, 2010, 109 pages.	
	EB004	Request for Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, Replacement Exhibit BB, Claim Charts with respect to Chatcom for Anticipation and Obviousness, filed January 5, 2010, 91 pages.	
	EB005	Request for Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, Replacement Exhibit CC, Claim Charts with respect to QuantumNet for Anticipation and Obviousness, filed January 5, 2010, 85 pages.	
	EB006	Request for Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, Replacement Exhibit DD, Claim Charts with respect to the Origin2000 Manual for Obviousness, filed January 5, 2010, 72 pages.	
	EB007	Request for Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, Replacement Exhibit EE, Claim Charts with respect to Gallagher for Anticipation and Obviousness, filed January 5, 2010, 107 pages.	
	EB008	Office Action in Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, mailed May 26, 2010, 39 pages.	
	EB009	Patent Owner's Response to Office Action in Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, filed July 27, 2010, 41 pages.	

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Examiner Name	Phan, Raymond Ngan
Attorney Docket Number	ACQI-010/10US 310578-2052

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	EC001	Request for Inter Partes Reexamination of US Patent No. 7,099,981, Control No. 95/001,310, filed February 9, 2010, 33 pages	
	EC002	Request for Inter Partes Reexamination of US Patent No. 7,099,981, Control No. 95/001,310, filed December 2, 2009, Exhibit O, Declaration Under 37 CFR 1.132 of Vincent P. Conroy, 11-24-2009, 3 pages.	
	EC003	Request for Inter Partes Reexamination of US Patent No. 7,099,981, Control No. 95/001,310, Exhibit AA, Claim Charts with respect to Gallagher for Anticipation and Obviousness, filed February 9, 2010, 164 pages	
	EC004	Request for Inter Partes Reexamination of US Patent No. 7,099,981, Control No. 95/001,310, Exhibit BB, Claim Charts with respect to QuantumNet for Anticipation and Obviousness, filed February 9, 2010, 158 pages	
	EC005	Request for Inter Partes Reexamination of US Patent No. 7,099,981, Control No. 95/001,310, Exhibit CC, Claim Charts with respect to Chatcom for Anticipation and Obviousness, filed February 9, 2010, 167 pages	
	EC006	Request for Inter Partes Reexamination of US Patent No. 7,099,981, Control No. 95/001,310, Exhibit DD, Claim Charts with respect to the Eversys for Obviousness, filed February 9, 2010, 111 pages	
	EC007	Office Action in Inter Partes Reexamination of US Patent No. 7,099,981, Control No. 95/001,310, mailed July 6, 2010, 83 pages	
	EC008	Patent Owner's Response to Office Action in Inter Partes Reexamination of US Patent No. 7,099,981, Control No. 95/001,310, filed September 3, 2010, 52 pages	
	EC009	Patent Owner's Response to Office Action in Inter Partes Reexamination of US Patent No. 7,099,981, Control No. 95/001,310, Exhibit A, Declaration of William Henry Mangione-Smith under 37 C.F.R. 1.132, filed September 3, 2010, 63 pages	
	ED001	Request for Inter Partes Reexamination of US Patent No. 7,146,446, Control No. 95/001,328, filed March 19, 2010, 35 pages.	
	ED002	Request for Inter Partes Reexamination of US Patent No. 7,146,446, Control No. 95/001,328, Exhibit AA (Part 1), Claim Charts with respect to Gallagher for Anticipation and Obviousness, filed March 19, 2010, 186 pages.	

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	ED003	Request for Inter Partes Reexamination of US Patent No. 7,146,446, Control No. 95/001,328, Exhibit AA (Part 2), Claim Charts with respect to Gallagher for Anticipation and Obviousness, filed March 19, 2010, 161 pages.	
	ED004	Request for Inter Partes Reexamination of US Patent No. 7,146,446, Control No. 95/001,328, Exhibit BB (Part 1), Claim Charts with respect to QuantumNet for Anticipation and Obviousness, filed March 19, 2010, 139 pages.	
	ED005	Request for Inter Partes Reexamination of US Patent No. 7,146,446, Control No. 95/001,328, Exhibit BB (Part 2), Claim Charts with respect to QuantumNet for Anticipation and Obviousness, filed March 19, 2010, 128 pages.	
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	ED009	Patent Owner's Response to Office Action in Inter Partes Reexamination of US Patent No. 7,146,446, Control No. 95/001,328, Exhibit A, Declaration of William Henry Mangione-Smith under 37 C.F.R. 1.132, filed September 3, 2010, 61 pages.	
	EE001	Request for Inter Partes Reexamination of US Patent No. 7,328,297, Control No. 95/001,336, filed April 19, 2010, 33 pages.	
	EE002	Request for Inter Partes Reexamination of US Patent No. 7,328,297, Control No. 95/001,336, Exhibit AA, Claim Charts with respect to Gallagher for Obviousness, filed April 19, 2010, 131 pages.	
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 20 of 26

Complete if Known	
Application Number	12/504,534
Filing Date	July 16, 2009
First Named Inventor	William W.Y. Chu
Art Unit	2111
Examiner Name	Phan, Raymond Ngan
Attorney Docket Number	ACQI-010/10US 310578-2052

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	EE006	Patent Owner's Response to Office Action in Inter Partes Reexamination of US Patent No. 7,328,297, Control No. 95/001,336, filed October 4, 2010, 49 pages.	
	EE007	Patent Owner's Response to Office Action in Inter Partes Reexamination of US Patent No. 7,328,297, Control No. 95/001,336, Exhibit A, Declaration of William Henry Mangione-Smith under 37 C.F.R. 1.132, filed October 4, 2010, 61 pages.	
	EF001	Request for Inter Partes Reexamination of US Patent No. 7,363,415, Control No. 95/001,424, filed August 25, 2010, 34 pages.	
	EF002	Request for Inter Partes Reexamination of US Patent No. 7,363,415, Control No. 95/001,424, Exhibit AA, Claim Charts with respect to Gallagher and Other References for Obviousness, filed August 25, 2010, 114 pages.	
	EF003	Request for Inter Partes Reexamination of US Patent No. 7,363,415, Control No. 95/001,424, Exhibit AB, Claim Charts with respect to Gallagher and Other References for Obviousness, filed August 25, 2010, 92 pages.	
	EF004	Request for Inter Partes Reexamination of US Patent No. 7,363,415, Control No. 95/001,424, Exhibit BA, Claim Charts with respect to QuantumNet and Other References for Obviousness, filed August 25, 2010, 121 pages.	
	EF005	Request for Inter Partes Reexamination of US Patent No. 7,363,415, Control No. 95/001,424, Exhibit BB, Claim Charts with respect to QuantumNet and Other References for Obviousness, filed August 25, 2010, 99 pages.	
	EF006	Request for Inter Partes Reexamination of US Patent No. 7,363,415, Control No. 95/001,424, Exhibit CA, Claim Charts with respect to Chatcom and Other References for Obviousness, filed August 25, 2010, 91 pages.	
	EF007	Request for Inter Partes Reexamination of US Patent No. 7,363,415, Control No. 95/001,424, Exhibit CB, Claim Charts with respect to Chatcom and Other References for Obviousness, filed August 25, 2010, 94 pages.	
	EF008	Office Action in Inter Partes Reexamination of US Patent No. 7,363,415, Control No. 95/001,424, mailed November 1, 2010, 75 pages.	
	EG001	Request for Inter Partes Reexamination of US Patent No. 7,376,779, Control No. 95/001,475, filed October 27, 2010, 35 pages.	
	EG002	Request for Inter Partes Reexamination of US Patent No. 7,376,779, Control No. 95/001,475, Exhibit AA, Claim Charts with respect to Gallagher and Other References for Obviousness, filed October 27, 2010, 128 pages.	

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Examiner Name	Phan, Raymond Ngan
Attorney Docket Number	ACQI-010/10US 310578-2052

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	EG003	Request for Inter Partes Reexamination of US Patent No. 7,376,779, Control No. 95/001,475, Exhibit AB, Claim Charts with respect to Gallagher and Other References for Obviousness, filed October 27, 2010, 153 pages.	
	EG004	Request for Inter Partes Reexamination of US Patent No. 7,376,779, Control No. 95/001,475, Exhibit BA, Claim Charts with respect to QuantumNet and Other References for Obviousness, filed October 27, 2010, 108 pages.	
	EG005	Request for Inter Partes Reexamination of US Patent No. 7,376,779, Control No. 95/001,475, Exhibit BB, Claim Charts with respect to QuantumNet and Other References for Obviousness, filed October 27, 2010, 112 pages.	
	EG006	Request for Inter Partes Reexamination of US Patent No. 7,376,779, Control No. 95/001,475, Exhibit CA, Claim Charts with respect to Chatcom and Other References for Obviousness, filed October 27, 2010, 112 pages.	
	EG007	Request for Inter Partes Reexamination of US Patent No. 7,376,779, Control No. 95/001,475, Exhibit CB, Claim Charts with respect to Chatcom and Other References for Obviousness, filed October 27, 2010, 118 pages.	
	EG008	Office Action in Inter Partes Reexamination of US Patent No. 7,376,779, Control No. 95/001,475, mailed December 20, 2010, 105 pages.	
	EH001	Request for Inter Partes Reexamination of US Patent No. 7,363,416, Control No. 95/001,476, filed October 27, 2010, 37 pages.	
	EH002	Request for Inter Partes Reexamination of US Patent No. 7,363,416, Control No. 95/001,476, Exhibit AA, Claim Charts with respect to Gallagher and Other References for Obviousness, filed October 27, 2010, 70 pages.	
	EH003	Request for Inter Partes Reexamination of US Patent No. 7,363,416, Control No. 95/001,476, Exhibit AB, Claim Charts with respect to Gallagher and Other References for Obviousness, filed October 27, 2010, 64 pages.	
	EH004	Request for Inter Partes Reexamination of US Patent No. 7,363,416, Control No. 95/001,476, Exhibit BA, Claim Charts with respect to QuantumNet and Other References for Obviousness, filed October 27, 2010, 64 pages.	
	EH005	Request for Inter Partes Reexamination of US Patent No. 7,363,416, Control No. 95/001,476, Exhibit BB, Claim Charts with respect to QuantumNet and Other References for Obviousness, filed October 27, 2010, 71 pages.	

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Sheet 22 of 26

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Filing Date	July 16, 2009
First Named Inventor	William W.Y. Chu
Art Unit	2111
Examiner Name	Phan, Raymond Ngan
Attorney Docket Number	ACQI-010/10US 310578-2052

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	EH006	Request for Inter Partes Reexamination of US Patent No. 7,363,416, Control No. 95/001,476, Exhibit CA, Claim Charts with respect to Chatcom and Other References for Obviousness, filed October 27, 2010, 64 pages.	
	EH007	Request for Inter Partes Reexamination of US Patent No. 7,363,416, Control No. 95/001,476, Exhibit CB, Claim Charts with respect to Chatcom and Other References for Obviousness, filed October 27, 2010, 67 pages.	
	EH008	Office Action in Inter Partes Reexamination of US Patent No. 7,363,416, Control No. 95/001,476, mailed December 6, 2010, 63 pages.	
	IC01	"Defendants' Amended Invalidity Contentions," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 18 pages.	
	IC02	"Exhibit A (Asserted Claims)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 2 pages.	
	IC03	"Exhibit B - Table 1," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 75 pages.	
	IC04	"Exhibit C," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 2 pages.	
	IC05	"Exhibit D," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 106 pages.	
	IC06	"Exhibit E," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 2 pages.	
	IC07	"Invalidity Chart for Base Reference IBM 8260," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 53 pages.	
	IC08	"Invalidity Chart for Base Reference IBM 8265," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 56 pages.	
	IC09	"Invalidity Chart for Base Reference U.S. Patent No. 4,453,215 (Reid)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 56 pages.	

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Sheet 23 of 26

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Application Number	12/504,534
Filing Date	July 16, 2009
First Named Inventor	William W.Y. Chu
Art Unit	2111
Examiner Name	Phan, Raymond Ngan
Attorney Docket Number	ACQI-010/10US 310578-2052

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	IC10	"Invalidity Chart for Base Reference Origin2000," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 56 pages.	
	IC11	"Invalidity Chart for Base Reference QuantumNet," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 49 pages.	
	IC12	"Invalidity Chart for Base Reference U.S. Patent No. 6,564,274 (Heath)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 57 pages.	
	IC13	"Invalidity Chart for Base Reference U.S. Patent No. 5,577,205," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 60 pages.	
	IC14	"Invalidity Chart for Base Reference U.S. Patent No. 5,802,391," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 61 pages.	
	IC15	"Invalidity Chart for Base Reference U.S. Patent No. 6,715,100," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 64 pages.	
	IC16	"Invalidity Chart for Base Reference Cubix BC/Density," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 64 pages.	
	IC17	"Invalidity Chart for Base Reference JP6-289956," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 62 pages.	
	IC18	"Invalidity Chart for Base Reference Gallagher 068 and Gallagher 503," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 108 pages.	
	IC19	"Invalidity Chart for Base Reference Compaq ProLiant Cluster," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 81 pages.	

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	IC20	"Invalidity Chart for Base Reference U.S. Patent No. 5,325,517 to Baker et al. (Appendix 1, Exhibit 15)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 59 pages.	
	IC21	"Invalidity Chart for Japanese Patent Application H7-64672 (Toshiba '672)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 55 pages.	
	IC22	"Invalidity Chart for Base Reference ChatCom," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 52 pages.	
	IC23	"Invalidity Chart for Base Reference Ziatech Corp. Ketris 9000 System," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 68 pages.	
	IC24	"Invalidity Chart for Base Reference Ziatech STD 32 Star System," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 62 pages.	
	IC25	"Invalidity Chart for Base Reference U.S. Patent No. 7,339,786 (Bottom et al.)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 57 pages.	
	IC26	"Invalidity Chart for Base References RLX Patents, U.S. Patent Nos. 6,747,878, 6,411,506, 6,325,636, 6,757,748, and 6,985,967 (Hipp et al.)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 58 pages.	
	IC27	"Invalidity Chart for Base Reference Network Engines P6000 Server," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 59 pages.	
	IC28	"Invalidity Chart for Base Reference Eversys 8000 System," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 60 pages.	
	IC29	"Invalidity Chart for Base Reference Eversys CAPserver," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 59 pages.	

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	IC30	"Invalidity Chart for Base Reference U.S. 5,809,262," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 62 pages.	
	IC31	"Invalidity Chart for Base Reference WhiteCross 9800 System," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 62 pages.	
	IC32	"Invalidity Chart for Base Reference U.S. 5,339,408," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 61 pages.	
	IC33	"Invalidity Chart for Base Reference Tyuluman 536," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 76 pages.	
	IC34	"Invalidity Chart for Base Reference Hong 737," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 77 pages.	
	IC35	"Invalidity Chart for Base Reference U.S. 5,436,857 (Nelson)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 6 pages.	
	IC36	"Invalidity Chart for Base Reference U.S. 5,999,952 (Jenkins)", submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 6 pages.	
	IC37	"Invalidity Chart for Base Reference U.S. 5,608,608 (Flint)", submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 6 pages.	
	IC38	"Invalidity Chart for Base Reference U.S. 5,978,821 (Freeny)", submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 6 pages.	
	IC39	"Invalidity Chart for Base Reference WO 92/18924 (Wallsten)", submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 6 pages.	

Examiner Signature		Date Considered	

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This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 26 of 26

Complete if Known	
Application Number	12/504,534
Filing Date	July 16, 2009
First Named Inventor	William W.Y. Chu
Art Unit	2111
Examiner Name	Phan, Raymond Ngan
Attorney Docket Number	ACQI-010/10US 310578-2052

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	IC40	"Invalidity Chart for Base Reference Ergo Moby Brick", submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 5 pages.	
	IC41	"Invalidity Chart for Base Reference U.S. Patent No. 5,463,742 (Kobayashi)", submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 5 pages.	
	IC42	"Invalidity Chart for Base Reference Japanese Patent Application Publication H6-289953 (Hitachi)", submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 5 pages.	
	IC43	"Invalidity Chart for Base Reference Japanese Patent Application Publication H7-84675 (Hitachi)", submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 5 pages.	
	IC44	"Invalidity Chart for Base Reference U.S. Patent No. 5,187,645 (Spalding)", submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 6 pages.	
	IC45	"Defendants' Notice of Errata Relating to Defendants' P.R. 3-3 Invalidity Contentions," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 14 pages.	
	IF01	"Exhibit 5 - Disclosure of Asserted Claims and Infringement Contentions", submitted by the Plaintiff in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED, 14 pages.	
	F01	"Memorandum Opinion and Order Construing Claim Terms and Denying Defendants' Motion for Partial Summary Judgment," Issued by the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on August 2, 2010, 18 pages.	
	H01	"Transcript of Videotaped Deposition of William Mangione-Smith," taken by the Defendants in connection with Case No. 6:09-cv-148-LED in the U.S. District Court for the Eastern District of Texas, September 9, 2010, 192 pages.	

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This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: **Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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March 8, 2004

OPAP IAP4 JAN 28 2011 PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	William W.Y. Chu	Confirmation No.:	1286
Serial No.:	12/504,534	Examiner:	Phan , Raymond Ngan
Filed:	July 16, 2009	Group Art Unit:	2111

For: MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNIDIRECTIONAL SERIAL BIT CHANNELS

Express Mail Label Number: EV 602682073 US
Date of Deposit: January 28, 2011

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to the Director of Patents, PO Box 1450, Alexandria, VA 22318-1450

Date: January 28, 2011 By: Bobbie Jutras
Bobbie Jutras

Mail Stop: Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT

In response to the Office Action mailed October 28, 2010, please amend the subject application as follows:

Amendments to the Specification begin on page 2 of this paper.

Remarks begin on page 3 of this paper.

IN THE SPECIFICATION

Please replace the title with the following amended title. The amendments to the title are indicated by strikethrough and underlining.

MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNIDIRECTIONAL SERIAL BIT CHANNELS TO TRANSMIT ENCODED PERIPHERAL COMPONENT INTERCONNECT BUS TRANSACTION DATA

REMARKS

Claims 1-83 are pending in the subject application. No claim amendments are being submitted with this paper.

The Examiner has objected to the title of the subject application. Applicant is amending the title to be more descriptive.

The Examiner has rejected certain claims on the ground of nonstatutory obviousness-type double patenting as allegedly unpatentable over certain claims of U.S. Patent No. 7,818,487 and U.S. Patent No. 7,676,624. In an effort to expedite the prosecution of the subject application (and without in any way conceding as to the substance of the rejections), Applicant is submitting herewith Terminal Disclaimers over the two issued patents, and respectfully requests withdrawal of the double patenting rejections.

Claims 19-27, 34-43, and 67-72 were allowed. Applicant respectfully submits that these claims remain allowable.

Conclusion

Accordingly, in view of the foregoing amendments and remarks, Applicant respectfully submits that the subject application is now in condition for allowance. The Examiner is invited to contact the undersigned if there are any residual issues that can be resolved through a telephone call.

The Commissioner is hereby authorized to charge any required fees and to credit any overpayments to Cooley LLP's deposit account No. 50-1283.

Respectfully submitted,
COOLEY LLP

Date: January 28, 2011

By: _____
Cliff Z. Liu
Reg. No. 50,834

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Washington, DC 20001
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:	CHU, William W. Y.	Confirmation No.:	1286
Serial No.:	12/504,534	Group Art Unit:	2111
Filed:	July 16, 2009	Examiner:	Phan , Raymond Ngan

For: MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNIDIRECTIONAL SERIAL BIT CHANNELS TO TRANSMIT ENCODED PERIPHERAL COMPONENT INTERCONNECT BUS TRANSACTION DATA

Mail Stop: Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT

In response to the Office Action mailed October 28, 2010, please amend the subject application as follows:

Amendments to the Claims are reflected in the listing of the claims which begins on page 2 of this paper.

Remarks begin on page 22 of this paper.

The Director is hereby authorized to charge any appropriate fees under 37 C.F.R. §§1.16, 1.17, and 1.21 that may be required by this paper, and to credit any overpayment, to Deposit Account No. 50-1283.

IN THE CLAIMS

1. (Original) A computer system comprising:

a console comprising

a plurality of coupling sites,

a serial communication hub controller, and

an enclosure housing the coupling sites and the serial communication hub controller; and

a plurality of computer modules coupled to respective ones of the coupling sites, at least one of the computer modules comprising

a processing unit,

a main memory coupled to the processing unit,

a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels to transmit data in opposite directions,

a serial controller coupled to the serial communication hub controller, and

a first interface controller coupled to the LVDS channel to communicate an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction.

2. (Original) The computer system of claim 1, wherein the computer modules are similar in design to each other.

3. (Original) The computer system of claim 1, wherein the console further comprises a second interface controller to communicate with the at least one of the computer modules through the LVDS channel.

4. (Original) The computer system of claim 1, wherein the console further comprises a hard disk drive coupled to the at least one of the computer modules.

5. (Original) A computer system comprising:

a console comprising

a plurality of coupling sites, and

an enclosure housing the coupling sites; and

a plurality of computer modules coupled to respective ones of the coupling sites, each of the computer modules comprising

a processing unit,

a main memory coupled to the processing unit,

a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels in opposite directions,

an Ethernet controller to communicate with an external network, and

a first interface controller coupled to the LVDS channel to communicate an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction.

6. (Original) The computer system of claim 5, wherein the computer modules are similar in design to each other.

7. (Original) The computer system of claim 5, wherein the console further comprises a second interface controller to communicate with the first interface controller of at least one of the computer modules through the LVDS channel of the at least one of the computer modules.

8. (Original) The computer system of claim 5, wherein the console further comprises an Ethernet hub controller coupled to the Ethernet controller of at least one of the computer modules to communicate with the external network.

9. (Original) A computer system comprising:

a console comprising

a plurality of coupling sites, each of the coupling sites comprising a slot,

a power supply, and

an enclosure housing the coupling sites and the power supply; and

a plurality of computer modules, each of the computer modules coupled to a respective one of the coupling sites through the slot of the respective one of the coupling sites, each of the computer modules comprising

a processing unit,

a main memory coupled to the processing unit,

a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels in opposite directions, and

an interface controller coupled to the LVDS channel to transmit encoded Peripheral Component Interconnect (PCI) bus transaction data,

wherein the computer modules receive power from the power supply upon coupling to the console.

10. (Original) The computer system of claim 9, wherein the computer modules are similar in design to each other.

11. (Original) The computer system of claim 9, wherein at least one of the computer modules further comprises an Ethernet controller to communicate with an external network.

12. (Original) The computer system of claim 9, wherein the console further comprises a mass storage device that is shared between the computer modules.

13. (Original) A computer system comprising:

a console comprising

a plurality of coupling sites,

a power supply,

a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels in opposite directions,

an interface controller coupled to the LVDS channel to communicate an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction, and

an enclosure housing the coupling sites, the power supply, the LVDS channel, and the interface controller; and

a computer module coupled to one of the coupling sites and comprising

a processing unit,

a main memory coupled to the processing unit, and

a mass storage device coupled to the processing unit,

wherein the computer module receives power from the power supply for operation.

14. (Original) The computer system of claim 13, wherein the mass storage device comprises a flash memory.

15. (Original) The computer system of claim 13, wherein the computer module further comprises a serial controller coupled to the console for data communication.

16. (Original) A computer system comprising:

a console comprising

a plurality of coupling sites, each of the coupling sites comprising a connector,

a pair of unidirectional, multiple serial bit, low voltage differential signal (LVDS) channels to transmit encoded Peripheral Component Interconnect (PCI) bus transaction data in opposite directions, and

an enclosure housing the coupling sites and the LVDS channels; and

a computer module coupled to one of the coupling sites through the connector of the one of the coupling sites, the computer module comprising

a processing unit,

a main memory coupled to the processing unit,

a mass storage device comprising a flash memory, and

a serial communication controller,

wherein the serial communication controller is coupled to the console for data communication upon coupling of the computer module to the console.

17. (Original) The computer system of claim 16, wherein the data communication of the serial communication controller comprises Universal Serial Bus (USB) communication.

18. (Original) The computer system of claim 16, wherein the computer module further comprises a computing environment for a personal computer user.

19. (Original) A computer system comprising:

a console comprising

a plurality of coupling sites, at least one of the coupling sites comprising a connector,

a Digital Versatile Disk (DVD) drive,

a first differential signal channel comprising a pair of unidirectional, serial bit channels to transmit data in opposite directions, and

an enclosure housing the coupling sites, the DVD drive, and the first differential signal channel; and

a computer module coupled to the at least one of the coupling sites through the connector, the computer module comprising

a processing unit,

a main memory coupled to the processing unit,

a mass storage device comprising a flash memory,

a second differential signal channel comprising a pair of unidirectional, serial bit channels to transmit data in opposite directions, and

an interface controller coupled to the console through the second differential signal channel and the connector,

wherein the first differential signal channel and the second differential signal channel are coupled to each other upon insertion of the computer module into the console.

20. (Original) The computer system of claim 19, wherein the computer module further comprises a computing environment for a personal computer user.

21. (Original) The computer system of claim 19, wherein the console further comprises a power supply, and the computer module receives power from the power supply upon insertion of the computer module into the console.

22. (Original) A computer system comprising:

a console comprising

a plurality of coupling sites, each of the coupling sites comprising a connector,

a power supply,

an integrated Liquid Crystal Display (LCD),

a first differential signal channel comprising a pair of unidirectional, serial bit channels to transmit data in opposite directions, and

an enclosure housing the coupling sites, the power supply, the LCD, and the first differential signal channel; and

a computer module coupled to one of the coupling sites through the connector of the one of the coupling sites, the computer module comprising

a processing unit,

a main memory coupled to the processing unit,

a mass storage device comprising a flash memory, and

a second differential signal channel comprising a pair of unidirectional, serial bit channels to transmit data in opposite directions,

wherein the first differential signal channel and the second differential signal channel are coupled to each other upon insertion of the computer module into the console, and the computer module is at least partially powered by the power supply for operation.

23. (Original) The computer system of claim 22, wherein the computer module further comprises a computing environment for a personal computer user.

24. (Original) The computer system of claim 22, wherein the console further comprises a Digital Versatile Disk (DVD) drive.

25. (Original) A computer system comprising:

a console comprising

a plurality of coupling sites, each of the coupling sites comprising a connector, and

a first pair of unidirectional, multiple bit, low voltage differential signal (LVDS) channels to transmit encoded Peripheral Component Interconnect (PCI) bus transaction as serial data along a pair of directions that are different from each other; and

a computer module coupled to one of the coupling sites through the connector of the one of the coupling sites, the computer module comprising

a processing unit,

a main memory coupled to the processing unit,

a mass storage device coupled to the processing unit,

a second pair of unidirectional, multiple bit, LVDS channels to transmit encoded PCI bus transaction as serial data along a pair of directions that are different from each other, and

an interface controller coupled to the second pair of LVDS channels,

wherein the interface controller is coupled to the console for data communication upon coupling of the computer module to the console.

26. (Original) The computer system of claim 25, wherein the console further comprises a Digital Versatile Disk (DVD) drive.

27. (Original) The computer system of claim 25, wherein the computer module further comprises a password mechanism to control access to the computer module.

28. (Original) A computer system comprising:

a console comprising

a plurality of coupling sites, each of the coupling sites comprising a slot,

a mass storage device, and

an enclosure housing the coupling sites and the mass storage device; and

a plurality of computer modules, each of the computer modules coupled to a respective one of the coupling sites through the slot of the respective one of the coupling sites, each of the computer modules comprising

a processing unit,

a main memory coupled to the processing unit,

a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels in opposite directions,

a serial communication controller, and

an interface controller coupled to the LVDS channel to transmit encoded Peripheral Component Interconnect (PCI) bus transaction data,

wherein the computer modules are similar in design to each other, and wherein the mass storage device is coupled to the computer modules during operation.

29. (Original) The computer system of claim 28, wherein the serial communication controller of at least one of the computer modules is coupled to the console for data communication.

30. (Original) The computer system of claim 28, wherein the console further comprises a power supply to supply power to the computer modules.

31. (Original) A computer system comprising:

a console comprising

a plurality of coupling sites, each of the coupling sites comprising a slot,

a mass storage device, and

an enclosure housing the coupling sites and the mass storage device; and

a plurality of computer modules, each of the computer modules coupled to a respective one of the coupling sites through the slot of the respective one of the coupling sites, at least one of the computer modules comprising

a processing unit,

a main memory coupled to the processing unit,

a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels in opposite directions,

a serial communication controller, and

an interface controller coupled to the LVDS channel to transmit encoded Peripheral Component Interconnect (PCI) bus transaction data,

wherein the computer modules are similar in design to each other, and wherein the at least one of the computer modules is configured to provide protection against failure of another one of the computer modules.

32. (Original) The computer system of claim 31, wherein the serial communication controller of the at least one of the computer modules is coupled to the console for data communication.

33. (Original) The computer system of claim 31, wherein the mass storage device is coupled to the computer modules upon insertion of the computer modules into the console.

34. (Original) A computer system comprising:

a plurality of coupling sites;

a power supply;

a low voltage differential signal (LVDS) channel associated with at least one of the coupling sites, the LVDS channel comprising two sets of unidirectional, multiple serial bit channels in opposite directions;

a first interface controller associated with the at least one of the coupling sites and coupled to the LVDS channel to communicate an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction; and

a plurality of computer modules coupled to respective ones of the coupling sites, at least one of the computer modules comprising

a processing unit,

a main memory coupled to the processing unit, and

a second interface controller coupled to the first interface controller through the LVDS channel,

wherein the computer modules receive power from the power supply for operation.

35. (Original) The computer system of claim 34, wherein at least one of the computer modules further comprises an Ethernet controller to communicate with an external network.

36. (Original) The computer system of claim 34, wherein the computer system further comprises a mass storage device that is shared between the computer modules.

37. (Original) A computer system comprising:

a console comprising

a first coupling site,

a second coupling site,

a power supply,

a first low voltage differential signal (LVDS) channel associated with the first coupling site, the first LVDS channel comprising two sets of unidirectional, multiple serial bit channels in opposite directions,

a second LVDS channel associated with the second coupling site, the second LVDS channel comprising two sets of unidirectional, multiple serial bit channels in opposite directions,

a first interface controller coupled to at least one of the first LVDS channel and the second LVDS channel to communicate an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction, and

an enclosure housing the first coupling site, the second coupling site, the power supply, the first LVDS channel, the second LVDS channel, and the first interface controller.

38. (Original) The computer system of claim 37, further comprising:

a first computer module coupled to the first coupling site; and

a second computer module coupled to the second coupling site,

wherein at least one of the first computer module and the second computer module comprises

a processing unit,

a main memory coupled to the processing unit, and

a second interface controller to communicate with the console through one of the first LVDS channel and the second LVDS channel.

39. (Original) The computer system of claim 38, wherein each of the first computer module and the second computer module receives power from the power supply for operation.

40. (Original) A computer system comprising:

a console comprising

a coupling site,

a power supply,

a first low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels in opposite directions to communicate an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction,

a second differential channel associated with the coupling site, the second differential channel comprising two sets of unidirectional, serial bit channels in opposite directions,

a first interface controller coupled to the second differential channel, and

an enclosure housing the coupling site, the power supply, the first LVDS channel, the second differential channel, and the first interface controller.

41. (Original) The computer system of claim 40, further comprising:

a computer module coupled to the coupling site,

wherein the computer module comprises

a processing unit,

a main memory coupled to the processing unit, and

a second interface controller to communicate, via Universal Serial Bus (USB) communication, with the console through the second differential channel.

42. (Original) The computer system of claim 41, wherein the computer module receives at least partial power from the power supply of the console for operation upon coupling to the console.

43. (Original) The computer system of claim 41, wherein the computer module further comprises a computing environment for a personal computer user.

44. (Currently Amended) A computer module insertable into a coupling site of a console for data communication, comprising:

a main circuit board;

a processing unit coupled to the main circuit board;

a main memory coupled to the processing unit;

a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels to transmit data in opposite directions for communicating an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction; and

a peripheral bridge directly coupled to the processing unit, the peripheral bridge comprising an interface controller directly coupled to the LVDS channel.

45. (Previously Presented) The computer module of claim 44, further comprising a removable hard disk drive.

46. (Previously Presented) The computer module of claim 44, further comprising a serial communication controller to couple to the console for data communication.

47. (Previously Presented) The computer module of claim 46, wherein the data communication of the serial communication controller comprises Ethernet communication.

48. (Previously Presented) The computer module of claim 46, wherein the data communication of the serial communication controller comprises Universal Serial Bus (USB) communication.

49. (Previously Presented) The computer module of claim 44, wherein the computer module is configured to operate upon receiving power from the console.

50. (Previously Presented) The computer module of claim 44, further comprising an enclosure housing the main circuit board, the processing unit, the main memory, the LVDS channel, and the interface controller, and the enclosure is insertable into the coupling site of the console.

51. (Previously Presented) The computer module of claim 44, further comprising a connector distinct from the main circuit board, and the connector is configured to couple to the coupling site of the console for data communication.

52. (Previously Presented) The computer module of claim 51, wherein the interface controller is configured to communicate the encoded serial bit stream of PCI bus transaction through the LVDS channel and the connector.

53. (Previously Presented) A computer module comprising:

an enclosure insertable into a slot of a console for guidance to a first connector of the console for operation;

a processing unit housed in the enclosure;

a main memory coupled to the processing unit and housed in the enclosure;

an Ethernet controller coupled to the processing unit and housed in the enclosure;

a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels to transmit data in opposite directions;

a second connector configured to couple to the first connector of the console; and

an interface controller housed in the enclosure and coupled to the second connector through the LVDS channel for communicating an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction.

54. (Previously Presented) The computer module of claim 53, wherein the Ethernet controller is configured to couple to the first connector of the console for data communication.

55. (Previously Presented) The computer module of claim 54, wherein the Ethernet controller is coupled to the second connector.

56. (Previously Presented) The computer module of claim 54, wherein the Ethernet controller is configured to communicate with an external network through the console.

57. (Previously Presented) The computer module of claim 53, wherein the computer module is configured to operate only upon receiving power from the console.

58. (Previously Presented) The computer module of claim 53, wherein the enclosure defines a set of grooves to engage a corresponding set of rails of the slot of the console.

59. (Previously Presented) A computer module comprising:

a main circuit board;

a first connector distinct from the main circuit board;

a processing unit coupled to the main circuit board;

a main memory coupled to the processing unit;

a hard disk drive coupled to the processing unit;

a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels to transmit data in opposite directions; and

an interface controller coupled to the LVDS channel and the first connector for communicating an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction,

wherein the computer module is configured to engage rails on opposite sides of a slot of a console for guidance towards a second connector of the console.

60. (Previously Presented) The computer module of claim 59, wherein the LVDS channel is configured to couple to the console.

61. (Previously Presented) The computer module of claim 59, wherein the first connector of the computer module is configured to mate with the second connector of the console upon the computer module being inserted into the console for operation.

62. (Previously Presented) The computer module of claim 61, wherein the LVDS channel is configured to couple to the console through the first connector of the computer module and the second connector of the console.

63. (Previously Presented) A computer module comprising:

a processing unit;

a main memory coupled to the processing unit;

a mass storage device coupled to the processing unit;

a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels to transmit data in opposite directions for communicating an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction; and

a serial communication controller configured to couple to a console,

wherein the computer module is insertable into a slot of the console for guidance to a connector of the console for serial data communication.

64. (Previously Presented) The computer module of claim 63, wherein the mass storage device comprises a SCSI hard disk drive.

65. (Previously Presented) The computer module of claim 63, wherein the computer module is configured to operate only upon receiving power from the console.

66. (Previously Presented) The computer module of claim 63, wherein the serial communication controller comprises an Ethernet controller to communicate with an external network through the console.

67. (Previously Presented) A console to couple to a plurality of computer modules to form a server system, comprising:

a first coupling site to couple to a first computer module;

a second coupling site to couple to a second computer module;

a power supply coupled to at least one of the first coupling site and the second coupling site;

a printed circuit board;

a first low voltage differential signal (LVDS) channel coupled to the printed circuit board and comprising two sets of unidirectional, multiple serial bit channels in opposite directions;

a second LVDS channel coupled to the printed circuit board and comprising two sets of unidirectional, multiple serial bit channels in opposite directions; and

an enclosure housing the first coupling site, the second coupling site, the power supply, the first LVDS channel, the second LVDS channel, and the printed circuit board.

68. (Previously Presented) The console of claim 67, further comprising a first interface controller coupled to at least one of the first LVDS channel and the second LVDS channel to communicate an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction.

69. (Previously Presented) The console of claim 68, wherein at least one of the first computer module and the second computer module comprises a second interface controller, and the first interface controller is configured to couple to the second interface controller.

70. (Previously Presented) The console of claim 67, wherein the power supply is configured to provide power to each of the first computer module and the second computer module for operation.

71. (Previously Presented) The console of claim 67, further comprising a hard disk drive configured to couple to at least one of the first computer module and the second computer module.

72. (Previously Presented) The console of claim 67, further comprising an Ethernet hub controller configured to couple to at least one of the first computer module and the second computer module for communication with an external network.

73. (Previously Presented) A console to couple to a plurality of computer modules to form a server system, comprising:

a first coupling site to couple to a first computer module;

a second coupling site to couple to a second computer module;

a power supply;

a printed circuit board coupled to the first coupling site and the second coupling site;

a serial communication hub controller coupled to the printed circuit board;

a low voltage differential signal (LVDS) channel associated with at least one of the first coupling site and the second coupling site, the LVDS channel comprising two sets of

unidirectional, multiple serial bit channels in opposite directions for communicating an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction; and

an enclosure housing the first coupling site, the second coupling site, the power supply, the printed circuit board, the serial communication hub controller, and the LVDS channel.

74. (Previously Presented) The console of claim 73, wherein each of the first coupling site and the second coupling site comprises a slot and a connector.

75. (Previously Presented) The console of claim 73, further comprising an interface controller housed in the enclosure and coupled to the LVDS channel to communicate the encoded serial bit stream of PCI bus transaction.

76. (Previously Presented) The console of claim 73, further comprising an integrated display device.

77. (Previously Presented) The console of claim 73, wherein the serial communication hub controller comprises a multi-port, serial communication hub controller to support communication between the first computer module and the second computer module and with an external network.

78. (Previously Presented) The console of claim 73, further comprising a storage subsystem housed in the enclosure and shared by the first computer module and the second computer module.

79. (Previously Presented) The console of claim 73, wherein the power supply is configured to provide power to each of the first computer module and the second computer module for operation.

80. (Currently Amended) A server comprising:

a processing unit;

a main memory coupled to the processing unit;

a mass storage device coupled to the processing unit;

a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels to transmit data in opposite directions for communicating an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction; and

a peripheral bridge directly coupled to the processing unit, the peripheral bridge comprising an interface controller directly coupled to the LVDS channel;

wherein the processing unit is configured to couple to an external network through the LVDS channel.

81. (Previously Presented) The server of claim 80, further comprising an Ethernet controller coupled to the LVDS channel.

82. (Previously Presented) A server comprising:

a processing unit;

a main memory coupled to the processing unit;

a SCSI hard disk drive coupled to the processing unit;

a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels to transmit data in opposite directions for communicating an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction; and

an interface controller coupled to the LVDS channel;

wherein the processing unit is coupled to the interface controller for data communication with an external Ethernet network.

83. (Previously Presented) The server of claim 82, further comprising an Ethernet controller coupled to the LVDS channel.

84. (New) The computer system of claim 1, wherein the encoded serial bit stream of PCI bus transaction comprises encoded PCI address and data bits.

85. (New) The computer system of claim 5, wherein the encoded serial bit stream of PCI bus transaction comprises encoded PCI address and data bits.

86. (New) The computer system of claim 9, wherein the encoded PCI bus transaction data comprises encoded PCI address and data bits.

87. (New) The computer system of claim 13, wherein the encoded serial bit stream of PCI bus transaction comprises encoded PCI address and data bits.

88. (New) The computer system of claim 16, wherein the encoded PCI bus transaction data comprises encoded PCI address and data bits.

89. (New) The computer system of claim 28, wherein the encoded PCI bus transaction data comprises encoded PCI address and data bits.

90. (New) The computer system of claim 31, wherein the encoded PCI bus transaction data comprises encoded PCI address and data bits.

91. (New) The computer system of claim 34, wherein the encoded serial bit stream of PCI bus transaction comprises encoded PCI address and data bits.

92. (New) The computer system of claim 37, wherein the encoded serial bit stream of PCI bus transaction comprises encoded PCI address and data bits.

93. (New) The computer system of claim 40, wherein the encoded serial bit stream of PCI bus transaction comprises encoded PCI address and data bits.

94. (New) The computer module of claim 44, wherein the peripheral bridge corresponds to a north bridge.

95. (New) The computer module of claim 44, wherein the encoded serial bit stream of PCI bus transaction comprises encoded PCI address and data bits.

96. (New) The computer module of claim 53, wherein the encoded serial bit stream of PCI bus transaction comprises encoded PCI address and data bits.

97. (New) The computer module of claim 59, wherein the encoded serial bit stream of PCI bus transaction comprises encoded PCI address and data bits.

98. (New) The computer module of claim 63, wherein the encoded serial bit stream of PCI bus transaction comprises encoded PCI address and data bits.

99. (New) The console of claim 68, wherein the encoded serial bit stream of PCI bus transaction comprises encoded PCI address and data bits.

100. (New) The console of claim 73, wherein the encoded serial bit stream of PCI bus transaction comprises encoded PCI address and data bits.

101. (New) The server of claim 80, wherein the peripheral bridge corresponds to a north bridge.

102. (New) The server of claim 80, wherein the encoded serial bit stream of PCI bus transaction comprises encoded PCI address and data bits.

103. (New) The server of claim 82, wherein the encoded serial bit stream of PCI bus transaction comprises encoded PCI address and data bits.

REMARKS

Claims 1-83 were pending in the subject application. Claims 44 and 80 are amended to further specify "a peripheral bridge directly coupled to the processing unit, the peripheral bridge comprising" an interface controller "directly" coupled to a LVDS channel. New dependent claims 84-103 are added. Support for the amendments can be found, for example, at Figure 8 and paragraphs [0093] and [0119]-[0124]. No new matter has been added.

Entry of the foregoing amendments is respectfully requested.

Date: March 10, 2011

Respectfully submitted,
COOLEY LLP

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PTO/SB/08a (01-10)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	12504534
Filing Date	2009-07-16
First Named Inventor	William W.Y. Chu
Art Unit	2111
Examiner Name	Phan, Raymond Ngan
Attorney Docket Number	ACQI-010/10US 310578-2052

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	12504534
	Filing Date	2009-07-16
	First Named Inventor	William W.Y. Chu
	Art Unit	2111
	Examiner Name	Phan, Raymond Ngan
	Attorney Docket Number	ACQI-010/10US 310578-2052

	1	"Memorandum Opinion and Order Construing Claim Terms," Issued by the U.S. District Court for the Eastern District of Texas, Tyler Division, Case No. 6:09-cv-148-LED, Document 602, Feb. 3, 2011, 12 pgs.	☐

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Examiner Signature		Date Considered	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	12504534
	Filing Date	2009-07-16
	First Named Inventor	William W.Y. Chu
	Art Unit	2111
	Examiner Name	Phan, Raymond Ngan
	Attorney Docket Number	ACQI-010/10US 310578-2052

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

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☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☒ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Cliff Z. Liu/	Date (YYYY-MM-DD)	2011-03-10
Name/Print	Cliff Z. Liu	Registration Number	50834

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Electronic Patent Application Fee Transmittal

Application Number:	12504534
Filing Date:	16-Jul-2009
Title of Invention:	MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNDIRECTIONAL SERIAL BIT CHANNELS
First Named Inventor/Applicant Name:	William W. Y. Chu
Filer:	Cliff Z. Liu/Bobbie Jutras
Attorney Docket Number:	ACQI-010/10US 310578-2052

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Claims in excess of 20	1202	20	52	1040
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
		Total in USD ($)		**1220**

Electronic Acknowledgement Receipt

EFS ID:	9636375
Application Number:	12504534
International Application Number:	
Confirmation Number:	1286
Title of Invention:	MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNDIRECTIONAL SERIAL BIT CHANNELS
First Named Inventor/Applicant Name:	William W. Y. Chu
Customer Number:	58249
Filer:	Cliff Z. Liu/Bobbie Jutras
Filer Authorized By:	Cliff Z. Liu
Attorney Docket Number:	ACQI-010/10US 310578-2052
Receipt Date:	10-MAR-2011
Filing Date:	16-JUL-2009
Time Stamp:	20:59:27
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$1220
RAM confirmation Number	8385
Deposit Account	501283
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The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		ACQI-010-10US_03-10-11_Amendment.pdf	369848 fa097022f173b58c03ad0855d3fdae6547e549b4	yes	22

Multipart Description/PDF files in .zip description

Document Description	Start	End
Amendment/Req. Reconsideration-After Non-Final Reject	1	1
Claims	2	21
Applicant Arguments/Remarks Made in an Amendment	22	22

Warnings:

Information:

2	Information Disclosure Statement (IDS) Filed (SB/08)	ACQI-010-10US_03-10-11_IDS.pdf	612270 9d22f39dec4c20c93d880a78e12eaf2116764854	no	4

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3	NPL Documents	OpinionandOrderConstruingClaims-Feb_3_2011.pdf	2728434 8d8de522d1041d81cd3da51e9120a2b3a0f6bcd2	no	12

Warnings:

Information:

4	Fee Worksheet (PTO-875)	fee-info.pdf	32426 5a1a2b1f10b6d08b18913ddbac66103138a81f50	no	2

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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
12/504,534	07/16/2009	

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY ☒ RATE ($)	SMALL ENTITY ☒ FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT 03/10/2011	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 103	Minus	** 83	= 20	X $26 =	520	OR	X $ =	
Independent (37 CFR 1.16(h))	* 21	Minus	***21	= 0	X $110 =	0	OR	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE	520	OR	TOTAL ADD'L FEE	

AMENDMENT 03/10/2011	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)	OR	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 103	Minus	** 123	= 0	X $26 =	0	OR	X $ =	
Independent (37 CFR 1.16(h))	* 21	Minus	*** 21	= 0	X $110 =	0	OR	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE	0	OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/CAROLYN THOMAS/

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Application Number	Application/Control No.	Applicant(s)/Patent under Reexamination	
	12/504,534	CHU, WILLIAM W. Y.	

Document Code - DISQ	Internal Document – DO NOT MAIL

TERMINAL DISCLAIMER	☒ APPROVED	☐ DISAPPROVED
Date Filed : 01-28-11	This patent is subject to a Terminal Disclaimer	

Approved/Disapproved by:
KAREN L. WARD (2 TDs)

U.S. Patent and Trademark Office

PTO/SB/08a (01-10)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	12504534
Filing Date	2009-07-16
First Named Inventor	William W.Y. Chu
Art Unit	2111
Examiner Name	Phan , Raymond Ngan
Attorney Docket Number	ACQI-010/10US 310578-2052

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	6161157		2000-12-12	Tripathi	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	12504534
	Filing Date	2009-07-16
	First Named Inventor	William W.Y. Chu
	Art Unit	2111
	Examiner Name	Phan , Raymond Ngan
	Attorney Docket Number	ACQI-010/10US 310578-2052

	1	CHU, Inter Partes Reexam of USP 6,718,415, Reexam Control No. 95/001,276, "Final Judgement", issued by the US District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2011, 1 pg.	☐
	2	CHU, Inter Partes Reexam of USP 6,718,415, Reexam Control No. 95/001,276, "Jury Verdict Form", Executed by Jury in the US District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on February 23, 2011, 2 pgs.	☐
	3	CHU, Inter Partes Reexam of USP 6,718,415, Reexam Control No. 95/001,276, "Supplemental Comments by Third Party Requestor Pursuant to 37 CFR 1.947", 05/12/11, 45 pgs.	☐
	4	CHU, Inter Partes Reexam of USP 6,718,415, Reexam Control No. 95/001,276, "Supplemental Comments by Third Party Requestor Pursuant to 37 CFR 1.947, Exhibit AA-2: Claim Charts with Respect to QuantumNet", 05/12/11, 120 pgs.	☐
	5	CHU, Inter Partes Reexam of USP 6,718,415, Reexam Control No. 95/001,276, "Supplemental Comments by Third Party Requestor Pursuant to 37 CFR 1.94, 7Exhibit BB-2: Claim Charts with Respect to Chatcom", 05/12/11, 94 pgs.	☐
	6	CHU, Inter Partes Reexam of USP 6,718,415, Reexam Control No. 95/001,276, "Supplemental Comments by Third Party Requestor Pursuant to 37 CFR 1.947, Exhibit CC-2: Claim Charts with Respect to Eversys", 05/12/11, 165 pgs.	☐
	7	CHU, Inter Partes Reexam of USP 6,718,415, Reexam Control No. 95/001,276, "Supplemental Comments by Third Party Requestor Pursuant to 37 CFR 1.947, Exhibit DD-2: Claim Charts with Respect to Origin2000 Manual", 05/12/11, 108 pgs.	☐
	8	CHU, Inter Partes Reexam of USP 6,718,415, Reexam Control No. 95/001,276, "Supplemental Comments by Third Party Requestor Pursuant to 37 CFR 1.947, Exhibit EE-2: Claim Charts with Respect to Gallagher", 05/12/11, 91 pgs.	☐
	9	KUNZMAN et al., "1394 High Performance Serial Bus: The Digital Interface for ATV", IEEE Transactions on Consumer Electronics, Vol. 41, No. 3, 3 Aug 1995, pp. 893-900	☐
	10	PARKES, SM, "High-Speed, Low-Power, Excellent EMC: LVDS For On-Board Data Handling," Proceedings of 6th International Workshop on Digital Signal Processing Techniques for Space Applications, IEEE (1998), Sep. 1998, pp. 16 ("Parkes 1355") [includes a reference page establishing date of publication retrieved from <http://spacetech.dundee.ac.uklresearch/spacecraft-onboard-data-handling/publications/high-speed-low-power-excellent-emc-lvds-board>	☐

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	12504534
	Filing Date	2009-07-16
	First Named Inventor	William W.Y. Chu
	Art Unit	2111
	Examiner Name	Phan , Raymond Ngan
	Attorney Docket Number	ACQI-010/10US 310578-2052

EXAMINER SIGNATURE			
Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	12504534
	Filing Date	2009-07-16
	First Named Inventor	William W.Y. Chu
	Art Unit	2111
	Examiner Name	Phan , Raymond Ngan
	Attorney Docket Number	ACQI-010/10US 310578-2052

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☒ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Cliff Z. Liu/	Date (YYYY-MM-DD)	2011-05-17
Name/Print	Cliff Z. Liu	Registration Number	50834

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

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Electronic Patent Application Fee Transmittal

Application Number:	12504534
Filing Date:	16-Jul-2009
Title of Invention:	MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNDIRECTIONAL SERIAL BIT CHANNELS
First Named Inventor/Applicant Name:	William W. Y. Chu
Filer:	Cliff Z. Liu/Bobbie Jutras
Attorney Docket Number:	ACQI-010/10US 310578-2052

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
		Total in USD ($)		**180**

Electronic Acknowledgement Receipt

EFS ID:	10113074
Application Number:	12504534
International Application Number:	
Confirmation Number:	1286
Title of Invention:	MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNDIRECTIONAL SERIAL BIT CHANNELS
First Named Inventor/Applicant Name:	William W. Y. Chu
Customer Number:	58249
Filer:	Cliff Z. Liu/Bobbie Jutras
Filer Authorized By:	Cliff Z. Liu
Attorney Docket Number:	ACQI-010/10US 310578-2052
Receipt Date:	17-MAY-2011
Filing Date:	16-JUL-2009
Time Stamp:	20:40:10
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$180
RAM confirmation Number	6032
Deposit Account	501283
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Filed (SB/08)	ACQI-010-10US_05-17-11_IDS.pdf	613282 7d077203cd4a7faaa6547d79a9348edd891c9064	no	5
Warnings:					
Information:					
2	NPL Documents	ACQI01011_03-01-11-Final_Judgment.pdf	648154 7b1f8c7af399582fcea49ec433cfc061a4503314	no	1
Warnings:					
Information:					
3	NPL Documents	ACQI01011_02-23-11-Jury_Verdict_Form.pdf	1022391 000e0d2c34ce0596734147acd26ce1c8816db793	no	2
Warnings:					
Information:					
4	NPL Documents	ACQI01011_05-12-11-Suppl_Comm_by_3rdPty_Requestor.pdf	2446798 2c856be52cce49bf54d0804de6e0b5dfac0f3e47	no	45
Warnings:					
Information:					
5	NPL Documents	ACQI01011_05-12-11-Claim_Charts_with_Respect_to_QuantumNet.pdf	8721319 1cfcb057b00c3aecd37a1917d4bebdcce0818c48	no	120
Warnings:					
Information:					
6	NPL Documents	ACQI01011_05-12-11-Claim_Charts_with_Respect_to_Chatcom.pdf	6527741 dcba8f822267dde63c3a92c106db1b71fa9d3508	no	94
Warnings:					
Information:					
7	NPL Documents	ACQI01011_05-12-11-Claim_Charts_with_Respect_to_Eversys.pdf	8129622 450e45d50d3b065767ae39778220194e09aebe7c	no	165
Warnings:					
Information:					
8	NPL Documents	ACQI01011_05-12-11-Claim_Charts_with_Respect_to_Origin_2000_Manual.pdf	7497132 66166c7e5b9e2a243919105c323d3dc14902d2b1	no	108
Warnings:					
Information:					

9	NPL Documents	ACQI01011_05-12-11-Claim_Charts_with_Respect_to_Gallagher.pdf	6735510 6272b2d34f98ae96625acf3730c72f238eed9f95	no	91
Warnings:					
Information:					
10	NPL Documents	KUNZMAN-1394_High_Performance_Serial_Bus.pdf	503474 86bae017b05a0d615764342ce1689f36d6f675a4	no	8
Warnings:					
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11	NPL Documents	PARKES-High-Speed_Low-Power_Excellent_EMC.pdf	876170 a39ad171ccdd8fbab9e3d504a38f7b197611e22b	no	12
Warnings:					
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12	Fee Worksheet (PTO-875)	fee-info.pdf	30819 04e6465072d747c37de6ecf060f37168b6cf6d03	no	2
Warnings:					
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58249 7590 06/03/2011

COOLEY LLP
ATTN: Patent Group
Suite 1100
777 - 6th Street, NW
WASHINGTON, DC 20001

EXAMINER
PHAN, RAYMOND NGAN

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 06/03/2011

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/504,534	07/16/2009	William W. Y. Chu	ACQI-010/10US 310578-2052	1286

TITLE OF INVENTION: MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNDIRECTIONAL SERIAL BIT CHANNELS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	$755	$300	$0	$1055	09/06/2011

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

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I. Review the SMALL ENTITY status shown above.

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B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

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III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

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Alexandria, Virginia 22313-1450
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58249 7590 06/03/2011

COOLEY LLP
ATTN: Patent Group
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777 - 6th Street, NW
WASHINGTON, DC 20001

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(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/504,534	07/16/2009	William W. Y. Chu	ACQI-010/10US 310578-2052	1286

TITLE OF INVENTION: MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNDIRECTIONAL SERIAL BIT CHANNELS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	$755	$300	$0	$1055	09/06/2011

EXAMINER	ART UNIT	CLASS-SUBCLASS
PHAN, RAYMOND NGAN	2111	710-313000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

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(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

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❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

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❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/504,534	07/16/2009	William W. Y. Chu	ACQI-010/10US 310578-2052	1286

58249 7590 06/03/2011

COOLEY LLP
ATTN: Patent Group
Suite 1100
777 - 6th Street, NW
WASHINGTON, DC 20001

EXAMINER	
PHAN, RAYMOND NGAN	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 06/03/2011

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)

(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No.	Applicant(s)	
	12/504,534	CHU, WILLIAM W. Y.	
	Examiner	Art Unit	
	RAYMOND PHAN	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the Terminal Disclaimer filed on January 28, 2011*.

2. ☒ The allowed claim(s) is/are *1-103*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 121610/012811/031011/051711
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/RAYMOND N PHAN/
Primary Examiner, Art Unit 2111

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12504534	CHU, WILLIAM W. Y.
	Examiner	**Art Unit**
	RAYMOND PHAN	2111

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	10/22/2010	05/25/2011							
1	1	✓	=							
2	2	✓	=							
3	3	✓	=							
4	4	✓	=							
6	5	✓	=							
7	6	✓	=							
8	7	✓	=							
9	8	✓	=							
11	9	✓	=							
12	10	✓	=							
13	11	✓	=							
14	12	✓	=							
16	13	✓	=							
17	14	✓	=							
18	15	✓	=							
20	16	✓	=							
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22	18	✓	=							
23	19	=	=							
24	20	=	=							
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26	22	=	=							
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30	26	=	=							
31	27	=	=							
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34	29	✓	=							
36	30	✓	=							
37	31	✓	=							
38	32	✓	=							
39	33	✓	=							
41	34	=	=							
42	35	=	=							
43	36	=	=							

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
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	Examiner	**Art Unit**
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☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	10/22/2010	05/25/2011							
45	37	=	=							
46	38	=	=							
47	39	=	=							
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56	46	✓	=							
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80	66	✓	=							
81	67	=	=							
83	68	=	=							
84	69	=	=							
85	70	=	=							
86	71	=	=							
87	72	=	=							

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12504534	CHU, WILLIAM W. Y.
	Examiner	**Art Unit**
	RAYMOND PHAN	2111

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	10/22/2010	05/25/2011							
89	73	✓	=							
90	74	✓	=							
91	75	✓	=							
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93	77	✓	=							
94	78	✓	=							
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97	80	✓	=							
98	81	✓	=							
101	82	✓	=							
102	83	✓	=							
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10	85		=							
15	86		=							
19	87		=							
32	88		=							
36	89		=							
40	90		=							
44	91		=							
48	92		=							
53	93		=							
60	94		=							
61	95		=							
71	96		=							
76	97		=							
82	98		=							
88	99		=							
96	100		=							
99	101		=							
100	102		=							
103	103		=							

Issue Classification

Application/Control No.	Applicant(s)/Patent Under Reexamination
12504534	CHU, WILLIAM W. Y.
Examiner	**Art Unit**
RAYMOND PHAN	2111

ORIGINAL

CLASS	SUBCLASS
710	313

CROSS REFERENCE(S)

CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
710	301	315			
709	227				

INTERNATIONAL CLASSIFICATION

CLAIMED	NON-CLAIMED
G 0 6 F 13 / 20 (2006.01.01)	

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	21	17	39	33	57	49	79	65	98	81	76	97		
2	2	22	18	41	34	58	50	80	66	101	82	82	98		
3	3	23	19	42	35	59	51	81	67	102	83	88	99		
4	4	24	20	43	36	64	52	83	68	5	84	96	100		
6	5	25	21	45	37	65	53	84	69	10	85	99	101		
7	6	26	22	46	38	66	54	85	70	15	86	100	102		
8	7	27	23	47	39	67	55	86	71	19	87	103	103		
9	8	28	24	49	40	68	56	87	72	32	88				
11	9	29	25	50	41	69	57	89	73	36	89				
12	10	30	26	51	42	70	58	90	74	40	90				
13	11	31	27	52	43	72	59	91	75	44	91				
14	12	33	28	54	44	73	60	92	76	48	92				
16	13	34	29	55	45	74	61	93	77	53	93				
17	14	35	30	56	46	75	62	94	78	60	94				
18	15	37	31	62	47	77	63	95	79	61	95				
20	16	38	32	63	48	78	64	97	80	71	96				

NONE (Assistant Examiner) (Date)	**Total Claims Allowed:** 103
/RAYMOND PHAN/ Primary Examiner.Art Unit 2111 5/25/11 (Primary Examiner) (Date)	O.G. Print Claim(s): 1 O.G. Print Figure: 9

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12504534	CHU, WILLIAM W. Y.
	Examiner	Art Unit
	RAYMOND N PHAN	2111

SEARCHED

Class	Subclass	Date	Examiner
710	300-317,62-64,72-74	10/21/10	RP
709	214-219,226-227	10/21/10	RP
714	43-44, 11, 13	10/21/10	RP
710	300-317,62-64,72-74	5/20/11	RP
709	214-219,226-227	5/20/11	RP
714	43-44,11,13	5/20/11	RP

SEARCH NOTES

Search Notes	Date	Examiner
EAST Search	10/22/10	RP

INTERFERENCE SEARCH

Class	Subclass	Date	Examiner
710	313,301,315	5/25/11	RP
709	227	5/25/11	RP

	/RAYMOND PHAN/ Primary Examiner.Art Unit 2111

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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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OPAP IAP4 JAN 28 2011 PATENT & TRADEMARK OFFICE

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 26

Complete if Known	
Application Number	12/504,534
Filing Date	July 16, 2009
First Named Inventor	William W.Y. Chu
Art Unit	2111
Examiner Name	Phan, Raymond Ngan
Attorney Docket Number	ACQI-010/10US 310578-2052

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	A105	4,141,068	02-20-1979	Mager et al.	
	A104	4,670,837	06-02-1987	Sheets	
	AU002	4,799,258	01-17-1989	Davies	
	AO003	5,103,446	04-07-1992	Fischer	
	AO004	5,191,581	03-02-1993	Woodbury et al.	
	AK002	5,293,487	03-08-1994	Russo et al.	
		5,293,497	03-08-1994	Free	
	AO005	5,519,843	05-21-1996	Moran et al.	
	AU003	5,546,463	08-13-1996	Caputo et al.	
	AO006	5,572,441	11-05-1996	Boie	
	AR001	5,590,377	12-31-1996	Smith	
	AP002	5,623,637	04-22-1997	Jones et al.	
	AO007	5,648,762	07-15-1997	Ichimura et al.	
	A107	5,737,524	04-07-1998	Cohen et al.	
	AO008	5,751,711	05-12-1998	Sakaue	
	AO009	5,838,932	11-17-1998	Alzien	
	A103	5,862,350	01-19-1999	Coulson	
	AO002	5,862,381	01-19-1999	Advani et al.	
	AW001	5,878,211	03-02-1999	Delagrange et al.	
	AR002	5,884,049	03-16-1999	Atkinson	
	AM002	5,930,110	07-27-1999	Nishigaki et al.	
	AO010	5,933,609	08-03-1999	Walker et al.	
	A102	5,965,957	10-12-1999	Bourgeois	
	AR003	5,974,486	10-26-1999	Siddappa	
	AO011	6,006,243	12-21-1999	Karidis	
	AO012	6,012,145	01-04-2000	Mathers et al.	
	AO013	6,046,571	04-04-2000	Bovio et al.	

Examiner Signature	/Raymond Phan/	Date Considered	05/09/2011

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1]Applicant's unique citation designation number (optional). [2]See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3]Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6]Applicant is to place a check mark here if English language Translation is attached.

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American LegalNet, Inc. www.FormsWorkFlow.com

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /R.P./

PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 2 of 26

Complete if Known	
Application Number	12/504,534
Filing Date	July 16, 2009
First Named Inventor	William W.Y. Chu
Art Unit	2111
Examiner Name	Phan, Raymond Ngan
Attorney Docket Number	ACQI-010/10US 310578-2052

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Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	AM001	6,088,620	07-11-2000	Ninomiya et al.	
	AO014	6,104,921	08-15-2000	Cosley et al.	
	AO015	6,256,689	07-03-2001	Khosrowpour	
	AO016	6,266,539	07-24-2001	Pardo	
	AR004	6,301,637	10-09-2001	Krull et al.	
	AC038	6,498,361 B1	12-24-2002	Osann, Jr.	
	A094	6,578,103 B1	06-10-2003	Hill et al.	
	A106	6,606,253 B2	08-12-2003	Jackson et al.	
	A096	6,664,377 B1	12-16-2003	Xu	
	A012	6,757,748 B1	06-29-2004	Hipp	
	AH001	7,676,624 B2	03-09-2010	Chu	
	AI001	7,818,487 B2	10-19-2010	Chu	
	AQ001	RE41,076 E	01-12-2010	Chu	
	AU001	RE41,092	01-26-2010	Chu	
	AP001	RE41,294 E	04-27-2010	Chu	
	AO001	RE41,961	11-23-2010	Chu	
		2001/0011312 A1	08-02-2001	Chu	
	AG002	2005/0182882 A1	08-18-2005	Chu	
	AJ001	2010/0174844 A1	07-08-2010	Chu	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] "Number[4] "Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	B004	JP 6-289953	10-18-1994	Hitachi, Ltd.		
	BN001	WO 97/00481	01-03-1997	Intel Corporation		

Examiner Signature	/Raymond Phan/	Date Considered	05/09/2011

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1]Applicant's unique citation designation number (optional). [2]See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3]Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6]Applicant is to place a check mark here if English language Translation is attached.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 3 of 26

Complete if Known	
Application Number	12/504,534
Filing Date	July 16, 2009
First Named Inventor	William W.Y. Chu
Art Unit	2111
Examiner Name	Phan, Raymond Ngan
Attorney Docket Number	ACQI-010/10US 310578-2052

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	C004	QuantumNet, Inc., QuantumNet Product Overview [online], 1996 [retrieved on November 16, 2009], Retrieved from the Internet: <URL: http://web.archive.org/web/19971011194003/www.quantumnet.com/products.htm>, 1 page.	
	C005	QuantumNet, Inc., QuantumNet: The Next Generation Computing and Networking Environment [online], 1996 [retrieved on November 16, 2009], Retrieved from the Internet: <URL: http://web.archive.org/web/19971011194123/www.quantumnet.com/qnetovw.htm>, 7 pages.	
	C006	QuantumNet, Inc., QuantumNet 6500 Processor Modules [online], 1996 [retrieved on November 16, 2009], Retrieved from the Internet: <URL:http://web.archive.org/web/19971011194317/www.quantumnet.com/ds6500.htm>, 4 pages.	
	C007	QuantumNet, Inc., QuantumServer Chassis [online], 1996 [retrieved on November 16, 2009], Retrieved from the Internet: <URL: http://web.archive.org/web/19971011194309/www.quantumnet.com/dsq6000.htm>, 3 pages.	
	C009	Cubix Corporation, Datasheet: Single-Board Computers with Pentium Processors [online], 1997 [retrieved on July 31, 2009], Retrieved from the Internet: <URL: http://web.archive.org/web/19970716204717/www.cubix.com/corporate/data/bcp5t.htm>, 5 pages.	
	C010	Cubix Corporation, Datasheet: ERS/FT II Server Chassis [online], 1997 [retrieved on July 31, 2009], Retrieved from the Internet: <URL: http://web.archive.org/web/19970716204623/www.cubix.com/corporate/data/ersft2.htm>, 3 pages.	
	C011	Cubix Corporation, Cubix ERS/FT II Systems [online], 1997 [retrieved on July 31, 2009], Retrieved from the Internet: <URL: http://web.archive.org/web/19980124213320/www.cubix.com/support/steps/ers-ft2/intro.htm>, 5 pages.	
	C012	Cubix Corporation, Cubix Product Catalog, Summer 1995, 56 pages.	
	C013	Cubix Corporation, BC Series, Processor Boards Installation Guide, DOC 800A, August 1994, 149 pages.	
	C014	Cubix Corporation, ERS/FT II - Enhanced Resource Subsystem/Fault Tolerant II, November 1994, 4 pages.	

Examiner Signature	/Raymond Phan/	Date Considered	05/09/2011

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Sheet 4 of 26

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Application Number	12/504,534
Filing Date	July 16, 2009
First Named Inventor	William W.Y. Chu
Art Unit	2111
Examiner Name	Phan, Raymond Ngan
Attorney Docket Number	ACQI-010/10US 310578-2052

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	C015	Cubix Corporation, Density Series Plug-In Servers, Plug-In Computers for Managed Server Farms, September 15, 1998, 2 pages.	
	C016	Cubix Corporation, Cubix Pentium II Plug-In Computers for Density Series Systems, September 15, 1998, 1 page.	
	C017	Cubix Corporation, Density Series Multi-Server Systems, September 10, 1999, 4 pages.	
	C018	Compaq Computer Corporation, White Paper, "Order and Configuration Guide for Compaq ProLiant Cluster Series F Model 100," September 1998, pages 1-8.	
	C019	Compaq Computer Corporation, QuickSpecs, Compaq ProLiant Cluster Series F Model 100, (undated), pages 8-36 to 8-37.	
	C020	Compaq Computer Corporation, Compaq Performance Brief, ProLiant 1600 ServerBench Performance Summary, August 1998, pages 1-7.	
	C021	Compaq Computer Corporation, Compaq ActiveAnswers Installation Guide, Installation and Configuration Guide for Linux and Apache Web Server on Compaq Prosignia and ProLiant Servers, May 1999, pages 1-40.	
	C022	Compaq Computer Corporation, Compaq White Paper, "Microsoft Internet Information Server 4.0 on the Compaq ProLiant 6500," August 1998, pages 1-14.	
	C023	Compaq Computer Corporation, Compaq White Paper, "Accelerating Financial Spreadsheet Simulations with Workstation Clusters," October 1998, pages 1-14.	
	C024	Compaq Computer Corporation, ProLiant 6500-PDC/O1000 C/S with 4 ProLiant 1850R, TPC-C Rev. 3.4, Report Date: Dec. 22, 1998, pages 1-3.	
	C026	Compaq Computer Corporation, Compaq White Paper, "ServerNet - A High Bandwith, Low Latency Cluster Interconnection," September 1998, pages 1-9.	
	C027	JL ChatCom, Inc. - Web Site, JL ChatCom, Inc., ChatterBox Communications and Server Solutions [online], 1996 [retrieved on December 2, 2009], Retrieved from the Internet: <URL: http://web.archive.org/web/19970104221841/http://www.jlchatcom.com/>, 1 page.	
	C028	JL ChatCom, Inc. - Scaleable Application and Communication Servers, "ChatCom, Inc. Announces Complete Line of Scaleable Application and Communication Servers," August 30, 1996 [retrieved on December 2, 2009], JL ChatCom, Inc., ChatterBox Communications and Server Solutions [online], Retrieved from the Internet: <URL: http://web.archive.org/web/19970104221932/www.jlchatcom.com/cpofrel.htm>, 4 pages.	

Examiner Signature	/Raymond Phan/	Date Considered	05/09/2011

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Sheet 5 of 26

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Application Number	12/504,534
Filing Date	July 16, 2009
First Named Inventor	William W.Y. Chu
Art Unit	2111
Examiner Name	Phan, Raymond Ngan
Attorney Docket Number	ACQI-010/10US 310578-2052

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	C029	JL ChatCom, Inc. - Highly Adaptable Intranet and Web Servers, "ChatCom, Inc. Announces Highly Adaptable Intranet and Web Servers," September 3, 1996 [retrieved on December 2, 2009], JL ChatCom, Inc., ChatterBox Communications and Server Solutions [online], Retrieved from the Internet: <URL: http://web.archive.org/web/19970104221941/www.jlchatcom.com/chat4int.htm>, 2 pages.	
	C030	JL ChatCom, Inc., "ChatPower Plus," 1996 [retrieved on December 2, 2009], JL ChatCom, Inc., ChatterBox Communications and Server Solutions [online], Retrieved from the Internet: <URL: http://web.archive.org/web/19970104222122/www.jlchatcom.com/chatplus.htm>, 3 pages.	
	C031	JL ChatCom, Inc., "ChatterBox ChatPower Plus," (undated) [retrieved on December 2, 2009], JL ChatCom, Inc., ChatterBox Communications and Server Solutions [online], Retrieved from the Internet: <URL: http://web.archive.org/web/19970104222556/www.jlchatcom.com/cpp1.gif>, 1 page.	
	C032	JL ChatCom, Inc., "ChatExpress PB5 Series P166 Pentium PCI/ISA CPU Card," 1996 [retrieved on December 2, 2009], JL ChatCom, Inc., ChatterBox Communications and Server Solutions [online], Retrieved from the Internet: <URL: http://web.archive.org/web/19970104222157/www.jlchatcom.com/chatp599.htm>, 2 pages.	
	C033	JL ChatCom, Inc., "ChatExpress - 2 Slot," [retrieved on December 2, 2009], JL ChatCom, Inc., ChatterBox Communications and Server Solutions [online], Retrieved from the Internet: <URL: http://web.archive.org/web/19970104222644/www.jlchatcom.com/exp2ill.gif>, 1 page.	
	C034	Ziatech Corporation, Ketris 9000, August 1, 2000, 4 pages.	
	C035	Ziatech Corporation, Ketris 9000 System Hardware Manual, 2000, 46 pages.	
	C036	Ziatech Corporation, Ketris Server Blade Hardware Manual, 2000, pages 1-60.	
	C037	Ziatech Corporation, Ketris Media Blade Hardware Manual, 2000, pages 1-17.	
	C038	Ziatech Corporation, Ketris Manager Software Manual, 2000, pages 1-28.	
	C039	Ziatech Corporation, Ketris System Management Overview, June 22, 2000, 4 pages.	
	C041	Ziatech Corporation, STD 32 Star System Multiprocessing Computer System, 1998, 6 pages.	
	C042	Ziatech Corporation, ZT 8907 Single Board Computer with IntelDX4 Microprocessor, 1998, 4 pages.	
	C043	Ziatech Corporation, ZT 8908 Single Board Computer with Pentium Processor or AMD-K6, 1998, 6 pages.	

Examiner Signature	/Raymond Phan/	Date Considered	05/09/2011

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Sheet 6 of 26

Complete if Known	
Application Number	12/504,534
Filing Date	July 16, 2009
First Named Inventor	William W.Y. Chu
Art Unit	2111
Examiner Name	Phan, Raymond Ngan
Attorney Docket Number	ACQI-010/10US 310578-2052

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	C044	Ziatech Corporation, System Designer's Guide, Expanding STD Bus Performance Through Multiprocessing, April 1996, 6 pages.	
	C045	Ziatech Corporation, System Designer's Guide, Hot Swap Capability on STD 32 Computers, January 1996, 6 pages.	
	C046	Ziatech Corporation, STD 32 zVID2 Local Bus Super VGA/FPD Adapter, April 1996, 2 pages.	
	C047	Wolfpack or Microsoft Cluster Services on STAR System, (undated), 3 pages.	
	C048	Ziatech Corporation, Ziatech Industrial BIOS for CompactPCI and STD 32 Systems, Software Manual for Industrial BIOS Version 4.7, July 27, 1998, 134 pages.	
	C049	Ziatech Corporation, "New STD 32 Fault Tolerant Computer Provides Modular Platform for 'Non-Stop' Applications," February 5, 1996, 2 pages.	
	C052	Eversys Corporation, System 8000 Consolidated Network Server Product Brief, (undated), 2 pages.	
	C053	Eversys Corporation, System 8000 Consolidated Server, (undated), [retrieved on November 9, 2009], Retrieved from C: drive <path: file://C:\Documents and Settings\Daniel\M Documents\Eversys\Eversys Web Site Master...>, 6 pages.	
	C054	Eversys Corporation, System 8000 Consolidated Server Presentation, (undated), 23 pages.	
	C055	Eversys Corporation, System 8000 Consolidated Network Server, Pentium II Processor Module User's Guide for Module version P2D-BXT, January 1998, 49 pages.	
	C056	Eversys Corporation, EVERSYS System 8000 Peripheral Sharing Switch (PSS) User's Guide, 1st Edition-June 1997, 2nd Edition-January 1998, 17 pages.	
	C057	Eversys Corporation, WebView 8000 version 1.1 User's Guide, Web-Based Management Software fo the EVERSYS System 8000 Consolidated Server, Revision A-November 1998, Revision B-December 1998, 56 pages.	
	C058	Eversys Corporation, S8000 Single Module Body Assemby, October 9, 1998, 9 pages.	
	C059	Eversys CAPserver Product Brief [online], (undated), [retrieved on November 16, 2009], Retrieved from the Internet: <URL: http://web.archive.org/web/19961104093115/www.eversys.com/CAPbrief.htm>, 10 pages.	
	C060	Eversys CAPcard 9500/sa Product Brief [online], (undated), [retrieved on November 16, 2009], Retrieved from the Internet: <URL: http://web.archive.org/web/19961104093144/www.eversys.com/cc95sa_Brief.htm>, 3 pages.	

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Filing Date	July 16, 2009
First Named Inventor	William W.Y. Chu
Art Unit	2111
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	C062	PHILLIPS, J., "9800 Disk Card Design Specification," May 26, 1998, White Cross Systems Limited, pages 1-44.	
	C063	PHILLIPS, J., "9800 Disk Card Layout Specification," April 6, 1998, White Cross Systems Limited, pages 1-22.	
	C064	FEAKES, L., "Disk Connector Card Functional Requirement Specification," January 14, 1998, White Cross Systems Limited, pages 1-4.	
	C065	FEAKES, L., "Disk Connector Card Layout Specification," January 14, 1998, White Cross Systems Limited, pages 1-6.	
	C066	White Cross Systems Limited, WhiteCross Data Exploration Configuration and Maintenance Manual, July 2000, 354 pages.	
	C067	White Cross Systems Limited, WhiteCross Data Exploration, White Paper: R&D 99Q3-01, "WXDES-Technical Information," September 3, 1999, pages 1-38.	
	C068	White Cross Systems Limited, WhiteCross Configuration & Maintenance Manual, November 2002, Version 5.2, 305 pages.	
	C069	BURROW, M., WhiteCross Data Exploration, "A Technical Overview of the WXDES/9800," March 2, 1999, Revision 2.00, White Cross Systems Limited, pages 1-90.	
	C070	White Cross Systems Limited, WhiteCross WX/DES Hardware Maintenance, 2000, pages 1-72.	
	C073	KHAN, M. F., "Ethernet Switch Card Design Specification," March 8, 2001, White Cross Systems Limited, pages 1-32.	
	C074	KHAN, M. F., "Ethernet Switch Card Layout Specifications," March 8, 2001, pages 1-31.	
	C075	SMITH, B., Processor Backplane Functional Requirement Specification, July 31, 1997, White Cross Systems Limited, pages 1- 11.	
	C076	SMITH, B., "Processor Backplane Design Specification," February 3, 1998, White Cross Systems Limited, pages 1-16.	
	C077	SMITH, B., "Processor Backplane Layout Specification," November 12, 1997, White Cross Systems Limited, pages 1-7.	
	C078	PHILLIPS, J., "9800 Processor Card Design Specification," February 25, 1998, White Cross Systems Limited, pages 1-41.	
	C079	PHILLIPS, J., "9800 Processor Card Layout Specification," September 29, 1997, White Cross Systems Limited, pages 1-13.	

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	C080	MIASTKOWSKI, S. (Editor), "A Whale of a System," BYTE, August 1991, 4 pages, Vol. 16, No. 8.	
	C081	Advanced Micro Devices, Inc., "AMD-K6-III Processor Data Sheet," 21918B/0, October 1999, 326 pages.	
	C084	Digital Equipment Corporation, "DIGITAL AlphaServer 4000 and 4100 systems," [Brochure], 1998, 4 pages.	
	C089	EVERSYS, "CAPserver Product Brief" [online], [retrieved on 11-16-2009], Retrieved from the Internet: <URL: http://web.archieve.org/web/19961104093115/www.eversys.com/CAPbrief.htm>, 10 pages.	
	C090	EVERSYS, "CAPcard 9500/sa Product Brief," [online], [retrieved on 11-16-2009], Retrieved from the Internet: <URL: http://web.archieve.org/web/19961104093144/www.eversys.com/cc95sa_Brief.htm>, 3 pages.	
	C100	ELLIS, S., "IRIS FailSafe™ Administrator's Guide," Document Number 007-3109-003, April 6, 1997, 212 pages.	
	C101	Microsoft Cluster Service Center, "MSCS Basics," [online], [retrieved on 02-07-2005]. Retrieved from the Internet at <URL: http://www.nwnetworks.com/mscsbasics.htm>, 6 pages.	
	C103	Novell, Inc., "Novell's NetWare 4.1 Momentum Continues - NetWare 4 Now World's Best-Selling Network Operating System," [online], March 21, 1996, [retrieved on November 16, 2009]. Retrieved from the Internet: <URL: http://www.novell.com/news/press/archive/1996/03/pr96056.html>, 2 pages.	
	C104	Chapter 7: Maintaining the NetWare Server, "Supervising the Network," (undated), pages 514-517.	
	C105	Chapter 7: Designing a Data Protection Plan, (undated), pages 170-171.	
	C106	Concepts, Disk Driver and Disk Duplexing, (undated), pages 82-83.	
	C107	Network Engines, "P6000EXP Fault-tolerant Load-balanced Clustered Server," 1997, 3 pages.	
	C110	Sun Microsystems Computer Company, "Sun™ Enterprise™ 250 Server Owner's Guide," June 1998, Part No. 805-5160-10, Revision A, 324 pages.	
	C111	Sun Microsystems, Inc., "UltraSPARC™ -II CPU Module, Datasheet 400 MHz CPU, 2.0 MP E-Cache," July 1999, 28 pages.	

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First Named Inventor	William W.Y. Chu
Art Unit	2111
Examiner Name	Phan, Raymond Ngan
Attorney Docket Number	ACQI-010/10US 310578-2052

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	C113	Compaq Computer Corporation, et al., "Universal Serial Bus Specification," September 23, 1998, Revision 1.1, 327 pages.	
	C114	Compaq Computer Corporation, et al., "Universal Serial Bus Specification," April 27, 2000, Revision 2.0, 650 pages.	
	C115	Silicon Graphics International, "Additional Information for: IRIS FailSafe Administrator's Guide (IRIX 6.4)," [online], Document Number: 007-3109-003, Published April 6, 1997, [retrieved on November 5, 2009], Retrieved from the Internet: <URL: http://techpubs.sgi.com/library/tpl/cgi-bin/summary.cgi?coll=0640&db=bks&docnumber=...>, 2 pages.	
	C116	Origin and Onyx Theory of Operations Manual, Document Number 007-3439-002, 1997, Silicon Graphics, Inc., 124 pages.	
	C117	QuantumNet, Inc., QuantumNet 6000 Sharing Modules [online], 1996 [retrieved on November 16, 2009], Retrieved from the Internet: <URL: http://web.archive.org/web/19971011194326/www.quantumnet.com/dsq60xx.htm>, 3 pages.	
	C118	JL ChatCom, Inc., "ChatTwin," [retrieved on December 2, 2009], JL ChatCom, Inc., ChatterBox Communications and Server Solutions [online], Retrieved from the Internet: <URL: http://web.archive.org/web/19970104222644/www.jlchatcom.com/chattwin.htm>, 2 pages.	
	C119	EVERSYS, "Welcome to EverSys" [online], [retrieved on 11-16-2009], Retrieved from the Internet: <URL: http://web.archieve.org/web/19961104092834/www.eversys.com/index2.htm>, 1 page.	
	C120	EVERSYS, "Products" [online], [retrieved on 11-16-2009], Retrieved from the Internet: <URL: http://web.archieve.org/web/19961104093103/www.eversys.com/prodinfo.htm>, 2 pages.	
	C121	"Microsoft Press Computer Dictionary, Third Edition," Microsoft Press, 1997, pages 199 and 332, Kim Fryer ed.	
	C122	Excerpt from "Microsoft Computer Dictionary, 5th Edition", Microsoft Press, 2002, pages 96 and 547	
	C123	Excerpt from IEEE 100: The Authoritative Dictionary of IEEE Standards Terms (7th Ed., 2000), pages 78, 79 and 128	

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	C124	ANDERSON, C.R. et al., "IEEE 1355 HS-Links: Present Status and Future Prospects," [online], 1998, [retrieved on 08-11-2010], Retrieved from the Internet: <URL: http://www94.web.cern.ch/HIS/dshs/publications/wotug21/hslink/pdf/hslinkpaper.pdf>, 14 pages.	
	C125	MAMAKOS, L. et al., "Request for Comments 2516 - A method for Transmitting PPP Over Ethernet (PPPoE)," [online], 1999, [retrieved on 08-18-2010], Retrieved from the Internet: <URL: http://ttols.ietf.org/html/rfc2516>, 35 pages.	
	C126	HAAS, S., "The IEEE 1355 Standard: Developments, Performance and Application in High Energy Physics," Thesis for degree of Doctor of Philosophy, University of Liverpool, December 1998, 138 pages.	
	C127	"IEEE Std 1355-1995 Standard for Heterogeneous InterConnect (HIC)," Open Micro-processor systems Initiative (OMI), [online], October 30, 1998, [retrieved on 08-06-2010], Retrieved from the Internet: <URL: http://grouper.ieee.org/groups/1355/index.html>, 6 pages.	
	C128	GALLES, M., "Spider: A Hide-Speed Network Interconnect," IEEE Micro, 1997, pp. 34-39. (6 pages)	
	C129	Excerpt from "Microsoft Computer Dictionary, 4th Edition", Microsoft Press, 1999, pages 184-85, 241, 432 (7 pages)	
	C130	Excerpt from "Microsoft Computer Dictionary, 4th Edition", Microsoft Press, 1999, pages 40, 241, 432 (6 pages)	
	C131	Excerpt from IEEE 100: The Authoritative Dictionary of IEEE Standards Terms (7th Ed., 2000), pages 181,304 and 771.	
	C132	"Family of VME Technology Specifications," [online], date unknown, [retrieved on 12-29-2010], Retrieved from the Internet: <URL: http://www.vita.com/specifications.html>, 1 page.	
	CB001	"SQL Server and NT Cluster Manager Availability Demo," Microsoft WindowsNT Server, Microsoft Server Programmer Developers Conference, Nov. 4-6, 1996, 15 pages.	
	CB004	MPL Brochure, "The First Rugged All-in-One Industrial 486FDX-133 MHz PC," MPL [online], [retrieved on February 16, 2006]. Retrieved from the Internet at <URL: http://www.mpl.ch/DOCs/ds48600.pdf>, 2 pages.	
	CB006	SNYDER, J., "Better Management Through Consolidation," August 18, 1997, Network World [online], [retrieved on June 22, 2004]. Retrieved from the Internet at <URL: http://www.opus1.com/www.jms/nw-con-0818rev.html.>, pp. 1-6.	

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	CB041	GALITZINE, G., "Industrial Computers," April 1999, Internet Telephony Roundup [online], [retrieved on June 23, 2004]. Retrieved from the Internet at <URL: http://www.tmcnet.com/articles/itmag/0499/0499roundup.htm>, 5 pages.	
	CB042	CRYSTAL Group Press Release, "Crystal Group Products Offer Industrial PCs With Built-In Flexibility," March 1, 1997, Crystal Group Inc. [online], [retrieved on May 14, 2004]. Retrieved from the Internet at <URL: http://www.crystalpc.com/news/pressreleases/prodpr.asp>, 2 pages.	
	CB043	DY 4 Systems, Inc. Press Release, "Enhanced COTS SBC from DY 4 Systems Features 166MHz Pentium (TM) Processor," April 8, 1998, [online]. Retrieved from the Internet at <URL: http://www.realtime-info.be/VPR/layout/display/pr.asp?/PRID=363>, 2 pages.	
	CB044	DY 4 Systems, Inc. Product Brochure, "SVME/DMV-192 Pentium® II Single Board Computer," Revision D June 1999, pp. 1-9.	
	CB045	EVERSYS Corporation Web Product Brief, "System 8000," Bomara Associates [online], [retrieved on June 22, 2004]. Retrieved from the Internet at <URL: http://www.bomara.com/Eversys/brief/Default.htm>, 4 pages.	
	CB046	CUBIX Product Brochure, "ERS/FT II System (includes PowerSMP and RemoteServ/IS)," ©2000, Cubix [online], [retrieved on June 22, 2004]. Retrieved from the Internet at <URL: http://64.173.211.7/support/techinfo/system/ersft2/ersft2.htm>, 4 pages.	
	CB047	CUBIX Product Manual, "ERS II and ERS/FT II," Chapter 3, System Components, ©1997, Cubix [online], [retrieved on June 22, 2004]. Retrieved from the Internet at <URL: http://64.173.211.7/support/techinfo/manuals/ers2/ers2-c3.htm>, 21 pages.	
	CB048	CUBIX Product Manual, "ERS II and ERS/FT II," Chapter 6, Component Installation, ©1997, Cubix [online], [retrieved on June 22, 2004]. Retrieved from the Internet at <URL: http://64.173.211.7/support/techinfo/manuals/ers2/ers2-c6.htm>, 18 pages.	
	CB049	NT Enterprise, NT Product Pipeline - Hardware, "Cubix PowerSMP Series 4000," November 1997, Windows Magazine [online], [retrieved on June 22, 2004]. Retrieved from the Internet at <URL: http://www.techweb.com/winmag/library/1997/1101/ntent008.htm>, p. NT07, 1 page.	
	CB050	EVERSYS Corporation Slide Presentation, "Eversys System 8000 Consolidated Network Server, Market and Product Overview," Product to be Released March 1, 2007, [online]. Retrieved from the Internet at <URL: http://eversys.com>, 20 pages.	

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	CB051	CUBIX Customer Service Support System, "Click on the Front Panel That Matches Your System," ©2000, Cubix [online], [retrieved on June 22, 2004]. Retrieved from the Internet at <URL: http://64.173.211.7/support/techinfo/density/density.htm>, 1 page.	
	CC001	MPL Brochure, "The First Rugged All-in-One Industrial 486FDX-133 MHz PC," IMP486/IPM5 User Manual, 1998, 15 pages.	
	CK001	International Search Report for International Patent Application No. PCT/US99/09369, report mailed November 16, 1999, 7 pages.	
	CK002	International Preliminary Examination Report for International Patent Application No. PCT/US99/09369, report completed July 5, 2000, 4 pages.	
	CK003	IBM Corporation, "Grounding Spring for Peripheral Device and Bezel Bracket," IBM Technical Disclosure Bulletin, November 1, 1993, Vol. 36, No. 11, 2 pages.	
	CL001	DIGITAL SEMICONDUCTOR Product Brief, "21152 PCI-to-PCI Bridge," February 1996, 6 pages.	
	CL002	INTEL CORPORATION Architectural Overview, "Intel 430TX PCISET: 82439TX System Controller (MTXC)," February 1997, 4 pages.	
	CL003	INTEL CORPORATION Architectural Overview, "Intel 82371AB PCI-to-ISA/IDE XCELERATOR (PIIX4)," April 1997, 3 pages.	
	CL004	INTEL CORPORATION Advance Information, "Intel 440LX AGPSET: 82443LX PCI A.G.P. Controller (PAC)," August 1997, 4 pages.	
	CL005	NATIONAL SEMICONDUCTOR, "DS90CR215/DS90CR216 +3.3V Rising Edge Data Strobe LVDS 21-Bit Channel Link-66 MHz, July 1997, 2 pages.	
	CL006	NATIONAL SEMICONDUCTOR Product Folder, "DS90CR215 Plus-3.3V Rising Edge Data Strobe LVDS 21-Bit Channel and Link - 66 MHz," National Semiconductor Corporation [online], [retrieved on October 30, 1997]. Retrieved from the Internet at <URL: http://www.national.com/search/search.cgi/design?keywords=DS90CR215>, 2 pages.	
	CL007	VIDEO ELECTRONICS Standards Association (VESA), Plug and Display (P&D) Standard, P&D and Digital Transition Minimized Differential Signaling (TMDS) Video Transmission Overview, 1997, Version 1, Revision 0, pp. 13 & 31-34.	
	CN001	LIQUORMAN, M., "Convergent Technologies Had This Idea," December 5, 1997, Jesse Berst's Anchor Desk [online], [retrieved on July 10, 1998]. Retrieved from the Internet at: <URL: http://www.zdnet.com/anchordesk/talkback/talkback_56555.html>, 1 page.	

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	CN002	BERST, J., "Hope For The Modular PCs We All Really Want," December 5, 1997, Jesse Berst's Anchor Desk [online], [retrieved on July 10, 1998]. Retrieved from the Internet at: <URL: http://www.zdnet.com/anchordesk/story/story_1504.html>, 3 pages.	
	CN003	BOYD-MERRITT, R., "Upgradable-PC Effort Takes Divergent Paths," EE Times - Headline News [online], [retrieved on July 31, 1998]. Retrieved from the Internet at : <URL: http://techweb.cmp.com/eet/news/97/949news/effort.html>, 3 pages.	
	CN004	FAEGRE, D. S. et al., "CTOS Revealed - Unisys' Best-Kept Secret Is An Operating System Built For Distributed Business Applications," December 1994, Core Technologies, BYTE [online], [retrieved on July 10, 1998]. Retrieved from the Internet at: <URL: http://www.byte.com/art/9412/sec13/art2.htm>, 6 pages.	
	CN005	SPANG, K., "Component House: Design Technology for 'PCs in a Snap' - NeoSystems Offers Building Blocks," Computer Reseller News, April 21, 1997, Issue: 732, Section: Channel Assembly, TechWeb [online], [retrieved on July 31, 1998]. Retrieved from the Internet at: <URL: http://www.techweb.com/se/directlink.cgi?CRN19970421S0054>, 2 pages.	
	CN006	"Think Modular," June 10, 1997, PC Magazine [online], [retrieved on July 31, 1998]. Retrieved from the Internet at: <URL: wysiwyg://60/http://homezdnet.com/pcmag/issues/1611/pcmg0072.htm>, 1 page.	
	DA001	Office Action for U.S. Patent No. 6,718,415, mailed October 10, 2002, 7 pages.	
	DA002	Response for U.S. Patent No. 6,718,415, filed November 7, 2002, 9 pages.	
	DA003	Office Action for U.S. Patent No. 6,718,415, mailed January 29, 2003, 7 pages.	
	DA004	Response for U.S. Patent No. 6,718,415, filed March 6, 2003, 8 pages.	
	DA005	Office Action for U.S. Patent No. 6,718,415, mailed June 4, 2003, 8 pages.	
	DA006	Response for U.S. Patent No. 6,718,415, filed September 4, 2003, 10 pages.	
	DB001	Amendment Submitted With RCE for U.S. Patent No. 7,099,981, filed March 1, 2006, 23 pages.	
	DC001	Office Action for U.S. Patent No. 7,363,415, mailed on April 12, 2007, 23 pages.	
	DC002	Response for U.S. Patent No. 7,363,415, filed on April 24, 2007, 25 pages.	
	DD001	Office Action for U.S. Patent No. 7,328,297, mailed February 8, 2007, 5 pages.	
	DD002	Response for U.S. Patent No. 7,328,297, filed April 19, 2007, 32 pages.	
	DD003	Office Action for U.S. Patent No. 7,328,297, mailed July 12, 2007, 13 pages.	
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 14 of 26

Complete if Known	
Application Number	12/504,534
Filing Date	July 16, 2009
First Named Inventor	William W.Y. Chu
Art Unit	2111
Examiner Name	Phan, Raymond Ngan
Attorney Docket Number	ACQI-010/10US 310578-2052

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	DF001	Office Action for U.S. Patent No. 7,363,416, mailed April 12, 2007, 23 pages.	
	DF002	Response for U.S. Patent No. 7,363,416, filed April 24, 2007, 23 pages.	
	DG001	Office Action for U.S. Patent No. 7,376,779, mailed September 28, 2007, 24 pages.	
	DG002	Response for U.S. Patent No. 7,376,779, filed October 16, 2007, 23 pages.	
	DH001	Office Action for U.S. Patent No. 7,676,624, mailed December 1, 2008, 8 pages.	
	DH002	Response for U.S. Patent No. 7,676,624, filed January 13, 2009, 14 pages.	
	DH003	Supplemental Response for U.S. Patent No. 7,676,624, filed on February 6, 2009, 13 pages.	
	DI001	Office Action for U.S. Patent No. 7,818,487, mailed September 29, 2009, 10 pages.	
	DI002	Response for U.S. Patent No. 7,818,487, filed November 6, 2009, 3 pages.	
	DI003	Amendment for U.S. Patent No. 7,818,487, filed May 11, 2010, 15 pages.	
	DI004	Amendment Submitted After Notice of Allowance for U.S. Patent No. 7,818,487, filed August 17, 2010, 14 pages.	
	DJ001	Office Action for U.S. Publication No. 2010/0174844, mailed October 28, 2010, 11 pages.	
	DK001	Office Action for U.S. Patent No. 6,216,185, mailed April 12, 2000, 9 pages.	
	DK002	Response for U.S. Patent No. 6,216,185, filed August 3, 2000, 15 pages.	
	DK003	Office Action for U.S. Patent No. 6,216,185, mailed August 25, 2000, 9 pages.	
	DK004	Response for U.S. Patent No. 6,216,185, filed October 24, 2000, 10 pages.	
	DL001	Office Action for U.S. Patent No. 6,345,330, mailed June 15, 2000, 7 pages.	
	DL002	Amendment for U.S. Patent No. 6,345,330, filed September 12, 2000, 5 pages.	
	DL003	Restriction Requirement for U.S. Patent No. 6,345,330, mailed December 19, 2000, 5 pages.	
	DL004	Amendment filed with Continued Prosecution Application for U.S. Patent No. 6,345,330, filed January 17, 2001, 5 pages.	
	DL005	Office Action for U.S. Patent No. 6,345,330, mailed March 23, 2001, 6 pages.	
	DL006	Response to Office Action for U.S. Patent No. 6,345,330, filed July 19, 2001, 5 pages.	
	DM001	Office Action for U.S. Patent Application No. 09/642,628, mailed April 5, 2001, 9 pages.	
	DO001	Office Action for U.S. Application No. 10/963,825, mailed October 27, 2005, 25 pages.	
	DO002	Response for U.S. Application No. 10/963,825, filed January 9, 2006, 22 pages.	
	DO003	Office Action for U.S. Application No. 10/963,825, mailed May 31, 2006, 29 pages.	
	DO004	Amendment Submitted with RCE for U.S. Application No. 10/963,825, filed July 27, 2006, 29 pages.	
	DO005	Office Action for U.S. Application No. 10/963,825, mailed October 20, 2006, 28 pages.	

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Art Unit	2111
Examiner Name	Phan, Raymond Ngan
Attorney Docket Number	ACQI-010/10US 310578-2052

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	DO006	Appellants' Brief for U.S. Application No. 10/963,825, filed January 8, 2007, 31 pages.	
	DO007	Revised Appellants' Brief for U.S. Application No. 10/963,825, filed April 20, 2007, 34 pages.	
	DO008	Examiner's Answer for U.S. Application No. 10/963,825, mailed August 8, 2007, 30 pages.	
	DO009	Reply Brief for U.S. Application No. 10/963,825, filed September 4, 2007, 4 pages.	
	DO010	Decision on Appeal for U.S. Application No. 10/963,825, mailed February 4, 2009, 13 pages.	
	DO011	Amendment Submitted with RCE for U.S. Application No. 10/963,825, filed February 20, 2009, 24 pages.	
	DO012	Office Action for U.S. Application No. 10/963,825, mailed May 14, 2009, 5 pages.	
	DO013	Response for U.S. Application No. 10/963,825, filed May 22, 2009, 2 pages.	
	DO014	Office Action for U.S. Application No. 10/963,825, mailed September 15, 2009, 14 pages.	
	DO015	Response for U.S. Application No. 10/963,825, filed October 1, 2009, 7 pages.	
	DP001	Office Action for RE 41,294, mailed November 16, 2007, 10 pages.	
	DP002	Response for RE 41,294, filed December 20, 2007, 21 pages.	
	DP003	Office Action for RE 41,294, mailed April 15, 2008, 10 pages.	
	DP004	Amendment Submitted with RCE for RE 41,294, filed May 27, 2008, 14 pages.	
	DP005	Supplemental Amendment Submitted with RCE for RE 41,294, filed July 8, 2008, 12 pages.	
	DP006	Office Action for RE 41,294, mailed September 16, 2008, 11 pages.	
	DP007	Response for RE 41,294, filed October 30, 2008, 14 pages.	
	DP008	Supplemental Response for RE 41,294, filed February 20, 2009, 13 pages.	
	DP009	Supplemental Response for RE 41,294, filed August 17, 2009, 3 pages.	
	DP010	Examiner Interview Summary Record, mailed January 15, 2009, 1 page.	
	DQ001	Office Action for RE 41,076, mailed July 13, 2007, 38 pages.	
	DQ002	Response for RE 41,076, filed September 26, 2007, 18 pages.	
	DQ003	Office Action for RE 41,076, mailed October 17, 2007, 55 pages.	
	DQ004	Amendment Submitted with RCE for RE 41,076, filed November 5, 2007, 19 pages.	
	DQ005	Office Action for RE 41,076, mailed February 11, 2008, 62 pages.	
	DQ006	Response for RE 41,076, filed April 7, 2008, 18 pages.	
	DQ007	Office Action for RE 41,076, mailed June 9, 2008, 25 pages.	
	DQ008	Amendment Submitted with RCE for RE 41,076, filed December 8, 2008, 44 pages.	
	DQ009	Office Action for RE 41,076, mailed December 30, 2008, 8 pages.	
	DQ010	Response for RE 41,076, filed January 16, 2009, 14 pages.	

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Filing Date	July 16, 2009
First Named Inventor	William W.Y. Chu
Art Unit	2111
Examiner Name	Phan, Raymond Ngan
Attorney Docket Number	ACQI-010/10US 310578-2052

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	DQ011	Amendment Submitted with RCE for RE 41,076, filed August 4, 2009, 2 pages.	
	DQ012	Examiner Interview Summary Record, mailed February 24, 2009, 4 pages.	
	DQ013	Applicant Summary of Interview, filed March 24, 2009, 1 page.	
	DQ014	Examiner Interview Summary Record, mailed September 22, 2009, 5 pages.	
	DR001	Office Action for U.S. Application No. 12/322,858, mailed March 4, 2010, 24 pages.	
	DR002	Response for U.S. Application No. 12/322,858, filed June 4, 2010, 15 pages.	
	DR003	Office Action for U.S. Application No. 12/322,858, mailed June 25, 2010, 22 pages.	
	DR004	Response for U.S. Application No. 12/322,858, filed October 25, 2010, 12 pages.	
	DS001	Office Action for U.S. Application No. 12/577,074, mailed April 13, 2010, 7 pages.	
	DS002	Response for U.S. Application No. 12/577,074, filed July 13, 2010, 3 pages.	
	DS003	Office Action for U.S. Application No. 12/577,074, mailed November 10, 2010, 6 pages.	
	DT001	Office Action for U.S. Application No. 09/312,199, mailed March 26, 2003, 5 pages.	
	DT002	Response for U.S. Application No. 09/312,199, filed June 11, 2003, 5 pages.	
	DU001	Office Action for RE 41,092, mailed September 17, 2008, 8 pages.	
	DU002	Response for RE 41,092, filed October 27, 2008, 27 pages.	
	DU003	Examiner's Amendment for RE 41,092, mailed November 4, 2009, 4 pages.	
	DV001	Office Action for U.S. Application No. 11/545,056, mailed March 12, 2010, 26 pages.	
	DV002	Response for U.S. Application No. 11/545,056, filed June 14, 2010, 18 pages.	
	DW001	Office Action for U.S. Application No. 12/561,138, mailed September 29, 2010, 4 pages.	
	EA001	Request for Ex Parte Reexamination of US Patent No. 6,216,185, Control No. 90/010,816, filed January 8, 2010, 39 pages.	
	EA002	Request for Ex Parte Reexamination of US Patent No. 6,216,185, Control No. 90/010,816, filed January 8, 2010, Exhibit AA to Request Claim Charts with respect to the Hitachi '953 for Anticipation and Obviousness, 136 pages	
	EA003	Request for Ex Parte Reexamination of US Patent No. 6,216,185, Control No. 90/010,816, filed January 8, 2010, Exhibit BB Claim Charts with respect to Kobayashi for Anticipation and Obviousness, 128 pages	
	EA004	Request for Ex Parte Reexamination of US Patent No. 6,216,185, Control No. 90/010,816, filed January 8, 2010, Exhibit CC Claim Charts with respect to Byte for Anticipation and Obviousness, 122 pages	

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	EA005	Request for Ex Parte Reexamination of US Patent No. 6,216,185, Control No. 90/010,816, filed January 8, 2010, Exhibit DD Claim Charts with respect to the Hitachi '675 for Anticipation and Obviousness, 119 pages	
	EA006	Office Action in Ex Parte Reexamination of US Patent No. 6,216,185, Control No. 90/010,816, mailed July 27, 2010, 103 pages	
	EA007	Patent Owner's Response to Office Action in Ex Parte Reexamination of US Patent No. 6,216,185, Control No. 90/010,816, filed September 27, 2010, 55 pages	
	EB001	Request for Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, filed December 2, 2009, 44 pages.	
	EB002	Request for Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, filed December 2, 2009, Exhibit O, Declaration Under 37 CFR 1.132 of Vincent P. Conroy, 11-24-2009, 3 pages.	
	EB003	Request for Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, Replacement Exhibit AA, Claim Charts with respect to QuantumNet for Anticipation and Obviousness, filed January 5, 2010, 109 pages.	
	EB004	Request for Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, Replacement Exhibit BB, Claim Charts with respect to Chatcom for Anticipation and Obviousness, filed January 5, 2010, 91 pages.	
	EB005	Request for Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, Replacement Exhibit CC, Claim Charts with respect to QuantumNet for Anticipation and Obviousness, filed January 5, 2010, 85 pages.	
	EB006	Request for Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, Replacement Exhibit DD, Claim Charts with respect to the Origin2000 Manual for Obviousness, filed January 5, 2010, 72 pages.	
	EB007	Request for Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, Replacement Exhibit EE, Claim Charts with respect to Gallagher for Anticipation and Obviousness, filed January 5, 2010, 107 pages.	
	EB008	Office Action in Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, mailed May 26, 2010, 39 pages.	
	EB009	Patent Owner's Response to Office Action in Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, filed July 27, 2010, 41 pages.	

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	EC005	Request for Inter Partes Reexamination of US Patent No. 7,099,981, Control No. 95/001,310, Exhibit CC, Claim Charts with respect to Chatcom for Anticipation and Obviousness, filed February 9, 2010, 167 pages	
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	ED002	Request for Inter Partes Reexamination of US Patent No. 7,146,446, Control No. 95/001,328, Exhibit AA (Part 1), Claim Charts with respect to Gallagher for Anticipation and Obviousness, filed March 19, 2010, 186 pages.	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 19 of 26

Complete if Known	
Application Number	12/504,534
Filing Date	July 16, 2009
First Named Inventor	William W.Y. Chu
Art Unit	2111
Examiner Name	Phan, Raymond Ngan
Attorney Docket Number	ACQI-010/10US 310578-2052

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	ED003	Request for Inter Partes Reexamination of US Patent No. 7,146,446, Control No. 95/001,328, Exhibit AA (Part 2), Claim Charts with respect to Gallagher for Anticipation and Obviousness, filed March 19, 2010, 161 pages.	
	ED004	Request for Inter Partes Reexamination of US Patent No. 7,146,446, Control No. 95/001,328, Exhibit BB (Part 1), Claim Charts with respect to QuantumNet for Anticipation and Obviousness, filed March 19, 2010, 139 pages.	
	ED005	Request for Inter Partes Reexamination of US Patent No. 7,146,446, Control No. 95/001,328, Exhibit BB (Part 2), Claim Charts with respect to QuantumNet for Anticipation and Obviousness, filed March 19, 2010, 128 pages.	
	ED006	Request for Inter Partes Reexamination of US Patent No. 7,146,446, Control No. 95/001,328, Exhibit CC, Claim Charts with respect to Chatcom for Anticipation and Obviousness, filed March 19, 2010, 68 pages.	
	ED007	Office Action in Inter Partes Reexamination of US Patent No. 7,146,446, Control No. 95/001,328, mailed June 24, 2010, 86 pages.	
	ED008	Patent Owner's Response to Office Action in Inter Partes Reexamination of US Patent No. 7,146,446, Control No. 95/001,328, filed August 24, 2010, 45 pages.	
	ED009	Patent Owner's Response to Office Action in Inter Partes Reexamination of US Patent No. 7,146,446, Control No. 95/001,328, Exhibit A, Declaration of William Henry Mangione-Smith under 37 C.F.R. 1.132, filed September 3, 2010, 61 pages.	
	EE001	Request for Inter Partes Reexamination of US Patent No. 7,328,297, Control No. 95/001,336, filed April 19, 2010, 33 pages.	
	EE002	Request for Inter Partes Reexamination of US Patent No. 7,328,297, Control No. 95/001,336, Exhibit AA, Claim Charts with respect to Gallagher for Obviousness, filed April 19, 2010, 131 pages.	
	EE003	Request for Inter Partes Reexamination of US Patent No. 7,328,297, Control No. 95/001,336, Exhibit BB, Claim Charts with respect to QuantumNet for Obviousness, filed April 19, 2010, 139 pages.	
	EE004	Request for Inter Partes Reexamination of US Patent No. 7,328,297, Control No. 95/001,336, Exhibit CC, Claim Charts with respect to Chatcom for Obviousness, filed April 19, 2010, 114 pages.	
	EE005	Office Action in Inter Partes Reexamination of US Patent No. 7,328,297, Control No. 95/001,336, mailed August 4, 2010, 95 pages.	

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	EE006	Patent Owner's Response to Office Action in Inter Partes Reexamination of US Patent No. 7,328,297, Control No. 95/001,336, filed October 4, 2010, 49 pages.	
	EE007	Patent Owner's Response to Office Action in Inter Partes Reexamination of US Patent No. 7,328,297, Control No. 95/001,336, Exhibit A, Declaration of William Henry Mangione-Smith under 37 C.F.R. 1.132, filed October 4, 2010, 61 pages.	
	EF001	Request for Inter Partes Reexamination of US Patent No. 7,363,415, Control No. 95/001,424, filed August 25, 2010, 34 pages.	
	EF002	Request for Inter Partes Reexamination of US Patent No. 7,363,415, Control No. 95/001,424, Exhibit AA, Claim Charts with respect to Gallagher and Other References for Obviousness, filed August 25, 2010, 114 pages.	
	EF003	Request for Inter Partes Reexamination of US Patent No. 7,363,415, Control No. 95/001,424, Exhibit AB, Claim Charts with respect to Gallagher and Other References for Obviousness, filed August 25, 2010, 92 pages.	
	EF004	Request for Inter Partes Reexamination of US Patent No. 7,363,415, Control No. 95/001,424, Exhibit BA, Claim Charts with respect to QuantumNet and Other References for Obviousness, filed August 25, 2010, 121 pages.	
	EF005	Request for Inter Partes Reexamination of US Patent No. 7,363,415, Control No. 95/001,424, Exhibit BB, Claim Charts with respect to QuantumNet and Other References for Obviousness, filed August 25, 2010, 99 pages.	
	EF006	Request for Inter Partes Reexamination of US Patent No. 7,363,415, Control No. 95/001,424, Exhibit CA, Claim Charts with respect to Chatcom and Other References for Obviousness, filed August 25, 2010, 91 pages.	
	EF007	Request for Inter Partes Reexamination of US Patent No. 7,363,415, Control No. 95/001,424, Exhibit CB, Claim Charts with respect to Chatcom and Other References for Obviousness, filed August 25, 2010, 94 pages.	
	EF008	Office Action in Inter Partes Reexamination of US Patent No. 7,363,415, Control No. 95/001,424, mailed November 1, 2010, 75 pages.	
	EG001	Request for Inter Partes Reexamination of US Patent No. 7,376,779, Control No. 95/001,475, filed October 27, 2010, 35 pages.	
	EG002	Request for Inter Partes Reexamination of US Patent No. 7,376,779, Control No. 95/001,475, Exhibit AA, Claim Charts with respect to Gallagher and Other References for Obviousness, filed October 27, 2010, 128 pages.	

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Attorney Docket Number	ACQI-010/10US 310578-2052

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	EG003	Request for Inter Partes Reexamination of US Patent No. 7,376,779, Control No. 95/001,475, Exhibit AB, Claim Charts with respect to Gallagher and Other References for Obviousness, filed October 27, 2010, 153 pages.	
	EG004	Request for Inter Partes Reexamination of US Patent No. 7,376,779, Control No. 95/001,475, Exhibit BA, Claim Charts with respect to QuantumNet and Other References for Obviousness, filed October 27, 2010, 108 pages.	
	EG005	Request for Inter Partes Reexamination of US Patent No. 7,376,779, Control No. 95/001,475, Exhibit BB, Claim Charts with respect to QuantumNet and Other References for Obviousness, filed October 27, 2010, 112 pages.	
	EG006	Request for Inter Partes Reexamination of US Patent No. 7,376,779, Control No. 95/001,475, Exhibit CA, Claim Charts with respect to Chatcom and Other References for Obviousness, filed October 27, 2010, 112 pages.	
	EG007	Request for Inter Partes Reexamination of US Patent No. 7,376,779, Control No. 95/001,475, Exhibit CB, Claim Charts with respect to Chatcom and Other References for Obviousness, filed October 27, 2010, 118 pages.	
	EG008	Office Action in Inter Partes Reexamination of US Patent No. 7,376,779, Control No. 95/001,475, mailed December 20, 2010, 105 pages.	
	EH001	Request for Inter Partes Reexamination of US Patent No. 7,363,416, Control No. 95/001,476, filed October 27, 2010, 37 pages.	
	EH002	Request for Inter Partes Reexamination of US Patent No. 7,363,416, Control No. 95/001,476, Exhibit AA, Claim Charts with respect to Gallagher and Other References for Obviousness, filed October 27, 2010, 70 pages.	
	EH003	Request for Inter Partes Reexamination of US Patent No. 7,363,416, Control No. 95/001,476, Exhibit AB, Claim Charts with respect to Gallagher and Other References for Obviousness, filed October 27, 2010, 64 pages.	
	EH004	Request for Inter Partes Reexamination of US Patent No. 7,363,416, Control No. 95/001,476, Exhibit BA, Claim Charts with respect to QuantumNet and Other References for Obviousness, filed October 27, 2010, 64 pages.	
	EH005	Request for Inter Partes Reexamination of US Patent No. 7,363,416, Control No. 95/001,476, Exhibit BB, Claim Charts with respect to QuantumNet and Other References for Obviousness, filed October 27, 2010, 71 pages.	

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Sheet 22 of 26

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Filing Date	July 16, 2009
First Named Inventor	William W.Y. Chu
Art Unit	2111
Examiner Name	Phan, Raymond Ngan
Attorney Docket Number	ACQI-010/10US 310578-2052

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	EH007	Request for Inter Partes Reexamination of US Patent No. 7,363,416, Control No. 95/001,476, Exhibit CB, Claim Charts with respect to Chatcom and Other References for Obviousness, filed October 27, 2010, 67 pages.	
	EH008	Office Action in Inter Partes Reexamination of US Patent No. 7,363,416, Control No. 95/001,476, mailed December 6, 2010, 63 pages.	
	IC01	"Defendants' Amended Invalidity Contentions," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 18 pages.	
	IC02	"Exhibit A (Asserted Claims)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 2 pages.	
	IC03	"Exhibit B - Table 1," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 75 pages.	
	IC04	"Exhibit C," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 2 pages.	
	IC05	"Exhibit D," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 106 pages.	
	IC06	"Exhibit E," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 2 pages.	
	IC07	"Invalidity Chart for Base Reference IBM 8260," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 53 pages.	
	IC08	"Invalidity Chart for Base Reference IBM 8265," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 56 pages.	
	IC09	"Invalidity Chart for Base Reference U.S. Patent No. 4,453,215 (Reid)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 56 pages.	

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	IC10	"Invalidity Chart for Base Reference Origin2000," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 56 pages.	
	IC11	"Invalidity Chart for Base Reference QuantumNet," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 49 pages.	
	IC12	"Invalidity Chart for Base Reference U.S. Patent No. 6,564,274 (Heath)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 57 pages.	
	IC13	"Invalidity Chart for Base Reference U.S. Patent No. 5,577,205," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 60 pages.	
	IC14	"Invalidity Chart for Base Reference U.S. Patent No. 5,802,391," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 61 pages.	
	IC15	"Invalidity Chart for Base Reference U.S. Patent No. 6,715,100," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 64 pages.	
	IC16	"Invalidity Chart for Base Reference Cubix BC/Density," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 64 pages.	
	IC17	"Invalidity Chart for Base Reference JP6-289956," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 62 pages.	
	IC18	"Invalidity Chart for Base Reference Gallagher 068 and Gallagher 503," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 108 pages.	
	IC19	"Invalidity Chart for Base Reference Compaq ProLiant Cluster," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 81 pages.	

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	IC20	"Invalidity Chart for Base Reference U.S. Patent No. 5,325,517 to Baker et al. (Appendix 1, Exhibit 15)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 59 pages.	
	IC21	"Invalidity Chart for Japanese Patent Application H7-64672 (Toshiba '672)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 55 pages.	
	IC22	"Invalidity Chart for Base Reference ChatCom," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 52 pages.	
	IC23	"Invalidity Chart for Base Reference Ziatech Corp. Ketris 9000 System," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 68 pages.	
	IC24	"Invalidity Chart for Base Reference Ziatech STD 32 Star System," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 62 pages.	
	IC25	"Invalidity Chart for Base Reference U.S. Patent No. 7,339,786 (Bottom et al.)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 57 pages.	
	IC26	"Invalidity Chart for Base References RLX Patents, U.S. Patent Nos. 6,747,878, 6,411,506, 6,325,636, 6,757,748, and 6,985,967 (Hipp et al.)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 58 pages.	
	IC27	"Invalidity Chart for Base Reference Network Engines P6000 Server," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 59 pages.	
	IC28	"Invalidity Chart for Base Reference Eversys 8000 System," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 60 pages.	
	IC29	"Invalidity Chart for Base Reference Eversys CAPserver," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 59 pages.	

Examiner Signature	/Raymond Phan/	Date Considered	05/09/2011

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Sheet 25 of 26

Complete if Known	
Application Number	12/504,534
Filing Date	July 16, 2009
First Named Inventor	William W.Y. Chu
Art Unit	2111
Examiner Name	Phan, Raymond Ngan
Attorney Docket Number	ACQI-010/10US 310578-2052

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	IC30	"Invalidity Chart for Base Reference U.S. 5,809,262," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 62 pages.	
	IC31	"Invalidity Chart for Base Reference WhiteCross 9800 System," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 62 pages.	
	IC32	"Invalidity Chart for Base Reference U.S. 5,339,408," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 61 pages.	
	IC33	"Invalidity Chart for Base Reference Tyuluman 536," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 76 pages.	
	IC34	"Invalidity Chart for Base Reference Hong 737," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 77 pages.	
	IC35	"Invalidity Chart for Base Reference U.S. 5,436,857 (Nelson)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 6 pages.	
	IC36	"Invalidity Chart for Base Reference U.S. 5,999,952 (Jenkins)", submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 6 pages.	
	IC37	"Invalidity Chart for Base Reference U.S. 5,608,608 (Flint)", submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 6 pages.	
	IC38	"Invalidity Chart for Base Reference U.S. 5,978,821 (Freeny)", submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 6 pages.	
	IC39	"Invalidity Chart for Base Reference WO 92/18924 (Wallsten)", submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 6 pages.	

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	IC40	"Invalidity Chart for Base Reference Ergo Moby Brick", submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 5 pages.	
	IC41	"Invalidity Chart for Base Reference U.S. Patent No. 5,463,742 (Kobayashi)", submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 5 pages.	
	IC42	"Invalidity Chart for Base Reference Japanese Patent Application Publication H6-289953 (Hitachi)", submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 5 pages.	
	IC43	"Invalidity Chart for Base Reference Japanese Patent Application Publication H7-84675 (Hitachi)", submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 5 pages.	
	IC44	"Invalidity Chart for Base Reference U.S. Patent No. 5,187,645 (Spalding)", submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 6 pages.	
	IC45	"Defendants' Notice of Errata Relating to Defendants' P.R. 3-3 Invalidity Contentions," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 14 pages.	
	IF01	"Exhibit 5 - Disclosure of Asserted Claims and Infringement Contentions", submitted by the Plaintiff in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED, 14 pages.	
	F01	"Memorandum Opinion and Order Construing Claim Terms and Denying Defendants' Motion for Partial Summary Judgment," Issued by the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on August 2, 2010, 18 pages.	
	H01	"Transcript of Videotaped Deposition of William Mangione-Smith," taken by the Defendants in connection with Case No. 6:09-cv-148-LED in the U.S. District Court for the Eastern District of Texas, September 9, 2010, 192 pages.	

Examiner Signature	/Raymond Phan/	Date Considered	05/09/2011

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Application Number	12504534
Filing Date	2009-07-16
First Named Inventor	William W.Y. Chu
Art Unit	2111
Examiner Name	Phan, Raymond Ngan
Attorney Docket Number	ACQI-010/10US 310578-2052

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	Attorney Docket Number	ACQI-010/10US 310578-2052

	1	"Memorandum Opinion and Order Construing Claim Terms," Issued by the U.S. District Court for the Eastern District of Texas, Tyler Division, Case No. 6:09-cv-148-LED, Document 602, Feb. 3, 2011, 12 pgs.	☐

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Examiner Name	Phan , Raymond Ngan
Attorney Docket Number	ACQI-010/10US 310578-2052

	1	CHU, Inter Partes Reexam of USP 6,718,415, Reexam Control No. 95/001,276, "Final Judgement", issued by the US District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2011, 1 pg.	☐
	2	CHU, Inter Partes Reexam of USP 6,718,415, Reexam Control No. 95/001,276, "Jury Verdict Form", Executed by Jury in the US District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on February 23, 2011, 2 pgs.	☐
	3	CHU, Inter Partes Reexam of USP 6,718,415, Reexam Control No. 95/001,276, "Supplemental Comments by Third Party Requestor Pursuant to 37 CFR 1.947", 05/12/11, 45 pgs.	☐
	4	CHU, Inter Partes Reexam of USP 6,718,415, Reexam Control No. 95/001,276, "Supplemental Comments by Third Party Requestor Pursuant to 37 CFR 1.947, Exhibit AA-2: Claim Charts with Respect to QuantumNet", 05/12/11, 120 pgs.	☐
	5	CHU, Inter Partes Reexam of USP 6,718,415, Reexam Control No. 95/001,276, "Supplemental Comments by Third Party Requestor Pursuant to 37 CFR 1.94, 7Exhibit BB-2: Claim Charts with Respect to Chatcom", 05/12/11, 94 pgs.	☐
	6	CHU, Inter Partes Reexam of USP 6,718,415, Reexam Control No. 95/001,276, "Supplemental Comments by Third Party Requestor Pursuant to 37 CFR 1.947, Exhibit CC-2: Claim Charts with Respect to Eversys", 05/12/11, 165 pgs.	☐
	7	CHU, Inter Partes Reexam of USP 6,718,415, Reexam Control No. 95/001,276, "Supplemental Comments by Third Party Requestor Pursuant to 37 CFR 1.947, Exhibit DD-2: Claim Charts with Respect to Origin2000 Manual", 05/12/11, 108 pgs.	☐
	8	CHU, Inter Partes Reexam of USP 6,718,415, Reexam Control No. 95/001,276, "Supplemental Comments by Third Party Requestor Pursuant to 37 CFR 1.947, Exhibit EE-2: Claim Charts with Respect to Gallagher", 05/12/11, 91 pgs.	☐
	9	KUNZMAN et al., "1394 High Performance Serial Bus: The Digital Interface for ATV", IEEE Transactions on Consumer Electronics, Vol. 41, No. 3, 3 Aug 1995, pp. 893-900	☐
	10	PARKES, SM, "High-Speed, Low-Power, Excellent EMC: LVDS For On-Board Data Handling," Proceedings of 6th International Workshop on Digital Signal Processing Techniques for Space Applications, IEEE (1998), Sep. 1998, pp. 16 ("Parkes 1355") [includes a reference page establishing date of publication retrieved from <http://spacetech.dundee.ac.uklresearch/spacecraft-onboard-data-handling/publications/high-speed-low-power-excellent-emc-lvds-board>	☐

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	1	WO9700481	WO		1997-01-03	Intel Corporation		☐

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	1	PC MAGAZINE, "Think Modular" (06-10-1997)	☐
	2	LIQUORMAN, "Convergent Technologies Had This Idea" (12/05/1997)	☐
	3	BERST, "Hope For The Modular PCs We all Really Want" (12/05/1997)	☐
	4	BOYD-MERRITT, "Upgradable-PC Effort Takes Divergent Paths" (EE Times 1997) http://techweb.cmp/com/eet/news/97/949news/effort.html	☐
	5	FAEGRE, et al., "Unisys' Best-Kept Secret Is An Operating System Built For Distributed Business Applications." BYTE (12/1994)	☐
	6	SPANG, "Component House: Design Technology For 'PCs in a snap' -- NeoSystems Offers Building Blocks" TECHWEB (04/21/1997:732)	☐

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Examiner Signature	/Raymond Phan/	Date Considered	05/09/2011

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571) 273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

58249
COOLEY LLP
777 6th Street, NW Suite 1100
Washington, DC 20001

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/504,534	07/16/2009	William W. Y. Chu	ACQI-010/10US 310578-2052	1286

TITLE OF INVENTION: MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNIDIRECTIONAL SERAL BIT CHANNELS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$1810	09/06/2011

EXAMINER	ART UNIT	CLASS-SUBCLASS
PHAN, RAYMOND NGAN	2111	710-313000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 COOLEY LLP
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: ACQIS LLC
(B) RESIDENCE: (CITY and STATE OR COUNTRY): McKinney, Texas

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☑ Corporation or other private group entity ☐ Government

4a. The following fee(s) are enclosed:
☑ Issue Fee
☑ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s):
☐ A check in the amount of the fee(s) is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☑ The Director is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number 50-1283 .

5. **Change in Entity Status** (from status indicated above)
☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
☑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

The Director of the USPTO is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.
NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date July 8, 2011

Typed or printed name Cliff Z. Liu Registration No. 50,834

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	William W.Y. Chu	Confirmation No.:	1286
Serial No.:	12/504,534	Examiner:	Phan , Raymond Ngan
Filed:	July 16, 2009	Group Art Unit:	2111

For: MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNIDIRECTIONAL SERIAL BIT CHANNELS TO TRANSMIT ENCODED PERIPHERAL COMPONENT INTERCONNECT BUS TRANSACTION DATA

Mail Stop: Issue Fee
Commissioner for Patents
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Alexandria, VA 22313-1450

AMENDMENT UNDER 37 CFR §1.312

In response to the Notice of Allowance mailed June 3, 2011, please amend the subject application as follows:

Amendments to the Specification begin on page 2 of this paper.

Remarks begin on page 3 of this paper.

IN THE SPECIFICATION

Please replace the title with the following amended title. The amendments to the title are indicated by strikethrough and underlining.

MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING ~~UNDIRECTIONAL~~ UNIDIRECTIONAL SERIAL BIT CHANNELS TO TRANSMIT ENCODED PERIPHERAL COMPONENT INTERCONNECT BUS TRANSACTION DATA

REMARKS

The Examiner has previously objected to the title of the subject application in the Office Action mailed October 28, 2010. The title is amended to be more descriptive, and to correct a typographical error. No new matter is added. Applicant respectfully requests entry of these amendments, as they neither require further consideration or further search.

Conclusion

If there are any residual issues that need to be resolved prior to issuance of the application, the Examiner is requested to contact the undersigned.

The Commissioner is hereby authorized to charge any required fees and to credit any overpayments to Cooley LLP's deposit account No. 50-1283.

Date: July 7, 2011

Respectfully submitted,
COOLEY LLP

By: _____
Cliff Z. ~~Liu~~
Reg. No. 50,834

Customer No. 58249
COOLEY LLP
ATTN: Patent Group
777 6th Street NW, Suite 1100
Washington, DC 20001
Tel: (650) 843-5852
Fax: (202) 842-7899

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	12504534
Filing Date	2009-07-16
First Named Inventor	William W.Y. Chu
Art Unit	2111
Examiner Name	Phan, Raymond Ngan
Attorney Docket Number	ACQI-010/10US 310578-2052

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	12504534
	Filing Date	2009-07-16
	First Named Inventor	William W.Y. Chu
	Art Unit	2111
	Examiner Name	Phan, Raymond Ngan
	Attorney Docket Number	ACQI-010/10US 310578-2052

	1	Request for Inter Partes Reexamination of US Patent No. 7,099,981, Control No. 95/001,310, "Comments by Third Party Requester", filed April 8, 2011, total: 32 pgs.	☐
	2	Request for Inter Partes Reexamination of US Patent No. 7,146,446, Control No. 95/001,328, Comments by Third Party Requester", filed April 8, 2011, 23 pgs.	☐
	3	Request for Inter Partes Reexamination of US Patent No. 7,376,779, Control No. 95/001,475, Banankhah, Majid A., Art Unit 3992, Action Closing Prosecution, April 27, 2011, 209 pgs.	☐
	4	Request for Inter Partes Reexamination of US Patent No. 7,328,297, Control No. 95/001,336, "Supplemental Comments by Third Party Requester" filed May 12, 2011, 32 pgs.	☐
	5	Request for Ex Parte Reexamination of US Patent No. 6,216,185, Control No. 90/010,816, Banankhah, Majid A., Art Unit 3992, Nonfinal Office Action, June 14, 2011, 44 pgs.	☐
	6	Request for Inter Partes Reexamination of US Patent No. 7,376,779, Control No. 95/001,475, "Comments by Third Party Requestor", filed June 24, 2011, 24 pgs.	☐

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	12504534
	Filing Date	2009-07-16
	First Named Inventor	William W.Y. Chu
	Art Unit	2111
	Examiner Name	Phan, Raymond Ngan
	Attorney Docket Number	ACQI-010/10US 310578-2052

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☒ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☒ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Cliff Z. Liu/	Date (YYYY-MM-DD)	2011-07-08
Name/Print	Cliff Z. Liu	Registration Number	50834

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	12504534
Filing Date:	16-Jul-2009
Title of Invention:	MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNDIRECTIONAL SERIAL BIT CHANNELS
First Named Inventor/Applicant Name:	William W. Y. Chu
Filer:	Cliff Z. Liu/Bobbie Jutras
Attorney Docket Number:	ACQI-010/10US 310578-2052

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1510	1510
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
		Total in USD ($)		**1990**

Electronic Acknowledgement Receipt

EFS ID:	10484049
Application Number:	12504534
International Application Number:	
Confirmation Number:	1286
Title of Invention:	MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNDIRECTIONAL SERIAL BIT CHANNELS
First Named Inventor/Applicant Name:	William W. Y. Chu
Customer Number:	58249
Filer:	Cliff Z. Liu/Bobbie Jutras
Filer Authorized By:	Cliff Z. Liu
Attorney Docket Number:	ACQI-010/10US 310578-2052
Receipt Date:	08-JUL-2011
Filing Date:	16-JUL-2009
Time Stamp:	20:13:33
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$1990
RAM confirmation Number	15481
Deposit Account	501283
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	ACQI-010-10US_07-08-11_IFPmt.pdf	420301 33d51b0c1497479ad0d8e615c1e430d879118fc3	no	1
Warnings:					
Information:					
2	Amendment after Notice of Allowance (Rule 312)	ACQI-010-10US_07-08-11_312Amd.pdf	348535 2c789c752a4fa13e55e7a8728ff5d12fef61a5f0	no	3
Warnings:					
Information:					
3	Information Disclosure Statement (IDS) Form (SB08)	ACQI-010-10US_07-08-11_IDS.pdf	612624 33aa6fa0475f94824343aa4c2ebaced0f3e65591	no	4
Warnings:					
Information:					
A U.S. Patent Number Citation or a U.S. Publication Number Citation is required in the Information Disclosure Statement (IDS) form for autoloading of data into USPTO systems. You may remove the form to add the required data in order to correct the Informational Message if you are citing U.S. References. If you chose not to include U.S. References, the image of the form will be processed and be made available within the Image File Wrapper (IFW) system. However, no data will be extracted from this form. Any additional data such as Foreign Patent Documents or Non Patent Literature will be manually reviewed and keyed into USPTO systems.					
4	Non Patent Literature	04-08-11_Third_Party_Comments_ACQI-010-12US.pdf	1698144 622282adae75b8b6932cebb2b691c9779f83e6d5	no	32
Warnings:					
Information:					
5	Non Patent Literature	04-08-11_Third_Party_Comments_ACQI-010-13US.pdf	1205217 8049457068b0c64d0609edf5d8cba37dcfc305fe	no	23
Warnings:					
Information:					
6	Non Patent Literature	04-27-11_Action_Closing_Prosecution_ACQI-010-17US.pdf	10004344 3f6bd5583815facf872e5cce0669a99665988f7d	no	209
Warnings:					
Information:					
7	Non Patent Literature	05-12-11_Third_Party_Requester_Suppl_Comments_ACQI-010-14US.pdf	1633661 6d8ad1a82b652be84c684c90829aeb8b78900134	no	32
Warnings:					
Information:					
8	Non Patent Literature	06-14-11_Nonfinal_Office_Action_ACQI-001-05US.pdf	2368447 20318601f44abc80831244029fdc1e38c314d042	no	44

Warnings:					
Information:					
9	Non Patent Literature	06-24-11_Third_Party_Comments_ACQI-010-17US.pdf	1139723 0663433acd1faa4791a76f00d0657e6a3553eacc	no	24
Warnings:					
Information:					
10	Fee Worksheet (SB06)	fee-info.pdf	34077 0074f38bb1dda6b0d3feab1fd2d8b6e6dfebb0ba	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	19465073		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

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United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

Bib Data Sheet

CONFIRMATION NO. 1286

SERIAL NUMBER	FILING OR 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
12/504,534	07/16/2009 RULE	710	2111	ACQI-010/10US 310578-2052

APPLICANTS

William W. Y. Chu, Los Altos, CA;

**** CONTINUING DATA ***************************

This application is a CON of 12/077,503 03/18/2008 PAT 7,676,624
which is a CON of 11/166,656 06/24/2005 PAT 7,376,779
which is a CON of 11/097,694 03/31/2005 PAT 7,363,415
which is a CON of 10/772,214 02/03/2004 PAT 7,099,981
which is a CON of 09/569,758 05/12/2000 PAT 6,718,415
which claims benefit of 60/134,122 05/14/1999

**** FOREIGN APPLICATIONS *********************

IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** SMALL ENTITY **
** 07/27/2009

Foreign Priority claimed	35 USC 119 (a-d) conditions met	Verified and Acknowledged	STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
☐ yes ☑ no	☐ yes ☑ no ☐ Met after Allowance	Examiner's Signature Initials	CA	24	43	13

ADDRESS
58249

TITLE
MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNDIRECTIONAL SERIAL BIT CHANNELS TO TRANSMIT ENCODED PERIPHERAL COMPONENT INTERCONNECT BUS TRANSACTION DATA

FILING FEE RECEIVED		
7340	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/504,534	07/16/2009	William W. Y. Chu	ACQI-010/10US 310578-2052	1286

58249 7590 07/14/2011

COOLEY LLP
ATTN: Patent Group
Suite 1100
777 - 6th Street, NW
WASHINGTON, DC 20001

EXAMINER	
PHAN, RAYMOND NGAN	

ART UNIT	PAPER NUMBER
2111	

MAIL DATE	DELIVERY MODE
07/14/2011	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Response to Rule 312 Communication	Application No.	Applicant(s)
	12/504,534	CHU, WILLIAM W. Y.
	Examiner	Art Unit

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address –

1. ☒ The amendment filed on *08 July 2011* under 37 CFR 1.312 has been considered, and has been:

   a) ☒ entered.

   b) ☐ entered as directed to matters of form not affecting the scope of the invention.

   c) ☐ disapproved because the amendment was filed after the payment of the issue fee.
   Any amendment filed after the date the issue fee is paid must be accompanied by a petition under 37 CFR 1.313(c)(1) and the required fee to withdraw the application from issue.

   d) ☐ disapproved. See explanation below.

   e) ☐ entered in part. See explanation below.

Publishing Division

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CONFIRMATION NO. 1286

Bib Data Sheet

SERIAL NUMBER	FILING OR 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
12/504,534	07/16/2009 RULE	710	2111	ACQI-010/10US 310578-2052

APPLICANTS

William W. Y. Chu, Los Altos, CA;

**** CONTINUING DATA ***************************

This application is a CON of 12/077,503 03/18/2008 PAT 7,676,624
which is a CON of 11/166,656 06/24/2005 PAT 7,376,779
which is a CON of 11/097,694 03/31/2005 PAT 7,363,415
which is a CON of 10/772,214 02/03/2004 PAT 7,099,981
which is a CON of 09/569,758 05/12/2000 PAT 6,718,415
which claims benefit of 60/134,122 05/14/1999

**** FOREIGN APPLICATIONS *********************

IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** SMALL ENTITY **
** 07/27/2009

Foreign Priority claimed	STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
☐ yes ☐ no	CA	24	43	13
35 USC 119 (a-d) conditions met ☐ yes ☐ no ☐ Met after Allowance				
Verified and Acknowledged Examiner's Signature Initials				

ADDRESS
58249

TITLE
MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNIDIRECTIONAL SERIAL BIT CHANNELS TO TRANSMIT ENCODED PERIPHERAL COMPONENT INTERCONNECT BUS TRANSACTION DATA

FILING FEE RECEIVED	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:
7340	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/504,534	07/16/2009	William W. Y. Chu	ACQI-010/10US 310578-2052	1286

58249 7590 09/14/2011

COOLEY LLP
ATTN: Patent Group
Suite 1100
777 - 6th Street, NW
WASHINGTON, DC 20001

EXAMINER	
PHAN, RAYMOND NGAN	
ART UNIT	**PAPER NUMBER**
2111	

MAIL DATE	DELIVERY MODE
09/14/2011	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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U.S. Patent and Trademark Office
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APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR / PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.
12/504,534	16 July, 2009	CHU, WILLIAM W. Y.	ACQI-010/10US 310578-2052

COOLEY LLP
ATTN: Patent Group
Suite 1100
777 - 6th Street, NW
WASHINGTON, DC 20001

EXAMINER	
RAYMOND PHAN	
ART UNIT	PAPER
2111	20110912

DATE MAILED:

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner for Patents

PTO-1449, received on July 8, 2011, was considered by the Examiner.

/RAYMOND N PHAN/
Primary Examiner, Art Unit 2111

PTO-90C (Rev.04-03)

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /R.P./

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	12504534
Filing Date	2009-07-16
First Named Inventor	William W.Y. Chu
Art Unit	2111
Examiner Name	Phan, Raymond Ngan
Attorney Docket Number	ACQI-010/10US 310578-2052

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2]	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /R.P./

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	12504534
	Filing Date	2009-07-16
	First Named Inventor	William W.Y. Chu
	Art Unit	2111
	Examiner Name	Phan, Raymond Ngan
	Attorney Docket Number	ACQI-010/10US 310578-2052

	1	Request for Inter Partes Reexamination of US Patent No. 7,099,981, Control No. 95/001,310, "Comments by Third Party Requester", filed April 8, 2011, total: 32 pgs.	☐
	2	Request for Inter Partes Reexamination of US Patent No. 7,146,446, Control No. 95/001,328, Comments by Third Party Requester", filed April 8, 2011, 23 pgs.	☐
	3	Request for Inter Partes Reexamination of US Patent No. 7,376,779, Control No. 95/001,475, Banankhah, Majid A., Art Unit 3992, Action Closing Prosecution, April 27, 2011, 209 pgs.	☐
	4	Request for Inter Partes Reexamination of US Patent No. 7,328,297, Control No. 95/001,336, "Supplemental Comments by Third Party Requester" filed May 12, 2011, 32 pgs.	☐
	5	Request for Ex Parte Reexamination of US Patent No. 6,216,185, Control No. 90/010,816, Banankhah, Majid A., Art Unit 3992, Nonfinal Office Action, June 14, 2011, 44 pgs.	☐
	6	Request for Inter Partes Reexamination of US Patent No. 7,376,779, Control No. 95/001,475, "Comments by Third Party Requestor", filed June 24, 2011, 24 pgs.	☐

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature	/Raymond Phan/	Date Considered	09/12/2011

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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BIB DATA SHEET

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12/504,534	07/16/2009	710	2111	ACQI-010/10US 310578-2052

APPLICANTS

William W. Y. Chu, Los Altos, CA;

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This application is a CON of 12/077,503 03/18/2008 PAT 7,676,624
which is a CON of 11/166,656 06/24/2005 PAT 7,376,779
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which claims benefit of 60/134,122 05/14/1999

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED **** ** SMALL ENTITY **
07/27/2009

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /Raymond Ngan Phan/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		CA	24	43	13

ADDRESS

COOLEY LLP
ATTN: Patent Group
Suite 1100
777 - 6th Street, NW
WASHINGTON, DC 20001
UNITED STATES

TITLE

MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNIDIRECTIONAL SERIAL BIT CHANNELS TO TRANSMIT ENCODED PERIPHERAL COMPONENT INTERCONNECT BUS TRANSACTION DATA

FILING FEE RECEIVED		
7340	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /R.P./

Please type a plus sign (+) inside this box → [+]

PTO/SB/08A (07-05)
Approved for use through 07/31/2006. OMB 0651-0031

Substitute for form 1449A/PTO		*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Application Number	12/504,534
		Filing Date	July 16, 2009
		First Named Inventor	William W.Y. Chu
(use as many sheets as necessary)		Group Art Unit	2111
		Examiner Name	Unassigned
Sheet	3 of 6	Attorney Docket No.	ACQI-010/10US 310578-2052

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	102.	US-6,643,777	11-04-2003	Chu	
	103.	US-6,718,415	04-06-2004	Chu	
	104.	US-6,725,317	04-20-2004	Bouchier et al.	
	105.	US-6,324,605 B1	11-27-2001	Rafferty et al.	
	106.	US-2009/0157939	06/18/2009	Chu	
	107.	US-5,978,919	11-1999	Doi et al.	
	108.	US-6,009,488	12-28-1999	Kavipurapu	
	109.	US-6,025,989	02-15-2000	Ayd et al.	
	110.	US-6,070,214	05-30-2000	Ahern	
	111.	US-7,099,981 B2	08-29-2006	Chu	
	112.	US-~~7,446,446~~ 7,146,446 B2	12-05-2006	Chu	
	113.	US-7,328,297 B2	02-05-2008	Chu	
	114.	US-7,363,415 B2	04-22-2008	Chu	
	115.	US-7,363,416 B2	04-22-2008	Chu	
	116.	US-7,376,779 B2	05-20-2008	Chu	
	117.	US-6,161,524	12-19-2000	Akbarian et al.	

Change(s) applied to document, /D.H.P./ 8/24/2011

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	1.	WO 92/18924	10-29-1992			
	2.	WO 94/00097	01-06-1994			
	3.	WO 95/13640	05-18-1995			
	4.	EP 722138A1	07-17-1996			
	5.	JP 6-289953	10-18-1994			

OTHER – NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[6]
	1.	Agerwala, T. et al., "SP2 System Architecture", IBM Systems Journal, Vol. 34, No. 2 (1995)	
	2.	Bernal, Carlos, product brochure entitled: "PowerSMP Series 4000", (March 1998) <<http://www/winnetmag.com/Windows/Article/ArticleID/3095//3095.html, downloaded from web on June 22, 2004, 2 pgs.	
	3.	Cragle, Jonathan, "Density System 1100", (May 1999) <<http://www.winnetmag.com/Windows/Article/ArtideID/5199/5199.html>>, downloaded from web on June 21, 2004, 4 pgs.	
	4.	Feldman, Jonathan, "Rack Steady: The Four Rack-Mounted Servers That Rocked Our Network", <<http://www.networkcomputing.com/shared/printArtide.jhtml?article=/910/910r3sidel .htm...>> June 23, 2004, 3 pgs.	
	5.	Fetters, Dave, "Cubix High-Density Server Leads the Way With Standout Management Software", (February 8. 1999) <<http://www. nwc. com/shared/printArticle.jhtml?article=/1003/1003r3full.html&pub=nwc>>, downloaded from web on June 23, 2004, 5 pgs.	
	6.	Gardner, Michael and Null, Christopher, "A Server Condominium", <<http://www.lantimes.com/testing/98jun/806a042a.html>>, June 23, 2004, 3 pgs.	
	7.	Harrison, Dave, "VME in the Military: The M1A2 Main Battle Tank Upgrade Relies on COTS VME"	

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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/504,534	10/18/2011	8041873	ACQI-010/10US 310578-2052	1286

58249 7590 09/28/2011

COOLEY LLP
ATTN: Patent Group
Suite 1100
777 - 6th Street, NW
WASHINGTON, DC 20001

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

William W. Y. Chu, Los Altos, CA;

AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
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In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Eastern District of Texas on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
13-cv-638	9/9/2013	Eastern District of Texas

PLAINTIFF	DEFENDANT
ACQIS LLC	Alcatel-Lucent USA, Inc., and Alcatel-Lucent S.A.

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	7,363,416	4/22/2008	ACQIS Technology, Inc.
2	7,676,624	3/9/2010	ACQIS LLC
3	7,818,487	10/19/2010	ACQIS LLC
4	8,041,873	10/18/2011	ACQIS LLC
5	RE 41,294	4/27/2010	ACQIS Technology, Inc.

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 RE 41,961	11/23/2010	ACQIS Technology, Inc.
2 RE 42,814	10/4/2011	ACQIS Technology, Inc.
3 RE 43,171	2/7/2012	ACQIS LLC
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director **Copy 3—Upon termination of action, mail this copy to Director**
Copy 2—Upon filing document adding patent(s), mail this copy to Director **Copy 4—Case file copy**

AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
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☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
6:13-cv-639	9/9/2013	Eastern District of Texas

PLAINTIFF	DEFENDANT
ACQIS LLC	EMC Corporation

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	7,363,416	4/22/2008	ACQIS Technology, Inc.
2	7,676,624	3/9/2010	ACQIS LLC
3	7,818,487	10/19/2010	ACQIS LLC
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☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
6:13-cv-640	9/9/2013	Eastern District of Texas

PLAINTIFF	DEFENDANT
ACQIS LLC	Ericsson, Inc., and Telefonaktiebolaget LM Ericsson

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	7,363,416	4/22/2008	ACQIS Technology, Inc.
2	7,818,487	10/19/2010	ACQIS LLC
3	8,041,873	10/18/2011	ACQIS LLC
4	RE 41,294	4/27/2010	ACQIS Technology, Inc.
5	RE 42,814	10/4/2011	ACQIS Technology, Inc.

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 RE 43,119	1/17/2012	ACQIS LLC
2 RE 43,171	2/7/2012	ACQIS LLC
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

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☑ Trademarks or ☐ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
2:13-cv-05866-RSWL	8/12/2013	for the Central District of California

PLAINTIFF	DEFENDANT
Moofly Productions, LLC	Sandra Favila, et al.

PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☑ Other Pleading	
8/12/2013		
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 77009913	9/28/2006	Registrant: Get Flipped!, Inc.
2 77061664	12/11/2006	Registrant: Get Flipped!, Inc.
3 77061670	12/6/2006	Registrant: Get Flipped!, Inc.
4 77579867	9/26/2008	Registrant: Get Flipped!, Inc.
5		

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Trials@uspto.gov
571–272–7822

Paper 61
Entered: March 8, 2016

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

EMC CORPORATION,
Petitioner,

v.

ACQIS LLC,
Patent Owner.

Case IPR2014-01462
Patent 8,041,873 B2

Before MICHAEL P. TIERNEY, MICHAEL J. FITZPATRICK, and ROBERT J. WEINSCHENK, *Administrative Patent Judges*.

WEINSCHENK, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

EMC Corporation ("Petitioner") filed a Corrected Petition (Paper 4, "Pet.") requesting an *inter partes* review of claims 54 and 56–61 of U.S. Patent No. 8,041,873 B2 (Ex. 1001, "the '873 patent"). ACQIS LLC ("Patent Owner") filed a Preliminary Response (Paper 11, "Prelim. Resp.") to the Petition. On March 11, 2015, we instituted an *inter partes* review of claims 54 and 56–61 ("the challenged claims") of the '873 patent on the following grounds:

Claim(s)	**Statutory Basis**	**Applied References(s)**
54, 57, 60, and 61	35 U.S.C. § 103(a)	Robert W. Horst, *TNet: A Reliable System Area Network* (Feb. 1995) (Ex. 1011, "Horst"); and National Semiconductor, *LVDS Owner's Manual: Design Guide* (Spring 1997) (Ex. 1019, "LVDS Owner's Manual")
56 and 59	35 U.S.C. § 103(a)	Horst; LVDS Owner's Manual; and U.S. Patent No. 5,428,806 (issued June 27, 1995) (Ex. 1016, "Pocrass")
58	35 U.S.C. § 103(a)	Horst; LVDS Owner's Manual; and U.S. Patent No. 5,227,957 (issued July 13, 1993) (Ex. 1017, "Deters")

Paper 14 ("Dec. on Inst."), 18.

After institution, Patent Owner filed a Response (Paper 30, "PO Resp.") to the Petition, Petitioner filed a Reply (Paper 42, "Pet. Reply") to the Response, and Patent Owner filed a Surreply (Paper 54, "PO Surreply").[1] An oral hearing was held on December 8, 2015, and a transcript of the hearing is included in the record. Paper 60 ("Tr.").

[1] We authorized Patent Owner to file a surreply. Paper 47, 3.

We issue this Final Written Decision pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons set forth below, Petitioner has not shown by a preponderance of the evidence that claims 54 and 56–61 of the '873 patent are unpatentable.

A. *Related Proceedings*

The parties indicate that the '873 patent is at issue in the following district court cases: *ACQIS LLC v. Alcatel-Lucent USA, Inc.*, No. 6:13-cv-00638 (E.D. Tex.); *ACQIS LLC v. EMC Corp.*, No. 6:13-cv-00639 (E.D. Tex.); *ACQIS LLC v. Ericsson, Inc.*, No. 6:13-cv-00640 (E.D. Tex.); and *ACQIS LLC v. Huawei Technologies Co.*, No. 6:13-cv-00641 (E.D. Tex.). Pet. 56–57; Paper 8, 2.

Petitioner identifies the following petitions for *inter partes* review as being related to this case (Pet. 57):

Case No.	**Involved U.S. Patent No.**
IPR2014-01452	RE43,171 E
IPR2014-01469	RE42,814 E

B. *The '873 Patent*

A typical computer system includes various components, such as a central processing unit ("CPU"), memory, and peripheral devices (e.g., a printer). Ex. 1001, col. 1, ll. 39–63; Ex. 2021 ¶ 44. These components often are connected to one another using buses. Ex. 1003 ¶¶ 25, 26; Ex. 2021 ¶¶ 44, 45. A bus can be parallel or serial. Ex. 1003 ¶¶ 25, 26; Ex. 2021 ¶¶ 55, 57. A parallel bus transmits all the bits in a word at one time. Ex. 1003 ¶ 25; Ex. 2021 ¶ 55. For example, to communicate a 32-bit word, a parallel bus would have 32 lines so that it can transmit all the bits in the 32-bit word at one time. Ex. 1003 ¶ 25; Ex. 2021 ¶ 55. A serial bus, on the other hand, does not transmit all the bits in a word at one time. Ex. 1003

¶¶ 26, 27; Ex. 2021 ¶ 57. For example, to communicate a 32-bit word, a serial bus would have fewer than 32 lines. Ex. 1003 ¶ 27; Ex. 2021 ¶ 57.

The '873 patent relates to, *inter alia*, interfacing two Peripheral Component Interconnect ("PCI") buses. Ex. 1001, col. 5, ll. 31–33, Fig. 6. According to the '873 patent, prior systems for interfacing two PCI buses used parallel connectors. *Id.* at col. 3, ll. 11–21, col. 3, ll. 48–54, Fig. 5. Parallel connectors, however, were bulky and expensive. *Id.* at col. 3, ll. 54–63. The '873 patent explains that the system disclosed therein overcomes these disadvantages by interfacing two PCI buses using a serial connector. *Id.* at col. 5, ll. 31–33, col. 18, ll. 42–47. Specifically, a PCI bus transaction is encoded so it can be communicated in serial form over a low voltage differential signal ("LVDS") channel, which is smaller, faster, consumes less power, and generates less noise than the parallel connectors used in prior systems. *Id.* at col. 3, ll. 63–67, col. 5, ll. 46–62, col. 16, ll. 55–58.

C. *Illustrative Claim*

Claim 54 is independent and is reproduced below.

> 54. A computer module insertable into a coupling site of a console for data communication, comprising:
>
> a main circuit board;
>
> a processing unit coupled to the main circuit board;
>
> a main memory coupled to the processing unit;
>
> a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels to transmit data in opposite directions for communicating an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction; and
>
> a peripheral bridge directly coupled to the processing unit, the peripheral bridge comprising an interface controller directly coupled to the LVDS channel.

Id. at col. 43, ll. 40–52.

II. ANALYSIS

A. *Claim Construction*

The claims of an unexpired patent are interpreted using the broadest reasonable interpretation in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b); *In re Cuozzo Speed Techs., LLC*, 793 F.3d 1268, 1278–79 (Fed. Cir. 2015), *cert. granted sub nom. Cuozzo Speed Techs., LLC v. Lee*, No. 15-446, 84 U.S.L.W. 3218 (Jan. 15, 2016). In applying that standard, claim terms generally are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the specification. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). An applicant may provide a different definition of the term in the specification with reasonable clarity, deliberateness, and precision. *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994). In the absence of such a definition, limitations are not to be read into the claims from the specification. *In re Van Geuns*, 988 F.2d 1181, 1184 (Fed. Cir. 1993).

1. *Peripheral Component Interconnect (PCI) Bus Transaction*

Petitioner proposes construing the claim term "Peripheral Component Interconnect (PCI) bus transaction" to mean "a data signal communication with an interconnected peripheral component." Pet. 14. Patent Owner agrees with the construction in the Decision on Institution that the claim term "Peripheral Component Interconnect (PCI) bus transaction" means "Peripheral Component Interconnect (PCI) industry standard bus transaction." PO Resp. 17–18. We see no reason now to deviate from the

construction in the Decision on Institution. The evidence indicates that the term "Peripheral Component Interconnect (PCI) bus transaction" refers to a particular industry standard, not just any communication with an interconnected peripheral component.

Industry literature and dictionaries use the proper noun "Peripheral Component Interconnect" and the abbreviation "PCI" to refer to a particular industry specification for a local bus. *See, e.g.*, Ex. 2001, 1; Ex. 2002, 6–7; Ex. 2003, 7–8. The challenged claims recite "Peripheral Component Interconnect" as a proper noun and abbreviate it as "PCI," indicating that the challenged claims use those terms consistent with the understood industry meaning. Ex. 1001, col. 43, ll. 48–49, col. 44, l. 6; *see Azure Networks, LLC v. CSR PLC*, 771 F.3d 1336, 1348 (Fed. Cir. 2014). The written description similarly uses the abbreviation "PCI" to refer to a particular industry standard, and uses the common noun "peripheral bus" to refer to a generic peripheral bus. *Compare* Ex. 1001, col. 5, ll. 31–33 ("The present invention . . . interface[s] two PCI or PCI-like buses"), *with id.* at col. 10, ll. 53–55 ("Additionally, the peripheral controller is coupled to a clock control logic, a configuration signal, and *a peripheral bus*.") (emphasis added).

Petitioner and Petitioner's declarant, Mr. Bruce Young, acknowledge that the term "Peripheral Component Interconnect (PCI)" refers to an industry standard. Ex. 1003 ¶ 58; Ex. 2006, 1, 3; Ex. 2031, 16:8–12. The evidence Petitioner identifies in support of its proposed construction is the claim construction order issued in *ACQIS LLC v. Appro International, Inc.*, No. 6:09-cv-00148 (E.D. Tex. Feb. 3, 2011). Pet. 13–15 (citing Ex. 1015). In that case, though, the parties did not appear to dispute that the term "Peripheral Component Interconnect (PCI)" refers to an industry standard.

See Ex. 1015, 7 ("The parties' primary dispute is whether the term is limited to the conventional, parallel PCI Local Bus, and, therefore excludes PCI Express bus architecture and bus transaction protocol."). Moreover, the district court subsequently reconsidered its construction and clarified that the term "PCI bus transaction" refers to a PCI industry standard bus transaction. Ex. 1030, 8–10.

Therefore, we construe the claim term "Peripheral Component Interconnect (PCI) bus transaction" to mean "Peripheral Component Interconnect (PCI) industry standard bus transaction," and we construe the claim term "PCI bus transaction" to mean "PCI industry standard bus transaction."

B. *Obviousness of Claims 54 and 56–61*

Petitioner argues that claims 54, 57, 60, and 61 would have been obvious over Horst and LVDS Owner's Manual; claims 56 and 59 would have been obvious over Horst, LVDS Owner's Manual, and Pocrass; and claim 58 would have been obvious over Horst, LVDS Owner's Manual, and Deters. Pet. 58–59. A claim is unpatentable as obvious under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) any objective indicia of non-obviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18

(1966). We have considered the parties' arguments and supporting evidence, and we determine that Petitioner has not shown by a preponderance of the evidence that claims 54 and 56–61 would have been obvious over the cited references.

1. *Overview of Horst*

Petitioner relies primarily on Horst as teaching the limitations of independent claim 54. *See* Pet. 30–34. Horst describes a new network called a TNet network, which is a "major departure from traditional I/O systems." Ex. 1011, 1. The TNet network "is not a direct replacement for any existing type of local area network or I/O bus," but, rather, "is a new interconnection layer." *Id.* Specifically, the TNet network allows hundreds of CPUs and I/O devices to communicate over TNet links using TNet transactions. *Id.* at 1, Figs. 2, 5. Figure 2 of Horst is reproduced below.

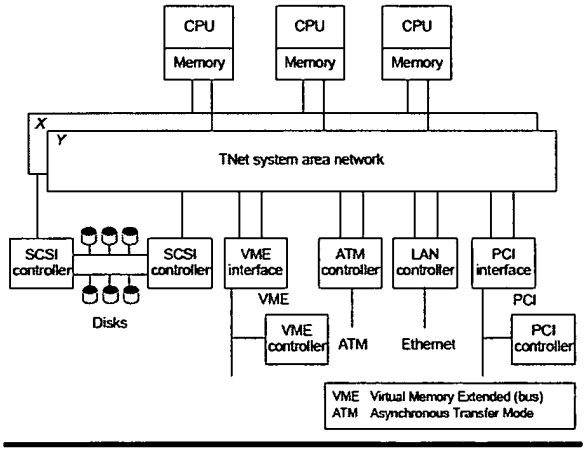


Figure 2. CPU cluster connected with the TNet system area network.

Id. at Fig. 2. Figure 2 of Horst shows a CPU cluster connected to the TNet network. *Id.*

Each CPU is connected to the TNet links by a TNet processor interface that translates a CPU transaction into a TNet transaction. *Id.* at 6 (describing "Processor interface"), Fig. 7; Ex. 2021 ¶ 103. Each I/O device

is connected to the TNet links by a TNet bus interface that translates a TNet transaction into a bus transaction for that I/O device. Ex. 1011, 7 (describing "Bus interface"), Fig. 8; Ex. 2021 ¶ 103. Figures 7 and 8 of Horst are reproduced below.

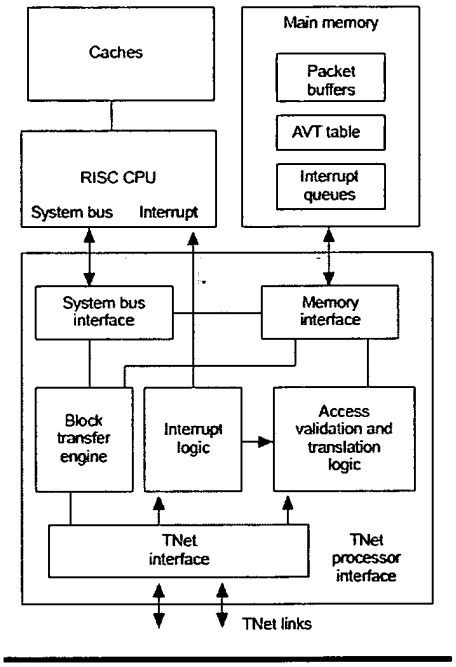


Figure 7. TNet processor interface.

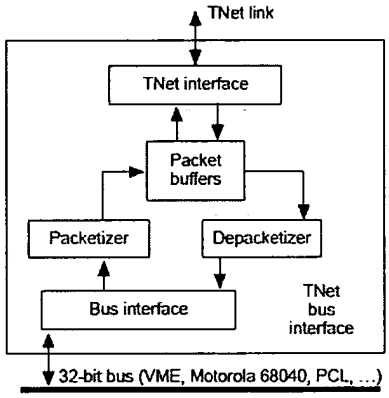


Figure 8. TNet bus interface.

Ex. 1011, Figs. 7, 8. Figure 7 of Horst shows a TNet processor interface, and Figure 8 of Horst shows a TNet bus interface. *Id.*

2. *Encoded Serial Bit Stream of Peripheral Component Interconnect (PCI) Bus Transaction*

As discussed above, the '873 patent explains that prior systems for interfacing two PCI buses used parallel connectors. Ex. 1001, col. 3, ll. 49–54. The '873 patent sought to overcome the disadvantages associated with using a parallel connector by encoding a PCI industry standard bus

transaction so that it can be communicated on a serial connector.[2] *Id.* at col. 3, ll. 63–67, col. 5, ll. 46–54, col. 16, ll. 55–58; Ex. 1003 ¶ 98. This feature is reflected in independent claim 54, which recites a "computer module" that comprises "a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels to transmit data in opposite directions for communicating an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction." Ex. 1001, col. 43, ll. 40–41, col. 43, ll. 45–49. Patent Owner argues that Petitioner has not shown sufficiently that communicating an encoded serial bit stream of a PCI industry standard bus transaction would have been obvious to a person of ordinary skill in the art. PO Resp. 27–36. For the reasons discussed below, we agree with Patent Owner.

a. *TNet processor interface*

In the Petition, Petitioner argues that the TNet processer interface in Horst outputs an encoded serial bit stream of a PCI bus transaction over the TNet links. Pet. 32. Petitioner's argument is not persuasive. The TNet processor interface in Horst translates a CPU transaction into a TNet transaction. Ex. 1011, 5 ("The interface to the destination CPU or I/O device provides mapping and validation hardware translating this virtual TNet address to the appropriate physical memory address."), Figs. 5, 7; Ex. 2021 ¶ 103 ("The TNet Processor Interface generates TNet transactions from CPU frontside bus transactions."). The TNet processor interface then encodes the TNet transaction using an 8B/9B encoder so that it can be output

[2] At the time of the '873 patent, a PCI industry standard bus transaction included a 32-bit address followed by one or more data phases. Ex. 2001, 25; Ex. 2021 ¶¶ 60, 63, 64.

over the 9-bit serial TNet links. Pet. 32; PO Resp. 38; Pet. Reply 7; Ex. 1003 ¶¶ 48, 128; Ex. 1011, 3, Figs. 3, 4 (showing "8B/9B encoder"), Table 1; Ex. 2021 ¶ 115. Petitioner does not identify persuasive evidence indicating that either the CPU transaction or the TNet transaction is a PCI industry standard bus transaction. Pet. 32 (citing Ex. 1011, 4, 5, 7, 8, Figs. 5, 8, 9, Table 1; Ex. 1003 ¶¶ 128, 131[54D]); Ex. 2021 ¶ 134. Thus, the evidence identified in the Petition does not indicate that the information output by the TNet processor interface over the TNet links is an encoded serial bit stream of a PCI industry standard bus transaction.

Petitioner points out that, *after* a TNet transaction is communicated over the TNet links, a TNet bus interface in the console may use information in the TNet transaction to create a PCI industry standard bus transaction if a particular I/O device is connected to a PCI bus. Pet. 32 (citing Ex. 1011, 7, Fig. 8). But claim 54 requires more than just communicating information over serial bit channels that subsequently might be used in the console to create a PCI industry standard bus transaction. Claim 54, when read in light of the specification, requires that the information actually communicated over the serial bit channels is a PCI industry standard bus transaction that has been encoded. Ex. 1001, col. 5, ll. 31–39, col. 16, ll. 53–60, col. 20, ll. 27–47, col. 43, ll. 45–49, Fig. 13; Ex. 2022, 15:12–16:2, 22:11–16. As discussed above, the evidence identified in the Petition does not indicate that the information output by the TNet processor interface over the TNet links is a PCI industry standard bus transaction that has been encoded.

In the Reply, Petitioner argues that the TNet transaction output by the TNet processor interface includes PCI data bits. Pet. Reply 10. Petitioner cites to certain portions of the deposition testimony of Patent Owner's

declarant, Dr. Volker Lindenstruth, as evidence that Patent Owner "does not dispute that PCI data bits are communicated over TNet links." *Id.* (citing Ex. 1029, 316:24–317:6). Petitioner's argument and evidence are not persuasive. We are not persuaded that the TNet transaction output by the TNet processor interface includes any data bits of a PCI industry standard bus transaction because Petitioner does not identify persuasive evidence indicating that any data bits of a PCI industry standard bus transaction exist in the CPU, memory, or TNet processor interface. *See* Pet. Reply 10. Further, the evidence identified by Petitioner is not an admission by Patent Owner that a TNet transaction includes PCI data bits. The cited deposition testimony of Dr. Lindenstruth relates to the teachings of a reference known as Bogaerts, not the teachings of Horst. Ex. 1029, 312:13–317:19. Even if the cited deposition testimony did relate to Horst, Dr. Lindenstruth simply acknowledges that "some data" is communicated, not that PCI data bits are communicated. *Id.* at 316:24–317:6.

Petitioner also argues in the Reply that the TNet transaction output by the TNet processor interface includes PCI address bits. Pet. Reply 10–12. Petitioner cites to the declaration testimony of its declarant, Mr. Young, as evidence that the TNet transaction includes PCI address bits. *Id.* (citing Ex. 1031 ¶¶ 32–37). Mr. Young states that a person of ordinary skill in the art would have known to place a 32-bit PCI address into the 32-bit TNet address portion of a TNet transaction or, alternatively, to use typical one-to-one mapping. Ex. 1031 ¶¶ 34, 36. Petitioner's argument and evidence are not persuasive. We are not persuaded that the TNet transaction output by the TNet processor interface includes any address bits of a PCI industry standard bus transaction because Petitioner does not identify persuasive evidence

indicating that any address bits of a PCI industry standard bus transaction exist in the CPU, memory, or TNet processor interface. *See* Pet. Reply 10–12; Ex. 1031 ¶¶ 32–37.

Further, the cited declaration testimony of Mr. Young is not persuasive because it is inconsistent with the express teachings of Horst. Horst teaches that a TNet transaction includes a TNet *virtual* address. Ex. 1011, 5 ("virtual TNet address"), Fig. 5; Ex. 2021 ¶¶ 104, 113. A PCI industry standard bus transaction, in contrast, includes a PCI *physical* address. Ex. 2001, 25; Ex. 2021 ¶¶ 60, 63–65, 113. Horst teaches that the physical address of a CPU or I/O device must be translated into a TNet virtual address. Ex. 1011, 5 ("The interface to the destination CPU or I/O device provides mapping and validation hardware translating this virtual TNet address to the appropriate physical memory address."). Thus, a PCI physical address cannot simply be placed into the TNet address portion of a TNet transaction. *Id.*; Ex. 2021 ¶¶ 113, 137, 138. Horst also teaches that typical one-to-one mapping is not used for TNet transactions. Ex. 1011, 5 ("Typically, I/O devices use one-to-one mapping, but because TNet node identifications differ for each I/O bus, each I/O node has its own independent 32-bit address space."); Ex. 2021 ¶ 112.

Petitioner also argues in the Reply that claim 54 "does not require that a complete PCI bus transaction originate in the computer module (or a complete PCI bus transaction exist at all)" because claim 54 only requires "two or more bits" of a PCI bus transaction. Pet. Reply 3, 5, 13, 14. Petitioner's argument is not persuasive. Claim 54, when read in light of the specification, requires communicating a PCI industry standard bus

transaction that has been encoded.[3] Ex. 1001, col. 5, ll. 31–39, col. 16, ll. 53–60, col. 20, ll. 27–47, col. 43, ll. 45–49, Fig. 13; Ex. 2022, 15:12–16:2, 22:11–16. Petitioner does not explain specifically how it would have been possible to communicate a PCI industry standard bus transaction that has been encoded if the PCI industry standard bus transaction never existed. *See* Pet. Reply 3, 5, 13, 14. Moreover, even if we adopted Petitioner's interpretation of claim 54, Petitioner's argument still is not persuasive. For the reasons discussed above, Petitioner does not identify persuasive evidence indicating that *any* bits of a PCI industry standard bus transaction exist in the CPU, memory, or TNet processor interface, or that *any* bits of a PCI industry standard bus transaction are included in the TNet transaction output by the TNet processor interface over the TNet links.

b. *TNet bus interface*

In the Reply, Petitioner argues that the TNet bus interface outputs an encoded serial bit stream of a PCI industry standard bus transaction over the TNet links. Pet. Reply 14–15 (citing Ex. 1011, 7; Ex. 1031 ¶¶ 44–46; Ex. 1026, 197:12–198:25, 199:16–201:24, 202:15–204:6, 214:15–215:10, 217:4–17). Specifically, Petitioner argues that "the PCI device creates a PCI bus transaction, which is then serialized to be communicated over the TNet channel." Pet. Reply 15. Petitioner's argument and evidence are not persuasive. Claim 54 recites "*two sets of* unidirectional, multiple *serial bit channels* to transmit data in opposite directions *for communicating* an

[3] Petitioner's claim differentiation argument (*see* Pet. Reply 5) cannot broaden claim 54 beyond its correct scope, as determined in light of the specification. *Seachange Int'l, Inc. v. C-COR Inc.*, 413 F.3d 1361, 1369 (Fed. Cir. 2005).

encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction." Ex. 1001, col. 43, ll. 45–49 (emphasis added). Thus, claim 54 requires two sets of serial bit channels for communicating an encoded serial bit stream of a PCI industry standard bus transaction. *Id.* at col. 21, ll. 32–67, col. 43, ll. 45–49, Figs. 9, 13, 15. Even if the TNet bus interface communicates an encoded serial bit stream of a PCI industry standard bus transaction over one set of TNet links in one direction, Petitioner still has not shown sufficiently that the TNet processor interface communicates an encoded serial bit stream of a PCI industry standard bus transaction over a second set of TNet links in the opposite direction.[4]

For the reasons discussed above, we determine that Petitioner has not shown by a preponderance of the evidence that claim 54 would have been obvious over Horst and LVDS Owner's Manual. Because claims 56–61 depend from claim 54, we also determine that Petitioner has not shown by a preponderance of the evidence that claims 56–61 would have been obvious over the cited references.

C. *Patent Owner's Motion to Exclude*

Patent Owner filed a Motion to Exclude (Paper 52, "PO Mot."), to which Petitioner filed an Opposition (Paper 55), and Patent Owner filed a Reply (Paper 57). Patent Owner argues that Exhibits 1027 and 1033–1036,

[4] In addition, Horst teaches that the TNet bus interface translates an I/O bus transaction, such as a PCI bus transaction, into a TNet transaction *before* the transaction is encoded for serial communication over the TNet links. Ex. 1011, 3, 7, Fig 4 (showing TNet packet data as an input to the 8B/9B encoder); Ex. 2021 ¶ 115. As a result, the TNet bus interface outputs a TNet transaction that has been encoded, not a PCI industry standard bus transaction that has been encoded. Ex. 2021 ¶¶ 111, 115.

and portions of Exhibit 1031 should be excluded. PO Mot. 1, 8. We have considered the parties' arguments, and, for the reasons discussed below, Patent Owner's Motion to Exclude is *denied-in-part* and *dismissed-in-part*.

1. *Exhibit 1027*

Exhibit 1027 is a document entitled "SCI implementation study for LHCb Data Acquisition." Patent Owner argues that Exhibit 1027 should be excluded as irrelevant because it relates to an asserted ground of unpatentability for which we did not institute an *inter partes* review in this case. PO Mot. 8. Patent Owner's Motion to Exclude Exhibit 1027 is *dismissed as moot* because this Decision does not rely on Exhibit 1027.

2. *Exhibit 1031*

Exhibit 1031 is the Reply Declaration of Mr. Bruce Young. Patent Owner argues that paragraphs 10–24 and 31–37 of Exhibit 1031 should be excluded as irrelevant and prejudicial because Petitioner relies on those paragraphs to support improper arguments in the Reply. PO Mot. 8. Petitioner argues in the Reply that the TNet transaction in Horst includes PCI address bits, and that claim 54 only requires communicating two bits of a PCI bus transaction. PO Mot. 1. Patent Owner contends that both arguments exceed the scope of a proper reply, as set forth in 37 C.F.R. § 42.23(b), and that the portions of Exhibit 1031 that Petitioner relies upon to support those arguments should be excluded as irrelevant and prejudicial. PO Mot. 2–4, 6, 7. Patent Owner's argument is not persuasive.

Patent Owner argues in the Response that the TNet transaction in Horst does not include PCI address bits. PO Resp. 27–29. As such, Petitioner's argument in the Reply that the TNet transaction includes PCI address bits is responsive to an argument raised in the Response. *See* 37

C.F.R. § 42.23(b) (generally permitting a reply to respond to arguments raised in a response). Patent Owner also argues in the Response that claim 54 requires communicating a 32-bit PCI address. PO Resp. 8–11. As such, Petitioner's argument in the Reply that claim 54 only requires communicating two bits of a PCI bus transaction is responsive to an argument raised in the Response. Because we are not persuaded that the identified arguments in the Reply are improper, the premise of Patent Owner's Motion to Exclude Exhibit 1031 fails. Therefore, Patent Owner's Motion to Exclude paragraphs 10–24 and 31–37 of Exhibit 1031 is *denied.*

3. *Exhibits 1033–1036*

Exhibit 1033 is a Decision on Appeal by the Board in Appeal No. 2013-007833, Exhibit 1034 is a Decision on Request for Rehearing by the Board in Appeal No. 2013-007833, Exhibit 1035 is a document entitled "The IEEE 1394 Bus," and Exhibit 1036 is a document entitled "1999 IEEE Nuclear Science Symposium Conference Record." Patent Owner argues that Exhibits 1033–1036 should be excluded as irrelevant and prejudicial because Petitioner relies on Exhibits 1033–1036 to support improper arguments in the Reply. PO Mot. 8–9. Because Patent Owner does not explain specifically why the arguments in the Reply that rely upon Exhibits 1033–1036 are improper, the premise of Patent Owner's Motion to Exclude Exhibits 1033–1036 fails. *Id.* To the extent Patent Owner relies on the same arguments discussed above with respect to Exhibit 1031, the premise of Patent Owner's Motion to Exclude Exhibits 1033–1036 fails for the reasons discussed above. *See supra* Section II.C.2. Therefore, Patent Owner's Motion to Exclude Exhibits 1033–1036 is *denied.*

D. *Patent Owner's Motion for Observations*

Patent Owner filed a Motion for Observations on the cross examination of Mr. Bruce Young (Paper 51), to which Petitioner filed a Response (Paper 56). We have considered Patent Owner's observations and Petitioner's responses, and we have given Mr. Young's testimony the appropriate weight in making our determination in this case.

III. CONCLUSION

Petitioner has not shown by a preponderance of the evidence that claims 54 and 56–61 of the '873 patent are unpatentable.

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that claims 54 and 56–61 of the '873 patent are not shown unpatentable;

FURTHER ORDERED that Patent Owner's Motion to Exclude is *denied-in-part* and *dismissed-in-part*; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

PETITIONER:

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

EMC CORPORATION
Petitioner

v.

ACQIS LLC
Patent Owner

IPR2014-01462

U.S. Patent No. 8,041,873

PETITIONER'S NOTICE OF APPEAL

Director of the United States Patent and Trademark Office
c/o Office of the General Counsel
P.O. Box 1450
Alexandria, VA 22313-1450

Pursuant to 35 U.S.C. §§ 141 and 142 and 37 C.F.R. § 90.2(a), Petitioner EMC Corporation hereby provides notice that it appeals to the United States Court of Appeals for the Federal Circuit from the Final Written Decision of the Patent Trial and Appeal Board ("Board") entered March 8, 2016 (Paper 61), and from all underlying findings, orders, decisions, rulings, and opinions, including, without limitation, the Decision, Institution of *Inter Partes* Review entered March 11, 2015 (Paper 14).

In accordance with 37 C.F.R. § 90.2(a)(3)(ii), Petitioner states that the issues for appeal include, but are not limited to: the Board's determination that claims 54 and 56-61 of U.S. Patent No. 8,041,873 have not been shown to be unpatentable; the Board's construction and interpretation of those claims; the Board's consideration of the expert testimony, prior art, and other evidence in the record; the Board's determinations in the Decision, Institution of *Inter Partes* Review; and the Board's factual findings, conclusions of law, or other determinations supporting or relating to the above issues.

Pursuant to 35 U.S.C. § 142 and 37 C.F.R. § 90.2(a), this Notice is being filed with the Director of the United States Patent and Trademark Office. Simultaneous with this submission, a copy of this Notice is being filed with the Patent Trial and Appeal Board. In addition, a copy of this Notice, along with the

required docketing fees, is being filed with the Clerk's Office for the United States Court of Appeals for the Federal Circuit.

Respectfully submitted,

DATED: April 11, 2016

By: */s/ Brian M. Buroker*

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Attorneys for Petitioner EMC Corporation

CERTIFICATE OF SERVICE

The undersigned certifies that, in addition to being filed electronically through the Patent Trial and Appeal Board's PRPS, the foregoing Notice of Appeal was filed by Express Mail on April 11, 2016, with the Director of the United States Patent and Trademark Office, at the following address:

Director of the United States Patent and Trademark Office
c/o Office of the General Counsel
P.O. Box 1450
Alexandria, VA 22313-1450

The undersigned certifies that a copy of the foregoing Notice of Appeal, along with the required docket fee, was filed on April 11, 2016, with the Clerk's Office of the United States Court of Appeals for the Federal Circuit through the Court's CM/ECF filing system.

The undersigned certifies service pursuant to 37 C.F.R. § 42.6(e) of a copy of this Notice of Appeal by electronic mail on April 11, 2016, on the counsel of record of the Patent Owner:

Wayne Stacy, wstacy@cooley.com, ACQIS-IPR@cooley.com

Britton Davis, bdavis@cooley.com

Joseph Drayton, jdrayton@cooley.com

DATED: April 11, 2016

By: /s/ *Brian M. Buroker*
Brian M. Buroker (Reg. No. 39,125)
Attorney for Petitioner EMC Corporation

NOTE: This order is nonprecedential.

United States Court of Appeals for the Federal Circuit

EMC CORPORATION,
Appellant

v.

ACQIS LLC,
Appellee

2016-1827, 2016-1828

Appeals from the United States Patent and Trademark Office, Patent Trial and Appeal Board in Nos. IPR2014-01462, IPR2014-01469.

ON MOTION

PER CURIAM.

O R D E R

The parties having so agreed, it is

ORDERED that the proceeding is DISMISSED under Fed. R. App. P. 42 (b). Each side shall bear its own costs.

FOR THE COURT

March 30, 2017
Date

/s/ Peter R. Marksteiner
Peter R. Marksteiner
Clerk of Court

ISSUED AS A MANDATE: March 30, 2017

NOTE: This order is nonprecedential.

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Peter R. Marksteiner
Clerk of Court

ISSUED AS A MANDATE: March 30, 2017

(12) **INTER PARTES REVIEW CERTIFICATE** (904th)
United States Patent
Chu

(10) **Number: US 8,041,873 K1**
(45) **Certificate Issued: Feb. 23, 2018**

(54) **MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNIDIRECTIONAL SERIAL BIT CHANNELS TO TRANSMIT ENCODED PERIPHERAL COMPONENT INTERCONNECT BUS TRANSACTION DATA**

(75) Inventor: **William W. Y. Chu**

(73) Assignee: **ACQIS LLC**

Trial Number:

IPR2014-01462 filed Sep. 10, 2014

Inter Partes Review Certificate for:

Patent No.: **8,041,873**
Issued: **Oct. 18, 2011**
Appl. No.: **12/504,534**
Filed: **Jul. 16, 2009**

The results of IPR2014-01462 are reflected in this inter partes review certificate under 35 U.S.C. 318(b).

AS A RESULT OF THE INTER PARTES REVIEW PROCEEDING, IT HAS BEEN DETERMINED THAT:

Claims **54** and **56-61** are found patentable.

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