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Paper 135
Entered: May 12, 2023

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
OPENSKY INDUSTRIES, LLC,
Petitioner,[*]

v.

VLSI TECHNOLOGY LLC,
Patent Owner.

IPR2021-01064
Patent 7,725,759 B2

Before THOMAS L. GIANNETTI, BRIAN J. MCNAMARA, and JASON W. MELVIN, *Administrative Patent Judges*.

MELVIN, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)
Denying Patent Owner's Motion to Exclude
37 C.F.R. § 42.64

[*] Intel Corporation, which filed a petition in IPR2022-00366, has been joined as a party to this proceeding. Paper 43.

I. INTRODUCTION

OpenSky Industries, LLC filed a Petition (Paper 2, "Pet.") requesting institution of *inter partes* review of claims 1, 14, 17, 18, 21, 22, and 24 ("the challenged claims") of U.S. Patent No. 7,725,759 B2 (Ex. 1001, "the '759 patent"), owned by VLSI Technology LLC ("Patent Owner").

After preliminary briefing, we instituted review. Paper 17 ("Institution Decision" or "Inst."). Following institution, Intel Corporation filed a petition for *inter partes* review and a Motion for Joinder in IPR2022-00366, requesting that Intel be joined as a petitioner to this proceeding. IPR2022-00366, Papers 3, 4. We instituted trial in IPR2022-00366, granted the Motion for Joinder, and added Intel as a petitioner here. *Id.*, Paper 14. A copy of that decision was entered into the record of this proceeding. Paper 43. Thus, OpenSky and Intel are, collectively, "Petitioner" here.

Patent Owner filed a Response (Paper 40 ("PO Resp.")), Petitioner filed a Reply (Paper 49 ("Pet. Reply")), and Patent Owner filed a Sur-Reply (Paper 85 ("PO Sur-Reply")). We held oral argument on September 22, 2022. Paper 105 ("Tr.").

Additionally, Patent Owner filed a Motion to Exclude two expert declarations filed by Petitioner. Paper 88 ("PO Mtn. Exclude"). Petitioner Opposed (Paper 94) and Patent Owner replied (Paper 95).

We have jurisdiction under 35 U.S.C. § 6(b). This is a Final Written Decision under 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons set forth below, we find Petitioner has demonstrated by a preponderance of evidence that the challenged claims are unpatentable. We deny Patent Owner's Motion to Exclude.

A. Related Matters

The parties both identify the following matter related to the '759 patent: *VLSI Technology LLC v. Intel Corporation*, No. 6:19-cv-00254-ADA (consolidated as 1:19-cv-00977) (W.D. Tex.) (trial concluded with jury verdict). Pet. 5; Paper 5. Patent Owner identifies the following additional matters: *VLSI Tech. LLC v. Intel Corp.*, No. 6:21-cv-00057 (W.D. Tex.); *VLSI Tech. LLC v. Intel Corp.*, No. 6:21-cv-00299 (W.D. Tex.); *Intel Corp. v. VLSI Tech. LLC*, IPR2020-00498 (PTAB) (on appeal to Federal Circuit, No. 21-1617); *Intel Corp. v. CLSI Tech. LLC*, IPR2020-00106 (PTAB) (on appeal to Federal Circuit, No. 21-1614). Paper 5.

B. Real Parties in Interest

Petitioner OpenSky identifies only itself as the real party in interest. Pet. 5. Petitioner Intel identifies only itself as the real party in interest. *See* Paper 42, 4. Patent Owner identifies VLSI Technology LLC and CF VLSI Holdings LLC as real parties in interest. Paper 5.

C. The '759 Patent

The '759 patent is titled "System and Method of Managing Clock Speed in an Electronic Device." Ex. 1001, code (54). It describes a method of monitoring a plurality of master devices coupled to a bus, receiving an input from a master device that is a request to increase the bus clock frequency, and increasing the bus clock frequency in response to the request. *Id.*, code (57). The '759 patent's Figure 1 is reproduced below:

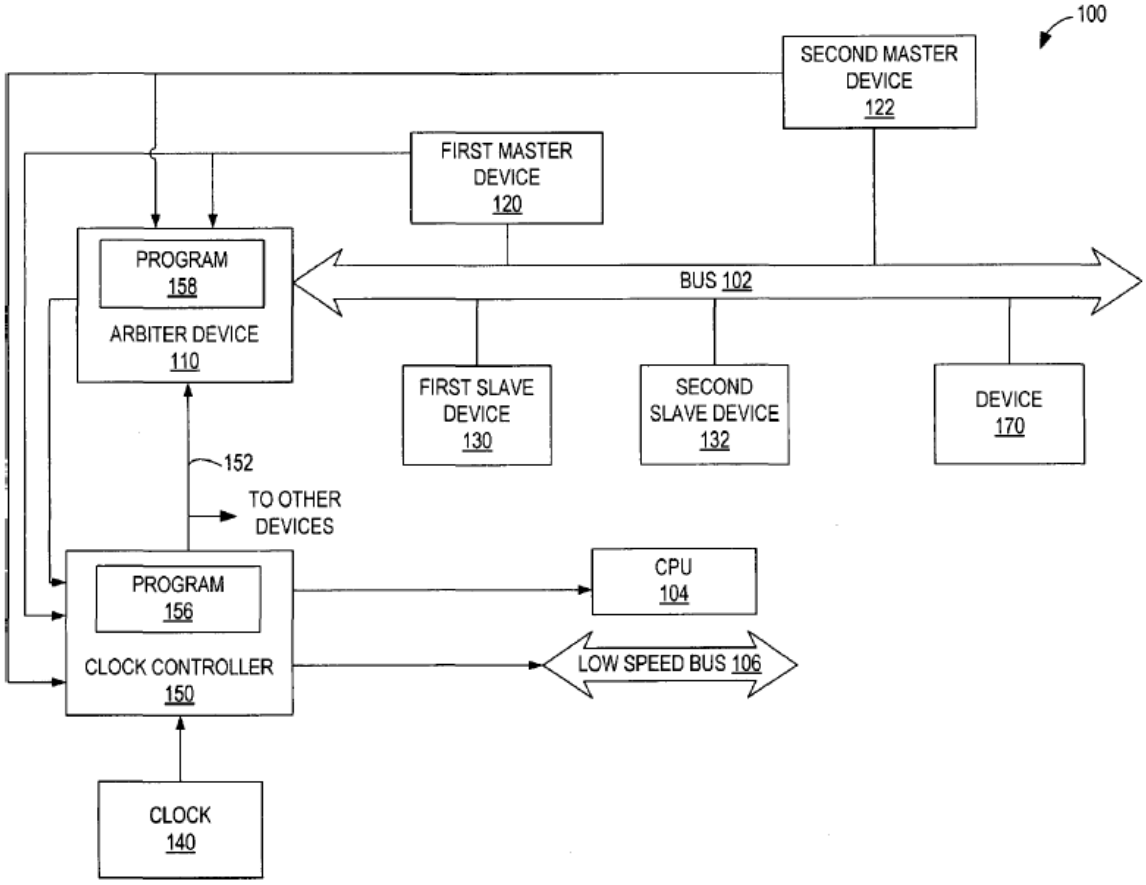

FIG. 1

Figure 1 is a block diagram depicting electronic system 100 with first master device 120 and second master device 122 coupled to bus 102, which is also coupled to arbiter 110. *Id.* at 2:58–3:3. Clock controller 150 is coupled to arbiter 110, clock 140, CPU 104, first master device 120, and second master device 122. *Id.* at 3:3–10.

The '759 patent describes that, in an illustrative embodiment, "clock controller 150 can output a high speed clock 152 having a variable clock frequency to the bus 102 via the arbiter 110 and another high speed clock output to the CPU 104." *Id.* at 3:32–35. Bus devices may generate trigger outputs indicating a request to change the high-speed clock frequency. *Id.* at 3:64–4:17. Then, "clock controller 150 controls and/or adjusts the high

speed clock 152 by changing the clock frequency in response to the plurality of trigger signal inputs." *Id.* at 4:22–24. The '759 patent also describes that, "[i]n a particular embodiment, the clock controller 150 may determine that a change in the high speed clock 152 may not be desired" and, would therefore not change the clock frequency. *Id.* at 4:58–62.

D. CHALLENGED CLAIMS

Challenged claim 1 is reproduced below:

1. A method, comprising:

monitoring a plurality of master devices coupled to a bus;

receiving a request, from a first master device of the plurality of master devices, to change a clock frequency of a high-speed clock, the request sent from the first master device in response to a predefined change in performance of the first master device, wherein the predefined change in performance is due to loading of the first master device as measured within a predefined time interval; and

in response to receiving the request from the first master device:

providing the clock frequency of the high-speed clock as an output to control a clock frequency of a second master device coupled to the bus; and

providing the clock frequency of the high-speed clock as an output to control a clock frequency of the bus.

Ex. 1001, 7:66–8:15. Claims 14 and 18 are independent and recite limitations similar to claim 1. *Id.* at 8:50–9:4, 9:19–40. Each of the other challenged claims depends from one of the independent claims.

E. PRIOR ART AND ASSERTED GROUNDS

Petitioner asserts the following grounds of unpatentability:

Claim(s) Challenged	35 U.S.C. §	References/Basis
1, 14, 17	103	Shaffer[1], Lint[2]
18, 21, 22, 24	103	Shaffer, Lint, Kiriake[3]
1, 14, 17	103	Chen[4], Terrell[5]
18, 21, 22, 24	103	Chen, Terrell, Kiriake

Pet. 7. Petitioner relies also on the Declarations of Dr. Bruce Jacob. Exs. 1002, 1046, 1055.

II. ANALYSIS

A. CLAIM CONSTRUCTION

1. "request"

Petitioner proposes that we apply the plain and ordinary meaning to each term of the claims. Pet. 17. According to Patent Owner "[t]he plain meaning of 'request' is to ask for something." PO Resp. 4. Patent Owner submits that Shaffer does not disclose the claimed "request" because a "request" does not encompass a command that mandates action, whereas Shaffer acts on the identified signals without assessment. *Id.* at 4–5, 9–14. Petitioner asserts that "nothing in the challenged claims excludes the scenario in which requests must be followed." Reply 5. Thus, we consider

[1] US 6,298,448 B1, issued Oct. 2, 2001 (Ex. 1005).
[2] US 7,360,103 B2, issued Apr. 15, 2008 (Ex. 1006).
[3] US 2003/0159080 A1, published Aug. 21, 2003 (Ex. 1028).
[4] US 5,838,995, issued Nov. 17, 1998 (Ex. 1003).
[5] US 2004/0098631 A1, published May 20, 2004 (Ex. 1004).

whether "request" implies a negative limitation that excludes a signal, e.g., a command or instruction, acted upon without assessment.

According to Patent Owner, the specification of the '759 patent, supports its claim construction because "the decision-making for frequency control resides in the PCC, *not* the master device."[6] PO Resp. 4; *accord id.* at 9 ("[T]he PCC has an embedded computer program with instructions 156 that decides whether to grant or ignore the request." (citing Ex. 1001, 3:3–6, 5:4–15)). Despite that position, which could be viewed as addressing a capability of the PCC itself rather than the request received by the PCC, Patent Owner asks us to construe "request" as excluding a command. *See* Tr. 50:16–18. Indeed, in distinguishing its claims over Shaffer based on a "request," Patent Owner does not address apparatus claims 14 and 18 separately from method claim 1, although the apparatus claims both recite a "programmable clock controller" that receives a request, whereas method claim 1 does not. *See* PO Resp. 4–14. Thus, we consider whether "request" excludes a signal that is acted on without assessment.

Claim 1 does not include a limitation that requires assessing whether to act on an incoming request. Claim 1 merely recites "receiving a request" from a first master device and, "in response to receiving the request," providing the clock frequency to control a second master device's clock frequency and the bus's clock frequency. Claim 1's language recites only that the claimed outputs are provided "in response to receiving the

[6] "PCC" refers to programmable clock controller, a term in claim 14 and the specification. *See* Ex. 1001, 2:41–50, 5:4–21, 8:59–61.

request"—claim 1 does not require an intervening assessment of any kind be performed.[7]

Patent Owner relies heavily on the specification to argue that the '759 patent's described "PCC need not grant 'requests.'" PO Resp. 11. The specification describes a PCC that receives a request and independently assesses whether to act on the request. Ex. 1001, 5:55–56 ("Moving to decision step 204, the controller determines whether to enable the request to increase the bus speed."). But the specification indicates that this approach is "[i]n a particular embodiment." *Id.* at 5:48–49. It also describes alternative embodiments in which a controller determines whether to set flags indicating high-frequency operation and then increases clock frequency if flags are set. *See id.* at 6:1–7:14.

We do not read the specification's disclosure of alternative embodiments as establishing that the claimed "request" mandates deciding whether to act on the request. Nothing in the specification describes a request that itself requires independent assessment. Stated otherwise, although any given "request" could be evaluated to determine what, if any, action to take in response, any such evaluation does not depend on the nature of the request. The claims do not include language restricting how a request is processed, but instead read on systems or methods in which a certain

[7] As noted, Patent Owner hinges its arguments on construing "request." *See* Tr. 50:16–18. Independent claim 14's programmable clock controller includes instructions to perform a method that, like claim 1's method, receives the request provided by the first master device and provides the claimed outputs without reciting any intervening assessment of the request. Independent claim 18 similarly recites that a clock controller coupled to an arbiter is configured to adjust a variable clock frequency of the bus in response to receiving the request from the first master device, without reciting any intervening assessment of the request.

action is taken in response to a request. At least one example disclosed in the specification is consistent with a system that makes no independent assessment of a request. The example states that "[t]he clock controller can output a variable clock frequency that varies in response to one or more inputs from the at least one master device." *Id.* at 2:38–40. This exemplary embodiment supports Petitioner's contention that we should not construe "request" as requiring independent assessment before acting on the request.

The prosecution history further supports an understanding of the claimed "request" as not requiring assessment before acting. Original application claim 1 recited "receiving an input . . . wherein the input is to request an increase to the clock frequency." Ex. 1010, 18.[8] Original application claim 2, which depended from original application claim 1, recited "determining whether to enable the request to increase the clock frequency of the bus." Ex. 1010, 18 (original claim 2). Thus, the application for the '759 patent included claims that differentiated between requesting an increase in clock frequency with no further assessment of the request (e.g., original application claim 1) and claims that required determining whether to enable the request (e.g., original application claim 2). During prosecution, original application claim 2 and others reciting "determining" steps in connection with a request were cancelled. *See id.* at 18–20; Ex. 1019, 5 (canceling claims 1–29). Accordingly, the prosecution history shows that the applicant intentionally cancelled claims limited to determining whether a request to change the clock frequency should be enabled, i.e., the applicant

[8] Unless noted otherwise, our citations refer to the exhibit's page number, rather than the page numbers of the original documents in the exhibit.

understood the possibility of claiming the distinction now sought, but decided not to limit the claims in that manner.

Finally, Petitioner points out prior art that uses the terms "command," "instruction," and "request" synonymously, suggesting that "request" did not carry the special meaning for which Patent Owner now argues. *See* Pet. Reply 7 (citing Ex. 1055, ¶¶29–32; Ex. 1006, 3:16–17 ("the OS makes a request to set the P-state"), 4:40–44, 5:47–49 ("when the OS specifies a first P-state via SET_PSTATE command"), 9:16–20 ("the OS communicates with the processor to instruct … the new P-state")).

Based on the claim language, the examples in the specification, and the prosecution history, we decline to infer the additional limitation on the term "request" as urged by Patent Owner. Accordingly, we find that the intrinsic evidence supports a construction of "request" that does not require assessing the request before acting in response to the request. We further find that such a construction is consistent with Petitioner's extrinsic evidence of typical usage of the term in the relevant art, i.e. that the challenged claims do not expressly require a determination before acting on the request.

Considering the record as a whole, we conclude that the claims do not require assessing whether to act on a request.

2. "master device"

According to Patent Owner, "[w]hile offering no construction of 'master device,' Petitioner argues that Shaffer's controllers are 'master devices' because they 'could initiate communications like those of the '759 patent.'" PO Resp. 19 (citing Pet. 23); *see* Pet. Reply 11. Patent Owner

submits that "master devices can make clock frequency change requests, while [the '759 patent's] slave devices cannot." PO Resp. 23.

Method claim 1 recites "receiving a request, from a first master device of the plurality of master devices, to change a clock frequency" and, in response to receiving that request, "providing the clock frequency . . . as an output to control a clock frequency of a second master device coupled to the bus." Thus, the claim language requires only that the first master device be able to request clock-frequency changes. The only feature of a master device recited in independent claims 1, 14, and 18 is that a first master device sends a request to change the clock frequency in response to a predefined change in its performance caused by loading during a predetermined interval. *See, e.g.,* Ex. 1001, 8:1–8. The claims do not otherwise limit a master device. None of the claims recites a "slave" device.

The specification describes an embodiment in which two master devices are each coupled to a bus, a clock controller, and an arbiter. Ex. 1001, 2:66–3:5, 3:8–10, Fig. 1. The specification also states that "[t]he first master device 120 may initiate communication with the first slave device 130 by requesting an access token from the arbiter 110 to communicate over the bus 102." *Id.* at 3:12–15. The specification contrasts "slave" devices: "The first slave device 130 may receive data but may not initiate communication with a master." *Id.* at 3:15–17; *accord id.* at 3:17–19 ("That is, the first slave device 130 is disabled to initiate communication."). The patent thus distinguishes "master" from "slave" devices based on the ability to initiate bus communication.

The specification also discloses an embodiment in which "[e]ach of the plurality of devices coupled to the bus 102 provide[s] a corresponding trigger output" where "the trigger output is indicative of a request to change

the clock frequency of the high speed clock 152." *Id.* at 3:64–65, 4:15–17 ("[t]he generation of the trigger output is indicative of a request to change the clock frequency of the high speed clock 152"). That functionality—using trigger outputs to request speed changes—is agnostic as to whether a device is a "master" or "slave" device. Stated otherwise, although the particular embodiment describes master devices that can request frequency changes, the slave devices can also request frequency changes because the specification states that "each" device provides a trigger output. Thus, the specification does not support Patent Owner's assertion that the ability to request clock speed changes distinguishes "master devices" from "slave devices."

We construe master devices as those devices that can initiate communications with other devices but need not be able to send requests to a clock module.

3. "clock frequency of a second master device"

Contesting whether Chen discloses providing an "output to control a clock frequency of a second master device coupled to the bus," Patent Owner asserts that "the separate clock frequency of the second master device in the claims refers to the internal clock frequency of the master device, not to an I/O bus frequency." PO Resp. 52. Petitioner replies that receiving a clock frequency for bus transactions satisfies the claim language, regardless of whether a device has a separate internal clock. Pet. Reply 21.

We agree with Petitioner that nothing in the claim language requires that "a clock frequency of a second master device" refer to the "internal clock frequency" of the second master device. *See* Pet. Reply 21 ("[I]t is irrelevant whether [Chen's master] devices could also have other clocks

within them."). Rather, the phrase "a clock frequency" is generic and does not limit whether the provided clock controls bus communications or another aspect of a second master device. Nor has Patent Owner directed us to the specification's disclosures that would limit the term beyond a specific embodiment. Patent Owner's reference to Dr. Conte's declaration (PO Resp. 52 (citing Ex. 2065 ¶ 186)), cites testimony that simply asserts that skilled artisans "would understand that the I/O bus clock in Chen has nothing to do with the internal clock of the I/O device." Ex. 2065 ¶ 186. This testimony does not address the proper understanding of "a clock frequency." On the other hand, Petitioner's expert, Dr. Jacob, discusses the claims' broad language. *See* Ex. 1055 ¶¶ 95–96.

We discuss Patent Owner's implicit claim construction in more detail below. *See infra* at 38 (§ II.D.2).

B. Obviousness over Shaffer and Lint (Claims 1, 14, and 17)

Shaffer discloses a CPU speed control system that provides "the CPU and other system buses in the device with a variable clocking frequency based on the application or interrupt being executed by the device." Ex. 1005, code (57). Shaffer's Figure 1 is reproduced below:

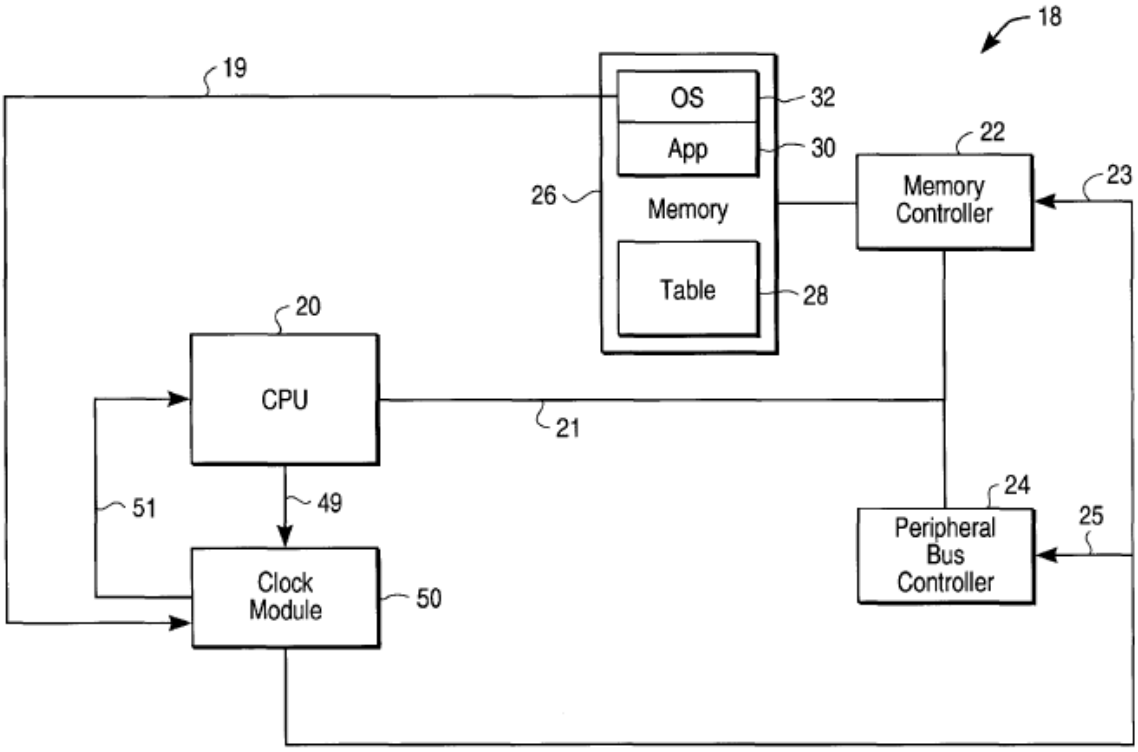

FIG. 1

Figure 1 is a block diagram showing intelligent programmable clock module 50 that provides CPU 20 with a clocking signal and informs CPU 20 of the frequency through line 51. *Id.* at 3:8–23. Additionally, clock module 50 supplies a clocking signal to memory controller 22 through memory clock control line 23 and to peripheral bus controller 24 (also referred to as system bus controller 24) through system bus clock control line 25. *Id.* at 4:26–29. Schaffer discloses that its speed control system "provide[s] a programmable variable clock frequency to the other controllers and buses in the system" such that "data and commands will travel through the data/command bus 21 at a proportionally slower speed" along with CPU 20 operating at the slower speed. *Id.* at 4:15–25.

Shaffer discloses "a multiprocessor system" in which "a single clock module 50 may drive all the processor clocks." *Id.* at 6:2–5. Petitioner

contends that each of the multiple CPUs in a multiprocessor system "are master devices, per the '759 patent." Pet. 23.

Shaffer discloses "a CPU utilization application that dynamically monitors the level of CPU usage." Ex. 1005, 4:53–54; *see id.* 4:50–5:20. That application provides CPU utilization values to the operating system, OS 32, which may then generate "an interrupt to the clock module 50 instructing it to raise or lower the clocking frequency provided to the CPU 20." *Id.* at 5:5–8.

Petitioner relies on Schaffer for most limitations of claim 1, further relying on Lint as teaching the limitation that a "predefined change in performance is due to loading of the first master device as measured within a predefined time interval." Pet. 22–31. Petitioner first asserts that Shaffer teaches this limitation by disclosing that "the CPU 20 operates at a lower speed when the OS 32 determines that no processing is occurring or has not occurred for a predetermined amount of time." *Id.* at 27 (quoting Ex. 1005, 4:6–8). Petitioner relies on Lint as an alternative to Shaffer's teachings in that regard, submitting that Lint discloses "changing the 'performance state . . . based in part on the data representing the average performance over the previous period of time.'" *Id.* (quoting Ex. 1006, 3:1–7). Petitioner reasons (1) that Shaffer describes a "CPU utilization percentage," (2) that Lint discloses a way of calculating the utilization percentage that would allow Shaffer's system "to better interface with processor chips featuring hardware coordination of [performance]-states" by saving power, and (3) that doing so would amount to nothing more than using a known technique to improve similar devices in the same way. *Id.* at 27–30 (citing Ex. 1006, 3:2–7, 2:33).

1. "request"

Petitioner identifies Shaffer's "instructions via lines 19 and 49" as requests from CPU 20 to change a clock frequency of clock module 50. Pet. 23–24 (citing Ex. 1005, 3:8–22 ("CPU 20 in turn can instruct through line 49 the clock module 50 to increase or decrease the output frequency as needed"), 4:50–54 ("OS 32 is used to control the frequency of the clock module 50 in response to a CPU utilization application that dynamically monitors the level of CPU usage.")). Patent Owner argues that Shaffer's instruction is not a "request" because "Shaffer's clock module may not reject these commands; it simply does as it's told." PO Resp. 5–14. As discussed above, however, we do not construe "request" as requiring independent assessment of whether to act on the request. *See supra* at 6 (§ II.A.1). Accordingly, we find that Shaffer teaches a request as claimed.

2. "monitoring a plurality of master devices"

Petitioner asserts that Shaffer discloses "monitoring a plurality of master devices coupled to a bus" because CPU 20, memory controller 22, bus controller 24, and another CPU are coupled to data/command bus 21. Pet. 22 (citing Ex. 1005, Fig. 1, 6:2–5). As to "monitoring," Petitioner cites Shaffer's "CPU utilization application that dynamically monitors the level of CPU usage." Ex. 1005, 4:53–54. As to the memory and bus controllers, Petitioner asserts that skilled artisans "would have understood that Shaffer's 'controllers' could initiate communications, like those of the '759 patent." Pet. 23. Petitioner's expert, Dr. Jacob, testifies that CPU 20, memory controller 22, and peripheral bus controller 24 are master devices, as claimed, because "they are all on the system bus, a shared bus organization." Ex. 1055 ¶ 51; *see also id.* ¶ 46 (asserting that a shared bus supports multiple

masters and requires each to "make its own decisions about when and how to access the shared bus").

Patent Owner argues that Shaffer does not teach or suggest monitoring controllers 22 or 24. PO Resp. 15. According to Patent Owner, because those controllers have no ability to signal a speed change, "there would be no reason to monitor their utilization." *Id.* Additionally, Patent Owner reasons that those devices are much slower than CPU 20, because "the most cost effective method to reduce power consumption is to vary the CPU 20 clock speed." *Id.* (quoting Ex. 1005, 6:12–14). Petitioner replies that skilled artisans would have understood Shaffer's controllers 22 and 24 are monitored. Pet. Reply 9 (citing Ex. 1055 ¶¶ 104–107).

Shaffer discusses "monitoring" in several ways. First, Shaffer describes its clock module as responding to OS-generated signals and gives an example of an idle signal indicating whether the CPU is in an idle state. Ex. 1005, 3:27–59. Shaffer also discloses that the clock module may respond to interrupts indicating user activity like mouse movement or keyboard input. *Id.* at 3:60–4:14. Shaffer further describes that OS signals may be generated by "a CPU utilization application that dynamically monitors the level of CPU usage." *Id.* at 4:51–5:20. Finally, Shaffer describes controlling the clock frequency "in response to the particular application or task being executed by the system." *Id.* at 5:21–47. Dr. Jacob testifies that skilled artisans would have understood Shaffer to disclose monitoring its controllers along with the CPU, explaining that:

> monitoring software typically monitors all of a system's activity, including network traffic, memory traffic, disk traffic, etc. Shaffer's memory controller 22 and peripheral bus controller 24 would be monitored, even if the devices

> consumed little power themselves, because the data traffic through them could very well add up to a significant amount.

Ex. 1055 ¶ 106.

Considering the record as a whole, we are not persuaded that Shaffer discloses monitoring devices beyond CPUs. Although Dr. Jacob asserts that Shaffer's memory controller and peripheral bus controller "would be monitored," Shaffer discloses monitoring through interrupts and a "CPU utilization application," as described above. Petitioner does not explain, through Shaffer's disclosures or Dr. Jacob's testimony, how either a CPU utilization application or interrupt monitoring would include monitoring memory controller 22 or peripheral bus controller 24. Petitioner's assertion that "typical" monitoring software would have included network, memory, and disk traffic, even if true, is insufficient to show that Shaffer's monitoring is consistent with that assertion.

Petitioner, however, relies additionally on Shaffer's disclosure of a multiprocessor system. Pet. 23 ("Shaffer discloses multiple CPUs. These CPUs are master devices, per the '759 patent.") (citations omitted). Petitioner relies also on Shaffer's "CPU utilization application" as monitoring the CPUs. *Id.*

Patent Owner incorrectly asserts that the Petitioner relied "*solely* on Shaffer monitoring *single* CPU 20." PO Sur-Reply 11 (citing Pet. 22–23). The Petition states "[a] POSA would have found it obvious that other CPUs disclosed by Shaffer would have been coupled to the bus." Pet. 23 (citing Ex. 1002 ¶¶ 228–233). The Petition also identifies "another CPU" as one of the plurality of master devices and identifies Shaffer's "CPU utilization application" as monitoring the master devices. Pet. 22–23 (citing, e.g. Ex. 1005, 6:2–5 ("in a multiple processor system (not shown), a separate

clock module 50 may be used for each processor, or a single clock module may drive all the processor clocks").

Patent Owner asserts that "Shaffer does not teach monitoring multiple CPUs in its vague reference to a multi-CPU configuration." PO Sur-Reply 12; *accord* PO Resp. 15–16 ("Shaffer does not provide any details of how such a [multiprocessor] system would operate" and therefore "does not disclose monitoring each CPU in Shaffer's multiprocessor embodiment."). Patent Owner emphasizes Dr. Jacob's statement that "I don't really know what it would do" because Shaffer does not disclose its algorithm "in a multiprocessor scenario." PO Sur-Reply 12 (quoting Ex. 2066, 41:13–42:5). That statement, however, relates to the particular algorithm that Shaffer would apply to make clock-speed changes in a multiprocessor system. Ex. 2066, 41:25–42:1. The challenged claims are not directed to the particular algorithm that would be used in such a multiprocessor system, and therefore, Dr. Jacob's testimony cited by Patent Owner does not diminish Shaffer or Dr, Jacob's opinion that Shaffer's CPU monitoring would include multiple CPUs in a multiprocessor system. Ex. 1055 ¶¶ 105–106; *see also* Pet. Reply 9 (citing Ex. 2066, 89:5–10).

We are persuaded that Shaffer discloses monitoring "CPU utilization" including multiple CPUs in a multiprocessor system. Shaffer's disclosures are not limited to monitoring a single CPU, but rather consider "CPU utilization" generally. Ex. 1005, 4:51–54. Thus, in Shaffer's multiprocessor embodiment, an application that "dynamically monitors the level of CPU usage" would monitor multiple CPUs. This conclusion is further supported by Shaffer's claims, which recite a computer system comprising "one or more CPUs," "a CPU resource utilization monitor to determine the amount of CPU resources being used by the computer system," and "an intelligent

clock module to provide a variable operating frequency to said one or more CPUs." Ex. 1005, 8:10–26.

3. "control a clock frequency of a second master device"

Petitioner asserts that Shaffer discloses, in response to a request from CPU 20 executing OS 32, providing a signal from its clock module 50 to control a clock frequency of another CPU coupled to bus 21.[9] Pet. 30; Ex. 1005, 6:2–5 ("[A] single clock module 50 may drive all the processor clocks")).

Patent Owner asserts "Shaffer does not teach or suggest that CPU 20 would change the clock frequency of a second CPU." PO Resp. 17 (citing Ex. 2066, 39:12–19 (Dr. Jacob's testimony about Shaffer's disclosures with two clock modules)). We, however, base our conclusion on Shaffer's discussion of a *single* clock module, and Dr. Jacob's testimony about Shaffer's two-clock-module embodiment is inapposite. Patent Owner submits it would be "contrary to Shaffer's principle of operation and stated goal" to operate both CPUs at the same clock rate despite different utilizations. PO Resp. 17–18. We do not agree, as Shaffer discloses both CPUs operating with a single clock module. Moreover, we credit Dr. Jacob's testimony that symmetric multiprocessor arrangements, in which two processors share in running OS and application tasks, were more common at the time of the invention and more broadly applicable than the single instruction, multiple data (SIMD) arrangement cited by Patent Owner's expert, Dr. Conte, in which two processors perform the same task

[9] Because we determine above that Shaffer does not disclose monitoring its memory controller 22 or peripheral bus controller 24, we do not address Petitioner's further contentions that rely on those elements and focus instead on Shaffer's multiprocessor embodiment.

simultaneously. Ex. 1055 ¶¶ 56–57. Dr. Jacob testifies that SIMD architecture is "a very narrow type of accelerator architecture in computer design," and is "used in very specific application areas that can exploit such an arrangement (e.g., graphics processing and some high-performance computing)." Ex. 1055 ¶ 57.

Shaffer discloses speed-control systems for personal computers targeting, for example, savings when computers "are left on for extended periods of time, even when not being actively used." Ex. 1005, 1:15–28. Shaffer discloses that its invention is applicable to a broad range of "microprocessor-based devices and/or battery powered intelligent devices that need to conserve battery power, such as PCS, cellular phones, personal digital assistants (PDA), and battery backed-up systems like private branch exchange (PBXs) or medical equipment." *Id.* at 2:55–62. We therefore find Shaffer's disclosures are broadly applicable to multiple architectures, and are not limited to the particular processor arrangement that Dr. Conte proposes. In a multiprocessor system using a single clock module, as Shaffer discloses, the single clock frequency is provided to control the clock frequency of all CPUs (i.e., control a clock frequency of a second master device). *See* Pet. 23 (citing Ex. 1002 ¶ 232 ("As the system uses a shared-bus organization, a person of ordinary skill would understand that any additional CPUs, if present, would be attached to the system bus 21 in the same manner as CPU 20.")).

Shaffer's system operating as Petitioner describes would not be "contrary to Shaffer's principle of operation," as Patent Owner alleges, because Shaffer seeks "to ensure that the CPU is operating at the most power efficient level for *any* given task." Ex. 1005, 2:26–30 (emphasis added). Seeking optimum performance in Shaffer necessarily occurs within the

constraints of a hardware system, and even if a system with two clock modules could achieve higher efficiency in certain situations, that would nonetheless permit an approach using one clock module to control two CPUs performing different tasks. Thus, we find that Shaffer discloses reducing power consumption by reducing system clock speed when the processing workload allows, and discloses doing so in a multiprocessor system with one clock module. Ex. 1005, 4:51–54, 5:5–8, 6:2–5.

4. "output to control a clock frequency of the bus"

Petitioner relies on Shaffer's clock module 50 providing a clock signal to Shaffer's system bus. Pet. 31 (citing Ex. 1005, 2:17–19, 4:15–25, 5:66–6:2). Patent Owner contends that Petitioner relies on different buses for different limitations, by pointing to Shaffer's "data/command bus 21" as the bus connecting the asserted master devices, but pointing to Shaffer's "system bus" as receiving the clock signal. PO Resp. 25–28. Patent Owner acknowledges that Petitioner treats the "data/command bus 21" and "system bus" as one and the same, but asserts that Shaffer consistently describes the two separately and assigns a reference numeral to only the data/command bus 21. *Id.* at 26–27.

We find that Shaffer discloses its clock module 50 providing a clock signal to data/command bus 21, the same bus that Petitioner relies on for other limitations. That conclusion arises from Shaffer's disclosures that show its data/command bus 21 is the described system bus. Shaffer's Summary of the Invention refers to "the CPU and other system buses" without mentioning any more-specific bus. Ex. 1005, 2:17–19; accord *id.*, code (57). Shaffer also discloses that the "CPU speed control system 18" provides the clock frequency "to the other controllers and buses in the

system" and specifically mentions the "data/command bus 21." *Id.* at 4:15–25. Figure 1 shows that "data/command bus 21" connects CPU 20 with memory controller 22 and peripheral bus controller 24. *Id.* Fig. 1. Finally, Shaffer discloses that "the clock module 50 drives the entire system bus (as mentioned above) and thereby reduces power requirements for the processor, related chipsets, memory, controllers and the like." *Id.* at 5:66–6:2. Those disclosures demonstrate that Shaffer's clock module 50 provides an output to control a clock frequency of data/command bus 21, because that bus connects the processor, memory, and peripheral controller.

5. Objective indicia of nonobviousness

Patent Owner asserts that objective indicia of nonobviousness show that the claimed invention would not have been obvious. PO Resp. 56–61. Patent Owner alleges the existence of commercial success and that the '759 patent proceeded contrary to conventional wisdom. *Id.*

As to commercial success, Patent Owner relies on the jury's verdict awarding damages of $675 million against Intel. *Id.* at 57 (citing Ex. 1027, 6). To establish a nexus between Intel's alleged commercial success and the '759 patent's claims, Patent Owner asserts that the jury was "instructed to determine damages solely based upon the value of the patented inventions apart from any unpatented features." PO Resp. 58 (citing Ex. 2067, 1544:14–16, 1545:13–1546:9); PO Sur-reply 20 (noting that the district court rejected Intel's post-trial motions and entered final judgment).

When the evidence shows that a product includes "the invention disclosed and claimed in the patent," we presume that any commercial success of the product is due to the patented invention. *PPC Broadband v. Corning Optical Commc'ns,* 815 F. 3d 734, 746–747 (Fed. Cir. 2016). Such

a presumed nexus requires not only that a commercial product embodies the claims, but also that it is coextensive with them. *See Fox Factory, Inc. v. SRAM, LLC*, 944 F.3d 1366, 1373 (Fed. Cir. 2019) ("[P]resuming nexus is appropriate 'when the patentee shows that the asserted objective evidence is tied to a specific product and that product embodies the claimed features, and is coextensive with them." (quoting *Polaris Indus., Inc. v. Arctic Cat, Inc.*, 882 F.3d 1056, 1072 (Fed. Cir. 2018))).

Petitioner notes that the jury infringement verdict is on appeal and does not apply to all of the challenged claims. Pet. Reply 22–23, n. 8. According to Petitioner, notwithstanding Patent Owner's citation to "cases in support of the proposition that a jury verdict can form part of a commercial success analysis, those cases don't excuse [Patent Owner's] burden on the elements that it must prove." *Id.* at 22–23 (citing *Gambro Lundia AB v. Baxter Healthcare Corp.*, 110 F.3d 1573, 1579 (Fed. Cir. 1997) ("Of course the record must show a sufficient nexus between this commercial success [of the infringing product] and the patented invention.").

Petitioner contends that Patent Owner fails to provide meaningful explanation of its commercial success allegations and fails to show nexus between the claimed features and the alleged commercial success. *Id.* at 22. Petitioner argues that the challenged claims were not the basis for customer demand of the accused products. *Id.* at 23 (citing Ex. 1058, 811:13–812:24 (Intel employee Adam King testifying that Intel's customers care about numerous technical attributes, including graphics performance for video editing, camera quality for video conferencing and power efficiency for laptops)).

Other than the jury verdict, Patent Owner's sole argument that the infringing product's alleged commercial success arose from features claimed

in the '759 patent cites Intel's article in an IEEE publication promoting its "Speed Shift" technology. PO Resp. 58 (citing Ex. 2068, 54); PO Sur-reply 20–21. Patent Owner asserts that the IEEE paper describes a "revolutionary" approach in which a device called a PCU, functioning as a programmable clock controller, improves performance over operating-system-based approaches. *Id.* (citing Ex. 2068, 54, Ex. 2065 ¶¶ 72–73).

The IEEE article cited by Patent Owner is not sufficient evidence to demonstrate the requisite nexus. Intel's employee testified that it takes years and thousands of engineers to build a new generation of processors because such devices include thousands of features and enhancements. Ex. 1058, 811:2–12. Petitioner notes that Patent Owner accused only the Speed Shift feature of infringing the '759 patent and that Patent Owner's damages expert, Dr. Sullivan, "conceded that many of the thousands of other features 'have nothing to do with what [Patent Owner] accuses.'" Pet. Reply 23 (quoting Ex. 1057, 690:19–691:24). Petitioner additionally points out that, in a subsequent trial, Patent Owner's expert agreed that Intel would have sold the accused products regardless of the alleged infringement. *Id.* (citing Ex. 1061, 771:13–22 (testifying that Intel would have made the same sales, even if the jury found the products not to infringe)).

The record before us does not show that Intel's product or products underlying the infringement verdict are coextensive with "the invention disclosed and claimed." *See Fox Factory*, 944 F.3d at 1373, 1377; *see Facebook, Inc. v. Express Mobile Inc.*, IPR2021-01457 Paper 38 at 76–80 (PTAB March 14, 2023) (concluding an infringement verdict was insufficient to establish nexus). Rather, the record shows that the accused products contained many features beyond those relevant to the '749 patent. Ex. 1057, 690:19–691:24; Ex. 1058, 815:16–816:21.

Other than the jury verdict, Patent Owner has not provided financial information that would allow us to weigh the extent of Intel's commercial success based on the alleged sales of products infringing the claimed invention. In particular, the record does not reflect whether the infringing device represented an increase in market share over a prior, noninfringing device or any other aspect that would allow us to place the verdict's amount in context. *See, e.g.*, *In re Applied Materials, Inc.*, 692 F.3d 1289, 1300 (Fed. Cir. 2012) ("An important component of the commercial success inquiry in the present case is determining whether Applied had a significant market share."). On this record we do not find evidence of commercial success sufficient for purposes of establishing non-obviousness.

As to proceeding contrary to accepted wisdom, Patent Owner submits that, prior to the '759 patent, skilled artisans used the operating system to make speed changes. PO Resp. 59. In Patent Owner's view, the '759 patent instead "uses a request mechanism in which the decision-making for speed changes resides in another component, *e.g.*, the programmable clock controller 150." *Id.* at 60–61. Patent Owner's argument depends on our adopting Patent Owner's construction of "request," which we decline to do. *See supra* at 6 (§ II.A.1); Pet. Reply 24. Accordingly, we do not agree with Patent Owner's assertions that the '759 patent proceeded contrary to accepted wisdom, as the prior art disclosed a "request mechanism" under our construction.

Having considered Patent Owner's assertions regarding objective indicia of non-obviousness, we conclude the evidence of record does not persuasively show success of the infringing products with a nexus to the challenged claims or that the claims proceeded contrary to accepted wisdom.

6. Conclusion

We have considered the full record, including evidence and arguments presented by Petitioner and Patent Owner on whether Shaffer and Lint teach or suggest claim 1's limitations, whether there was a reason that skilled artisans at the time would have combined Shaffer and Lint as asserted, and whether objective indicia indicate the claims would not have been obvious. Based on the full record, we conclude that Petitioner has shown by a preponderance of the evidence that claim 1 would have been obvious over Shaffer and Lint.

7. Claim 14

For claim 14, Petitioner relies mainly on its claim 1 contentions, additionally addressing the language in claim 14 that differs from claim 1. Pet. 31–33. Patent Owner separately addresses claims 14 and 18, which recite systems rather than claim 1's method. PO Resp. 19–25.

As discussed above, we agree with Patent Owner that Shaffer does not disclose monitoring its memory controller 22 and peripherical bus controller 24. *See supra* at 16 (§ II.B.2) (discussing claim 1's "monitoring a plurality of master devices"). Claims 14 and 18 recite a first and second master device and a programmable clock controller that interacts with the master devices, but, unlike claim 1, claims 14 and 18 do not require monitoring multiple master devices. Ex. 1001, 8:50–9:4. Thus, our conclusion regarding claim 1's "monitoring" limitation—that Shaffer does not disclose monitoring its memory and peripheral bus controllers (*see supra* at 16 (§ II.B.2)—does not apply to claims 14 or 18.

Other than the "monitoring" aspect, Patent Owner's arguments against Petitioner's analysis of claims 14 and 18 parallel those made for claim 1.

PO Resp. 14–18 (addressing claim 1's limitations reciting "master devices" and "second master device"), 19–25 (addressing claim 14 and 18's "master devices" and "second master device"). As discussed above, we do not agree that claim construction requires a "second master device" that can request speed changes from the clock controller. *See supra* at 10 (§ II.A.2). Thus, we do not agree with Patent Owner that Shaffer's memory controller and peripheral bus controller cannot be the claimed "second master device" in claims 14 and 18. *See* PO Resp. 20–24 ("Thus, Petitioner fails to prove that a POSITA would have understood Shaffer's controllers 22 and 24 to be master devices within the meaning of the '759."). We conclude that the "second master device" claim language in claims 14 and 18 reads on Shaffer's controllers 22 and 24 as Petitioner asserts. *See* Pet. 30–31, 33. This conclusion is consistent with our construction for "master device," as discussed above. *See supra* at 10 (§ II.A.2).

Patent Owner challenges also whether Shaffer discloses claim 14's requirement that the clock controller controls the clock frequency of a second mater device based on Shaffer's multiple-CPU embodiment. PO Resp. 25 (citing *id.* at 16–18). For the reasons discussed above, we find that Shaffer's multiple-CPU embodiment discloses a single clock controller controlling the clock frequency of a second master device (a second CPU) coupled to the bus. *See supra* at 20 (§ II.B.3). This conclusion is independent of our construction of "master device," as Patent Owner does not argue Shaffer's additional CPU's could not request speed changes.

Considering the full record, including Patent Owner's asserted objective indicia discussed above, we conclude that Petitioner has shown by a preponderance of the evidence that claim 14 would have been obvious over Shaffer and Lint.

8. Claim 17

Petitioner relies on Shaffer as disclosing the additional limitations of claim 17, which depends from claim 14. Pet. 31, 33. Patent Owner does not challenge those contentions. We have reviewed Petitioner's contentions and determine that Petitioner has shown claim 17 would have been obvious over Shaffer and Lint.

C. Obviousness over Shaffer, Lint, and Kiriake (Claims 18, 21–22, 24)

For independent claim 18, Petitioner relies on its claim 1 contentions, addressing the differences in the language between claims 1 and 18, and asserting that Kiriake discloses both master devices and the claimed arbiter. Pet. 34–38. For claims 21, 22, and 24, each of which depends from claim 18, Petitioner points to Shaffer's additional disclosures that teach or suggest the additional limitations recited in those claims. Pet. 38–39. Other than as discussed above regarding claim 1, Patent Owner does not dispute Petitioner's contentions. We have reviewed the record, including Patent Owner's asserted objective indicia of nonobviousness, and determine that Petitioner has shown claims 18, 21, 22, and 24 would have been obvious over Shaffer, Lint, and Kiriake.

D. Obviousness over Chen and Terrell (Claims 1, 14, 17)

Relying on Chen for most limitations of claim 1, Petitioner submits that Terrell teaches requesting a clock speed change "in response to a predefined change in performance of the first master device" and that the predefined change "is due to loading of the first master device as measured within a predefined time interval." Pet. 40–49.

Chen discloses an extension to an input/output ("I/O") bus and bridge chip that allows higher-speed operation. Ex. 1003, code (57), 1:6–8. To that end, Chen discloses a system "for switching between different data transfer speeds." *Id.* at 1:61–62. Chen's host bridge "interconnects a system bus with an I/O bus" and includes control logic to allow "bus transactions at both a high frequency and a lower frequency." *Id.* at 2:1–6.

Chen's Figure 1 is reproduced below:

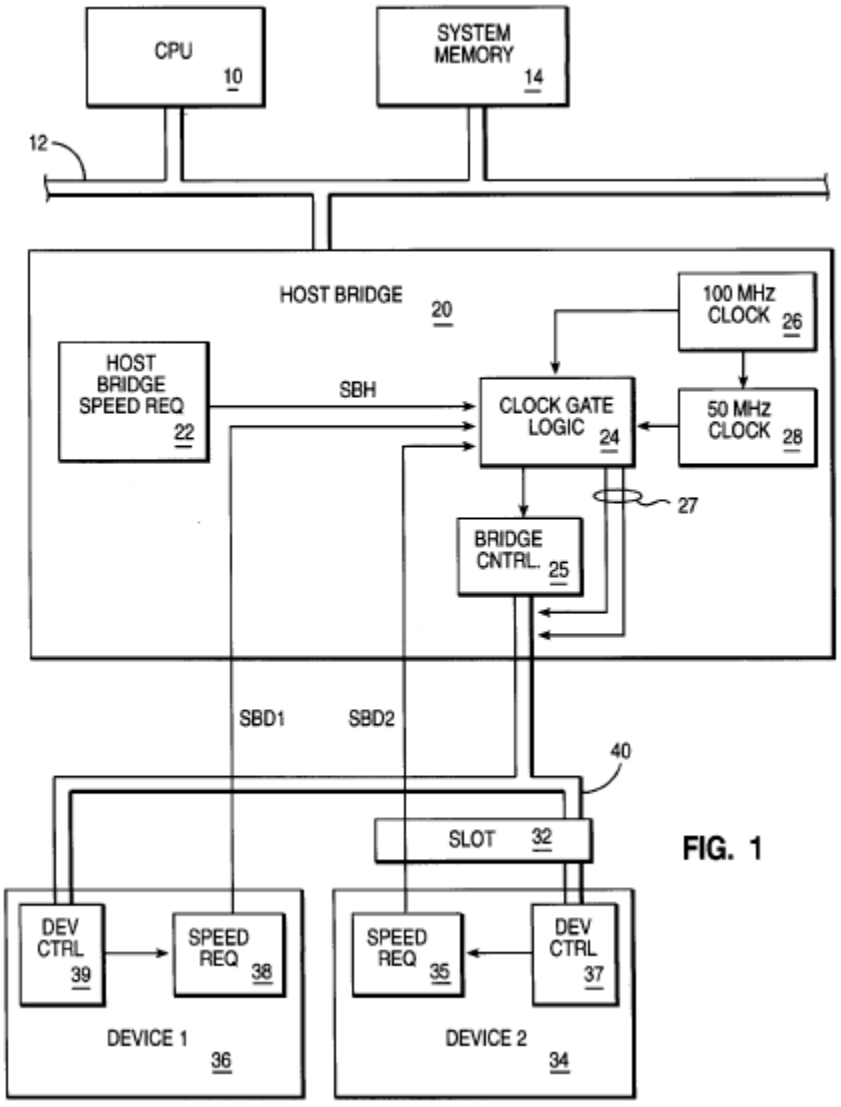

FIG. 1

Figure 1 depicts CPU 10 connected to system bus 12, which connects to host bridge 20, which interconnects system bus 12 with I/O bus 40 that communicates with devices 34 and 36. *Id.* at 2:50–3:4. Device 36 is a "soldered device" while device 34 is a "pluggable device" in slot 32. *Id.* at 3:1–3. Devices 34 and 36 have speed requesting circuits 38 and 35, respectively, that communicate with clock gate logic circuit 24, which causes the frequency of bus 40 to be dynamically changed through unique clock lines 27. *Id.* at 3:4–22.

Terrell discloses a system and method for controlling the frequency of a common clock shared by a number of processing elements. Ex. 1004, code (57). Terrell states that "it is desirable to be able to reduce the frequency of a shared clock to the minimum frequency that allows the processing elements to function correctly while using the least amount of power." *Id.* ¶ 5. Terrell states that its goal would be desirable in "[a]n on-chip bus that hosts two or more bus masters, all of which share a common bus clock." *Id.* ¶ 8.

To implement its approach, Terrell discloses "two basic steps":

> 1. Over a sample period, measure how many clock cycles are being used by each processing element that is attached to the shared clock.
>
> 2. Adjust the system clock frequency to provide the minimum number of clock cycles required by the processing element that is using the largest number of clock cycles.

Id. ¶¶ 25–27.

1. Reason to combine

Petitioner asserts that Chen's master devices 34 and 36 send requests to change a clock frequency, and that skilled artisans would have had reason

to modify Chen's master devices so that they send requests in response to a predefined change in their performance. Pet. 42–47. Petitioner submits that "it was well-known, desirable, and taught by Terrell to save power." *Id.* at 44 (quoting Ex. 1004 ¶ 5 ("[I]t is desirable to be able to reduce the frequency of a shared clock to the minimum frequency that allows the processing elements to function correctly while using the least amount of power.")). Petitioner contends further that Chen teaches embodiments relevant to "a cost-oriented solution and/or low-frequency operations for saving power." *Id.* at 44 (citing Ex. 1003, 5:21–24, 4:36–39, 3:25–29, 3:42–44).

We agree that Chen discloses operating at lower speeds for certain circumstances. For example, Chen discloses using increased frequency for only memory read and write operations, while using lower frequency for bus arbitration and other operations. Ex. 1003, 4:24–36. Chen notes further that the system could use its high-frequency mode for all operations if the "additional cost and complexity is not a factor." *Id.* at 4:36–39. As Patent Owner points out, however, "this increased cost and complexity is fixed at the time of design regardless of whether the bus is run at higher or lower speed." PO Resp. 35–36. Thus, we find that Chen discloses the reduced fixed cost of components that operate only at a lower frequency, but does not disclose reduced power consumption when operating at a lower frequency.

While Chen does not expressly disclose power savings, the record supports a finding that skilled artisans would have understood power savings as an important consideration. *See* Ex. 1056, 386:2–4 (Patent Owner's expert, Dr. Conte, testifying in the litigation that "power savings in designing a processor" is "extremely important"). Indeed, Terrell discloses

that "it is desirable to be able to reduce the frequency of a shared clock to the minimum frequency that allows the processing elements to function correctly while using the least amount of power." Ex. 1005 ¶ 5. We conclude therefore that the prospect of achieving power savings would have motivated skilled artisans to operate Chen's system at a reduced clock frequency when not required by performance demands. *See Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1380 (Fed. Cir. 2023) ("'[U]niversal' motivations known in a particular field to improve technology provide 'a motivation to combine prior art references even absent any hint of suggestion in the references themselves.'" (quoting *Intel Corp. v. Qualcomm Inc.*, 21 F.4th 784, 797–99 (Fed. Cir. 2021))).

Patent Owner contends that Chen and Terrell have opposite goals because Chen focuses on increasing frequency for performance while Terrell focuses on reducing frequency for power savings. PO Resp. 32–37. Petitioner, however, explains how the teachings would work together to "select a clock frequency that increases the devices' frequency only when needed, to reduce power consumption, even if the devices can use higher speeds." Pet. 45. Such a combination is consistent with Chen's teachings of increasing frequency for certain operations, and also consistent with Terrell's teachings of reducing frequency when possible. In this way, we credit Dr. Jacob's testimony that the combination would have balanced "the inherent trade-off between highest performance at the highest cost, and lower (but perhaps still acceptable) performance at a lower cost." Ex. 1055 ¶ 112. Thus, the combined system Petitioner asserts would have been able to operate at reduced frequency (conserving power) in low-activity times and increased frequency when the system required higher performance. *Id.* ¶ 117.

Because the asserted combination would have been able to satisfy a performance demand, we do not agree with Patent Owner that the combination defeats Chen's intended purpose. *See* PO Resp. 37–42. Patent Owner's interpretation, that Chen requires maximum speed at all times, is implausible in light of Terrell's recognition that systems may spend time in an idle state (Ex. 1004 ¶ 54), and Chen's disclosure of operating devices below their maximum speed (Ex. 1003, 3:42–43 ("I/O devices which normally operate at 66 M[H]z can be operated at 50 M[H]z.")). We conclude that Chen's "principle of operation and stated goal" are preserved by the asserted combination, in which bus speed is reduced when performance needs allow and then increased to the limit of a device's capabilities when required.

Patent Owner argues additionally that the asserted combination would have required modifying devices to support reduced speed, and that the required modifications would increase cost and complexity such that skilled artisans would not have made the combination. PO Resp. 42–47. Petitioner responds, on the other hand, that devices with thousands of transistors were commonplace at the time of the '759 patent's invention. Pet. Reply 18 (citing Ex. 1055 ¶¶ 118–119). We agree with Petitioner that the added complexity required by the asserted combination would not have risen to a level that skilled artisans would have been dissuaded from making the combination. In particular, we agree that, by 2005, when the application resulting in the '759 patent was filed, Terrell's approach did not present a significant technological obstacle to a skilled artisan seeking to modify Chen's system. *See* Pet. Reply 18. We credit Dr. Jacob's testimony that technology had advanced considerably following Chen's mid-1990s disclosure such that the modification would have imposed a modest

challenge. *See* Ex. 1055 ¶ 118–119. That same technological progress likewise would minimize any challenge skilled artisans would have had with modifying Chen's master devices. *See* PO Resp. 42–43. Those devices would have required only modest changes to work with the modified system, and skilled artisans implementing Chen's system in 2005 would have done so with integrated devices, thus eliminating Patent Owner's asserted need to modify a host of disparate devices. *See* Ex. 1055 ¶¶ 119, 132–137.

Patent Owner further challenges Petitioner's reliance on Terrell's statement that its teachings apply to "[a]n on-chip bus that hosts two or more bus masters, all of which share a common bus clock." Ex. 1004 ¶¶ 6, 8; PO Resp. 47–48 (citing Pet. 46). Patent Owner points out that Chen's bus 40 is a peripheral, off-chip bus and implicates different design constraints. *Id.* Petitioner contends that, regardless of whether Chen's bus is itself an on-chip bus, technological progression after Chen resulted in master devices moving on-chip and using an on-chip bus. Pet. Reply 19 (citing Ex. 1055 ¶¶ 132–137). Notwithstanding Dr. Jacob's testimony that Chen's system would be implemented differently by the time of the '759 patent, the dispute does not change our determination because, as discussed above, Petitioner has shown that skilled artisans would have made the asserted combination, aside from Terrell's statement about on-chip buses. Terrell's statement of particular applicability to on-chip buses does not undermine its separate statement regarding the desirability of reducing power consumption by reducing clock frequency when possible. Ex. 1004 ¶ 5. That express teaching shows that skilled artisans understood the possibility of reducing power by reducing frequency.

We conclude that skilled artisans had reason to arrive at the asserted combination.

2. "providing the clock frequency . . . as an output to control a clock frequency of a second master device"

Petitioner contends that, in Chen, when the first master device requests a clock-frequency change, Chen's clock gate logic 24 provides the high-speed clock on clock line 27 as an output to control a clock frequency of a second master device coupled to the bus. Pet. 48. Because the master devices may conduct "peer to peer transactions," when both indicate they support high-speed communications, they both receive the same clock frequency. Ex. 1003, 5:13–24 ("With the PCI, and some other I/O bus specifications, each device is required to receive its own unique clock signal."), 5:25–29 ("[E]ach device receives its own unique clock line which will be clocked at the appropriate frequency."), 5:59–65 (discussing peer-to-peer transfer).

Further, Petitioner contends Chen provides that same frequency to the bus to facilitate the communication. Pet. 49 (citing Ex. 1003, 2:8–14 ("In response to" a signal indicating high-frequency capability, "control logic in the bridge chip causes the higher frequency clock in the bridge chip to be activated such that the host bridge, bus and I/O device are all then operating at the higher frequency.")).

Patent Owner responds that Chen does not disclose providing the clock frequency as an output to control a clock frequency of a second master device because Chen discloses controlling only the bus frequency, not the master device frequency itself. PO Resp. 48–56. Patent Owner points to Chen's disclosure that "[c]lock gate circuit 24 causes the frequency of bus 40 to be dynamically changed (gated) by transmitting the appropriate device unique clock lines 27." *Id.* at 49–50 (quoting Ex. 1003, 3:20–22). In Patent Owner's view, Chen's clock lines 27 can serve to control the bus

frequency *or* the master devices' frequencies, but not both. *Id.* at 49. Patent Owner reasons that Chen's I/O devices "included an internal clock, separate and apart from the PCI bus clock," and thus cannot satisfy the claim language. *Id.* at 50. For support, Patent Owner cites "the OTI Sound/Fax Card," which Patent Owner views as an exemplary device from Chen. *Id.* at 50–52; PO Sur-Reply 18 (citing Ex. 1003, 1:18–22).

Chen states in its discussion of the background that "many I/O devices, such as . . . sound cards, and the like still operate at frequencies ranging from 33 M[H]z to 66 M[H]z." Ex. 1003, 1:18–22. Although Patent Owner argues the OTI Sound/Fax Card is an exemplary sound card contemporaneous with Chen, Patent Owner does not establish that all I/O devices compatible with Chen would have had internal clocks such that Chen did not provide a clock output to its I/O devices. We agree with Dr. Jacob, who testifies that Chen indicates the opposite—that its bus devices did not necessarily have separate, internal clocks. Ex. 1055 ¶ 124–126. Dr. Jacob explains that because Chen discloses distinct bus clock lines for each bus device, Chen suggests that the bus clock *does* run the devices' internal circuitry. *Id.* On Chen's shared bus, devices not involved in an active communication would have no need for their bus interfaces to remain active, so there would be no point to sending them a clock signal different from the active bus clock. If, instead, those devices were relying on the bus clock for more than bus communication—i.e., to run their internal circuity—then sending the distinct clock signal at a frequency different from active bus communication would allow those devices to remain operational while bus communication occurs with other devices. *Id.* Because multiple distinct clock lines come at a cost, Chen's designers would only include those clock lines if they provided a benefit. *Id.* Based on the record, we agree with

Petitioner and find that at least some of Chen's bus devices use the bus clock to control their internal operations.

Moreover, we do not agree with Patent Owner's implicit claim construction that "providing the clock frequency . . . to control a clock frequency of a second master device" refers only to "the internal clock frequency of the master device, not to an I/O bus frequency" PO Resp. 52 (citing Ex. 2065 ¶ 186). To assert that Chen does not teach providing the clock to control a clock frequency of a second master device, Patent Owner relies on the testimony of Dr. Conte. Dr. Conte explains that in the exemplary OTI Sound/Fax Card, "the LCLK is an input clock – the PCI clock – that would allow the OTI Sound/Fax Card to communicate over the PCI bus" and "is separate from and has nothing to do with an internal clock source (MCLKSR) of the OTI Sound/Fax Card." Ex. 2065 ¶ 186. Dr. Conte concludes that skilled artisans "would understand that the I/O bus clock in Chen has nothing to do with the internal clock of the I/O device (such as the OTI Sound/Fax Card's MCLKSR clock)." *Id.* Dr. Conte does not explain why "a clock frequency of a second master device" is restricted as a matter of claim construction to an internal clock frequency separate from the commanded bus frequency. Without a sound basis in the intrinsic record—which Patent Owner has not explained—we decline to limit "a clock frequency of a second master device" as a matter of claim construction to "an internal clock separate and apart from the bus clock" as Patent Owner seeks. PO Resp. 50–52 (distinguishing I/O devices with "an internal clock . . . separate and apart from the PCI clock"); Pet. Reply 21; Ex. 1055 ¶ 94–96 (explaining that controlling "a clock frequency" includes "controlling the device's data-interface frequency"); *see supra* at 12 (§ II.A.3). Accordingly, we agree with Petitioner that "Chen's master devices and bus would be

clocked to the same frequency when conducting transactions over the bus" and that, therefore, "it is irrelevant whether such devices could also have other clocks within them." Pet. Reply 21.

Relatedly, Patent Owner argues that Chen's "clock line 27 output by clock gate logic 24" can satisfy only one of the limitations that require both (1) an output to the second master device and (2) an output to the bus. PO Resp. 53–55. We do not agree, in light of Chen's disclosure that "control logic in the bridge chip causes the higher frequency clock in the bridge chip to be activated such that the host bridge, bus and I/O device are all then operating at the higher frequency." Ex. 1003, 2:8–14; *accord id.* at 4:63–5:5 ("Clock gate logic 24 will then enable the high frequency clock 26 and drive bus 40 at 100M[H]z."). Chen's disclosures support that clock gate logic 24 provides the clock frequency to both the bus itself (via the bridge chip) and the bus devices (via the distinct device clock lines).

In view of the foregoing, we find that Chen discloses providing the clock frequency of the high-speed clock as an output to control a clock frequency of a second master device coupled to the bus and as an output to control a clock frequency of the bus.

3. Conclusion

We have considered the full record, including evidence and arguments presented by Petitioner and Patent Owner on whether Chen and Terrell teach or suggest claim 1's limitations, whether there was a reason that skilled artisans at the time would have combined Chen and Terrell as asserted, and whether objective indicia indicate the claims would not have been obvious. Based on the full record, we conclude that Petitioner has shown by a preponderance of the evidence that claim 1 would have been obvious over

Chen and Terrell. Patent Owner's arguments discussed above apply to claims 1 and 14. *See* PO Resp. 48–49. We conclude that Petitioner has shown by a preponderance of the evidence that claim 14 would have been obvious over Chen and Terrell. Pet. 49–52.

Petitioner relies on Chen and Terrell as disclosing the additional limitations of claim 17, which depends from claim 14. Pet. 52–53. Patent Owner does not challenge those contentions. We have reviewed Petitioner's contentions and determine that Petitioner has shown claim 17 would have been obvious over Chen and Terrell.

E. Obviousness over Chen, Terrell, and Kiriake (Claims 18, 21, 22, 24)

For independent claim 18, Petitioner relies on its claim 1 contentions, additionally addressing the unique claim language and asserting that Kiriake discloses both master devices and the claimed arbiter. Pet. 54–59. For claims 21, 22, and 24, each of which depends from claim 18, Petitioner points to Chen's additional disclosures that render obvious the additional limitations. Pet. 59–60. Patent Owner does not challenge those contentions. We have reviewed Petitioner's contentions and determine that Petitioner has shown claims 18, 21, 22, and 24 would have been obvious over Chen, Terrell, and Kiriake.

F. Patent Owner's Motion to Exclude

Patent Owner moves to exclude Dr. Jacob's Declarations (Ex. 1002 and Ex. 1046, "Original Declarations") as inadmissible hearsay under Federal Rules of Evidence 801 and 802. Paper 88 ("PO Mtn. Exclude"). Patent Owner argues that the Original Declarations were not "executed in connection with the current proceeding, and therefore were not made 'while

testifying at the current trial or hearing.'" PO Mtn. Exclude, 2–3; Fed. R. Evid. 801(c)(1).[10] Patent Owner asserts that the Board was incorrect in the Institution Decision when we concluded that cross-examination would address hearsay concerns. *Id.* at 4. Finally, Patent Owner contends that no hearsay exceptions apply, citing Fed. R. Evid. 804(b)(1), 803(18).

Petitioner argues that Dr. Jacob's Original Declarations are not inadmissible hearsay. Paper 94 ("Pet. Opp. Mtn. Exclude"), 11. Petitioner points to 37 C.F.R. § 42.53(a), which states "[u]ncompelled direct testimony must be submitted in the form of an affidavit." *Id.* Despite that the Original Declarations were prepared for another proceeding, Petitioner argues that they are not hearsay because (1) they were submitted as sworn witness statements in lieu of live testimony in this proceeding, (2) Dr. Jacob reaffirmed them in the joinder proceeding (IPR2022-00366, Ex. 1049), and (3) Dr. Jacob was subject to cross-examination on the contents of the Original Declarations in this proceeding. *Id.* at 12–13. Indeed, during cross-examination, Dr. Jacob confirmed that the Original Declarations set forth his opinions regarding the '759 patent. Ex. 2066, 69:12–17 (identifying Ex. 1002), 72:11–21 (identifying Ex. 1046), 73:4–10 (confirming the declarations set forth his opinions).

We agree with Petitioner and deny Patent Owner's motion because Dr. Jacob's cross-examination and his confirmation of the declarations in this proceeding address Patent Owner's hearsay concern.[11] IPR testimony is

[10] Petitioner does not dispute that Dr. Jacob's Original Declarations are offered "to prove the truth of the matter asserted." PO Mtn. Exclude 3; Fed. R. Evid. 801(c)(2).

[11] Patent Owner's argument that OpenSky did not contact Dr. Jacob before filing its Petition with Dr. Jacob's Declarations is not persuasive in light of his willingness to testify in this proceeding. PO Mtn. Exclude 6–10.

different from that in district courts. Notably, the Board's rules generally do not allow an expert to "testify" in person at an IPR hearing. *See* 37 C.F.R. § 42.53 (a)–(b)(1); 35 U.S.C. § 316(a)(5); 35 U.S.C. § 23. Testimony is instead submitted as evidence in the form of affidavits and deposition transcripts. *See* 37 C.F.R. §§ 42.53, 42.63. Our rules, therefore, contemplate that declarants in IPRs do not "testify" in the traditional sense of giving live testimony in a courtroom.

As other Board decisions have noted, "[w]ithout exception, the Board accepts the filing of sworn witness declarations in lieu of live testimony in administrative patent trials." *Grünenthal Gmbh v. Antecip Bioventures II LLC*, PGR2018-00062, Paper 32 at 15 (PTAB Oct. 29, 2019). Our procedures adopt that practice for its efficiency and ensure fairness by allowing cross-examination. *See id.*; 37 C.F.R. § 42.51(b)(ii). Dr. Jacob has made himself available for cross-examination and confirmed that the declarations express his opinions here, in this proceeding. Thus, in these respects, the Original Declarations are no different than the other testimony relied on by the parties, and are not hearsay subject to exclusion.

Indeed, during his cross-examination, Dr. Jacob confirmed that the Original Declarations set forth his opinions regarding the '759 patent. Ex. 2066, 69:12–17 (identifying Ex. 1002), 72:11–21 (identifying Ex. 1046), 73:4–10 (confirming the declarations set forth his opinions). In Intel's proceeding asserting the same grounds and seeking joinder, Dr. Jacob filed a declaration reaffirming his Original Declarations and confirming that he would appear for cross-examination. IPR2022-00366, Ex. 1049. We noted that Dr. Jacob's reaffirming declaration and availability for cross-examination allayed concerns about hearsay. Paper 43 (joinder decision), 15. While the reaffirming declaration is not of record in this proceeding,

Dr. Jacob's deposition in this proceeding and statements confirming his opinions serve the same role. Patent Owner has suffered no prejudice from Dr. Jacob's Original Declarations.

We have considered Patent Owner's other arguments (Paper 95) and find them just as unavailing. The fact that the Jacob declarations were prepared for another proceeding is immaterial in this case because Dr, Jacob has expressly adopted them for *this* proceeding. *Id.* at 1–3. Nor is a hearsay exception necessary, as the reaffirmance of the prior testimony by Dr. Jacob and his cross-examination *in this proceeding* overcomes any plausible hearsay argument or the necessity for a hearsay exception. *Id.* at 3–5. Finally, there is no merit to Patent Owner's suggestion (*id.* at 5) that reliance on Dr. Jacob's reply declaration is somehow contrary to our procedures, which specifically provide for replies by the petitioner (including new declarations). *See* USPTO Consolidated Trial Practice Guide 73 (Nov. 2019).[12]

For the reasons given, we deny Patent Owner's Motion to Exclude.

III. CONCLUSION[13]

For the reasons discussed and based on the entire record, Petitioner has shown by a preponderance of the evidence that claims 1, 14, 17, 18, 21,

[12] Available at https://www.uspto.gov/TrialPracticeGuideConsolidated.

[13] Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. *See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of

22, and 24 are unpatentable. Patent Owner has not shown that we should exclude Exhibits 1002 and 1046.

In summary:

Claim(s)	35 U.S.C. §	Reference(s)/Basis	Claim(s) Shown Unpatentable	Claim(s) Not shown Unpatentable
1, 14, 17	103	Shaffer, Lint	1, 14, 17	
18, 21, 22, 24	103	Shaffer, Lint, Kiriake	18, 21, 22, 24	
1, 14, 17	103	Chen, Terrell	1, 14, 17	
18, 21, 22, 24	103	Chen, Terrell, Kiriake	18, 21, 22, 24	
Overall Outcome			1, 14, 17, 18, 21, 22, 24	

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that Petitioner has shown by a preponderance of the evidence that claims 1, 14, 17, 18, 21, 22, and 24 are unpatentable;

FURTHER ORDERED that Patent Owner's Motion to Exclude (Paper 88) is denied; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

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