Categories and Evolution to Home/Residential Gateway

This huge installed base of set-top boxes can be broadly classified into the following categories:

- Analog set-top boxes perform the function of receiving, tuning, and de-scrambling incoming television signals. These receivers have changed very little over the past twenty years.
- Dial-up set-top boxes allow subscribers to access the Internet from the comfort of their living room through the television.
- Entry-level digital set-top boxes are capable of receiving broadcast digital television that is complemented with a pay-per-view system and a very basic navigation tool. They have no return channel, and therefore do not interact with computer servers. Characteristics of this type of low-cost box include limited quantities of memory, interface ports and processing power. Figure 2 shows a digital set-top box.
- Mid-range digital set-top boxes include a return (back) channel, which provides communication with a server located. These set-top boxes provide e-commerce, Internet browsing, and multimedia services. The return channel further allows for customized broadcasts to the local viewing population. These types of boxes have higher processing power and storage capabilities of entry-level boxes.
- Advanced digital set-top boxes are like multimedia desktop computers, containing much higher processing power than other set-top boxes. Enhanced capabilities in conjunction with a high-speed return path can be used to access a variety of advanced services such as video teleconferencing, home networking, IP telephony, VoD, and high-speed Internet TV services. Additionally, it has enhanced graphical capabilities to receive high definition TV signals and can store video on a hard disk drive, while providing the capability to record and view video simultaneously. Such receivers have a range of high-speed interface ports, and resemble residential gateways. For cable, terrestrial, and satellite companies, set-top boxes that support advanced technologies are an opportunity to increase revenue streams through providing services.

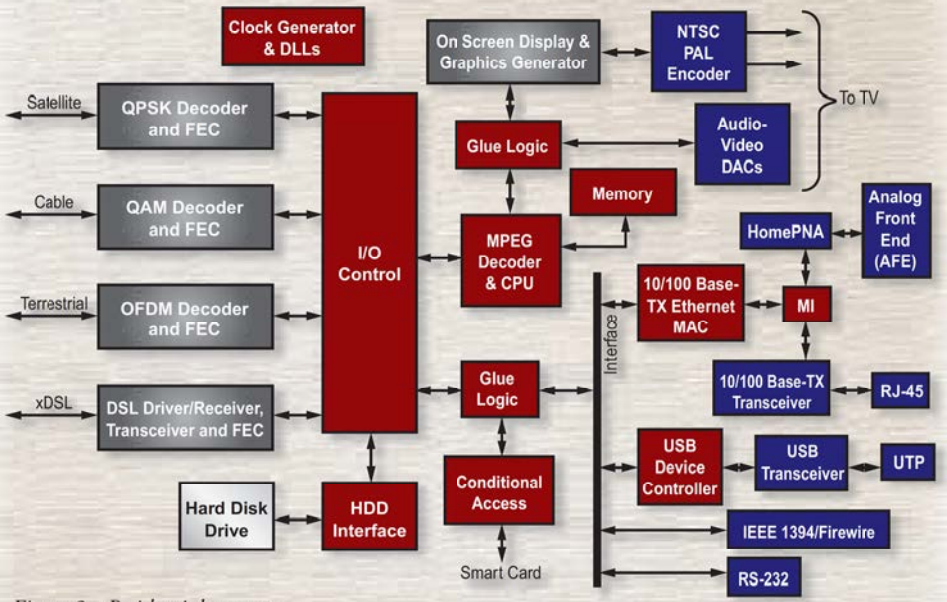


Figure 3 - Residential gateway

The residential gateway is a platform to bring broadband into the house and connect or bridge to home networking technologies. It enables communication between networked appliances in the home and across the Internet. The evolution of new data broadcasting services has created the need for a device to pass digital content between the Internet and the home network. Future gateways will provide integrated services such as remote management, home automation, and home security.

Mass deployment of gateways will come in three distinct phases. While the gateway is a new term, it already exists in many homes. Most of our homes have a set-top box for receiving television and a modem to connect to the Internet. Phase two includes advanced features such as broadband connectivity, home networking interfaces, and IP telephony in the residential gateway. The third phase will be deployment of powerful gateways, capable of delivering video, voice and data throughout the home and providing services such as home automation, energy management, security control, and so on.

Supporting multiple technologies makes the gateway less likely to become obsolete. Support for modularity will fuel the evolution of gateways into a type of application server that consumers will use to distribute broadband services throughout their homes. The gateway must have a reliable and robust hardware platform, and software that is not susceptible to errors. Unlike PC users, consumers will not stand rebooting their gateways. Supporting multiple services with complete security is essential. Functions such as e-commerce transactions, and remote home control and access from authorized service providers are critical. Providing quality of service to support multiple intelligent devices from different vendors is extremely important.

Figure 3 shows the block diagram of a residential gateway. The gateway provides a unified platform to satisfy the needs of most consumers, providing infotainment, conveniences, and communication. The success of the set-top box, and hesitation by a large population to own a PC, allows for the set-top box to grow into a successful residential gateway. Set-top boxes will evolve into multimedia servers, forming the hub of the

home network for primary access to the Internet, such as the residential gateway.

Programmable Logic Solutions Enable Future Set-Top Boxes

For residential gateways to be successful, programmable solutions will have to be at the heart of the system. Programmable logic devices address the fundamental disconnect between ASSPs and provide the interface and protocol translation between different broadband and home-networking chipsets. They provide significant time-to-market advantages and the ability to upgrade quickly, which is imperative for a successful product. This gives you the cutting edge to bring products first to market, while having the ability to remotely add features to the set-top box already deployed in the home.

The set-top box will combine components such as digital modem chipsets, home networking chipsets, processors, memory, and software. Digital modem chipsets provide connectivity to different broadband networks, and home networking chipsets provide interconnectivity technologies between appliances. Other ASSPs/ASICs handle and process digital video and audio services. These ASSPs communicate with each other via buses on the system board. The processor is responsible for coordinating the different components. With additional features, set-top boxes will require higher performance processors to keep pace with increased data throughput. However, all these standards and ASSPs promote differing interfaces making glueless connectivity impossible between the different ASSPs, memories, and processors.

There are three types of set-top box software: operating systems, middleware, and applications. The operating system operates the set-top box parts. The middleware is a layer of software programs that operates between the interactive TV applications and the operating system. Viewers use application software to watch TV and use interactive features. The middleware also enables the smooth interoperation of information appliances and services within the home, to eliminate the complexity, distribution, and technical disparity of the system elements.

For video processing conventional DSPs (digital signal processors) provide a fixed data width and inflexible architecture. They typically have 1-4 MAC units and require serial processing, which limits data throughput. This causes a need for high clock frequency DSPs, which creates system challenges. Hence, multiple DSPs are needed to meet bandwidth requirements, thus causing power and board space issues. Programmable logic devices have a flexible architecture with distributed DSP resources and embedded multipliers. These devices can support any level of parallelism or serial processing through an optimal performance/cost tradeoff. This parallel processing maximizes the data throughput. Hence, programmable logic solutions exceed DSP requirements of the video market – providing both flexibility and performance. FPGAs are off-the-shelf devices, which provide fast time-to-market, rapid adoption of standards, optimal bit widths, and real-time prototyping along with support for high data rates. With a whole suite of DSP algorithms/cores and tools created for programmable logic devices, development time can be reduced by weeks while increasing the performance of the system. For example, the implementation of the DCT/IDCT core in a programmable logic device can off-load the system processor performing MPEG encoding/decoding with a 50X to 200X performance gain.

Programmable solutions also provide the ability to interface to different hard-disk drive types as well as NAND and NOR flash memory types (depending on availability). They also provide content protection capabilities using DES, triple DES, AES, and even proprietary encryption schemes. They also provide system interface functions such as PCI, USB, and so on, in the set-top box and residential gateway. In addition, the presence of the FPGA in the system provides the capability to remotely upgrade features through the Internet when the box has been shipped to the customer, hence providing a significant cost savings.

Summary

The set-top box is driving the digital revolution right into your living room. Your fingertips now command a wealth of high-quality digital information and digital entertainment, right from your favorite armchair. The set-top box revolutionizes home entertainment by providing vibrant television images with crystal clear sound, along with e-mail, Web surfing, and customized information such as stock quotes, weather and traffic updates, on-line shopping, and video-on-demand – right through a traditional television.

The set-top box will evolve into home multimedia centers, possibly forming the hub of the home network system and the primary access for consumers to connect to the Internet. There will be a convergence of technology with equipment connected to the television, such as adding hard drives for television program storage and instant replay. As the set-top box evolves, it will also provide home networking capabilities and value-added services, while becoming the residential gateway of the future.

Programmable logic solutions are necessary for the success of set-top boxes and residential gateways as they provide time-to-market and time-in-market advantages in interfacing disparate technologies, components and system interfaces. They also provide a significant performance advantage over digital video processors. What is clear is that the set-top box market is growing at a very dramatic rate, and when markets are so dynamic and the future is very unpredictable, decreased time-to-market and the ability to upgrade very quickly is imperative for a successful product.

Low-cost Digital Video IEEE 1394 Hardware Reference Design

New reference designs provide OEMs with a complete low-cost solution for integrating digital video in consumer products.

by Xilinx Staff

Xilinx and Convergent Designs recently announced the availability of Centauri, a low-cost digital video (DV) IEEE 1394 hardware reference design based on the low-cost Xilinx Spartan™ FPGA and the Divio NW701 DV codec. The new reference design provides OEM manufacturers with a complete low-cost solution for easily integrating DV over IEEE 1394 into a variety of consumer digital video products such as DVD R/Ws, digital VHS recorders, set-top boxes, residential gateways, Personal Video Recorders (PVRs), Digital TVs (DTVs), video projectors, video editors, and professional digital audio and video equipment.

"The Spartan family of FPGAs provided an ideal low-cost solution," said Michael Schell, president of Convergent Design. "Because of the Xilinx commitment to the Digital Video market, we're able to rapidly introduce cost effective consumer solutions that reduce overall time-to-market and cost."

"The introduction of this hardware reference design is a great example of the compelling value that FPGAs offer the consumer marketplace," said Robert Bielby, senior director of Strategic Solutions Marketing at Xilinx. "Working closely with Convergent Designs and utilizing their digital video and audio design expertise allows us to provide some exciting solutions for the consumer market."

> "The Spartan family of FPGAs provided an ideal low-cost solution. Because of the Xilinx commitment to the Digital Video market, we're able to rapidly introduce cost effective consumer solutions that reduce overall time-to-market and cost." — Michael Schell, president of Convergent Design.

Pricing and Availability

Centauri is priced at $450 and immediately available for purchase on the Xilinx eSP website (*www.xilinx.com/esp*).

Xilinx eSP for Digital Video

Xilinx eSP (*www.xilinx.com/esp*) is the industry's first Web portal dedicated to accelerating the design and development of consumer products based upon emerging standards and protocols. Recently updated to contain broad coverage of digital video technologies, the eSP Web portal is a comprehensive resource delivering a powerful array of solutions and information in a single location.

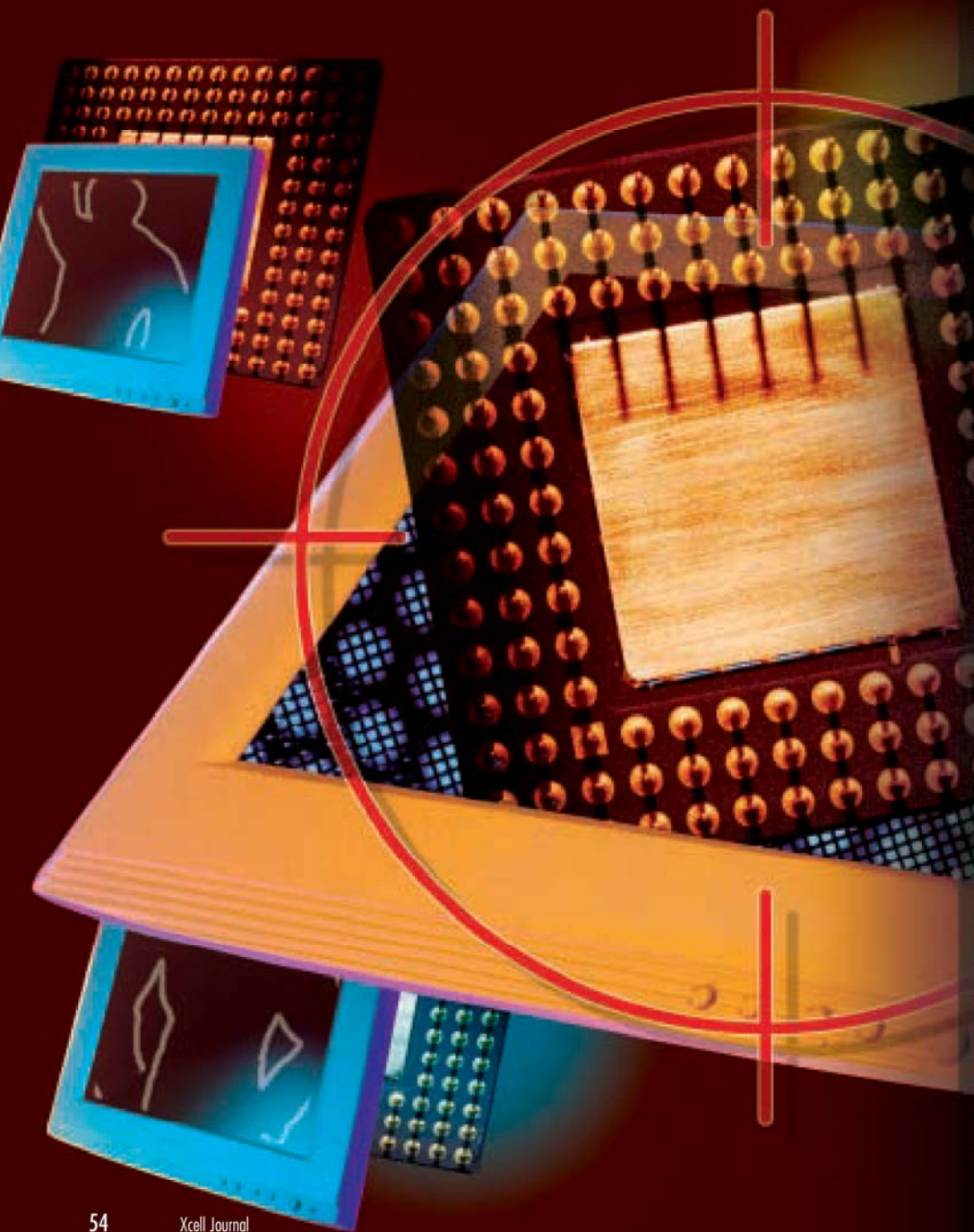
About Convergent Design

Convergent Design has joined the Xilinx XPERTS program, a worldwide third-party Certified Design Service Center trained to take full advantage of the features in Xilinx FPGAs, software, and IP cores.

Convergent Design LLC specializes in the design and development of analog digital video/audio conversion and processing products. Specific technologies include: PCI, 1394, DV/MPEG2 compression, component video, SDI digital video, balanced audio, and AES/EBU digital audio. Convergent Design offers comprehensive design services including initial product specification, schematic capture, FPGA code development, PCB prototype and debug, compatibility testing, and release to contract manufacturer.

Programmable Logic Enables Digital Displays

An overview of an important emerging market.



by Mike Nelson
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DisplaySearch Inc. forecasts that by 2005, digital displays will eclipse conventional display technologies in market revenue. Digital liquid crystal displays (LCDs), digital plasma display panels (PDPs), digital light processors (DLPs), and many others are fast becoming the display technologies of choice.

This article will explain why this is happening and document the universe of complexity that has been spawned in the process. Next we will examine some of the unique challenges that digital display systems pose for you. Finally, we will review a representative case study to illustrate how programmable logic can be used to your advantage in developing digital display products.

The Digitization of Display Technologies

What's driving the digital display transition? There are three basic answers to this question:

- Content has become digital
- Digital displays achieve superior quality
- Digital display technologies have enabled new and desirable form factors.

Content is king. Analog television became inexpensive because it served a huge content market: broadcast television. But things have changed. The emergence of commodity PCs, the Internet, digital cable and satellite TV, and consumer DVD have combined to establish a huge new universe of digital content. And, as the transition to digital broadcast television unfolds (SDTV and HDTV), virtually the entire display universe will have become natively digital.

With regard to quality, digital content has several advantages.

- Digital content can more effectively filter noise as illustrated by the lack of background hiss on an audio CD as compared to an analog cassette.
- Digital content enables digital manipulation of the content which means that you can effect highly specific enhancements. For example: shadow enhancement, sharpness control, and color manipulations commonly used in medical imaging.
- Digital content can be quickly and repeatedly replicated with precision and widely distributed much more efficiently than analog formats.

And then there is form factor. Without digital displays, products such as today's laptop computer would simply not be possible (remember the first Compaq CRT based portable PCs?). The same applies to wall mounted televisions, PDAs, seat back displays on airplanes, and the mini-displays on the back of digital cameras. The inherent flat panel nature of most digital display technologies is thus a key factor in their increasing success. These applications could not be fulfilled without them.

The Opening of Pandora's Box

While the emergence of digital display technologies has been a good thing, the developments behind them have been the equivalent of opening Pandora's Box. In the frantic rush to digitization, technologies have been invented and re-invented on a multi-dimensional scale across diverse geographies, industries, and suppliers. The result is a multitude of standards, formats, regulations, specifications, and derivatives, all of which makes your job ever more challenging.

To illustrate the complexity that we have wrought, I have compiled a representative list of technologies, formats, and standards introduced as part of the mass digital emergence, in Table 1.

Difficult Questions

While by no means complete, Table 1 nevertheless illustrates a foremost challenge facing you today: risk and complexity. Which are the correct features to support? How do they vary by market segment? How do they vary by geography? How are they evolving? How do you implement the mix of features you need quickly and efficiently? Can you effectively support a family of configurations to service multiple market segments? How do you get to market fast enough to gain market share?

Digital convergence is driving these technologies together, in new ways and in new products – and making that happen is your responsibility.

Unique Challenges of Digital Display Design

Beyond the complexity of their world, environment digital displays also present some unique challenges to you. These include achieving the performance required for the target application, correcting for technology-specific display characteristics, and generating the drive signals for the target display.

Performance is particularly challenging in digital video display applications due to the tremendous computational loads involved.

- You require a high-bandwidth connection from the source.
- You need to perform a complex string of operations on the data. These can include decryption from a secure transmission format, decoding into pixel maps, and optimization of these pixel maps for display.
- You must use the resulting data to generate the driver signals for the display.
- Finally the display driver generates a family of signals that will be distributed to drive each individual pixel. The format of these signals varies with each technology, they have exacting timing requirements, and their specifications are often unique to each and every model.

To make things worse this must all be achieved in real time, and while transiting this pipeline the dataflow will expand from about 25 Mbps (streaming HDTV) to 1.5 Gbps (raw uncompressed 1080i HDTV display data).

The optimization stage of the pipeline is a challenge in and of itself. Here the digital

Wired Connection Technologies	Broadband Access Technologies	Chip to Chip Technologies	LVDS Interconnect Technologies	Television Standards	Streaming Media Formats
IEEE 1394	ISDN	LVTTL	LVDS	NTSC	MPEG-1
USB 2.0	DSL	LVCMOS	LVPECL	PAL	MPEG-2
Ethernet	Cable	Chip to Memory Technologies	BLVDS	SECAM	MPEG-4
HomePNA	WCDMA	HSTL-I	PC Display Formats	SDTV 480i	MJPEG
HomePlug	Chip to	HSTL-III	EGA	SDTV 480p	Real Networks
Wireless Connection Technologies	Backplane Technologies	HSTL-IV	VGA	HDTV 720p	QuickTime
802.11b	5V PCI	SSTL-I	SVGA	HDTV 1080i	MS Media Player
802.11a	3.3V PCI	SSTL-II	XGA	Digital Imaging File Formats	Encryption Standards
HiperLAN2	3.3V PCI-X	SSTL2-I	SXGA	TIFF	DES
Bluetooth	GTL	SSTL2-II	UXGA	JPEG	3DES
HomeRF	GTL+	SSTL3-I	WXGA	Scitex	AES
	AGP	SSTL3-II		Targa	PKI
		CTT		GIF	

Table 1 - Standards and technologies spawned in the mass digital emergence

image data must be adapted to the specific characteristics of the target display technology. This is necessary because while all displays operate on similar principles of color science, each has its own specific (and non-linear) behavioral characteristics. Thus, RGB data (which is most typically targeted for a CRT display) must be processed to display with acceptable results on an LCD, PDP, or other display technology. This processing can be as simple as color correction, or much more involved with algorithms applied for scaling, contrast, brightness, gradation smoothing, edge sharpness, shadow enhancement, and so on. Almost anything is possible, it simply takes adequate processing power.

A Case Study

To illustrate the challenges of digital display design let's analyze a case study example for a digital projector. In the generic case such products traditionally accept analog RGB video input, perform some moderate processing on the data, and then drive the projection display. This is typically effected through a variety of analog (blue), digital (black), and control (green) components as illustrated in Figure 1.

With the advent of digital convergence, the next iteration of such a product may well be required to support some form, or forms, of direct digital input and include the ability to accept and display encoded file formats. In such a case, you face the dilemmas regarding which inputs and formats to support, and then you must select and integrate appropriate components to realize them in a design that meets performance requirements.

Figure 2 illustrates an example for such a design that would support a fast serial USB 2.0 connection as well as an 802.11 wireless LAN connection.

The simplicity of these illustrations belies the complexity of the task. How do you implement the new logic in the system controller to manage the new data flows? What interfaces and signaling standards are required in order to integrate the new components? What extensions to your user interface and control software need to be developed? And, if it is determined that you need to implement and support a variety of these technologies and options, your task becomes much more complex.

The Value of Programmable Logic

Programmable logic is an ideal solution for addressing these challenges. By their nature these devices are flexible – the premium requirement for success in this

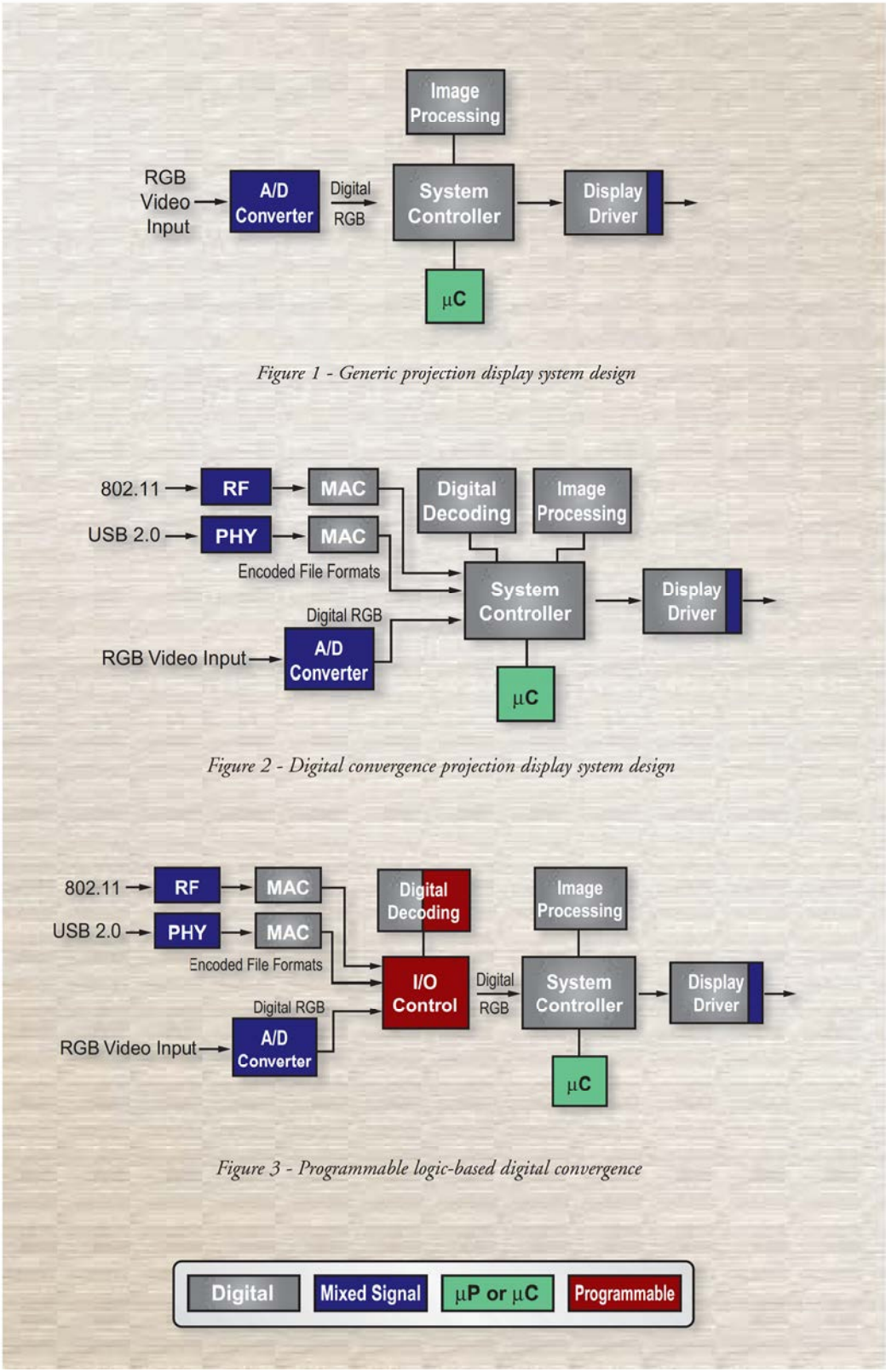


Figure 1 - Generic projection display system design

Figure 2 - Digital convergence projection display system design

Figure 3 - Programmable logic-based digital convergence

endeavor. In addition FPGAs are fast and efficient development platforms, enabling rapid development cycles. Finally, modern FPGAs are extremely cost effective, and therefore viable production solutions for almost any application.

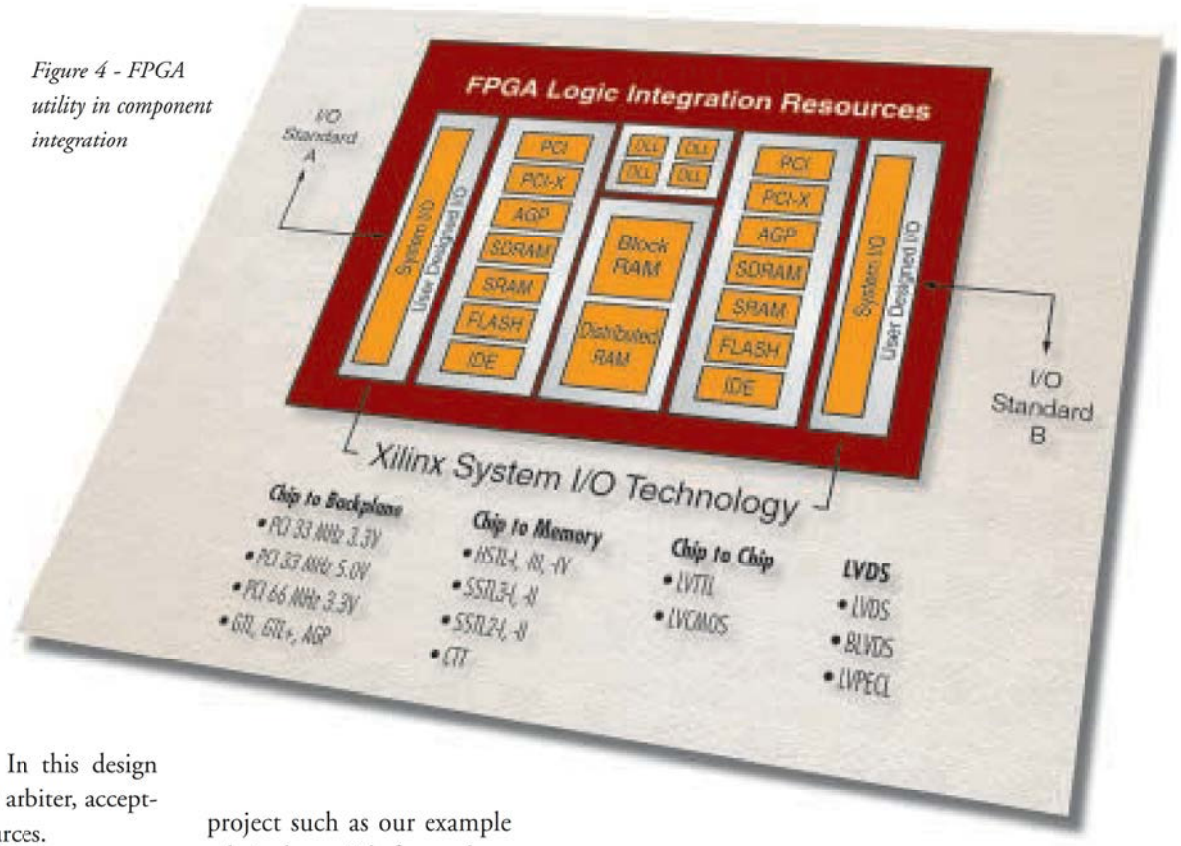


Figure 4 - FPGA utility in component integration

Figure 3 illustrates how an FPGA-based solution could be used to affect our digital convergence projector. As you can see this design inserts an FPGA (illustrated in red) and associated logic between the A/D converter and existing system controller. In this design the FPGA serves as the I/O arbiter, accepting input from all three sources.

In operation the legacy digital RGB signal is simply passed through when this connection is active. In the case of USB 2.0 and 802.11 however, the FPGA serves to manage these new interfaces completely, as well as decode the incoming data stream into the legacy digital RGB format. Decoding can be accomplished entirely in the FPGA or with the assistance of an ASIC or ASSP as appropriate (illustrated by the combined black/red block).

This approach has several important advantages.

- It retains the existing backend of the legacy design essentially unchanged. This bounds development complexity and reduces risk.
- The programmable bridge imposes no schedule penalties for numerous iterations. This can be a significant advantage when you are tasked with integrating new and unfamiliar technologies.
- Upon completion the design can be released and in production very quickly.

How is all this possible? Figure 4 illustrates some of the standard features and IP available in Xilinx FPGAs that make a project such as our example relatively straightforward.

On the perimeter of Figure 4 is System I/O, which allows each and every I/O pin to be programmed to support any of 17 different signaling standards. But System I/O doesn't stop there. In addition to the basic signaling parameters it supports programmable drive strength and multiple slew rates too. These features make it easy to deal with unanticipated PCB behaviors (in those not so rare cases where fabrication reality doesn't match design theory) as illustrated in Figure 5.

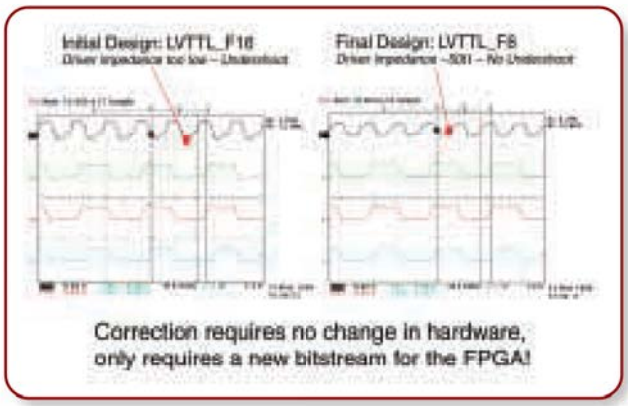


Figure 5 - The benefit of programmable drive strength in System I/O

Some FPGAs, such as the new Spartan™-IIE family from Xilinx, even go a step further including support for LVDS, BLVDS, and LVPECL differential signaling standards at up to 400 Mbps per pin pair. This enables very high-performance component interconnection without the need to resort to higher pin count and more expensive packaging. Further, it reduces system power, lowers EMI, and is much less sensitive to noise as illustrated in Figure 6.

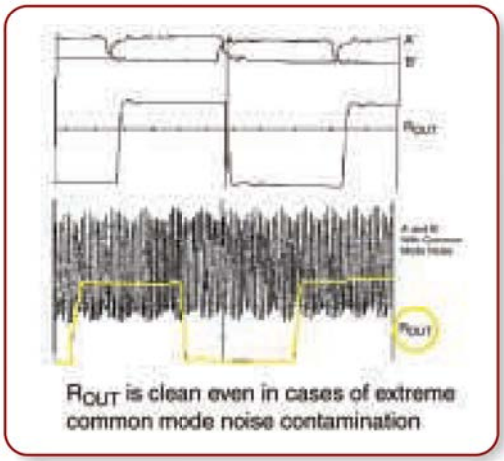


Figure 6 - Noise immunity benefit of LVDS signaling

Figure 4 also shows a representative sample of the standard controller IP modules available for FPGAs. These are commercial quality function blocks that are available to jump-start your design. Much can be accomplished with standard IP as solutions are available to address most of the topics listed in Table 1.

For buffers and FIFOs you have a variety of on-chip memory resources to choose from. These include 200 MHz flip-flops, true dual ported Block RAM, a Shift Register Mode (SRL16) capability in the FPGA's fabric Look-up Table (LUT) structures, and highly configurable Distributed RAM. These features provide high-performance and silicon-efficient solutions for almost any on-chip memory need.

For clock management Xilinx FPGAs feature four or more Delay-Locked Loops (DLL) per device. These provide the resources to synchronize and connect your system elements together and manage EMI. These DLLs exhibit superior noise immunity compared to PLLs, and they feature excellent jitter specifications, making your job easier. A few examples of their utility are illustrated in Figure 7.

Finally, an array of Configurable Logic Blocks (CLB) and internal interconnect resources tie everything together. These are illustrated in Figure 8 and are the underlying fabric that make an FPGA an FPGA.

The FPGA Way

While the benefits of programmable logic are obvious as illustrated in our example, its value can be even greater when leveraged as a foundation element in your design. Figure 9 illustrates how our digital convergence projector might look if it were designed from scratch, only this time the FPGA way.

In this design the flexibility of FPGAs is being leveraged to maximum advantage. By designing the core logic of the system controller into an FPGA component you gain maximum flexibility in the selection of every other component you require – be they HSTL, SSTL, LVTTL, LVDS, or whatever, they can be quickly and efficiently integrated.

Another advantage in our example is the modular architecture for system input. In this design we could support a family of configurations to address a variety of geographic and application requirements. Further, there is no reason why these cannot be developed in a serial fashion, enabling the most important configurations to get to market first. And, all that would change from configuration to configuration in the core design is the bitstream program in the FPGA.

With programmable logic in the data path you have tremendous ability to tailor encoding/decoding, encryption/decryption, and image processing functionality to your precise needs. More importantly, you also have the flexibility to keep up with changes as these needs evolve over time. Take file decryption for streaming media as an example. Today there are no firmly established standards, and the standards that do exist vary widely by geography and content provider. And remember, Content is king, and that using a programmable device as the decryption engine could allow you to support whatever your customers require both today and tomorrow.

When used as the heart of the display driver circuit, programmable logic can give your design the ability to support two or more display options. This can be of tremendous value in managing the cost for this high dollar bill of materials component (more than paying for the FPGA in many cases) or to support a family of products based upon a common core design that increases your accessible market. In addition, you can use LVDS to route these signals around the board (which quite often involves traversing large tracts of real estate) and thus minimize system level EMI and the impact of noise on these critical signals.

FPGAs are also well suited for crafting a unique and attractive user interface for your design. They are the very definition of GPIO (General Purpose I/O) and can implement microcontrollers (or even a PowerPC microprocessor) for supervisory control. In today's competitive markets the user interface can be one of the most effective ways to differentiate your prod-

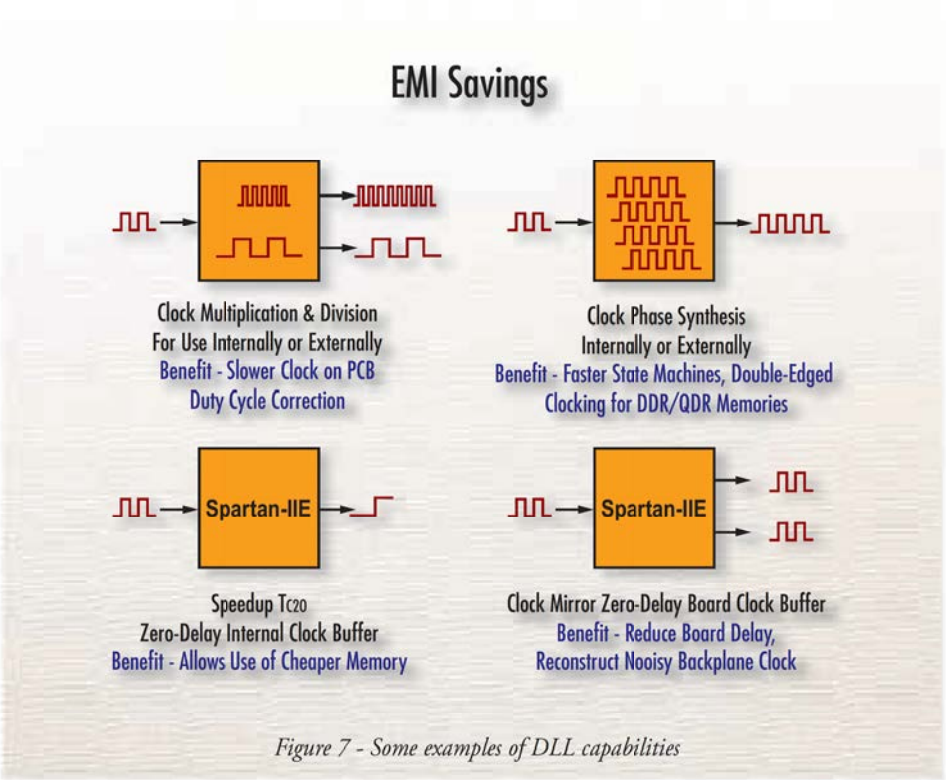


Figure 7 - Some examples of DLL capabilities

uct from that of your competition, and an FPGA gives you the maximum freedom to innovate.

Finally, your FPGA based solution is never frozen. If a customer comes to you requesting a new feature, a slightly different capability, or a new configuration, you have a platform to quickly and efficiently deliver it. When inevitable bugs and incompatibilities crop up you can not only fix them quickly, you can also update deployed systems in the field. This can greatly reduce support and service costs. And if you ever face a supply problem for a system component while in production, you have the flexibility to find and support an alternate solution to keep your factory running, your product shipping, and revenue coming in.

Conclusion

The era of digital convergence is upon us. From pictures to e-mail, from music to news, the world has gone digital. And because of this digital explosion today's systems require ever more connectivity and intelligence. It is no longer good enough to have the best widget or display. Now you need a more digitally connected and data manipulating widget or display, one that supports the standards and formats in your target market and geography – and one that does it before your competition.

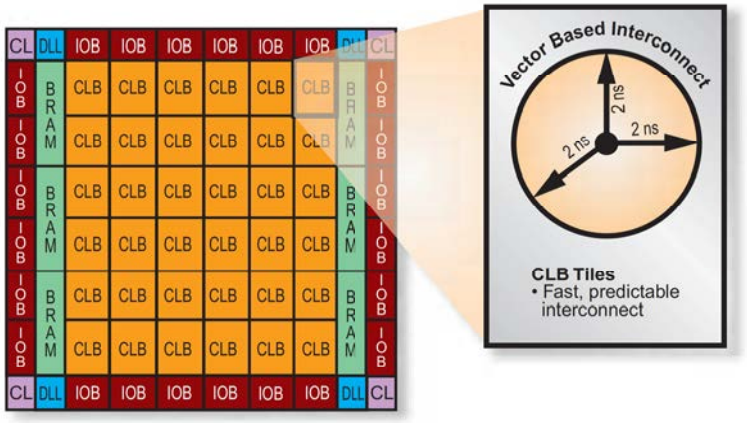


Figure 8 - FPGA CLBs and interconnect resources

Programmable logic is an invaluable asset in confronting this challenge. Its inherent flexibility makes it an ideal mechanism for grafting new functionality into an existing design. Its rich features, efficient development flow, and extensive IP support will simplify your job and give you a chance to meet aggressive schedules. The newest generations of devices are cost efficient solutions for almost any design. And when made a fundamental part of your architecture from the beginning, this technology can be exploited to modularize your configurations, provide flexibility with critical and costly components, and tailor your product functionality to your exact needs.

To learn more about digital video and digital convergence technologies, and how FPGAs can help with them, visit the Emerging Standards and Protocols (eSP) Web portal at *www.xilinx.com/esp*. This website was developed by Xilinx as a resource for the digital system design community and is specifically targeted at dealing with these new and challenging technologies. To date, segments have been deployed for home networking, Bluetooth, and digital video technologies, and more are on the way.

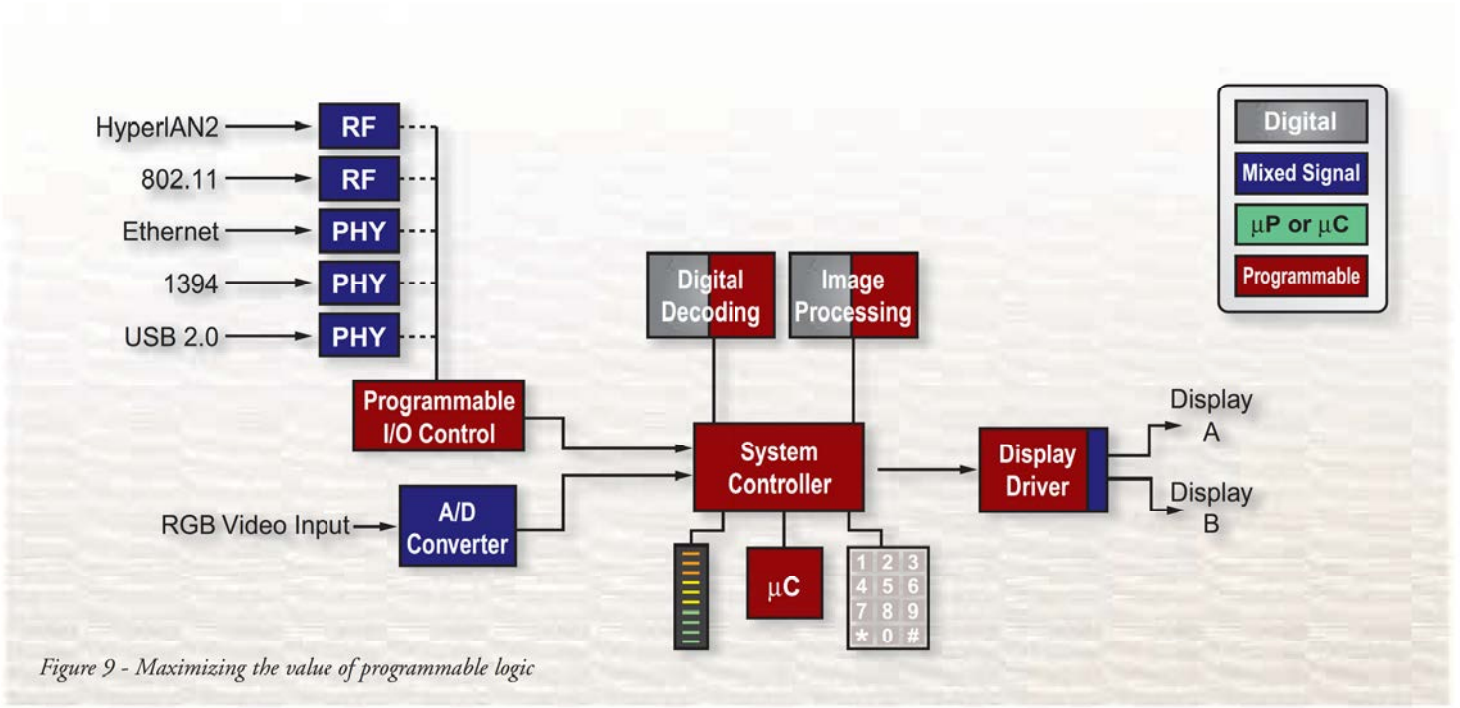
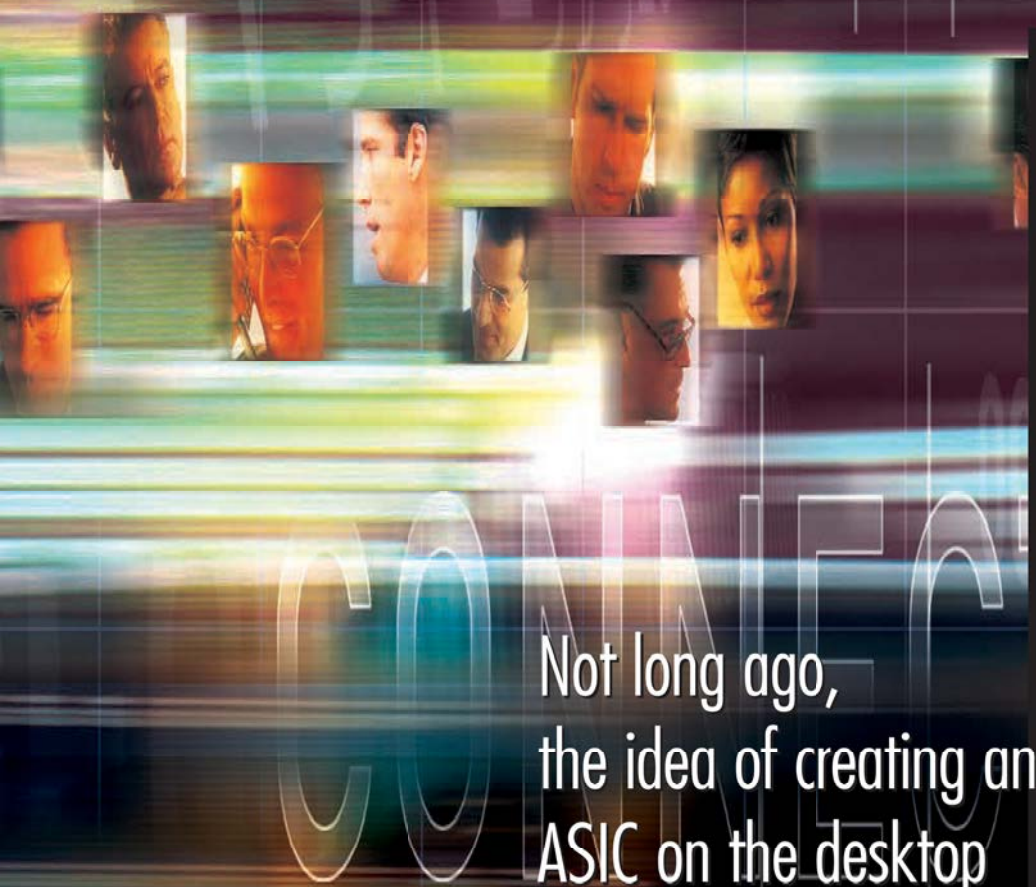


Figure 9 - Maximizing the value of programmable logic

Digital Consumer Convergence Demands Reprogrammability



Not long ago, the idea of creating an ASIC on the desktop was considered a novel concept.

by Robert Bielby
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Seventeen years ago, Xilinx developed the industry's first Field Programmable Gate Array (FPGA). The concept was quite simple – using Static Random Access Memory (SRAM) as the basis of the logic fabric, you could instantly develop integrated logic circuits directly on your desktop. The benefits were far reaching, because this technology did away with the risk and delay typically associated with designing custom Application Specific Integrated Circuits (ASICs).

While the concept of "user programmable" logic was perhaps first pioneered by enterprising engineers who used Programmable Read Only Memories (PROMs) as a "programmable ASIC", this solution was able to achieve only small levels of integration. The cost efficiency and logic density achieved by using PROMs as custom logic was extremely poor compared to ASICs. Interestingly, however, the concept of using look-up tables to implement logic functions is actually a basic technology used in today's multi-million gate FPGAs.

Today, FPGAs have evolved into a mainstream technology because their current densities and performance compete with custom ASICs. Additionally, designing for an FPGA is almost exactly the same as an ASIC – your circuit can be described either by schematic, or by a high-level hardware description language such as VHDL or Verilog. This description is then synthesized for the FPGA with the final result being a configuration bitstream that ultimately programs device look-up tables that are interconnected by programmable wires. Just like the look-up tables, the configuration bitstream also determines the connectivity for the programmable wires.

Because the programmability is based upon volatile, SRAM technology, there is a requirement to "re-write" the configuration bit stream every time power is removed and re-applied to the FPGA. This configuration bit stream is usually contained in an external, memory which is dedicated for configuration, or by reserving a portion of a main system memory with the FPGA configuration information.

When FPGAs were first introduced, the fact that they required programming from an external memory source, and that they lost their configuration once power was removed, was generally considered a liability. Fixed ASICs had none of these requirements or added complexities. And for the most part, ASICs were still significantly cheaper than FPGAs – at least on a unit cost basis.

However, for applications that shipped a relatively low number of units, it could be shown that the high non-recurring charges for the ASIC more than offset the higher unit costs of the FPGA. Because of these cost constraints, the use of FPGAs was historically relegated to the lower volume, less cost sensitive applications that had large-scale integration requirements.

Over time, the additional benefits of being first to market and the ability to fix bugs or accommodate late specification changes rose in importance, and the decision to select an FPGA over an ASIC became common. This proved to be true even in cases where it could be demonstrated that an ASIC solution provided a lower overall solution cost than the FPGA. However, there were practical limits to how great the unit volumes or disparity in price would become before a design would transition from FPGA to ASIC.

These fundamental benefits of being first to market and of risk aversion have proven to be especially important to the networking and communications industries – as demonstrated by the fact that currently 70% of the $5 billion market for programmable logic is consumed by networking and communications applications. FPGAs have been particularly important in these markets because they have been able to keep up with the pace and innovation in those markets and accommodate the wide range of new standards that continuously emerge.

Flexibility for the Masses

Moore's Law, which says that transistor density of an ASIC will double every 18 months due to advances in semiconductor technology, has played a key role in driving larger density FPGAs with greater features and performance. This has in turn continued to fuel the increased demand and consumption of FPGAs in networking and communications applications.

The advances in semiconductor technology have not only yielded larger and faster FPGAs, they have also yielded FPGAs that are 10,000% cheaper than they were five years ago! The result is that FPGAs, which were previously practical only for prototyping or low volume, high-end applications, are now appearing in some of the hottest, newest high-volume consumer electronics.

Four years ago, Xilinx developed the Spartan series family of FPGAs that were optimized for low-cost, high-volume applications. The results are impressive; from MP3 players, to DVD writers, digital cameras, digital modems, and a host of other consumer electronics – FPGAs have rapidly become a key driver behind the digital consumer revolution.

And reprogrammability, which used to be considered a liability, is now clearly seen as a key benefit in not only getting a product to market sooner, but keeping it longer in the market by providing the ability to upgrade it and add new features once it's in the field. But how and why programmable logic is being used is sometimes just as interesting as where it's being used.

ReplayTV – Personal Video Recorder

Personal video recorders (PVRs) are perhaps one of the most exciting consumer products to offer new features and capabilities made possible only by the combination of digital technologies and FPGAs. With a PVR, traditional analog video programming is converted to digital using MPEG 2 encoding and stored directly to

a hard drive – enabling instant search access and high quality video imaging.

PVRs represent a quantum leap in capability and quality compared to traditional videocassette recorders (VCRs). For example, a PVR such as ReplayTV's can store as much as 60 hours of programming, allowing viewers to watch programming on their personal schedules instead of those set by broadcasters.

The ReplayTV also contains an integrated 56K-baud modem, which is used to download the equivalent of a TV guide that can be searched, sorted, and grouped like traditional database programs. This allows for easy recording setup and unique programming search capabilities. This modem connection also enables additional unique capabilities – such as reconfig-

uring the FPGA. The reprogrammable logic is updated simply by downloading a new bitstream. If the unit is already installed in a customer's home, the bitstream is downloaded from ReplayTV's Internet server. This allows bugs to be fixed even after the customer takes the unit home, and lets ReplayTV add new features as necessary. Obviously, this extends the life of the product too, because rather than having to replace it as market requirements change; the customer simply has the unit's logic reprogrammed via the modem.

ReplayTV reprogramming takes place in the background: each evening the PVR automatically downloads TV schedule information from the company server, along with any bug fixes, operating system updates, or program modifications. The customer's unit is improved as he sleeps without intervention on his part. End users are typically never made aware of changes or fixes to their systems unless the functionality of the PVR changes as new features are added.

In one case, ReplayTV found itself forced to deal with a condition that caused degraded video quality in a few systems already in homes – one of the chips in the system had an undocumented clock threshold switching problem that varied as a function of lot processing. Because the control signals for this device were generated in the FPGA, it was possible to eliminate the problem by changing the timing of the FPGA-generated signal.

The company responded with a software change that was uploaded to all ReplayTV systems in the field as soon as it was debugged and certified. Most customers never realized that the change had been made; though some may have noticed improved video quality. A revolutionary capability enabled by FPGA programmable technology!

KB Gear – JAMCAM 3.0 Digital Camera

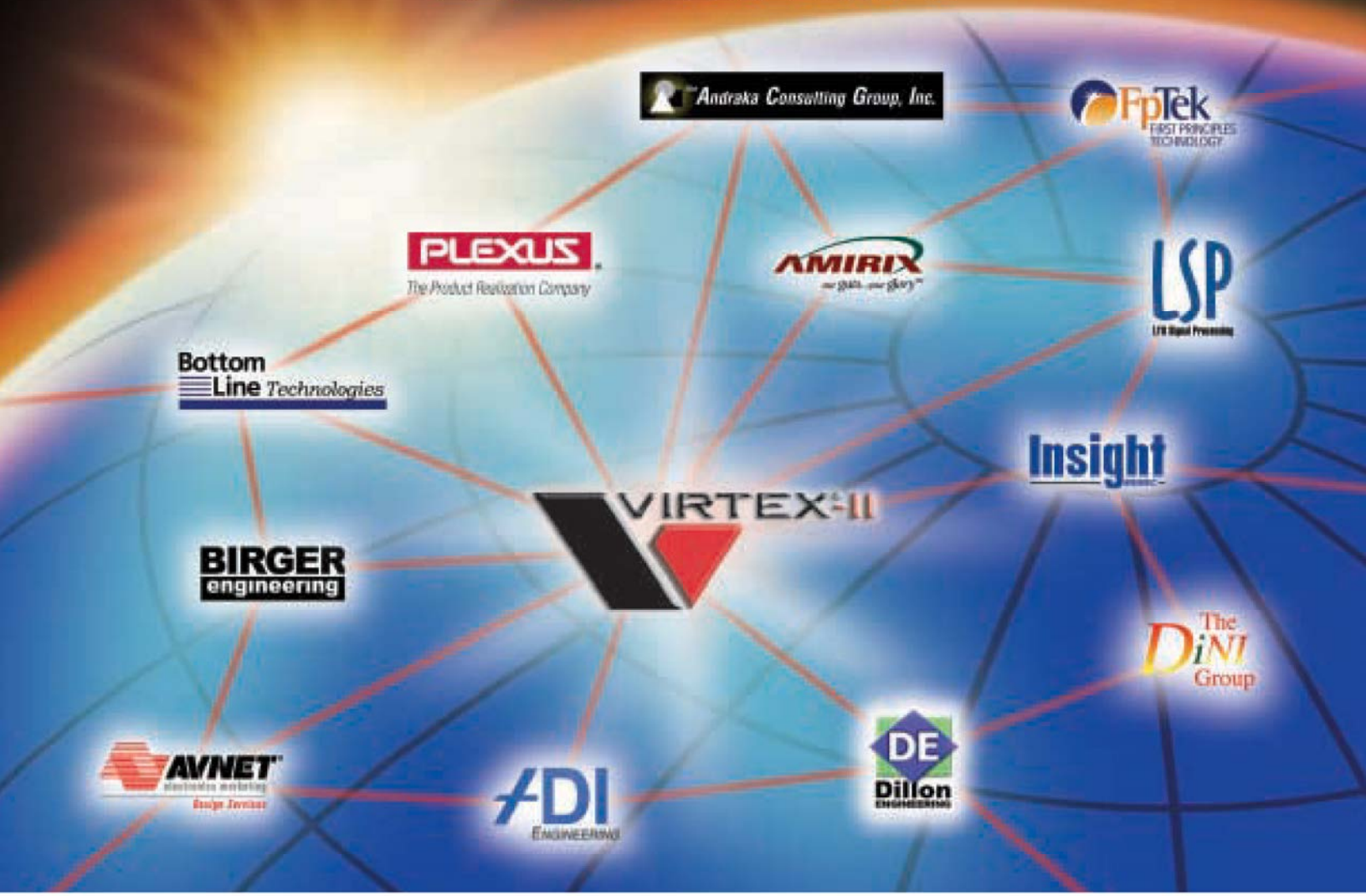
Perhaps one of the least likely places one would expect to find an FPGA would be in a toy digital camera. But time to market pressures and the risk of missing the narrow Christmas window of opportunity drove KB Gear Interactive, a manufacturer of Internet communications products and interactive gear for young computer trekkers, to chose the low cost Spartan™ FPGA because of its affordability and design flexibility.

As a testament to the viability of FPGAs in such a cost sensitive consumer product – the JAMCAM 3.0, which cost just $99, was sold in over 14,000 retail outlets including Best Buy, Target, K-Mart, WalMart, Circuit City, and a host of other highly recognizable consumer retail outlets. Because KB Gear had designed a toy that had broad appeal and used a Spartan FPGA, they were able to deliver one of the "must have" toys for the 2000 Christmas season on the shelves in time for the Christmas season. Years ago, the thoughts of an FPGA in a $99 kid's toy would have seemed impossible.

Conclusion

Seventeen years ago the idea of creating an ASIC on the desktop was considered a novel concept; they were primarily limited to prototyping and low volume production. The fact that the FPGAs needed to be programmed every time they were powered up was considered both a liability and a risk. Today, because of their lower cost and high flexibility, FPGAs have found a home in a wide range of applications. Xilinx FPGAs are now used in a wide range of high-volume, cost sensitive applications, especially those that require reprogrammability to meet the continuously changing standards and demands of the new digital consumer markets.

For High-Speed Design, You're Better Connected With Xilinx.



SystemIO Through our XPERTS program, Xilinx certifies many 3rd party design centers specializing in terabit applications. By taking advantage of industry-unique features such as the SelectI/O™-Ultra technology in the Virtex®-II Platform FPGA, Xilinx and its XPERTS partners provide the fastest and most flexible high-bandwith solution supporting rapidly evolving connectivity standards.

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Using Virtex-II 840 Mbps LVDS performance and an abundance of memory and logic resources, Xilinx is able to provide solutions for 10GE MAC, PCI & PCI-X, RapidIO, POS-PHY Level 3 and 4, Flexbus 4, HyperTransport, and other source-synchronous bus standards.

With SystemIO and our XPERTS program, you're better connected with Xilinx.

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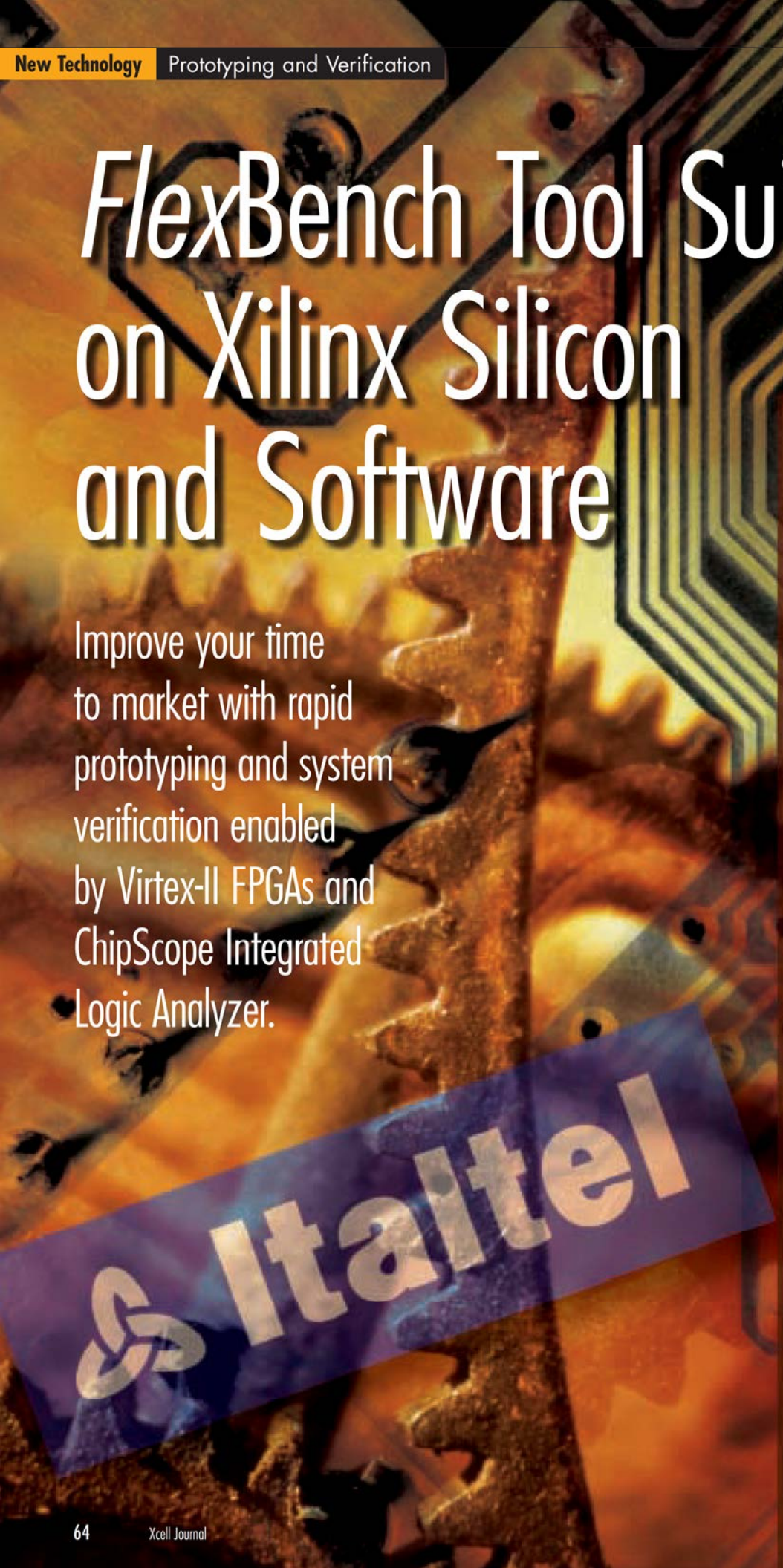
*Flex*Bench Tool Suite Relies on Xilinx Silicon and Software

Improve your time to market with rapid prototyping and system verification enabled by Virtex-II FPGAs and ChipScope Integrated Logic Analyzer.



by Marco Pavesi
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System verification is the major bottleneck in the development of contemporary and future system-on-a-chip (SoC) designs. Increasing numbers of applications that process large quantities of data in real time (such as telecom and video) require verification techniques that run at or near real-time speeds. Delaying your software development until working devices are available is not a viable option in the face of enormous competitive time-to-market pressures.

Thus, early hardware/software (HW/SW) co-verification is not just practical – it's essential. At Italtel SpA, we and our partners have developed a superior method of improving system verification confidence through high-speed register transfer level (RTL) prototyping and the Virtex™ family of FPGAs.

Prototyping at Real Time Speeds

RTL prototyping allows you to run system hardware and software at speeds high enough to hunt and find hidden bugs. Just as important, you can confidently evaluate subjective characteristics, such as audio and video quality.

RTL prototyping uses off-the-shelf FPGAs to implement SoC custom logic, as well as test physical, real devices like memories, interfaces, and processors that comprise the other parts of the system to be verified. This strategy enables us to create, in effect, a clone of the SoC and all the parts of system that it interfaces with. We call this

assembling a "demonstrator." With a demonstrator, we can map the hardware and run the application software. RTL prototyping can be roughly divided in two types, custom and modular:

- Custom prototyping is the fastest technique, in terms of frequency. FPGAs and other devices are assembled on a board expressly designed for the demonstrator to be verified. Such a demonstrator may reach speeds as high as 200 MHz – but it requires several months from initial system design to the end of the verification process because of the intrinsic delay of the board fabrication process.
- Modular prototyping is not quite as fast as custom prototyping for verification – but when it comes to giving you the time-to-market advantage, it is, by far, the better solution. With modular prototyping, you can assemble FPGAs and other devices on general-purpose daughterboards that allow you to create a wide range of different demonstrators. Modular prototyping is a HW/SW co-development scheme based on a set of configurable carrier boards where daughterboards can be inserted and interconnected as necessary during the co-design process.

Avoiding the FPIC Dead End

Modular RTL prototyping platforms have intrinsic speed limitations related to modularity, accessibility, and routability. Field programmable interconnect chips (FPICs) have been the traditional solution for routability problems. Unfortunately, the existing technology trends for FPICs are insignificant (in terms of speed and the number of I/Os) compared to the skyrocketing speed and size of Virtex-II and Virtex-II PRO™ FPGAs. In short, no modular rapid prototyping platform based on FPIC technology can meet your customers' need for speed and time to market.

To approach real-time system speeds, a modular rapid prototyping tool with new interconnection technologies and a novel topology had to be developed. Such a tool – with single-ended, point-to-point signals – would have a physical speed limit ranging from 80 MHz to 100 MHz.

Figure 1 - Co-verification solution: Italtel FlexBench hardware with Temento Diaflex software

Given these parameters, three European companies collaborated for two years to design and develop the *Flex*Bench™ modular rapid prototyping tool suite:

- Italtel SpA, the largest Italian telecom manufacturer, is the leader for hardware development.
- Mistel SpA, another Italian telecom manufacturer, supports the hardware effort.
- Temento Systems, based in France, is dedicating its electronic test automation (ETA) software resources to the testing of SoCs and electronic boards.

Moreover, Oktet Ltd., a design service company based in St. Petersburg, Russia, was also deeply involved in the development the *Flex*Bench verification system.

Putting Together *Flex*Bench Hardware

As the *Flex*Bench project leader, I had been searching for a practical means of modular rapid prototyping in a HW/SW co-design environment. In 1999, two new technologies emerged that enabled our team to create and patent the *Flex*Bench concept:

1. QuickSwitch™ bus switches from Integrated Device Technology (IDT), Inc.
2. Mictor™ high-speed connectors from Tyco Electronics.

These two technological innovations gave our team the means of reconfiguring multiple printed circuit boards (PCBs) as needed during the HW/SW co-design process. Employing the reliable and fast-growing Xilinx FPGA technology, we envisaged it was possible to design the unique *Flex*Bench HW/SW tool suite.

The *Flex*Bench challenge was to create a rapid prototyping tool so general in purpose as to become the industry standard. Taking such a concept and turning it into a high-powered tool, however, is quite an undertaking that requires strategic alliances and adequate funding.

We applied for – and received – start-up funding from the European Commission. With that funding, we worked in a frenetic manner for two years to gather the expertise and to execute the rapid prototyping tool we envisioned.

At the hardware level, the *Flex*Bench rapid prototyping platform was to be basically a set of complex board designs. Fortunately, we had the PCB know-how and related resources in-house at Italtel – and valuable contributions from Mistel.

On the software side, the development of the computer assisted engineering (CAE) software we needed was not our area of competency. Therefore, we entered into a partnership with Temento Systems, a company known for its excellent ETA software. Temento developed the DiaFlex™ software tool we needed to monitor the *Flex*Bench system in action. See Figure 1.

Our acquisition of Certify™ RTL partitioning software from industry-leading Synplicity™ Inc. completed our primary software tool set.

Now that we had the boards and the software, we had to find the best programmable logic devices. It was a short search. In a class by themselves, Virtex-II Platform FPGAs from Xilinx perfectly fit the needs of our verification engineers: high speed, fast and simple compilation, and high capacity.

You can see the *Flex*Bench design chain in Figure 2.

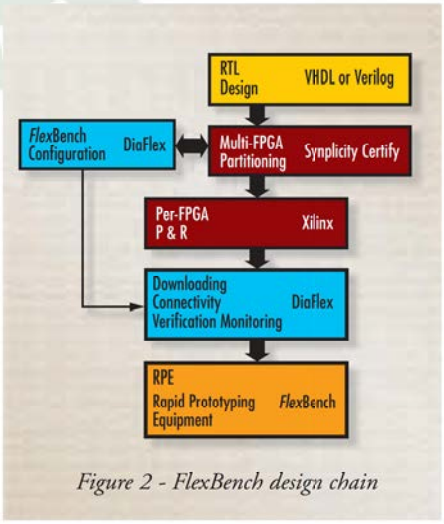

Figure 2 - FlexBench design chain

*Flex*Bench Rapid Prototyping at 100 MHz

As we said earlier, to achieve the speed edge in RTL prototyping with a modular tool, the FPIC approach is simply not suitable. A novel technology had to be introduced, based on the speed of IDT's QuickSwitch bus switches. By using pass-transistors, you can select interconnections among neighboring HW modules on multipurpose panels.

We built QuickSwitch bus switches and receptacles into the *Flex*Bench motherboards, which are populated by daughterboards named FlexPlugs. These modules are based on an open standard form factor. Using advanced, off-the-shelf interconnect technology, FlexPlug modules make available up to 888 functional signals. FlexPlugs host active devices, such as the leading edge Virtex-II 6000 Platform FPGA. The FlexPlugs also host power converters. Memories are allocated on small modules, named MiniPlugs, directly inserted into FlexPlugs in order to minimize interconnect delays.

We obtained the *Flex*Bench speed characteristics by interconnecting different FlexPlug modules through the distributed network of pass-transistors. Each side of a FlexPlug contacts the side of the nearest other FlexPlugs by means of channels. Channel size is configurable, through the JTAG port, from 0 to 222 functional wires with 8-bit granularity. Trace length minimization is achieved through a clever three-dimensional architecture.

The relatively short trace length of QuickSwitch delays (0.1 nanosecond) and the best-in-class set-up and clock-to-output parameters of Virtex-II FPGAs permits us to achieve 100 MHz clock speed (and over) on modular systems populated by up to 18 FPGAs.

The *Flex*Bench rapid prototyping equipment (RPE) is composed of a rack, a backplane (FlexPanel), a software-controlled clock generator (FlexClock), some carrier boards (FlexMothers), and several modules (FlexPlugs and MiniPlugs). FlexMother boards are connected through flexible printed circuits (FlexCable) and through the FlexPanel. See Figure 3 to see how the whole Flex hardware family interacts to form the *Flex*Bench verification system. Figure 4 shows a populated FlexMother.

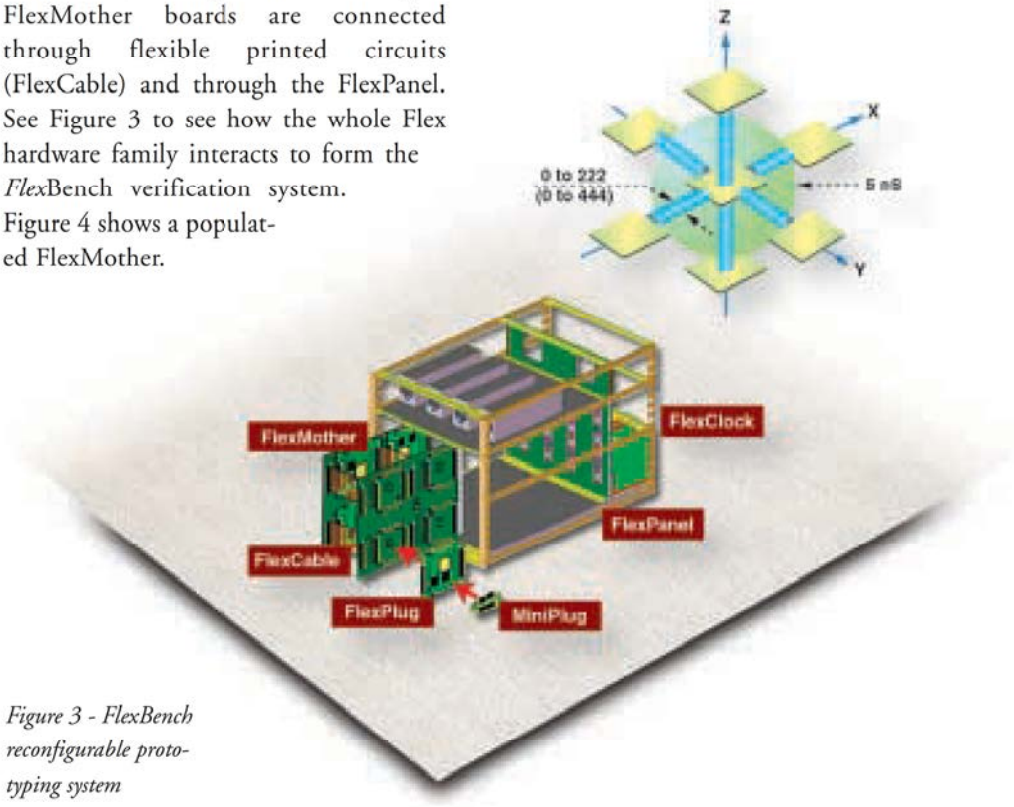

Figure 3 - FlexBench reconfigurable prototyping system

Integrating DiaFlex Software

Complementing the *Flex*Bench hardware is the DiaFlex software tool developed by Temento Systems. Dedicated to configuring, downloading, verifying, and controlling the *Flex*Bench RPE, the DiaFlex program suite allows you to design the RPE configuration through an intuitive, three-dimensional graphical user interface. Starting from RPE configuration, the DiaFlex application generates a flattened description of the platform definition into a Verilog format, called a VB

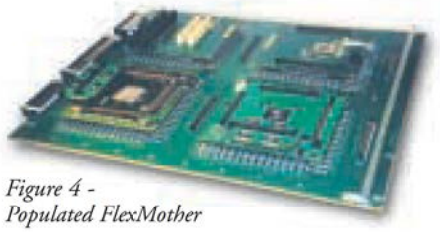

Figure 4 - Populated FlexMother

file. The VB file provides the Certify verification software with an easy view of the RPE resources and connectivity. Moreover, it provides direct channel configuration bitstreams .

The Certify program compiles RTL code, and spreads it according to the VB file description of the RPE. The Certify tool also

synthesizes all FPGAs. The FPGAs are then placed-and-routed via proprietary tools to produce FPGA configuration bitstreams.

The DiaFlex application downloads all bitstreams to the RPE and provides interactive debugging through a TemTag™ JTAG PCI board. Moreover, the DiaFlex software provides diagnostics, reports errors, and analyzes test results. This allows debugging at the signal name level, functional testing, and automatic management of IEEE 1149.1 test bench generation. Additionally, the DiaFlex program takes complete control of the FlexClock board. This enables you to configure FlexClock parameters: the frequency of clock synthesizers, the selection of global clock sources, and the control of other timing functions.

A Flexible Prototyping Library

To perform effective rapid prototyping, you must have a set of FlexPlugs and MiniPlugs. These plugs enable you to interconnect state-of-the-art FPGAs, memories, I/Os, processors, design platforms, and other components of your design.

While Italtel and our affiliates have designed general-purpose *Flex*Bench modules, design-specific modules must developed by final OEM customer. This is where the services of a company like Oktet Systems can become essential.

Sixteen general-purpose modules currently comprise the *Flex*Bench library. Some of the modules are displayed in Figure 5.

A Matter of Observability

Compared with the "observability" you can get with emulators, the classic argument against rapid prototyping has been that you can't "see" what's going on inside the design, because invasive physical probing is difficult, if not impossible, to accomplish in modular equipment.

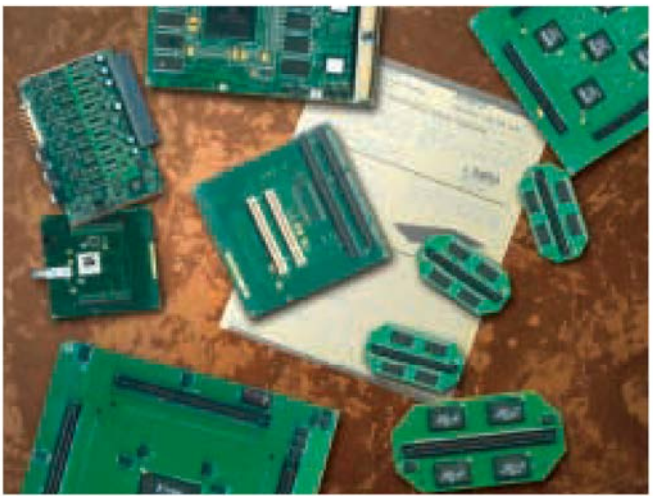

Figure 5 - FlexBench library

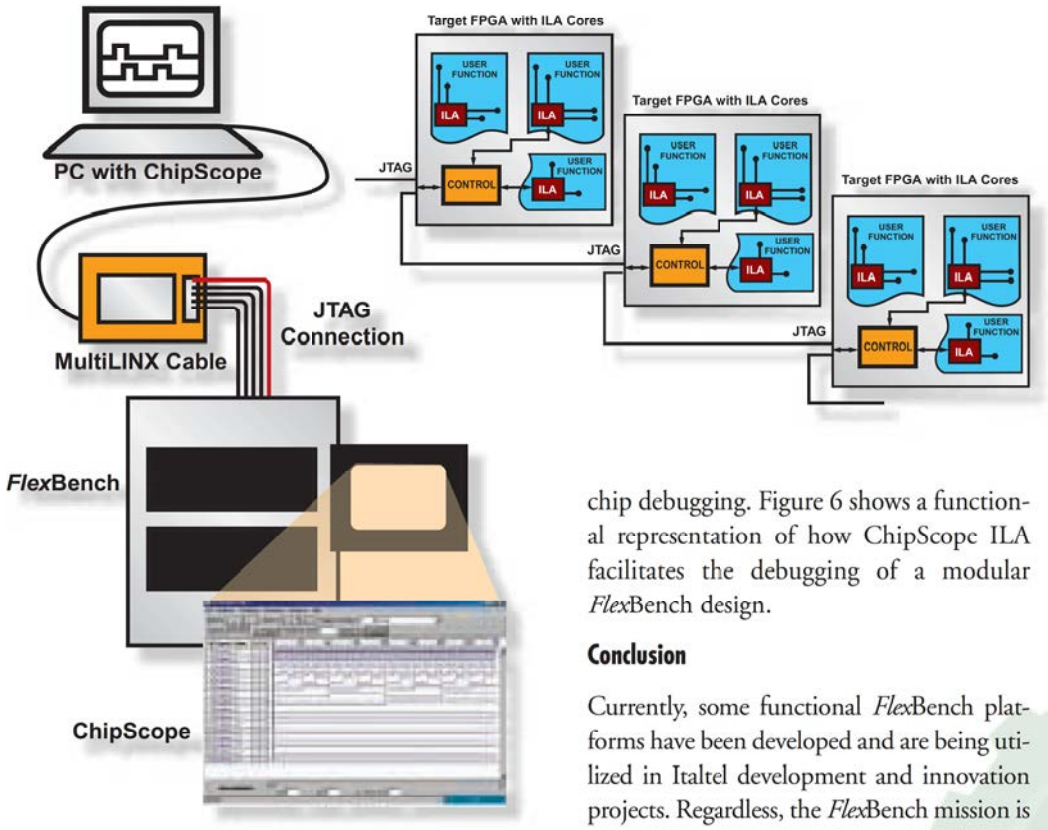

Figure 6 - ChipScope and FlexBench solution

Xilinx has removed this weakness thanks to its Integrated Logic Analysis (ILA) core, a solution that provides trigger and trace capture capability within the FPGA itself. Implemented by the Xilinx ChipScope™ Analyzer, the ILA core allows real-time access to any node in the *Flex*Bench chips. An easy-to-use graphical user interface provides the same functional controls of a sophisticated logic analyzer. With ChipScope ILA, you spend less time verifying chip functionality, and therefore, speed up your time to market.

By means of the ChipScope ILA, you get full visibility into the *Flex*Bench RPE. ChipScope ILA lets you see every selected node in every FPGA used in your design. This virtually eliminates the need for invasive physical probing of the *Flex*Bench RPE. With the Xilinx ChipScope ILA solution, you can perform real-time, on-chip debugging. Figure 6 shows a functional representation of how ChipScope ILA facilitates the debugging of a modular *Flex*Bench design.

Conclusion

Currently, some functional *Flex*Bench platforms have been developed and are being utilized in Italtel development and innovation projects. Regardless, the *Flex*Bench mission is not to become a proprietary tool, but to become an industrial standard.

Italtel/Temento are and will be engaged in trials with major silicon vendors to demonstrate and to prove the *Flex*Bench technology. We believe the versatile *Flex*Bench model is a major step in rapid prototyping and system verification. We are proud to have designed it. To ensure best diffusion of this tool, we are now researching the best sales channel.

Multiprotocol Modular Engineering Solutions Platform Offers Design Flexibility and Faster Time to Market

The Nu Horizons Engineering Solutions Platform presents a cost-effective alternative to single-board tools for developing high-end data communication and server applications.

Virtex-II daughtercard

by Bill Pratt
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Today's one-sided trend toward shorter system development cycles and increasingly complex designs are driving the need for more timely system validation. Although designers recognize this weighted ratio, and are turning more and more to Xilinx FPGAs for their designs, they have also recognized a need for development boards that are up to the challenge.

Nu Horizons Electronics Corp. understands this short-cycle/high-complexity design ratio and has introduced a line of hardware development platform tools that facilitate system verification within an integrated environment. The Nu Horizons Engineering Solutions Platforms are based on a modular design concept that allows the re-use of expansion cards with other interface expansion cards to create a unique development evaluation environment.

Modular Design Solution

The Engineering Solutions Platform solution consists of up to three boards in a modular environment. With this modularity, you may combine a number of different expansion cards for multiple solutions, or you can build a total solution in a modular environment. The days of purchasing a development board for a single application are gone.

Engineering Support Platform motherboard

Motherboard

The primary function of the Engineering Solutions Platform motherboard is to provide a high-speed backplane for board-to-board data transfers. This backplane is called the Horizon Bus. With the high-density board-to-board connectors, you can evaluate the functions of two expansion cards, which allows emulation of a total solution. The Horizon Bus has an aggregate bandwidth of 26 Gbps, and is highly suited for developing solutions for the telecommunications and data network markets.

The main board, or motherboard (Figure 1), has the following features:

- Xilinx XCR3128XL -10PQ VQ100 CoolRunner™ CPLD
- High-density board-to-board connectors for two expansion cards
- Dual seven-segment LCD display
- RS-232 level shifter for UART core instantiation
- JTAG configuration headers
- Two 44-pin PLCC sockets for Xilinx configuration PROMs
- Fifty test points
- Power management
- Reset controller
- Status LEDs.

Virtex-II Expansion Card

The Xilinx Virtex™-II expansion card (Figure 2) is a cost-effective development board with a broad suite of features. Available now is the XC2V1000 FG456 one-million-gate Virtex-II device with the following features as implemented on the Engineering Solutions Platform daughtercard:

- 16 channels of LVDS interface
  - – User-configurable as eight transmit and eight receive or 16 transmit channels
- Multiprotocol serial clock/data transceivers with auto cable termination
  - – Certified TBR-1, TBR-2, NET-1, and NET-2 compliant.
- 16 megabits of synchronous NBT SRAM
  - – Flow through and pipelined
- Programmable clock from 1 MHz to 200 MHz
- Six user clock inputs
- High speed 133-bit at 200 MHz backplane
- DCI (digitally controlled impedance).

Design Platform for High-End Applications

Targeted at high-end data communications applications, the Virtex-II daughtercard is applicable to many scenarios, including SPI-3 to CSIX bus interface or offering transparency within high-end networking solutions. The 16 channels of high-performance LVDS (low voltage differential signaling) provide the capability to prototype high-speed differential interfaces such as the SPI-3 and SPI-4 bus technologies. The Receive port includes parallel termination; the Transmit side does not require this feature.

The multiprotocol clock/data transceivers with auto cable termination can support multiple protocols such as two channels of V.35 HDLC (high-level data link control). Coupled with the HDLC core from Xilinx, you can turn your Virtex-II FPGA into a powerful network engine. The multiprotocol clock/data transceivers also support X.21, V.11, RS-232, RS-449, and RS-53W\ serial interfaces.

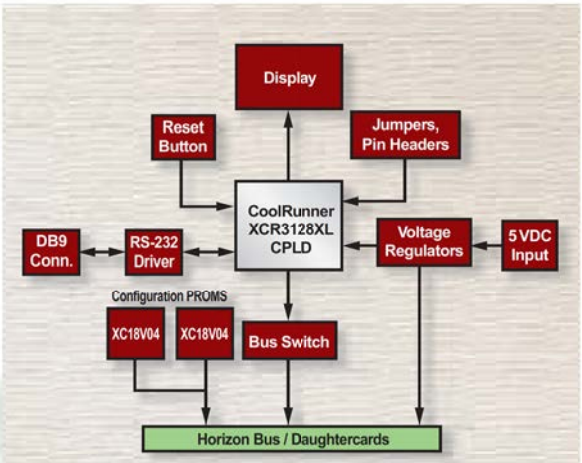

Figure 1 - ESP motherboard block diagram

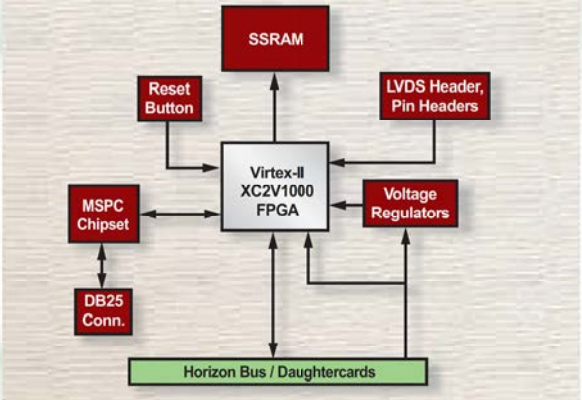

Figure 2 - Virtex-II daughtercard block diagram

NBT (no bus turnaround) RAM offers a standard packaging for high-speed SSRAM devices. The Virtex-II daughtercard has 16 MB of NBT SSRAM from GSI Technology, which allows for zero-wait, read-write bus utilization. This GSI SSRAM is programmable as FT (flow through) or pipelined, operating as a pipelined synchronous device. This means that in addition to the rising-edge triggered registers that capture input signals, the device incorporates a rising-edge triggered output register.

The daughtercard also incorporates an ICS525-02 user-configurable clock chip from Integrated Circuit Systems Inc. The ICS525-02 is the most flexible way to generate a wide range of highly accurate clock output from a standard crystal or clock oscillator. You can easily program the ICS525-02 to output a frequency from 1 MHz to 200 MHz by setting a bank of switches located on the board. You may also supply a LVDS clock, as well as four other single-ended user supplied clocks, for a total of six usable clock inputs.

With the Horizon Bus backplane, the Virtex-II daughtercard becomes a very powerful development platform offering up to 26 Gbps throughput and allowing the instantiation of a multitude of bus architectures, such as CSIX for telecommunications.

Nu Horizons Electronics Corp. is in the process of developing new daughtercards for the Engineering Solutions Platform. Future cards include an HTML server/white appliance controller and a high-speed AFE (analog front end) with an Ethernet interface.

Conclusion

The Engineering Solutions Platform from Nu Horizons Electronics Corp. is a modular Virtex-II development environment that provides designers with the hardware necessary to develop, prototype, verify, and test their designs before they are finalized. Intended to accelerate the design cycle timeline, the Engineering Solutions Platform is a modular solution that enhances and simplifies system design and validation processes. Its modularity makes it highly functional over many design cycles, thus providing a cost-effective alternative to single-board tools for developing high-end data communication and server applications. The Engineering Solutions Platform motherboard with the Virtex-II daughtercard sells for $999 and is available for immediate shipment. For more information, please log onto *www.nuhorizons.com.*

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Join Synplicity at Programmable World 2002, and attend our upcoming webcast seminar featuring Synplicity's Amplify Physical Optimizer and Xilinx® Virtex-II Pro™. Details at www.synplicity.com/events/xilinx_events.html

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Parallel Cable IV Connects Faster and Better

This new high-speed download cable supports ultra-low voltages.

by Theresa Vu
Product Marketing Engineer
Xilinx, Inc.
theresa.vu@xilinx.com

The new Parallel Cable IV downloads data more than 10X faster than the previous JTAG/Parallel Cable III. Now, you can download to one XC2V8000 Virtex™-II FPGA in less than eight seconds.

The PCIV features ultra low-voltage support for all Xilinx FPGA, CPLD, System ACE™ MPM (multi-package module), and ISP (in-system programmable) PROM devices (see Table 1).

The PCIV connects to any desktop or laptop computer using the standard IEEE 1284-compliant parallel port and draws power directly from the computer (through the mouse/keyboard port) or an external power supply.

A robust ribbon cable ships with the PCIV, which gives you the flexibility to use either the JTAG (IEEE 1149.1) or Slave Serial download mode at the fastest speeds. The small profile of the ribbon cable connector minimizes the need for board space. The ribbon cable offers an error-free, quick connect target interface compared to cumbersome flying lead wires of Parallel Cable III.

The PCIV is backward compatible with the PC III and offers a connector for flying lead wires.

PCIV extends Xilinx leadership in pre-engineered configuration solutions by offering a fast, simple, low-cost download solution for all Xilinx FGPA, CPLD, System ACE MPM, and ISP PROM devices. The Parallel Cable IV will be available in late March through Xilinx distributors and the Xilinx e-commerce site for $95. For more information, see *www.xilinx.com/support/programr/cables.htm.*

	Parallel Cable IV	Parallel Cable III
Download Speed	up to 4 Mbps	up to 300 Kbps
I/O Voltage Support	1.5V, 1.8V, 2.5V, 3.3V, 5V	2.5V, 3.3V, 5V
Download Modes	JTAG (IEEE 1149.1) and Slave Serial	JTAG (IEEE 1149.1) and Slave Serial
Power Supply	PC or External Power Supply	Target System
Board Connections	Ribbon Cable and Flying Wires	Flying Wires
Software Support	iMPACT	iMPACT

Table 1 - Parallel Cable IV vs. Parallel Cable III

Parallel Cable IV connected to PC

Parallel Cable IV connected to external power supply

Parallel Cable IV with ribbon cable connector

scc-*II* Microsequencer – A New Solution for Platform FPGA Designs

When your project design is too big for a finite state machine, but a microcontroller would be overkill, try Ponderosa Design's scc-*II* microsequencer.

by Aki Niimura
Consultant
Ponderosa Design
ponderosa_design@pacbell.net

As the complexity of FPGA-based systems grows every year, we are asked to implement larger, more complex functionality within tighter schedules. Furthermore, the type of design has changed rapidly in recent years. People used to design an FPGA taking an existing board design, often containing asynchronous clocks. Those days are over. You can not design today's Platform FPGA just by extending yesterday's design practices. New designs often require the implementation of complex sequences or communication protocols. The finite state machine (FSM) is a well-known design methodology to implement such sequences. FSM is very effective when the sequence is not very complex. However, implementing a complex sequence using an FSM is not practical and is often difficult to maintain.

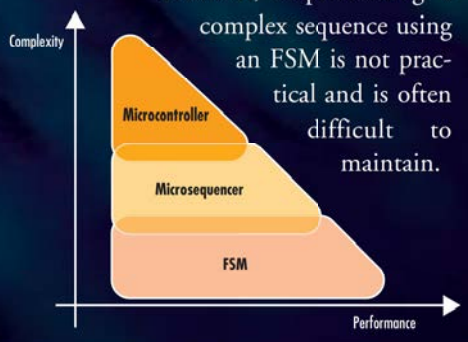

Figure 1 - Performance versus functional complexity

Microcontrollers are commonly used to implement complex protocols. However, they require substantial resources (memory, cost, pins, ...), which can be difficult to justify in real-life situations. On the other hand, software implementations allow designers to cope with mounting logic complexity. They are easy and quick to implement and easier to maintain.

There is a gap, however, between the range of design complexity that FSM methodology can handle and what microcontroller-based methodology is good for, as shown in Figure 1. As microcontrollers become more powerful, the gap is widening.

The scc-*II* is not just another set of microcontrollers. We specifically constructed the microsequencer to fill the gap between low-level FSM solutions and high-level microcontroller designs.

scc-*II* – A Configurable Microsequencer

Sequencers have been used in many LSI projects to implement functions. For example, instructions in a CISC (Complex Instruction Set Computer) CPU were often implemented in this way (called microcode, which is written in a proprietary assembly language). By allowing users to write programs in a high-level language, the scc-*II* can accommodate a wider range of FPGA applications.

The key architectural benefits of the scc-*II* are:

- Small footprint
- High-level language support
- Small code size
- Configurable and customizable
- Capable of handling 16-bit and 32-bit data types
- Timer (integrated into the core architecture)
- Support of interrupt handling
- Developing and debugging tools
- Utilization of Xilinx Spartan™-II and Virtex™-II devices.

A block diagram of the scc-*II* is shown in Figure 2. The core itself requires 400 to 600 LUTs, depending on the configuration and synthesis constraints.

How the scc-*II* Works

The scc-*II* employs a stack-based architecture. Stack computers use data stacks to evaluate given operations (Figure 3). The benefits of stack-based architecture are:

- High-level language ready – can execute syntax tree directly
- Simple hardware – easy to understand, easy to customize
- Small instruction code – most scc-*II* instructions are one byte long.

Another unique aspect of the scc-*II* architecture is the use of register windows. Register windows are used to pass arguments to a function being called. Because the scc-*II* does not use a stack frame in memory to pass arguments, the scc-*II* does not require data memory to run a high-level language program, thus making the scc-*II* more attractive for Platform FPGA applications.

Programs for the scc-*II* are almost entirely written in the high-level language SC.

The Language SC

The scc-*II* assumes the use of a high-level language. However, existing high-level languages are not designed for microsequencer applications. Therefore, we developed a stripped-down version of C language – SC. SC programs do not support "struct" and other complex data types, but SC has several enhancements to describe control applications efficiently. Timer, I/O, and debug features are natively supported in SC.

The following is a code fragment from a project that controls an SDRAM memory.

```
void
init_sdram()
{
   while(!eval_cond(DLL_RDY)) { }    // wait for DLL is ready

   wait(14);      // 286 uS
   outp(SDCMD, SD_PRE);
   repeat(8) {
    outp(SDCMD, SD_AREF);          // looping takes 7 cycles
   }          // tRC = 84nS; 20nS * 5
   outp(SDCMD, SD_MODE);
}
```

In the above code fragment, eval_cond(n), wait(n), and outp(port) are not function calls, but they are natively supported by SC. Note that the loop counter of the repeat statement is placed in the data stack and not in the register file.

scc-*II* Target Applications

The scc-*II* can be used in designing functional blocks to perform procedural control. For example, flow charts or simple arithmetic functions (such as averaging) are good candidates for implementation by the scc-*II*.

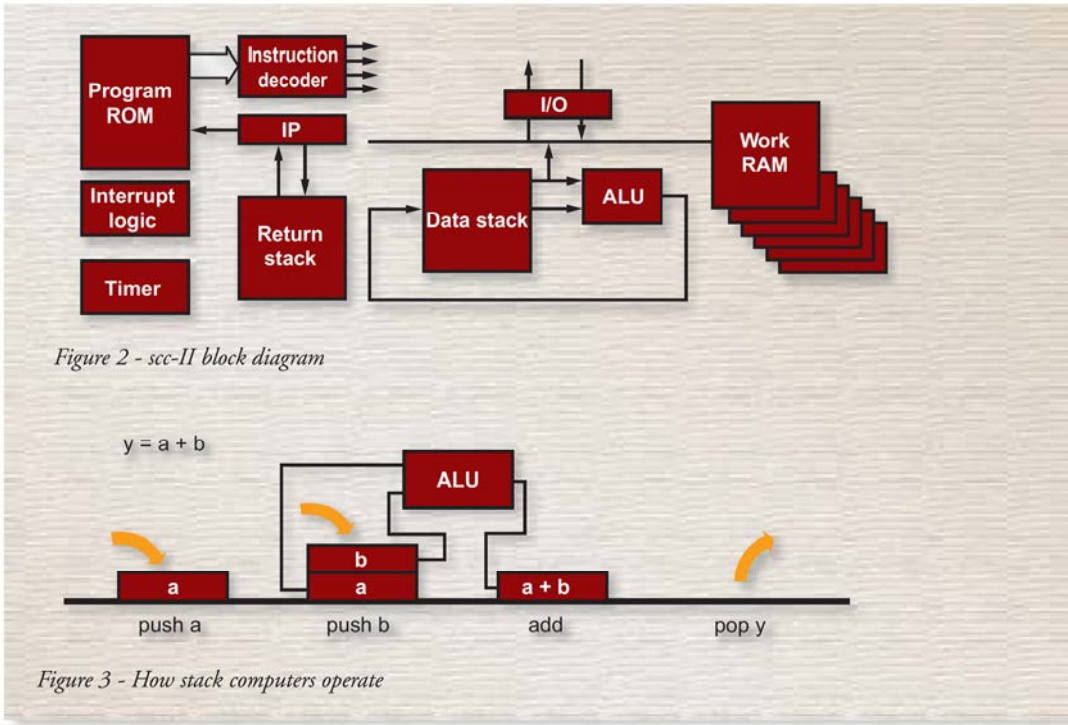

Figure 2 - scc-II block diagram

Figure 3 - How stack computers operate

Other target applications include:

- Read/write flash, EEPROM, 1-Wire™ devices
- Interface to I2C, RS-232, Ethernet, USB1.1, IrDA
- Command interpreter (a block is controlled through commands)
- User interface (such as keypad, LCD, touch panel)
- Servo controller (some arithmetic operations required)
- Design that requires many variants.

The scc-*II* and Virtex FPGAs

The Virtex family of FPGAs are true "system on a chip" platforms. The advanced technology available in Virtex-II devices provides further attractive features to the scc-*II*, including:

- The scc-*II* can run at 70 MHz or faster.
- Larger Block RAM allows larger program sizes (up to 8 KW).
- Native multiply operators are supported.

Case Study – Web on FPGA

To demonstrate the effectiveness of the scc-*II* solution, we have developed a Web server that uses less than 25% of the resources of a Spartan-II FPGA (XC2S150). The only additional hardware required beside the FPGA are an Ethernet PHY device and a signature ROM (optional). We found that the Spartan-II VoIP Development Kit from Insight Electronics *(www.insight-electronics.com)* included all the hardware components we needed. Thus, we decided to use this off-the-shelf board to create our Web server design. Figure 4 shows a screenshot from a Web server proj-

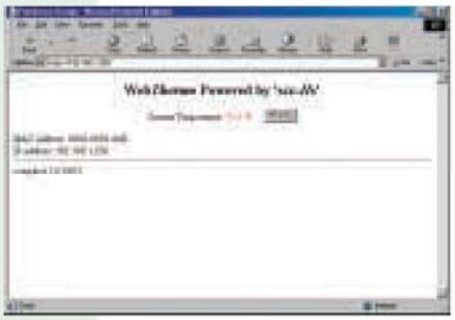

Figure 4 - WebThermo demo application

ect called WebThermo. The screen displays the current temperature every minute. Table 1 shows utilization statistics from a Synplify analysis of the XC2S150 device.

WebThermo	Usage of XC2S150	Note
LUTs	828 (23%)	Synplify 7.0
Block RAM	8 of 12	3 for TX, RX buffer, 5 for Program
BUFTs	320 (18%)	

Table 1 - WebThermo logic size

The 2 KB WebThermo program implements all Ethernet, TCP/IP, and Web (HTTP) protocols, as well as Celsius-to-Fahrenheit conversion. At start up, the program retrieves a unique 48-bit ID code from a Dallas 1-Wire device (DS18S20), which is used as an Ethernet MAC address. For further details on the WebThermo project, please visit home.pacbell.net/akineko/.

Program Development

One challenge of the scc-*II* solution is in providing reasonable program development and debugging tools. Figure 5 illustrates a typical program development flow. In addition to key software tools, we wrote many scripts and templates to automate the design process. While creating several projects with the scc-*II*, we refined the RTL design, as well as the development software and scripts. As a result, they have become mature and stable.

Currently the development environment is supported under Unix. It is also possible to port some of the tools to Windows platform using Cygwin from Cygnus (RedHat). The tools are developed assuming that the user's RTL design is in Verilog HDL.

Debugging, Then Debugging Again

Debugging is the biggest challenge in developing an scc-*II* based design. We are providing several debugging aids:

1. **Debugging starts with simulation:**
   - Three debug instructions (print, $dump, $stop)
   - Self-checking embedded in the code
   - Execution trace log generation
   - Dis-assembler to display current context (on-the-fly/offline)
2. **Ready to try on the board:**
   - JTAG debugger to download program without backend (synthesis + PAR)
   - UART customized for debugging (one can use printf())
   - "xdl" script to replace ROM contents without backend.

Lessons learned:

1. Logic simulation is always the best tool for debugging.
2. printf() is a primitive but very powerful means for debugging.
3. Use #ifdef ... #else ... #endif to switch between debug and release.
4. A bigger vehicle is needed for debugging (you may need 2 KB to develop a 1 KB program).

JTAG debugger

The JTAG debugger (jtagdbg) has proved to be a powerful tool to facilitate the debugging process. The JTAG debugger uses the Virtex USER1 JTAG command to communicate with a Virtex FPGA. By substituting the instruction ROM block in the scc-*II* design with a JTAG embedded ROM block, you can perform several debug commands, such as downloading a program without going through the FPGA backend design process. No signal change is required, as JTAG signals are hidden from your RTL code.

Conclusion

We have presented a microsequencer, the scc-*II*, which is new to conventional FPGA design practices. Unlike other IP cores, the potential of the scc-*II* is not limited to its original form. Rather, the scc-*II* can evolve to meet each application challenge. One avenue we plan to explore is adding Galois instructions to the original scc-*II* core. This enhancement can help in error correction or security applications.

Another avenue we plan to pursue is project automation, such as a wizard script that sets up project directories and tools – and then creates a skeleton version of RTL code, as well as skeleton SC program and header files.

The complete scc-*II* design solution is offered by Ponderosa Design in Sunnyvale, California Please write *ponderosa_design@pacbell.net* or visit *http://home.pacbell.net/akineko/*.

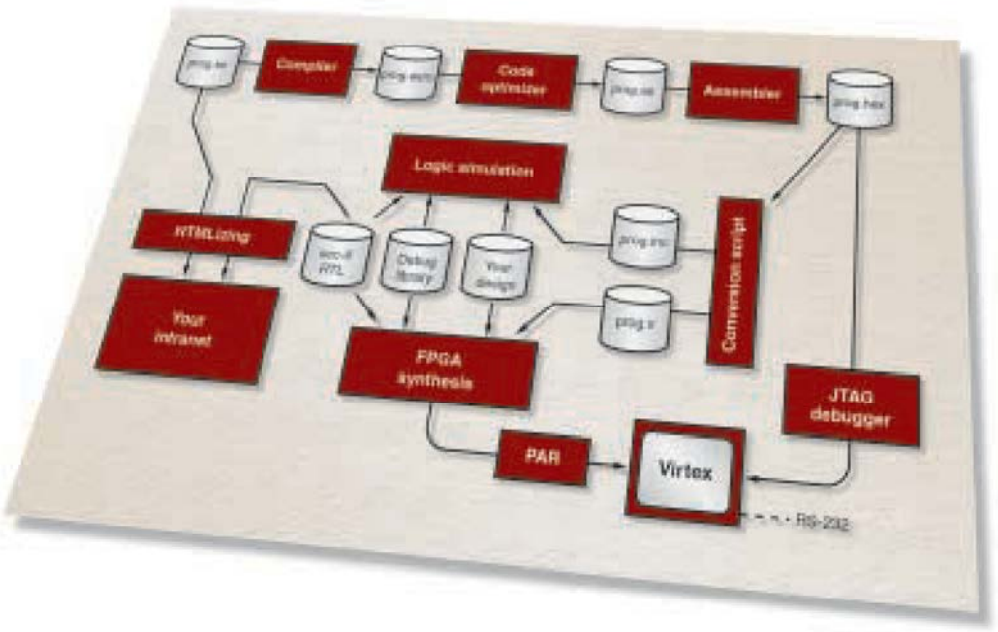

Figure 5 - The scc-II program development flow

Upgrade to Synopsys FPGA Compiler II Synthesis Tool to Maximize Virtex-II Pro Performance

FPGA Compiler II's unique algorithms aid in designing chips correctly and on time.

by Jackie Patterson
Director of Marketing Programs
Synopsys, Inc.
jackiep@synopsys.com

When you target Virtex-II Pro™ Platform FPGA, you are using one of the best FPGAs on the market – and you need a high-performance synthesis tool to match. That's why Synopsys Inc. is focusing efforts on its premier FPGA Compiler II™ FPGA synthesis tool and continuing to hone its support for top-of-the-line programmable logic devices. In 2002, FPGA Compiler II is superceding FPGA Express™, which will be discontinued.

This article will explain the differences between the two synthesis tools, summarize key features carried forward from FPGA Express to the FPGA Compiler II, and explain how you can upgrade to FPGA Compiler II today.

FPGA Compiler II Has Unique Capabilities

FPGA Compiler II (FCII) was developed for high-performance devices such as Virtex-II Pro Platform FPGAs. FCII combines the architecture-specific synthesis engine of FPGA Express with advanced technologies suitable for ASIC-like design challenges, as shown in Figure 1. These leading-edge capabilities are unique to FPGA Compiler II and not found in any other synthesis tools on the market.

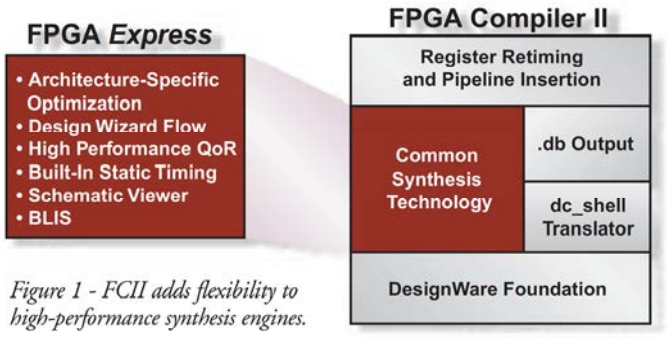

Figure 1 - FCII adds flexibility to high-performance synthesis engines.

Register Retiming

FCII uses sophisticated retiming algorithms to boost clock speed automatically. Retiming works by analyzing all the combinational logic in the design, and then selecting the optimal register placement to meet your design goals. See Figure 2.

Retiming can also pipeline your design automatically. Just code in the number of register banks to match your latency requirements, and FCII does the rest, moving the registers into the optimal position to form your pipeline.

Register retiming is easy to use in FCII. All you have to do is set the retiming variable in your script, and FCII will automatically position your registers in the optimal places to maximize clock speed.

```
current_chip my_chip
set_chip_retiming -enable
```

You can also use the FCII graphical interface to invoke retiming, if you prefer. Just select Edit->Constraints from the menu and check the retiming box in the Xilinx vendor options tab. Synopsys full-chip retiming optimizes performance of all datapath, control, and random logic in the high end of the Xilinx line – the Virtex™, Virtex-II, and Virtex-II Pro families of devices.

DesignWare Foundation IP Library

ASIC designers save design time by reusing components from the Synopsys DesignWare Foundation IP library. Although some components in the library are also useful for production FPGA designs, the biggest benefits come for those who are using a Virtex-II Pro device

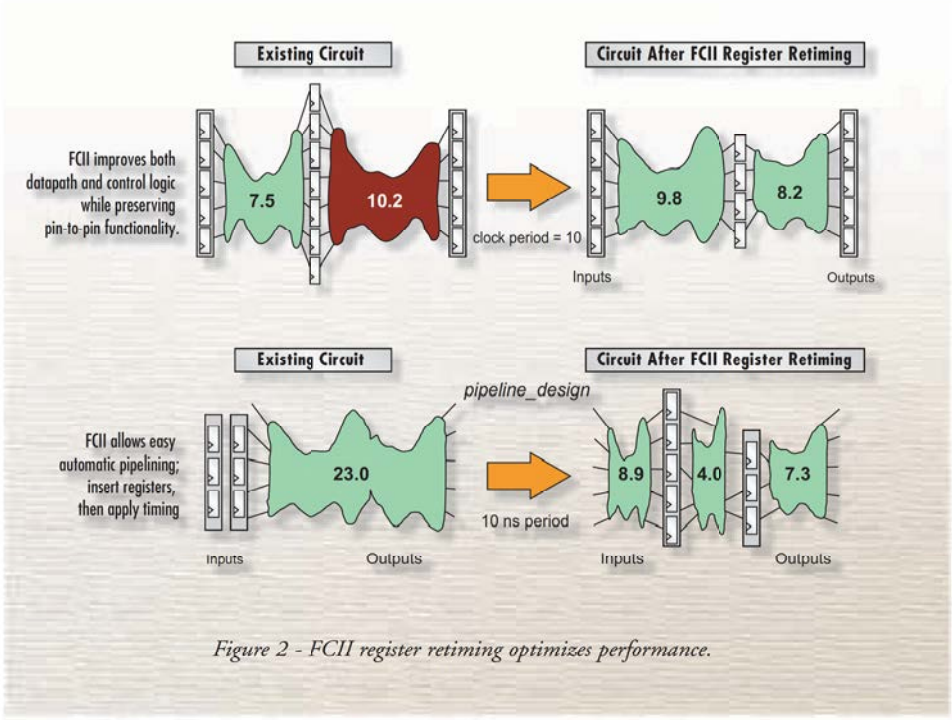

Figure 2 - FCII register retiming optimizes performance.

to prototype an ASIC or SOC. For a prototype, FCII's ability to implement the DesignWare components in the FPGA provides confidence that the ASIC will work as planned, because it allows you to verify exactly the same IP that is used in the ASIC.

Full Flow Support

FPGA Compiler II allows designers to take advantage of other high-performance tools for FPGA design and verification. When undertaking large, complex Virtex-II Pro devices, designers need to verify the silicon before it gets into the lab. That process starts with a quick analysis of the source code using the LEDA® HDL checker. The LEDA checker leverages general-purpose rules along with Xilinx-specific rules to alert designers to potential problems and optimization opportunities in the HDL. Then the HDL functionality is verified using a fast simulator such as VCS™ for Verilog or Scirocco™ for VHDL. After the optimization by FPGA Compiler II, designers can use Formality® to formally verify the design, avoiding time-consuming simulation runs. Of course, the timing of the design is comprehensively checked through static timing analysis. In this way, Synopsys FCII customers can leverage all available means to get their designs done correctly and on time.

Architecture-Specific Synthesis Engine

FPGA Compiler II carries forward the same architecture-specific synthesis engine you've relied on in FPGA Express. This includes:

- Support for all Xilinx devices through Virtex-II Pro and beyond
- Block Level Incremental Synthesis (BLIS) to speed your design cycle time by re-doing only the blocks in the design that have changed
- User control of register duplication to eliminate critical paths caused by high fan-out nets
- Networked licenses on both UNIX and PC
- Integrated schematic viewing and timing analysis
- Full TCL scripting
- ROM inference.

Upgrading to FPGA Compiler II

FPGA Compiler II is the choice for synthesis of high-performance FPGAs such as the Virtex-II Pro pf1.

To upgrade to FPGA Compiler II, contact your Synopsys account manager or visit *www.synopsys.com/fpga.*

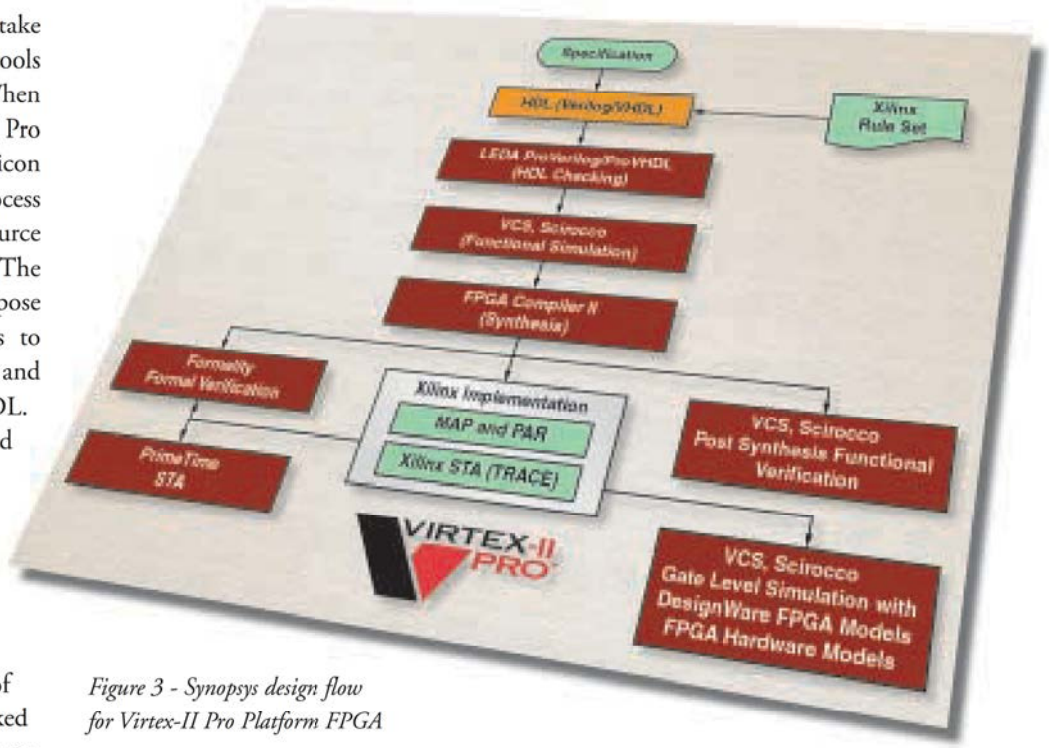

Figure 3 - Synopsys design flow for Virtex-II Pro Platform FPGA

Use Rocket I/O Multi-Gigabit Transceivers to Double Your FPGA Bandwidth

Virtex-II Pro Platform FPGAs break open the I/O bottleneck.

by Brian Von Herzen, Ph.D.
CEO, Rapid Prototypes, Inc.
a member of Xilinx XPERTS Program –
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Brian@FPGA.com

As FPGAs increase in size and performance, I/O resources become the main bottleneck to FPGA performance. Although the effective area of a chip grows as the square of the feature size, the perimeter I/Os grow only linearly. State of the art designs require higher performance I/O modules.

In response to this increasing demand on I/O resources, Xilinx has developed novel I/O structures called Rocket I/O™ multi-gigabit transceivers (MGTs) that enable order-of-magnitude increases in I/O performance. The Rocket I/O MGTs double the total I/O bandwidth of the Virtex-II Pro™ family of devices using only a few percent of the pins.

With up to 16 MGTs per device, the Virtex-II Pro achieves an additional 100 gigabits per second of I/O bandwidth in the larger devices over what is available with the general-purpose I/O blocks. Rocket I/O MGTs enable multiple gigabit I/O standards and maximize performance for FPGA-to-FPGA communications. Even though Rocket I/O MGTs dramatically increase performance for demanding applications, they are easy enough to use for simple FPGA-to-FPGA communications with special soft macros such as the Aurora core available from Xilinx. The interface has been simplified to the extent that no external resistive termination is required with the Rocket I/O MGTs. The transceivers can be internally configured to match 50Ω or 75Ω transmission lines.

MGTs Onboard

The Rocket I/O MGTs are shown in Figure 1, which illustrates the overall Virtex-II Pro architecture. The MGTs are located above and below columns of Block RAM, providing close availability of Block RAMs for ingress and egress FIFOs. As many as 16 MGTs are integrated on each FPGA above and below the Block RAM columns. The clock distribution networks can feed these transceivers for low-skew clock alignment between MGTs.

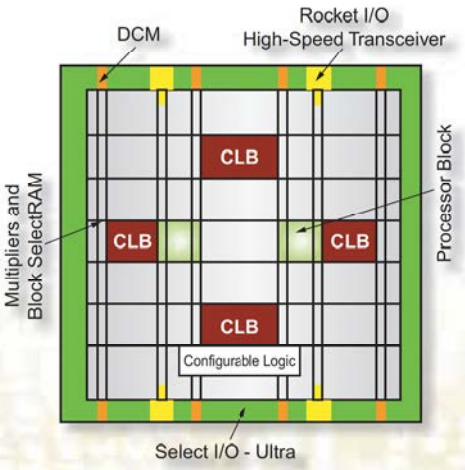


Figure 1 - Virtex-II Pro FPGA architecture, including up to 16 Rocket I/O MGTs

MGTs = Multiple Gigabit Standards

The Rocket I/O MGTs have been designed to be compliant with:

- Gigabit Ethernet
- 10 Gigabit Ethernet XAUI
- Fibre Channel
- InfiniBand™ Architecture
- Xilinx Aurora core

Configurable hardware support is provided for:

- 8B/10B encoding
- Disparity control
- Transmitter and receiver termination impedance
- Pre-emphasis
- Amplitude control
- Loopback testing.

These are the essential configurable hardware features that enable compliance with all of the main multi-gigabit signaling standards. You can find more information on Virtex-II Pro standards support on the Xilinx website at www.xilinx.com/partinfo/databook.htm.

MGTs Speed up FPGA Communications

Although MGTs have many important applications interfacing to industry standard gigabit communications protocols, they can serve another important function in boosting the bandwidth available among FPGAs.

Figure 2 shows a data communications application requiring two FPGAs. For a typical implementation, half of the I/O bandwidth is allocated to external links and half to the inter-FPGA link. With 800 general-purpose I/O pins available, running at a typical speed of 250 MHz, the pair of FPGAs can support a pipeline throughput of 100 gigabits per second.

If the 16 bidirectional MGT links are added, 16 links x 3.125 gigabits are available in each direction, for another 100 gigabits per second total. Figure 3 shows

Figure 2 - FPGA processing pipeline using general purpose I/O (GPIO) only

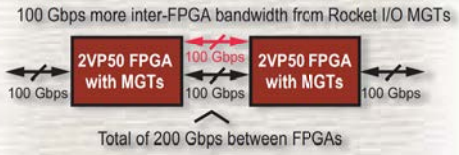


Figure 3 - FPGA processing pipeline using Rocket I/O multi-gigabit transceivers and general purpose I/O (GPIO)

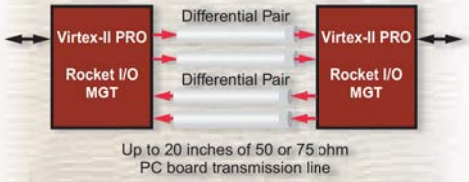


Figure 4 - Rocket I/O MGTs configured to pre-emphasize data transmission over PCB traces up to 20 inches long

the system diagram for two Virtex II Pro devices including the Rocket I/O MGTs between the devices. With Rocket I/O, the total bandwidth available between the two FPGAs increases to 200 gigabits per second. This extra bandwidth is extremely useful in switching applications that may require up to 100% internal overhead to handle control protocols over and above the datapath requirements. This 2X increase is an example of the dramatic I/O performance increase available in Virtex-II Pro Platform FPGAs.

Aurora Boosts FPGA-to-FPGA Links

Xilinx has developed a software macro called the Aurora core that provides easy 16-bit and 32-bit interfaces from FPGA-to-FPGA using one or more Rocket I/O MGTs. The Aurora core handles the framing, synchronization, and channel bonding tasks, allowing you to focus more on their application. A single MGT can provide a 16-bit or 32-bit FPGA-to-FPGA interface. The software Aurora core coupled with hard core (implemented in silicon) MGTs can create powerful serial-to-parallel and parallel-to-serial tranceivers.

Alternatively, multiple MGTs can be bonded together to form a higher-bandwidth interface. The Aurora macro ensures that channel-bonded data will appear on the same clock cycle at the other end of the communications link. The 8B/10B encoding method is used for the Aurora soft macro, giving an effective bandwidth of 10 gigabits per second for a set of four channel-bonded MGTs between two FPGAs.

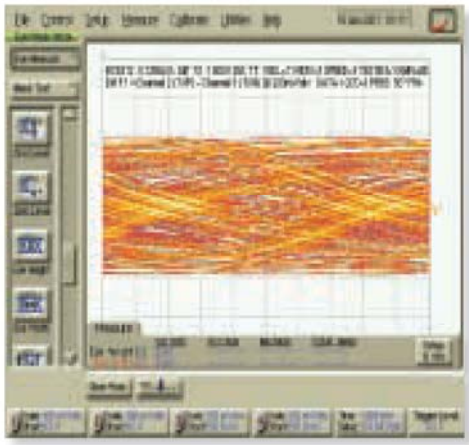
Pre-Emphasis Goes the Distance

Another important feature of the Rocket I/O solution is pre-emphasis, which compensates for the filtering effects of FR-4 PC board material at gigabit speeds. Pre-emphasis boosts the output levels to compensate for the filtering effects of extended PCB traces. With pre-emphasis, PCB runs of 20 inches or longer can be supported reliably at speeds of 3.125 gigabits per second.

Figure 4 shows how two MGTs on separate FPGAs can be easily linked up to 20 inches apart using standard PC board transmission-line traces. Pre-emphasis improves the noise and jitter performance at these high speeds for longer PC traces where dispersion affects timing and voltage margins.

You can clearly see in Figure 5, which shows oscilloscope traces at the receiver without pre-emphasis and with 30% pre-emphasis. The pre-emphasis enables reliable signal transmission at 3.125 Gigabits per second over long PC board traces in standard FR-4 PC board material. Transmitter and receiver termination is provided internally to each MGT, eliminating the need for external termination of these transmission lines. The termination impedance can be set to 50 ohms or to 75 ohms.

No Pre-Emphasis



30% Pre-Emphasis

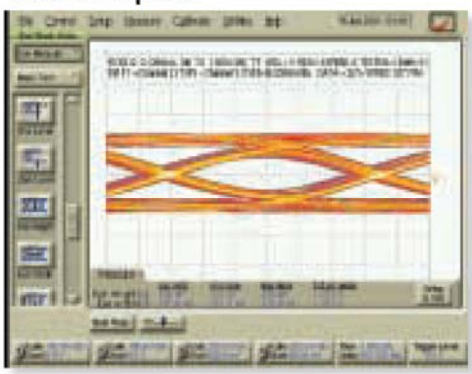


Figure 5 -Received signals after 50 inches FR-4 PC board material with no pre-emphasis and with 30% pre-emphasis in the Rocket I/O MGT.

Conclusion

The Rocket I/O MGTs enable high-speed interfaces for Virtex-II Pro Platform FPGAs. Standards such as InfiniBand Architecture, Fibre Channel, XAUI, and Gigabit Ethernet are directly supported. Inter-FPGA communications are greatly enhanced by Rocket I/O modules and the Aurora soft macro, which enable simple FPGA links with channel-bonded performance of over 10 gigabits per second. Using pre-emphasis, PCB trace runs of 20 inches or greater are possible at speeds of up to 3.125 gigabits per second per link. In the larger Virtex-II Pro devices, this represents a factor of two increase in total I/O performance available per FPGA. Clearly, Virtex-II Pro Platform FPGAs with Rocket I/O MGTs give you a competitive advantage, both in terms of performance and time to market.

New CoolRunner-II CPLD Development Kit

An ideal kit for applying CPLD technology to high-performance portable and battery-powered systems.

by Xilinx Staff

Insight Electronics recently introduced a complete solution for developing designs and applications based on the new high-performance, ultra-low power Xilinx CoolRunner™-II CPLD family. The Insight CoolRunner-II Development Kit enables experimentation with CoolRunner-II design concepts, including the investigation of multiple I/O standards, clock management, security, and CPLD power consumption.

> "Xilinx is pleased to have Insight providing timely support for our breakthrough CoolRunner-II RealDigital CPLDs. Through this development kit, users can evaluate the unbeatable combination of high performance and ultra low power that CoolRunner-II devices offer."
>
> – Steve Sharp, senior manager of Silicon Solutions Marketing.

"Releasing our CoolRunner-II Development Kit in tandem with the Xilinx CoolRunner-II family introduction continues Insight's successful development kit introduction strategy," said Jim Beneke, director of Technical Marketing at Insight. "This approach gives designers immediate access to the devices' full range of features, allowing them to verify the ultra-low power and high performance of the Xilinx second generation Fast Zero Power™ (FZP) technology as used in the CoolRunner-II family."

The Insight kit includes the 64 macrocell, 1.8V CoolRunner-II device; multiple options for power supplies, I/O voltages, and clock sources; a JTAG port; 45 user I/Os; a prototyping area; a two-digit LCD display; and two push-button switches. The Xilinx ISE WebPACK™ software contains all the development software you need, and can be downloaded at no cost from the Xilinx website, or is included in the WebPACK version of the kit.

"Xilinx is pleased to have Insight providing timely support for our breakthrough CoolRunner-II RealDigital CPLDs," stated Steve Sharp, senior manager of Silicon Solutions Marketing. "Through this development kit, users can evaluate the unbeatable combination of high performance and ultra low power that CoolRunner-II devices offer."

Price and Availability

Available for order now, Insight's CoolRunner-II Development Kit is priced at $95. For more information on this and other Xilinx design kits available from Insight, call 888-488-4133, or go to *www.insight-electronics.com/coolrunner2*.

About Insight Electronics

Insight Electronics is a member of The Memec Group, the world's leading distributor of proprietary advanced-technology semiconductors. With 52 divisions in the U.S., Mexico, Canada, and South America, Insight is the largest specialty semiconductor distributor in North and South America. Insight focuses its line card on leading semiconductor companies, enabling their sales team and field application engineers to devote their time and resources to mastery of supplier products, processes, and technologies. The company's value-added services, design expertise, inventory management, logistics, and e-business tools ensure that customers receive the products they need, when and where they need them. For more information, visit the Insight Website at *www.insight-electronics.com.*

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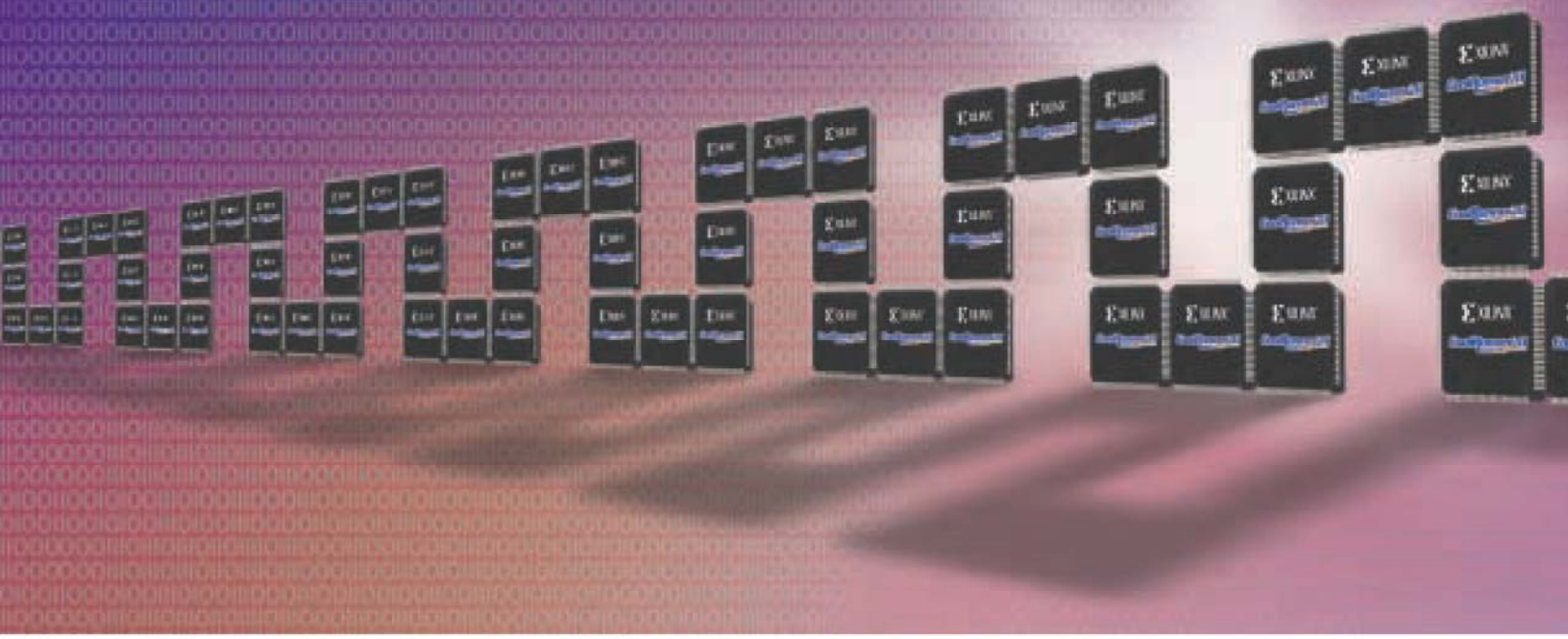

CoolRunner™-II The RealDigital CPLD is the breakthrough in high-performance and low-power you've been looking for. Shipping right now, the new CoolRunner™-II family of devices are the only CPLDs offering a 100% digital core, eliminating power-hungry analog sense amps.

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1.8V CORE VOLTAGE CPLD COMPETITIVE CHART

Manufacturer	Xilinx	Lattice	Altera
Device Family	CoolRunner-II	ispMACH4000C	None
Standby Current	<100 µA	2 mA	N/A
Clock Divider	YES	NO	N/A
Clock Doubler	YES	NO	N/A
I/O Standards Support	LVTTL, LVCMOS, HSTL, SSTL	LVTTL, LVCMOS	N/A
I/O Banks (max)	4	2	N/A

Only CoolRunner-II — with Fast Zero Power™ technology — provides ultra-high performance and ultra-low standby current. It's fast. It's cool. It's available now!

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Virtex-II Pro Platform FPGAs: Introduction and Overview

XCELL (v1.0) January 11, 2002

Advance Product Specification

Summary of Virtex-II Pro Features

- High-performance Platform FPGA solution including
  - Up to sixteen Rocket I/O™ embedded multi-gigabit transceiver blocks (based on Mindspeed's SkyRail™ technology)
  - Up to four IBM® PowerPC™ RISC processor blocks
- Based on Virtex™-II Platform FPGA technology
  - Flexible logic resources
  - SRAM-based in-system configuration
  - Active Interconnect™ technology
  - SelectRAM™ memory hierarchy
  - Dedicated 18-bit x 18-bit multiplier blocks
  - High-performance clock management circuitry
  - SelectI/O™-Ultra technology
  - Digitally Controlled Impedance (DCI) I/O

The members and resources of the Virtex-II Pro family are shown in Table 1.

Rocket I/O™ Features

- Full-duplex serial transceiver (SERDES) capable of baud rates from 622 Mb/s to 3.125 Gb/s
- 80 Gb/s duplex data rate (16 channels)
- Monolithic clock synthesis and clock recovery (CDR)
- Fibre Channel, Gigabit Ethernet, 10-Gbit Attachment Unit Interface (XAUI), and Infiniband-compliant transceivers
- 8-, 16-, or 32-bit selectable internal FPGA interface
- 8B/10B encoder and decoder
- 50Ω / 75Ω on-chip selectable transmit and receive terminations
- Programmable comma detection
- Channel bonding support (two to sixteen channels)
- Rate matching via insertion/deletion characters
- Four levels of selectable pre-emphasis
- Five levels of output differential voltage
- Per-channel internal loopback modes
- 2.5V transceiver supply voltage

PowerPC RISC Core Features

- Embedded 300+ MHz Harvard architecture core
- Low power consumption: 0.9 mW/MHz
- Five-stage data path pipeline
- Hardware multiply/divide unit
- Thirty-two 32-bit general purpose registers
- 16 KB two-way set-associative instruction cache
- 16 KB two-way set-associative data cache
- Memory Management Unit (MMU)
  - 64-entry unified Translation Look-aside Buffers (TLB)
  - Variable page sizes (1 KB to 16 MB)
- Dedicated on-chip memory (OCM) interface
- Supports IBM CoreConnect™ bus architecture
- Debug and trace support
- Timer facilities

Table 1: **Virtex-II Pro Field-Programmable Gate Array Family Members**

Device	Rocket I/O Transceiver Blocks	PowerPC Processor Blocks	CLB (1 CLB = 4 slices = Max 128 bits)			18 X 18 Bit Multiplier Blocks	Block SelectRAM		DCMs	Max I/O Pads
			Array Row x Col	Slices	Maximum Distributed RAM Kbits		18 Kbit Blocks	Max Block RAM Kbits		
XC2VP2	4	0	16 x 22	1,408	44	12	12	216	4	204
XC2VP4	4	1	40 x 22	3,008	94	28	28	504	4	348
XC2VP7	8	1	40 x 34	4,928	154	44	44	792	4	396
XC2VP20	8	2	56 x 46	9,280	290	88	88	1,584	8	564
XC2VP50	16	4	88 x 70	22,592	706	216	216	3,888	8	852

Virtex-II Pro Platform FPGA Technology

- SelectRAM memory hierarchy
  - Up to 4 Mbit of True Dual-Port RAM in 18-Kb block SelectRAM resources
  - Up to 706 Kb of distributed SelectRAM resources
  - High-performance interfaces to external memory
- Arithmetic functions
  - Dedicated 18-bit x 18-bit multiplier blocks
  - Fast look-ahead carry logic chains
- Flexible logic resources
  - Up to 45,184 internal registers / latches with Clock Enable
  - Up to 45,184 Look-Up Tables (LUTs) or cascadable variable (1 to 16 bits) shift registers
  - Wide multiplexers and wide-input function support
  - Horizontal cascade chain and Sum-of-Products support
  - Internal 3-state busing
- High-performance clock management circuitry
  - Up to eight Digital Clock Manager (DCM) modules
    - Precise clock de-skew
    - Flexible frequency synthesis
    - High-resolution phase shifting
  - 16 global clock multiplexer buffers in all parts
- Active Interconnect™ technology
  - Fourth-generation segmented routing structure
  - Fast, predictable routing delay, independent of fanout
  - Deep sub-micron noise immunity benefits
- SelectI/O-Ultra™ technology
  - Up to 852 user I/Os
  - Twenty two single-ended standards and five differential standards
  - Programmable LVTTL and LVCMOS sink/source current (2 mA to 24 mA) per I/O
  - Digitally Controlled Impedance (DCI) I/O: on-chip termination resistors for single-ended I/O standards
  - PCI support (designated banks only)
  - Differential signaling
    - 840 Mb/s Low-Voltage Differential Signaling I/O (LVDS) with current mode drivers
    - Bus LVDS I/O
    - HyperTransport (LDT) I/O with current driver buffers
    - Built-in DDR input and output registers
  - Proprietary high-performance SelectLink technology for communications between Xilinx devices
    - High-bandwidth data path
    - Double Data Rate (DDR) link
    - Web-based HDL generation methodology
- SRAM-based in-system configuration
  - Fast SelectMAP™ configuration
  - Triple Data Encryption Standard (DES) security option (bitstream encryption)
  - IEEE1532 support
  - Partial reconfiguration
  - Unlimited reprogrammability
  - Readback capability
- Supported by Xilinx Foundation™ and Alliance™ series development systems
  - Integrated VHDL and Verilog design flows
  - ChipScope™ Integrated Logic Analyzer
- 0.13-µm, nine-layer copper process with 90 nm high-speed transistors
- 1.5V (VCCINT) core power supply, dedicated 2.5V VCCAUX auxiliary and V_{CCO} I/O power supplies
- IEEE 1149.1 compatible boundary-scan logic support
- Flip-Chip and Wire-Bond Ball Grid Array (BGA) packages in standard 1.00 mm pitch
- Each device 100% factory tested

General Description

The Virtex-II Pro family is a platform FPGA for designs that are based on IP cores and customized modules. The family incorporates multi-gigabit transceivers and PowerPC CPU cores in Virtex-II Pro series FPGA architecture. It empowers complete solutions for telecommunication, wireless, networking, video, and DSP applications.

The leading-edge 0.13µm CMOS nine-layer copper process and the Virtex-II Pro architecture are optimized for high performance designs in a wide range of densities. Combining a wide variety of flexible features and IP cores, the Virtex-II Pro family enhances programmable logic design capabilities and is a powerful alternative to mask-programmed gates arrays.

Architecture

Virtex-II Pro Array Overview

Virtex-II Pro devices are user-programmable gate arrays with various configurable elements and embedded cores optimized for high-density and high-performance system designs. Virtex-II Pro implements the following functionality:

- Embedded high-speed serial transceivers enable data bit rate up to 3.125 Gb/s per channel.
- Embedded IBM PowerPC 405 RISC CPU cores provide performance of 300+ MHz.
- SelectI/O-Ultra blocks provide the interface between package pins and the internal configurable logic. Most popular and leading-edge I/O standards are supported by the programmable IOBs.
- Configurable Logic Blocks (CLBs) provide functional elements for combinatorial and synchronous logic, including basic storage elements. BUFTs (3-state buffers) associated with each CLB element drive dedicated segmentable horizontal routing resources.
- Block SelectRAM memory modules provide large 18-Kb storage elements of True Dual-Port RAM.
- Embedded multiplier blocks are 18-bit x 18-bit dedicated multipliers.
- DCM (Digital Clock Manager) blocks provide self-calibrating, fully digital solutions for clock distribution delay compensation, clock multiplication and division, and coarse- and fine-grained clock phase shifting.

A new generation of programmable routing resources called Active Interconnect Technology interconnects all of these elements. The general routing matrix (GRM) is an array of routing switches. Each programmable element is tied to a switch matrix, allowing multiple connections to the general routing matrix. The overall programmable interconnection is hierarchical and designed to support high-speed designs.

All programmable elements, including the routing resources, are controlled by values stored in static memory cells. These values are loaded in the memory cells during configuration and can be reloaded to change the functions of the programmable elements.

Virtex-II Pro Features

This section briefly describes Virtex-II Pro features.

Rocket I/O Multi-Gigabit Transceiver Cores

The Rocket I/O Multi-Gigabit Transceiver core, based on Mindspeed's SkyRail technology, is a flexible parallel-to-serial and serial-to-parallel transceiver embedded core used for high-bandwidth interconnection between buses, backplanes, or other subsystems.

Multiple user instantiations in an FPGA are possible, providing up to 80 Gb/s of full duplex raw data transfer. Each channel can be operated at a maximum data transfer rate of 3.125 Gb/s.

Each Rocket I/O core implements the following functionality:

- Serializer and deserializer (SERDES)
- Monolithic clock synthesis and clock recovery (CDR)
- Fibre Channel, Gigabit Ethernet, XAUI, and Infiniband compliant transceivers
- 8-, 16-, or 32-bit selectable FPGA interface
- 8B/10B encoder and decoder with bypassing option on each channel
- Channel bonding support (two to sixteen channels)
  - Elastic buffers for inter-chip deskewing and channel-to-channel alignment
- Receiver clock recovery tolerance of up to 75 non-transitioning bits
- 50Ω / 75Ω on-chip selectable TX and RX terminations
- Programmable comma detection
- Rate matching via insertion/deletion characters
- Automatic lock-to-reference function
- Optional TX and RX data inversion
- Four levels of pre-emphasis support
- Per-channel serial and parallel transmitter-to-receiver internal loopback modes
- Cyclic Redundancy Check (CRC) support

PowerPC 405

The PPC405 RISC CPU can execute instructions at a sustained rate of one instruction per cycle. On-chip instruction and data cache reduce design complexity and improve system throughput.

PPC405 features include:

- PowerPC RISC CPU
  - Implements the PowerPC User Instruction Set Architecture (UISA) and extensions for embedded applications
  - Thirty-two 32-bit general purpose registers (GPRs)
  - Static branch prediction
  - Five-stage pipeline with single-cycle execution of most instructions, including loads/stores
  - Unaligned and aligned load/store support to cache, main memory, and on-chip memory
  - Hardware multiply/divide for faster integer arithmetic (4-cycle multiply, 35-cycle divide)
  - Enhanced string and multiple-word handling
  - Big/little endian operation support
- Storage Control
  - Separate instruction and data cache units, both two-way set-associative and non-blocking
  - Eight words (32 bytes) per cache line
  - 16 KB array Instruction Cache Unit (ICU), 16 KB array Data Cache Unit (DCU)

- Operand forwarding during instruction cache line fill
- Copy-back or write-through DCU strategy
- Doubleword instruction fetch from cache improves branch latency

- Virtual mode memory management unit (MMU)
  - Translation of the 4 GB logical address space into physical addresses
  - Software control of page replacement strategy
  - Supports multiple simultaneous page sizes ranging from 1 KB to 16 MB
- OCM controllers provide dedicated interfaces between Block SelectRAM memory and processor core instruction and data paths for high-speed access
- PowerPC timer facilities
  - 64-bit time base
  - Programmable interval timer (PIT)
  - Fixed interval timer (FIT)
  - Watchdog timer (WDT)
- Debug Support
  - Internal debug mode
  - External debug mode
  - Debug Wait mode
  - Real Time Trace debug mode
  - Enhanced debug support with logical operators
  - Instruction trace and trace-back support
  - Forward or backward trace
- Two hardware interrupt levels support
- Advanced power management support

Input/Output Blocks (IOBs)

IOBs are programmable and can be categorized as follows:

- Input block with an optional single data rate (SDR) or double data rate (DDR) register
- Output block with an optional SDR or DDR register and an optional 3-state buffer to be driven directly or through SDR or DDR register
- Bi-directional block (any combination of input and output configurations)

These registers are either edge-triggered D-type flip-flops or level-sensitive latches.

IOBs support the following single-ended I/O standards:

- LVTTL
- LVCMOS (3.3V, 2.5V, 1.8V, and 1.5V)
- PCI (33 and 66 MHz)
- GTL and GTLP
- HSTL 1.5V and 1.8V (Class I, II, III, and IV)
- SSTL 3.3V and 2.5V, (Class I and II)

The digitally controlled impedance (DCI) I/O feature automatically provides on-chip termination for each single-ended I/O standard.

The IOB elements also support the following differential signaling I/O standards:

- LVDS and Extended LVDS (2.5V only)
- BLVDS (Bus LVDS)
- ULVDS
- LDT

Two adjacent pads are used for each differential pair. Two or four IOB blocks connect to one switch matrix to access the routing resources.

Configurable Logic Blocks (CLBs)

CLB resources include four slices and two 3-state buffers. Each slice is equivalent and contains:

- Two function generators (F & G)
- Two storage elements
- Arithmetic logic gates
- Large multiplexers
- Wide function capability
- Fast carry look-ahead chain
- Horizontal cascade chain (OR gate)

The function generators F & G are configurable as 4-input look-up tables (LUTs), as 16-bit shift registers, or as 16-bit distributed SelectRAM memory.

In addition, the two storage elements are either edge-triggered D-type flip-flops or level-sensitive latches.

Each CLB has internal fast interconnect and connects to a switch matrix to access general routing resources.

Block SelectRAM Memory

The block SelectRAM memory resources are 18 Kb of True Dual-Port RAM, programmable from 16K x 1 bit to 512 x 36 bit, in various depth and width configurations. Each port is totally synchronous and independent, offering three “read-during-write” modes. Block SelectRAM memory is cascadable to implement large embedded storage blocks. Supported memory configurations for dual-port and single-port modes are shown in Table 2.

Table 2: **Dual-Port and Single-Port Configurations**

16K x 1 bit	4K x 4 bits	1K x 18 bits
8K x 2 bits	2K x 9 bits	512 x 36 bits

18 X 18-Bit Multipliers

A multiplier block is associated with each SelectRAM memory block. The multiplier block is a dedicated 18 x 18-bit 2s complement signed multiplier, and is optimized for operations based on the block SelectRAM content on one port. The 18 x 18 multiplier can be used independently of the block SelectRAM resource. Read/multiply/accumulate operations and DSP filter structures are extremely efficient.

Both the SelectRAM memory and the multiplier resource are connected to four switch matrices to access the general routing resources.

Global Clocking

The DCM and global clock multiplexer buffers provide a complete solution for designing high-speed clock schemes.

Up to eight DCM blocks are available. To generate deskewed internal or external clocks, each DCM can be used to eliminate clock distribution delay. The DCM also provides 90, 180, and 270-degree phase-shifted versions of its output clocks. Fine-grained phase shifting offers high-resolution phase adjustments in increments of 1/256 of the clock period. Very flexible frequency synthesis provides a clock output frequency equal to a fractional or integer multiple of the input clock frequency. For exact timing parameters, see *Virtex-II Pro Platform FPGAs: DC and Switching Characteristics*.

Virtex-II Pro devices have 16 global clock MUX buffers, with up to eight clock nets per quadrant. Each clock MUX buffer can select one of the two clock inputs and switch glitch-free from one clock to the other. Each DCM can send up to four of its clock outputs to global clock buffers on the same edge. Any global clock pin can drive any DCM on the same edge.

Routing Resources

The IOB, CLB, block SelectRAM, multiplier, and DCM elements all use the same interconnect scheme and the same access to the global routing matrix. Timing models are shared, greatly improving the predictability of the performance of high-speed designs.

There are a total of 16 global clock lines, with eight available per quadrant. In addition, 24 vertical and horizontal long lines per row or column, as well as massive secondary and local routing resources, provide fast interconnect. Virtex-II Pro buffered interconnects are relatively unaffected by net fanout, and the interconnect layout is designed to minimize crosstalk.

Horizontal and vertical routing resources for each row or column include:

- 24 long lines
- 120 hex lines
- 40 double lines
- 16 direct connect lines (total in all four directions)

Boundary Scan

Boundary-scan instructions and associated data registers support a standard methodology for accessing and configuring Virtex-II Pro devices, complying with IEEE standards 1149.1 and 1532. A system mode and a test mode are implemented. In system mode, a Virtex-II Pro device will continue to function while executing non-test boundary-scan instructions. In test mode, boundary-scan test instructions control the I/O pins for testing purposes. The Virtex-II Pro Test Access Port (TAP) supports BYPASS, PRELOAD, SAMPLE, IDCODE, and USERCODE non-test instructions. The EXTEST, INTEST, and HIGHZ test instructions are also supported.

Configuration

Virtex-II Pro devices are configured by loading the bitstream into internal configuration memory using one of the following modes:

- Slave-serial mode
- Master-serial mode
- Slave SelectMAP mode
- Master SelectMAP mode
- Boundary-Scan mode (IEEE 1532)

A Data Encryption Standard (DES) decryptor is available on-chip to secure the bitstreams. One or two triple-DES key sets can be used to optionally encrypt the configuration data.

The Xilinx System Advanced Configuration Enviornment (System ACE) family offers high-capacity and flexible solution for FPGA configuration as well as program/data storage for the processor. See **DS080**, ***System ACE CompactFlash Solution*** for more information.

Readback and Integrated Logic Analyzer

Configuration data stored in Virtex-II Pro configuration memory can be read back for verification. Along with the configuration data, the contents of all flip-flops/latches, distributed SelectRAM, and block SelectRAM memory resources can be read back. This capability is useful for real-time debugging.

The Xilinx ChipScope Pro Integrated Logic Analyzer (ILA) cores and Integrated Bus Analyzer (IBA) cores, along with the ChipScope Pro Analyzer software, provide a complete solution for accessing and verifying user designs within Virtex-II Pro devices.

IP Core and Reference Support

Intellectual Property is part of the Platform FPGA solution. In addition to the existing FPGA fabric cores, the list below shows some of the currently available hardware and software intellectual properties specially developed for Virtex-II Pro by Xilinx. Each IP core is modular, portable, Real-Time Operating System (RTOS) independent, and CoreConnect compatible for ease of design migration. Refer to **www.xilinx.com** for the latest and most complete list of cores.

Hardware Cores

- Bus Infastructure cores (arbiters, bridges, and more)
- Memory cores (Flash, SRAM, and more)
- Peripheral cores (UART, IIC, and more)
- Networking cores (ATM, Ethernet, and more)

Software Cores

- Boot code
- Test code
- Device drivers
- Protocol stacks
- RTOS integration
- Customized board support package

Virtex-II Pro Device/Package Combinations and Maximum I/Os

Offerings include ball grid array (BGA) packages with 1.0 mm pitch. In addition to traditional wire-bond interconnects, flip-chip interconnect is used in some of the BGA offerings. The use of flip-chip interconnect offers more I/Os than is possible in wire-bond versions of the similar packages. Flip-chip construction offers the combination of high pin count and excellent power dissipation.

The Virtex-II Pro device/package combination table (Table 3) details the maximum number of I/Os for each device and package using wire-bond or flip-chip technology.

- FG denotes wire-bond fine-pitch BGA (1.00 mm pitch).
- FF denotes flip-chip fine-pitch BGA (1.00 mm pitch).
- BF denotes flip-chip fine-ptich BGA (1.27 mm pitch).

Table 3: **Virtex-II Pro Device/Package Combinations and Maximum Number of Available I/Os (Advance Information)**

Package	Pitch (mm)	Size (mm)	User Available I/Os				
			XC2VP2	XC2VP4	XC2VP7	XC2VP20	XC2VP50
FG256	1.00	17 x 17	140	140			
FG456	1.00	23 x 23	156	248	248		
FF672	1.00	27 x 27	204	348	396		
FF896	1.00	31 x 31			396	556	
FF1152	1.00	35 x 35				564	692
FF1517	1.00	40 x 40					852
BF957	1.27	40 x 40				564	584

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Xilinx FPGA Product Selection Matrix

Device	Rocket I/O™ Transceiver Blocks	PowerPC™ Processor Blocks	CLB (1 CLB = 4 slices = Max 128 bits) Array Row x Col	Slices	Maximum Distributed RAM Kbits	18 x 18 Bit Multiplier Blocks	Block SelectRAM 18 Kbit Blocks	Max Block RAM Kbits	DCMs	Max I/O Pads
XC2VP2	4	0	16 x 22	1,408	44	12	12	216	4	204
XC2VP4	4	1	40 x 22	3,008	94	28	28	504	4	348
XC2VP7	8	1	40 x 34	4,928	154	44	44	792	4	396
XC2VP20	8	2	56 x 46	9,280	290	88	88	1,584	8	564
XC2VP50	16	4	88 x 70	22,592	706	216	216	3,888	8	852

	System Gates (see note 1)	CLB Resources: CLB Array (Row X Col)	CLB Resources: Number of Slices	CLB Resources: Logic Cells (see note 2)	CLB Resources: CLB Flip-Flops	CLB Resources: Max. Distributed RAM Bits	BLK RAM: # Block RAM Blocks	BLK RAM: Block RAM Bits	CLK Resources: # Dedicated Multipliers	CLK Resources: DLL Frequency (min/max)	CLK Resources: # DLL's	CLK Resources: Frequency Synthesis	CLK Resources: Phase Shift	I/O Features: Digitally Controlled Impedance	I/O Features: Number of Differential I/O Pairs	I/O Features: Max. I/O	I/O Features: I/O Standards	Speed: Commercial Speed Grades (slowest to fastest)	Speed: Industrial Speed Grades (slowest to fastest)	Serial PROM Family		Config. Memory (Bits)
Virtex-II Family — 1.5 Volt																						**.15um Eight Layer Metal Process**
XC2V40	40K	8 x 8	256	576	512	8K	4	72K	4	24/420	4	DCM	DCM	YES	44	88	LDT-25, LVPECL-33,	-4 -5 -6	-4 -5			0.4M
XC2V80	80K	16 x8	512	1,152	1,024	16K	8	144K	8	24/420	4	DCM	DCM	YES	60	120	LVDS-33, LVDS-25,	-4 -5 -6	-4 -5			0.6M
XC2V250	250K	24 x16	1,536	3,456	3,072	48K	24	432K	24	24/420	8	DCM	DCM	YES	100	200	LVDSEXT-33, LVDSEXT-25,	-4 -5 -6	-4 -5			1.7M
XC2V500	500K	32 x 24	3,072	6,912	6,144	96K	32	576K	32	24/420	8	DCM	DCM	YES	132	264	BLVDS-25, ULVDS-25,	-4 -5 -6	-4 -5			2.8M
XC2V1000	1M	40 x 32	5,120	11,520	10,240	160K	40	720K	40	24/420	8	DCM	DCM	YES	216	432	LVTTL, LVCMOS33,	-4 -5 -6	-4 -5			4.1M
XC2V1500	1.5M	48 x 40	7,680	17,280	15,360	240K	48	864K	48	24/420	8	DCM	DCM	YES	264	528	LVCMOS25, LVCMOS18,	-4 -5 -6	-4 -5	ISP	OTP	5.7M
XC2V2000	2M	56 x 48	10,752	24,192	21,504	336K	56	1008K	56	24/420	8	DCM	DCM	YES	312	624	LVCMOS15, PCI33, PCI66,	-4 -5 -6	-4 -5			7.5M
XC2V3000	3M	64 x 56	14,336	32,256	28,672	448K	96	1728K	96	24/420	12	DCM	DCM	YES	360	720	PCI-X, GTL, GTL+, HSTL I,	-4 -5 -6	-4 -5			10.5M
XC2V4000	4M	80 x 72	23,040	51,840	46,080	720K	120	2160K	120	24/420	12	DCM	DCM	YES	456	912	HSTL II, HSTL III, HSTL IV,	-4 -5 -6	-4 -5			15.7M
XC2V6000	6M	96 x 88	33,792	76,032	67,584	1056K	144	2592K	144	24/420	12	DCM	DCM	YES	552	1104	SSTL21, SSTL211,	-4 -5 -6	-4 -5			21.9M
XC2V8000	8M	112 x 104	46,592	104,832	93,184	1456K	168	3024K	168	24/420	12	DCM	DCM	YES	554	1108	SSTL3 I, SSTL3 II	-4 -5	-4			29.1M
Virtex-E Family — 1.8 Volt																						**.18um Six Layer Metal Process**
XCV50E	72K	16 x 24	768	1,728	1,536	24K	16	64K	NA	25/350	8	YES	YES	NA	88	176		-6 -7 -8	-6 -7			0.6M
XCV100E	128K	20 x 30	1,200	2,700	2,400	37.5K	20	80K	NA	25/350	8	YES	YES	NA	98	196		-6 -7 -8	-6 -7			0.9M
XCV200E	306K	28 x 42	2,352	5,292	4,704	73.5K	28	112K	NA	25/350	8	YES	YES	NA	142	284	LVTTL, LVCMOS2,	-6 -7 -8	-6 -7			1.45M
XCV300E	412K	32 x 48	3,072	6,912	6,144	96K	32	128K	NA	25/350	8	YES	YES	NA	158	316	LVCMOS18, PCI33,	-6 -7 -8	-6 -7			1.88M
XCV400E	570K	40 x 60	4,800	10,800	9,600	150K	40	160K	NA	25/350	8	YES	YES	NA	202	404	PCI66, GTL, GTL+,	-6 -7 -8	-6 -7			2.7M
XCV600E	986K	48 x 72	6,912	15,552	13,824	216K	72	288K	NA	25/350	8	YES	YES	NA	256	512	HSTL I, HSTL III, HSTL IV,	-6 -7 -8	-6 -7	ISP	OTP	3.97M
XCV1000E	1,569K	64 x 96	12,288	27,648	24,576	384K	96	384K	NA	25/350	8	YES	YES	NA	330	660	SSTL3 I, SSTL3 II,	-6 -7 -8	-6 -7			6.6M
XCV1600E	2,188K	72 x 180	25,920	34,992	51,840	486K	144	576K	NA	25/350	8	YES	YES	NA	362	724	SSTL21, SSTL211, BLVDS,	-6 -7 -8	-6 -7			8.4M
XCV2000E	2,542K	80 x 120	19,200	43,200	38,400	600K	160	640K	NA	25/350	8	YES	YES	NA	402	804	LVDS, LVPECL	-6 -7 -8	-6 -7			10.2M
XCV2600E	3,264K	92 x 138	25,392	57,132	50,784	793.5K	184	736K	NA	25/350	8	YES	YES	NA	402	804		-6 -7 -8	-6 -7			13M
XCV3200E	4,074K	104 x 156	32,448	73,008	64,896	1014K	208	832K	NA	25/350	8	YES	YES	NA	402	804		-6 -7 -8	-6 -7			16.3M
Virtex-EM Family — 1.8 Volt																						**.18um Six Layer Metal Process**
XCV405E	1.31M	40 x 60	4,800	10,800	9,600	150K	140	560K	NA	25/350	8	YES	YES	NA	202	404	Same As	-6 -7 -8	-6 -7	ISP	OTP	3.43M
XCV812E	2.54M	56 x 84	9,408	21,168	18,816	294K	280	1120K	NA	25/350	8	YES	YES	NA	278	556	Virtex-E	-6 -7 -8	-6 -7			6.52M
Spartan-IIE Family — 1.8 Volt																						**.18um Six Layer Metal Process**
XC2S50E	50K	16 x 24	768	1,728	1,536	24K	8	32K	NA	25/320	4	YES	YES	NA	84	182	LVTTL,LVCMOS2, LVCMOS18,	-6 -7	-6			0.6M
XC2S100E	100K	20 x 30	1,200	2,700	2,400	37.5K	10	40K	NA	25/320	4	YES	YES	NA	86	202	PCI33, PCI66, GTL, GTL+,	-6 -7	-6			0.9M
XC2S150E	150K	24 x 36	1,728	3,888	3,456	54K	12	48K	NA	25/320	4	YES	YES	NA	114	263	HSTL I, HSTL III, HSTL IV, SSTL3 I,	-6 -7	-6	ISP	OTP	1.1M
XC2S200E	200K	28 x 42	2,352	5,292	4,704	73.5K	14	56K	NA	25/320	4	YES	YES	NA	120	289	SSTL3 II, SSTL2 I, SSTL2 II, AGP-2X,	-6 -7	-6			1.4M
XC2S300E	300K	32 x 48	3,072	6,912	6,144	96K	16	64K	NA	25/320	4	YES	YES	NA	120	329	CTT, LVDS, BLVDS, LVPECL	-6 -7	-6			1.9M
Spartan-II Family — 2.5 Volt																						**.22/.18um Six Layer Metal Process**
XC2S15	15K	8 x 12	192	432	384	6K	4	16K	NA	25/200	4	YES	YES	NA	NA	86	LVTTL, LVCMOS2,	-5 -6	-5			0.2M
XC2S30	30K	12 x 18	432	972	864	13.5K	6	24K	NA	25/200	4	YES	YES	NA	NA	132	PCI33 (3.3V & 5V),	-5 -6	-5			0.4M
XC2S50	50K	16 x 24	768	1,728	1,536	24K	8	32K	NA	25/200	4	YES	YES	NA	NA	176	PCI66 (3.3V), GTL, GTL+,	-5 -6	-5	ISP	OTP	0.6M
XC2S100	100K	20 x 30	1,200	2,700	2,400	37.5K	10	40K	NA	25/200	4	YES	YES	NA	NA	196	HSTL I, HSTL III, HSTL IV,	-5 -6	-5			0.8M
XC2S150	150K	24 x 36	1,728	3,888	3,456	54K	12	48K	NA	25/200	4	YES	YES	NA	NA	260	SSTL3 I, SSTL3 II, SSTL2 I,	-5 -6	-5			1.1M
XC2S200	200K	28 x 42	2,352	5,292	4,704	73.5K	14	56K	NA	25/200	4	YES	YES	NA	NA	284	SSTL2 II, AGP-2X, CTT	-5 -6	-5			1.4M

Note: 1. System Gates include 20-30% of CLBs used as RAM
2. A Logic Cell is defined as a 4 input LUT and a register
DCM – Digital Clock Management

Important: Verify all Data with Device Data Sheet

Xilinx FPGA Package Options and User I/O

VIRTEX-II PRO

			User Available I/Os				
Package	Pitch (mm)	Size (mm)	XC2VP2	XC2VP4	XC2VP7	XC2VP20	XC2VP50
FG256	1.00	17 x 17	140	140			
FG456	1.00	23 x 23	156	248	248		
FF672	1.00	27 x 27	204	348	396		
FF896	1.00	31 x 31			396	556	
FF1152	1.00	35 x 35				564	692
FF1517	1.00	40 x 40					852
BF957	1.27	40 x 40				564	584

		VIRTEX-II										
		Virtex-II (1.5V)										
Pins	Body Size	I/O's	XC2V40	XC2V80	XC2V250	XC2V500	XC2V1000	XC2V1500	XC2V2000	XC2V3000	XC2V4000	XC2V6000	XC2V8000
PQFP Packages (PQ)													
208	28 x 28 mm												
240	32 x 32 mm												
HQFP Packages (HQ)													
240	32 x 32 mm												
VQFP Packages (VQ)													
100	14 x 14 mm												
TQFP Packages (TQ)													
144	20 x 20 mm												
Chip Scale Packages — wire-bond chip-scale BGA (0.8 mm ball spacing)													
144	12 x 12 mm		88	92	92								
BGA Packages (BG) — wire-bond standard BGA (1.27 mm ball spacing)													
352	40 x 40 mm												
432	40 x 40 mm												
560	42.5 x 42.5 mm												
575	31 x 31 mm						328	392	408				
728	35 x 35 mm								456	516			
FGA Packages (FT) — wire-bond fine-pitch thin BGA (1.0 mm ball spacing)													
256	17 x 17 mm												
FGA Packages (FG) — wire-bond fine-pitch BGA (1.0 mm ball spacing)													
256	17 x 17 mm		88	120	172	172	172						
456	23 x 23 mm				200	264	324						
676	27 x 27 mm							392	456	484			
680	40 x 40 mm												
860	42.5 x 42.5 mm												
900	31 x 31 mm												
1156	35 x 35 mm												
FFA Packages (FF) — flip-chip fine-pitch BGA (1.0 mm ball spacing)													
896	31 x 31 mm						432	528	624				
1152	35 x 35 mm									720	824	824	824
1517	40 x 40 mm										912	1104	1108
BFA Packages (BF) — flip-chip fine-pitch BGA (1.27 mm ball spacing)													
957	40 x 40 mm								624	684	684	684	684

		VIRTEX-E												
		Virtex-E (1.8V)										V-EM		
Pins	Body Size	I/O's	XCV50E	XCV100E	XCV200E	XCV300E	XCV400E	XCV600E	XCV1000E	XCV1600E	XCV2000E	XCV2600E	XCV3200E	XCV405E	XCV812E
PQFP Packages (PQ)															
208	28 x 28 mm														
240	32 x 32 mm		158	158	158	158	158	158	158						
HQFP Packages (HQ)															
240	32 x 32 mm			158				158							
VQFP Packages (VQ)															
100	14 x 14 mm														
TQFP Packages (TQ)															
144	20 x 20 mm														
Chip Scale Packages — wire-bond chip-scale BGA (0.8 mm ball spacing)															
144	12 x 12 mm		94	94	94										
BGA Packages (BG) — wire-bond standard BGA (1.27 mm ball spacing)															
352	40 x 40 mm			196	260	260									
432	40 x 40 mm					316	316	316							
560	42.5 x 42.5 mm						404	404	404	404	404			404	404
575	31 x 31 mm														
728	35 x 35 mm														
FGA Packages (FT) — wire-bond fine-pitch thin BGA (1.0 mm ball spacing)															
256	17 x 17 mm														
FGA Packages (FG) — wire-bond fine-pitch BGA (1.0 mm ball spacing)															
256	17 x 17 mm		176	176	176	176									
456	23 x 23 mm				284	312									
676	27 x 27 mm						404	444						404	
680	40 x 40 mm							512	512	512	512				
860	42.5 x 42.5 mm								660	660	660				
900	31 x 31 mm							512	660	700					556
1156	35 x 35 mm								660	724	804	804	804		
FFA Packages (FF) — flip-chip fine-pitch BGA (1.0 mm ball spacing)															
896	31 x 31 mm														
1152	35 x 35 mm														
1517	40 x 40 mm														
BFA Packages (BF) — flip-chip fine-pitch BGA (1.27 mm ball spacing)															
957	40 x 40 mm														

		SPARTAN-IIE					SPARTAN-II					
		Spartan-IIE (1.8V)					Spartan-II (2.5V)					
Pins	Body Size	I/O's	XC2S50E	XC2S100E	XC2S150E	XC2S200E	XC2S300E	XC2S15	XC2S30	XC2S50	XC2S100	XC2S150	XC2S200
PQFP Packages (PQ)													
208	28 x 28 mm		146	146	146	146	146		132	140	140	140	140
240	32 x 32 mm												
HQFP Packages (HQ)													
240	32 x 32 mm												
VQFP Packages (VQ)													
100	14 x 14 mm							60	60				
TQFP Packages (TQ)													
144	20 x 20 mm		102	102				86	92	92	92		
Chip Scale Packages — wire-bond chip-scale BGA (0.8 mm ball spacing)													
144	12 x 12 mm							86	92				
BGA Packages (BG) — wire-bond standard BGA (1.27 mm ball spacing)													
352	40 x 40 mm												
432	40 x 40 mm												
560	42.5 x 42.5 mm												
575	31 x 31 mm												
728	35 x 35 mm												
FGA Packages (FT) — wire-bond fine-pitch thin BGA (1.0 mm ball spacing)													
256	17 x 17 mm		182	182	182	182	182						
FGA Packages (FG) — wire-bond fine-pitch BGA (1.0 mm ball spacing)													
256	17 x 17 mm									176	176	176	176
456	23 x 23 mm			202	263	289	329				196	260	284
676	27 x 27 mm												
680	40 x 40 mm												
860	42.5 x 42.5 mm												
900	31 x 31 mm												
1156	35 x 35 mm												
FFA Packages (FF) — flip-chip fine-pitch BGA (1.0 mm ball spacing)													
896	31 x 31 mm												
1152	35 x 35 mm												
1517	40 x 40 mm												
BFA Packages (BF) — flip-chip fine-pitch BGA (1.27 mm ball spacing)													
957	40 x 40 mm												

Note: Virtex-II packages FG456 and FG676 are footprint compatible.
Virtex-II packages FF896 and FF1152 are footprint compatible.
Important: Verify all Data with Device Data Sheet

Numbers indicated in the matrix are the maximum number of user I/O's for that package and device combination.

Xilinx CPLD Product Selection Matrix

PRODUCT SELECTION MATRIX

	System Gates	Macrocells	Product terms per Macrocell	Input Voltage Compatible	Output Voltage Compatible	I/O Features: Max. I/O	I/O Features: I/O Banking	Speed: Min. Pin-to-Pin Logic Delay (ns)	Speed: Commercial Speed Grades (fastest to slowest)	Speed: Industrial Speed Grades (fastest to slowest)	Clocking: Global Clocks	Clocking: Product Term Clocks per Function Block
XC9500XV Family — 2.5 Volt												
XC9536XV	800	36	90	1.8/2.5/3.3	1.8/2.5/3.3	36	1	3.5	-3 -4 -5 -7	-7	3	18
XC9572XV	1600	72	90	1.8/2.5/3.3	1.8/2.5/3.3	72	1	4	-4 -5 -7	-7	3	18
XC95144XV	3200	144	90	1.8/2.5/3.3	1.8/2.5/3.3	117	2	4	-4 -5 -7	-7	3	18
XC95288XV	6400	288	90	1.8/2.5/3.3	1.8/2.5/3.3	192	4	5	-5 -7 -10	-10	3	18
XC9500XL Family — 3.3 Volt												
XC9536XL	800	36	90	2.5/3.3/5	2.5/3.3	36		5	-5 -7 -10	-7 -10	3	18
XC9572XL	1600	72	90	2.5/3.3/5	2.5/3.3	72		5	-5 -7 -10	-7 -10	3	18
XC95144XL	3200	144	90	2.5/3.3/5	2.5/3.3	117		5	-5 -7 -10	-7 -10	3	18
XC95288XL	6400	288	90	2.5/3.3/5	2.5/3.3	192		6	-6 -7 -10	-7 -10	3	18
CoolRunner XPLA3 — 3.3 Volt												
XCR3032XL	750	32	48	3.3/5	3.3	36		5	-5 -7 -10	-7 -10	4	16
XCR3064XL	1500	64	48	3.3/5	3.3	68		6	-6 -7 -10	-7 -10	4	16
XCR3128XL	3000	128	48	3.3/5	3.3	108		6	-6 -7 -10	-7 -10	4	16
XCR3256XL	6000	256	48	3.3/5	3.3	164		7.5	-7 -10 -12	-10 -12	4	16
XCR3384XL	9000	384	48	3.3/5	3.3	220		7.5	-7 -10 -12	-10 -12	4	16
XCR3512XL	12000	512	48	3.3/5	3.3	260		7.5	-7 -10 -12	-10 -12	4	16
CoolRunner-II Family — 1.8 Volt												
XC2C32	750	32	40	1.5/1.8/2.5/3.3	1.5/1.8/2.5/3.3	33	1	3.5	-3 -4 -6	-4 -6	3	17
XC2C64	1500	64	40	1.5/1.8/2.5/3.3	1.5/1.8/2.5/3.3	64	1	4	-4 -5 -7	-5 -7	3	17
XC2C128	3000	128	40	1.5/1.8/2.5/3.3	1.5/1.8/2.5/3.3	100	2	4.5	-4 -6 -7	-6 -7	3	17
XC2C256	6000	256	40	1.5/1.8/2.5/3.3	1.5/1.8/2.5/3.3	184	2	5	-5 -6 -7	-6 -7	3	17
XC2C384	9000	384	40	1.5/1.8/2.5/3.3	1.5/1.8/2.5/3.3	240	4	6	-6 -7 -10	-7 -10	3	17
XC2C512	12000	512	40	1.5/1.8/2.5/3.3	1.5/1.8/2.5/3.3	270	4	6	-6 -7 -10	-7 -10	3	17

PACKAGE OPTIONS AND USER I/O

	Body Size	XC9500XV: XC9536XV	XC9572XV	XC95144XV	XC95288XV	XC9500XL: XC9536XL	XC9572XL	XC95144XL	XC95288XL	CoolRunner XPLA3: XCR3032XL	XCR3064XL	XCR3128XL	XCR3256XL	XCR3384XL	XCR3512XL	CoolRunner II: XC2C32	XC2C64	XC2C128	XC2C256	XC2C384	XC2C512
PLCC Packages (PC)																					
44	17.5 x 17.5 mm	34	34			34	34			36	36					33	33				
PQFP Packages (PQ)																					
208	28 x 28 mm				168				168				164	172	180				173	173	173
VQFP Packages (VQ)																					
44	12 x 12 mm	34	34			34	34			36	36					33	33				
64	12 x 12 mm					36	52														
100	16 x 16 mm										68	84					64	80	80		
TQFP Packages (TQ)																					
100	14 x 14 mm		72	81			72	81													
144	20 x 20 mm			117	117			117	117			108	120	118				100	118	118	
Chip Scale Packages (CP) — wire-bond chip-scale BGA (0.5 mm ball spacing)																					
56	6 X 6 mm										48					33	45				
Chip Scale Packages (CS) — wire-bond chip-scale BGA (0.8 mm ball spacing)																					
48	7 x 7mm	36	38			36	38			36	40										
144	12 x 12 mm			117				117				108									
280	16 x 16 mm				192				192				164								
BGA Packages (BG) — wire-bond standard BGA (1.27 mm ball spacing)																					
256	27 x 27 mm								192										184	212	212
FBGA Packages (FG) — wire-bond Fineline BGA (1.0 mm ball spacing)																					
256	17 x 17 mm				192				192				164	212	212						
324	23 x 23 mm													220	260					240	270

Important: Verify all Data with Device Data Sheet and Product Availability with your local Xilinx Rep

Xilinx Software

	Feature	ISE *WebPACK*	ISE *BaseX*	ISE *Foundation*	ISE *Alliance*
	Platform	PC	PC	PC/UNIX	PC/UNIX
Device Support	Virtex Series	Up to 300K (Virtex E and Virtex II)	Up to 300K	ALL	ALL
	Spartan Series	Spartan-II Series	ALL	ALL	ALL
	XC4000 Series	No	4KE & Newer	4KE & Newer	4KE & Newer
	CoolRunner Series	ALL	ALL	ALL	ALL
	XC9500 Series	ALL	ALL	ALL	ALL
Design Planning	Modular Design	No	Sold as an Option	Sold as an Option	Sold as an Option
	Educational Services	Yes	Yes	Yes	Yes
	Design Services	Yes	Yes	Yes	Yes
	Support Services	Web Only	Yes	Yes	Yes
Design Entry	Schematic Editor (Gate & Block Level HDL)	Yes	Yes	PC Only	No
	HDL Editor	Yes	Yes	Yes	Yes
	State Diagram Editor	Yes	Yes	PC Only	No
	CORE Generator	No	Yes	Yes	Yes
	Xilinx System Generator for Simulink	No	Sold as an Option	Sold as an Option	Sold as an Option
Synthesis	FPGA Express	No	Yes	PC Only	No
	Xilinx Synthesis Technology (XST)	Yes	Yes	Yes	No
	Synplify/Pro Integration	No	Yes	PC Only	PC Only
	Leonardo Integration	Yes	Yes	Yes	Yes
	ABEL	CPLD	CPLD	CPLD (PC Only)	No
Implementation Tools	iMPACT	Yes	Yes	Yes	Yes
	FloorPlanner	Yes	Yes	Yes	Yes
	Xilinx Constraints Editor	Yes	Yes	Yes	Yes
	Timing Driven Place & Route	Yes	Yes	Yes	Yes
	Timing Improvement Wizard	No	Yes	Yes	Yes
Board Level Integration	IBIS Models	Yes	Yes	Yes	Yes
	STAMP Models	Yes	Yes	Yes	Yes
	LMG SmartModels	Yes	Yes	Yes	Yes
Verification	HDL Bencher	Yes	Yes	PC Only	No
	ModelSim Xilinx Edition (XE)	ModelSim XE Starter Included	ModelSim XE Starter Included	ModelSim XE Starter Included	ModelSim XE Starter Included
	(See www.xilinx.com for more information)	(ModelSim XE Sold as an Option)	(ModelSim XE Sold as an Option)	(ModelSim XE Sold as an Option)	(ModelSim XE Sold as an Option)
	Static Timing Analyzer	Yes	Yes	Yes	Yes
	Chipscope ILA	No	Sold as an Option	Sold as an Option	Sold as an Option
	FPGA Editor with Probe	No	Yes	Yes	Yes
	ChipViewer	Yes	Yes	Yes	Yes
	XPower (Power Analysis)	Yes	Yes	Yes	Yes
	3rd Party Simulator Support	Yes	Yes	Yes	Yes
IP/CORE	For more information on the complete list of Xilinx IP products, visit the Xilinx IP Center at http://www.xilinx.com/ipcenter				

Xilinx Configuration Storage Solutions

System ACE	Memory Density	Number of Components	Min board space	Compression	FPGA Config. Mode	Multiple Designs	Software Storage	Removable	IRL Hooks	Max Config. Speed	Non-Volatile Media
System ACE CF	up to 8 Gbit	2	25 cm^2	No	JTAG	Unlimited	Yes	Yes	Yes	30 Mbit/sec	CompactFlash
System ACE MPM	16 Mbit 32 Mbit 64 Mbit	1	12.25 cm^2	Yes	SelectMAP (up to 4 FPGA) Slave-Serial (up to 8 FPGA chains)	Up to 8	No	No	Yes	152 Mbit/sec	AMD Flash Memory
System ACE SC	16 Mbit 32 Mbit 64 Mbit	3	Custom	Yes	SelectMAP (up to 4 FPGA) Slave-Serial (up to 8 FPGA chains)	Up to 8	No	No	Yes	152 Mbit/sec	AMD Flash memory

PROM

	Density	PD8	VO8	SO20	PC20	PC44	VQ44	Core Voltage	I/O Voltage 2.5V	I/O Voltage 3.3V
In-System Programming (ISP) Configuration PROMs										
XC18V256	256Kb			Y	Y		Y	3.3V	Y	Y
XC18V512	512Kb			Y	Y		Y	3.3V	Y	Y
XC18V01	1Mb			Y	Y		Y	3.3V	Y	Y
XC18V02	2Mb					Y	Y	3.3V	Y	Y
XC18V04	4Mb					Y	Y	3.3V	Y	Y
One-Time Programmable (OTP) Configuration PROMs										
XC17V01	1.6Mb		Y	Y	Y			3.3V	Y	Y
XC17V02	2Mb				Y	Y	Y	3.3V	Y	Y
XC17V04	4Mb				Y	Y	Y	3.3V	Y	Y
XC17V08	8Mb					Y	Y	3.3V	Y	Y
XC17V16	16Mb					Y	Y	3.3V	Y	Y

	FPGA	PD8	VO8	SO20	PC20	PC44	VQ44	Core Voltage	I/O Voltage 2.5V	I/O Voltage 3.3V
OTP Configuration PROMs for Spartan-II/IIE										
XC17S50A	XC2S50E	Y	Y	Y				3.3V	Y	Y
XC17S100A	XC2S100E	Y	Y	Y				3.3V	Y	Y
XC17S200A	XC2S150E	Y	Y				Y	3.3V	Y	Y
XC17S200A	XC2S200E	Y	Y				Y	3.3V	Y	Y
XC17S300A	XC2S300E						Y	3.3V	Y	Y
XC17S15A	XC2S15	Y	Y	Y				3.3V	Y	Y
XC17S30A	XC2S30	Y	Y	Y				3.3V	Y	Y
XC17S50A	XC2S50	Y	Y	Y				3.3V	Y	Y
XC17S100A	XC2S100	Y	Y	Y				3.3V	Y	Y
XC17S150A	XC2S150	Y	Y	Y				3.3V	Y	Y
XC17S200A	XC2S200	Y	Y				Y	3.3V	Y	Y

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Xilinx IP Selection Guide

Function	Vendor Name	IP Type	Virtex-II	Virtex	Spartan-II	Spartan	Implementation Example			Key Features	Application Examples
							Occupancy	MHz	Device		
Communication & Networking											
BUFE-based Multiplexer Slice	Xilinx	LogiCORE	V-II	V	S-II					1-256 bits wide	
3G FEC Package	Xilinx	LogiCORE	V-II	V						Viterbi Decoder, Turbo Codec, Convolutional Enc	3G Wireless Infrastructure
3GPP Compliant Turbo Convolutional Decoder	Xilinx	LogiCORE	V-II	V			80%	40	XC2V500	3GPP specs, 2 Mbps, BER=10-6 for 1.5dB SNR	3G Wireless Infrastructure
3GPP Compliant Turbo Convolutional Encoder	Xilinx	LogiCORE	V-II	V			65%	60	XC2V250	Compliant w/ 3GPP, puncturing	3G Wireless Infrastructure
3GPP Turbo Decoder	sysonchip	AllianceCORE	V-II	V			87%	66	XC2V500-5	3GPP/UMTS compliant, MT-2000, 2Mbps data	Error correction, wireless
8b/10b Decoder	Xilinx	LogiCORE	V-II	V	S-II		1 BRAM	100	XC2V1000	Industry std 8b/10b en/decode for serial data transmission	Physical layer of Fiber Channel
8b/10b Encoder	Xilinx	LogiCORE	V-II	V	S-II		1 BRAM	100	XC2V1000	Industry std 8b/10b en/decode for serial data transmission	Physical layer of Fiber Channel
ADPCM 1024 Channel	Amphion	AllianceCORE	V-II	V						G.721, 723, 726, 726a, 727, 727a, u-law, a-law	DECT, VOIP, cordless telephony
ADPCM 16 Channel	Amphion	AllianceCORE		V	S-II		89%	16	XCV150-6	G.721, 723, 726, 726a, 727, 727a, u-law, a-law	DECT, VOIP, cordless telephony
ADPCM 256 Channel	Amphion	AllianceCORE	V-II	V						G.721, 723, 726, 726a, 727, 727a, u-law, a-law	DECT, VOIP, cordless telephony
ADPCM 512 Channel	Amphion	AllianceCORE	V-II	V							
ADPCM 768 Channel	Amphion	AllianceCORE	V-II	V			89%	50	XC2V500-5	G.721, 723, 726, 726a, 727, 727a, u-law, a-law	DECT, VOIP, cordless telephony
ADPCM Speech Codec, 32 Channel (DO-DI-ADPCM32)	Xilinx	LogiCORE	V-II	V	S-II		62%	25	XC2V500	G.726, G.727, 32 duplex channels	DECT, VOIP, Wireless local loop, DSLAM, PBX
ADPCM Speech Codec, 64 Channel (DO-DI-ADPCM64)	Xilinx	LogiCORE	V-II	V	S-II		61%	27	XC2V500	G.726, G.727, 64 duplex channels	DECT, VOIP, Wireless local loop, DSLAM, PBX
BOOST Lite Bluetooth Baseband Processor	NewLogic	AllianceCORE	V-II	V			73%	33	XC2V1000-4	Compliant to Bluetooth v1.1, BQB qualified software for L2CAP, LHP, HC1, voice support	Bluetooth applications
Cell Assembler (CC-201)	Paxonet	AllianceCORE		V		S	44%	60	XC4005XL-1	Octet wide operation, HEC compute, cell scrambling	ATM adapter cards, routers, switches
Cell Delineation (CC-200)	Paxonet	AllianceCORE		V		S	67%	40	XC4010XL-9	Octet wide operation, HEC verification, cell scrambling	ATM adapter cards, routers, switches
Convolutional Encoder	TILAB	AllianceCORE		V	S-II	S	2%	144	XCV50-6	code rate, gen. vectors, CMSTR length customizable	Error correction
Convolutional Encoder	Xilinx	LogiCORE	V-II	V	S-II		10%	26	XC2V40	k from 3 to 9, puncturing from 2/3 to 12/13	3G base stations, broadcast, wireless LAN, cable modem, xDSL, satellite com, uwave
CRC10 Generator and Verifier (CC-130)	Paxonet	AllianceCORE		V		S	22%	20	XCS30-4	Separate generator and verifier blocks, compatible with ITU-T I.363 for AAL3/AAL4	ATM, SONET, and Ethernet
CRC32 Generator and Verifier (CC-131)	Paxonet	AllianceCORE		V		S	43%	29	XCS30-4	Separate generator and verifier blocks, compat with ITU-T I.363 for AAL5	ATM, SONET, and Ethernet
DES	MemecCore	AllianceCORE		V	S-II	S	79%	25	XC520-4	NIST certified, supports EBC, CBC, CFB, and OFB	Secure communication, data storage
DES - Triple DES Cryptoprocessor	inSilicon	AllianceCORE		V	S-II	S	93%	48	XC2S150-6	Compliant with ANSI X9.52, 128-bit key or two independent 64-bit keys	Secure communication, data storage
DES Cryptoprocessor	inSilicon	AllianceCORE		V	S-II	S	20%	94	XC2S100-6	NIST certified, supports ECB, CBC, CFB, OFB	Secure communication, data storage
Distributed Sample Descrambler	TILAB	AllianceCORE		V	S-II	S	14%	74	XCV50-6	ITU-T I.432. Param data width, cell & header length	ATM PHY layer
Distributed Sample Descrambler	TILAB	AllianceCORE		V	S-II	S	14%	74	XCV50-6	ITU-T I.432. Param data width, cell & header length	ATM PHY layer
Distributed Sample Scrambler	TILAB	AllianceCORE		V	S-II	S	9%	104	XCV50-6	Compliant with ITU-T I.432 scrambler. Param data width, cell length, header length	ATM PHY layer
DVB Satellite Modulator Core	MemecCore	AllianceCORE		V	S-II	S	39%	45–70	XCV50-4	Conforms to ETSI EN 300 421 v1.1.2, selectable convolutional code rate	Digital broadcast, microwave transmitter
DVB-RCS Turbo Decoder	iCODING	AllianceCORE	V-II	V			54%	69	XC2V2000-5	DVB-RCS compliant, 9Mbps, data rate, switchable code rates and frame sizes	Error correction, wireless, DVB, Satellite data link
Fast Ethernet (10/100 Mbps) MAC Evaluation Board	Paxonet	AllianceCORE		V	S-II	S					
Fast Ethernet (10/100 Mbps) Media Access Controller Transmitter and Receiver Cores	Paxonet	AllianceCORE		V	S-II	S	90%	50	XCV150-4	IEEE 802.3 compliant RMON, MIBs stats, MII	Ethernet switched, hub, NICS
Flexbus 4 Interface Core, 16-Channel (DO-DI-FLX4C16)	Xilinx	LogiCORE	V-II				31%	200	XC2V3000 FG676-5		Line card: terabit routers & optical switches
Flexbus 4 Interface Core, 4-Channel (DO-DI-FLX4C4)	Xilinx	LogiCORE	V-II				27%	200	XC2V1000 FG456-5		Line card: terabit routers & optical switches
Flexbus 4 Interface Core, 1-Channel (DO-DI-FLX4C1)	Xilinx	LogiCORE	V-II				12%	200	XC2V1000 FG456-5		Line card: terabit routers & optical switches
G.711 PCM Codec	Xilinx	LogiCORE		V	S-II		12%	44	XCV50	µ-Law, ITU G.711, EBI for A-Law	Digital telephony, DECT, T1 & E1 Links
G.711 PCM Compressor	Xilinx	LogiCORE		V	S-II		7%	44	XCV50	µ-Law, ITU G.711, EBI for A-Law	Digital telephony, DECT, T1 & E1 Links
G.711 PCM Expander	Xilinx	LogiCORE		V	S-II		6%	57	XCV50	Digital telephony DECT, T1 & E1	Digital telephony, DECT, T1 & E1 Links
HDLC Controller Core, 32 Channels	Xilinx	LogiCORE	V-II	V	S-II		34%	81	XC2V250	32 full duplex CRC-16/32, 8/16-bit address insertion/deletion	X.25, POS, cable modems, frame relay switches, video conferencing over ISDN
HDLC Controller Core, Single Channel	Xilinx	LogiCORE	V-II	V	S-II		15%	115	XC2V250	16/32-bit frame seq, 8/16-bit addr insert/delete, flag/zerop insert/detect	X.25, POS, cable modems, frame relay switches, video conferencing over ISDN
IMA-32 Inverse Multiplexer for ATM	Mindspeed	AllianceCORE		V			78%	50	XCV400E-6	Compliant ATM Forum IMA, prog. groups & links, SW driver available	Network adapters, routers, multiplexers
IMA-8 Inverse Multiplexer for ATM	Mindspeed	AllianceCORE			S-II		100%	50	XC2S150-5	Compliant with ATM Forum IMA, prog. groups & links, SW driver	Network adapters, routers, DSLAMs
Interleaver Deinterleaver	TILAB	AllianceCORE		V	S-II	S	21%	73	XVC50-6	Block & convolutional support. param features. 3GPP, UMTS, GSM, DVB compliant	Channel coding in telecom/wireless, broadcast
Interleaver/De-interleaver	Xilinx	LogiCORE	V-II	V	S-II		30%	187	XC2V40	Convolutional, width up to 256 bits, 256 branches	Broadcast, wireless LAN, cable modem, xDSL, satellite com,uwave nets, digital TV
IPlogiCAM Internet Protocol Content Addressable Memory	TILAB	AllianceCORE		V	S-II	S	9%	49	XCV50-6	Hardware control blk works with s/w CAM	IP routers
MT1F T1 Framer	Virtual	AllianceCORE					*	*	*	D4, ESF, SLC-96 formats. For XC4000.	DSI trunk, PBX I/F
Noisy Transmission Channel Model	TILAB	AllianceCORE		V	S-II	S	22%	100	XCV50-6	Programmable noise generation profile	Noise emulation in transmission channel
PARSER: Bit Stream Analyzer and Data Extractor	TILAB	AllianceCORE		V	S-II	S	32%	67	XCV50-6	Data syntax analysis of IP, MPEG, ATM	ATM, IP, MPEG
PE-MACMII Dual Speed 10/100 Mbps Ethernet MAC	Alcatel	AllianceCORE	V-II	V	S-II		33%	60	XC2V500-4	802.3 compliant, Supports single & multimode fiber optic devices, M11 interfaces, RMON and Etherstate statistics	Networking, Broadband, SOHO, Home networking, storage, routers, switches, printers, NIC
POS-PHY Level 3 Link Layer Interface Core, 48 Channel (DO-DI-POSL3LINK48A)	Xilinx	LogiCORE	V-II				33%	104	XC2V6000 FF1152-4		
POS-PHY L3 Link Layer Interface, 16-Ch (DO-DI-POSL3LINK16)	Xilinx	LogiCORE	V-II				40%	104	XC2V1000 FG456-4		Line card: terabit routers & optical switches
POS-PHY L3 Link Layer Interface, 4-Ch (DO-DI-POSL3LINK4)	Xilinx	LogiCORE	V-II	VE			15%	104	XC2V1000 FG456-4		Line card: terabit routers & optical switches
POS-PHY L3 Link Layer Interface, 2-Ch (DO-DI-POSL3LINK2)	Xilinx	LogiCORE	V-II	VE			55%	104	XCV50E-8		Line card: terabit routers & optical switches
POS-PHY L3 Link Layer Interface, Single Channel	Xilinx	LogiCORE	V-II	VE			6%	104	XC2V1000 FG456-4		
POS-PHY L3 Physical Layer Interface (DO-DI-POSL3PHY)	Xilinx	LogiCORE		VE			52%	104	XCV50E-8		Line card: terabit routers & optical switches
POS-PHY L4 Multi-Channel Interface (DO-DI-POSL4MC)	Xilinx	LogiCORE	V-II				29%	104	XC2V3000 FG676-5		
PPP8 HDLC Core CC318f	Paxonet	AllianceCORE		V	S-II		76%	80	XC2S150-6	RFC1619 (IP&IPX) POS, 16/32 bit FCS generation and verification, stats	Bridges, switches, WAN links
Reed-Solomon Decoder	MemecCore	AllianceCORE		V	S-II	S	83%	73	XCV50-6	Customizable, >580 Mbps	Error correction
Reed-Solomon Decoder	Amphion	AllianceCORE		V	S-II	S	51%	50	XCV100-4	Supports ETSI 300 421, 300 429, >300 Mbps	Error correction
Reed-Solomon Encoder	MemecCore	AllianceCORE		V	S-II	S	13%	113	XCV50-6	Customizable, > 900 Mbps	Error Correction
Reed-Solomon Encoder	Amphion	AllianceCORE		V	S-II	S	11%	82	XCV50-4	Supports ETSI 300 421, 300 429	Error correction
Reed-Solomon Decoder	Xilinx	LogiCORE	V-II	V	S-II	S	40%	98	XC2V250	Std or custom coding, 3-12 bit symbol width, up to 4095 symbols	Broadcast, wireless LAN, cable modem, xDSL, satellite com,uwave nets, digital TV

Function	Vendor Name	IP Type	Virtex-II	Virtex	Spartan-II	Spartan	Implementation Example: Occupancy	Implementation Example: MHz	Implementation Example: Device	Key Features	Application Examples
Microprocessors, Controllers & Peripherals (continued)											
OPB Timer/Counter	Xilinx	LogiCORE	V-II	V	S-II			125	Virtex-II	Bundled in the MicroBlaze Development Kit	Processor applications
OPB UART (16450, 16550)	Xilinx	LogiCORE	V-II	V	S-II			125	Virtex-II	Interfaces through OPB to MicroBlaze	Processor applications
OPB UART Lite	Xilinx	LogiCORE	V-II	V	S-II			125	Virtex-II	Bundled in the MicroBlaze Development Kit	Processor applications
OPB WD™	Xilinx	LogiCORE	V-II	V	S-II			125	Virtex-II	Bundled in the MicroBlaze Development Kit	Processor applications
PF3100 PC/104-Plus Reconfigurable Module	Derivation	AllianceCORE	V-II				N/A	N/A	XC2V1000 FG256	PC/104 & PC/104+ development board	Internet appliance, industrial control
R8051 RISC MicroController	CAST	AllianceCORE		V	S-II		76%	34	XC2S150-6	12X faster, SRF I/F	Embedded systems
R80515 High-speed 8-bit RISC Microcontroller	CAST	AllianceCORE		V			56%	42	XCV200E-8	RISC implementation, 8 bit ALU, 8 bit control, 32 bit IO, 16 bit timer/counters, SFR I/F, ext. memory I/F	High speed embedded systems, audio, video
SPI	Xilinx	LogiCORE	V-II	V	S-II				Virtex-II	Interfaces through OPB to MicroBlaze	Networking, communications, processor apps
Synchronous DRAM Controller	NMI	AllianceCORE		V	S-II		5%	137	XCV50-6	SDRAM refresh, customizable	Embedded systems using SDRAMs
uEBX Reference and Development Platform	NMI	AllianceCORE		V			NA	NA	NA	Interfaces NMI's MicroEngines to EBX bus	PC104 applications
uPCI Reference and Development Platform	NMI	AllianceCORE		V			NA	NA	NA	Interfaces NMI's MicroEngines to PCI bus	PCI ethernet/graphics applications
V8-uRISC 8-bit RISC Microprocessor	VAutomation	AllianceCORE					*	*	*	8-bit processor, 8 bit ALU, 16 bit stack pointer, 33 opcodes, 4 addr. Modes, 2 user opcodes	Embedded systems, 8-bit processing apps.
XF8250 UART	MemecCore	AllianceCORE				S	59%	10	XCS10-4	DC to 625K baud	Serial communications
XF8255 Programmable Peripheral Interface	MemecCore	AllianceCORE				S	64%	8	XCS05-4	Bit set/reset support	Embedded systems
XF8256 Multifunction Microprocessor Support Controller	MemecCore	AllianceCORE				S	89%	10	XCS20-4	Baud rate generator for 13 common baud rates, parallel I/O ports, prog. timer/counters	Communication, embedded systems
XF8279 Programmable Keyboard Display Interface	MemecCore	AllianceCORE				S	46%	8	XCS20-4	8 char keyboard FIFO, 2-key lockout, n-key rollover, 4-16 char display	Embedded systems interface
XF-TWSI Two-Wire Serial Interface Master-Only	MemecCore	AllianceCORE		V	S-II	S					
XF-TWSI-MS Two-Wire Serial Interface Master-Slave	MemecCore	AllianceCORE		V	S-II	S	24%	59	XCV50-4	I2C-like, multi master fast/std. modes	Embedded systems
XF-UART Asynchronous Communications Core	MemecCore	AllianceCORE	V-II	V		S	15%	50	XCS20-4	UART and baud rate generator	Serial data communication
Standard Bus Interfaces											
Arbiter	TILAB	AllianceCORE		V	S-II	S		33	XCV50-6	2 priority classes - strong/weak, access counters	General purpose bus arbitration
CAN Bus Interface R3.0	Sci-worx	AllianceCORE		V	S-II	S	*	*	*	Supports CAN 2.0A, 2.0B, error handling, stuff bit generation, SRC, individual acceptance filtering	Automotive, network, home automation
EP100 PowerPC Bus Slave	Eureka	AllianceCORE		V	S-II						
EP201 PowerPC Bus Master	Eureka	AllianceCORE		V	S-II						
PCI-X 64/66 Interface for Virtex-E (DO-DI-PCIX64-VE)	Xilinx	LogiCORE		VE			30%	66	XCV300E-8	PCI-X 1.0 comp, 64/32-bit, 66 MHz PCI-X initiator and target IF, PCI 2.2 comp, 64/32-bit, 33 MHz PCI initiator and target IF, 3.3 V PCI-X at 33-66 MHz, 3.3 V PCI at 0-33 MHz	Comm systems, SAN, clustered servers, Ultra 3 SCSI/Fibre Ch RAID, multi-port Gb
PCI-X 64/100 Interface for Virtex-II (DO-DI-PCIX64-VE)	Xilinx	LogiCORE	V-II				30%	100	XC2V1000 FG456-5	PCI-X 1.0 comp, 64/32-bit, 66 MHz PCI-X initiator and target IF, PCI 2.2 comp, 64/32-bit, 33 MHz PCI initiator and target IF, 3.3 V PCI-X at 33-66 MHz, 3.3 V PCI at 0-33 MHz	Server,Embedded,gb ethernet,U320 SCSI,Fibre Ch,RAID cntl,graphics
PCI32 Single-Use License for Spartan (DO-DI-PCI32-SP)	Xilinx	LogiCORE			S-II	S	12%	66	XC2S200 PQ208-6	v2.2 comp, assured PCI timing, 3.3/5-V, 0-waitstate, CPCI hot swap friendly	PC add-in boards, CPCI, Embedded
PCI32 Virtex Interface Design Kit (DO-DI-PCI32-DKT)	Xilinx	LogiCORE	V-II	V	S-II	S	6%	66	XC2V1000 FG456-5	Includes PCI32 board, drive development kit, and customer education 3-day training class	
PCI32 Virtex Interface, IP Only (DO-DI-PCI32-IP)	Xilinx	LogiCORE	V-II	V	S-II	S	6%	66	XC2V1000 FG456-5	v2.2 comp, assured PCI timing, 3.3/5-V, 0-waitstate, CPCI hot swap friendly	PC add-in boards, CPCI, Embedded
PCI64 & PCI32, IP Only (DO-DI-PCI-AL)	Xilinx	LogiCORE	V-II	V	S-II	S	6 - 7%	66	XC2V1000 FG456-5	v2.2 comp, assured PCI timing, 3.3/5-V, 0-waitstate, CPCI hot swap friendly	PC boards,CPCI,Embedded,hiperf video,gb ethernet
PCI64 Virtex Interface Design Kit (DO-DI-PCI64-DKT)	Xilinx	LogiCORE	V-II	V	S-II	S	7%	66	XC2V1000 FG456-5	v2.2 comp, assured PCI timing, 3.3/5-V, 0-waitstate, CPCI hot swap friendly	PC boards, CPCI, Embedded, hiperf video, gb ethernet
PCI64 Virtex Interface, IP Only (DO-DI-PCI64-IP)	Xilinx	LogiCORE	V-II	V	S-II		7%	66	XC2V1000 FG456-5	v2.2 comp, assured PCI timing, 3.3/5-V, 0-waitstate, CPCI hot swap friendly	PC boards,CPCI,Embedded,hiperf video,gb ethernet
RapidIO 8-bit port LP-LVDS Phy Layer (DO-DI-RIO8-PHY)	Xilinx	LogiCORE	V-II				24%	250	XC2V1000 FG456-5	RapidIO Interconnect v1.1 compliant, verified with Motorola's RapidIO bus functional model v1.4	Routers, switches, backplane, control plane, data path, embedded sys, high speed interface to memory and encryption engines, high end video
USB 1.1 Device Controller	MemecCore	AllianceCORE	V-II	V	S-II		21%	12	XC2V1000-5	Compliant with USB1.1 spec., Supports VCI bus, Performs CRC, Supports 1.5 Mbps & 12 Mbps	Scanners, Printers, Handhelds, Mass Storage
Video & Image Processing											
1-D Discrete Cosine Transform	Xilinx	LogiCORE	V-II	V	S-II					8-24 bits for coeff & input, 8-64 pts	
2-D DCT/IDCT Forward/Inverse Discrete Cosine Transform	Xilinx	LogiCORE	V-II	V	S-II						image, video phone, color laser printers
DCT/IDCT Forward/Inverse Discrete Cosine Transform	inSilicon	AllianceCORE		V	S-II	S	86%	29	XC2S100-6	DCT & IDCT, one clock cycle per sample. 38 MHz when operated as DCT	JPEG, MPEG, H261 designs
FASTJPEG_BW DECODER	BARCO-SILEX	AllianceCORE	V-II	V			67%	73	XC2V1000-4	Conforms to ISO/IEC Baseline 10918-1, Gray-Scale	Video editing, digital camera, scanners
FASTJPEG_C DECODER	BARCO-SILEX	AllianceCORE	V-II	V			78%	56	XC2V1000-4	Conforms to ISO/IEC Baseline 10918-1, color, multi-scan, Gray-Scale	Video editing, digital camera, scanners
FIDCT Forward/Inverse Discrete Cosine Transform	TILAB	AllianceCORE		V	S-II		77%	78	XCV200-6	DCT for 8X8, 16X16, IDCT IEEE1180-1990 compliant	JPEG, MPEG, H.26X
JPEG CODEC	inSilicon	AllianceCORE		V	S-II	S	75%	20	XCV400E-8	Conforms to ISO/IEC Baseline 10918-1, 4 quantization tables, 4 Huffman tables. Stallable	Video editing, digital camera, scanners
logiCVC - Compact Video Controller	xylon	AllianceCORE		V	S-II		35%	88	XC2V250-4	Single & double panel, LCD/CRT support, 4 gray, 256 colors	Video phone, Set-top box, PDA display
Longitudinal Time Code Generator	DELTATEC	AllianceCORE		V			12%	85	XCV100-4	SMTPE/EBU compliant, PAL/NTSC, lock-on external video reference	Audio/Video recording and editing equipment
RGB2YCrCb Color Space Converter	Perigee	AllianceCORE		V	S-II	S	22%	202	XCV100E-8	One clock cycle throughput	HDTV, real time TV output modulation
RGB2YCrCb Color Space Converter Core	Xilinx	LogiCORE		V	S-II		49%	65	XC2S30		TV, HDTV, color imaging, color video
RGB2YUV Color Space Converter Core	Xilinx	LogiCORE		V	S-II		53%	80	XC2S30		TV, HDTV, color imaging, color video
YCrCb2RGB Color Space Converter	Perigee	AllianceCORE		V	S-II	S	16%		XCV100E-8	One clock cycle throughput	HDTV, real time video
YCrCb2RGB Color Space Converter	Xilinx	LogiCORE		V	S-II		15%	70	XC2S100		TV, HDTV, color imaging, color video
YUV2RGB Color Space Converter	Xilinx	LogiCORE		V	S-II		12%	65	XC2S100		TV, HDTV, color imaging, color video
Basic Elements											
BUFE-based Multiplexer Slice	Xilinx	LogiCORE	V-II	V	S-II					1-256 bits wide	
BUFT-based Multiplexer Slice	Xilinx	LogiCORE	V-II	V	S-II					1-256 bits wide	
Binary Counter	Xilinx	LogiCORE	V-II	V	S-II					2-256 bits output width	
Binary Decoder	Xilinx	LogiCORE	V-II	V	S-II					2-256 bits output width	
Bit Bus Gate	Xilinx	LogiCORE	V-II	V	S-II					1-256 bits wide	
Bit Gate	Xilinx	LogiCORE	V-II	V	S-II					1-256 bits wide	
Bit Multiplexer	Xilinx	LogiCORE	V-II	V	S-II					1-256 bits wide	
Bus Gate	Xilinx	LogiCORE	V-II	V	S-II					1-256 bits wide	
Bus Multiplexer	Xilinx	LogiCORE	V-II	V	S-II					IO widths up to 256 bits	
Comparator	Xilinx	LogiCORE	V-II	V	S-II					1-256 bits wide	
FD-based Parallel Register	Xilinx	LogiCORE	V-II	V	S-II					1-256 bits wide	
FD-based Shift Register	Xilinx	LogiCORE	V-II	V	S-II					1-64 bits wide	
Four-Input MUX	Xilinx	LogiCORE				S					
LD-based Parallel Latch	Xilinx	LogiCORE	V-II	V	S-II					1-256 bits wide	
Parallel-to-Serial Converter	Xilinx	LogiCORE				S					
RAM-based Shift Register	Xilinx	LogiCORE	V-II	V	S-II					1-256 bits wide, 1024 words deep	
Register	Xilinx	LogiCORE				S					
Three-Input MUX	Xilinx	LogiCORE				S					
Two-Input MUX	Xilinx	LogiCORE				S					

Function	Vendor Name	IP Type	Virtex-II	Virtex	Spartan-II	Spartan	Occupancy	MHz	Device	Key Features	Application Examples
Communication & Networking (continued)											
Reed-Solomon Decoder	TILAB	AllianceCORE	V-II	V			56%	61	XC2V1000-5	parameterizable, RTL available	Error correction, wireless, DSL
Reed-Solomon Encoder	Xilinx	LogiCORE	V-II	V	S-II	S	42%	180	XC2V40	Std or cust coding, 3-12 bit width, up to 4095 symbols with 256 check symb	Broadcast, wireless LAN, cable modem, xDSL, satellite com,uwave nets, digital TV
SDLC Controller	CAST	AllianceCORE	V-II	V			38%	158	XC2V100-5	Like Intel 8XC152 Global Serial Channel, Serial Comm., HDLC apps, telecom	Embedded systems, professional audio, video
Single-Channel XF-HDLC Controller	MemecCore	AllianceCORE		V	S-II		95%	77	XC2S15-5	16/32-bit frame seq, 8/16-bit addr insert/delete, flag/zerop insert/detection	X.25, Frame Relay, B/D-Channel
SPEEDROUTER Network Processor	IP	AllianceCORE	V-II	V			64%	80, 2.5Gbps	XC2V1500-5	Solution requires SPEEDAnalyzer ASIC, 2.5 Gbps fdx wire speed; net processor (NPV)	Networking, edge and access, Switches and routers
T1 Deframer	Xilinx	LogiCORE		V	S-II		15%	54	XC2S150		ISDN PRA links, mux equip, satellite com, digital PABX, high-speed computer links
T1/E1 Framer	Xilinx	LogiCORE		V	S-II		7%	72	XC2S150		ISDN PRA links, mux equip, satellite com, digital PABX, high-speed computer links
Turbo Decoder - 3GPP	SysOnChip	AllianceCORE	V-II	V			88%	65	XC2V2000-5	3GPP/UMTS compliant, 2Mbps data rate	Error correction, wireless
Turbo Encoder	TILAB	AllianceCORE	V-II	V	S-II		48%	120	XC2V80-5	3GPP/UMTS compliant, upto 4 interleaver laws	Error correction, wireless
TURBO_DEC Turbo Decoder	TILAB	AllianceCORE	V-II	V			99%	65	XC2V2000-5	3GPP/UMTS compliant, >2Mbps data rate	Error correction, wireless
UTOPIA Level-2 PHY Side RX Interface	TILAB	AllianceCORE		V	S-II	S	8%	53	XCV50-6	Protocol conversion from Pb (RACE BLNT) to UTOPIA L2, 8/16 bit operation	ATM PHY layer
UTOPIA Level-2 PHY Side TX Interface	TILAB	AllianceCORE		V	S-II	S	10%	61	XCV50-6	Protocol conversion from UTOPIA L2 Pb (RACE BLNT), 8/16 bit operation	ATM PHY layer
UTOPIA Level-3 ATM Receiver	inSilicon	AllianceCORE		V	S-II	S	5%	164	XCV100E-8	Supports ATM Forum UTOPIA Level-3. Configurable cell format, data width	High capacity ATM switches
UTOPIA Level-3 ATM Transmitter	inSilicon	AllianceCORE		V	S-II	S	6%	150	XCV100E-8	Supports ATM Forum UTOPIA Level-3. Configurable cell format, data width	High capacity ATM switches
UTOPIA Level-3 PHY Receiver	inSilicon	AllianceCORE		V	S-II	S	21%	104	XCV100E-8	Supports ATM Forum UTOPIA Level-3. Configurable cell format, data width, configurable FIFO size	High capacity ATM switches
UTOPIA Level-3 PHY Transmitter	inSilicon	AllianceCORE		V	S-II	S	22%	100	XCV100E-8	Supports ATM Forum UTOPIA Level-3. Configurable cell format, data width, configurable FIFO size	High capacity ATM switches
UTOPIA Master (CC140f)	Paxonet	AllianceCORE		V	S-II	S	*	*	*	SPHY, MPHY, HEC processing, round robin polling, ind. transmitter receiver	ATM PHY layer
UTOPIA Slave (CC141)	Paxonet	AllianceCORE				S	*	*	*	Cell handshake in SPHY mode, 8/16 bit operation, internal FIFO, detects runt cells	ATM PHY layer
UTOPIA Slave (CC143S)	Paxonet	AllianceCORE		V	S-II	S	26%	79	XCV50-4	Cell handshake in SPHY mode, 8/16 bit operation, internal FIFO, detects runt cells	ATM PHY layer
Viterbi Decoder	TILAB	AllianceCORE		V	S-II	S	65%	56	XCV50-6	Radix-2/radix4 architectures, BER, depuncturing, Code rate, contraint length parameterizable	Data transmission, wireless
Viterbi Decoder	Xilinx	LogiCORE	V-II	V	S-II		80%	100	XC2V250	Puncturing, serial & parallel architecture,	3G base stations, broadcast, wireless LAN, cable modem, xDSL, satellite com, uwave
Viterbi Decoder, IEEE 802-compatible	Xilinx	LogiCORE	V-II	V	S-II		70%	147	XC2V250	Constraint length(k)=7, G0=171, G1=133	LMMDS, broadcast equip, wireless LAN, cable modem, xDSL, sat com, uwave nets
Digital Signal Processing											
1024-Point Complex FFT IFFT	Xilinx	LogiCORE		V							
1024-Point Complex FFT IFFT for Virtex-II	Xilinx	LogiCORE	V-II				62%	100, 41us	XC2V500	16 bit complex data, 2's comp, forward and inverse transform	
16-Point Complex FFT / IFFT	Xilinx	LogiCORE	V-II	V							
16-Point Complex FFT IFFT for Virtex-II	Xilinx	LogiCORE	V-II				37%	130, 123ns	XC2V500	16 bit complex data, 2's comp, forward and inverse transform	
256-Point Complex FFT / IFFT	Xilinx	LogiCORE	V-II	V							
256-Point Complex FFT IFFT for Virtex-II	Xilinx	LogiCORE	V-II				54%	100, 7.7us	XC2V500	16 bit complex data, 2's comp, forward and inverse transform	
32 Point Complex FFT/IFFT	Xilinx	LogiCORE	V-II	V	S-II						
64-Point Complex FFT IFFT	Xilinx	LogiCORE		V							
64-Point Complex FFT IFFT for Virtex-II	Xilinx	LogiCORE	V-II				38%	100, 1.9us	XC2V500	16 bit complex data, 2's comp, forward and inverse transform	
Bit Correlator	Xilinx	LogiCORE	V-II	V	S-II					4096 taps, serial/parallel input, 4096 bits width	
Cascaded Integrator Comb (CIC)	Xilinx	LogiCORE	V-II	V	S-II					32 bits data width, rate change from 8 to 16384	
Comb Filter	Xilinx	LogiCORE				S					
Direct Digital Synthesizer	Xilinx	LogiCORE	V-II	V	S-II					8-65K samples, 32-bits output precision, phase dithering/offset	
Distributed Arithmetic FIR Filter	Xilinx	LogiCORE	V-II	V	S-II					32-bit input/coeff width, 1024 taps, 1-8 chan, polyphase, online coeff reload	
Dual-Channel Numerically Controlled Oscillator	Xilinx	LogiCORE		V	S-II	S					
GVA-200A DSP Hardware Accelerator	GV	AllianceCORE				S	NA	NA	*	Ext SRAM I/F	DSP prototyping
GVA-220 DSP Hardware Accelerator	GV	AllianceCORE				S	NA	NA	*	Ext SRAM I/f, 2 FPGA's	DSP prototyping
GVA-250 Virtex DSP Hardware Accelerator	GV	AllianceCORE		V			NA	NA	*	2 FPGAs, 2 SRAMs	DSP prototyping
GVA-270 Virtex-E DSP Hardware Accelerator	GV	AllianceCORE		V			NA	NA	*	Virtex-E support, 2 FPGAs, ZBT SRAMs	DSP prototyping
GVA-290 Virtex-E DSP Hardware Accelerator	GV	AllianceCORE		V			NA	NA	*	2 Virtex-E, Spartan-II FPGAs, 1 CPLD, Matlab I/F	DSP prototyping
GVA-300 Virtex-II DSP Hardware Accelerator	GV	AllianceCORE	V-II				NA	NA	*	2 Virtex-II, Spartan-II FPGAs, 1 CPLD, Matlab I/F	DSP prototyping
LFSR, Linear Feedback Shift Register	Xilinx	LogiCORE	V-II	V	S-II					168 input widths, SRL16/register implementation	
Nonsymmetric 16-Deep Time-Skew Buffer	Xilinx	LogiCORE				S					
Nonsymmetric 32-Deep Time-Skew Buffer	Xilinx	LogiCORE				S					
Numerically Controlled Oscillator	Xilinx	LogiCORE		V	S-II	S					
Parallel Distributed Arithmetic FIR Filter	Xilinx	LogiCORE				S					
Serial Distributed Arithmetic FIR Filter	Xilinx	LogiCORE				S					
Symmetric 16 Deep Time-Skew Buffer	Xilinx	LogiCORE				S					
Math Functions											
1s and 2s Complement	Xilinx	LogiCORE				S					
Accumulator	Xilinx	LogiCORE	V-II	V	S-II					1-256s bit wide	
Adder Subtracter	Xilinx	LogiCORE	V-II	V	S-II					1-256s bit wide	
Constant Coefficient Multiplier	Xilinx	LogiCORE				S					
Constant Coefficient Multiplier - Pipelined	Xilinx	LogiCORE				S					
DFP2INT Floating Point to Integer Converter	Digital	AllianceCORE	V-II	V	S-II		39%	66	XC2V250-5	Full IEEE-754 compliance, 4 pipelines, Single precision real format support	DSP, Math, Arithmetic apps
DFPADD Floating Point Adder	Digital	AllianceCORE	V-II	V	S-II		39%	66	XC2V250-5	Full IEEE-754 compliance, 4 pipelines, Single precision real format support	DSP, Math, Arithmetic apps
DFPCOMP Floating Point Comparator	Digital	AllianceCORE	V-II	V	S-II		16%	91	XC2V80-5	Full IEEE-754 compliance, 4 pipelines, Single precision real format support	DSP, Math, Arithmetic apps.
DFPDIV Floating Point Divider	Digital	AllianceCORE	V-II	V	S-II		99%	53	XC2V250-5	Full IEEE-754 compliance, 15 pipelines Single precision real format support	DSP, Math, Arithmetic apps
DFPMUL Floating Point Multiplier	Digital	AllianceCORE	V-II	V	S-II		44%	74	XC2V250-5	Full IEEE-754 compliance, 7 pipelines, 32x32 mult, Single precision real format support	DSP, Math, Arithmetic apps.
DFPSQRT Floating Point Square Root	Digital	AllianceCORE	V-II	V	S-II		39%	66	XC2V250-5	Full IEEE-754 compliance, 4 pipelines, Single precision real format support	DSP, Math, Arithmetic apps
DINT2FF Integer to Floating Point Converter	Digital	AllianceCORE	V-II	V	S-II		37%	73	XC2V250-5	Full IEEE-754 compliance, double word input, 2 pipelines, Single precision real output	DSP, Math, Arithmetic apps
Dynamic Constant Coefficient Multiplier	Xilinx	LogiCORE		V							
Integrator	Xilinx	LogiCORE				S					
Multiply Accumulator (MAC)	Xilinx	LogiCORE	V-II	V	S-II					Input width up to 32 bits, 65-bit accumulator, truncation rounding	
Multiply Generator	Xilinx	LogiCORE	V-II	V	S-II					64-bit input data width, constant, reloadable or variable inputs, parallel/sequential implementation	
Parallel Multipliers Area Optimized	Xilinx	LogiCORE				S					
Pipelined Divider	Xilinx	LogiCORE	V-II	V	S-II	S				32-bit input data width, multiple clock per output	
Registered Adder	Xilinx	LogiCORE				S					
Registered Loadable Adder	Xilinx	LogiCORE				S					

Function	Vendor Name	IP Type	Virtex-II	Virtex	Spartan-II	Spartan	Implementation Example: Occupancy	MHz	Device	Key Features	Application Examples
Math Functions (continued)											
Registered Loadable Subtracter	Xilinx	LogiCORE				S					
Registered Scaled Adder	Xilinx	LogiCORE				S					
Registered Serial Adder	Xilinx	LogiCORE				S					
Registered Subtracter	Xilinx	LogiCORE				S					
Scaled-by-One-Half Accumulator	Xilinx	LogiCORE				S					
Sine Cosine Look Up Table	Xilinx	LogiCORE	V-II	V	S-II	S				3-10 bit in, 4-32 bit out, distributed/block ROM	
Square Root	Xilinx	LogiCORE				S					
Twos Complementer	Xilinx	LogiCORE	V-II	V	S-II					Input width up to 256 bits	
Variable Parallel Virtex Multiplier	Xilinx	LogiCORE		V	S-II						
Memories & Storage Elements											
Asynchronous FIFO	Xilinx	LogiCORE	V-II	V	S-II					1-256 bits, 15-65535 words, DRAM or BRAM, independent I/O clock domains	
Content Addressable Memory (CAM)	Xilinx	LogiCORE	V-II	V	S-II					1-512 bits, 2-10K words, SRL16	
Distributed Memory	Xilinx	LogiCORE	V-II	V	S-II					1-1024 bit, 16-65536 word, RAM/ROM/SRL16, opt output regs and pipelining	
Dual-Port Block Memory	Xilinx	LogiCORE	V-II	V	S-II					1-256 bits, 2-13K words	
Pipelined Delay Element	Xilinx	LogiCORE				S					
Registered ROM	Xilinx	LogiCORE				S					
Registered Single Port RAM	Xilinx	LogiCORE				S					
Single-Port Block Memory	Xilinx	LogiCORE	V-II	V	S-II					1-256 bits, 2-128K words	
Synchronous FIFO	Xilinx	LogiCORE				S					
Synchronous FIFO	Xilinx	LogiCORE	V-II	V	S-II					1-256 bits, 16-256 words, distributed/block RAM	
Microprocessors, Controllers & Peripherals											
10/100 Ethernet MAC	Xilinx	LogiCORE	V-II	V	S-II				Virtex-II	Interfaces through OPB to MicroBlaze	Networking, communications, processor apps
16-Word-Deep Registered Look Up Table	Xilinx	LogiCORE				S					
200 MHz SDRAM Controller Core	Rapid	AllianceCORE		V	S-II						
ARC 32-bit Configurable RISC Processor	ARC	AllianceCORE		V	S-II		89%	37	XC2S150-6	4 stage pipeline, 16 single cycle instructions10, 3 interrupt exception levels, 24 bit stack pointer	32 bit processing, DSP
AX161C 16-bit RISC Processor	Loarant	AllianceCORE	V-II	V	S-II		12%	91	XC2V500-5	44 opcode, 64-K word data, program, Harvard arch.	Control functions, State mach, Coprocessor
C16450 UART	CAST	AllianceCORE		V	S-II		29%	60	XC2S50-6	Independently controlled transmit, receive and data interrupts. 16X clock	Serial data applications, modems
C16550 UART with FIFOs	CAST	AllianceCORE		V	S-II			51	XC2S50-6	Prog. Data width, parity, stop bits. 16X internal clock, FIFO mode, false start bit detection	Serial data applications, modems
C165X MicroController	CAST	AllianceCORE	V-II	V	S-II		60%	134	XC2V80-5	Microchip 16C5X PIC like	Embeddec systems, telecom
C2901 Microprocessor Slice	CAST	AllianceCORE		V	S-II		19%	36	XC2S50-6	Eight function ALU, 4 status flags- Carry, Overflow, Zero and Negative	Simple microcontroller applications
C2910a Microprogram Controller	CAST	AllianceCORE		V	S-II	S	13%	63	XCV50-6	Based on AMD 2910a	High-speed bit slice design
C68000 Microprocessor	CAST	AllianceCORE	V-II	V			90%	32	XC2V500-5	MC68000 Compatible	Embedded systems, pro audio, video
C8051 MicroController	CAST	AllianceCORE		V	S-II		52%	68	XCV200E-8	80C31 instruction set, 8 bit ALU, 8 bit control, 32 bit I/O ports, two 16 bit timer/counters, SFR I/F	Embeddec systems, telecom
C8250 UART	CAST	AllianceCORE		V	S-II			98	XCV50E-8	UART & Baud rate generator, 16X clock generator, loopback & echo modes	Serial data applications, modems
C8254 Programmable Interval Timer/Counter	CAST	AllianceCORE		V	S-II		38%	66	XCV100E-8	Status feedback, counter latch, square wave mode, binary/BCD count, LSB/MSB R/W	Event counter, baud rate generator
C8255A Peripheral Interface	CAST	AllianceCORE		V	S-II		10%	227	XCV50E-8	Three 8-bit peripheral ports, 24 programmable IO lines, 8-bit bidi data bus	Processor I/O interface
C8259A Programmable Interrupt Controller	CAST	AllianceCORE		V	S-II		28%	47	XC2S50-6	8 vectored priority interrupts, all 8259/A modes programmable- e.g., special mask, buffer	Real-time interrupt based uP designs
Compact UART	CAST	AllianceCORE		V	S-II	S	7%	142	XCV50-6	1 start bit, 1 stop bit. Polling and interrupt modes	Serial data applications, modems
Compact Version of D80530 Microcontroller	CAST	AllianceCORE		V	S-II		88%	51	XC2S150-6	32 bit I/O, 3 counters, interrupt controller, SFR interface, dual data pointer	Low cost embedded systems, telecom
CPU + FPGA (Virtex/Spartan-II) MicroEngine Cards	NMI	AllianceCORE		V	S-II		NA	NA	NA	Hitachi SH-4 CPU	Embedded systems
CPU + FPGA (Virtex-II) MicroEngine Cards	NMI	AllianceCORE	V-II				NA	NA	NA	Hitachi SH-3 CPU	Embedded systems
CZ80CPU Microprocessor	CAST	AllianceCORE	V-II	V	S-II		55%	72	XC2V500-5	Zilog Z80 compatible, 8-bit processor	Embedded systems, Communications
D8053C 8-bit Microcontroller	CAST	AllianceCORE		V			81%	66	XCV200E-8	32 bit I/O, 3 counters, 27-bit watchdog timer, 3-priority interrupt controller, SFR interface	Embeddec systems, telecom
DDR SDRAM Controller Core	MemecCore	AllianceCORE	V-II	V	S-II		7%	133	XC2V1000-4	DDR SDRAM burst length support for 2,4, 8 per access, supports data 16, 32, 64, 72	Digital video, embedded computing , networking
DFPIC125X Fast RISC MicroController	Digital	AllianceCORE	V-II	V	S-II		49%	126	XC2V80-5	PIC 12c4x like, 2X faster, 12-bit wide instruction set, 33 instructions	Embedded systems, telecom, audio and video
DFPIC1655X Fast RISC MicroController	Digital	AllianceCORE	V-II	V	S-II		79%	140	XC2V80-5	S/W compatible with PIC16C55X, 14-bit instruction set, 35 instructions	Embedded systems, telecom, audio and video
DFPIC165X Fast RISC MicroController	Digital	AllianceCORE	V-II	V	S-II		49%	126	XC2V80-5	PIC 12c4x like, 2X faster, 12-bit wide instruction set, 33 instructions	Embedded systems, telecom, audio and video
DI2CM I2C Bus Controller Master	Digital	AllianceCORE	V-II	V	S-II	S	58%	143	XC2V50-5	I2C-like, multi master, fast/std. modes	Embedded systems
DI2CM I2C Bus Controller Slave	Digital	AllianceCORE	V-II	V	S-II	S	28%	157	XC2V50-5	I2C-like, Slave	Embedded
DI2CSB I2C Bus Controller Slave Base	Digital	AllianceCORE	V-II	V	S-II	S	15%	187	XC2V50-5	I2C-like, Slave	Embedded Systems
DR8051 RISC MicroController	Digital	AllianceCORE	V-II	V	S-II		68%	73	XC2V250-5	80C31 instruction set, RISC architecture 6.7X faster than standard 8051	Embedded systems, telecom, video
DR8051BASE RISC MicroController	Digital	AllianceCORE	V-II	V	S-II		46%	80–90	XC2V250-5	80C31 instruction set, high speed multiplier, RISC architecture 6.7X faster than standard 8051	Embedded systems, telecom, video
DR8052EX RISC MicroController	Digital	AllianceCORE	V-II	V	S-II		99%	71	XC2V250-5	80C31 instruction set, high speed mult/div ,RISC 6.7X faster than standard 8051	Embedded systems, telecom, video
e8254 Programmable Interval Timer/Courter	einfochips	AllianceCORE	V-II	V	S-II		1%	175	XC2V1000-5	Three 8-bit parallel ports, 24 programmable IO lines, 8-bit bidi data bus	Processor, I/O interface
e8255 Peripheral Interface	einfochips	AllianceCORE	V-II	V	S-II		1%	175	XC2V1000-5	Three 8-bit parallel ports, 24 programmable IO lines, 8-bit bidi data bus	Processor, I/O interface
EP520 SDRAM Controller	Eureka	AllianceCORE		V	S-II						
Flip805x-PR Core	Dolphin	AllianceCORE		V	S-II	S	68%	20	XC2S150-6	Avg 12X faster and code compatible v. legacy 8051, verification bus monitor, SFR interface	Telecom, industrial, high speed control
Flip805x-PS Microprocessor	Dolphin	AllianceCORE	V-II	V	S-II		39%	38	XC2V1000-5	Avg 8X faster & code compatible v. legacy 8051, verification bus monitor, SFR IF, DSP focused	DSP, Telecom, industrial, high speed control
IIC	Xilinx	LogiCORE	V-II	V	S-II				Virtex-II	Interfaces through OPB to MicroBlaze	Networking, communications, processor apps
IntelliCore Prototyping System	VAutomation	AllianceCORE					*	*	*	USB, 1394, 1284, RS-232, IVDA I/F	Prototyping
LavaCORE Configurable Java Processor Core	Derivation	AllianceCORE	V-II	V			38%	20	XC2V1000-5	32b data/address optional DES	Internet appliance, industrial control
LavaCORE Configurable Java Processor Core	Derivation	AllianceCORE	V-II	V			38%	20	XC2V1000-5	32b data/address optional DES	Internet appliance, industrial control
Lightfoot 32-bit Java Processor Core	Digital	AllianceCORE	V-II	V	S-II		33%	40	XC2V1000-5	32bit data, 24 bit address, 3 Stage pipeline, Java/C dev. tools	Internet appliance, industrial control, HAVi multimedia, set top boxes
M16450 Universal Asynchronous Receiver Transmitter	Virtual	AllianceCORE				S	29%	60	XC2S50-6	Independently controlled transmit, receive and data interrupts. 16X clock	Serial data applications, modems
M16550A UART with FIFOs	Virtual	AllianceCORE				S	90%	16	XCS20-4	Prog. Data width, parity, stop bits. 16X internal clock, FIFO mode, false start bit detection	Serial data applications, modems
M8254 Programmable Timer	Virtual	AllianceCORE		V	S-II	S					
M8255 Programmable Peripheral Interface	Virtual	AllianceCORE		V	S-II	S	10%	227	XCV50E-8	Three 8-bit peripheral ports, 24 programmable I/O lines, 8-bit bidi data bus	Processor I/O interface
M8259 Programmable Interrupt Controller	Virtual	AllianceCORE				S	28%		XC2S50-6	8 vectored priority interrupts, all 8259/A modes programmable – e.g., special mask, buffer	Real-time interrupt based uP designs
MicroBlaze Soft RISC Processor	Xilinx	LogiCORE	V-II	V	S-II		1%	125	XC2V6000	Soft RISC Processor, small footprint	Networking, communications
OPB Arbiter	Xilinx	LogiCORE	V-II	V	S-II			125	Virtex-II	Bundled in the MicroBlaze Development Kit	Processor applications
OPB GPIO	Xilinx	LogiCORE	V-II	V	S-II			125	Virtex-II	Bundled in the MicroBlaze Development Kit	Processor applications
OPB Interrupt Controller	Xilinx	LogiCORE	V-II	V	S-II			125	Virtex-II	Bundled in the MicroBlaze Development Kit	Processor applications
OPB Memory Interface (Flash, SRAM)	Xilinx	LogiCORE	V-II	V	S-II			125	Virtex-II	Bundled in the MicroBlaze Development Kit	Processor applications

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Xilinx Global Services

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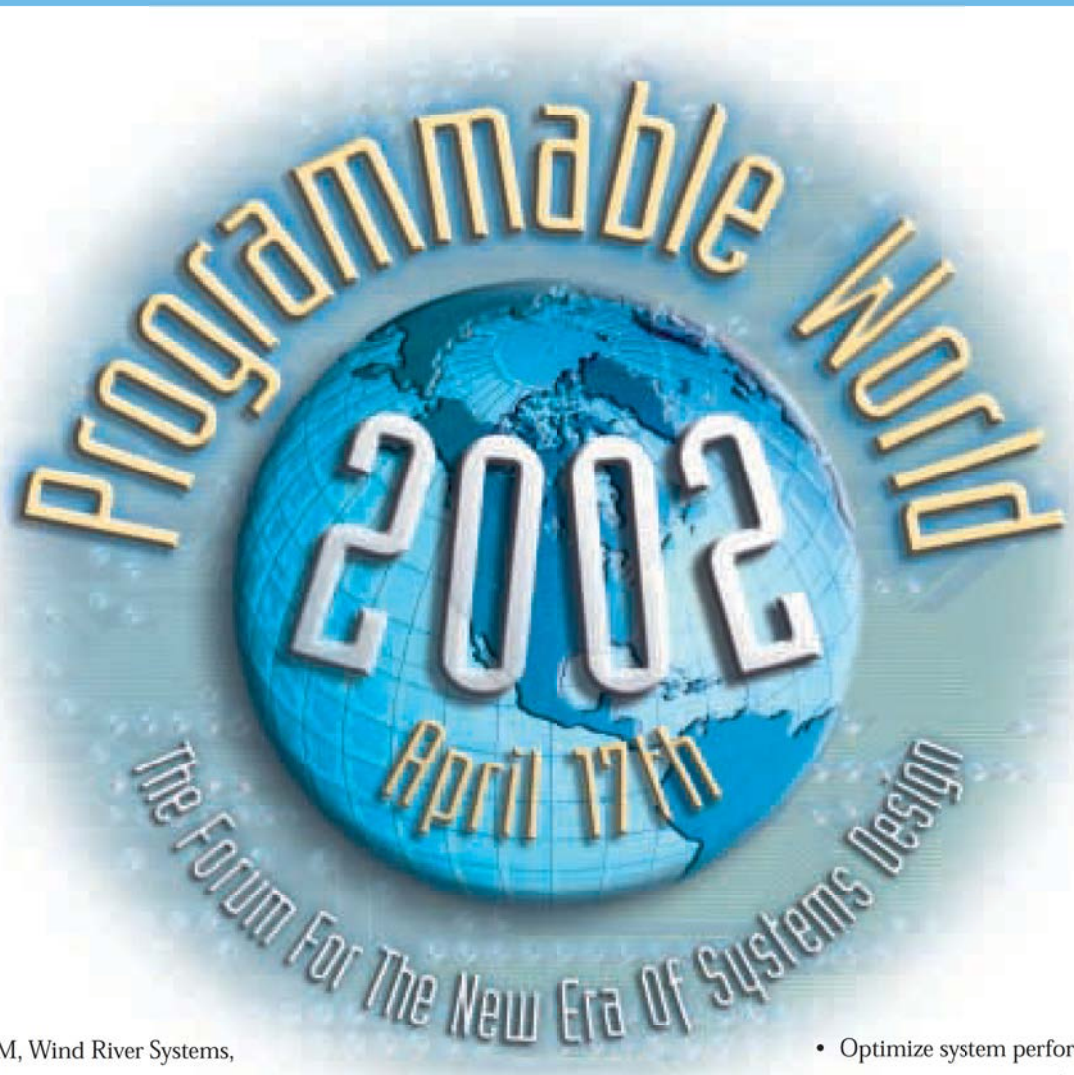

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