UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

ARBOR GLOBAL STRATEGIES LLC,
Patent Owner.

_____

Case IPR2020-01021
U.S. Patent No. 7,282,951

PATENT OWNER'S RESPONSE

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Exhibit-2010	Excerpts from Expert Report of Dr. Gabriel Robins on the Technical Background and Invalidity of U.S. Patent Nos. 6,781,226; 7,282,951; and RE42.035, *Arbor Global Strategies, LLC v. Samsung Elecs. Co., et al*., No. 19-cv-00333-JRG, dated December 7, 2020
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On May 29, 2020, Samsung Electronics Co., Ltd. ("Samsung" or "Petitioner") submitted a Petition to institute *inter partes* review of Arbor Global Strategies, LLC's ("Arbor" or "Patent Owner") U.S. Patent No. 7,282,951 (Ex. 1001, "the '951 Patent"), challenging Claims 1, 4, 5, 8, 10, 13, 14, and 15 ("the Challenged Claims"). The Board instituted trial on December 2, 2020. *See* Paper 11 ("Institution Decision"). Arbor requests that the Board find the Challenged Claims patentable because Petitioner has not proved by a preponderance of the evidence that any claim of the '951 Patent is unpatentable.

I. INTRODUCTION

The innovations in the '951 Patent relate to a new type of integrated circuit ("IC") module referred to the in the Specification as a "stacked die hybrid ("SDH") processor, which combines a microprocessor with cache memory and reprogrammable processor, such as a field programmable gate array ("FPGA"). The inventors of the SDH processors recited in the Challenged Claims overcame a number of significant technical challenges to realize a general purpose reconfigurable processor ("GPRP"). For example, previous attempts to create a GPRP were too large for many applications and took too long to reconfigure. In order to solve these problems, the inventive SDH processor arranges die-area contacts, such as through-silicon vias ("TSVs"), into a wide configuration data port that not only dramatically increases the number and decreases the length of

available connections between the SDH dies but also includes a memory array that accelerates memory references to the reprogrammable processor by use of specially configured buffer cells.

Petitioner presents no evidence that a SDH processor including a microprocessor and programmable array was known in the art prior to the '951 Patent. Instead, Petitioner asserts that the *Koyanagi* and *Bertin* references disclose "universal" 3D integration techniques sufficient to demonstrate that a person of ordinary skill in the art would have had a reasonable expectation of success in rearranging the elements of known GPRPs into the claimed SDH formation. Petitioner's argument vastly oversimplifies the state of the art and fails to acknowledge, let alone confront, a number of significant challenges, including how to make use of die-area connections and buffer cells to accelerate data to a reconfigurable processor and how to dissipate heat from a stacked processor having two processing elements.

Furthermore, Petitioner fails to demonstrates that *Koyanagi* in view of *Alexander* or *Bertin* in view of *Cooke* teach or suggest the element of "a memory array functional to accelerate external memory references to the programmable array [/processing element]" recited in Independent Claims 1, 5, and 10. Rather than demonstrating that these reference combinations disclose the novel memory array claimed in the independent claims and responsible for performing the

claimed acceleration, as shown in Figure 5, Petitioner ignores the disclosure of Figure 5 and falsely asserts that the claimed acceleration is attributable to the stacking of dies.

Because Petitioner failed to meet its statutory burden of demonstrating unpatentability by a preponderance of the evidence pursuant to 35 U.S.C. § 316(e), patentability of the challenged claims should be confirmed.

II. THE '951 PATENT

The '951 Patent is directed to an SDH processor module that includes hybrid stacked integrated circuit die elements. '951 Patent at Abstract. Specifically, the '951 Patent discloses stacking a thinned microprocessor die element, a thinned memory die element, and a thinned programmable array (*e.g.* an FPGA) die element and interconnecting the die elements using contacts that traverse the thickness of each die rather than being routed around the periphery of the stacked die elements. *Id.* at 2:41-46; *see also* Ex. 2015 (Declaration of Krishnendu Chakrabarty ("Chakrabarty Decl.")), ¶35.

The reconfigurable processor module has a memory array for the purpose of accelerating external memory references to the programmable array. '951 Patent at 2:65-3:2. As shown below in FIG. 5, memory array includes buffer cells 88. The '951 Patent explains how electrical connections, such as TSVs, are used to load configuration data in a parallel fashion to buffer cells in the memory array while

the programmable array is in operation. *Id.* at 5:29-43. Then, the configuration data can be loaded, in parallel, into configuration memory resulting in an acceleration of memory references to the programmable array. *Id*; *see also* Chakrabarty Decl., ¶36.

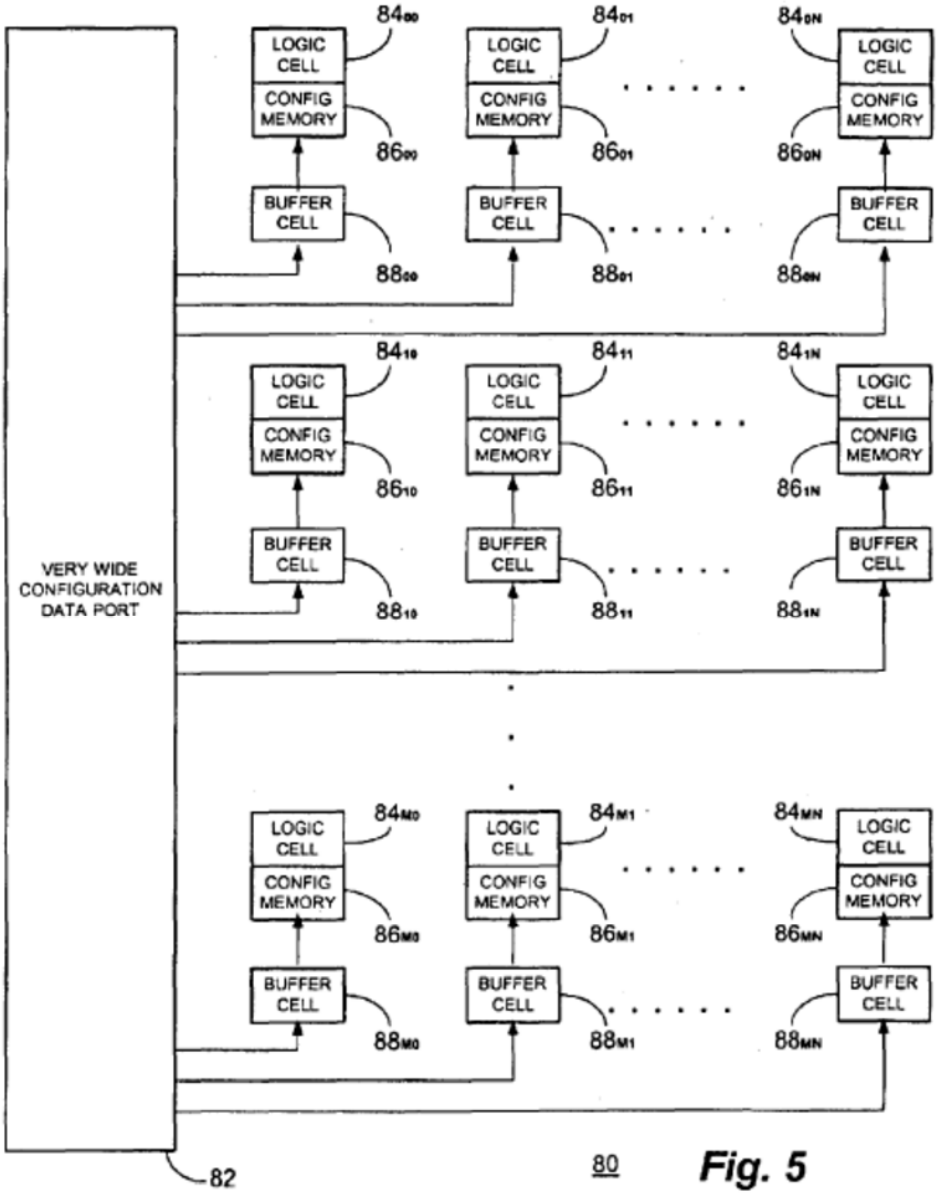


Fig. 5

'951 Patent at FIG. 5.

III. LEVEL OF ORDINARY SKILL

A person of ordinary skill in the art ("POSITA") around December 5, 2001 (the earliest effective filing date of the '951 Patent) would have had a Bachelor's degree in Electrical Engineering or a related field, and either (1) two or more years of industry experience; and/or (2) an advanced degree in Electrical Engineering or related field. *See* Chakrabarty Decl., ¶33.

IV. CLAIM CONSTRUCTION

Patent Owner sets forth the following claim construction positions to address Petitioner's overbroad interpretation of the Challenged Claims so that the Board can resolve the controversy between the parties. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) ("[W]e need only construe terms 'that are in controversy, and only to the extent necessary to resolve the controversy.'") (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)). Patent Owner explicitly reserves the right to address further mischaracterizations of claim terms in this and any other proceedings concerning the '951 Patent.

A. "a memory array functional to accelerate external memory references to the processing element [/ said programmable array]" (Claims 1, 5, and 10)

In its preliminary response, Patent Owner advocated that this term should be accorded its plain and ordinary meaning, which is "a memory array that functions

to accelerate external memory references to the processing element." *See* '951 Patent at 2:64-3:2. However, the Board adopted in its Institution Decision, and on the preliminary record, a construction of "a number of vertical contacts that traverse the memory die in the internal periphery of the die and provide contacts on the surface of the memory die." Institution Decision at 24.

Patent Owner respectfully requests that the Board reconsider its preliminary construction because it is inconsistent with Claims 1 and 15 and with how a POSITA would understand this term in the context of the entire patent disclosure. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc) ("the person of ordinary skill in the art is deemed to read the claim term…in the context of the entire patent, including the specification.").

First, as discussed in Patent Owner's Preliminary Response, the claim requires a memory array—not a number of contact points—that is functional to accelerate external memory references to the processing element. Preliminary Response at 18.

The term "a memory array functional to accelerate external memory references to the processing element" means "a memory array that allows the parallel loading of data through buffer cells." This construction is consistent with the specification and how a POSITA would understand this term in the context of patent. *See* Chakrabarty Decl., ¶38. The specification discloses that the memory

array includes buffer cells 88, as shown in Figure 5. *See* '951 Patent at 5:38-40 ("buffer cells 88 are preferably a portion of the memory die 66). The buffer cells 88 of the memory array are indicated in blue below:

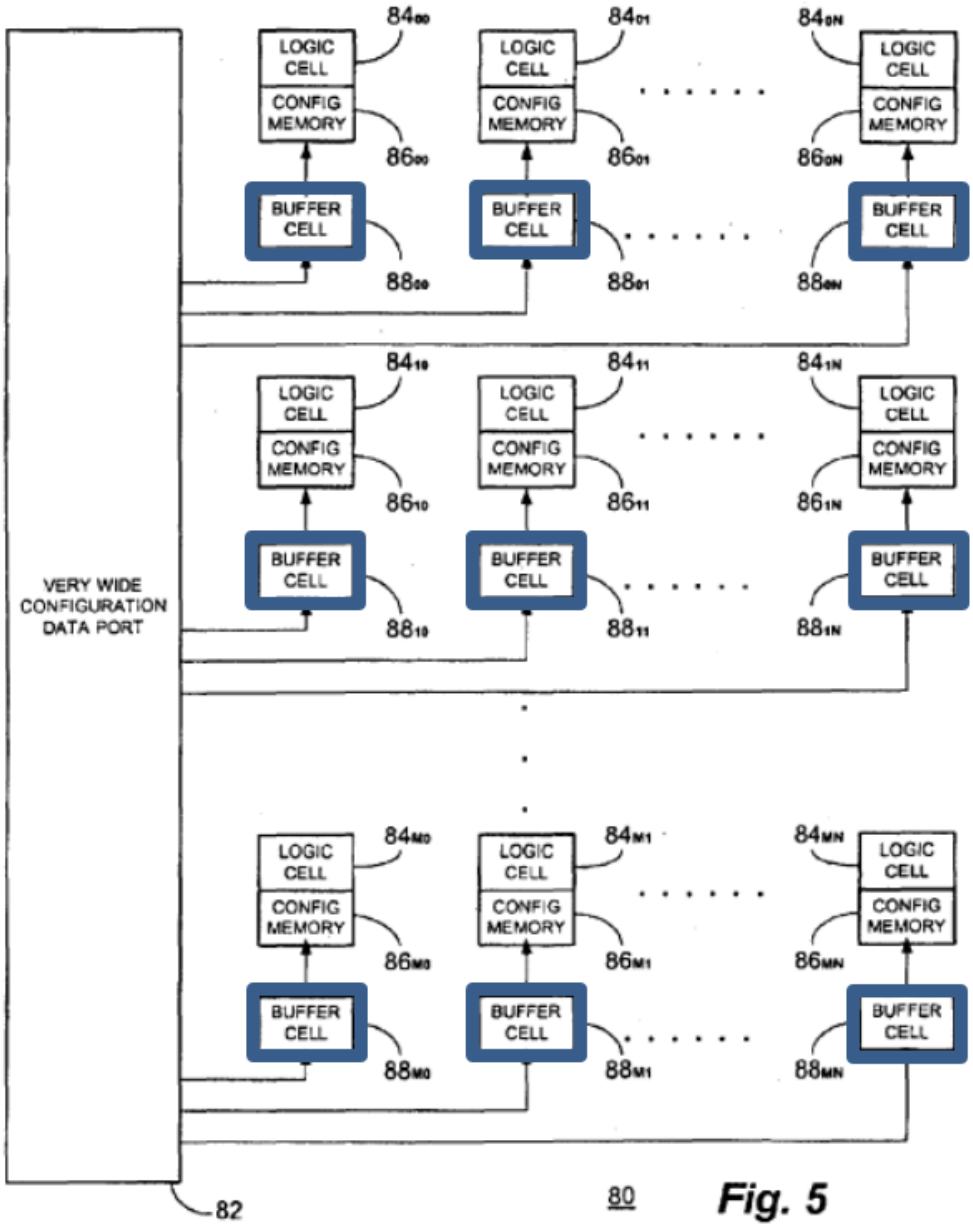


Fig. 5

Id. at FIG. 5 (annotated). The specification discloses that the buffer cells 88 (which are associated with the wide configuration data port) can be loaded in parallel with configuration data while the FPGA is in operation. *Id*. at 5:29-39. As a result of the parallel loading of data into the buffer cells while the FPGA and its logic cells are in operation, the memory array can accelerate memory references to the configuration memory 86 of the FPGA (because it doesn't need to wait for the FPGA to cease operating), as compared to a configuration that did not include the disclosed buffer cells. *Id.* at 5:42-44 ("FPGA 68 [can] be totally reconfigured in one clock cycle with all of its configuration logic cells 84 updated in parallel."); *see also* Chakrabarty Decl., ¶38.

Second, Patent Owner disagrees that the Board's preliminary construction represents the ordinary and customary meaning of the term as understood by one of ordinary skill in the art. In particular, the Board's preliminary construction describes an "***internal periphery***" of a die. Institution Decision at 24 (emphasis added). But the term "internal periphery" is not described in the specification, and will not add clarity to the meaning of the term. *See* Chakrabarty Decl., ¶39.

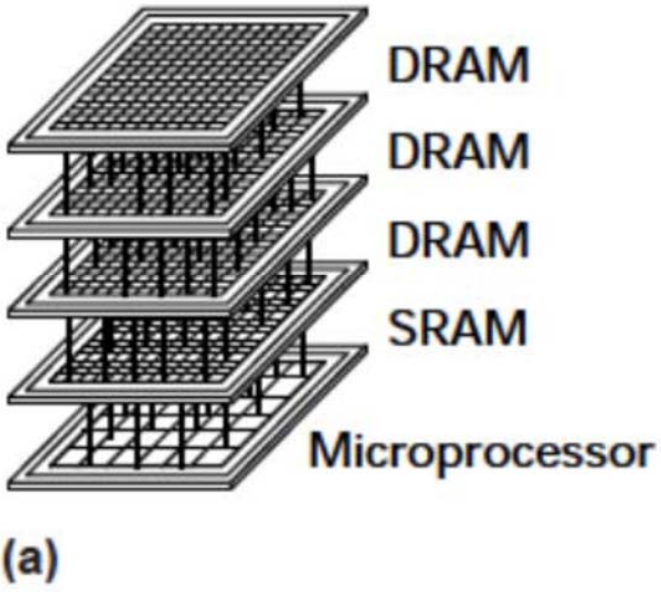
To the extent that the Board finds it necessary to mention contacts in the context of the claimed "memory array," Patent Owner suggests that the Board use the term "a number of vertical contacts distributed throughout the surface of and traversing the memory die." The Board's construction is also inconsistent with the

claims as the Claim 1 recites "a second integrated circuit functional element" has "a number of contact points distributed throughout the surfaces of said functional element." *See* '951 Patent, Claim 1 & Claim 15. Further, the Board's preliminary construction only adds ambiguity to the meaning of this term because it requires "a number of vertical contacts that…provide contacts on the surface of the memory die." Institution Decision at 24; *see also* Chakrabarty Decl., ¶39. Accordingly, the Board should adopt Patent Owner's construction of "a memory array functional to accelerate external memory references to the processing element" means "a memory array that allows the parallel loading of data through buffer cells."

V. OVERVIEW OF THE PRIOR ART

A. Summary of Koyanagi

Koyanagi (Ex. 1007) is an IEEE publication titled "Future System-On-Silicon LSI Chips." *Koyanagi* teaches vertically stacking several chip layers in a 3D large-scale integration (LSI) chips or 3D multichip modules (MCMs). *Koyanagi* at 17. Specifically, *Koyanagi* discloses a multichip module with several memory chips, including dynamic random-access memory ("DRAM") and static random-access memory (SRAM), as shown below:



Koyanagi at FIG. 1(a); *see also* Chakrabarty Decl., ¶44.

Koyanagi teaches using vertical interconnections to connect the different layers of the MCM. *Koyanagi*, pp. 17-18, FIG. 1(a)). *Koyanagi* teaches using vertical interconnections to connect the different layers of the MCM. *Id.* However, unlike the '951 Patent, *Koyanagi* does not teach or suggest incorporating a novel buffer cell configuration into a memory die for the purpose of accelerating data transfer to a reconfigurable processor. *See* Chakrabarty Decl., ¶45.

B. Summary of Alexander

Alexander (Ex. 1006) is an article entitled "Three-Dimensional Field-Programmable Arrays." *Alexander* at 1. *Alexander* proposed, but did not (and could not) fabricate, a 3D field-programmable gate array (FPGA). *Id*. The authors

modified a 2D FPGA model to propose a new design in which each logic element had six immediate neighbors instead of the usual four:

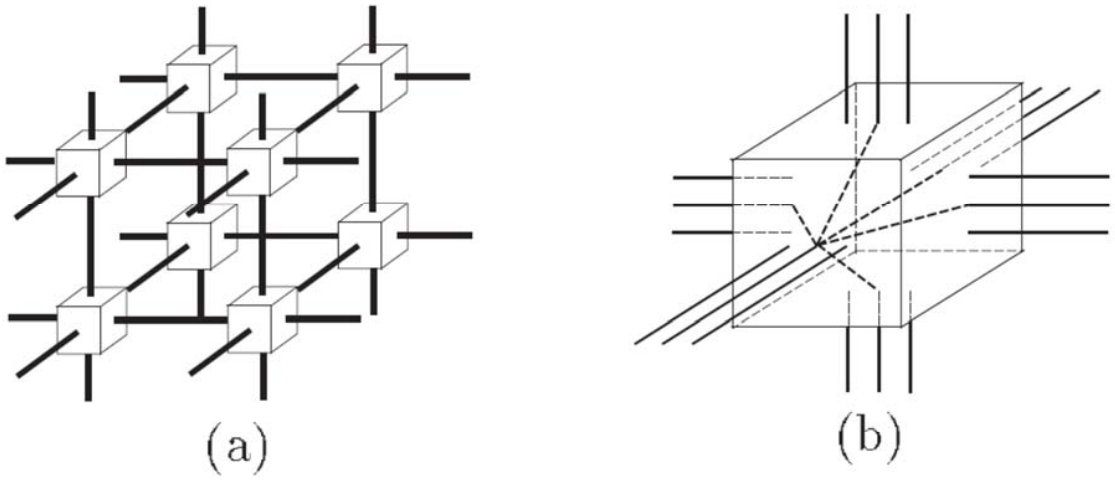


Figure 1: (a) 3D FPGA, and (b) 3D switch block.

Id. *Alexander's* 3D FPGA, however, does not include a memory, much less a memory array that includes the novel buffer cell configuration of the '951 Patent, and does not provide a motivation to stack its 3D FPGA with a memory or any other type of IC. Accordingly, *Alexander* does not disclose "a memory array functional to accelerate external memory references to the processing element. '951 Patent, Claim 1; *see also* Chakrabarty Decl., ¶46.

C. Summary of Bertin

Bertin (Ex. 1009) is directed to a semiconductor package that has through-chip conductors for low inductance chip-to-chip-integration and off-chip

connections. *Bertin* at Abstract. Figure 22 of *Bertin* teaches stacking similar chips while providing chip-to-chip connections through silicon. *Id.* at 7:16-18. As shown below, *Bertin* teaches that a stack of chips 142, 144, 146, and 148 can be mounted to a device 140, such as an logic chip, microprocessor, controller to minimize latency between the device and chips to and to maximize bandwidth. *Id.* at 7:18-22.

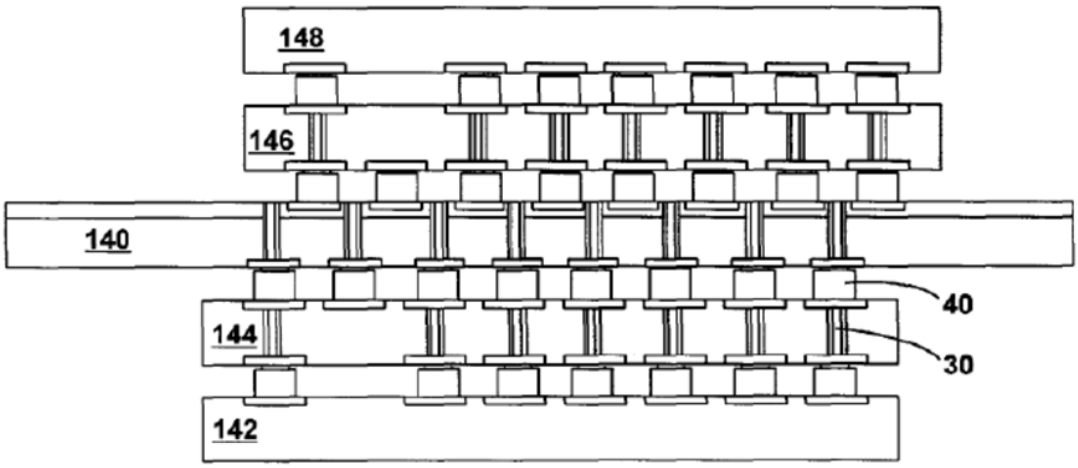


FIG. 22

Bertin at FIG. 22; *see also* Chakrabarty Decl., ¶47.

Unlike the '951 Patent which teaches that a memory array that includes a novel buffer cell configuration to accelerate external memory references to the processing element, *Bertin* teaches three or four chip-to-chip connections are sufficient to connect one chip to another chip without the use of buffer cells. *See*

Bertin at 7:16-34 ("The first four connections connects the device 140 to each chip" and "[t]hese last four connections allow for parallel input/output connections."). *Bertin* does not teach a memory array functional to accelerate external memory references to the processing element. *See* Chakrabarty Decl., ¶48.

D. Summary of Cooke

Cooke (Ex. 1008) is directed to a reconfigurable processor chip. *Cooke*, Abstract. Specifically, *Cooke* discloses a single die element comprising a microprocessor and three FPGA regions. *Cooke* at Abstract; *id.* at FIG. 2; *id.* at 2:45-48. *Cooke* teaches that these "blocks" enable software tools to recompile application code into a combination of software and reloadable hardware blocks, which provide a customer the flexibility of software development and the performance of dedicated hardware solutions.[1] *Id.* at 2:3-11. *Cooke*, however, does not teach or suggest a memory array that accelerates memory references to a reconfigurable processor using buffer cells. *See* Chakrabarty Decl., ¶49. Nor does

[1] While Figures 2 and 8 of Cooke depict these "blocks" as stacks, such a memory stacks, a POSITA would understand that Cooke's blocks are conceptual and Cooke does not teach or suggest physically stacking chips that include processing elements in a 3D integrated circuit. *See* Chakrabarty Decl., ¶ 49, n.1.

Cooke disclose or suggest a microprocessor stacked with a programmable array, as required in Claim 10 of the '951 Patent. *See id*.

VI. THE CHALLENGED CLAIMS ARE PATENTABLE

A. Ground 1: Claims 1, 4-5, 8, 10, and 13-15 Are Patentable Over *Koyanagi* and *Alexander*

1. Petitioner fails to demonstrate that *Koyanagi* in view of *Alexander* teaches or suggests "a memory array functional to accelerate external memory references to the processing element [/ said programmable array]" (Claims 1, 5, and 10).

As discussed *supra* in Section IV.A, the phrase "a memory array functional to accelerate external memory references to the processing element" means "a memory array that allows the parallel loading of data through buffer cells."

Petitioner's proposed combination of *Koyanagi* with *Alexander* does not satisfy this limitation as the combination does not teach or suggest a memory array that uses buffer cells to accelerate memory references to a processing element. *See* Chakrabarty Decl., ¶¶50-51. As Dr. Chakrabarty explains, a POSITA reading the Specification of the '951 Patent would understand that the buffer cells disclosed in Figure 5 are responsible in part for the claimed acceleration of memory references to the programmable array. *See id.*, ¶52

Figure 5 the '951 Patent describes how to interconnect a programmable array (such as an FPGA) into a 3D integrated circuit, such that the memory array can accelerate memory references to the processing element. *See* Chakrabarty

Decl., ¶52. Specifically, the '951 Patent explains how electrical connections, such as TSVs, are used to load configuration data in a parallel fashion to buffer cells while the programmable array is in operation. '951 Patent at 5:29-43. Then, once the programmable array ceases operation, the configuration data can be loaded, in parallel fashion, into configuration memory resulting in an acceleration of the memory references being delivered to the programmable array compared to prior systems. *Id.* This process is achieved using the wide configuration data port and its associated buffer cells 88 (indicated in blue), as shown below:

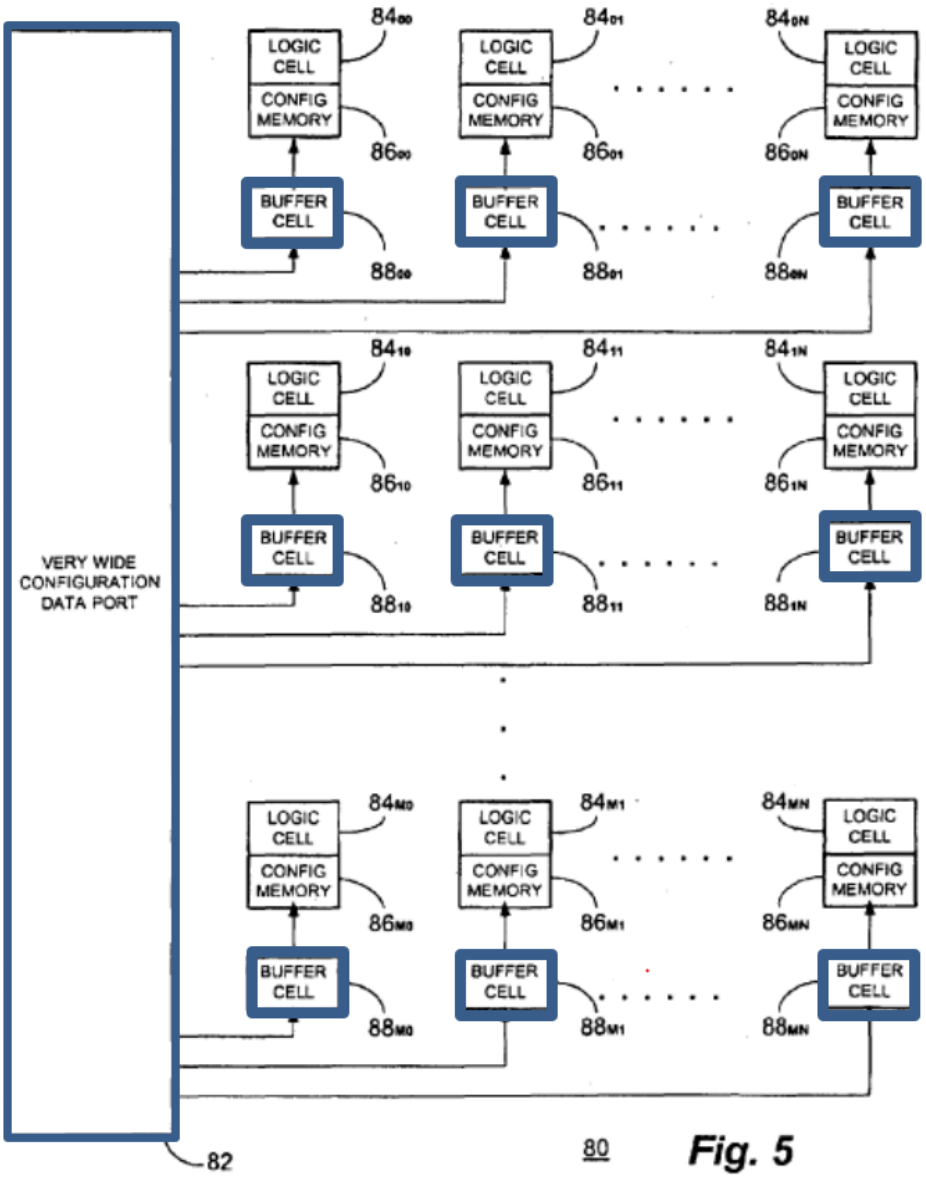


Fig. 5

'951 Patent at FIG. 5 (annotated); *see also* Chakrabarty Decl., ¶52.

Petitioner fails to even assert that *Koyanagi* or *Alexander* teach or suggest the buffer cells that are necessary for the memory array to accelerate memory references to the processing element. *See* Chakrabarty Decl., ¶53. While, Petitioner argues that "Koyanagi in view of Alexander renders the claimed

acceleration obvious because this prior art combination discloses the same way to accelerate external memory references as is described in the '951 Patent specification" (Petition at 28), Petitioner's superficial analysis fails to even allege that its proposed combination teaches '951 Patent's disclosed method of accelerating memory references, and specifically fails to teach or suggests the use of buffer cells, as disclosed in the '951 Patent. *See* Chakrabarty Decl., ¶53.

Accordingly, neither *Cooke* nor *Koyanagi* teach or suggest a memory array functional to accelerate external memory references to the processing element. *See id.*, ¶54.

2. A POSITA Would Not Have Been Motivated to Combine *Koyanagi* with *Alexander.*

Petitioner fails to demonstrate that it would have been obvious to modify *Koyanagi* with *Alexander* to yield the claimed invention. Indeed, not only has Petitioner failed to demonstrate that the combination of *Koyanagi* and *Alexander* reach the claimed invention, it also has failed to demonstrate that this combination would have been obvious to try with reasonable expectation of success.

A party who petitions the Board for a determination of obviousness must show that "a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention, and that the skilled artisan would have had a reasonable expectation of success in doing so." *Procter & Gamble Co. v. Teva Pharm. USA, Inc.*, 566 F.3d 989, 994 (Fed. Cir. 2009)

(quoting *Pfizer, Inc. v. Apotex, Inc.*, 480 F.3d 1348, 1361 (Fed. Cir. 2007)). This showing requires "more than a mere showing that the prior art includes separate references covering each separate limitation in a claim." *Unigene Labs., Inc. v. Apotex, Inc.*, 655 F.3d 1352, 1360 (Fed. Cir. 2011) (citation omitted). Rather, it requires the additional showing that "a person of ordinary skilled at the time of the invention would have selected and combined those prior art elements in the normal course of research and development to yield the claimed invention." *Id.* (citations omitted). Petitioner fails to make this showing.

(a) Petitioner fails to demonstrate that a POSITA would know how to combine Koyanagi's 3D multichip module with Alexander's FPGAs to achieve the claimed invention without relying on hindsight bias.

A POSITA would not have been motivated to combine *Koyanagi* with *Alexander* because neither *Koyanagi* nor *Alexander* disclose how to combine a programmable array, a microprocessor, and a memory die into a 3D IC, which would take undue experimentation to perform without using the '951 Patent as a roadmap. *See* Chakrabarty Decl., ¶55. In particular, Petitioner alleges that "a POSITA would have understood that *Koyanagi* discloses stacking dies in a universal 3D-integration scheme that is agnostic to the type and functionality of the stacked dies." Petition at 18. Alleging that *Koyanagi's* 3D-integration scheme is "agnostic," Petitioner concludes that "[s]tacking an FPGA die over memory and

microprocessor dies would have been obvious to try with a reasonable expectation of success." *Id.* at 20; *see also* Chakrabarty Decl., ¶56

Petitioner's argument is a vast oversimplification of the complicated technology at issue. A POSITA would understand that figuring out ***how*** to combine an FPGA, microprocessor, and memory into a 3D integrated circuit that accelerates memory references to the FPGA would require undue experimentation. *See* Chakrabarty Decl., ¶57. An obviousness determination cannot be reached where there is no explanation as to how or why the references would be combined, because without any explanation there is only the impermissible hindsight reconstruction, using the patent as a guide through the maze of prior art references so as to combine the right references to achieve the claimed invention. *See Metalcraft of Mayville, Inc. v. The Toro Co.*, 848 F.3d 1358, 1367 (Fed. Cir. 2017) ("Without any explanation as to how or why the references would be combined to arrive at the claimed invention, we are left with only hindsight bias that *KSR* warns against." (citing *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 419 (2007)); *see also Grain Processing Corp. v. Am. Maize-Prods. Co.*, 840 F.2d 902, 907 (Fed. Cir. 1988).

When Petitioner's expert was asked about combining different types of chips using TSVs into a 3D IC, Dr. Shanfield acknowledged such a combination cannot be casually thrown together:

> You have obviously got to have a circuit in mind that you're wanting to create a system-level circuit, a module-level circuit; and so you're going to need to consider which connections you want a TSV connecting to something below. ***So you don't just slap it together without worrying about what connects to what***.

Ex. 2014, Shanfield Tr. at 81:21-82:19 (emphasis added); *see also* Chakrabarty Decl., ¶57.

But Petitioner does just that—slaps *Koyanagi* and *Alexander* together without worrying about what connects to what. In fact, neither Petitioner, Dr. Shanfield, *Koyanagi*, nor *Alexander* explain how a POSITA would combine *Koyanagi* with *Alexander* to arrive at the claimed "3D integrated circuit." *See* Chakrabarty Decl., ¶58. Indeed, *Alexander* amplifies the complexity of stacking an FPGA, microprocessor, and memory dies because *Alexander* only teaches a single 3D FPGA, which would still have to be stacked and integrated with a memory and microprocessor. *Alexander* at 1 ("Our proposed 3D FPGA architecture is a generalization of the basic 2D model, where each logic block has six immediate neighbors (Figure 1(a))" and "[o]ne method to build a 3D FPGA entails stacking together a number of 2D FPGA bare dies . . . ."). Without an explanation, the Board is left with only hindsight bias from the Petitioner that *KSR* warns against.

The Federal Circuit in *In re Schweickert*, 676 F. App'x 988 (2017), was faced with similar facts as presented here, and found that the "Board ha[d] not explained why or how a skilled artisan would [] configure or manipulate Birrell's RAM such that there would be multiple lockable buffers as claimed in the '272 Patent." *Id.* at 995. The Federal Circuit noted that it is "important to identify a *reason* that would have prompted [a skilled artisan] to combine the elements *in the way* the claimed new invention does." *Id.* (emphasis in original) (citation omitted). Specifically, the Federal Circuit articulated that the asserted reference failed to provide any indication that the buffers in its figures are individually lockable as required by the claimed invention. *Id.* Therefore, the Federal Circuit held that the Board's "broadly-stated conclusion suffers from hindsight bias." *Id.* at 996 (citations omitted).

Likewise, Petitioner's overly simplistic obviousness argument, which trivializes how to accelerate memory references to an FPGA in a 3D IC using TSVs, suffers from hindsight bias. *See* Chakrabarty Decl., ¶59. Petitioner simply suggests—without any explanation as to how the references would be combined—that *Koyanagi's* vertical interconnection scheme would somehow accelerate data to an FPGA if the *Alexander's* 3D FPGA was stacked on *Koyanagi*'s 3D IC. Petitioner's flawed logic is grounded upon the impermissible use of the '951 Patent as a roadmap. More particularly, Petitioner uses the '951 Patent to glean

advantages from its key improvement over the art—a memory array that accelerates external memory references to the processing element (*see* '951 Patent at 1:53-58; *id*. at 5:29-35)—to disingenuously contend that a POSITA would have been motivated to use 3D vertical interconnections with FPGAs in an effort to yield the claimed invention. *See, e.g.*, *In re NTP, Inc.*, 654 F.3d 1279, 1298-99 (Fed. Cir. 2011). Petitioner's argument is notably deficient for its complete lack of explanation as to ***how*** a POSITA would configure or manipulate *Koyanagi* with *Alexander* in the specific way the '951 Patent's claimed invention does. *See* Chakrabarty Decl., ¶59. The reasons for this flaw is that it is based on impermissible hindsight analysis.

As Dr. Chakrabarty explains, Figure 5 the '951 Patent describes how to interconnect a programmable array (such as an FPGA) into a 3D integrated circuit, a process for interconnecting the components of the integrated circuit not taught by either *Koyanagi* or *Alexander*, and that would take undue experimentation beyond the disclosure of either reference. *See* Chakrabarty Decl., ¶60. For example, the '951 Patent explains how electrical connections, such as TSVs, are used to load configuration data in a parallel fashion to buffer cells while the programmable array is in operation. '951 Patent at 5:29-43. Then, the configuration data can be loaded, in parallel, into configuration memory resulting in the programmable array.

Id. This process is achieved using the wide configuration data port, and its associated buffer cells 88, as shown below:

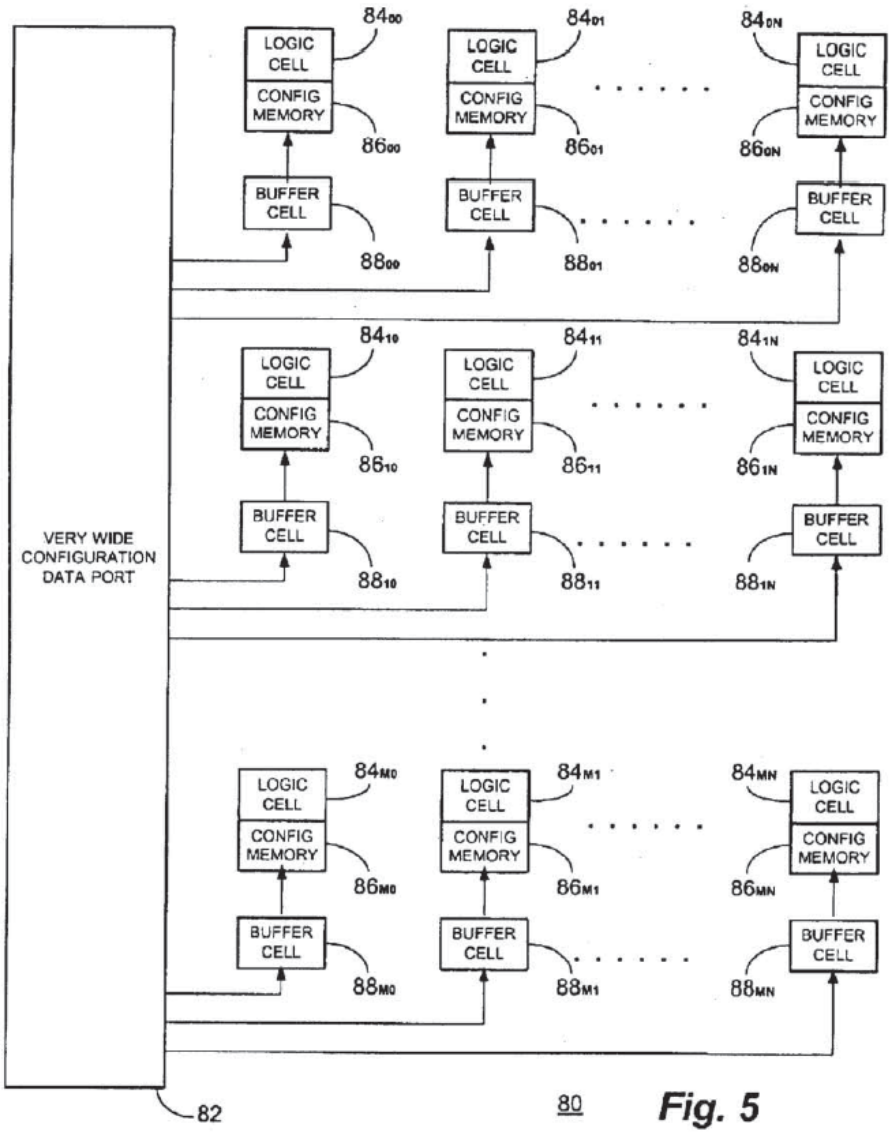


Fig. 5

'951 Patent at FIG. 5; *see also* Chakrabarty Decl., ¶60.

Petitioner overlooks that the '951 Patent describes a wide configuration data port that through ***buffer cells*** allows the parallel updating of logic cells in the

FPGA. '951 Patent at 5:29-43; *id.*, FIG. 5. In other words, the '951 Patent describes that the configuration of the ***buffer cells*** in the memory array that accelerate the speed at which data travels to the programmable array. *Id.* at 5:29-43. Indeed, the '951 Patent greatly improved upon FPGA reconfiguration time, which conventionally took "millions of processor clock cycles to complete the reconfiguration." *Id.* at 1:52-57. This improvement was the basis for the '951 Patent, and, further confirms the challenges that the inventors of the '951 Patent faced when innovating in this space, and illustrates that Petitioner trivializes these challenges to make its fallacious obviousness argument. *See* Chakrabarty Decl., ¶61.

Accordingly, Petitioner fails to demonstrate that a POSITA would have been motivated to combine these two references to meet the claimed invention, as the combination Petitioner proposes would result in such significant technical challenges that a POSITA would not be motivated to attempt this combination in an effort to achieve the claimed invention. *See id.*, ¶62. For at least these reasons, Ground 1 fails.

(b) Petitioner overlooks the thermal issues that plagued 3D stacked FPGA chips and which fatally undermine Petitioner's obvious to try theory as it would not result in a reasonable expectation of success.

Petitioner argues that a POSITA would have found it obvious to try stacking *Alexander's* FPGA on *Koyanagi's* memory chip layers and would have expected a

reasonable expectation of success. Petition at 20-21. This assertion is also meritless. Petitioner's overly simplistic obvious to try theory runs afoul of *KSR* because stacking FPGAs on a 3D multichip module is ***not*** one of "familiar elements according to known methods . . . [which] do[] no more than yield predictable results." *KSR*, 550 U.S. at 416. Rather, the exact opposite is the case. *See* Chakrabarty Decl., ¶63.

Petitioner fails to recognize the known thermal challenges that plagued 3D FPGA development and design. *See id*., ¶64. In fact, none of Petitioner's asserted references disclose stacking an FPGA with a microprocessor to form a SDH module, let alone a SDH module with die-area connections. *Alexander* proposed stacking several portions of a 2D FPGA to form a single 3D FPGA. *See id*. However, *Alexander* does not disclose stacking an FPGA with any other type of IC die (*i.e.* to form a hybrid stacked chip). Moreover, while *Alexander* proposed a 3D FPGA, the authors admitted that it could not fabricate its proposed design. *See, e.g.*, *Alexander* at 4 ("The proposed 3D architecture seems promising . . . [but] [a] number of important issues remain to be addressed for this 3D architecture paradigm."). Importantly, *Alexander* acknowledges that "[t]he 3D FPGA model gives rise to a number of new challenges" including heat dissipation and heat stress (collectively, "thermal issues"). *Id.* at 3-4. The thermal issues are due to FPGAs'

increase in power consumption that cause higher operating temperatures that can lead to a less reliable operation. *Id.* at 3; *see also* Chakrabarty Decl., ¶64.

As such, *Alexander* recognized that the industry must find ways of "reducing power consumption in 3D FPGA architectures" in order to mitigate the thermal issues. *Alexander* at 4. But until further investigation is performed, and resolution found, thermal issues will remain a major concern. *Id.* In fact, *Alexander's* concern of these thermal issues is shared throughout the industry, as persons of ordinary skill in the art recognize, even within the last decade, that while 3D FPGA "is one of the promising innovations . . . thermal issues are . . . a critical concern in 3D integration which results in degradation of device performance." Ex. 2016, Abstract; *see also* Ex. 2011, Abstract; Chakrabarty Decl., ¶65.

In the Institution Decision, the Board concluded that Petitioner's statements relate to "'how and why' an artisan of ordinary skill would have combined the stack die features of Koyanagi with the similar features of Alexander." Institution Decision at 34. This is incorrect. *See* Chakrabarty Decl., ¶66. Petitioner fails to provide sufficient evidence that a POSITA would have found *Koyanagi* agnostic to the types of dies stacked, despite the known thermal issues that deter 3D stacking of FPGAs. In other words, Petitioner fails to demonstrate not only why a POSITA would have ignored these known thermal issues, but also how the POSITA would modify *Koyanagi's* 3D multichip module with *Alexander's* FPGAs considering the

well-established 3D FPGA thermal issues. *See id.; see, e.g.*, *Metalcraft of Mayville*, 848 F.3d at 1367 ("Without any explanation as to how or why the references would be combined to arrive at the claimed invention, we are left with only hindsight bias that *KSR* warns against." (citing *KSR*, 550 U.S. at 419)).

In fact, Petitioner ignores all together the known 3D FPGA thermal issues recognized by *Alexander*. And *Koyanagi* does not offer a solution to these 3D thermal issues. In fact, *Koyanagi* admits that "[c]omplicated design features related to 3D interconnections are another concern in LSIs." *Koyanagi* at 17; *see also* Chakrabarty Decl., ¶67.

While *Koyanagi* does address a solution to heat dissipation, the solution is for the 3D stacking of Dynamic Random-Access Memory ("DRAM") chips on a microprocessor, not for 3D stacking of FPGAs. *See, e.g.*, *Koyanagi* at 17-18, FIGS. 1-2 (illustrating stacking of DRAMs on a microprocessor). As known by skilled artisans at that time, the 3D stacking of FPGA as opposed to DRAM was not trivial, as FPGA consume significantly more power than DRAM, which leads to heat dissipation problems. Chakrabarty Decl., ¶68. It was well established at the time that the power consumption needs of FPGAs, as well as other logic dies, as opposed to memory, were far greater as they are driven by dynamic power that is based upon the specific use of each resource and is a function of the signals toggling and capacitive loads charging and discharging. Ex. 2012 at 1; *see also*

Ex. 2013 at 4; Chakrabarty Decl., ¶68. In fact, the use of I/O pins impact the total power requirements since "considerations like I/O standards used and data rates expected determine how fast the I/Os toggle and how fast the logic must be clocked." Ex. 2012 at 1; Chakrabarty Decl., ¶68. Petitioner's own reference, *Alexander*, notes that a large portion of the power consumption is due to driving I/O buffers. *Alexander* at 4. That is, FPGAs, and other logic dies, perform computational operations that result in extensive switching activities that consume a significant amount of dynamic power. *See* Chakrabarty Decl., ¶68

By contrast, memory does not perform computational operations, rather just read and write operations, which consume very little dynamic power. *See* Chakrabarty Decl., ¶69. As such, FPGAs consume substantially more dynamic power than DRAM resulting in significantly higher temperatures and correspondingly heat dissipation problems. *See id*. Because of the power consumption by FPGAs, and other logic dies, and the resulting thermal issues, a POSITA would not have found it obvious to stack a programmable array, such as an FPGA, with other die, let alone a microprocessor. Simply put, a skilled artisan would not have ignored the well-established thermal issues that plagued the proposed 3D stacking of FPGAs. *Id*.

The Supreme Court's decision in *United States v. Adams*, 383 U.S. 39 (1966) is on point to the facts here. In *Adams*, the Supreme Court concluded that

patentee's battery—which included the combination of magnesium and cuprous chloride—was nonobvious, despite the fact that each element was well-known in the art, because "to combine them as did [patentee] ***required that a person reasonably skilled in the art must ignore that*** (1) batteries which continued to operate on an open circuit and which heated in normal use were not practical; and (2) water-activated batteries were successful only when combined with electrolytes detrimental to the use of magnesium." 383 U.S. at 51-52 (emphasis added). The *Adams* Court determined that these long accepted factors "***would . . . deter any investigation into such combination as is used by [patentee]***." *Id*. (emphasis added).

Applying the *Adam* Court's governing principles here, the long accepted thermal issues that plagued 3D FPGA development and design would have deterred investigation by POSITA into such combination as used by Patent Owner. That is, a POSITA would ***not*** have found the '951 Patent's claimed invention—stacking a thinned microprocessor die element, a memory die element, and a FPGA (*see* §II, *supra*)—obvious to try with a reasonable expectation of success because of the known thermal issues, which a POSITA would ***not*** have ignored.

Additionally, as explained above, and, here again, *Alexander* teaches that the serious thermal issues its proposed 3D FPGA configuration suffers from can lead to less reliable operation. *Alexander* at 3-4. This is because the power

consumption by logic dies, such as FPGAs and microprocessors, increase the operating temperatures. *Id.* As a result, a POSITA would understand that Petitioner's alleged combination of *Koyanagi's* 3D integration of memory chip layers with *Alexander's* FPGA would only exacerbate the high operating temperatures caused by logic dies and would render the combined device inoperable. *See* Chakrabarty Decl., ¶71.

Thus, Petitioner's contention that it would be obvious to try stacking *Alexander's* FPGAs on *Koyanagi's* 3D multichip module crumbles under the weight of contradictory evidence. *See id*., ¶70. For at least these reasons, Ground 1 fails.

B. Ground 2: Claims 1, 4-5, 8, 10, and 13-15 Are Patentable Over *Bertin* and *Cooke*

1. Petitioner Fails to Demonstrate that *Bertin* in View of *Cooke* teaches or suggests "a memory array functional to accelerate external memory references to the processing element [/ said programmable array]" (Claims 1, 5, and 10).

As discussed *supra* in Section IV.A , the phrase "a memory array functional to accelerate external memory references to the processing element" means "a memory array that allows the parallel loading of data through buffer cells." *See* Chakrabarty Decl., ¶73.

Petitioner's proposed combination of *Bertin* with *Cooke* does not satisfy this limitation as the combination does not teach or suggest a memory array that uses

buffer cells to accelerate memory references to a processing element. As Dr. Chakrabarty explains, a POSITA reading the Specification of the '951 Patent would understand that the buffer cells disclosed in Figure 5 are responsible in part for the claimed acceleration of memory references to the programmable array. *See id.*, ¶74

Figure 5 the '951 Patent describes how to interconnect a programmable array (such as an FPGA) into a 3D integrated circuit, such that the memory array can accelerate memory references to the processing element. *See id.*, ¶75. Specifically, the '951 Patent explains how electrical connections, such as TSVs, are used to load configuration data in a parallel fashion to buffer cells while the programmable array is in operation. '951 Patent at 5:29-43. Then, once the programmable array ceases operation, the configuration data can be loaded, in parallel fashion, into configuration memory resulting in an acceleration of the memory references being delivered to the programmable array compared to prior systems. *Id.* This process is achieved using the wide configuration data port and its associated buffer cells 88 (indicated in blue), as shown below:

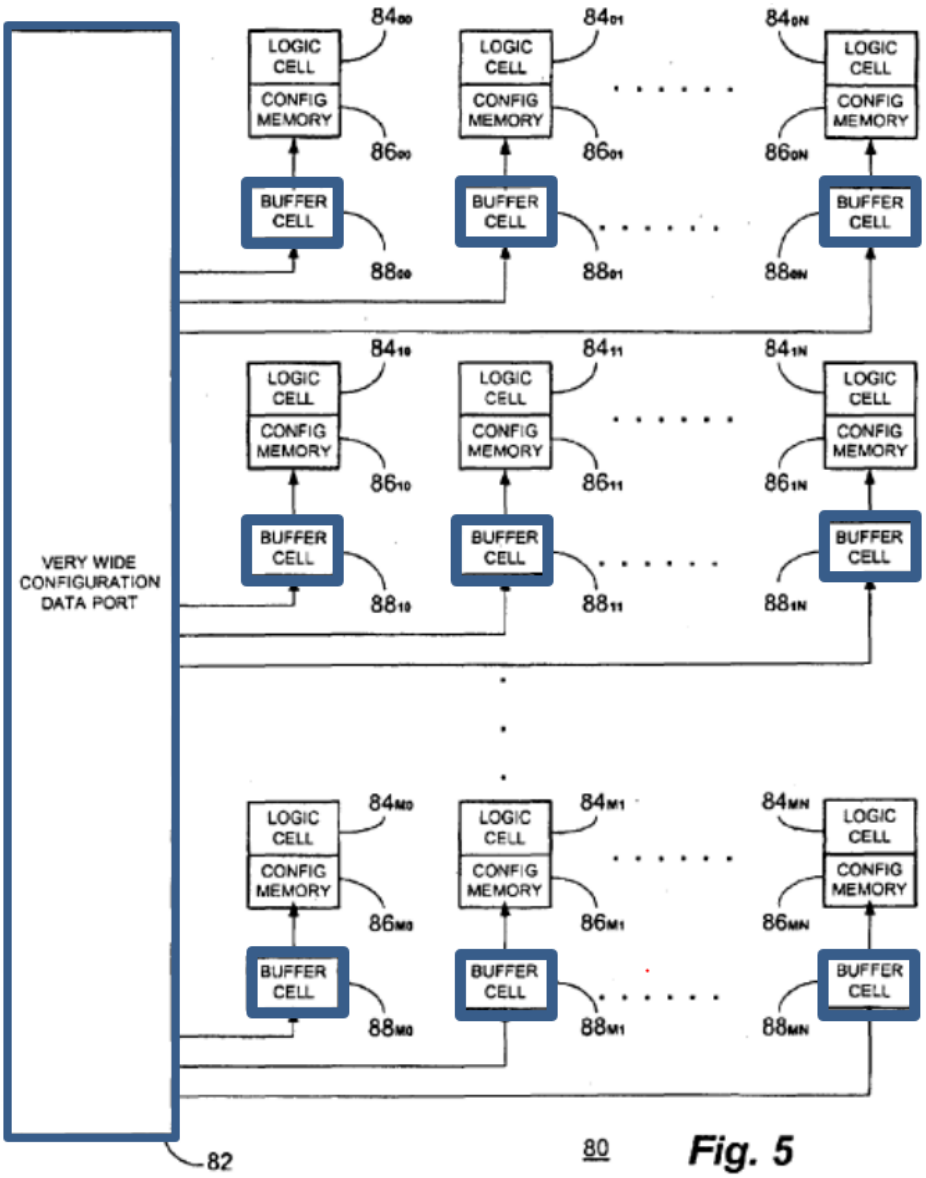


Fig. 5

'951 Patent at FIG. 5 (annotated); *see also* Chakrabarty Decl., ¶75.

Petitioner fails to even assert that *Bertin* or *Cooke* teach or suggest the buffer cells that are necessary for the memory array to accelerate memory references to the processing element. While Petitioner argues that "Bertin in view of Cooke renders the claimed acceleration obvious because this prior art combination

discloses the same way to accelerate external memory references as is described in the '951 Patent specification," Petitioner's superficial analysis fails to even allege that its proposed combination teaches the ''951 Patent's disclosed method of accelerating memory references, and specifically fails to teach or suggests the use of buffer cells, as disclosed in the '951 Patent. Petition at 56; *see also* Chakrabarty Decl., ¶76.

Accordingly, neither *Bertin* nor *Cooke* teach or suggest a memory array functional to accelerate external memory references to the processing element. *See* Chakrabarty Decl., ¶77.

2. Petitioner Fails to Show That a POSITA Would Have Been Motivated to Combine *Bertin* and *Cooke*.

For similar reasons as described *supra* in Section VI.A.2, Petitioner fails to demonstrate that it would have been obvious to modify *Bertin* with *Cooke* to yield the claimed invention. Indeed, not only has Petitioner failed to demonstrate that the combination of *Bertin* and *Cooke* reach the claimed invention, it also has failed to demonstrate that this combination would have been obvious to try with reasonable expectation of success. A party who petitions the Board for a determination of obviousness must show that "a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention, and that the skilled artisan would have had a reasonable expectation of success in doing so." *Procter & Gamble*, 566 F.3d at 994 (quoting

Pfizer, 480 F.3d at 1361). This showing requires "more than a mere showing that the prior art includes separate references covering each separate limitation in a claim." *Unigene*, 655 F.3d at 1360 (citation omitted). Rather, it requires the additional showing that "a person of ordinary skilled at the time of the invention would have selected and combined those prior art elements in the normal course of research and development to yield the claimed invention." *Id.* (citations omitted). Petitioner fails to make this showing.

(a) Petitioner fails to demonstrate that a POSITA would have known how to combine Bertin's 3D integration with Cooke's FPGAs to achieve the claimed invention without relying on hindsight bias.

A POSITA would not have been motivated to combine *Bertin* with *Cooke* because neither *Bertin* nor *Cooke* disclose how to combine a programmable array, a microprocessor, and a memory die into a 3D IC, which would take undue experimentation to perform without using the '951 Patent as a roadmap. *See* Chakrabarty Decl., ¶78. Petitioner alleges that "Bertin discloses a ***universal*** 3D integration scheme whereby different types of chips…can be vertically stacked and interconnected using through-chip conductors (TSVs) and chip-to-chip connectors." Petition at 47. By alleging that *Bertin's* scheme is "universal," Petitioner concludes that "a POSITA would have been motivated to vertically stack the functional components of the FPGA-based reconfigurable computer system described in *Cooke* according to *Bertin's* 3D integration teachings—which is

designed to universally 'accommodate different chip sizes and structures.'" *Id.* at 48.

Petitioner's argument is a vast oversimplification of the complicated technology at issue. A POSITA would understand that figuring out ***how*** to combine an FPGA, memory, and microprocessor into a 3D integrated circuit would require undue experimentation. *See* Chakrabarty Decl., ¶78. An obviousness determination cannot be reached where there is no explanation as to how or why the references would be combined, because without any explanation there is only the impermissible hindsight reconstruction, using the patent as a guide through the maze of prior art references so as to combine the right references to achieve the claimed invention. *See Metalcraft of Mayville*, 848 F.3d at 1367 ("Without any explanation as to how or why the references would be combined to arrive at the claimed invention, we are left with only hindsight bias that *KSR* warns against." (citing *KSR*, 550 U.S. at 419)); *see also Grain Processing*, 840 F.2d at 907.

When Petitioner's expert was asked about combining different types of chips using TSVs into a 3D IC, Dr. Shanfield, testified that:

> You have obviously got to have a circuit in mind that you're wanting to create a system-level circuit, a module-level circuit; and so you're going to need to consider which connections you want a TSV connecting to

> something below. ***So you don't just slap it together without worrying about what connects to what***.

Ex. 2014, Shanfield Tr. at 81:21-82:19 (emphasis added); *see also* Chakrabarty Decl., ¶79.

Here again, Petitioner does just that—slaps *Bertin* and *Cooke* together without worrying about what connects to what. In fact, neither Petitioner, Dr. Shanfield, *Bertin*, nor *Cooke* explain how a POSITA would combine *Bertin* with *Cooke* to arrive at a 3D integrated circuit integrating a programmable array, a memory, and microprocessor. *See* Chakrabarty Decl., ¶80. Without any explanation by Petitioner, the Board is left with only hindsight bias that *KSR* warns against.

As explained previously, the Federal Circuit in *In re Schweickert* was faced with similar facts as presented here, and found that the "Board ha[d] not explained how or why a skilled artisan would [] configure or manipulate Birrell's RAM such that there would be multiple lockable buffers as claimed in the '272 Patent." 676 F. App'x at 995. The Federal Circuit noted that it is "important to identify a *reason* that would have prompted [a skilled artisan] to combine the elements *in the way* the claimed new invention does." *Id.* (emphasis in original) (citation omitted). Specifically, the Federal Circuit articulated that the asserted reference failed to provide any indication that the buffers in its figures are individually lockable as

required by the claimed invention. *Id.* Thus, the Federal Circuit held that the Board's "broadly-stated conclusion suffers from hindsight bias." *Id.* at 996 (citations omitted).

Similar to its approach with *Koyanagi* and *Alexander*, Petitioner's overly simplistic obviousness argument, which trivializes how achieving instantaneous reconfiguration of a FPGA can be solved in a 3D IC using TSVs, suffers from hindsight bias. *See* Chakrabarty Decl., ¶81. Petitioner simply suggests—without any explanation as to how—that *Bertin's* through chip connectors would somehow achieve *Cooke's* aspirational goal of instantaneous reconfiguration of FPGAs in a processor chip. Petitioner's flawed logic is grounded upon the impermissible use of the '951 Patent as a roadmap. More particularly, Petitioner uses the '951 Patent to glean advantages from its instrumental improvement over the art—reconfiguration of FPGA in one clock cycle as opposed to the millions of clock cycles it took in the conventional art (*see* '951 Patent at 1:53-58; *id*. at 5:29-34) — to disingenuously contend that a POSITA would have been motivated to use 3D vertical interconnections with FPGAs in an effort to yield the claimed invention. *See, e.g.*, *In re NTP*, 654 F.3d at 1299. Petitioner's argument is notably deficient for its complete lack of explanation as to ***how*** a POSITA would configure or manipulate *Bertin* with *Cooke* in the specific way the '951 Patent's claimed

invention does. *See* Chakrabarty Decl., ¶81. The reason for this flaw is the impermissible hindsight analysis.

As Dr. Chakrabarty explains, Figure 5 the '951 Patent describes how to interconnect a programmable array (such as an FPGA) into a 3D integrated circuit, a process for interconnecting the components of the integrated circuit not taught by either *Bertin* or *Cooke*, and that would take undue experimentation beyond the disclosure of either reference. *See* Chakrabarty Decl., ¶82. For example, the '951 Patent explains how electrical connections, such as TSVs, are used to load configuration data in a parallel fashion to buffer cells while the programmable array is in operation. '951 Patent at 5:29-43. Then, the configuration data can be loaded, in parallel, into configuration memory resulting in the programmable array being reconfigured. *Id.* This process is achieved using the wide configuration data port, and its associated buffer cells 88, as shown below:

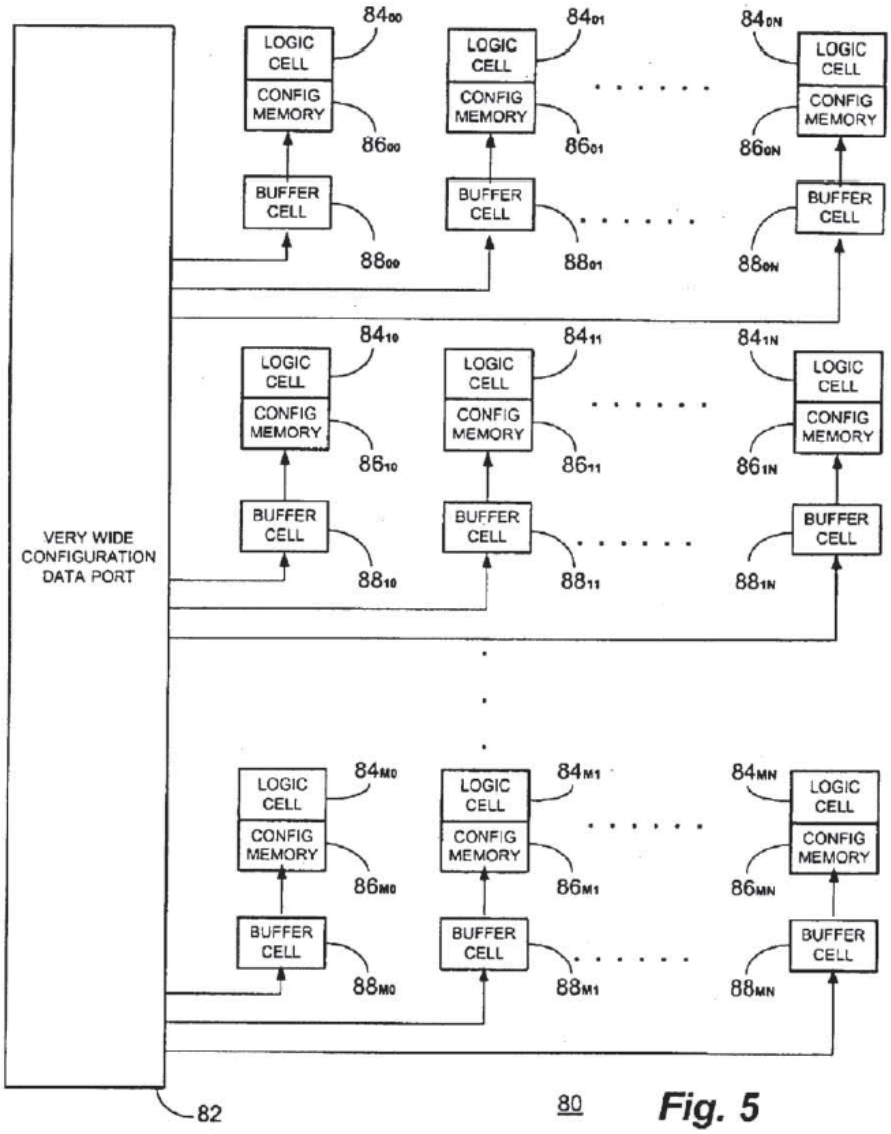


Fig. 5

'951 Patent at FIG. 5; *see also* Chakrabarty Decl., ¶82.

Petitioner overlooks that the '951 Patent describes a wide configuration data port that through ***buffer cells*** allows the parallel updating of logic cells in the FPGA. '951 Patent at 5:29-43; *id.* at FIG. 5. In other words, the '951 Patent describes that the configuration of the ***buffer cells*** in in the memory array that accelerate the speed at which data travels to the programmable array. *Id.* at 5:29-

43. Indeed, the '951 Patent greatly improved upon FPGA reconfiguration time, which conventionally took "millions of processor clock cycles to complete the reconfiguration." *Id.* at 1:52-57. This improvement was the basis for the '951 Patent, and, further confirms the challenges that the inventors of the '951 Patent faced when innovating in this space, and illustrates that Petitioner trivializes these challenges to make its fallacious obviousness argument. *See* Chakrabarty Decl., ¶83.

Accordingly, Petitioner fails to demonstrate that a POSITA would have been motivated to combine these two references to meet the claimed invention, as the references demonstrate that the combination Petitioner proposes would result in such significant technical challenges that a POSITA would not be motivated to attempt this combination in an effort to achieve the claimed invention. *See id.*, ¶78. For at least these reasons, Ground 1 fails.

(b) Petitioner overlooks the thermal issues that plagued 3D stacked FPGA chips and which fatally undermine Petitioner's obvious to try theory as it would not result in a reasonable expectation of success.

Petitioner argues that a POSITA would have found it obvious to try stacking *Cooke's* FPGA on *Bertin's* 3D integration and would have expected a reasonable expectation of success. Petition at 49. For similar reasons as described above, this assertion is also meritless. *See* §VI.A.2.b, *supra*; *see also* Chakrabarty Decl., ¶85.

In the Institution Decision, the Board concluded that:

> [A]n artisan of ordinary skill readily could have employed through-hole contacts to memory arrays using Bertin's and Cooke's stacked die techniques, where the advantages of FPGA's, stacked chips, and through-hole contacts were well-known.

Institution Decision at 37. The Board's conclusion rests on the assumption that Petitioner's obvious to try theory with reasonable expectation of success is correct. It is not. *See* Chakrabarty Decl., ¶86. Petitioner's overly simplistic obvious to try theory runs afoul of *KSR* because stacking FPGAs on a 3D multichip module is ***not*** one of "familiar elements according to known methods . . . [which] do[] no more than yield predictable results." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 416 (2007). Rather, the exact opposite is the case. *See* Chakrabarty Decl., ¶86.

Petitioner fails to recognize the known thermal challenges that plagued 3D FPGA development and design. *See id*., ¶87. In fact, none of Petitioner's asserted references discloses stacking an FPGA with a microprocessor to form a SDH module, let alone a SDH module with die-area interconnections. For example, while *Cooke* suggests utilizing vertically stacked memory with a single IC die having microprocessor and FPGA functionality, *Cooke* does not disclose either stacking the vertical memory stack above the FPGA or using die-area interconnects in such an arrangement. *See* Ex. 2014, Shanfield Tr. at 74:17-75:6 (admitting that FIG. 2 is merely a schematic relationship that does not show how the elements are

physically configured). *Cooke* never describes that the vertical memory stack is also stacked with the FPGA. *See* Chakrabarty Decl., ¶87. Moreover, as described above, and here again, *Alexander* proposed a 3D FPGA, the authors admitted that it could not fabricate its proposed design. *See* §VI.A.2.b, *supra*.

Further, *Bertin* does not cure the deficiencies of *Koyanagi* noted above. *Bertin,* like *Koyanagi*, does not teach stacking FPGAs on 3D multichip modules. Petitioner admits to this. *See* Petition at 47. But in a conclusory fashion supposes that *Bertin* inherently suggests 3D FPGA stacking because it describes logic chips. *Id.* This is a red herring. There are many specific types of ICs, including microprocessors, graphic processing units ("GPUs"), application specific integrated circuits ("ASICs"), and microcontrollers, that fall under the generic definition of a logic chip. *See* Chakrabarty Decl., ¶88.

However, "[i]t is well established that disclosure of a genus in the prior art is not necessarily a disclosure of every species that is a member of that genus." *Wasica Fin. GmbH v. Cont'l Auto. Sys., Inc.*, 853 F.3d 1272, 1285-86 (Fed. Cir. 2017) (quoting *Atofina v. Great Lakes Chem. Corp.*, 441 F.3d 991, 999 (Fed. Cir. 2006)) (affirming the Board's determination that "Oselin's broad invocation of 'any modulation scheme' (a genus) does not disclose with sufficient particularity the constant-frequency modulation scheme of claim 6 (a species).") (citation

omitted). *Bertin's* broad invocation of logic chips does not disclose with sufficient particularity a FPGA chip. *See* Chakrabarty Decl., ¶88.

Moreover, *Alexander* belies Petitioner's argument as it teaches that its proposed 3D FPGA stacking is deterred by thermal issues, as described above. *See* §VI.A.2.b, *supra*. In other words, a POSITA reading *Bertin* at the time of the invention—with an understanding of the known thermal issues as recognized by *Alexander* and other skilled artisans— would not have understood that *Bertin* inherently teaches stacking FPGAs. *See* Chakrabarty Decl., ¶89. Nowhere does *Bertin* offer a solution to the known 3D FPGA thermal issues that plagued stacking FPGAs on a 3D multichip module, as described above. *See* §VI.A.2.b, *supra*; *see also* Chakrabarty Decl., ¶89.

Further, the *Adam's* Court's principles discussed *supra* in Section VI.A.2.b applies here with equal force. *See Adams*, 383 U.S. at 51-52. As explained above, and, here again, a POSITA would ***not*** have found the '951 Patent's claimed invention—stacking a thinned microprocessor die element, a memory die element, and a FPGA (*see* §II, *supra*)—obvious to try with a reasonable expectation of success because of the known thermal issues, which a POSITA would ***not*** have ignored.

Finally, a POSITA would understand that Petitioner's alleged combination of *Bertin* with *Cooke's* FPGA would only exacerbate the high operating

temperatures caused by logic dies and would render the combined device inoperable. *See* Chakrabarty Decl., ¶90. As explained above, and, here again, *Alexander* teaches that the serious thermal issues its proposed 3D FPGA configuration suffers from can lead to less reliable operation. *Alexander* at 3-4. This is because the power consumption by logic dies, such as FPGAs and microprocessors, increase the operating temperatures. *Id.* As a result, a POSITA would understand that Petitioner's alleged combination of *Bertin's* 3D integration with *Cooke's* FPGA would only exacerbate the high operating temperatures caused by logic dies and would render the combined device inoperable. *See* Chakrabarty Decl., ¶90.

Therefore, Petitioner's contention that it would be obvious to try stacking *Cooke's* FPGAs on *Bertin's* 3D integration crumbles under the weight of contradictory evidence. *See id*., ¶91. For at least these reasons, Ground 2 fails.

VII. CONCLUSION

Petitioner has failed to prove by a preponderance of evidence that Challenged Claims 1, 4-5, 8, 10, and 13-15 of the '951 Patent are unpatentable. Arbor accordingly requests that the Board enter a final written decision affirming the patentability of those claims.

Respectfully submitted,

Dated: February 25, 2021 /James Hannah/

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(Case No. IPR2020-01021) *Attorneys for Patent Owner*

CERTIFICATE OF COMPLIANCE WITH 37 C.F.R. § 42.24

This paper complies with the type-volume limitation of 37 C.F.R. § 42.24. The paper includes 8,321 words, excluding the parts of the paper exempted by § 42.24(a).

This paper also complies with the typeface requirements of 37 C.F.R. § 42.6(a)(ii) and the type style requirements of § 42.6(a)(iii)&(iv).

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CERTIFICATE OF SERVICE

The undersigned certifies, in accordance with 37 C.F.R. § 42.6(e), that service was made on the Petitioner as detailed below.

Date of service	February 25, 2021
Manner of service	Electronic Mail (chris.mizzo@kirkland.com; greg.arovas@kirkland.com; bao.nguyen@kirkland.com; SAMSUNG-ARBOR-IPR@kirkland.com)
Documents served	PATENT OWNER'S RESPONSE
Persons Served	F. Christopher Mizzo Gregory S. Arovas Bao Nguyen

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