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Paper 34
Date: August 9, 2021

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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INTEL CORPORATION,
Petitioner,

v.

PACT XPP SCHWEIZ AG,
Patent Owner.

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IPR2020-00518
Patent 9,250,908 B2

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Before KEN B. BARRETT, CHARLES J. BOUDREAU, and CHRISTOPHER L. OGDEN, *Administrative Patent Judges*.

BARRETT, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining No Challenged Claim Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

A. Background and Summary

Intel Corporation ("Petitioner")[1] filed a Petition requesting *inter partes* review of U.S. Patent No. 9,250,908 B2 ("the '908 patent," Ex. 1001). Paper 3 ("Pet."). The Petition challenges the patentability of claim 5[2] of the '908 patent. PACT XPP Schweiz AG ("Patent Owner")[3] filed a Response to the Petition. Paper 21 ("PO Resp."). Petitioner filed a Reply (Paper 26, "Pet. Reply") and Patent Owner filed a Sur-reply (Paper 28, "PO Sur-reply"). With our authorization, Patent Owner filed, after its Sur-reply and prior to the final hearing, a copy of *Raytheon Technologies Corp. v. General Electric Co.*, 993 F.3d 1374, 2021 WL 1432964 (Fed. Cir. Apr. 16, 2021).[4] Ex. 2028.

An oral hearing was held on May 20, 2021, and a transcript of the hearing is included in the record. Paper 33 ("Tr.").

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[1] Petitioner identifies Intel Corporation as the real party-in-interest. Pet. 1.
[2] The Petition also has grounds directed to claim 4. However, because that claim has been statutorily disclaimed by Patent Owner, it is treated as if it never was part of the '908 patent. *See* Ex. 2002, 9; *see also* Paper 12, 14–15 (discussion of the status of claim 4 in the Decision Granting Institution). We do *not*, as Petitioner urges, treat the disclaimer as Patent Owner "conceding the invalidity of claim 4." Pet. Reply 1 (Petitioner presenting this argument without citation to supporting authority or to evidence of intent to concede unpatentability).
[3] Patent Owner identifies PACT XPP Schweiz AG (formerly known as Scientia Sol Mentis AG) as the real party-in-interest. Paper 5, 2.
[4] Patent Owner did not mention *Raytheon* during the hearing for this IPR but did file a demonstrative exhibit citing the case for the proposition that a disclaimer is not an admission that the disclaimed subject matter appears in the prior art. Ex. 2029, 12 (quoting *Raytheon*, 2021 WL 1432964 at *3 n.4).

This Final Written Decision is entered pursuant to 35 U.S.C. § 318(a). For the reasons discussed below, we determine that Petitioner has *not* shown by a preponderance of the evidence that claim 5 of the '908 patent is unpatentable.

B. Related Proceedings

One or both parties identify the following as matters involving or related to the '908 patent: *PACT XPP Schweiz AG v. Intel Corp.*, No. 19-cv-00267 (D. Del. Feb. 7, 2019); *PACT XPP Schweiz AG v. Intel Corp.*, No. 19-cv-00273 (W.D. Tex. Apr. 23, 2019); *Intel Corp. v. PACT XPP Schweiz AG*, No. 19-cv-02241 (N.D. Cal. Apr. 25, 2019); and *PACT XPP Schweiz AG v. Intel Corp.*, No. 1:19-cv-01006 (D. Del. May 30, 2019). Pet. 1; Paper 5, 1–2.

C. The '908 Patent

The '908 patent is titled "Multi-Processor Bus and Cache Interconnection System." Ex. 1001, code (54). According to the Abstract of the '908 patent,

> A multi-processor is provided [with] a segmented cache and an interconnection system for connecting the processors to the cache segments. An interface unit communicates to external devices using module IDs and timestamps.

Id. at code (57).

D. The Challenged Claim

The sole remaining challenged claim of the '908 patent, claim 5, depends from disclaimed independent claim 4. Independent claim 4 and dependent claim 5 are reproduced below with emphasis added.

> 4. A system, the system comprising:
> a processing system comprising
> a plurality of processors; and

at least one separated cache not part any processor;
a bus system connecting the processing system to one or more external devices;
at least one interface transmitting data between the processing system and external devices via the bus system;
at least some of the plurality of processors, the at least one interface, and the at least one separated cache having a module identification (ID); and wherein
the at least one interface to transmit data via the bus system using a protocol, comprising:
i. the module ID of an interface, a processor, a separated cache requesting a transmission,
ii. the module ID of an interface, a processor, a separated cache receiving a transmission; and/or
iii. the address of a target within the interface, the processor, the separated cache or the external device unit receiving a train mission; and
wherein *the at least one separated cache comprises a separated cache segment for at least some of the plurality of processors*; the system further comprising:
an interconnect system interconnecting each of the separated cache segments with each of the processors, each of the processors with neighboring processors, and each of the separated cache segments with neighboring separated cache segments; and
an arbiter, the arbiter controlling access of a processor to the interconnect system.

5. The bus system of claim 4 where the arbiter is operable to allow processor access in chronological sequence.

Ex. 1001, 52:43–53:7 (emphasis added).

E. Evidence

Petitioner relies on the following references:

Reference		**Dates**	**Exhibit No.**
Kabemoto	US 5,890,217	Filed Feb. 7, 1996; Issued Mar. 30, 1999	1005

Reference		Dates	Exhibit No.
Wu	US 6,047,355	Filed Mar. 10, 1997; Issued Apr. 4, 2000	1006
Bauman	US 5,680,571	Filed Dec. 28, 1995; Issued Oct. 21, 1997	1007
Chaney	US 5,930,822	Filed Sept. 27, 1996; Issued July 27, 1999	1008

Petitioner also relies on the Declaration of Dr. Pinaki Mazumder (Ex. 1003) in support of its arguments, and Patent Owner relies on the Declaration of Dr. Murali Annavaram (Ex. 2024) in support of its arguments. The parties rely on other exhibits as discussed below.

F. Asserted Grounds of Unpatentability

Petitioner asserts that the challenged claim is unpatentable on the following grounds:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
5	103(a)	Kabemoto, Bauman, Chaney
5	103(a)	Wu, Bauman, Chaney

II. ANALYSIS

A. Principles of Law

Petitioner bears the burden of persuasion to prove unpatentability of the claim challenged in the Petition, and that burden never shifts to Patent Owner. *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015). To prevail, Petitioner must establish by a preponderance of the evidence that the challenged claim is unpatentable. 35 U.S.C. § 316(e) (2018); 37 C.F.R. § 42.1(d) (2019).

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that

the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) any objective evidence of obviousness or non-obviousness.[5] *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

B. The Level of Ordinary Skill in the Art

In determining the level of ordinary skill in the art, various factors may be considered, including the "type of problems encountered in the art; prior art solutions to those problems; rapidity with which innovations are made; sophistication of the technology; and educational level of active workers in the field." *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995) (internal quotation marks and citation omitted).

Petitioner's declarant, Dr. Pinaki Mazumder, opines that "[a] person of ordinary skill in the art ('POSITA') at the time of the alleged invention would have had at least a[n] M.S. degree in electrical engineering, and at least three years of experience with processor design and memory architecture." Ex. 1003 ¶ 66; *see* Pet. 12. Patent Owner's declarant, Dr. Murali Annavaram, for purposes of his declaration, adopts Dr. Mazumder's definition (with the understanding that the referenced master's degree in electrical engineering includes related fields such as computer engineering). Ex. 2024 ¶ 21.

[5] The parties have not directed our attention to any objective evidence of obviousness or non-obviousness.

We determine that the definition offered by Dr. Mazumder comports with the qualifications a person would have needed to understand and implement the teachings of the '908 patent and the prior art of record. *Cf. Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (the prior art itself may reflect an appropriate level of skill in the art). For purposes of this decision, we apply Dr. Mazumder's description of the person of ordinary skill in the art.

C. Claim Construction

We apply the same claim construction standard used in district court actions under 35 U.S.C. § 282(b), namely that articulated in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). *See* 37 C.F.R. § 42.100(b) (2019).

In applying that standard, claim terms generally are given their ordinary and customary meaning as would have been understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips*, 415 F.3d at 1312–13. "In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence." *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17).

Petitioner does not propose an explicit claim construction for any term, asserting that every term should be given its ordinary and customary meaning. Pet. 5. Patent Owner similarly does not propose an explicit claim construction for any term. *See* PO Resp. *passim*. In their later respective briefs, the parties each argue that the other has, in the context of the Bauman

reference, applied an incorrect construction for "interconnect system"—disputing whether a connection between processors must be direct and have data flowing between the processors in two directions. *See* Pet. Reply 17; PO Sur-reply 12–13. As discussed below, we find that Petitioner identifies in each ground a component of the respective primary reference, Kabemoto and Wu, as the recited "interconnect system" in Petitioner's proposed combination. Therefore, we need not reach the issue of whether Bauman's structure(s) connect processors in the manner required by the claim, including any claim interpretation required to resolve this issue.

We determine that no claim terms require express construction.

D. The Alleged Obviousness of Claim 5 over Kabemoto, Bauman, and Chaney

Petitioner alleges that dependent claim 5 of the '908 patent would have been obvious over Kabemoto, Bauman, and Chaney. *See* Pet. 58–63; *see also id.* at 19–58 (Petitioner's analysis of the limitations of underlying independent claim 4). Claim 5 depends from disclaimed independent claim 4 and, therefore, includes all of the limitations of that underlying independent claim. Petitioner's challenge to dependent claim 5 is premised on the contention that underlying independent claim 4 would have been obvious over the combination of Kabemoto and Bauman. *Id.* at 58. Petitioner relies on Kabemoto for much of the claimed subject matter, and contends that Bauman teaches, *inter alia*, a segmented second-level cache that is shared between processors. *See, e.g.*, *id.* at 42. Petitioner relies on Chaney for teachings directed to the recitation of dependent claim 5, namely that regarding accessing in chronological sequence. *See id.* at 58–59.

Patent Owner's arguments in response pertain to the limitation reciting "wherein the at least one separated cache comprises a separated

cache segment for at least some of the plurality of processors" (identified as "element i" of claim 4) and the "interconnect system" limitation (identified as "element j"). *See* PO Resp. 14. Patent Owner argues that Petitioner has failed to establish that a person of ordinary skill in the art would have had a reason to combine Kabemoto and Bauman for element i or j and that Petitioner's proposed combination of references would lack element j, the "interconnect system." *See, e.g.*, *id.*

For the reasons discussed below, we agree with Patent Owner that Petitioner has not shown that claim 5 would have been obvious over Kabemoto, Bauman, and Chaney. Petitioner has not shown that the combination of Kabemoto, Bauman, and Chaney teaches or suggests all the limitations of claim 5 or that a person of ordinary skill in the art would have had a reason to combine the references in the proposed manner.

1. Kabemoto (Ex. 1005)

Kabemoto addresses the difficulty, in conventional systems, of achieving high speed processing due to the maintenance of cache coherence. Kabemoto pertains to:

> a cache coherence apparatus for a multiprocessor system in which a plurality of processor modules are connected through a system bus [(external common bus)] and, more particularly, to a coherence apparatus for a cache of a multiprocessor system in which a plurality of processor elements with caches are connected in a processor module through a main storage and an internal common bus [(a snoop bus)].

Ex. 1005, 1:5–11; *id.* at 3:11–14.

Kabemoto's system has the following: several processor modules, each processor module having one or more processors and each processor provided with a cache unit; a main storage shared by the processor group and divided into local storages (each local storage being "distributed main

storage"); and a memory control module. *Id.* at 2:66–3:40. "The distributed main storage and the cache unit are connected by a snoop bus (internal common bus) [and t]he processor modules are connected by a system bus (external common bus)." *Id.* at 3:11–14. "The cache unit divides the cache line into a plurality of sublines and manages the same." *Id.* at 3:41–42. Kabemoto's Figure 2 is reproduced below.

FIG. 2

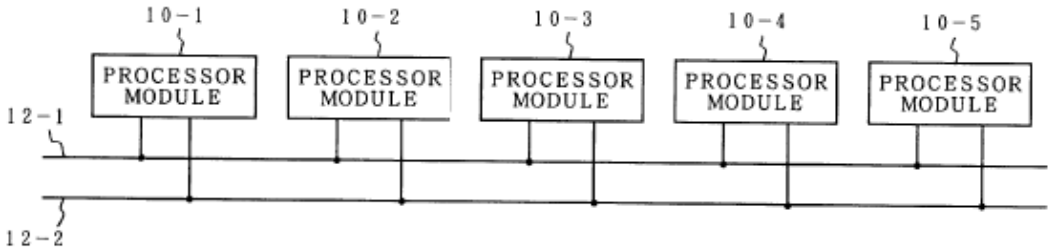


Figure 2 is a block diagram of a multiprocessor module construction of Kabemoto's system. *Id.* at 13:51–52. Figure 2 depicts five processor modules, 10-1 through 10-5, connected via system buses 12-1 and 12-2. *Id.* at 16:8–14. Figure 3 is reproduced below.

FIG. 3

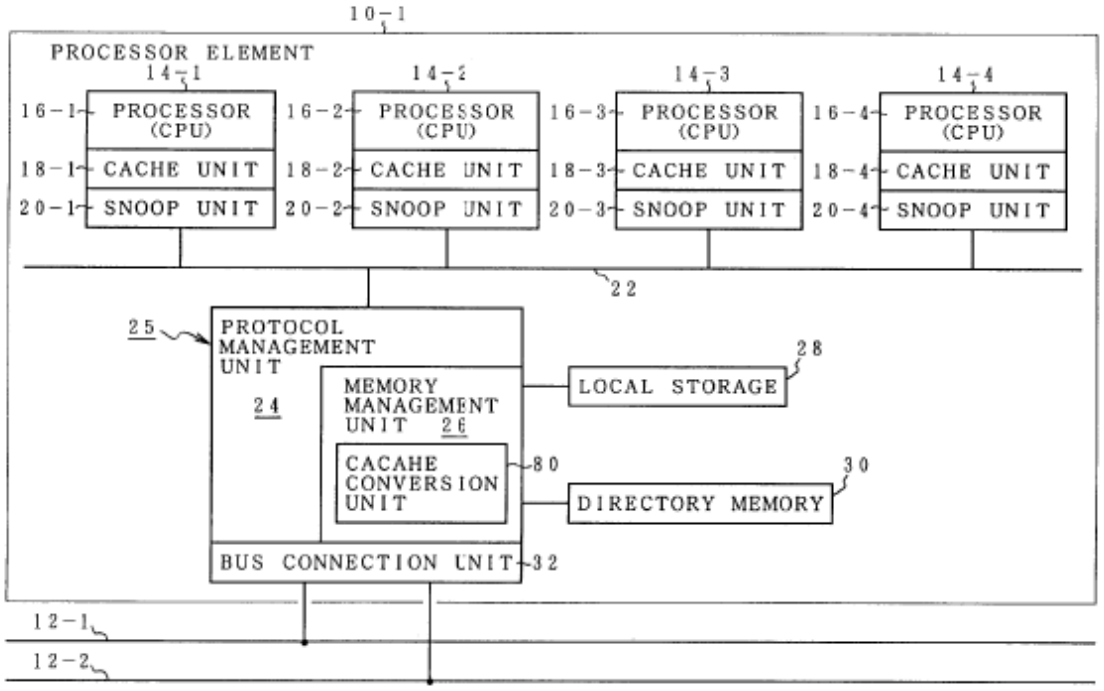
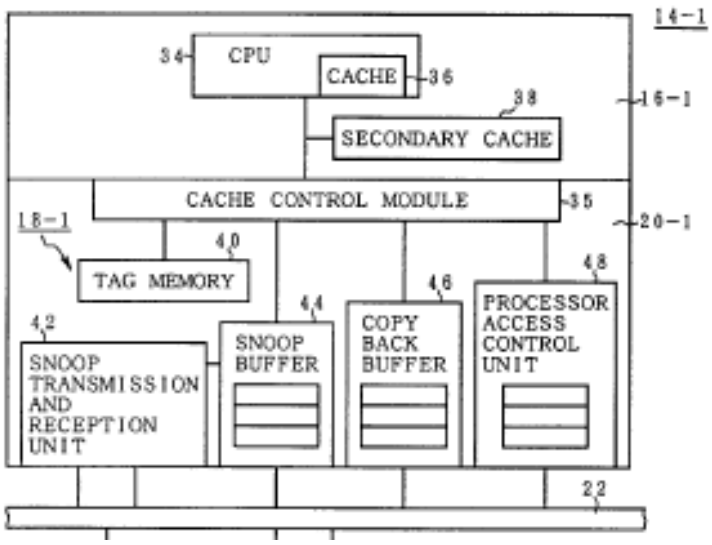


Figure 3 is a block diagram of an internal construction of a processor module of Figure 2. *Id.* at 13:53–54. Figure 3 depicts processor module 10-1 having four processor elements 14-1 to 14-4 connected through snoop bus 22. *Id.* at 16:14–18. Each processor element comprises a processor (central processing unit; "CPU"), a cache unit, and a snoop unit. *Id.* at 16:18–21. "To guarantee a coherence of data among the cache units 18-1 to 18-4 of, for example, the four processor elements 14-1 to 14-4 in FIG. 3 connected by the snoop bus 22, the secondary cache 38 is snooped by the snoop bus 22." *Id.* at 17:27–31.

A cropped version of Figure 4 is reproduced below.

FIG. 4



The figure above is a cropped version of Figure 4, which is a block diagram of an internal construction of the processor module of Figure 3. *Id.* at 13:55–56. Figure 4 depicts secondary cache 38 outside of CPU 34 and primary cache 36 of CPU 34. *Id.* at 17:4–12.

2. Bauman (Ex. 1007)

Bauman pertains to:

> cache architectures for data processing systems and more particularly to a shared memory multi-processor data processing system having a plurality of second-level caches, where each of the second-level is comprised of a separate instruction second-level cache and a separate operand second-level cache.

Ex. 1007, 1:18–23. Bauman discloses a system with eight Instruction Processors (IPs) and two Storage Controllers, with each Storage Controller coupled to four of the Instruction Processors. *Id.* at 4:25–51. Each Storage Controller has a Global SLC (second-level cache), with the two Global SLCs coupled to each other and with each Global SLC directly accessed by

four Instruction Processors and indirectly accessed by the other four Instruction Processors. *Id.* at 4:55–5:4. "[T]he second-level cache [is] divided into a plurality of segments [and e]ach of the segments is dedicated to caching a predetermined portion of addressable memory." *Id.* at 3:35–38.

Figure 1 is reproduced below.

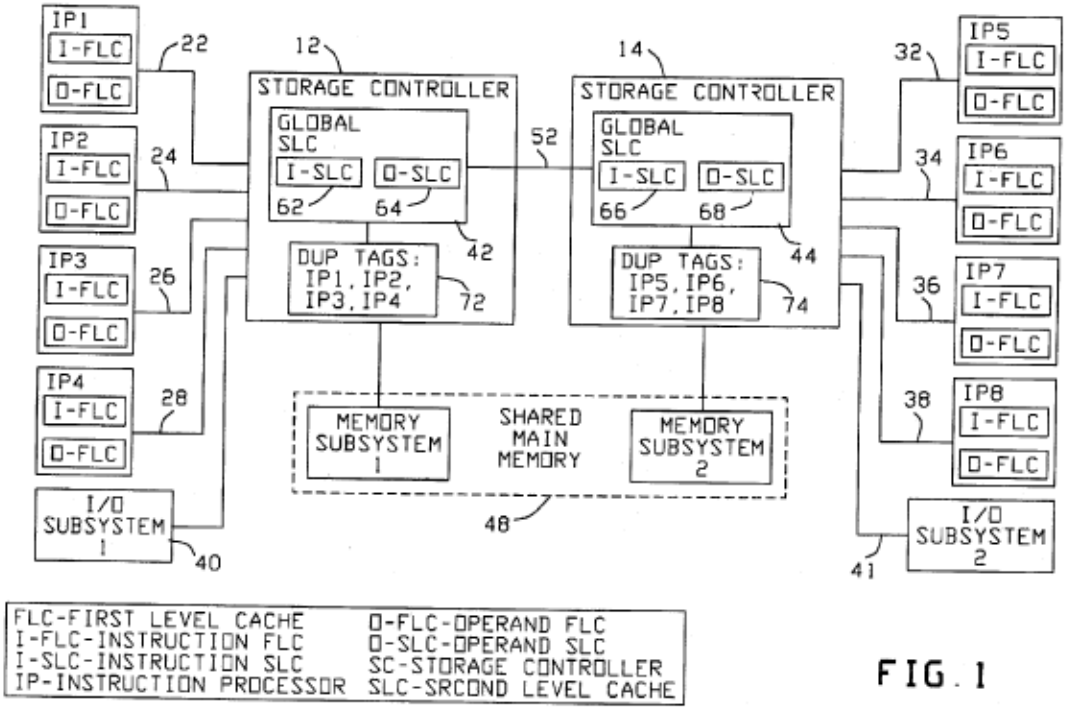


FIG. 1

Figure 1 is a block diagram of a multi-processor data processing system. *Id.* at 3:62–63. The figure shows, *inter alia*, four Instruction Processors, IP1 through IP4, coupled to Storage Controller 12, which has Global SLC 42, which, in turn, has dedicated Instruction Second-Level Cache (I-SLC) 62 and dedicated Operand Second-Level Cache (O-SLC) 64. *Id.* at 4:42–46, 4:56–57, 5:29–32. Bauman explains that "the instruction second-level cache and operand second-level cache tag cycles operate in tandem [and t]his simplifies maintaining cache coherency between the instruction and operand second-level caches." *Id.* at 14:27–31.

3. Chaney (Ex. 1008)

Chaney "pertains in general to multiprocessor computer systems and in particular to a method and system for maintaining cache coherency in such systems." Ex. 1008, 1:19–21. According to Chaney, "[i]n some multiprocessor systems, the caches are 'strongly ordered.'" *Id.* at 1:33–34. "In a strongly ordered system, a processor sees the stores of other processors in the same node in the same order in which the stores are made." *Id.* at 1:34–36; *see also id.* at 4:16-19. Chaney's system of maintaining strong ordering includes "[a]n arbitrator within the processor agent [that] receives the timestamps [for the memory transactions] and the memory transactions." *Id.* at code (57) (Abstract). "Using the timestamps, the arbitrator reorders the memory transactions and sends the transactions to the processors in the order in which the transactions were sent." *Id.*

4. Analysis

As mentioned, the only challenged claim, claim 5, depends directly from independent claim 4, and Patent Owner's arguments are directed to that underlying independent claim. PO Resp. 14. Independent claim 4 calls for, generally speaking and in pertinent part, a system having a plurality of processors, a separated cache not part of any processor and comprising a separated cache segment for some of the processors, and an interconnect system. *See* Ex. 1001, 52:43–53:5. As to the cache, the specific claim recitation is "wherein the at least one separated cache comprises a separated cache segment for at least some of the plurality of processors." *Id.* at 52:63–65. The "interconnect system" limitation requires three specific interconnecting relationships, which will be discussed further below. *See id.* at 52:66–53:3.

Petitioner contends that Kabemoto discloses a processor (CPU 34) and a separated cache (secondary cache 38), which is connected to the processor. Pet. 22–23, 41–42. Petitioner utilizes an annotated and cropped version of Kabemoto's Figure 4, which depicts this relationship for processor element 14-1. *See id.* at 23. To address the "plurality of processors" aspect of the claim, Petitioner contends that the CPUs 34 in the four processor elements 14-1 through 14-4 are the recited "processors." *Id.* at 22.

Petitioner turns to Bauman for the aspect of the claim pertaining to a cache segment for a plurality of processors. *Id.* at 42. Petitioner asserts that Bauman discloses a separated and segmented cache, the global second-level cache (SLC), and that there is a segment for a plurality of processors. *Id.* at 42–46. According to Petitioner, "Bauman discloses 'a second-level cache that is shared between the processors where the second-level cache also has a separate instruction cache and operand cache," and that the second-level cache comprises separate cache segments. *Id.* at 42–44 (quoting Ex. 1007, 1:56–63).

Petitioner proposes the modification of Kabemoto's system by the "use [of] Bauman's segmented global SLC in place of the secondary cache of Kabemoto's processor module." Pet. 48.

> Within each of Kabemoto's processor modules (which each contain a "processing system"), Bauman's segmented global SLC replaces Kabemoto's secondary caches and is connected to snoop bus 22 on the outside of element 14-1. Rather than four secondary caches housed in four different elements, Kabemoto's processing system would use a single second-level cache divided into four segments. *See id.*, ¶135.

Id. at 54. Thus, Petitioner proposes to remove Kabemoto's four secondary caches—one in each of the four processor elements—and insert a single

segmented cache of Bauman onto Kabemoto's snoop bus. Petitioner, as discussed below, identifies Kabemoto's snoop bus as the recited "interconnect system." *See, e.g.*, Pet. 54 ("A POSA [person of ordinary skill in the art] would have been motivated to use Bauman's segmented global SLC with Kabemoto's internal snoop bus ('interconnect system') for at least the reasons described in Section X.A.1.i.").

a. The Interconnect System Limitation

Patent Owner argues that Petitioner's proposed combination would lack the required "interconnect system." PO Resp. 26; *see also id.* at 4 ("[T]he resulting combination would not include the claimed interconnection system. As Professor Annavaram explains, neither Kabemoto [n]or Wu disclose[s] an interconnect system that interconnects all three sets of required elements; thus, if the caches in Kabemoto or Wu were simply replaced with Bauman's caches, the interconnect system would not be changed.").

The subject limitation recites:

> an interconnect system interconnecting
> [1] each of the separated cache segments with each of the processors,
> [2] each of the processors with neighboring processors, and
> [3] each of the separated cache segments with neighboring separated cache segments.

Ex. 1001, 52:66–53:3 (annotations and paragraphing added).

Patent Owner specifically argues, *inter alia*, that the recited segment-to-segment interconnection is missing from Petitioner's proposed combination.[6] PO Resp. 25 ("Because Kabemoto does not disclose

[6] Petitioner's Reply does not address Patent Owner's argument directly, instead incorrectly asserting: "[N]o reasonable dispute exists that Kabemoto

element i ('at least one separated cache compris[ing] a separated cache segment for at least some of the plurality of processors'), it also cannot disclose element j, which requires an interconnect system that interconnects, among other things, the separated cache segments of element i with each other and with other elements."); PO Sur-reply 5 ("[I]f Bauman's second-level cache is simply substituted for Kabemoto's secondary cache, the result lacks the claimed interconnect (at least because the snoop bus does not connect cache segments to neighboring cache segments).").

In addressing the "interconnect system" limitation, Petitioner begins with the assertion that "Kabemoto teaches a modular processing system where, within a module, all processors (CPUs) and secondary caches are interconnected by an interconnection system, namely, an internal snoop bus." Pet. 50. Petitioner's annotated version of Kabemoto's Figure 3 is reproduced below.

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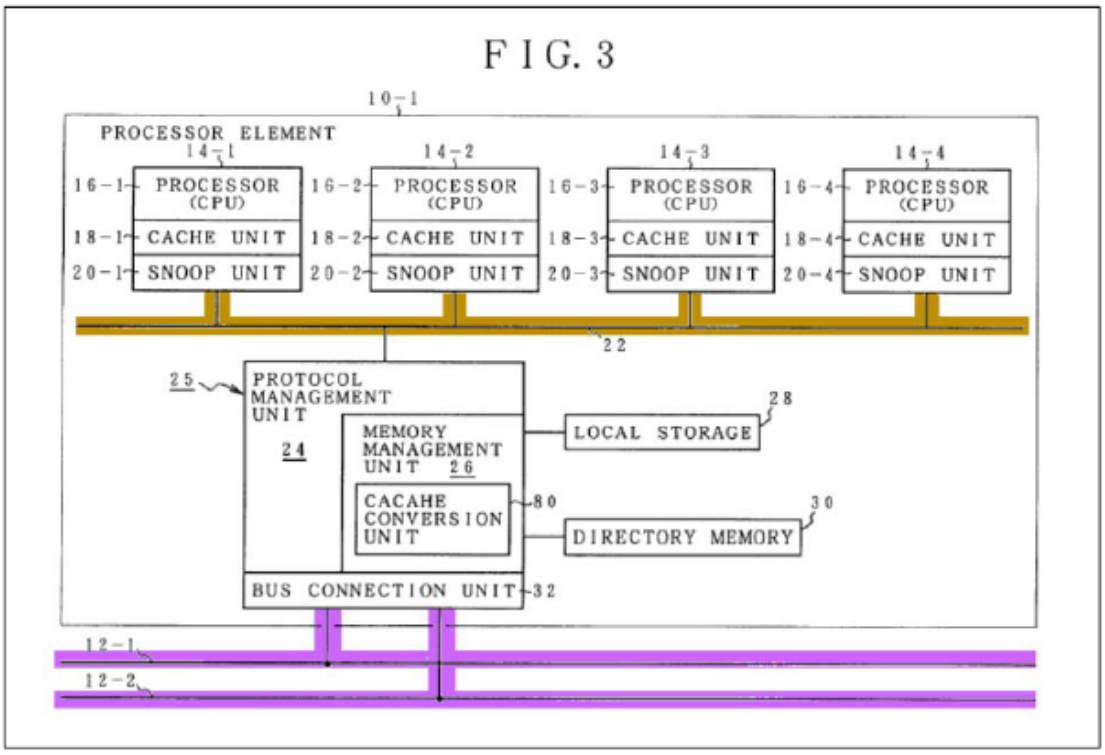
and Bauman teach the claimed 'interconnect system.' PACT does not dispute that Kabemoto and Bauman teach an interconnect system that interconnects . . . each separated cache segment with neighboring cache segments . . . ." Pet. Reply 13.



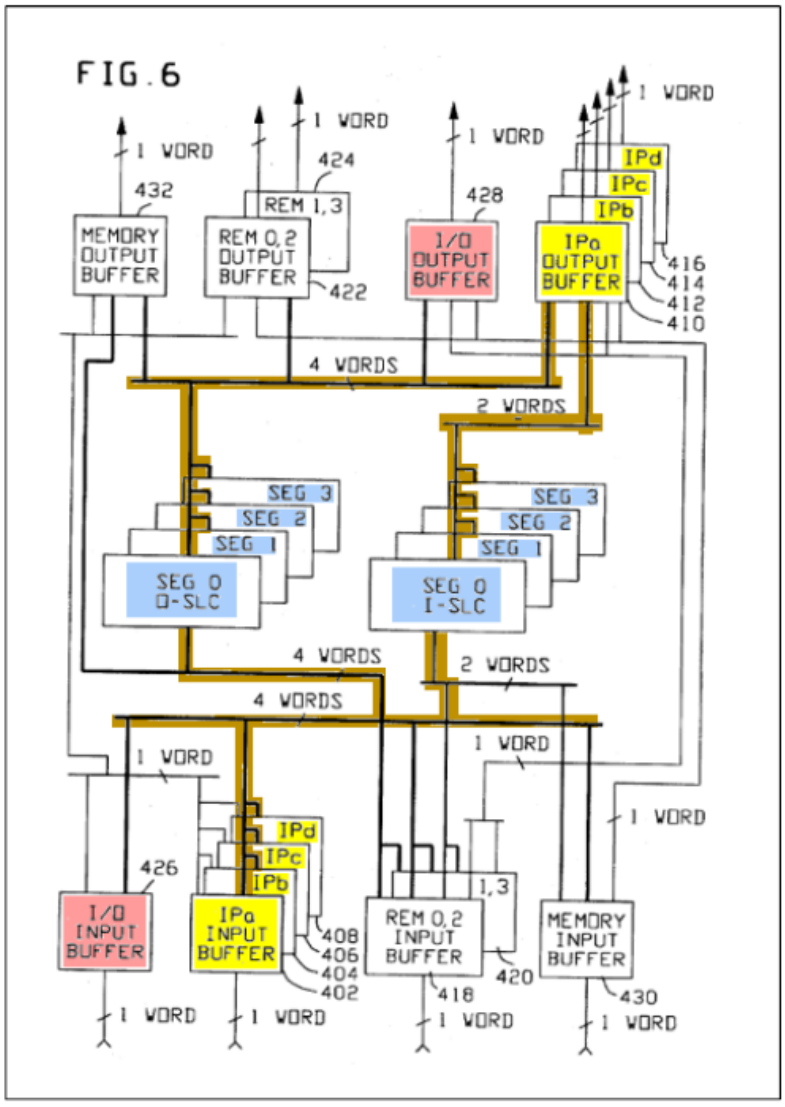
Above is Figure 3—a block diagram of an internal construction of a processor module—with, *inter alia*, Petitioner's highlighting in gold of snoop bus 22. Pet. 51; Ex. 1005, 13:53–54. Petitioner contends that snoop bus 22 interconnects the four processors located in each of processor elements 14-1 through 14-4. Pet. 51. Petitioner continues:

> Similarly, processor module 10-1 contains four separated caches (secondary cache 38) housed in elements 14-1 through 14-4. *See supra* Section X.A.1.c; *see also* Ex. 1005, FIGS. 3, 4. *Because each processor element 14-1 through 14-4 is connected to each neighboring processor element by virtue of snoop bus 22, snoop bus 22 interconnects each separated cache with each neighboring cache.* Ex. 1003, ¶130. Likewise, snoop bus 22 interconnects each separated cache with each processor. *Id.*, ¶131.

Id. at 52 (emphasis added). Thus, at this point in the Petition, Petitioner has alleged merely that the snoop bus is a cache-to-cache interconnection. However, the claim requires a structure that interconnects neighboring cache

segments, not simply neighboring caches. This distinction leads Patent Owner to argue, "Petitioner contends that Kabemoto's snoop bus 'interconnects each separated cache with each neighboring cache' (Petition, 52), but does not show that the snoop bus interconnects separated cache segments with neighboring segments . . . because Kabemoto does not have cache segments." PO Resp. 27. We agree.

Petitioner next argues that "the combination of Kabemoto and Bauman likewise discloses this limitation." Pet. 52. Petitioner's annotated version of Bauman's Figure 6 is reproduced below.



Above is Figure 6 of Bauman, "a block diagram that illustrates the data path between the requesting processors, the second-level cache, and the memory" (Ex. 1007, 11:18–20), with Petitioner's addition of highlighting of certain features. Pet. 53. Petitioner contends that Bauman's Figure 6 discloses processors (yellow), cache segments (blue), and data paths (gold), and that the gold data paths satisfy the three relationships of the "interconnect system" limitation. *Id.* at 53–54. In particular, Petitioner contends that "each of the cache segments is interconnected to each neighboring cache segment via the data paths." *Id.* at 54 (citing Ex. 1003 ¶¶ 133–134).

However, Petitioner's proposed combination utilizes the processors and interconnection system of Kabemoto, and only uses, from Bauman, the segmented global SLC. *See* Pet. 54. Petitioner, in articulating the proposed combination, explains that "Bauman's segmented global SLC [(second-level cache)] replaces Kabemoto's secondary caches and is connected to snoop bus 22 on the outside of element 14-1." *Id.* Petitioner repeatedly identifies Kabemoto's snoop bus as the recited "interconnect system" of the claim. *E.g.*, *id.* ("A POSA would have been motivated to use Bauman's segmented global SLC with Kabemoto's internal snoop bus ('interconnect system')."); *id.* ("A POSA would have further understood that Kabemoto's internal snoop bus ('interconnect system') would maintain cache coherence among the various cache segments and the primary caches embedded within each CPU 34 (the claimed 'processor')."); *id.* at 55 ("A POSA would have found it obvious that processor access unit 48 is an arbiter that control access of a processor to the internal snoop bus ('interconnect system').").

Even if, as Petitioner contends, Bauman teaches an interconnect system having the three relationships recited in the claim, Petitioner does not

articulate adequately a proposed combination that utilizes that teaching. Petitioner does not explain adequately how Kabemoto's internal snoop bus in the proposed combination is, as required by the claim, "interconnecting . . . each of the separated cache *segments* with neighboring separated cache *segments*." Ex. 1001, 52:66–53:3 (emphasis added). Thus, Petitioner has failed to demonstrate that the proposed combination has the claimed "interconnect system."

b. Reason to Combine

As mentioned, Petitioner's proposed combination involves replacing the four individual secondary caches located in Kabemoto's processor elements 14-1 through 14-4 with Bauman's single second-level cache divided into four segments, and placing Bauman's cache on Kabemoto's snoop bus outside of processor element 14-1. Pet. 54. Petitioner asserts that there are three reasons why a person of ordinary skill in the art would have been motivated to make the proposed modification. *Id.* at 48–50 (addressing the limitation requiring a separated segmented cache having a separated cache segment for at least some of the plurality of processors); *see also id.* at 54 (addressing the "interconnect system" limitation and relying on the same reasons). Petitioner argues: 1) "the combination of Kabemoto and Bauman represents the use of known techniques to improve similar devices in the same way," 2) "Kabemoto provides a teaching, suggestion, or motivation that would have led a POSA to combine the teachings of Kabemoto and Bauman to arrive at the claimed invention," and 3) "Bauman provides a teaching, suggestion, or motivation that would have led a POSA to combine the teachings of Kabemoto and Bauman to arrive at the claimed invention." *Id.* at 48–49. Patent Owner argues that Petitioner has failed to

satisfy its burden of establishing a reason to combine the references as proposed. *See, e.g.*, PO Resp. 14, 18.

We first address Petitioner's two "teaching, suggestion, or motivation" arguments and then address the "known techniques" argument.

(1) Kabemoto's Alleged Teaching, Suggestion, or Motivation

Petitioner contends that "Kabemoto provides an express motivation to combine, as segmentation of its cache line improves management of the cache." Pet. 49. According to Petitioner, the express motivation is found in Kabemoto's statement that "[t]he cache unit divides the cache line into a plurality of sublines and manages the same." *Id.* (citing Ex. 1005, 3:41–42, 3:62–64 ("The cache unit divides the cache line of, for example, 256 bytes into sublines each consisting of 64 bytes for management purposes.")). Petitioner concludes with the argument that, "[b]ased on this express disclosure, a [person of ordinary skill in the art] would have understood that Kabemoto's multiple separate secondary caches 38 benefit from segmentation, and would have been motivated to use Bauman's particular segmented second-level cache for management purposes." *Id.* (citing Ex. 1003 ¶ 126).

We do not find Petitioner's argument persuasive. Petitioner contends that Kabemoto teaches segmenting cache lines for management purposes and argues that a person of ordinary skill in the art would have understood that a segmented cache is easier to manage. Pet. 49. That, if correct, might suggest modifying Kabemoto by segmenting the existing secondary caches. However, the challenged claim requires more than mere segmentation. The claimed subject matter includes a cache segment for some of the plurality of processors. Neither Petitioner nor Dr. Mazumder explains adequately why a

segmentation teaching in Kabemoto would prompt a person of ordinary skill in the art to replace the existing four caches—each located with its respective processor—with a single cache of Bauman located on the snoop bus so as to be associated with a plurality of processors. *See* Pet. 49; Ex. 1003 ¶ 126 (Petitioner's expert concluding: "Based on this disclosure, a POSITA would have understood that a segmented cache is easier to manage and would have been motivated to use Bauman's segmented second-level cache as a global cache to achieve this benefit.").

(2) Bauman's Alleged Teaching, Suggestion, or Motivation

Petitioner also contends that "Bauman provides a teaching, suggestion, or motivation that would have led a POSA to combine the teachings of Kabemoto and Bauman to arrive at the claimed invention" and that "Bauman's global SLC would have improved the functionality of Kabemoto's processor." Pet. 49. According to Petitioner:

> *As Bauman teaches, segmenting the global cache "simplifies maintaining cache coherency between the instruction and operand second-level caches.*" Ex. 1007, 14:28–31. In other words, because the cache segments "operate in tandem" (*id.*, 14:28-30), Kabemoto's processing system would require fewer transactions to maintain cache coherency when using Bauman's global SLC.

Id. at 49–50 (emphasis added) (citing Ex. 1003 ¶ 127). Petitioner's expert, Dr. Mazumder, testifies somewhat similarly but does not include all of Petitioner's implied logical ties, for example, the language "In other words, because" at the transition between the two propositions quoted above. *See* Ex. 1003 ¶ 127 (Dr. Mazumder: "Bauman teaches that using a segmented global cache 'simplifies maintaining cache coherency between the instruction and operand second-level caches' and that the different cache

segments 'operate in tandem.' Ex. 1007, 14:28-31. A POSITA would have understood that Bauman's global SLC would require fewer transactions to maintain cache coherency.").

Petitioner also argues, "[i]n addition, the segmented global SLC has 'sufficient tag bandpass available to meet the request rate of all the requesters, with no significant performance loss' (*id.*, 14:31-34), meaning that Kabemoto's processing system would operate faster without experiencing any loss in performance." Pet. 50.

Patent Owner notes that the purported teaching relied on by Petitioner and Dr. Mazumder is an edited version of Bauman's statement, and argues that Petitioner mischaracterizes Bauman's disclosure. PO Resp. 24–25 (citing Ex. 2024 ¶ 46). In context, Bauman states:

> In the exemplary system, *the instruction second-level cache and operand second-level cache tag cycles operate in tandem. This simplifies maintaining cache coherency between the instruction and operand second-level caches.* In addition, there is sufficient tag bandpass available to meet the request rate of all the requesters, with no significant performance loss relative to any speed advantage that might be obtained by operating the instruction and operation second-level cache tags as independent elements.

Ex. 1004, 14:28–36 (emphasis added). Thus and as Patent Owner notes (PO Resp. 25), Bauman identifies that which simplifies maintaining cache coherency as "the instruction second-level cache and operand second-level cache tag cycles operate in tandem." Ex. 1004, 14:28–31. To the extent that Petitioner contends, and its expert opines, that Bauman's statement as to the source of the simplification means the same as "segmenting the global cache," Petitioner does not direct our attention to any adequately explained basis in the Petition or in Dr. Mazumder's declaration for this otherwise

conclusory assertion. *See* Pet. 49–50; Ex. 1003 ¶ 127. In contrast, Patent Owner's expert, Dr. Annavaram, testifies that "the portion of Bauman that Dr. Mazumder is quoting is not talking about *segmented* caches." Ex. 2024 ¶ 46 (emphasis added). Dr. Annavaram continues:

> This section is describing the advantages of using separate instruction and operand second-level caches with cache tags that operate in tandem. It also explains that there is no disadvantage to operating the instruction and operand cache tags in tandem rather than independently. It does not say, or even suggest, that using a segmented cache simplifies maintaining cache coherency or allows a proces[s]ing system to run faster.

Id. (citing Ex. 1007, 14:28–36). We find Dr. Annavaram's testimony on this issue to be more credible than Petitioner's expert, Dr. Mazumder.

In its Reply to Patent Owner's arguments, Petitioner contends that there is a tie between the language of Bauman's actual quote and Petitioner's assertion of an explicit motivating teaching. *See* Pet. Reply 12–13.[7] Petitioner asserts that, "as [Petitioner] Intel's expert explains—and as [Patent Owner] PACT's expert admits—the benefits of the instruction and operand caches are a direct result of segmenting the second-level cache." *Id.* (citing Ex. 1003 ¶ 127; Ex. 1047, 73:9–19, 72:5–9, 74:8–23). Contrary to Petitioner's assertions, we fail to discern an adequate explanation from Petitioner's expert in the cited paragraph that ties the relied-on purported

[7] Petitioner's Reply asserts that Bauman's purported express motivation to combine was "explained in the petition" and ambiguously cites to nine pages of the Petition and nine paragraphs of its expert's declaration. *See* Pet. Reply 12 (citing Pet. 42–50; Ex. 1003 ¶¶ 119–127). The single paragraph on point in the Petition, that beginning with "Third, Bauman provides a teaching, suggestion, or motivation . . . ," spans pages 49 to 50 of the Petition and cites only paragraph 127 of Dr. Mazumder's declaration.

benefit to the now-asserted "direct result." *See* Ex. 1003 ¶ 127. And, we fail to discern any clear admission from Patent Owner's expert that the purported benefit relied on in the Petition (*see* Pet. 49–50) is a "direct result" of that taught by Bauman. *See* Ex. 1047, 72:5–9, 73:9–19, 74:8–23.

Also in its Reply, Petitioner argues that Patent Owner's expert admitted on cross-examination "that segmenting a global cache provides several benefits." Pet. Reply 13 (citing Ex. 1047, 47:4–49:15, 76:11–24). However, even if there was such an admission, Petitioner does not identify how, in the Petition, the existence of such purported benefits—for example, "increased 'manufacturability,'"—were discussed as part of Petitioner's teaching-to-combine rationale. Pet. Reply 13; *see id.* at 12 (characterizing its theory in the Petition as: "Bauman provides an express motivation to combine—Bauman's segmented cache simplifies cache coherence and improves operating speed."). Additionally, we find persuasive Patent Owner's argument that an understanding of its expert today is not probative of the understanding of a person of ordinary skill in the art back in the pertinent timeframe. *See* PO Sur-reply 9–10.

We are not persuaded by Petitioner's argument that Bauman provides an explicit motivation to combine the references' teachings to arrive at the claimed subject matter.

(3) The "Known Technique" Rationale

Petitioner further argues that "the combination of Kabemoto and Bauman represents the use of known techniques to improve similar devices in the same way." Pet. 48. Petitioner is referring to the "known technique" rationale of *KSR*. *See* Pet. Reply 4 (reiterating its "known technique" position and citing *KSR*, 550 U.S. at 401). The Court, in *KSR*, explained that, "if a technique has been used to improve one device, and a person of

ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond that person's skill." *KSR*, 550 U.S. at 401.

After the initial indication that its theory of the case is the "known techniques" rationale, Petitioner presents several assertions regarding the purported similarity of the two relied-on references' structures and problems addressed. *See* Pet. 48. However, Petitioner does not, at least in this section of the Petition, identify clearly the known technique underlying Petitioner's rationale or how such a technique would improve a similar device. *See id.* at 48–49. Accordingly, the Petition fails to articulate adequately a "known technique" rationale.

As discussed above, Petitioner argues that "Bauman's global SLC would have improved the functionality of Kabemoto's processor [and, a]s Bauman teaches, segmenting the global cache 'simplifies maintaining cache coherency between the instruction and operand second-level caches.'" Pet. 49 (quoting Ex. 1007, 14:28–31). To the extent that the known technique of Petitioner's case is reflected implicitly in these assertions, we are not persuaded for the reasons set forth above in the context of Petitioner's argument that Bauman provides a teaching, suggestion, or motivation to make the proposed combination. Namely, Petitioner has not demonstrated that Bauman's segmenting of a global cache is an improvement in the manner alleged by Petitioner and as would be necessary to support Petitioner's "known technique" theory.

In its Reply, Petitioner argues that "both references use similar techniques to address the same problem: maintaining cache coherency in multiprocessor systems when multiple processors request access to

memory." Pet. Reply 3 (citations omitted); *see id.* at 4 (Arguing, after stating Bauman's purported teaching, "[s]imilarly, Kabemoto discloses a multiprocessor system that maintains cache coherence among second-level caches and employs mechanisms to improve performance of its coherence scheme."). Later in the Reply, Petitioner reiterates its position that, "[g]iven that both references teach the use of known techniques to improve similar devices in the same way—dividing caches into portions and maintaining separate coherence states for each portion that can be updated individually—a POSITA would have been motivated to combine their teachings." *Id.* at 10 (citations omitted); *but see* PO Resp. 19 ("Petitioner does not explain why POSITA would be motivated to replace Kabemoto's solution to the problem of cache coherency with Bauman's, or even that Bauman's solution is appropriate or beneficial for Kabemoto's particular system"). If, as Petitioner argues, Kabemoto already addresses its problem through the use of a known technique similar to that of Bauman's, we fail to see why one of ordinary skill in the art would regard Bauman's technique as an obvious improvement to Kabemoto.

5. Conclusion as to Petitioner's Challenge Based on Kabemoto, Bauman, and Chaney

Based on the foregoing, Petitioner has not established by a preponderance of the evidence that dependent claim 5 is unpatentable over the combination of Kabemoto, Bauman, and Chaney.

E. The Alleged Obviousness of Dependent Claim 5 over Wu, Bauman, and Chaney

Petitioner alleges that dependent claim 5 of the '908 patent would have been obvious over Wu, Bauman, and Chaney. *See* Pet. 96–101; *see also id.* at 63–96 (Petitioner's analysis of the limitations of underlying

independent claim 4). The parties' arguments regarding this ground, for the most part, are similar to those of the Kabemoto-based ground discussed above. In this ground, Petitioner relies on Wu, rather than Kabemoto, for disclosure of much of underlying independent claim 4, and, as it did for the Kabemoto-based ground, relies on Bauman for the recited "separated cache segment" aspect of independent claim 4 and on Chaney for the chronological access aspect of dependent claim 5. *See* Pet. 63–101.

Patent Owner's arguments again pertain to the limitation reciting "wherein the at least one separated cache comprises a separated cache segment for at least some of the plurality of processors" (identified as "element i") and the "interconnect system" limitation (identified as "element j"). *See* PO Resp. 34. Patent Owner argues that Petitioner has failed to establish that a person of ordinary skill in the art would have had a reason to combine Wu and Bauman for element i or j and that Petitioner's proposed combination of references would lack element j, the "interconnect system." *See, e.g.*, *id.*

For the reasons discussed below, we agree with Patent Owner that Petitioner has not shown that claim 5 would have been obvious over Wu, Bauman, and Chaney.

1. Wu (Ex. 1006)

Wu pertains to "an improved data processing system and, in particular, to a symmetric data processing system with unified process environment and distributed system functions." Ex. 1006, 1:20–24. Wu discloses symmetric multi-processing System 10 that includes Extended Architecture Multiple Processor (XA-MP) Bus 12, which interconnects a plurality of system functional units, which include one or more Processor Modules (PMs) 16. *Id.* at 2:62–3:4. Figure 20 of Wu is reproduced below.

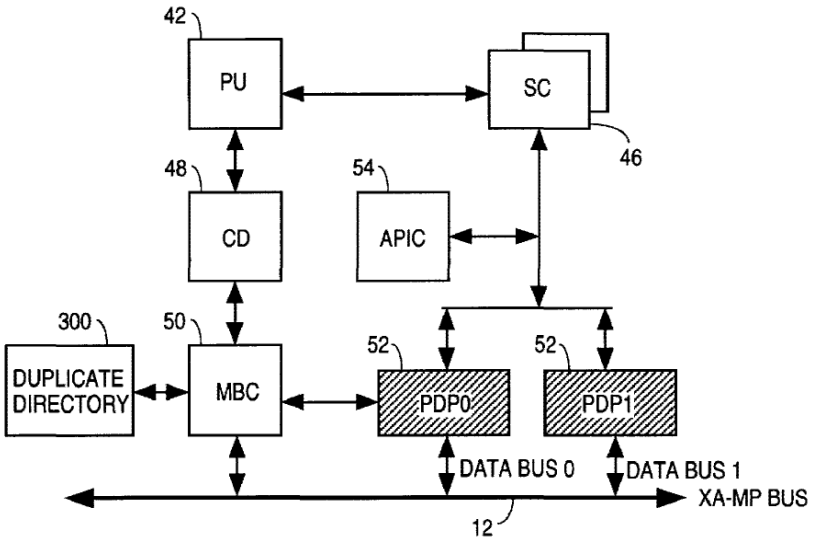
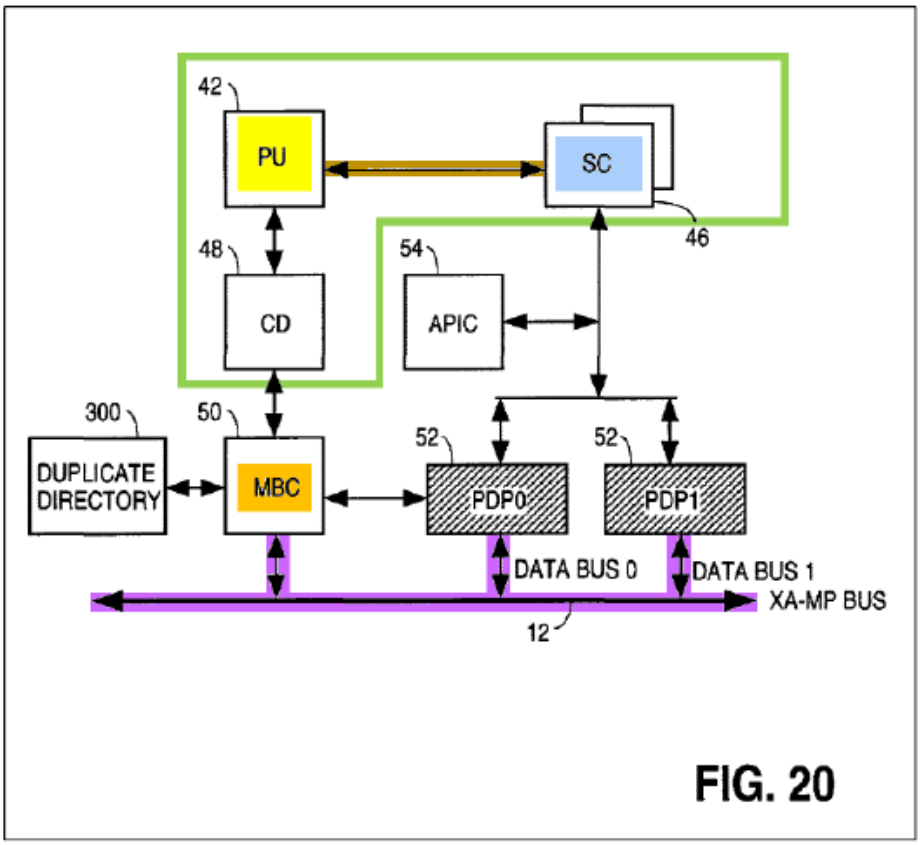


FIG. 20

Figure 20 is a block diagram of a processor functional unit and, specifically, depicts the "overall block diagram of a PM 16." *Id.* at 2:31, 29:49–50. A Processor Module 16 is "comprised of one or more Processor Units 42, each of which may have an internal, primary cache and an associated Cache Mechanism (CM) 44, each of which may in turn be comprised of a Secondary Cache (SC) 46 and a Cache Directory and Controller (CD) 48." *Id.* at 4:14–19. "There is a PM 16 bus interface control unit for each Processor Unit 42, represented as [a] Memory Bus Controller (MBC) 50." *Id.* at 4:19–21.

2. Analysis

Petitioner relies, in part, on Wu's Figure 20, reproduced below with Petitioner's annotations.



Pet. 87. The annotated figure above is Figure 20 of Wu, a block diagram of a processor functional unit, with a green line added to identify that which Petitioner contends is the claimed "processing system." *Id.* at 68; Ex. 1006, 2:31. The annotated Figure 20 depicts schematically Processor Unit (PU) 42 (yellow), Secondary Cache (SC) 46 (blue) (mapped by Petitioner to the recited "separated cache"), and a single line, in the form of a double headed arrow and highlighted in gold, connecting the Processor Unit and the Secondary Cache. *See* Pet. 86–87; Ex. 1006, 29:49–55. To address the claim recitation "a processing system comprising a plurality of processors," Petitioner relies on Wu's statement that, "[i]n the case of a PM 16, the operational elements are comprised of one or more Processor Units 42." Pet. 65 (quoting Ex. 1006, 4:14–15; citing *id.* at 29:40–30:5, Fig. 20). Building on this premise, Petitioner contends that each Processor Module 16

includes "its Processor Units ('plurality of processors') [and] secondary cache ('separated cache')." *Id.* at 74; *see also id.* at 76 ("Wu discloses a module ID (i.e., 'slice' number) of a Processor Module (PM 16), which contains one or more processors, a separated cache, and an interface."). Thus, Petitioner contends that Wu discloses a plurality of processors associated with a single separated cache. Petitioner further contends, "[a]s Wu further teaches, secondary cache (SC) 46 and Processing Units (PUs) 42 are connected by an interconnect system, namely, data paths" and that "[t]hese data paths" are shown in the annotated Figure 20 reproduced above. *Id.* at 86–87 (citing Ex. 1006, 29:40–30:5, Fig. 20). Thus, Petitioner refers to the single gold line in Figure 20 as a plurality of data paths.

Like the previous ground, Petitioner turns to Bauman for the aspect of the limitation pertaining to a cache segment for a plurality of processors. *Id.* at 78. Petitioner asserts that Bauman discloses a segmented cache, the global second-level cache (SLC), and that there is a segment for a plurality of processors. *Id.* at 78–83. According to Petitioner, "Bauman discloses 'a second-level cache that is shared between the processors where the second-level cache also has a separate instruction cache and operand cache," and that the second-level cache comprises separate cache segments. *Id.* at 78–79 (quoting Ex. 1007, 1:56–63).

Petitioner proposes the modification of Wu's system by the "use [of] Bauman's segmented global SLC as a secondary cache in Wu's Processor Module." *Id.* at 84.

a. The Interconnect System Limitation

Patent Owner argues that Petitioner's proposed combination would lack the required "interconnect system." PO Resp. 40–42; *see also id.* at 4. For the following reasons, we agree.

As mentioned above, Petitioner refers to the single gold line in its annotated Figure 20 as a plurality of data paths and as an interconnect system. Pet. 86–87. In a similar manner, Petitioner contends that a plurality of "[d]ata paths connecting secondary cache 46 to the one or more processor units 42 are shown in greater detail in Figure 21, reproduced below:"

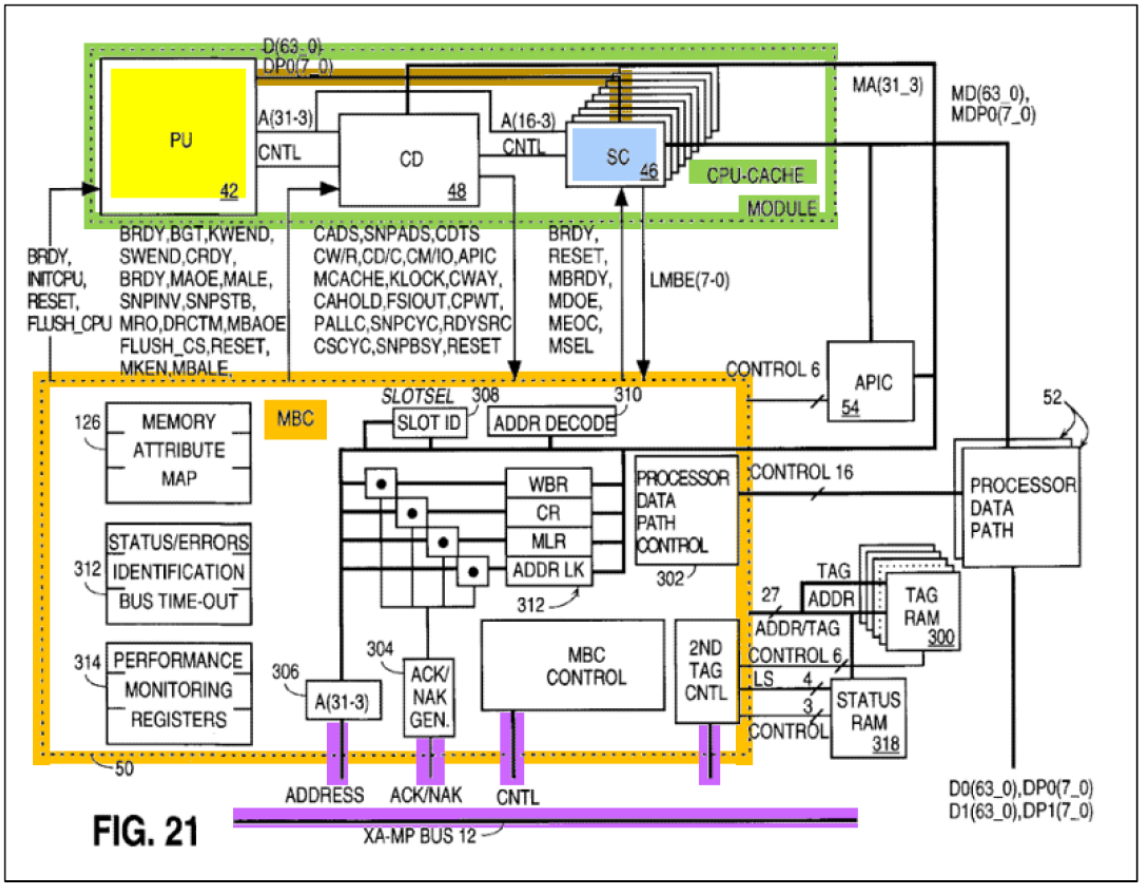


FIG. 21

Pet. 88. Above is Petitioner's annotated version of a block diagram of a memory bus controller. *See* Ex. 1006, 2:32. Petitioner argues that, "[a]s shown in Figure 21, within the 'CPU-Cache Module,' the one or more processor units 42 are directly connected to nine secondary caches 46 by nine 8-bit data paths (for a total of 64 bits, as indicated)." *Id.* at 88 (citing Ex. 1006, Fig. 21; Ex. 1003 ¶ 183). Petitioner further argues that a person of ordinary skill in the art "would have understood that Wu's data paths within

the 'CPU-Cache Module' interconnect the one or more processor units (PUs 42) with one or more secondary caches." *Id.* (citing Ex. 1003 ¶ 183).

Patent Owner disagrees with Petitioner's interpretation of Figure 21. Relying on the testimony of Dr. Annavaram, Patent Owner argues that "Wu's data paths only connect one Processing Unit 42 to one Secondary Cache 46—they do not connect processing units to neighboring processing units, or secondary caches to neighboring secondary caches." PO Resp. 41 (citing Ex. 2024 ¶ 75).

We find Patent Owner's position persuasive. Contrary to Petitioner's argument, we fail to discern, in the annotated Figure 21, nine paths between the yellow processor unit 42 (or a plurality thereof) and the blue secondary cache(s) 46. And, we find Petitioner's math that underlies that assertion questionable as it is unclear how 9 paths multiplied by 8 bits per path equals a total of 64 bits. Petitioner's expert, Dr. Mazumder, elaborates little on Petitioner's argument. Ex. 1003 ¶ 183 ("As can be seen [in Figure 21], there are nine data paths, connecting to nine secondary caches 46. . . . Additionally, each data path is 8 bits wide (indicated by 'DP0(7_0)' in gold), for a total of 64 bits (indicated by 'D(63_0)').").

In contrast, Patent Owner's expert, Dr. Annavaram, credibly testifies that "[t]he 'gold' colored line is just a data path between [a] processor and its associated local cache. It is not an interconnect to the rest of the processors." Ex. 2024 ¶ 74. In other words, there is a one-to-one relationship between a processor and a secondary cache, even when a plurality of processors are used. In support of the opinion, Dr. Annavaram walks through Wu's disclosure. *Id.* ¶ 75. Dr. Annavaram opines that Wu's statement that each Processor Module 16 may include "one or more

Processor Units 42, each of which may have an internal, primary cache," means that "each processor module (represented by the green box in Dr. Mazumder's annotated [Figure 21]) may include multiple Processor Units 42." *Id.* Dr. Annavaram, quoting from Wu, continues:

> Each Processor Unit 42 (and thus each processor) also has "an associated Cache Mechanism (CM) 44, each of which may in turn be comprised of a Secondary Cache (SC) 46 and a Cache Directory and Controller (CD) 48." [Ex. 1006,] 4:14-19. *Thus, each processor has its own secondary cache. Based on these descriptions, POSITA would understand that the data path shown in Figure 21 reflects that each processor (in the one or more Processor Units 42) is interconnected with its respective secondary cache.* There is no indication that any processor is connected to other processors' secondary caches, that any processor is connected to any other processor, or that any cache is connected to any other cache.

Id. (emphasis added).

We find Dr. Annavaram's testimony more credible than Dr. Mazumder's. Accordingly, we find that Wu—through its Figures 20 and 21 and through its textual description—discloses a single interconnection between a given processor and its associated second-level cache.

Thus, Wu is lacking, at least, an interconnect system having, as required by the claim, an interconnection between neighboring processors. Petitioner also has not shown how Wu teaches or suggests an interconnection between neighboring second-level *caches*. Further, because Wu's second-level caches are not segmented, Wu does not and could not teach or suggest the claim requirement of the interconnect system interconnecting neighboring *segments*.

In a similar fashion to the Kabemoto-based ground discussed above, Petitioner argues that Bauman discloses an interconnect system. *See* Pet. 89–90. And, as in the previous ground, Petitioner's proposed combination uses the purported interconnect system from the primary reference, not Bauman. For example, Petitioner argues that a person of ordinary skill in the art "would have been motivated to use Bauman's segmented global SLC [second-level cache] with Wu's data paths ('interconnect system') . . . ." *Id.* at 90 (citing Ex. 1003 ¶ 186); *see id.* ("A POSA would have further understood that Wu's data paths ('interconnect system') would maintain cache coherence . . . ."); *see also id.* at 83 (identifying the proposed modification as the "use [of] Bauman's segmented global SLC as a secondary cache in Wu's Processor Module").

Thus, even if, as Petitioner contends, Bauman teaches an interconnect system having the three relationships recited in the claim, Petitioner does not articulate adequately a proposed combination that utilizes that teaching. Petitioner does not explain adequately how Wu's data paths (the gold line) in the proposed combination is the claimed structure of an "interconnect system" having all of the three recited "interconnecting" relationships. Petitioner has failed to demonstrate that the proposed combination has the claimed "interconnect system."

b. Reason to Combine

Petitioner argues that a person of ordinary skill in the art "would have been motivated to use Bauman's segmented global SLC as a secondary cache in Wu's Processor Module for several reasons." Pet. 84. Petitioner identifies those reasons as: 1) "the combination of Wu and Bauman represents the use of known techniques to improve similar devices in the same way," 2) "Bauman provides a teaching, suggestion, or motivation to

combine the teachings of Wu and Bauman," and 3) "the combination of Wu and Bauman would have been a simple substitution for a [person of ordinary skill in the art] with predictable results." *Id.* at 84–86. We agree with Patent Owner's argument that Petitioner has failed to set forth an adequate reason why a person of ordinary skill in the art would have combined the references' teachings to arrive at the claimed subject matter. *See* PO Resp. 34.

(1) The "Known Technique" Rationale and Bauman's Alleged Teaching, Suggestion, or Motivation

Petitioner's "known techniques" rationale suffers from the same deficiencies as the prior ground. Petitioner repeats many of the same arguments from the Kabemoto-based ground. *Compare* Pet. 84–85, *with id.* at 48–49. Petitioner, for this Wu-based ground, again focuses on the purported similarities of the two references applied to the underlying independent claim but does not identify, in the "known techniques" section of the Petition, the relied-on technique. *See id.* at 84–85. In the Reply, Petitioner argues that the Wu and Bauman references address the same problem utilizing similar techniques. *See* Pet. Reply 19–20 (arguing that Patent Owner's assertion that the references use different techniques is incorrect). Petitioner does not explain how this is consistent with a rationale based on the use of a known technique to *improve* a similar device. *See KSR*, 550 U.S. at 401 ("[I]f a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond that person's skill.").

Petitioner's rationale premised on Bauman providing a teaching, suggestion, or motivation is almost identical with that of the previous

ground, substituting "Wu" for "Kabemoto." *Compare* Pet. 85, *with id.* at 49–50. For the same reasons given above, we find this rationale unpersuasive. Petitioner again argues that "[a]s Bauman teaches, segmenting the global cache 'simplifies maintaining cache coherency between the instruction and operand second-level caches,'" but fails to explain adequately a tie between the actual quote and the interpretation argued for Petitioner's modified version. *Id.* at 85 (citing Ex. 1007, 14:28–31); *see* PO Resp. 37–38 ("Petitioner repeats the same assertion from Ground I that 'Bauman teaches[] segmenting the global cache,' mischaracterizing Bauman's disclosure, which in fact teaches an advantage relating to Bauman's use of cache tags." (citing Ex. 2024 ¶ 67)).

(2) The "Simple Substitution" Rationale

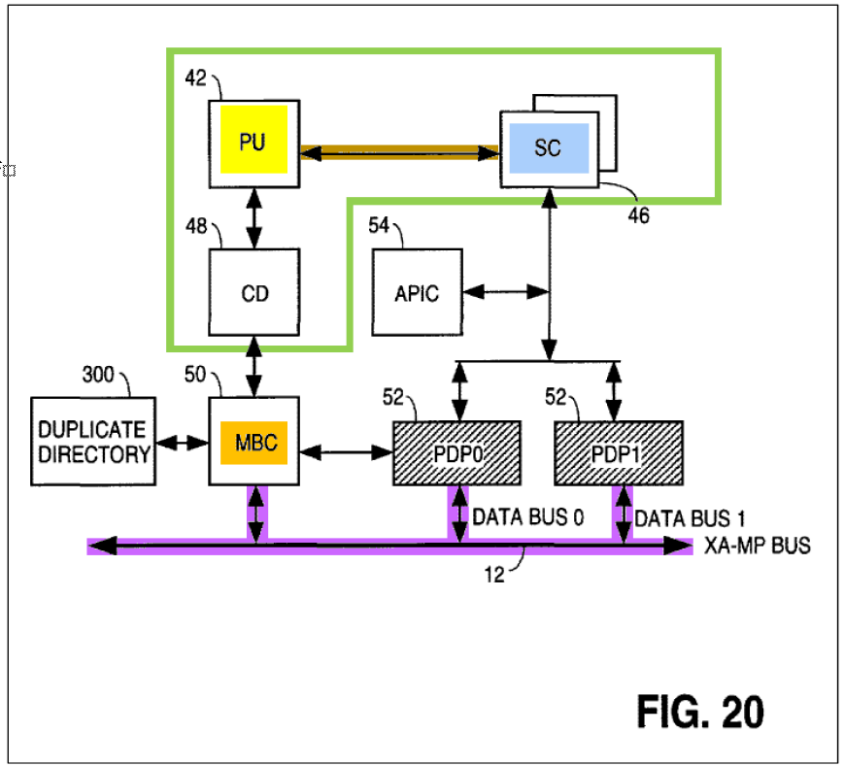
Petitioner also contends that the proposed combination of Wu's and Bauman's teachings would have been obvious as a simple substitution. Pet. 86. Petitioner argues that a person of ordinary skill in the art "would have easily substituted Wu's secondary cache 46 with Bauman's segmented global SLC because both caches are second-level caches within multiprocessor systems." *Id.* (citing Ex. 1003 ¶ 181).

Patent Owner argues that the simple substitution rationale is based on Petitioner's misinterpretation of Wu. *See* PO Resp. 38–40. According to Patent Owner, Petitioner is incorrect in asserting that Wu discloses a global cache provided for a plurality of processor units. *Id.* at 38 (citing Pet. 86). Patent Owner also argues that, "[b]ecause Wu's data paths do not provide the required interconnections of elements, simply replacing Wu's caches with Bauman's caches cannot cure this defect." *Id.* at 42.

We determine that Petitioner has not established that the proposed substitution is a simple one. To the contrary, Petitioner's proposed

modification is relatively complex. Petitioner begins with the assertion that "Wu discloses one or more Processing Units 42 ('processor') and a secondary cache 46 ('separated cache')." Pet. 86. Thus, as discussed further below, it appears that Petitioner contends that Wu discloses a plurality of processors associated with a single secondary cache.

Petitioner's modification is articulated, in part, by the use of an annotated version of Wu's Figure 20, reproduced again below.



Pet. 87. The annotated figure above is Figure 20 of Wu, a block diagram of a processor functional unit, with a green line added to identify that which Petitioner contends is the claimed "processing system." *Id.* at 68; Ex. 1006, 2:31. Petitioner contends that a plurality of "data paths" is shown in gold in the figure above. *See* Pet. 86.

Petitioner also contends that a plurality of "[d]ata paths connecting secondary cache 46 to the one or more processor units 42 are shown in greater detail in Figure 21, reproduced below:"

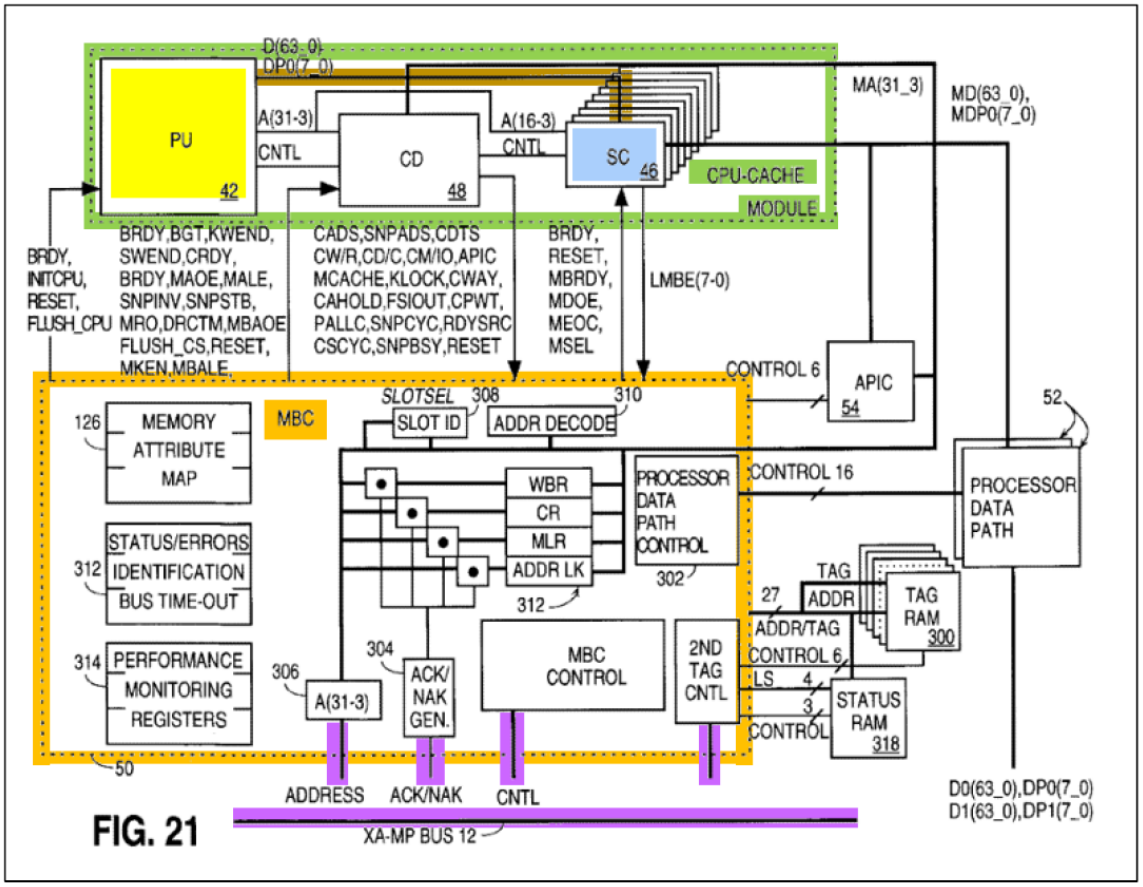


FIG. 21

Pet. 88. Above is Petitioner's annotated version of Wu's Figure 21, a block diagram of a memory bus controller. *See* Ex. 1006, 2:32.

The challenged claim is directed to a configuration where, *inter alia*, multiple processers are interconnected together and where those plural processors have access to a given segment of the separate cache. *See* Ex. 1001, 52:63–53:3. Figure 20 depicts a single processing unit (PU), secondary cache(s) (SC), and a single gold-highlighted line between those components. Similarly, Figure 21 depicts a single processing unit, secondary cache(s), and a single gold-highlighted line between them.

Simply substituting a segmented cache for each of Wu's second-level caches will not yield the recited segment-to-plural-processors configuration or the claimed three relationships of the "interconnect system." Petitioner addresses this gap, to some degree, by leveraging Wu's statement that one or more processors may be used in the processing system. *See, e.g.*, Pet. 64–66 (citing Ex. 1006, 2:67–3:6, 4:14–15, 29:40–30:5, Figs. 1, 20, 21); *id.* at 78. The description specific to Figure 20 provides:

> Referring to FIG. 20, therein is present an overall block diagram of a PM 16, as shown, and as discussed previously, *each PM 16 includes a Processing Unit 42* which includes a primary cache supporting data and instruction reads and writes for the Processing Unit 42 *in association with Secondary Cache Mechanism 46* and a Secondary Cache Directory 48 for support of direct Processor Unit 42 operations.

Ex. 1006, 29:49–55 (emphasis added). Thus, Wu describes a single processing unit in association with a secondary cache. The description specific to Figure 21 does not change this understanding. *See id.* at 30:6–19. Patent Owner's expert's credible testimony confirms this. Ex. 2024 ¶¶ 74–75.

Petitioner's proposed combination appears to be premised on Wu having a plurality of processors and a single associated secondary cache and a plurality of paths therebetween. *See, e.g.*, Pet. 86 ("Within each Processor Module 16, Wu discloses one or more Processing Units 42 ('processor') and a secondary cache 46 ('separated cache'). . . . As Wu further teaches, *secondary cache (SC) 46 and Processing Units (PUs) 42 are connected by an interconnect system*, namely, data paths." (emphasis added)). In terms of Figures 20 and 21 shown above, that would entail adding more yellow processing unit boxes, retaining the quantity of blue secondary cache(s), and adding gold connecting lines (or interpreting the single line as a plurality of

paths). It is only then that Petitioner's proposed "simple substitution" of Bauman's segmented second-level cache for Wu's secondary cache is applied. Then, one would have to adjust Wu's gold path(s) from the depicted single-line, one-to-one relationship to a multi-path configuration having the three relationships of the claimed interconnect system. Those claimed relationships require that particular structure—"an interconnect system"—where: 1) each cache segment is connected to each of the plurality of processors, 2) each processor is connected to its neighboring processor, and 3) each segment is connected to its neighboring segment. Ex. 1001, 52:66–53:3. We find that Petitioner's proposed combination is not the result of a substitution that merely is simple.

Petitioner replies to Patent Owner's argument that each Processing Unit of Wu has a respective secondary cache that is connected by a single data path. Pet. Reply 21–22. Petitioner asserts that Patent Owner's expert "admitted that each processor module contains one or more PUs [(processing units)] and 'multiple . . . secondary caches,' and that the multiple SCs (46) in Figure 21 suggests there may be additional Processor Units 42." *Id.* at 22 (citing Ex. 1047, 101:11–22; Ex. 2024 ¶ 75; Ex. 1003 ¶¶ 174, 181). Petitioner then argues that, "[t]hus, Figure 21's 'single data path'—as [Patent Owner] PACT identifies—is consistent with a shared bus connecting the processors and caches." *Id.* at 23. We do not find this helpful or dispositive. The purported admission is not inconsistent with Patent Owner's expert's opinion that Wu discloses a one-to-one relationship. And, even if Wu is describing a plurality of processors and a plurality of caches and a plurality of data paths in the form of a shared bus, Petitioner

has not established adequately whether or how all the components are interconnected as claimed.

Petitioner's proposed modification requires not merely the substitution of a segmented cache for a non-segmented one, but also the substitution of the claimed interconnect system for Wu's data path. Petitioner's arguments and evidence do not demonstrate that such substitutions would be simple.

3. Conclusion as to Petitioner's Challenge Based on Wu, Bauman, and Chaney

Based on the foregoing, Petitioner has not established by a preponderance of the evidence that dependent claim 5 is unpatentable over the combination of Wu, Bauman, and Chaney.

III. CONCLUSION

After reviewing the record developed during trial anew, we determine that Petitioner has not demonstrated by a preponderance of the evidence that claim 5 of the '908 patent is unpatentable over Kabemoto, Bauman, and Chaney, or is unpatentable over Wu, Bauman, and Chaney.

In summary:

Claims	**35 U.S.C. §**	**Reference(s)/Basis**	**Claims Shown Unpatentable**	**Claims Not Shown Unpatentable**
5	103(a)	Kabemoto, Bauman, Chaney		5
5	103(a)	Wu, Bauman, Chaney		5
Overall Outcome				5

IV. ORDER

For the foregoing reasons, it is hereby:

ORDERED that claim 5 of the '908 patent has *not* been proven to be unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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