# EXHIBIT 5-A

## U.S. Patent No. 7,503,026 to Ichiryu

U.S. Patent No. 7,503,026 to Ichiryu (hereinafter "Ichiryu") anticipates and/or renders obvious, at least under Tela's apparent infringement theories, all claims of U.S. Patent No. 7,948,012 under 35 U.S.C. §§ 102, 103. Ichiryu was filed on December 19, 2005, published on March 10, 2009, and is therefore prior art to the '012 patent.

Nothing stated in this chart shall be treated as an admission or suggestion that Respondent agrees with Tela regarding either the scope of any of the asserted claims or the claim constructions advanced by Tela in its infringement contentions, or that Respondent's accused products meet any limitations of the claims.

The chart below provides representative examples of where each element of each claim is found within Ichiryu, at least under Tela's apparent construction of the claims as applied in Tela's infringement contentions. The cited evidence is merely illustrative, and Respondent reserves the right to cite alternative or additional evidence.

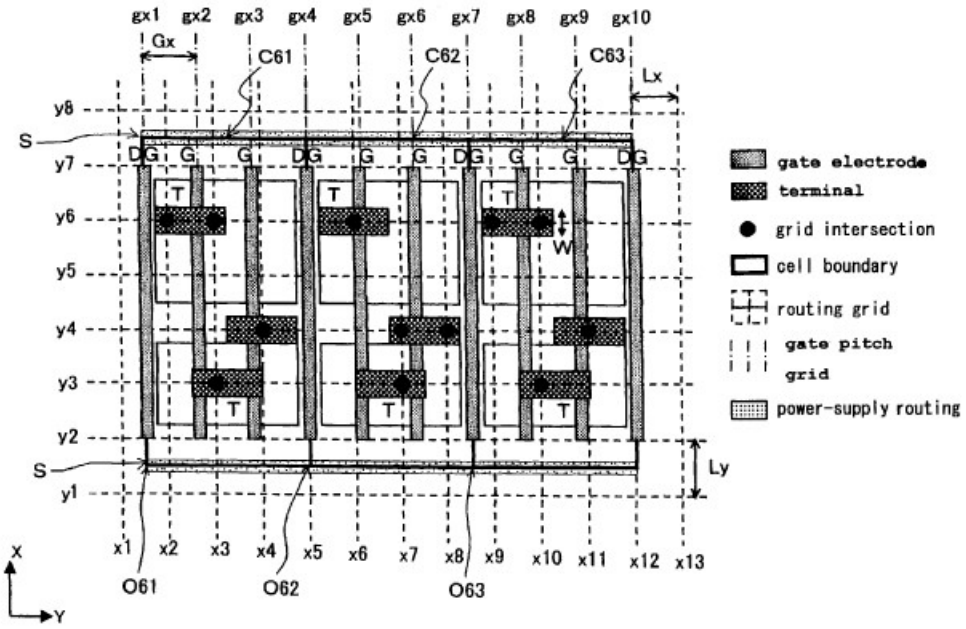
To the extent that Tela contends that Ichiryu does not disclose one or more limitations of the claims, it would have been obvious to combine the teachings of Ichiryu with: (1) the knowledge of one of ordinary skill in the art to show all the limitations of the claims; (2) the teachings of the prior art references set forth in Respondent's other invalidity charts with respect to the one or more limitations; and/or (3) the teachings of any of the prior art references set forth in the cover document of Respondent's invalidity contentions, as cited below for the one or more limitations.

Because Tela has yet to identify any limitation of the asserted claims that it contends is not fully disclosed by Ichiryu, either alone or in combination with other prior art cited by Respondent, Respondent expressly reserves the right to rebut any such contention, including by identifying additional obviousness combinations, if any such contention is made by Tela.

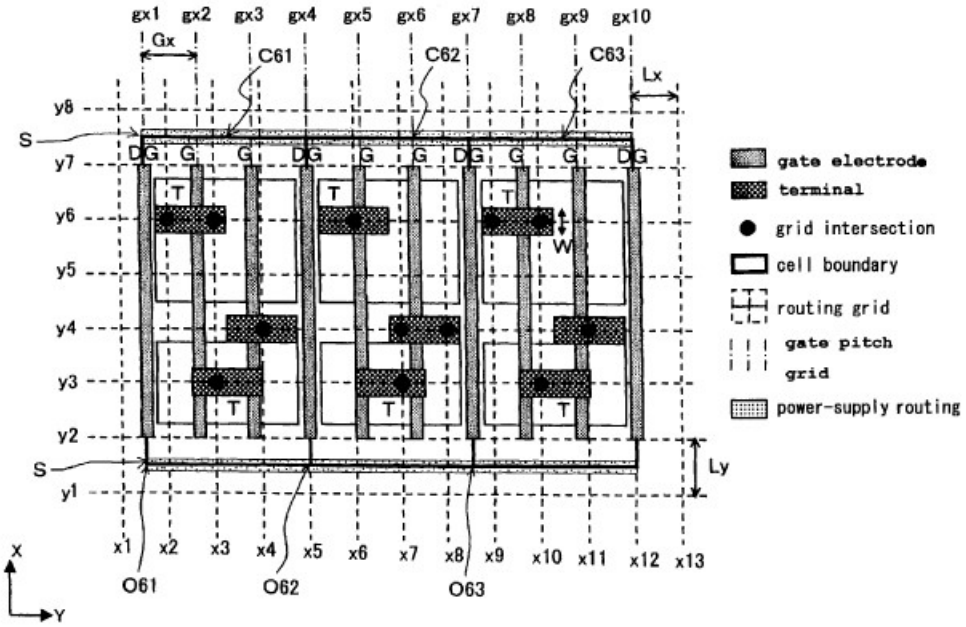
Where the chart below states that Ichiryu "discloses" a limitation, such disclosure may be express or inherent.

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| 2. An integrated circuit device, comprising: | At least under Tela’s apparent infringement theory, Ichiryu discloses and/or renders obvious an integrated circuit device.<br><br>Ichiryu describes the layout of a “semiconductor integrated circuit.” The mapping of this element is the same for Figure 11 and for Modified Fig. 11M.<br><br>*See, e.g.*:<br><br>“A cell according to the present invention comprises a plurality of terminals capable of transmitting an input signal or an output signal and serving as a minimum unit in designing a semiconductor integrated circuit….” (Ichiryu at Abstract).<br><br>“The present invention relates to a standard cell, a standard cell library and a placement method of standard cells for higher integration and area reduction.” (Ichiryu at 1:9-11).<br><br>“When the precision in the finished dimension of the gate electrode is deteriorated, performances of respective transistors of the semiconductor integrated circuit are increasingly inconstant, which leads to an increased variation in a performance of the semiconductor integrate[d] circuit.” (Ichiryu at 2:27-32).<br><br>“[A]s recited in No. H10-32253 of the Publication of the Unexamined Japanese Patent Applications, the interval and the length of the gate electrodes in each standard cell are set regular so that the OPC is processed per standard cell in the conventional technology.” (Ichiryu at 2:37-41).<br><br>“Therefore, a main object of the present invention is to provide a semiconductor integrated circuit capable of reducing a cell area and a chip area. Another main object of the present invention is to provide a semiconductor integrated circuit capable of improving a precision in a finished dimension of a gate electrode despite a process miniaturization and processing the OPC in each standard cell.” (Ichiryu at 3:43-50). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “[A] standard cell according to the present invention is a cell…serving as a minimum unit in designing the semiconductor integrated circuit….” (Ichiryu at 3:51-55).<br><br>“[A]n occupied area in the design of the semiconductor integrated circuit can be reflected on the area of the logic part, which results in the reduction of the chip area.” (Ichiryu at 5:35-38).<br><br>“In the present invention, the semiconductor integrated circuit may comprise the foregoing standard cell. Then, the semiconductor integrated circuit capable of reducing the chip area, improving the precision in the finished dimension of the gate electrodes and processing the OPC in each standard cell can be obtained.” (Ichiryu at 7:58-63).<br><br>“FIG. 1 also shows a part of the semiconductor integrated circuit designed using the cell described in the embodiment 1. It is needless to say that the area of the integrated circuit can be reduced when the cell described above is used.” (Ichiryu at 10:48-51). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | F I G. 11<br>  <br><br>(Ichiryu Fig. 11).<br>*See also* Ichiryu Figs. 1-10, 12-18.<br>This limitation also would have been obvious to a person of ordinary skill in the art based on (1) Ichiryu alone; and/or (2) the teachings with respect to this claim element as detailed in the cover document of Respondent’s invalidity contentions and Respondent’s other invalidity charts. |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| [2.1] a substrate region that forms part of an overall substrate of the integrated circuit device, | At least under Tela’s apparent infringement theory, Ichiryu discloses and/or renders obvious a substrate region that forms part of an overall substrate of the integrated circuit device.<br><br>Ichiryu discloses a “substrate on which [a] cell is mounted.” The mapping of this element is the same for Figure 11 and for Modified Fig. 11M.<br><br>*See*, *e.g.*:<br><br>“4. A semiconductor integrated circuit comprising the cell as claimed in claim 1 and a circuit substrate on which the cell is mounted.” (Ichiryu at Claim 4).<br><br>“8. A semiconductor integrated circuit comprising the cell as claimed in claim 5 and a circuit substrate on which the cell is mounted.” (Ichiryu at Claim 8).<br><br>“12. A semiconductor integrated circuit comprising the cell as claimed in claim 9 and a circuit substrate on which the cell is mounted.” (Ichiryu at Claim 12).<br><br>“16. A semiconductor integrated circuit comprising the cell as claimed in claim 13 and a circuit substrate on which the cell is mounted.” (Ichiryu at Claim 16).<br><br>“23. A semiconductor integrated circuit comprising the standard cell as claimed in claim 21 and a circuit substrate on which the standard cell is mounted.” (Ichiryu at Claim 23).<br><br>“26. A semiconductor integrated circuit comprising the standard cell as claimed in claim 24 and a circuit substrate on which the standard cell is mounted.” (Ichiryu at Claim 26).<br><br>“29. A semiconductor integrated circuit comprising the standard cell as claimed in claim 27 and a circuit substrate on which the standard cell is mounted.” (Ichiryu at Claim 29).<br><br>“32. A semiconductor integrated circuit comprising the standard cell as claimed in claim 30 and a circuit substrate on which the standard cell is mounted.” (Ichiryu at Claim 32). |

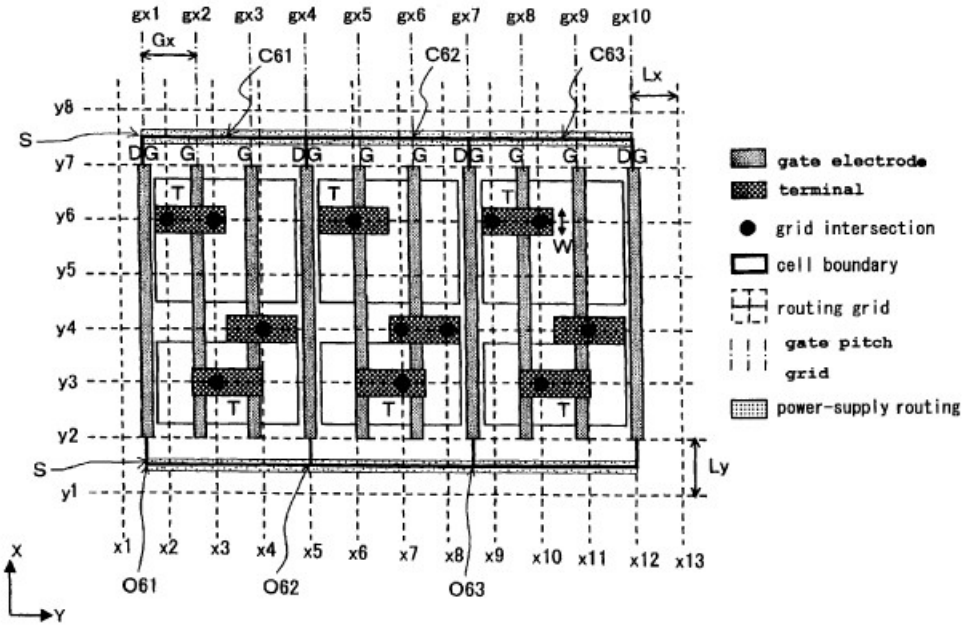
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | F I G. 11<br>  <br><br>(Ichiryu Fig. 11).<br>*See also* Ichiryu Figs. 1, 3, 8, 13, 14, 17, 18. |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | This limitation also would have been obvious to a person of ordinary skill in the art based on (1) Ichiryu alone; and/or (2) the teachings with respect to this claim element as detailed in the cover document of Respondent’s invalidity contentions and Respondent’s other invalidity charts. |
| [2.2] a gate electrode level region that forms part of an overall gate electrode level of the integrated circuit device, the gate electrode level region formed above and over the substrate region, wherein the gate electrode level region corresponds to a circular area having a radius of up to about 1965 nanometers and oriented substantially parallel to the substrate region, | At least under Tela’s apparent infringement theory, Ichiryu discloses and/or renders obvious a gate electrode level region that forms part of an overall gate electrode level of the integrated circuit device, the gate electrode level region formed above and over the substrate region, wherein the gate electrode level region corresponds to a circular area having “a radius of up to about 1965 nanometers” and oriented substantially parallel to the substrate region.<br><br>Ichiryu describes layout techniques for gate electrodes in a gate electrode region. Under Tela’s apparent infringement theory, Ichiryu has a gate electrode level region that corresponds to an area with “a radius of up to about 1965 nanometers.” The mapping of this element is the same for Figure 11 and for Modified Fig. 11M.<br><br>*See, e.g.*:<br><br>“[A]s the miniaturization of the process [continues], a precision in a finished dimension of the gate electrode ultimately obtained is deteriorated by an optical proximity effect when an interval between the gate electrodes and gate lengths of the gate electrodes are irregular in their patterns. When the precision in the finished dimension of the gate electrode is deteriorated, performances of respective transistors of the semiconductor integrated circuit are increasingly inconstant, which leads to an increased variation in a performance of the semiconductor integrate[d] circuit.” (Ichiryu at 2:23-32).<br><br>“[A]s recited in No. H10-32253 of the Publication of the Unexamined Japanese Patent Applications, the interval and the length of the gate electrodes in each standard cell are set regular so that the OPC is processed per standard cell in the conventional technology.” (Ichiryu at 2:37-41).<br><br>“The standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes….” (Ichiryu at 6:20-21). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “A standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes, wherein gate pitches of some of the gate electrodes are set to values different to the routing grid interval set along the X direction in parallel with the power-supply wiring of the standard cell, and a cell width along the X direction in parallel with the power-supply wiring of the standard cell is set to an integral multiple of a minimum value of the gate pitches of the gate electrodes set to the values different to the routing grid interval set along the X direction.” (Ichiryu at 6:26-35).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, a precision in a finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:41-45).<br><br>“A standard cell according to the present invention comprises a plurality of gate electrodes and a plurality of dummy gate electrodes, wherein a cell width in the X direction in parallel with the power-supply wiring of the standard cell is an integral multiple of a minimum gate pitch of gate pitches of the gate electrodes and the dummy gate electrodes different to the routing grid interval along the X direction.” (Ichiryu at 6:46-52).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:58-62).<br><br>“The gate pitches of the standard cell are all preferably equal. Thereby, the pattern of the gate electrodes can impart a perfect regularity to the gate pitches, and the precision in the finished dimension of the gate electrodes can be further improved.” (Ichiryu at 6:66-7:3).<br><br>“Further, because the pattern of the gate electrodes can have the regularity, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be performed in each standard cell.” (Ichiryu at 8:21-24). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “Referring to reference symbols in FIG. 11, x1-x13 denote routing grids for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, y1-y8 denote routing grids disposed in parallel with the X direction and adjacent to one another in the Y direction, gx1-gx10 denote grids of gate pitches for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, C61, C62 and C63 are standard cells, O61, O62 and O63 are respective origins of the standard cells C61, C62 and C63, … G denotes a gate electrode, and DG denotes a dummy gate electrode.” (Ichiryu at 14:32-44).<br><br>“In the standard cells C61, C62 and C63, gate lengths and gate intervals of the gate electrode G and dummy gate electrode DG are constant, and a cell width of the standard cells C61, C62 and C63 in the X direction is an integral multiple of a minimum value of a gate pitch Gx (value of gate pitch=gate length+gate interval) (In FIG. 11, the cell width of the standard cells C61, C62 and C63 is three times as wide as Gx).” (Ichiryu at 14:45-51).<br><br>“Not only inside the respective standard cells C61, C62 and C63, but also among the standard cells C61, C62 and C63 to one another, the gate lengths and the gate intervals are equal in the patterns of the gate electrodes and the dummy gate electrodes.” (Ichiryu at 15:47-51).<br><br>“In the embodiment 5, the gate lengths are all equal in the gate electrodes and the dummy gate electrodes….” (Ichiryu at 16:10-11).<br><br>“In FIG. 14, a reference symbol C81 denotes a standard cell. The standard cell C81 comprises gate electrodes G, dummy gate electrodes DG and two gate electrodes G2 having a gate length different to those of the gate electrode G and the dummy gate electrode DG, wherein a width of the gate electrode G2 is set so that a cell width of the standard cell C81 in the X direction is an integral multiple of the gate pitch Gx. In FIG. 14, the cell width of the standard cell C81 is nine times as wide as the gate pitch Gx. The width of the gate electrode G2 is thus set because a processing speed is expected to be faster when the cell width of each cell in the X direction is the integral multiple of the gate pitch Gx than when the cell width of each cell takes an arbitrary value in the placement using the |

| '012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | conventional automatic placement & routing tool. However, the width of the gate electrode G2 is not necessarily set in the foregoing manner." (Ichiryu at 16:15-30).<br><br>"As described, in the case of including the standard cell comprising the gate electrodes having the different gate lengths…." (Ichiryu at 16:32-34).<br><br>"In the constitution, the distance from the cell boundary of each standard cell to the gate electrode in the closest vicinity and the distance from the cell boundary of another standard cell adjacent thereto to the gate electrode in the closest vicinity are constant." (Ichiryu at 16:65-17:2).<br><br>"For example, a distance from each of the cell boundary of the standard cells C61, C62 and C63 to the gate electrode in the X direction is 'Gx-gate length/2' and constant even in the constitution shown in FIG. 11 where the dummy gate electrodes DG are not provided. A distance between a transistor disposed at the end of each standard cell and the gate electrode G of the adjacent standard cell is '2Gx-gate length' and constant. For example, even in the case where the dummy gate electrode DG is not provided in the constitution described referring to FIG. 11, the distance from each of the cell boundary of the respective standard cells C61, C62 and C63 to the gate electrode G located at the end of each of the standard cells in the X direction is constant at (Gx-gate length/2). Further, the distance from the gate electrode G located at the end of each of the standard cells to the gate electrode G located at the end of each of adjacent standard cells in the X direction is constant at (2Gx-gate length)." (Ichiryu at 17:6-22).<br><br>"Further, in the embodiment 6, the standard cells described in the embodiments 1 and 5 are used. The gate lengths and the gate intervals are thereby equal in the patterns of the gate electrodes of the placed standard cells C91, C92 and C93, which leads to the improvement of the precision in the finished dimension of the gate electrodes. The improvement of the precision in the finished dimension of the gate electrodes can be realized not only inside each of the standard cells C91, C92 and C93 but also between the standard cells." (Ichiryu at 18:1-9). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “[W]hen the standard cells are adjacently located, the gate lengths and the gate intervals in the patterns of the gate electrodes and the dummy gate electrodes are the same as when they are located alone.” (Ichiryu at 18:10-13).<br><br>F I G. 11<br><br>  <br><br><br>(Ichiryu Fig. 11).<br><br>*See also* Ichiryu at Figs. 1, 2, 3, 8, 12, 13, 14. |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | Ichiryu describes layout techniques for gate electrodes being placed apart with equal pitch, and one of Ichiryu’s stated goals is to decrease the surface area covered by the gates.<br><br>*See, e.g.*:<br><br>“[A] main object of the present invention is to provide a semiconductor integrated circuit capable of reducing a cell area and a chip area.” (Ichiryu at 3:43-45).<br><br>“Another main object of the present invention is to provide a semiconductor integrated circuit capable of improving a precision in a finished dimension of a gate electrode despite a process miniaturization….” (Ichiryu at 3:46-49).<br><br>“A standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes, wherein gate pitches of some of the gate electrodes are set to values different to the routing grid interval set along the X direction in parallel with the power-supply wiring of the standard cell, and a cell width along the X direction in parallel with the power-supply wiring of the standard cell is set to an integral multiple of a minimum value of the gate pitches of the gate electrodes set to the values different to the routing grid interval set along the X direction.” (Ichiryu at 6:26-35).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, a precision in a finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:41-45).<br><br>“A standard cell according to the present invention comprises a plurality of gate electrodes and a plurality of dummy gate electrodes, wherein a cell width in the X direction in parallel with the power-supply wiring of the standard cell is an integral multiple of a minimum gate pitch of gate pitches of the gate electrodes and the dummy gate electrodes different to the routing grid interval along the X direction.” (Ichiryu at 6:46-52). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:58-62).<br><br>“The gate pitches of the standard cell are all preferably equal. Thereby, the pattern of the gate electrodes can impart a perfect regularity to the gate pitches, and the precision in the finished dimension of the gate electrodes can be further improved.” (Ichiryu at 6:66-7:3).<br><br>“Further, because the pattern of the gate electrodes can have the regularity, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be performed in each standard cell.” (Ichiryu at 8:21-24).<br><br>“Referring to reference symbols in FIG. 11, x1-x13 denote routing grids for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, y1-y8 denote routing grids disposed in parallel with the X direction and adjacent to one another in the Y direction, gx1-gx10 denote grids of gate pitches for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, C61, C62 and C63 are standard cells, O61, O62 and O63 are respective origins of the standard cells C61, C62 and C63, … G denotes a gate electrode, and DG denotes a dummy gate electrode.” (Ichiryu at 14:32-44).<br><br>“In the standard cells C61, C62 and C63, gate lengths and gate intervals of the gate electrode G and dummy gate electrode DG are constant, and a cell width of the standard cells C61, C62 and C63 in the X direction is an integral multiple of a minimum value of a gate pitch Gx (value of gate pitch=gate length+gate interval) (In FIG. 11, the cell width of the standard cells C61, C62 and C63 is three times as wide as Gx).” (Ichiryu at 14:45-51).<br><br>“Not only inside the respective standard cells C61, C62 and C63, but also among the standard cells C61, C62 and C63 to one another, the gate lengths and the gate intervals are equal in the patterns of the gate electrodes and the dummy gate electrodes.” (Ichiryu at 15:47-51). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “In the embodiment 5, the gate lengths are all equal in the gate electrodes and the dummy gate electrodes….” (Ichiryu at 16:10-11).<br><br>“In FIG. 14, a reference symbol C81 denotes a standard cell. The standard cell C81 comprises gate electrodes G, dummy gate electrodes DG and two gate electrodes G2 having a gate length different to those of the gate electrode G and the dummy gate electrode DG, wherein a width of the gate electrode G2 is set so that a cell width of the standard cell C81 in the X direction is an integral multiple of the gate pitch Gx. In FIG. 14, the cell width of the standard cell C81 is nine times as wide as the gate pitch Gx. The width of the gate electrode G2 is thus set because a processing speed is expected to be faster when the cell width of each cell in the X direction is the integral multiple of the gate pitch Gx than when the cell width of each cell takes an arbitrary value in the placement using the conventional automatic placement & routing tool. However, the width of the gate electrode G2 is not necessarily set in the foregoing manner.” (Ichiryu at 16:15-30).<br><br>“In the constitution, the distance from the cell boundary of each standard cell to the gate electrode in the closest vicinity and the distance from the cell boundary of another standard cell adjacent thereto to the gate electrode in the closest vicinity are constant.” (Ichiryu at 16:65-17:2).<br><br>“For example, a distance from each of the cell boundary of the standard cells C61, C62 and C63 to the gate electrode in the X direction is ‘Gx-gate length/2’ and constant even in the constitution shown in FIG. 11 where the dummy gate electrodes DG are not provided. A distance between a transistor disposed at the end of each standard cell and the gate electrode G of the adjacent standard cell is ‘2Gx-gate length’ and constant. For example, even in the case where the dummy gate electrode DG is not provided in the constitution described referring to FIG. 11, the distance from each of the cell boundary of the respective standard cells C61, C62 and C63 to the gate electrode G located at the end of each of the standard cells in the X direction is constant at (Gx-gate length/2). Further, the distance from the gate electrode G located at the end of each of the standard cells to the gate electrode G located at the end of each of adjacent standard cells in the X direction is constant at (2Gx-gate length).” (Ichiryu at 17:6-22). |

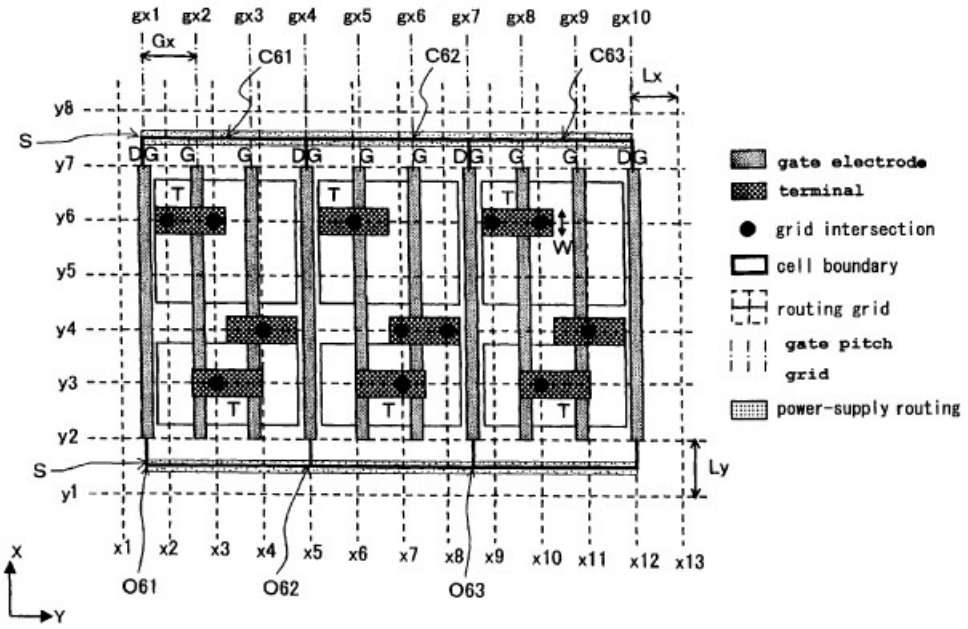
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “Further, in the embodiment 6, the standard cells described in the embodiments 1 and 5 are used. The gate lengths and the gate intervals are thereby equal in the patterns of the gate electrodes of the placed standard cells C91, C92 and C93, which leads to the improvement of the precision in the finished dimension of the gate electrodes. The improvement of the precision in the finished dimension of the gate electrodes can be realized not only inside each of the standard cells C91, C92 and C93 but also between the standard cells.” (Ichiryu at 18:1-9).<br><br>“[W]hen the standard cells are adjacently located, the gate lengths and the gate intervals in the patterns of the gate electrodes and the dummy gate electrodes are the same as when they are located alone.” (Ichiryu at 18:10-13).<br><br>This limitation also would have been obvious to a person of ordinary skill in the art based on (1) Ichiryu alone; and/or (2) the teachings with respect to this claim element as detailed in the cover document of Respondent’s invalidity contentions and Respondent’s other invalidity charts. |
| [2.3a] wherein the gate electrode level region includes a plurality of linear conductive segments each formed to have a respective length and a respective width as measured parallel to the substrate region, wherein a size of the length of a given linear conductive segment is greater than or equal to a size of the width of the given linear conductive segment, | At least under Tela’s apparent infringement theory, Ichiryu discloses and/or renders obvious wherein the gate electrode level region includes a plurality of linear conductive segments each formed to have a respective length and a respective width as measured parallel to the substrate region, wherein a size of the length of a given linear conductive segment is greater than or equal to a size of the width of the given linear conductive segment.<br><br>Ichiryu describes layout techniques for gate electrodes, which are linear conductive segments, including placing them such that they extend in parallel with a length greater than a width. The mapping of this element is the same for Figure 11 and for Modified Fig. 11M.<br><br>*See, e.g.*:<br><br>“[A]s the miniaturization of the process [continues], a precision in a finished dimension of the gate electrode ultimately obtained is deteriorated by an optical proximity effect when an interval between the gate electrodes and gate lengths of the gate electrodes are irregular in their patterns. When the precision in the finished dimension of the gate electrode is deteriorated, performances of respective |

| '012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | transistors of the semiconductor integrated circuit are increasingly inconstant, which leads to an increased variation in a performance of the semiconductor integrate[d] circuit." (Ichiryu at 2:23-32).<br><br>"[A]s recited in No. H10-32253 of the Publication of the Unexamined Japanese Patent Applications, the interval and the length of the gate electrodes in each standard cell are set regular so that the OPC is processed per standard cell in the conventional technology." (Ichiryu at 2:37-41).<br><br>"The standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes…." (Ichiryu at 6:20-21).<br><br>"A standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes, wherein gate pitches of some of the gate electrodes are set to values different to the routing grid interval set along the X direction in parallel with the power-supply wiring of the standard cell, and a cell width along the X direction in parallel with the power-supply wiring of the standard cell is set to an integral multiple of a minimum value of the gate pitches of the gate electrodes set to the values different to the routing grid interval set along the X direction." (Ichiryu at 6:26-35).<br><br>"[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, a precision in a finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell." (Ichiryu at 6:41-45).<br><br>"A standard cell according to the present invention comprises a plurality of gate electrodes and a plurality of dummy gate electrodes, wherein a cell width in the X direction in parallel with the power-supply wiring of the standard cell is an integral multiple of a minimum gate pitch of gate pitches of the gate electrodes and the dummy gate electrodes different to the routing grid interval along the X direction." (Ichiryu at 6:46-52). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:58-62).<br><br>“The gate pitches of the standard cell are all preferably equal. Thereby, the pattern of the gate electrodes can impart a perfect regularity to the gate pitches, and the precision in the finished dimension of the gate electrodes can be further improved.” (Ichiryu at 6:66-7:3).<br><br>“Further, because the pattern of the gate electrodes can have the regularity, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be performed in each standard cell.” (Ichiryu at 8:21-24).<br><br>“Referring to reference symbols in FIG. 11, x1-x13 denote routing grids for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, y1-y8 denote routing grids disposed in parallel with the X direction and adjacent to one another in the Y direction, gx1-gx10 denote grids of gate pitches for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, C61, C62 and C63 are standard cells, O61, O62 and O63 are respective origins of the standard cells C61, C62 and C63, … G denotes a gate electrode, and DG denotes a dummy gate electrode.” (Ichiryu at 14:32-44).<br><br>“In the standard cells C61, C62 and C63, gate lengths and gate intervals of the gate electrode G and dummy gate electrode DG are constant, and a cell width of the standard cells C61, C62 and C63 in the X direction is an integral multiple of a minimum value of a gate pitch Gx (value of gate pitch=gate length+gate interval) (In FIG. 11, the cell width of the standard cells C61, C62 and C63 is three times as wide as Gx).” (Ichiryu at 14:45-51).<br><br>“Not only inside the respective standard cells C61, C62 and C63, but also among the standard cells C61, C62 and C63 to one another, the gate lengths and the gate intervals are equal in the patterns of the gate electrodes and the dummy gate electrodes.” (Ichiryu at 15:47-51). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “In the embodiment 5, the gate lengths are all equal in the gate electrodes and the dummy gate electrodes….” (Ichiryu at 16:10-11).<br><br>“In FIG. 14, a reference symbol C81 denotes a standard cell. The standard cell C81 comprises gate electrodes G, dummy gate electrodes DG and two gate electrodes G2 having a gate length different to those of the gate electrode G and the dummy gate electrode DG, wherein a width of the gate electrode G2 is set so that a cell width of the standard cell C81 in the X direction is an integral multiple of the gate pitch Gx. In FIG. 14, the cell width of the standard cell C81 is nine times as wide as the gate pitch Gx. The width of the gate electrode G2 is thus set because a processing speed is expected to be faster when the cell width of each cell in the X direction is the integral multiple of the gate pitch Gx than when the cell width of each cell takes an arbitrary value in the placement using the conventional automatic placement & routing tool. However, the width of the gate electrode G2 is not necessarily set in the foregoing manner.” (Ichiryu at 16:15-30).<br><br>“As described, in the case of including the standard cell comprising the gate electrodes having the different gate lengths….” (Ichiryu at 16:32-34).<br><br>“In the constitution, the distance from the cell boundary of each standard cell to the gate electrode in the closest vicinity and the distance from the cell boundary of another standard cell adjacent thereto to the gate electrode in the closest vicinity are constant.” (Ichiryu at 16:65-17:2).<br><br>“For example, a distance from each of the cell boundary of the standard cells C61, C62 and C63 to the gate electrode in the X direction is ‘Gx-gate length/2’ and constant even in the constitution shown in FIG. 11 where the dummy gate electrodes DG are not provided. A distance between a transistor disposed at the end of each standard cell and the gate electrode G of the adjacent standard cell is ‘2Gx-gate length’ and constant. For example, even in the case where the dummy gate electrode DG is not provided in the constitution described referring to FIG. 11, the distance from each of the cell boundary of the respective standard cells C61, C62 and C63 to the gate electrode G located at the end of each of the standard cells in the X direction is constant at (Gx-gate length/2). Further, the distance from the gate electrode G located at the end of each of the standard cells to the gate electrode G |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | located at the end of each of adjacent standard cells in the X direction is constant at (2Gx-gate length).” (Ichiryu at 17:6-22).<br><br>“Further, in the embodiment 6, the standard cells described in the embodiments 1 and 5 are used. The gate lengths and the gate intervals are thereby equal in the patterns of the gate electrodes of the placed standard cells C91, C92 and C93, which leads to the improvement of the precision in the finished dimension of the gate electrodes. The improvement of the precision in the finished dimension of the gate electrodes can be realized not only inside each of the standard cells C91, C92 and C93 but also between the standard cells.” (Ichiryu at 18:1-9).<br><br>“[W]hen the standard cells are adjacently located, the gate lengths and the gate intervals in the patterns of the gate electrodes and the dummy gate electrodes are the same as when they are located alone.” (Ichiryu at 18:10-13). |

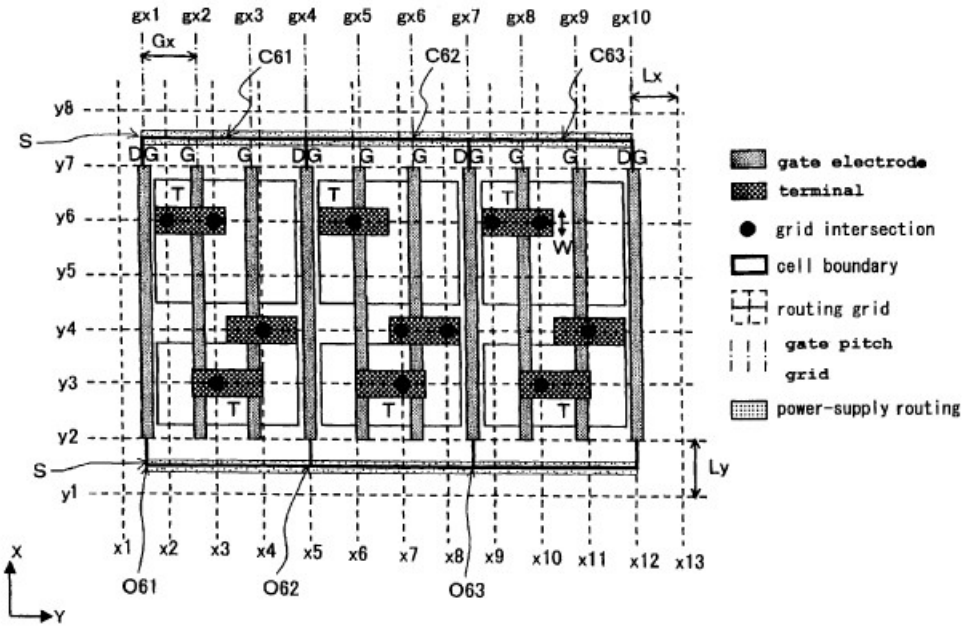
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | FIG. 11<br>  <br><br>(Ichiryu Fig. 11).<br>*See also* Ichiryu at Figs. 1, 2, 3, 8, 12, 13, 14.<br>This limitation also would have been obvious to a person of ordinary skill in the art based on (1) Ichiryu alone; and/or (2) the teachings with respect to this claim element as detailed in the cover document of Respondent’s invalidity contentions and Respondent’s other invalidity charts. |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| [2.3b] wherein the plurality of linear conductive segments are formed to have their lengths extend in a first direction in a parallel manner, and | At least under Tela’s apparent infringement theory, Ichiryu discloses and/or renders obvious wherein the plurality of linear conductive segments are formed to have their lengths extend in a first direction in a parallel manner.<br><br>Ichiryu describes layout techniques for gate electrodes, which are linear conductive segments, including placing them such that they extend in a parallel manner. The mapping of this element is the same for Figure 11 and for Modified Fig. 11M.<br><br>*See, e.g.*:<br><br>“[A]s the miniaturization of the process [continues], a precision in a finished dimension of the gate electrode ultimately obtained is deteriorated by an optical proximity effect when an interval between the gate electrodes and gate lengths of the gate electrodes are irregular in their patterns. When the precision in the finished dimension of the gate electrode is deteriorated, performances of respective transistors of the semiconductor integrated circuit are increasingly inconstant, which leads to an increased variation in a performance of the semiconductor integrate[d] circuit.” (Ichiryu at 2:23-32).<br><br>“[A]s recited in No. H10-32253 of the Publication of the Unexamined Japanese Patent Applications, the interval and the length of the gate electrodes in each standard cell are set regular so that the OPC is processed per standard cell in the conventional technology.” (Ichiryu at 2:37-41).<br><br>“The standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes….” (Ichiryu at 6:20-21).<br><br>“A standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes, wherein gate pitches of some of the gate electrodes are set to values different to the routing grid interval set along the X direction in parallel with the power-supply wiring of the standard cell, and a cell width along the X direction in parallel with the power-supply wiring of the standard cell is set to an integral multiple of a minimum value of the gate pitches of the gate |

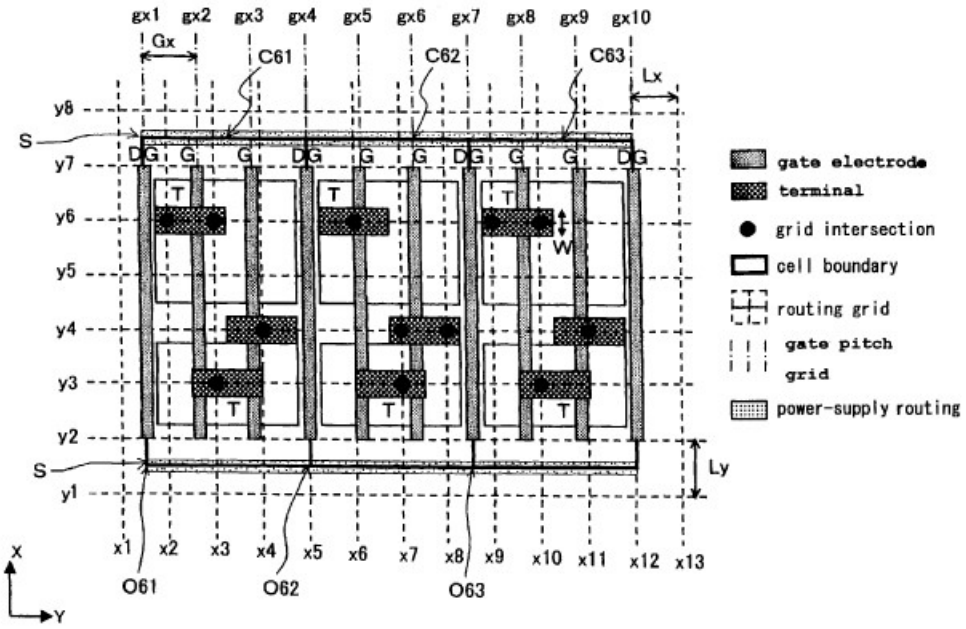
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | electrodes set to the values different to the routing grid interval set along the X direction.” (Ichiryu at 6:26-35).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, a precision in a finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:41-45).<br><br>“A standard cell according to the present invention comprises a plurality of gate electrodes and a plurality of dummy gate electrodes, wherein a cell width in the X direction in parallel with the power-supply wiring of the standard cell is an integral multiple of a minimum gate pitch of gate pitches of the gate electrodes and the dummy gate electrodes different to the routing grid interval along the X direction.” (Ichiryu at 6:46-52).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:58-62).<br><br>“The gate pitches of the standard cell are all preferably equal. Thereby, the pattern of the gate electrodes can impart a perfect regularity to the gate pitches, and the precision in the finished dimension of the gate electrodes can be further improved.” (Ichiryu at 6:66-7:3).<br><br>“Further, because the pattern of the gate electrodes can have the regularity, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be performed in each standard cell.” (Ichiryu at 8:21-24).<br><br>“Referring to reference symbols in FIG. 11, x1-x13 denote routing grids for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, y1-y8 denote routing grids disposed in parallel with the X direction and adjacent to one another in the Y direction, gx1-gx10 denote grids of gate pitches for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, C61, C62 and C63 are |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | standard cells, O61, O62 and O63 are respective origins of the standard cells C61, C62 and C63, … G denotes a gate electrode, and DG denotes a dummy gate electrode.” (Ichiryu at 14:32-44).<br><br>“In the standard cells C61, C62 and C63, gate lengths and gate intervals of the gate electrode G and dummy gate electrode DG are constant, and a cell width of the standard cells C61, C62 and C63 in the X direction is an integral multiple of a minimum value of a gate pitch Gx (value of gate pitch=gate length+gate interval) (In FIG. 11, the cell width of the standard cells C61, C62 and C63 is three times as wide as Gx).” (Ichiryu at 14:45-51).<br><br>“Not only inside the respective standard cells C61, C62 and C63, but also among the standard cells C61, C62 and C63 to one another, the gate lengths and the gate intervals are equal in the patterns of the gate electrodes and the dummy gate electrodes.” (Ichiryu at 15:47-51).<br><br>“In the embodiment 5, the gate lengths are all equal in the gate electrodes and the dummy gate electrodes….” (Ichiryu at 16:10-11).<br><br>“In FIG. 14, a reference symbol C81 denotes a standard cell. The standard cell C81 comprises gate electrodes G, dummy gate electrodes DG and two gate electrodes G2 having a gate length different to those of the gate electrode G and the dummy gate electrode DG, wherein a width of the gate electrode G2 is set so that a cell width of the standard cell C81 in the X direction is an integral multiple of the gate pitch Gx. In FIG. 14, the cell width of the standard cell C81 is nine times as wide as the gate pitch Gx. The width of the gate electrode G2 is thus set because a processing speed is expected to be faster when the cell width of each cell in the X direction is the integral multiple of the gate pitch Gx than when the cell width of each cell takes an arbitrary value in the placement using the conventional automatic placement & routing tool. However, the width of the gate electrode G2 is not necessarily set in the foregoing manner.” (Ichiryu at 16:15-30).<br><br>“As described, in the case of including the standard cell comprising the gate electrodes having the different gate lengths….” (Ichiryu at 16:32-34). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “In the constitution, the distance from the cell boundary of each standard cell to the gate electrode in the closest vicinity and the distance from the cell boundary of another standard cell adjacent thereto to the gate electrode in the closest vicinity are constant.” (Ichiryu at 16:65-17:2).<br><br>“For example, a distance from each of the cell boundary of the standard cells C61, C62 and C63 to the gate electrode in the X direction is ‘Gx-gate length/2’ and constant even in the constitution shown in FIG. 11 where the dummy gate electrodes DG are not provided. A distance between a transistor disposed at the end of each standard cell and the gate electrode G of the adjacent standard cell is ‘2Gx-gate length’ and constant. For example, even in the case where the dummy gate electrode DG is not provided in the constitution described referring to FIG. 11, the distance from each of the cell boundary of the respective standard cells C61, C62 and C63 to the gate electrode G located at the end of each of the standard cells in the X direction is constant at (Gx-gate length/2). Further, the distance from the gate electrode G located at the end of each of the standard cells to the gate electrode G located at the end of each of adjacent standard cells in the X direction is constant at (2Gx-gate length).” (Ichiryu at 17:6-22).<br><br>“Further, in the embodiment 6, the standard cells described in the embodiments 1 and 5 are used. The gate lengths and the gate intervals are thereby equal in the patterns of the gate electrodes of the placed standard cells C91, C92 and C93, which leads to the improvement of the precision in the finished dimension of the gate electrodes. The improvement of the precision in the finished dimension of the gate electrodes can be realized not only inside each of the standard cells C91, C92 and C93 but also between the standard cells.” (Ichiryu at 18:1-9).<br><br>“[W]hen the standard cells are adjacently located, the gate lengths and the gate intervals in the patterns of the gate electrodes and the dummy gate electrodes are the same as when they are located alone.” (Ichiryu at 18:10-13). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | F I G. 11<br>  <br><br>(Ichiryu Fig. 11).<br>*See also* Ichiryu at Figs. 1, 2, 3, 8, 12, 13, 14.<br>This limitation also would have been obvious to a person of ordinary skill in the art based on (1) Ichiryu alone; and/or (2) the teachings with respect to this claim element as detailed in the cover document of Respondent’s invalidity contentions and Respondent’s other invalidity charts. |

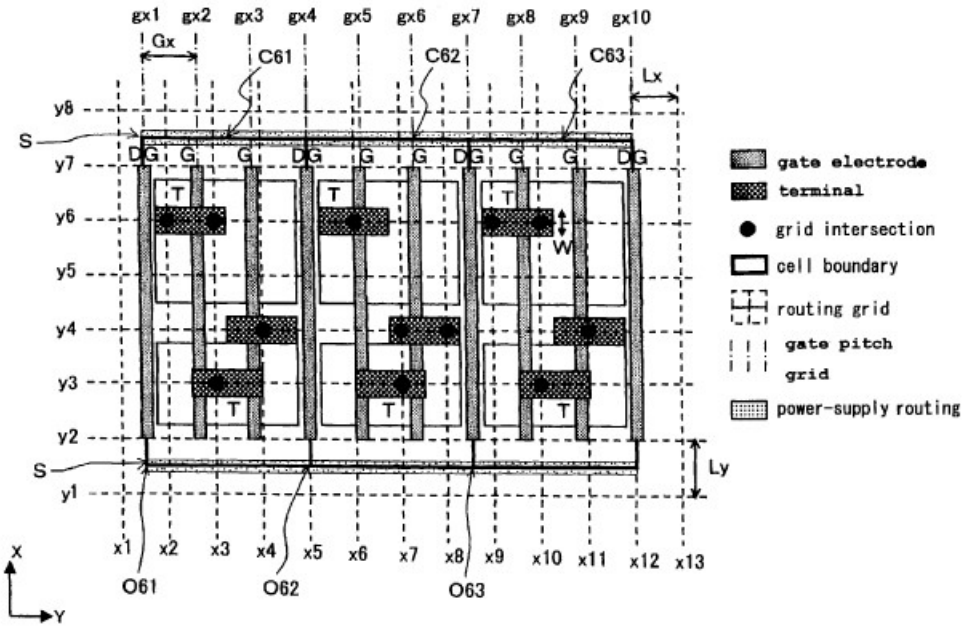
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| [2.4] wherein at least four of the plurality of linear conductive segments are active linear conductive segments, wherein each active linear conductive segment forms at least one gate electrode of at least one transistor device, and | At least under Tela’s apparent infringement theory, Ichiryu discloses and/or renders obvious wherein at least four of the plurality of linear conductive segments are active linear conductive segments, wherein each active linear conductive segment forms at least one gate electrode of at least one transistor device.<br><br>Ichiryu describes and depicts multiple gate electrodes that form transistors of different types, including at least four active linear conductive segments that each form the gate of at least one transistor. The mapping of this element is the same for Figure 11 and for Modified Fig. 11M.<br><br>*See, e.g.*:<br><br>“When the prevision in the finished dimension of the gate electrode is deteriorated, performances of respective transistors of the semiconductor integrated circuit are increasingly inconstant….” (Ichiryu at 2:27-30).<br><br>“[A] distance from each of the cell boundary of the standard cells C61, C62 and C63 to the gate electrode in the X direction is ‘Gx-gate length/2’ and constant even in the constitution shown in FIG. 11 where the dummy gate electrodes DG are not provided. A distance between a transistor disposed at the end of each standard cell and the gate electrode G of the adjacent standard cell is ‘2Gx-gate length’ and constant.” (Ichiryu at 17:6-13). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | F I G. 11<br>  <br><br>(Ichiryu Fig. 11).<br>*See also* Ichiryu Figs. 1, 2, 3, 8, 12, 13, 14.<br>This limitation also would have been obvious to a person of ordinary skill in the art based on (1) Ichiryu alone; and/or (2) the teachings with respect to this claim element as detailed in the cover document of Respondent’s invalidity contentions and Respondent’s other invalidity charts. |

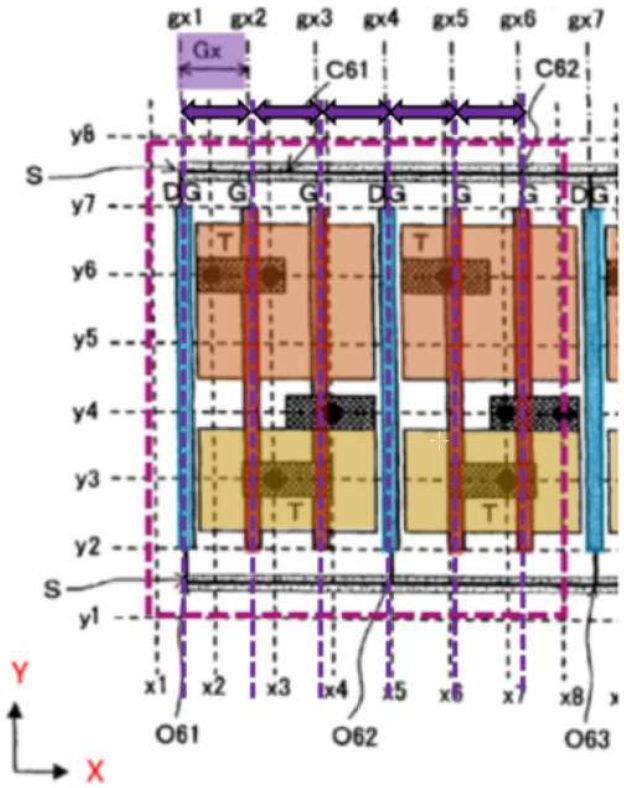
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| [2.5] wherein at least one of the plurality of linear conductive segments is a non-gate linear conductive segment, wherein the non-gate linear conductive segment does not form a gate electrode of a transistor device. | At least under Tela’s apparent infringement theory, Ichiryu discloses and/or renders obvious wherein at least one of the plurality of linear conductive segments is a non-gate linear conductive segment, wherein the non-gate linear conductive segment does not form a gate electrode of a transistor device.<br><br>The mapping of this element is the same for Figure 11 and for Modified Fig. 11M. Ichiryu describes and depicts multiple dummy gates, e.g. “dummy gate electrodes” or “DG.”<br><br>*See, e.g.*:<br><br>“Dummy gate electrodes DG are provided on cell boundaries of standard cells C41’, C4[2]’ and C43’ disposed on the upper side in FIG. 18. These dummy gate electrodes DG are shared between the adjacent standard cells. The gate electrodes G and the dummy gate electrodes DG are respectively equally spaced, and their gate [] lengths are equal.” (Ichiryu at 2:45-50).<br><br>“[W]hen the regions R1, R2 and R3 for adjusting the cell width to the integral multiple of the routing grid interval are provided, the gate electrode located on the cell boundary of the standard cell cannot be shared. There is a possibility that the dummy electrodes DG are located with less than a minimum interval allowed in a design rule therebetween, which results in an error in the design rule. In order to avoid the foregoing error in the design rule, it is necessary to enlarge the gate length, for example, in the same manner as the dummy gate DG2 disposed on the lower side in FIG. 18.” (Ichiryu at 3:7-16).<br><br>“Though the gate interval in each standard cell can be maintained at the constant level when such the gate length enlargement is executed, the gate length becomes irregular at the dummy gate electrodes DG2, which results in the imprecision of the finished dimension of the gate electrodes. Further, the OPC cannot be processed in each standard cell due to the different gate lengths in the dummy gate electrodes DG in each standard cell and the dummy gate electrodes DG2 adjacent thereto.” (Ichiryu at 3:17-25).<br><br>“A standard cell according to the present invention comprises a plurality of gate electrodes and a plurality of dummy gate electrodes, wherein a cell width in the X direction in parallel with the power-supply wiring of the standard cell is an integral multiple of a minimum gate pitch of gate |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | pitches of the gate electrodes and the dummy gate electrodes different to the routing grid interval along the X direction.” (Ichiryu at 6:46-52).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell. As another advantage, the provision of the dummy gate electrodes can further improve the regularity of the gate length and gate interval, which largely contributes to the facilitation of the OPC process in each standard cell.” (Ichiryu at 6:58-65).<br><br>“Referring to reference symbols in FIG. 11, x1-x13 denote routing grids for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, y1-y8 denote routing grids disposed in parallel with the X direction and adjacent to one another in the Y direction, gx1-gx10 denote grids of gate pitches for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, C61, C62 and C63 are standard cells, O61, O62 and O63 are respective origins of the standard cells C61, C62 and C63, … G denotes a gate electrode, and DG denotes a dummy gate electrode.” (Ichiryu at 14:32-44).<br><br>“Not only inside the respective standard cells C61, C62 and C63, but also among the standard cells C61, C62 and C63 to one another, the gate lengths and the gate intervals are equal in the patterns of the gate electrodes and the dummy gate electrodes.” (Ichiryu at 15:47-51).<br><br>“In FIG. 14, a reference symbol C81 denotes a standard cell. The standard cell C81 comprises gate electrodes G, dummy gate electrodes DG and two gate electrodes G2 having a gate length different to those of the gate electrode G and the dummy gate electrode DG, wherein a width of the gate electrode G2 is set so that a cell width of the standard cell C81 in the X direction is an integral multiple of the gate pitch Gx. In FIG. 14, the cell width of the standard cell C81 is nine times as wide as the gate pitch Gx. The width of the gate electrode G2 is thus set because a processing speed is expected to be faster when the cell width of each cell in the X direction is the integral multiple of the gate pitch Gx than when the cell width of each cell takes an arbitrary value in the placement using the |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | conventional automatic placement & routing tool. However, the width of the gate electrode G2 is not necessarily set in the foregoing manner.” (Ichiryu at 16:15-30).<br><br>“[T]he embodiment 5 can be applied in the same manner to a cell structure where the dummy gate electrodes having the different gate lengths are provided and a cell structure where the gate electrodes and the dummy gate electrodes having the different gate intervals are provided. The description of the embodiment 5 is premised on the provision of the dummy gates DG….” (Ichiryu at 16:53-59).<br><br>“[W]hen the standard cells are adjacently located, the gate lengths and the gate intervals in the patterns of the gate electrodes and the dummy gate electrodes are the same as when they are located alone.” (Ichiryu at 18:10-13). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | F I G. 11<br>  <br><br>(Ichiryu Fig. 11).<br>*See also* Ichiryu at Figs. 1, 2, 3, 8, 12, 13, 14.<br>This limitation also would have been obvious to a person of ordinary skill in the art based on (1) Ichiryu alone; and/or (2) the teachings with respect to this claim element as detailed in the cover document of Respondent’s invalidity contentions and Respondent’s other invalidity charts. |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| [4.0] An integrated circuit device as recited in claim 2,<br><br>wherein the plurality of linear conductive segments are positioned in a side-by-side manner according to a substantially equal centerline-to-centerline spacing as measured in a second direction perpendicular to the first direction. | At least under Tela’s apparent infringement theory, Ichiryu discloses and/or renders obvious an integrated circuit device as recited in claim 2, wherein the plurality of linear conductive segments are positioned in a side-by-side manner according to a substantially equal centerline-to-centerline spacing as measured in a second direction perpendicular to the first direction.<br><br>Ichiryu describes layout techniques for gate electrodes, which are linear conductive segments, including placing them such that they extend in parallel. Ichiryu discloses that “ “[i]n the standard cells C61, C62 and C63, gate lengths and gate intervals of the gate electrode[s] G and dummy gate electrode[s] DG are constant ….” Ichiryu at 14:45-47. Gx is “gate pitch=gate length+gate interval” |

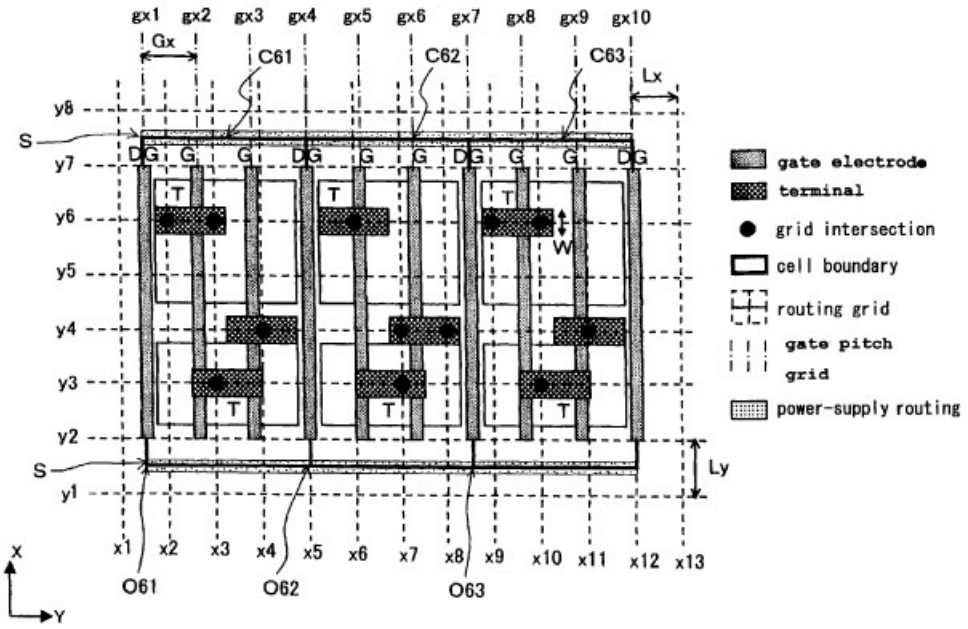
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | **Fig. 11 (excerpt)**<br>  <br><br>*See, e.g.*:<br>“[A]s the miniaturization of the process [continues], a precision in a finished dimension of the gate electrode ultimately obtained is deteriorated by an optical proximity effect when an interval between the gate electrodes and gate lengths of the gate electrodes are irregular in their patterns. When the |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | precision in the finished dimension of the gate electrode is deteriorated, performances of respective transistors of the semiconductor integrated circuit are increasingly inconstant, which leads to an increased variation in a performance of the semiconductor integrate[d] circuit.” (Ichiryu at 2:23-32).<br><br>“[A]s recited in No. H10-32253 of the Publication of the Unexamined Japanese Patent Applications, the interval and the length of the gate electrodes in each standard cell are set regular so that the OPC is processed per standard cell in the conventional technology.” (Ichiryu at 2:37-41).<br><br>“The standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes….” (Ichiryu at 6:20-21).<br><br>“A standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes, wherein gate pitches of some of the gate electrodes are set to values different to the routing grid interval set along the X direction in parallel with the power-supply wiring of the standard cell, and a cell width along the X direction in parallel with the power-supply wiring of the standard cell is set to an integral multiple of a minimum value of the gate pitches of the gate electrodes set to the values different to the routing grid interval set along the X direction.” (Ichiryu at 6:26-35).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, a precision in a finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:41-45).<br><br>“A standard cell according to the present invention comprises a plurality of gate electrodes and a plurality of dummy gate electrodes, wherein a cell width in the X direction in parallel with the power-supply wiring of the standard cell is an integral multiple of a minimum gate pitch of gate pitches of the gate electrodes and the dummy gate electrodes different to the routing grid interval along the X direction.” (Ichiryu at 6:46-52). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:58-62).<br><br>“The gate pitches of the standard cell are all preferably equal. Thereby, the pattern of the gate electrodes can impart a perfect regularity to the gate pitches, and the precision in the finished dimension of the gate electrodes can be further improved.” (Ichiryu at 6:66-7:3).<br><br>“Further, because the pattern of the gate electrodes can have the regularity, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be performed in each standard cell.” (Ichiryu at 8:21-24).<br><br>“Referring to reference symbols in FIG. 11, x1-x13 denote routing grids for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, y1-y8 denote routing grids disposed in parallel with the X direction and adjacent to one another in the Y direction, gx1-gx10 denote grids of gate pitches for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, C61, C62 and C63 are standard cells, O61, O62 and O63 are respective origins of the standard cells C61, C62 and C63, … G denotes a gate electrode, and DG denotes a dummy gate electrode.” (Ichiryu at 14:32-44).<br><br>“In the standard cells C61, C62 and C63, gate lengths and gate intervals of the gate electrode G and dummy gate electrode DG are constant, and a cell width of the standard cells C61, C62 and C63 in the X direction is an integral multiple of a minimum value of a gate pitch Gx (value of gate pitch=gate length+gate interval) (In FIG. 11, the cell width of the standard cells C61, C62 and C63 is three times as wide as Gx).” (Ichiryu at 14:45-51).<br><br>“Not only inside the respective standard cells C61, C62 and C63, but also among the standard cells C61, C62 and C63 to one another, the gate lengths and the gate intervals are equal in the patterns of the gate electrodes and the dummy gate electrodes.” (Ichiryu at 15:47-51). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “In the embodiment 5, the gate lengths are all equal in the gate electrodes and the dummy gate electrodes….” (Ichiryu at 16:10-11).<br><br>“In FIG. 14, a reference symbol C81 denotes a standard cell. The standard cell C81 comprises gate electrodes G, dummy gate electrodes DG and two gate electrodes G2 having a gate length different to those of the gate electrode G and the dummy gate electrode DG, wherein a width of the gate electrode G2 is set so that a cell width of the standard cell C81 in the X direction is an integral multiple of the gate pitch Gx. In FIG. 14, the cell width of the standard cell C81 is nine times as wide as the gate pitch Gx. The width of the gate electrode G2 is thus set because a processing speed is expected to be faster when the cell width of each cell in the X direction is the integral multiple of the gate pitch Gx than when the cell width of each cell takes an arbitrary value in the placement using the conventional automatic placement & routing tool. However, the width of the gate electrode G2 is not necessarily set in the foregoing manner.” (Ichiryu at 16:15-30).<br><br>“As described, in the case of including the standard cell comprising the gate electrodes having the different gate lengths….” (Ichiryu at 16:32-34).<br><br>“In the constitution, the distance from the cell boundary of each standard cell to the gate electrode in the closest vicinity and the distance from the cell boundary of another standard cell adjacent thereto to the gate electrode in the closest vicinity are constant.” (Ichiryu at 16:65-17:2).<br><br>“For example, a distance from each of the cell boundary of the standard cells C61, C62 and C63 to the gate electrode in the X direction is ‘Gx-gate length/2’ and constant even in the constitution shown in FIG. 11 where the dummy gate electrodes DG are not provided. A distance between a transistor disposed at the end of each standard cell and the gate electrode G of the adjacent standard cell is ‘2Gx-gate length’ and constant. For example, even in the case where the dummy gate electrode DG is not provided in the constitution described referring to FIG. 11, the distance from each of the cell boundary of the respective standard cells C61, C62 and C63 to the gate electrode G located at the end of each of the standard cells in the X direction is constant at (Gx-gate length/2). Further, the distance from the gate electrode G located at the end of each of the standard cells to the gate electrode G |

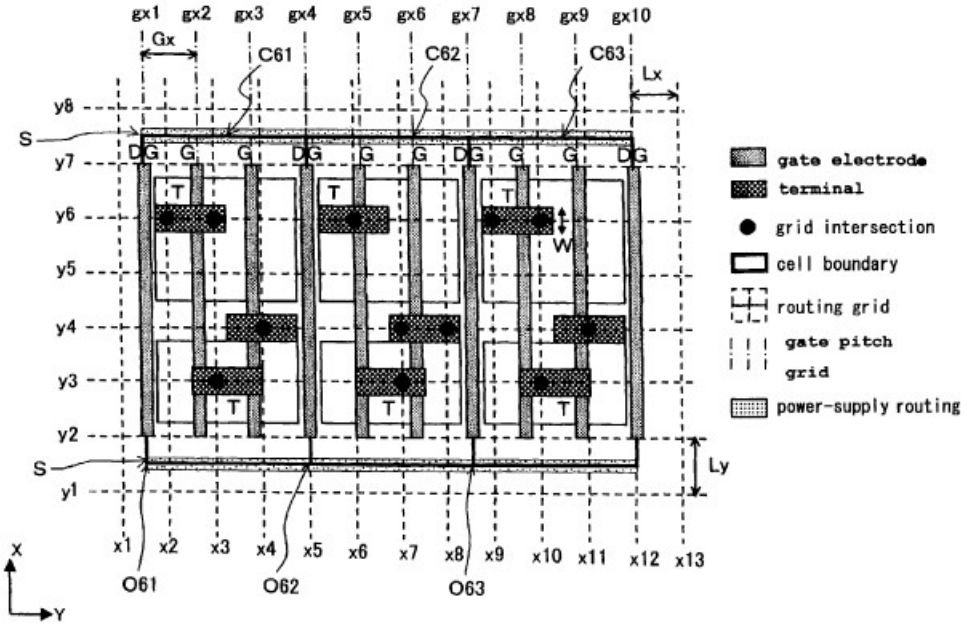
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | located at the end of each of adjacent standard cells in the X direction is constant at (2Gx-gate length).” (Ichiryu at 17:6-22).<br><br>“Further, in the embodiment 6, the standard cells described in the embodiments 1 and 5 are used. The gate lengths and the gate intervals are thereby equal in the patterns of the gate electrodes of the placed standard cells C91, C92 and C93, which leads to the improvement of the precision in the finished dimension of the gate electrodes. The improvement of the precision in the finished dimension of the gate electrodes can be realized not only inside each of the standard cells C91, C92 and C93 but also between the standard cells.” (Ichiryu at 18:1-9).<br><br>“[W]hen the standard cells are adjacently located, the gate lengths and the gate intervals in the patterns of the gate electrodes and the dummy gate electrodes are the same as when they are located alone.” (Ichiryu at 18:10-13). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | F I G. 11<br>  <br><br>(Ichiryu Fig. 11).<br>*See also* Ichiryu at Figs. 1, 2, 3, 8, 12, 13, 14.<br>Ichiryu describes layout techniques for gate electrodes, including that they have equal centerline-to-centerline spacing.<br>*See, e.g.*: |

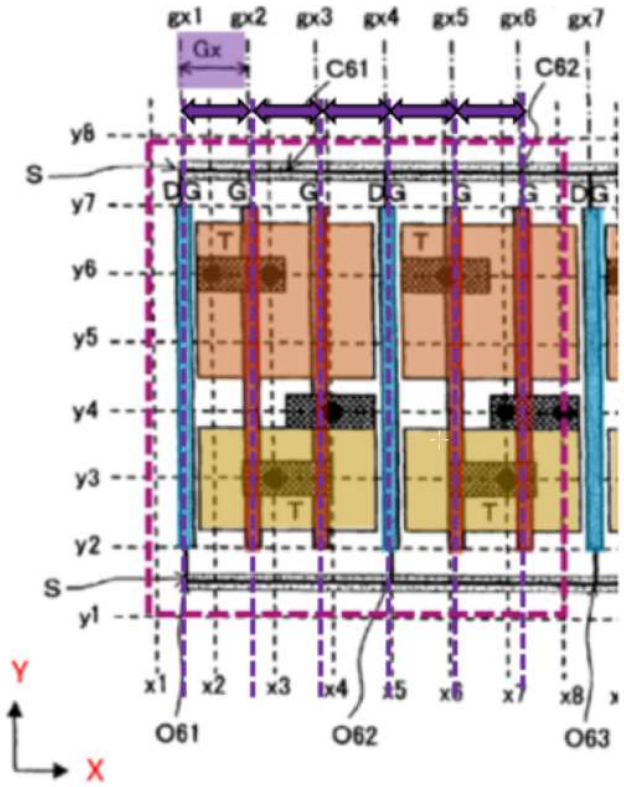
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “[A]s recited in No. H10-32253 of the Publication of the Unexamined Japanese Patent Applications, the interval and the length of the gate electrodes in each standard cell are set regular so that the OPC is processed per standard cell in the conventional technology.” (Ichiryu at 2:37-41).<br><br>“The standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes….” (Ichiryu at 6:20-21).<br><br>“A standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes, wherein gate pitches of some of the gate electrodes are set to values different to the routing grid interval set along the X direction in parallel with the power-supply wiring of the standard cell, and a cell width along the X direction in parallel with the power-supply wiring of the standard cell is set to an integral multiple of a minimum value of the gate pitches of the gate electrodes set to the values different to the routing grid interval set along the X direction.” (Ichiryu at 6:26-35).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, a precision in a finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:41-45).<br><br>“A standard cell according to the present invention comprises a plurality of gate electrodes and a plurality of dummy gate electrodes, wherein a cell width in the X direction in parallel with the power-supply wiring of the standard cell is an integral multiple of a minimum gate pitch of gate pitches of the gate electrodes and the dummy gate electrodes different to the routing grid interval along the X direction.” (Ichiryu at 6:46-52).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:58-62). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “The gate pitches of the standard cell are all preferably equal. Thereby, the pattern of the gate electrodes can impart a perfect regularity to the gate pitches, and the precision in the finished dimension of the gate electrodes can be further improved.” (Ichiryu at 6:66-7:3).<br><br>“Further, because the pattern of the gate electrodes can have the regularity, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be performed in each standard cell.” (Ichiryu at 8:21-24).<br><br>“Referring to reference symbols in FIG. 11, x1-x13 denote routing grids for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, y1-y8 denote routing grids disposed in parallel with the X direction and adjacent to one another in the Y direction, gx1-gx10 denote grids of gate pitches for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, C61, C62 and C63 are standard cells, O61, O62 and O63 are respective origins of the standard cells C61, C62 and C63, … G denotes a gate electrode, and DG denotes a dummy gate electrode.” (Ichiryu at 14:32-44).<br><br>“In the standard cells C61, C62 and C63, gate lengths and gate intervals of the gate electrode G and dummy gate electrode DG are constant, and a cell width of the standard cells C61, C62 and C63 in the X direction is an integral multiple of a minimum value of a gate pitch Gx (value of gate pitch=gate length+gate interval) (In FIG. 11, the cell width of the standard cells C61, C62 and C63 is three times as wide as Gx).” (Ichiryu at 14:45-51).<br><br>“Not only inside the respective standard cells C61, C62 and C63, but also among the standard cells C61, C62 and C63 to one another, the gate lengths and the gate intervals are equal in the patterns of the gate electrodes and the dummy gate electrodes.” (Ichiryu at 15:47-51).<br><br>“In the embodiment 5, the gate lengths are all equal in the gate electrodes and the dummy gate electrodes….” (Ichiryu at 16:10-11).<br><br>“In FIG. 14, a reference symbol C81 denotes a standard cell. The standard cell C81 comprises gate electrodes G, dummy gate electrodes DG and two gate electrodes G2 having a gate length different to |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | those of the gate electrode G and the dummy gate electrode DG, wherein a width of the gate electrode G2 is set so that a cell width of the standard cell C81 in the X direction is an integral multiple of the gate pitch Gx. In FIG. 14, the cell width of the standard cell C81 is nine times as wide as the gate pitch Gx. The width of the gate electrode G2 is thus set because a processing speed is expected to be faster when the cell width of each cell in the X direction is the integral multiple of the gate pitch Gx than when the cell width of each cell takes an arbitrary value in the placement using the conventional automatic placement & routing tool. However, the width of the gate electrode G2 is not necessarily set in the foregoing manner.” (Ichiryu at 16:15-30).<br><br>“In the constitution, the distance from the cell boundary of each standard cell to the gate electrode in the closest vicinity and the distance from the cell boundary of another standard cell adjacent thereto to the gate electrode in the closest vicinity are constant.” (Ichiryu at 16:65-17:2).<br><br>“For example, a distance from each of the cell boundary of the standard cells C61, C62 and C63 to the gate electrode in the X direction is ‘Gx-gate length/2’ and constant even in the constitution shown in FIG. 11 where the dummy gate electrodes DG are not provided. A distance between a transistor disposed at the end of each standard cell and the gate electrode G of the adjacent standard cell is ‘2Gx-gate length’ and constant. For example, even in the case where the dummy gate electrode DG is not provided in the constitution described referring to FIG. 11, the distance from each of the cell boundary of the respective standard cells C61, C62 and C63 to the gate electrode G located at the end of each of the standard cells in the X direction is constant at (Gx-gate length/2). Further, the distance from the gate electrode G located at the end of each of the standard cells to the gate electrode G located at the end of each of adjacent standard cells in the X direction is constant at (2Gx-gate length).” (Ichiryu at 17:6-22).<br><br>“Further, in the embodiment 6, the standard cells described in the embodiments 1 and 5 are used. The gate lengths and the gate intervals are thereby equal in the patterns of the gate electrodes of the placed standard cells C91, C92 and C93, which leads to the improvement of the precision in the finished dimension of the gate electrodes. The improvement of the precision in the finished |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | dimension of the gate electrodes can be realized not only inside each of the standard cells C91, C92 and C93 but also between the standard cells.” (Ichiryu at 18:1-9).<br><br>“[W]hen the standard cells are adjacently located, the gate lengths and the gate intervals in the patterns of the gate electrodes and the dummy gate electrodes are the same as when they are located alone.” (Ichiryu at 18:10-13).<br><br>F I G. 11<br>  <br><br><br>(Ichiryu Fig. 11). |

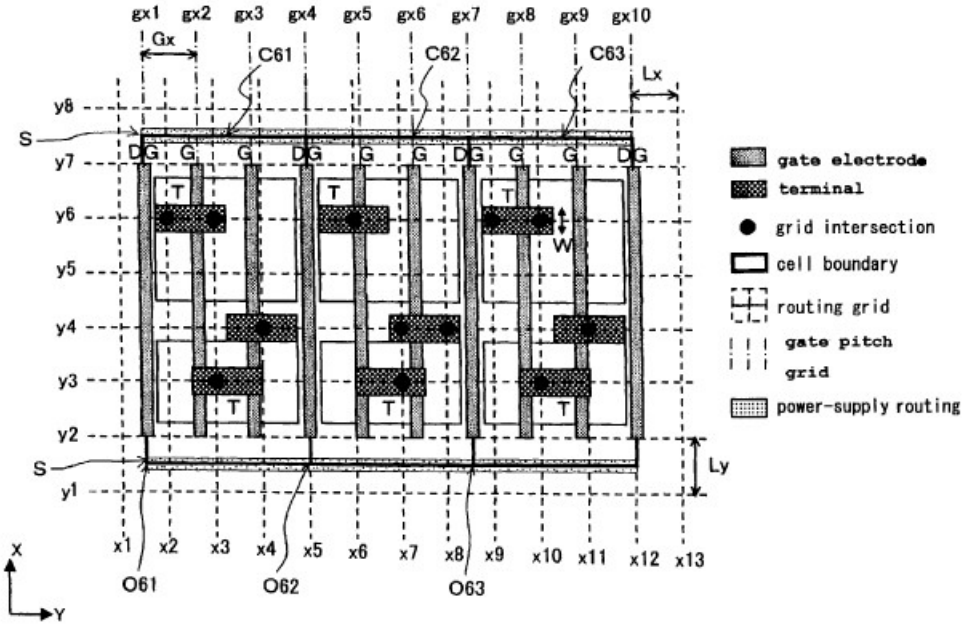
| '012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | *See also* Ichiryu at Figs. 1, 2, 3, 8, 12, 13, 14.<br><br>This limitation also would have been obvious to a person of ordinary skill in the art based on (1) Ichiryu alone; and/or (2) the teachings with respect to this claim element as detailed in the cover document of Respondent's invalidity contentions and Respondent's other invalidity charts. |
| [5.0] An integrated circuit device as recited in claim 4,<br><br>wherein the substantially equal centerline-to-centerline spacing as measured in the second direction is less than 360 nanometers. | At least under Tela's apparent infringement theory, Ichiryu discloses and/or renders obvious an integrated circuit device as recited in claim 4, wherein the substantially equal centerline-to-centerline spacing as measured in the second direction is less than 360 nanometers.<br><br>Ichiryu describes layout techniques for gate electrodes, including equal centerline-to-centerline spacing. Ichiryu discloses that " "[i]n the standard cells C61, C62 and C63, gate lengths and gate intervals of the gate electrode[s] G and dummy gate electrode[s] DG are constant …." Ichiryu at 14:45-47. Gx is "gate pitch=gate length+gate interval" |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | Fig. 11 (excerpt)<br>  <br><br>*See, e.g.*: |

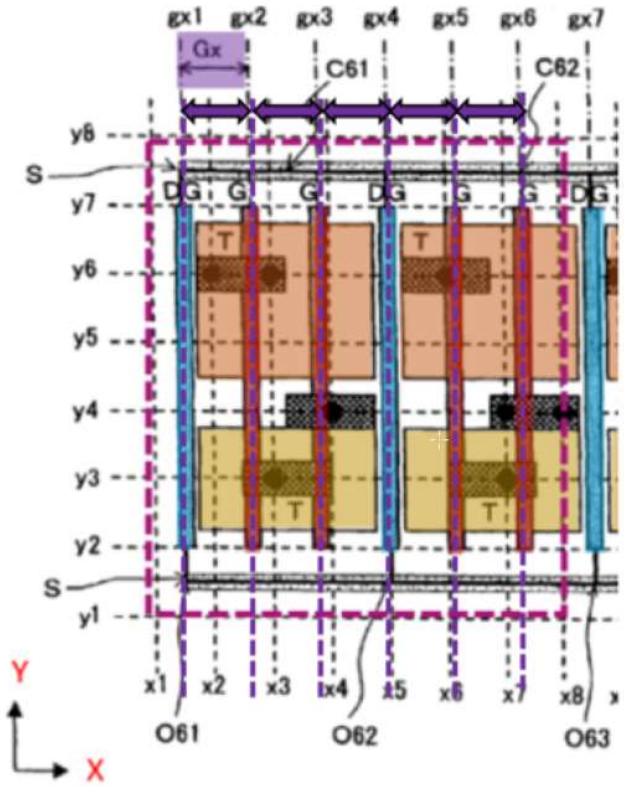
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “[A]s recited in No. H10-32253 of the Publication of the Unexamined Japanese Patent Applications, the interval and the length of the gate electrodes in each standard cell are set regular so that the OPC is processed per standard cell in the conventional technology.” (Ichiryu at 2:37-41).<br><br>“The standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes….” (Ichiryu at 6:20-21).<br><br>“A standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes, wherein gate pitches of some of the gate electrodes are set to values different to the routing grid interval set along the X direction in parallel with the power-supply wiring of the standard cell, and a cell width along the X direction in parallel with the power-supply wiring of the standard cell is set to an integral multiple of a minimum value of the gate pitches of the gate electrodes set to the values different to the routing grid interval set along the X direction.” (Ichiryu at 6:26-35).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, a precision in a finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:41-45).<br><br>“A standard cell according to the present invention comprises a plurality of gate electrodes and a plurality of dummy gate electrodes, wherein a cell width in the X direction in parallel with the power-supply wiring of the standard cell is an integral multiple of a minimum gate pitch of gate pitches of the gate electrodes and the dummy gate electrodes different to the routing grid interval along the X direction.” (Ichiryu at 6:46-52).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:58-62). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “The gate pitches of the standard cell are all preferably equal. Thereby, the pattern of the gate electrodes can impart a perfect regularity to the gate pitches, and the precision in the finished dimension of the gate electrodes can be further improved.” (Ichiryu at 6:66-7:3).<br><br>“Further, because the pattern of the gate electrodes can have the regularity, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be performed in each standard cell.” (Ichiryu at 8:21-24).<br><br>“Referring to reference symbols in FIG. 11, x1-x13 denote routing grids fo the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, y1-y8 denote routing grids disposed in parallel with the X direction and adjacent to one another in the Y direction, gx1-gx10 denote grids of gate pitches for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, C61, C62 and C63 are standard cells, O61, O62 and O63 are respective origins of the standard cells C61, C62 and C63, … G denotes a gate electrode, and DG denotes a dummy gate electrode.” (Ichiryu at 14:32-44).<br><br>“In the standard cells C61, C62 and C63, gate lengths and gate intervals of the gate electrode G and dummy gate electrode DG are constant, and a cell width of the standard cells C61, C62 and C63 in the X direction is an integral multiple of a minimum value of a gate pitch Gx (value of gate pitch=gate length+gate interval) (In FIG. 11, the cell width of the standard cells C61, C62 and C63 is three times as wide as Gx).” (Ichiryu at 14:45-51).<br><br>“Not only inside the respective standard cells C61, C62 and C63, but also among the standard cells C61, C62 and C63 to one another, the gate lengths and the gate intervals are equal in the patterns of the gate electrodes and the dummy gate electrodes.” (Ichiryu at 15:47-51).<br><br>“In the embodiment 5, the gate lengths are all equal in the gate electrodes and the dummy gate electrodes….” (Ichiryu at 16:10-11).<br><br>“In FIG. 14, a reference symbol C81 denotes a standard cell. The standard cell C81 comprises gate electrodes G, dummy gate electrodes DG and two gate electrodes G2 having a gate length different to |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | those of the gate electrode G and the dummy gate electrode DG, wherein a width of the gate electrode G2 is set so that a cell width of the standard cell C81 in the X direction is an integral multiple of the gate pitch Gx. In FIG. 14, the cell width of the standard cell C81 is nine times as wide as the gate pitch Gx. The width of the gate electrode G2 is thus set because a processing speed is expected to be faster when the cell width of each cell in the X direction is the integral multiple of the gate pitch Gx than when the cell width of each cell takes an arbitrary value in the placement using the conventional automatic placement & routing tool. However, the width of the gate electrode G2 is not necessarily set in the foregoing manner.” (Ichiryu at 16:15-30).<br><br>“In the constitution, the distance from the cell boundary of each standard cell to the gate electrode in the closest vicinity and the distance from the cell boundary of another standard cell adjacent thereto to the gate electrode in the closest vicinity are constant.” (Ichiryu at 16:65-17:2).<br><br>“For example, a distance from each of the cell boundary of the standard cells C61, C62 and C63 to the gate electrode in the X direction is ‘Gx-gate length/2’ and constant even in the constitution shown in FIG. 11 where the dummy gate electrodes DG are not provided. A distance between a transistor disposed at the end of each standard cell and the gate electrode G of the adjacent standard cell is ‘2Gx-gate length’ and constant. For example, even in the case where the dummy gate electrode DG is not provided in the constitution described referring to FIG. 11, the distance from each of the cell boundary of the respective standard cells C61, C62 and C63 to the gate electrode G located at the end of each of the standard cells in the X direction is constant at (Gx-gate length/2). Further, the distance from the gate electrode G located at the end of each of the standard cells to the gate electrode G located at the end of each of adjacent standard cells in the X direction is constant at (2Gx-gate length).” (Ichiryu at 17:6-22).<br><br>“Further, in the embodiment 6, the standard cells described in the embodiments 1 and 5 are used. The gate lengths and the gate intervals are thereby equal in the patterns of the gate electrodes of the placed standard cells C91, C92 and C93, which leads to the improvement of the precision in the finished dimension of the gate electrodes. The improvement of the precision in the finished |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | dimension of the gate electrodes can be realized not only inside each of the standard cells C91, C92 and C93 but also between the standard cells.” (Ichiryu at 18:1-9).<br><br>“[W]hen the standard cells are adjacently located, the gate lengths and the gate intervals in the patterns of the gate electrodes and the dummy gate electrodes are the same as when they are located alone.” (Ichiryu at 18:10-13).<br><br>F I G. 11<br>  <br><br><br>(Ichiryu Fig. 11). |

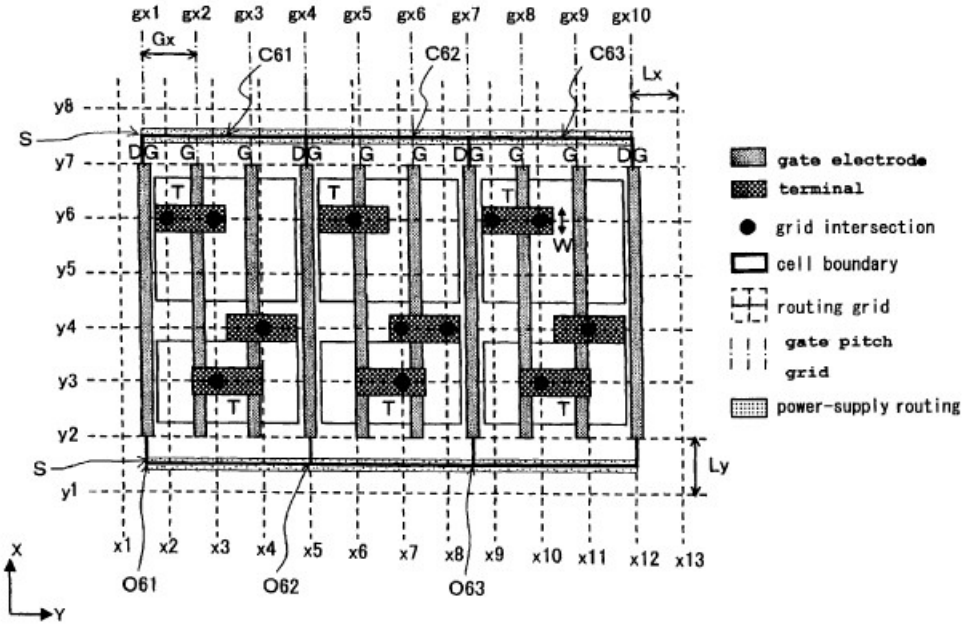
| '012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | *See also* Ichiryu at Figs. 1, 2, 3, 8, 12, 13, 14.<br><br>This limitation also would have been obvious to a person of ordinary skill in the art based on (1) Ichiryu alone; and/or (2) the teachings with respect to this claim element as detailed in the cover document of Respondent's invalidity contentions and Respondent's other invalidity charts. |
| [6.0] An integrated circuit device as recited in claim 4,<br><br>wherein a side-to-side spacing between each adjacently positioned pair of the plurality of linear conductive segments is less than 360 nanometers, wherein the side-to-side spacing is measured in the second direction. | At least under Tela's apparent infringement theory, Ichiryu discloses and/or renders obvious an integrated circuit device as recited in claim 4, wherein a side-to-side spacing between each adjacently positioned pair of the plurality of linear conductive segments is less than 360 nanometers, wherein the side-to-side spacing is measured in the second direction.<br><br>Ichiryu describes and depicts multiple gate electrodes that form transistors of different types and are placed on a grid having the same pitch and width, and thus equal side-to-side spacing of less than 360nm. Ichiryu discloses that " "[i]n the standard cells C61, C62 and C63, gate lengths and gate intervals of the gate electrode[s] G and dummy gate electrode[s] DG are constant …." Ichiryu at 14:45-47. Gx is "gate pitch=gate length+gate interval" Side by side spacing is smaller than gate pitch. |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | Fig. 11 (excerpt)<br>  <br><br>*See, e.g.*: |

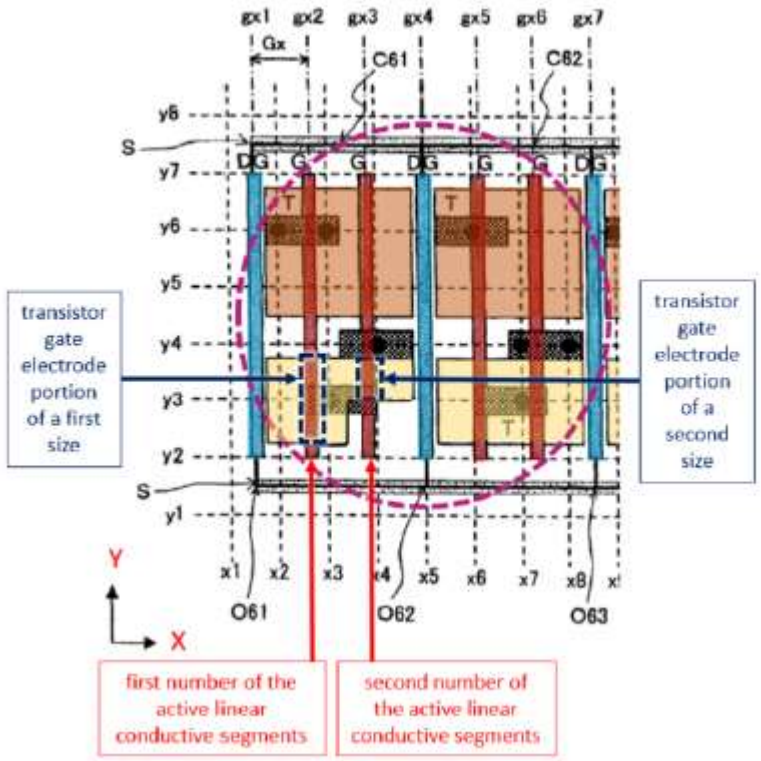
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “[A]s recited in No. H10-32253 of the Publication of the Unexamined Japanese Patent Applications, the interval and the length of the gate electrodes in each standard cell are set regular so that the OPC is processed per standard cell in the conventional technology.” (Ichiryu at 2:37-41).<br><br>“The standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes….” (Ichiryu at 6:20-21).<br><br>“A standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes, wherein gate pitches of some of the gate electrodes are set to values different to the routing grid interval set along the X direction in parallel with the power-supply wiring of the standard cell, and a cell width along the X direction in parallel with the power-supply wiring of the standard cell is set to an integral multiple of a minimum value of the gate pitches of the gate electrodes set to the values different to the routing grid interval set along the X direction.” (Ichiryu at 6:26-35).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, a precision in a finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:41-45).<br><br>“A standard cell according to the present invention comprises a plurality of gate electrodes and a plurality of dummy gate electrodes, wherein a cell width in the X direction in parallel with the power-supply wiring of the standard cell is an integral multiple of a minimum gate pitch of gate pitches of the gate electrodes and the dummy gate electrodes different to the routing grid interval along the X direction.” (Ichiryu at 6:46-52).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:58-62). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “The gate pitches of the standard cell are all preferably equal. Thereby, the pattern of the gate electrodes can impart a perfect regularity to the gate pitches, and the precision in the finished dimension of the gate electrodes can be further improved.” (Ichiryu at 6:66-7:3).<br><br>“Further, because the pattern of the gate electrodes can have the regularity, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be performed in each standard cell.” (Ichiryu at 8:21-24).<br><br>“Referring to reference symbols in FIG. 11, x1-x13 denote routing grids for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, y1-y8 denote routing grids disposed in parallel with the X direction and adjacent to one another in the Y direction, gx1-gx10 denote grids of gate pitches for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, C61, C62 and C63 are standard cells, O61, O62 and O63 are respective origins of the standard cells C61, C62 and C63, … G denotes a gate electrode, and DG denotes a dummy gate electrode.” (Ichiryu at 14:32-44).<br><br>“In the standard cells C61, C62 and C63, gate lengths and gate intervals of the gate electrode G and dummy gate electrode DG are constant, and a cell width of the standard cells C61, C62 and C63 in the X direction is an integral multiple of a minimum value of a gate pitch Gx (value of gate pitch=gate length+gate interval) (In FIG. 11, the cell width of the standard cells C61, C62 and C63 is three times as wide as Gx).” (Ichiryu at 14:45-51).<br><br>“Not only inside the respective standard cells C61, C62 and C63, but also among the standard cells C61, C62 and C63 to one another, the gate lengths and the gate intervals are equal in the patterns of the gate electrodes and the dummy gate electrodes.” (Ichiryu at 15:47-51).<br><br>“In the embodiment 5, the gate lengths are all equal in the gate electrodes and the dummy gate electrodes….” (Ichiryu at 16:10-11).<br><br>“In FIG. 14, a reference symbol C81 denotes a standard cell. The standard cell C81 comprises gate electrodes G, dummy gate electrodes DG and two gate electrodes G2 having a gate length different to |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | those of the gate electrode G and the dummy gate electrode DG, wherein a width of the gate electrode G2 is set so that a cell width of the standard cell C81 in the X direction is an integral multiple of the gate pitch Gx. In FIG. 14, the cell width of the standard cell C81 is nine times as wide as the gate pitch Gx. The width of the gate electrode G2 is thus set because a processing speed is expected to be faster when the cell width of each cell in the X direction is the integral multiple of the gate pitch Gx than when the cell width of each cell takes an arbitrary value in the placement using the conventional automatic placement & routing tool. However, the width of the gate electrode G2 is not necessarily set in the foregoing manner.” (Ichiryu at 16:15-30).<br><br>“In the constitution, the distance from the cell boundary of each standard cell to the gate electrode in the closest vicinity and the distance from the cell boundary of another standard cell adjacent thereto to the gate electrode in the closest vicinity are constant.” (Ichiryu at 16:65-17:2).<br><br>“For example, a distance from each of the cell boundary of the standard cells C61, C62 and C63 to the gate electrode in the X direction is ‘Gx-gate length/2’ and constant even in the constitution shown in FIG. 11 where the dummy gate electrodes DG are not provided. A distance between a transistor disposed at the end of each standard cell and the gate electrode G of the adjacent standard cell is ‘2Gx-gate length’ and constant. For example, even in the case where the dummy gate electrode DG is not provided in the constitution described referring to FIG. 11, the distance from each of the cell boundary of the respective standard cells C61, C62 and C63 to the gate electrode G located at the end of each of the standard cells in the X direction is constant at (Gx-gate length/2). Further, the distance from the gate electrode G located at the end of each of the standard cells to the gate electrode G located at the end of each of adjacent standard cells in the X direction is constant at (2Gx-gate length).” (Ichiryu at 17:6-22).<br><br>“Further, in the embodiment 6, the standard cells described in the embodiments 1 and 5 are used. The gate lengths and the gate intervals are thereby equal in the patterns of the gate electrodes of the placed standard cells C91, C92 and C93, which leads to the improvement of the precision in the finished dimension of the gate electrodes. The improvement of the precision in the finished |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | dimension of the gate electrodes can be realized not only inside each of the standard cells C91, C92 and C93 but also between the standard cells.” (Ichiryu at 18:1-9).<br><br>“[W]hen the standard cells are adjacently located, the gate lengths and the gate intervals in the patterns of the gate electrodes and the dummy gate electrodes are the same as when they are located alone.” (Ichiryu at 18:10-13).<br><br>F I G. 11<br>  <br><br><br>(Ichiryu Fig. 11). |

| '012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | *See also* Ichiryu at Figs. 1, 2, 3, 8, 12, 13, 14.<br><br>This limitation also would have been obvious to a person of ordinary skill in the art based on (1) Ichiryu alone; and/or (2) the teachings with respect to this claim element as detailed in the cover document of Respondent's invalidity contentions and Respondent's other invalidity charts. |
| [8.0] An integrated circuit device as recited in claim 2,<br><br>wherein each of a first number of the active linear conductive segments respectively includes a transistor gate electrode portion of a first size as measured in the first direction, and | At least under Tela's apparent infringement theory, Ichiryu discloses and/or renders obvious an integrated circuit device as recited in claim 2, wherein each of a first number of the active linear conductive segments respectively includes a transistor gate electrode portion of a first size as measured in the first direction.<br><br>Ichiryu discloses transistors in the larger diffusion regions in Figures 1, 2, 3, 8, 12, 13, and 14 are PMOS transistors, and the transistors in the smaller diffusion regions in those figures are NMOS transistors, and the length of the NMOS transistor gates are different than the length of the PMOS transistor gates. Therefore, there is a first number of the active linear conductive segments that include a transistor gate electrode portion of a first size (e.g. size of the PMOS transistor gate electrode portion). |

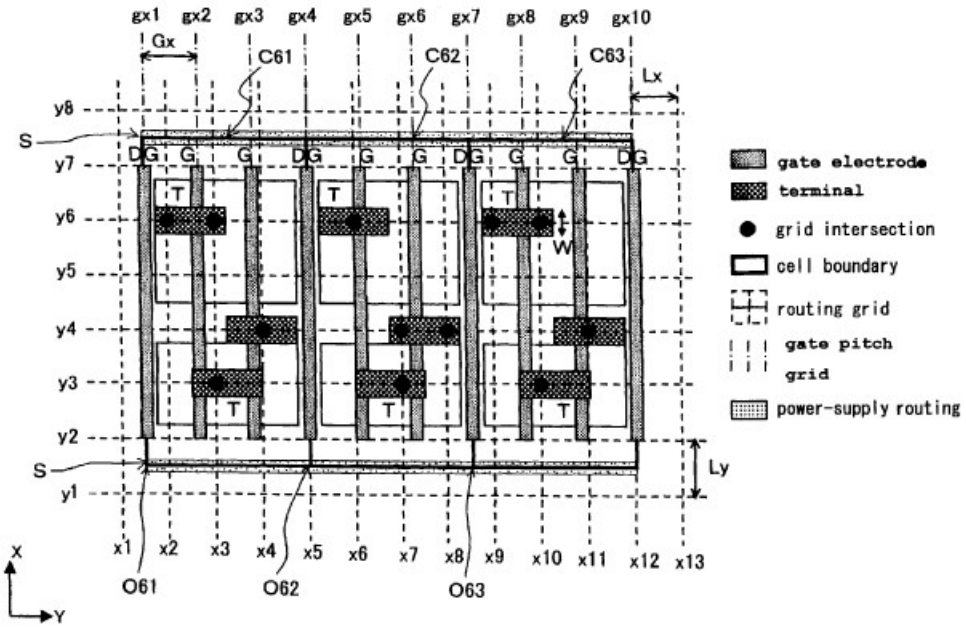
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | **Modified Fig. 11M**<br>  <br><br>*See, e.g.*:<br><br>“[A]s the miniaturization of the process [continues], a precision in a finished dimension of the gate electrode ultimately obtained is deteriorated by an optical proximity effect when an interval between the gate electrodes and gate lengths of the gate electrodes are irregular in their patterns. When the precision in the finished dimension of the gate electrode is deteriorated, performances of respective |

| '012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | transistors of the semiconductor integrated circuit are increasingly inconstant, which leads to an increased variation in a performance of the semiconductor integrate[d] circuit." (Ichiryu at 2:23-32).<br><br>"[A]s recited in No. H10-32253 of the Publication of the Unexamined Japanese Patent Applications, the interval and the length of the gate electrodes in each standard cell are set regular so that the OPC is processed per standard cell in the conventional technology." (Ichiryu at 2:37-41).<br><br>"The standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes…." (Ichiryu at 6:20-21).<br><br>"A standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes, wherein gate pitches of some of the gate electrodes are set to values different to the routing grid interval set along the X direction in parallel with the power-supply wiring of the standard cell, and a cell width along the X direction in parallel with the power-supply wiring of the standard cell is set to an integral multiple of a minimum value of the gate pitches of the gate electrodes set to the values different to the routing grid interval set along the X direction." (Ichiryu at 6:26-35).<br><br>"[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, a precision in a finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell." (Ichiryu at 6:41-45).<br><br>"A standard cell according to the present invention comprises a plurality of gate electrodes and a plurality of dummy gate electrodes, wherein a cell width in the X direction in parallel with the power-supply wiring of the standard cell is an integral multiple of a minimum gate pitch of gate pitches of the gate electrodes and the dummy gate electrodes different to the routing grid interval along the X direction." (Ichiryu at 6:46-52). |

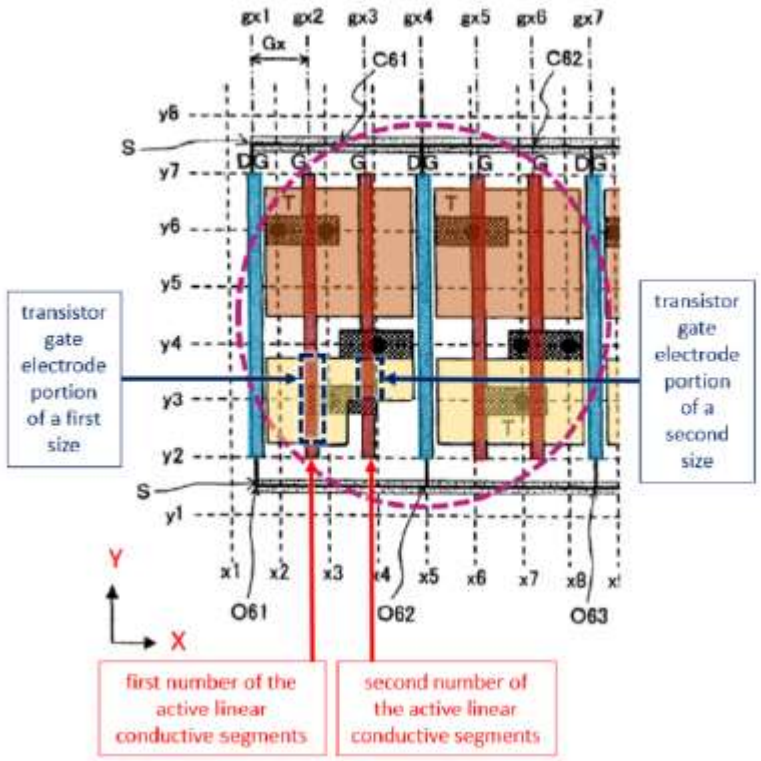
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:58-62).<br><br>“The gate pitches of the standard cell are all preferably equal. Thereby, the pattern of the gate electrodes can impart a perfect regularity to the gate pitches, and the precision in the finished dimension of the gate electrodes can be further improved.” (Ichiryu at 6:66-7:3).<br><br>“Further, because the pattern of the gate electrodes can have the regularity, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be performed in each standard cell.” (Ichiryu at 8:21-24).<br><br>“Referring to reference symbols in FIG. 11, x1-x13 denote routing grids for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, y1-y8 denote routing grids disposed in parallel with the X direction and adjacent to one another in the Y direction, gx1-gx10 denote grids of gate pitches for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, C61, C62 and C63 are standard cells, O61, O62 and O63 are respective origins of the standard cells C61, C62 and C63, … G denotes a gate electrode, and DG denotes a dummy gate electrode.” (Ichiryu at 14:32-44).<br><br>“In the standard cells C61, C62 and C63, gate lengths and gate intervals of the gate electrode G and dummy gate electrode DG are constant, and a cell width of the standard cells C61, C62 and C63 in the X direction is an integral multiple of a minimum value of a gate pitch Gx (value of gate pitch=gate length+gate interval) (In FIG. 11, the cell width of the standard cells C61, C62 and C63 is three times as wide as Gx).” (Ichiryu at 14:45-51).<br><br>“Not only inside the respective standard cells C61, C62 and C63, but also among the standard cells C61, C62 and C63 to one another, the gate lengths and the gate intervals are equal in the patterns of the gate electrodes and the dummy gate electrodes.” (Ichiryu at 15:47-51). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “In the embodiment 5, the gate lengths are all equal in the gate electrodes and the dummy gate electrodes….” (Ichiryu at 16:10-11).<br><br>“In FIG. 14, a reference symbol C81 denotes a standard cell. The standard cell C81 comprises gate electrodes G, dummy gate electrodes DG and two gate electrodes G2 having a gate length different to those of the gate electrode G and the dummy gate electrode DG, wherein a width of the gate electrode G2 is set so that a cell width of the standard cell C81 in the X direction is an integral multiple of the gate pitch Gx. In FIG. 14, the cell width of the standard cell C81 is nine times as wide as the gate pitch Gx. The width of the gate electrode G2 is thus set because a processing speed is expected to be faster when the cell width of each cell in the X direction is the integral multiple of the gate pitch Gx than when the cell width of each cell takes an arbitrary value in the placement using the conventional automatic placement & routing tool. However, the width of the gate electrode G2 is not necessarily set in the foregoing manner.” (Ichiryu at 16:15-30).<br><br>“As described, in the case of including the standard cell comprising the gate electrodes having the different gate lengths….” (Ichiryu at 16:32-34).<br><br>“In the constitution, the distance from the cell boundary of each standard cell to the gate electrode in the closest vicinity and the distance from the cell boundary of another standard cell adjacent thereto to the gate electrode in the closest vicinity are constant.” (Ichiryu at 16:65-17:2).<br><br>“For example, a distance from each of the cell boundary of the standard cells C61, C62 and C63 to the gate electrode in the X direction is ‘Gx-gate length/2’ and constant even in the constitution shown in FIG. 11 where the dummy gate electrodes DG are not provided. A distance between a transistor disposed at the end of each standard cell and the gate electrode G of the adjacent standard cell is ‘2Gx-gate length’ and constant. For example, even in the case where the dummy gate electrode DG is not provided in the constitution described referring to FIG. 11, the distance from each of the cell boundary of the respective standard cells C61, C62 and C63 to the gate electrode G located at the end of each of the standard cells in the X direction is constant at (Gx-gate length/2). Further, the distance from the gate electrode G located at the end of each of the standard cells to the gate electrode G |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | located at the end of each of adjacent standard cells in the X direction is constant at (2Gx-gate length).” (Ichiryu at 17:6-22).<br><br>“Further, in the embodiment 6, the standard cells described in the embodiments 1 and 5 are used. The gate lengths and the gate intervals are thereby equal in the patterns of the gate electrodes of the placed standard cells C91, C92 and C93, which leads to the improvement of the precision in the finished dimension of the gate electrodes. The improvement of the precision in the finished dimension of the gate electrodes can be realized not only inside each of the standard cells C91, C92 and C93 but also between the standard cells.” (Ichiryu at 18:1-9).<br><br>“[W]hen the standard cells are adjacently located, the gate lengths and the gate intervals in the patterns of the gate electrodes and the dummy gate electrodes are the same as when they are located alone.” (Ichiryu at 18:10-13). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | F I G. 11<br>  <br><br>(Ichiryu Fig. 11).<br>*See also* Ichiryu Figs. 1, 2, 3, 8, 12, 13, 14.<br>This limitation also would have been obvious to a person of ordinary skill in the art based on (1) Ichiryu alone; and/or (2) the teachings with respect to this claim element as detailed in the cover document of Respondent’s invalidity contentions and Respondent’s other invalidity charts. |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| [8.1] wherein each of a second number of the active linear conductive segments respectively includes a transistor gate electrode portion of a second size as measured in the first direction, wherein the second size is different than the first size. | At least under Tela’s apparent infringement theory, Ichiryu discloses and/or renders obvious wherein each of a second number of the active linear conductive segments respectively includes a transistor gate electrode portion of a second size as measured in the first direction, wherein the second size is different than the first size.<br><br>Ichiryu discloses transistors in the larger diffusion regions in Figures 1, 2, 3, 8, 12, 13, and 14 are PMOS transistors, and the transistors in the smaller diffusion regions in those figures are NMOS transistors, and the length of the NMOS transistor gates are different than the length of the PMOS transistor gates. |

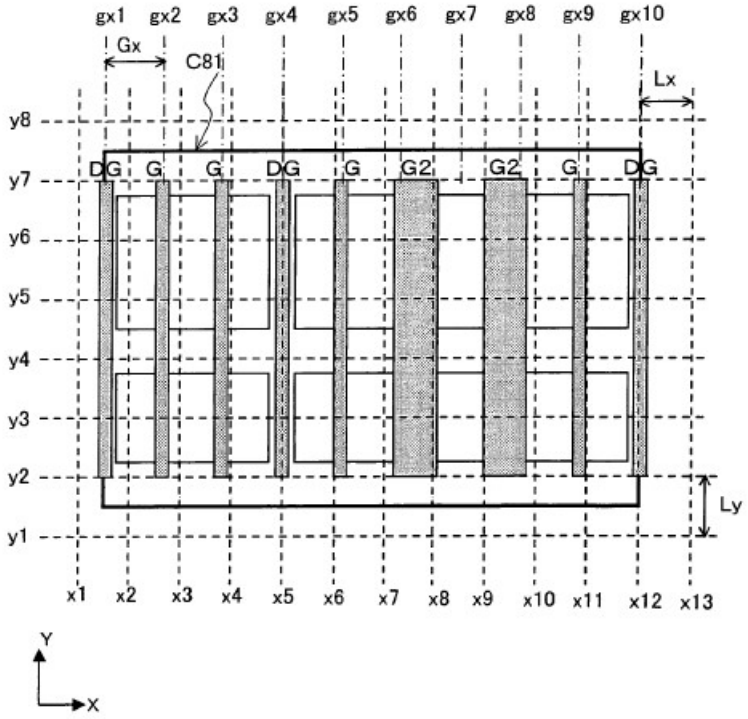
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | **Modified Fig. 11M**<br>  <br><br>*See, e.g.*:<br><br>“[A]s the miniaturization of the process [continues], a precision in a finished dimension of the gate electrode ultimately obtained is deteriorated by an optical proximity effect when an interval between the gate electrodes and gate lengths of the gate electrodes are irregular in their patterns. When the precision in the finished dimension of the gate electrode is deteriorated, performances of respective |

| '012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | transistors of the semiconductor integrated circuit are increasingly inconstant, which leads to an increased variation in a performance of the semiconductor integrate[d] circuit." (Ichiryu at 2:23-32).<br><br>"[A]s recited in No. H10-32253 of the Publication of the Unexamined Japanese Patent Applications, the interval and the length of the gate electrodes in each standard cell are set regular so that the OPC is processed per standard cell in the conventional technology." (Ichiryu at 2:37-41).<br><br>"The standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes…." (Ichiryu at 6:20-21).<br><br>"A standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes, wherein gate pitches of some of the gate electrodes are set to values different to the routing grid interval set along the X direction in parallel with the power-supply wiring of the standard cell, and a cell width along the X direction in parallel with the power-supply wiring of the standard cell is set to an integral multiple of a minimum value of the gate pitches of the gate electrodes set to the values different to the routing grid interval set along the X direction." (Ichiryu at 6:26-35).<br><br>"[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, a precision in a finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell." (Ichiryu at 6:41-45).<br><br>"A standard cell according to the present invention comprises a plurality of gate electrodes and a plurality of dummy gate electrodes, wherein a cell width in the X direction in parallel with the power-supply wiring of the standard cell is an integral multiple of a minimum gate pitch of gate pitches of the gate electrodes and the dummy gate electrodes different to the routing grid interval along the X direction." (Ichiryu at 6:46-52). |

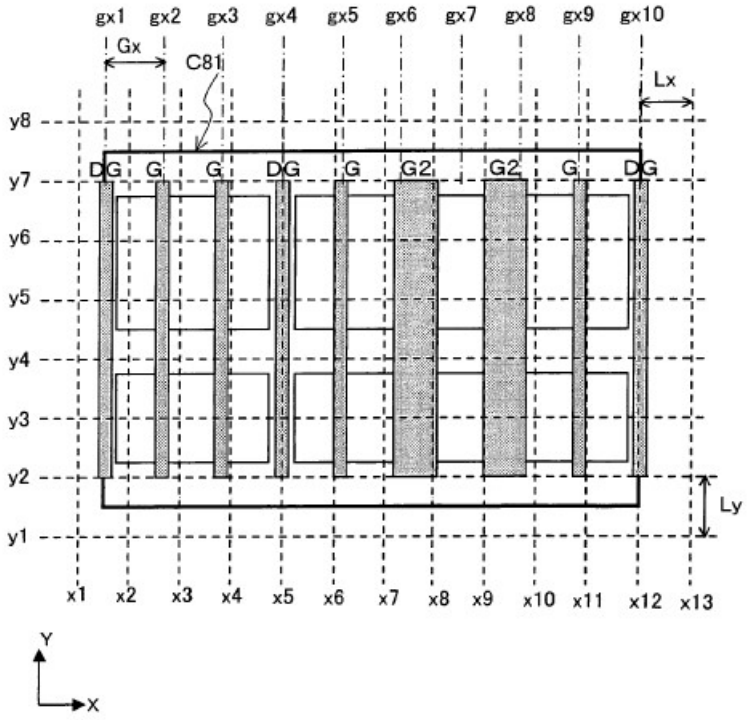
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:58-62).<br><br>“The gate pitches of the standard cell are all preferably equal. Thereby, the pattern of the gate electrodes can impart a perfect regularity to the gate pitches, and the precision in the finished dimension of the gate electrodes can be further improved.” (Ichiryu at 6:66-7:3).<br><br>“Further, because the pattern of the gate electrodes can have the regularity, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be performed in each standard cell.” (Ichiryu at 8:21-24).<br><br>“FIG. 14 is a layout of a standard cell including gate electrodes having different gate lengths in the embodiment 5.” (Ichiryu at 9:4-5).<br><br>“Referring to reference symbols in FIG. 11, x1-x13 denote routing grids for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, y1-y8 denote routing grids disposed in parallel with the X direction and adjacent to one another in the Y direction, gx1-gx10 denote grids of gate pitches for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, C61, C62 and C63 are standard cells, O61, O62 and O63 are respective origins of the standard cells C61, C62 and C63, … G denotes a gate electrode, and DG denotes a dummy gate electrode.” (Ichiryu at 14:32-44).<br><br>“In the standard cells C61, C62 and C63, gate lengths and gate intervals of the gate electrode G and dummy gate electrode DG are constant, and a cell width of the standard cells C61, C62 and C63 in the X direction is an integral multiple of a minimum value of a gate pitch Gx (value of gate pitch=gate length+gate interval) (In FIG. 11, the cell width of the standard cells C61, C62 and C63 is three times as wide as Gx).” (Ichiryu at 14:45-51). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “Not only inside the respective standard cells C61, C62 and C63, but also among the standard cells C61, C62 and C63 to one another, the gate lengths and the gate intervals are equal in the patterns of the gate electrodes and the dummy gate electrodes.” (Ichiryu at 15:47-51).<br><br>“In the embodiment 5, the gate lengths are all equal in the gate electrodes and the dummy gate electrodes….” (Ichiryu at 16:10-11).<br><br>“In FIG. 14, a reference symbol C81 denotes a standard cell. The standard cell C81 comprises gate electrodes G, dummy gate electrodes DG and two gate electrodes G2 having a gate length different to those of the gate electrode G and the dummy gate electrode DG, wherein a width of the gate electrode G2 is set so that a cell width of the standard cell C81 in the X direction is an integral multiple of the gate pitch Gx. In FIG. 14, the cell width of the standard cell C81 is nine times as wide as the gate pitch Gx. The width of the gate electrode G2 is thus set because a processing speed is expected to be faster when the cell width of each cell in the X direction is the integral multiple of the gate pitch Gx than when the cell width of each cell takes an arbitrary value in the placement using the conventional automatic placement & routing tool. However, the width of the gate electrode G2 is not necessarily set in the foregoing manner.” (Ichiryu at 16:15-30).<br><br>“As described, in the case of including the standard cell comprising the gate electrodes having the different gate lengths….” (Ichiryu at 16:32-34).<br><br>“In the constitution, the distance from the cell boundary of each standard cell to the gate electrode in the closest vicinity and the distance from the cell boundary of another standard cell adjacent thereto to the gate electrode in the closest vicinity are constant.” (Ichiryu at 16:65-17:2).<br><br>“For example, a distance from each of the cell boundary of the standard cells C61, C62 and C63 to the gate electrode in the X direction is ‘Gx-gate length/2’ and constant even in the constitution shown in FIG. 11 where the dummy gate electrodes DG are not provided. A distance between a transistor disposed at the end of each standard cell and the gate electrode G of the adjacent standard cell is ‘2Gx-gate length’ and constant. For example, even in the case where the dummy gate electrode DG is not provided in the constitution described referring to FIG. 11, the distance from each of the cell |

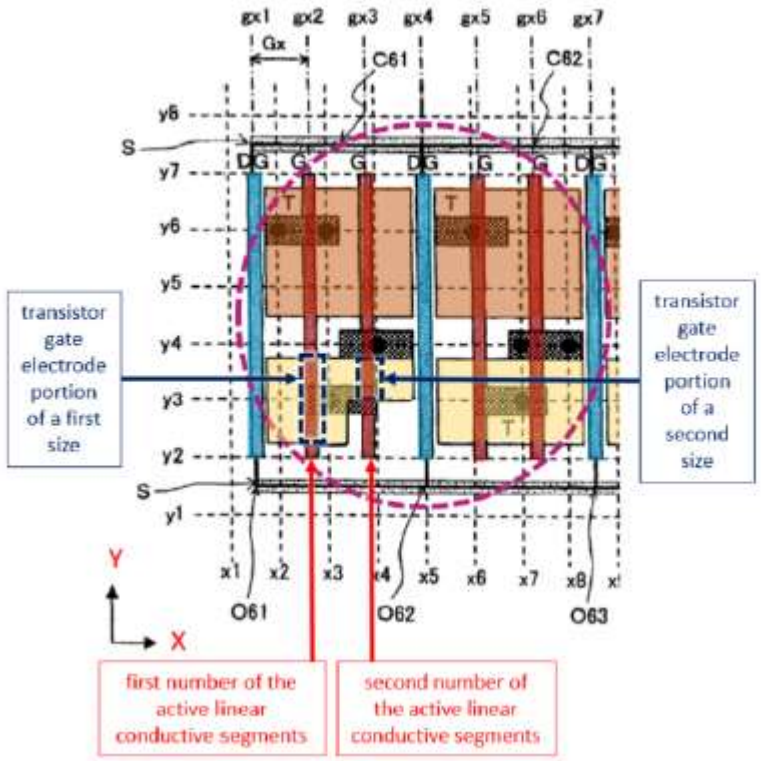
| '012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | boundary of the respective standard cells C61, C62 and C63 to the gate electrode G located at the end of each of the standard cells in the X direction is constant at (Gx-gate length/2). Further, the distance from the gate electrode G located at the end of each of the standard cells to the gate electrode G located at the end of each of adjacent standard cells in the X direction is constant at (2Gx-gate length)." (Ichiryu at 17:6-22).<br><br>"Further, in the embodiment 6, the standard cells described in the embodiments 1 and 5 are used. The gate lengths and the gate intervals are thereby equal in the patterns of the gate electrodes of the placed standard cells C91, C92 and C93, which leads to the improvement of the precision in the finished dimension of the gate electrodes. The improvement of the precision in the finished dimension of the gate electrodes can be realized not only inside each of the standard cells C91, C92 and C93 but also between the standard cells." (Ichiryu at 18:1-9).<br><br>"[W]hen the standard cells are adjacently located, the gate lengths and the gate intervals in the patterns of the gate electrodes and the dummy gate electrodes are the same as when they are located alone." (Ichiryu at 18:10-13). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | F I G. 14<br>  <br><br>(Ichiryu Fig. 14).<br>*See also* Ichiryu at Figs. 1, 2, 3, 8, 11, 12, 13. |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | Ichiryu discloses transistors in the larger diffusion regions in Figures 1, 2, 3, 8, 12, 13, and 14 are PMOS transistors, and the transistors in the smaller diffusion regions in those figures are NMOS transistors, and the length of the NMOS transistor gates are different than the length of the PMOS transistor gates.<br><br>*See, e.g.*:<br><br>“FIG. 14 is a layout of a standard cell including gate electrodes having different gate lengths in the embodiment 5.” (Ichiryu at 9:4-5).<br><br>“Referring to reference symbols in FIG. 11, x1-x13 denote routing grids for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, y1-y8 denote routing grids disposed in parallel with the X direction and adjacent to one another in the Y direction, gx1-gx10 denote grids of gate pitches for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, C61, C62 and C63 are standard cells, O61, O62 and O63 are respective origins of the standard cells C61, C62 and C63, … G denotes a gate electrode, and DG denotes a dummy gate electrode.” (Ichiryu at 14:32-44).<br><br>“In FIG. 14, a reference symbol C81 denotes a standard cell. The standard cell C81 comprises gate electrodes G, dummy gate electrodes DG and two gate electrodes G2 having a gate length different to those of the gate electrode G and the dummy gate electrode DG, wherein a width of the gate electrode G2 is set so that a cell width of the standard cell C81 in the X direction is an integral multiple of the gate pitch Gx. In FIG. 14, the cell width of the standard cell C81 is nine times as wide as the gate pitch Gx. The width of the gate electrode G2 is thus set because a processing speed is expected to be faster when the cell width of each cell in the X direction is the integral multiple of the gate pitch Gx than when the cell width of each cell takes an arbitrary value in the placement using the conventional automatic placement & routing tool. However, the width of the gate electrode G2 is not necessarily set in the foregoing manner.” (Ichiryu at 16:15-30). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “As described, in the case of including the standard cell comprising the gate electrodes having the different gate lengths….” (Ichiryu at 16:32-34).<br><br>F I G. 14<br><br>  |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | (Ichiryu Fig. 14).<br><br>*See also* Ichiryu at Figs. 1, 2, 3, 8, 11, 12, 13.<br><br>Alternatively, either the PMOS or NMOS diffusion could be L-shaped, such that one of the gates of the NMOS or PMOS transistors has a unique length.<br><br>This limitation also would have been obvious to a person of ordinary skill in the art based on (1) Ichiryu alone; and/or (2) the teachings with respect to this claim element as detailed in the cover document of Respondent’s invalidity contentions and Respondent’s other invalidity charts. |
| [9.0] An integrated circuit device as recited in claim 8,<br><br>wherein the first number is equal to the second number. | At least under Tela’s apparent infringement theory, Ichiryu discloses and/or renders obvious an integrated circuit device as recited in claim 8, wherein the first number is equal to the second number. |

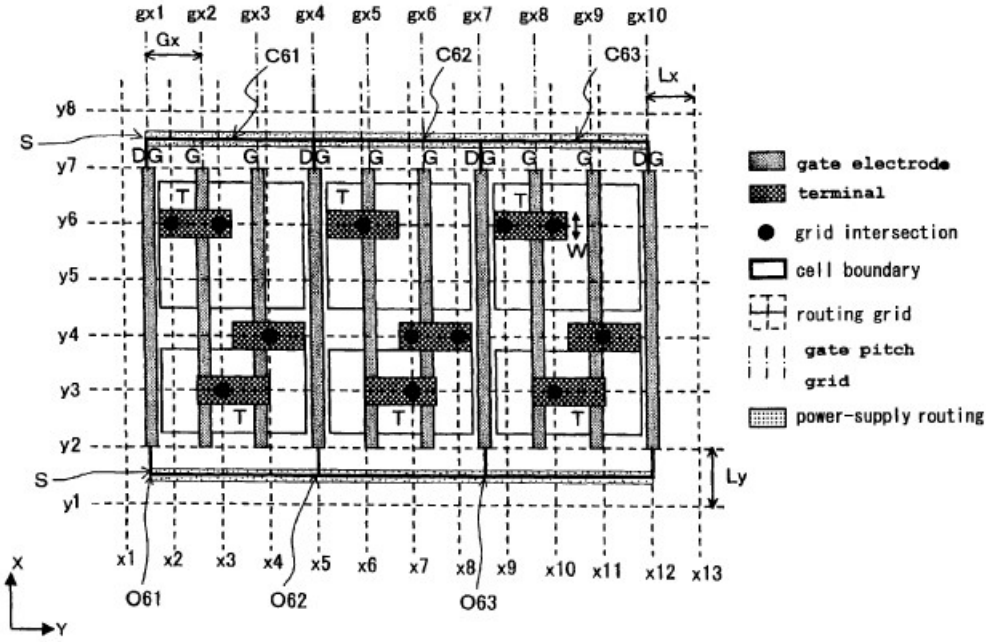
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | **Modified Fig. 11M**<br>  <br><br>*See, e.g.*:<br><br>“[A]s the miniaturization of the process [continues], a precision in a finished dimension of the gate electrode ultimately obtained is deteriorated by an optical proximity effect when an interval between the gate electrodes and gate lengths of the gate electrodes are irregular in their patterns. When the precision in the finished dimension of the gate electrode is deteriorated, performances of respective |

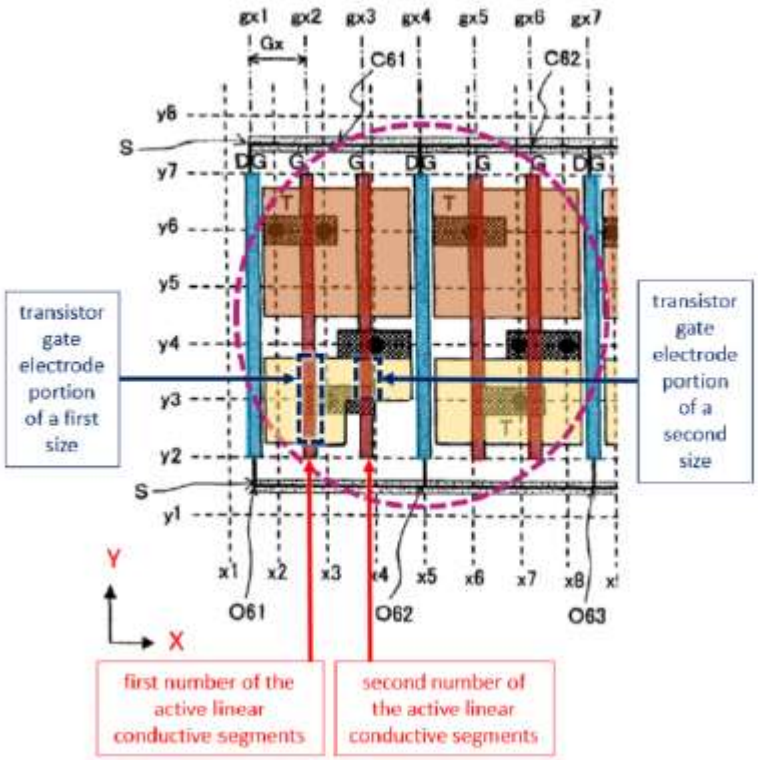
| '012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | transistors of the semiconductor integrated circuit are increasingly inconstant, which leads to an increased variation in a performance of the semiconductor integrate[d] circuit." (Ichiryu at 2:23-32).<br><br>"[A]s recited in No. H10-32253 of the Publication of the Unexamined Japanese Patent Applications, the interval and the length of the gate electrodes in each standard cell are set regular so that the OPC is processed per standard cell in the conventional technology." (Ichiryu at 2:37-41).<br><br>"The standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes…." (Ichiryu at 6:20-21).<br><br>"A standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes, wherein gate pitches of some of the gate electrodes are set to values different to the routing grid interval set along the X direction in parallel with the power-supply wiring of the standard cell, and a cell width along the X direction in parallel with the power-supply wiring of the standard cell is set to an integral multiple of a minimum value of the gate pitches of the gate electrodes set to the values different to the routing grid interval set along the X direction." (Ichiryu at 6:26-35).<br><br>"[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, a precision in a finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell." (Ichiryu at 6:41-45).<br><br>"A standard cell according to the present invention comprises a plurality of gate electrodes and a plurality of dummy gate electrodes, wherein a cell width in the X direction in parallel with the power-supply wiring of the standard cell is an integral multiple of a minimum gate pitch of gate pitches of the gate electrodes and the dummy gate electrodes different to the routing grid interval along the X direction." (Ichiryu at 6:46-52). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:58-62).<br><br>“The gate pitches of the standard cell are all preferably equal. Thereby, the pattern of the gate electrodes can impart a perfect regularity to the gate pitches, and the precision in the finished dimension of the gate electrodes can be further improved.” (Ichiryu at 6:66-7:3).<br><br>“Further, because the pattern of the gate electrodes can have the regularity, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be performed in each standard cell.” (Ichiryu at 8:21-24).<br><br>“Referring to reference symbols in FIG. 11, x1-x13 denote routing grids for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, y1-y8 denote routing grids disposed in parallel with the X direction and adjacent to one another in the Y direction, gx1-gx10 denote grids of gate pitches for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, C61, C62 and C63 are standard cells, O61, O62 and O63 are respective origins of the standard cells C61, C62 and C63, … G denotes a gate electrode, and DG denotes a dummy gate electrode.” (Ichiryu at 14:32-44).<br><br>“In the standard cells C61, C62 and C63, gate lengths and gate intervals of the gate electrode G and dummy gate electrode DG are constant, and a cell width of the standard cells C61, C62 and C63 in the X direction is an integral multiple of a minimum value of a gate pitch Gx (value of gate pitch=gate length+gate interval) (In FIG. 11, the cell width of the standard cells C61, C62 and C63 is three times as wide as Gx).” (Ichiryu at 14:45-51).<br><br>“Not only inside the respective standard cells C61, C62 and C63, but also among the standard cells C61, C62 and C63 to one another, the gate lengths and the gate intervals are equal in the patterns of the gate electrodes and the dummy gate electrodes.” (Ichiryu at 15:47-51). |

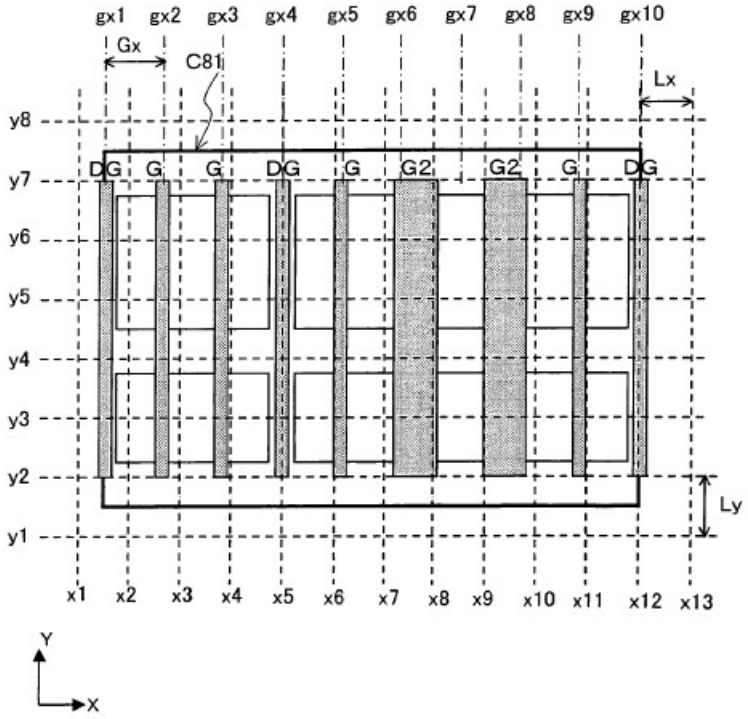
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “In the embodiment 5, the gate lengths are all equal in the gate electrodes and the dummy gate electrodes….” (Ichiryu at 16:10-11).<br><br>“In FIG. 14, a reference symbol C81 denotes a standard cell. The standard cell C81 comprises gate electrodes G, dummy gate electrodes DG and two gate electrodes G2 having a gate length different to those of the gate electrode G and the dummy gate electrode DG, wherein a width of the gate electrode G2 is set so that a cell width of the standard cell C81 in the X direction is an integral multiple of the gate pitch Gx. In FIG. 14, the cell width of the standard cell C81 is nine times as wide as the gate pitch Gx. The width of the gate electrode G2 is thus set because a processing speed is expected to be faster when the cell width of each cell in the X direction is the integral multiple of the gate pitch Gx than when the cell width of each cell takes an arbitrary value in the placement using the conventional automatic placement & routing tool. However, the width of the gate electrode G2 is not necessarily set in the foregoing manner.” (Ichiryu at 16:15-30).<br><br>“As described, in the case of including the standard cell comprising the gate electrodes having the different gate lengths….” (Ichiryu at 16:32-34).<br><br>“In the constitution, the distance from the cell boundary of each standard cell to the gate electrode in the closest vicinity and the distance from the cell boundary of another standard cell adjacent thereto to the gate electrode in the closest vicinity are constant.” (Ichiryu at 16:65-17:2).<br><br>“For example, a distance from each of the cell boundary of the standard cells C61, C62 and C63 to the gate electrode in the X direction is ‘Gx-gate length/2’ and constant even in the constitution shown in FIG. 11 where the dummy gate electrodes DG are not provided. A distance between a transistor disposed at the end of each standard cell and the gate electrode G of the adjacent standard cell is ‘2Gx-gate length’ and constant. For example, even in the case where the dummy gate electrode DG is not provided in the constitution described referring to FIG. 11, the distance from each of the cell boundary of the respective standard cells C61, C62 and C63 to the gate electrode G located at the end of each of the standard cells in the X direction is constant at (Gx-gate length/2). Further, the distance from the gate electrode G located at the end of each of the standard cells to the gate electrode G |

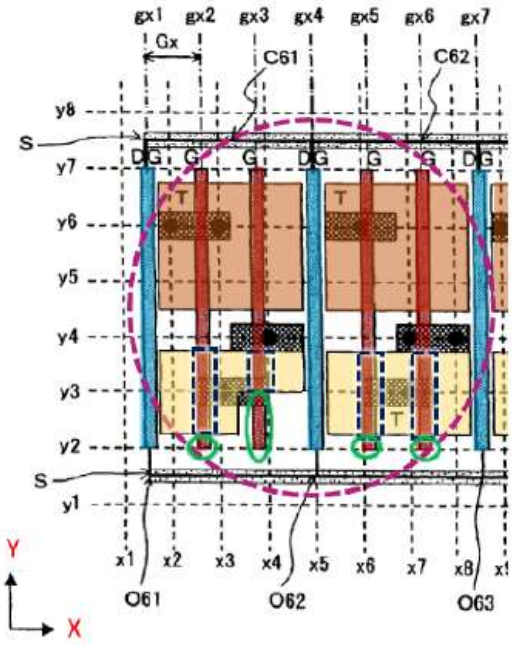
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | located at the end of each of adjacent standard cells in the X direction is constant at (2Gx-gate length).” (Ichiryu at 17:6-22).<br><br>“Further, in the embodiment 6, the standard cells described in the embodiments 1 and 5 are used. The gate lengths and the gate intervals are thereby equal in the patterns of the gate electrodes of the placed standard cells C91, C92 and C93, which leads to the improvement of the precision in the finished dimension of the gate electrodes. The improvement of the precision in the finished dimension of the gate electrodes can be realized not only inside each of the standard cells C91, C92 and C93 but also between the standard cells.” (Ichiryu at 18:1-9).<br><br>“[W]hen the standard cells are adjacently located, the gate lengths and the gate intervals in the patterns of the gate electrodes and the dummy gate electrodes are the same as when they are located alone.” (Ichiryu at 18:10-13). |

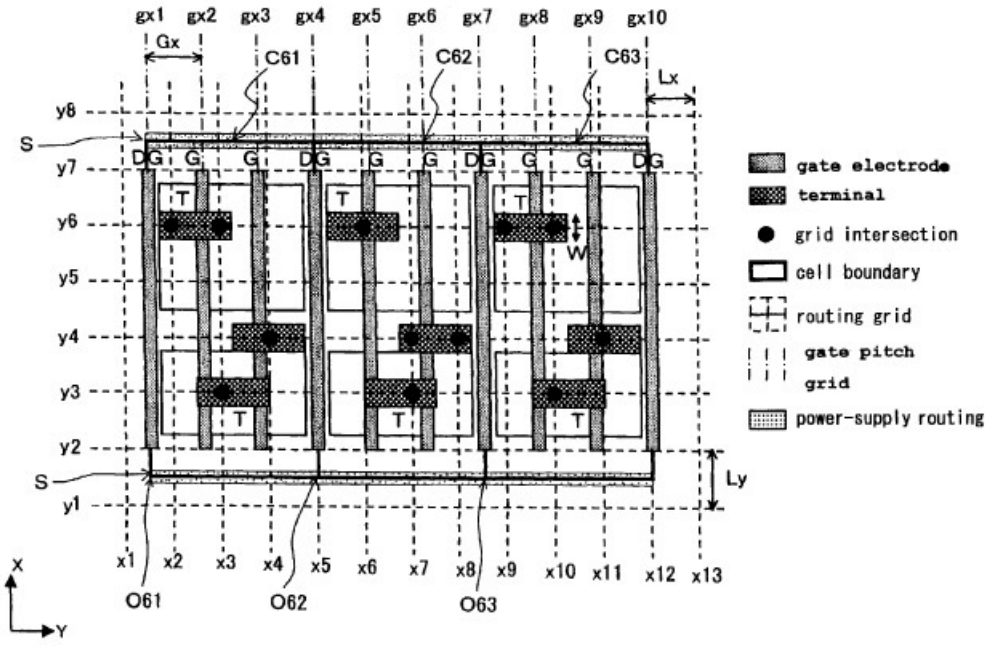
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | F I G. 11<br>  <br><br>(Ichiryu Fig. 11).<br>*See also* Ichiryu Figs. 1, 2, 3, 8, 12, 13, 14.<br>This limitation also would have been obvious to a person of ordinary skill in the art based on (1) Ichiryu alone; and/or (2) the teachings with respect to this claim element as detailed in the cover document of Respondent’s invalidity contentions and Respondent’s other invalidity charts. |

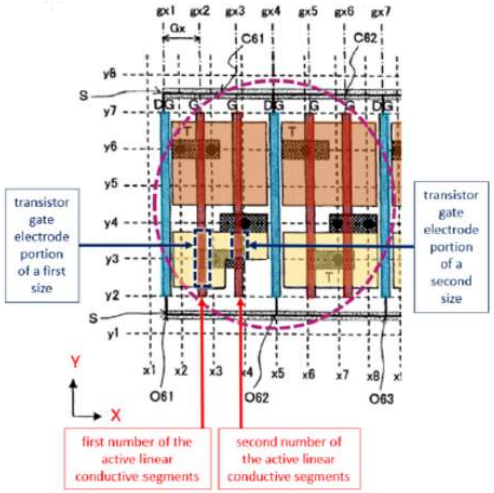
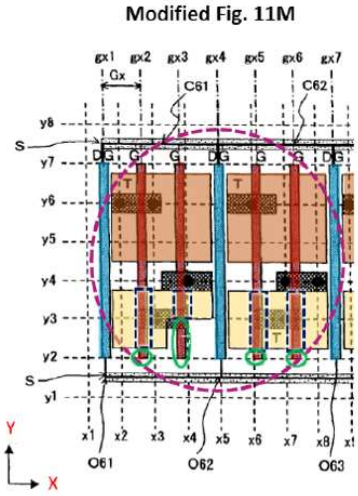
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| [10.0] An integrated circuit device as recited in claim 8,<br><br>wherein the first size is larger than the second size. | At least under Tela’s apparent infringement theory, Ichiryu discloses and/or renders obvious an integrated circuit device as recited in claim 8, wherein the first size is larger than the second size.<br><br>**Modified Fig. 11M**<br>  <br><br>*See, e.g.*:<br><br>“FIG. 14 is a layout of a standard cell including gate electrodes having different gate lengths in the embodiment 5.” (Ichiryu at 9:4-5). |

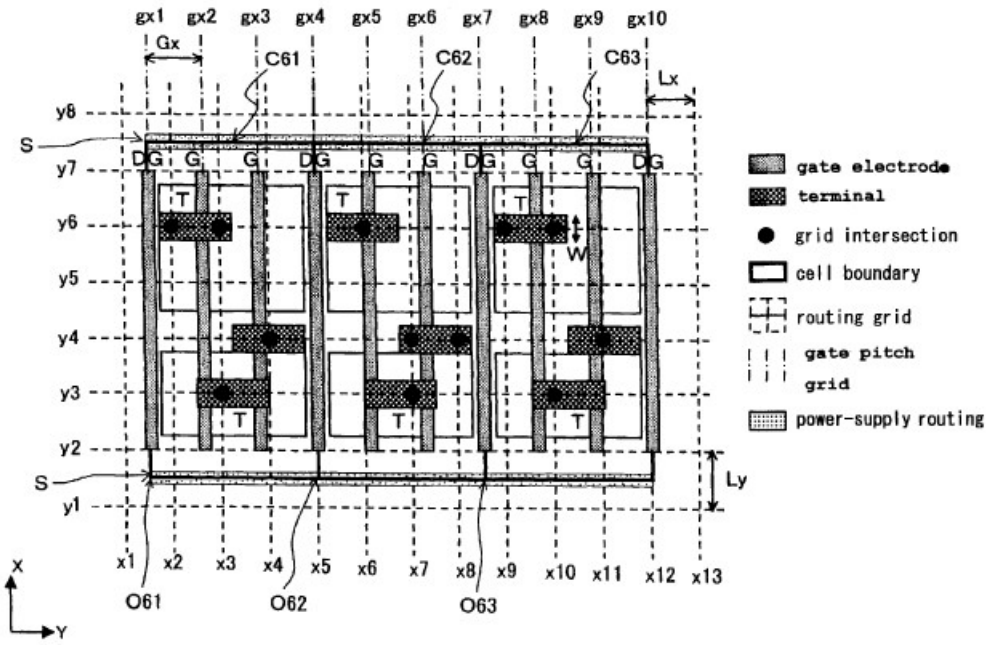
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “Referring to reference symbols in FIG. 11, x1-x13 denote routing grids for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, y1-y8 denote routing grids disposed in parallel with the X direction and adjacent to one another in the Y direction, gx1-gx10 denote grids of gate pitches for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, C61, C62 and C63 are standard cells, O61, O62 and O63 are respective origins of the standard cells C61, C62 and C63, … G denotes a gate electrode, and DG denotes a dummy gate electrode.” (Ichiryu at 14:32-44).<br><br>“In FIG. 14, a reference symbol C81 denotes a standard cell. The standard cell C81 comprises gate electrodes G, dummy gate electrodes DG and two gate electrodes G2 having a gate length different to those of the gate electrode G and the dummy gate electrode DG, wherein a width of the gate electrode G2 is set so that a cell width of the standard cell C81 in the X direction is an integral multiple of the gate pitch Gx. In FIG. 14, the cell width of the standard cell C81 is nine times as wide as the gate pitch Gx. The width of the gate electrode G2 is thus set because a processing speed is expected to be faster when the cell width of each cell in the X direction is the integral multiple of the gate pitch Gx than when the cell width of each cell takes an arbitrary value in the placement using the conventional automatic placement & routing tool. However, the width of the gate electrode G2 is not necessarily set in the foregoing manner.” (Ichiryu at 16:15-30).<br><br>“As described, in the case of including the standard cell comprising the gate electrodes having the different gate lengths….” (Ichiryu at 16:32-34). |

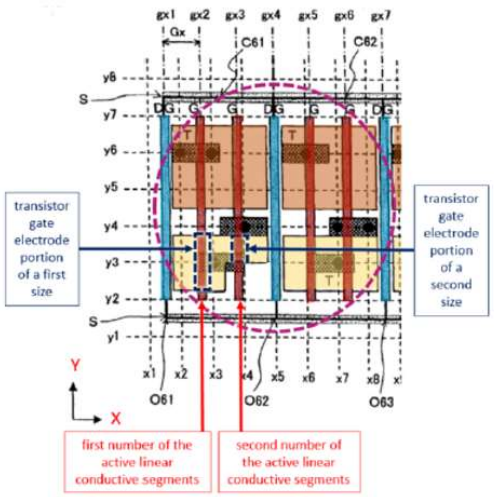
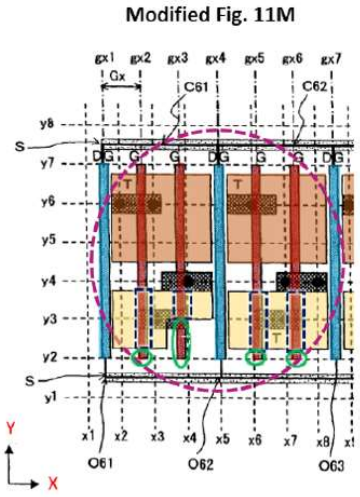
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | F I G. 14<br>  <br><br>(Ichiryu Fig. 14).<br>*See also* Ichiryu at Figs. 1, 2, 3, 8, 11, 12, 13. |

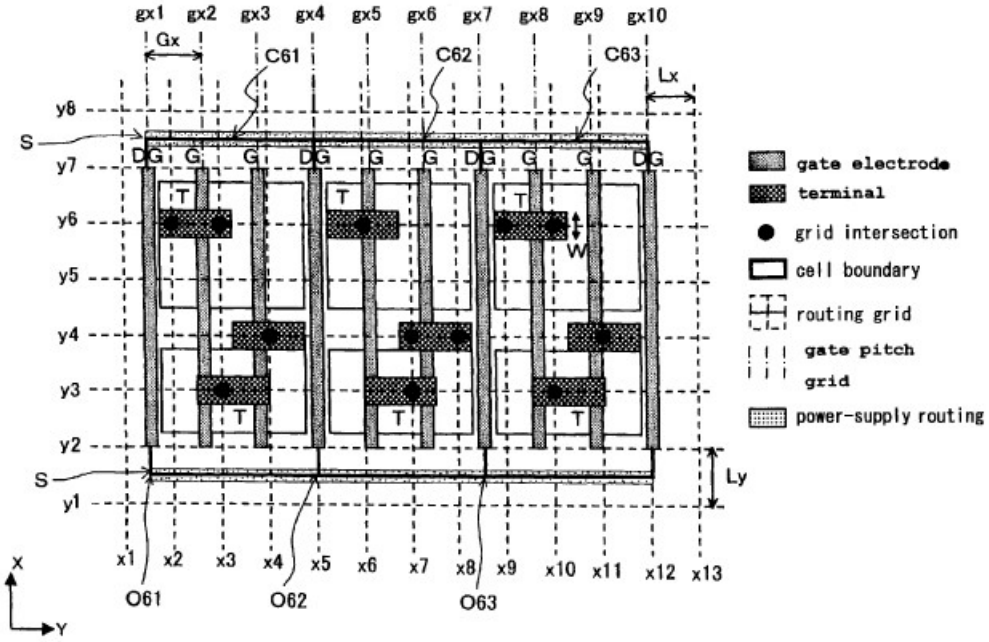
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | This limitation also would have been obvious to a person of ordinary skill in the art based on (1) Ichiryu alone; and/or (2) the teachings with respect to this claim element as detailed in the cover document of Respondent’s invalidity contentions and Respondent’s other invalidity charts. |
| [11.0] An integrated circuit device as recited in claim 8,<br><br>wherein each of the active linear conductive segments respectively includes a uniformity extending portion that extends in the first direction away from its transistor gate electrode portion. | At least under Tela’s apparent infringement theory, Ichiryu discloses and/or renders obvious an integrated circuit device as recited in claim 8, wherein each of the active linear conductive segments respectively includes a uniformity extending portion that extends in the first direction away from its transistor gate electrode portion.<br><br>**Modified Fig. 11M**<br>  <br> |

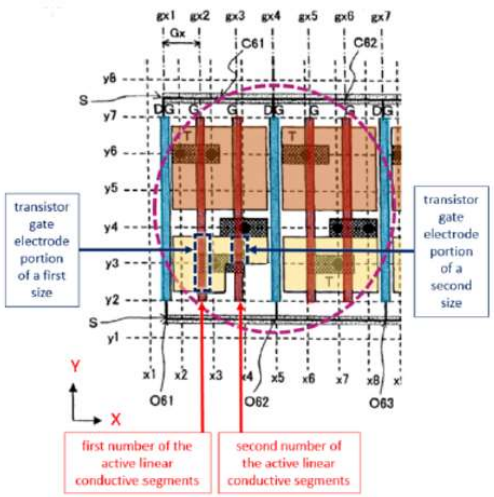
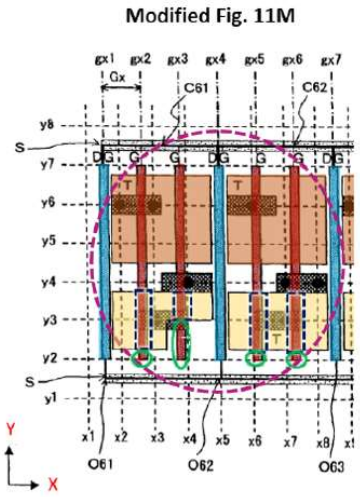
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | Ichiryu depicts transistors that have extending portions, which are the portions of the gate structure that extend beyond the diffusion region.<br><br>*See, e.g.*:<br><br>F I G. 11<br>  <br><br><br>(Ichiryu Fig. 11). |

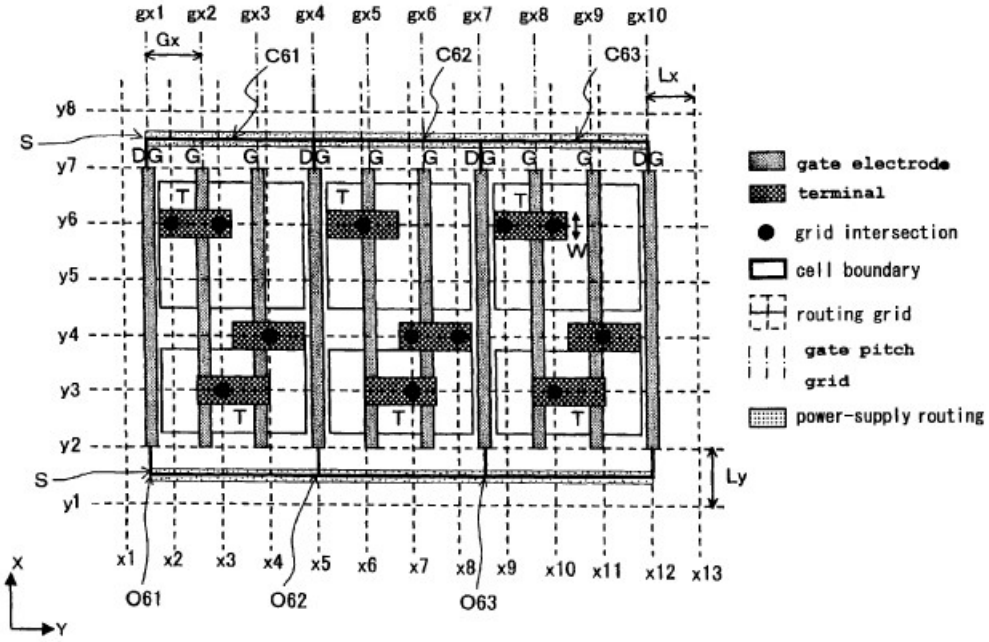
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | *See also* Ichiryu Figs. 1, 2, 3, 8, 12, 13, 14.<br><br>This limitation also would have been obvious to a person of ordinary skill in the art based on (1) Ichiryu alone; and/or (2) the teachings with respect to this claim element as detailed in the cover document of Respondent’s invalidity contentions and Respondent’s other invalidity charts. |
| [12.0] An integrated circuit device as recited in claim 11,<br><br>wherein the uniformity extending portion of each of the first number of the active linear conductive segments has a first length as measured in the first direction, | At least under Tela’s apparent infringement theory, Ichiryu discloses and/or renders obvious an integrated circuit device as recited in claim 11, wherein the uniformity extending portion of each of the first number of the active linear conductive segments has a first length as measured in the first direction.<br><br>Ichiryu depicts transistors that have extending portions.<br><br>Modified Fig. 11M<br>  <br><br>Modified Fig. 11M<br>  <br>*See, e.g.*: |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | F I G. 11<br>  <br><br>(Ichiryu Fig. 11).<br>*See also* Ichiryu Figs. 1, 2, 3, 8, 12, 13, 14.<br>This limitation also would have been obvious to a person of ordinary skill in the art based on (1) Ichiryu alone; and/or (2) the teachings with respect to this claim element as detailed in the cover document of Respondent’s invalidity contentions and Respondent’s other invalidity charts. |

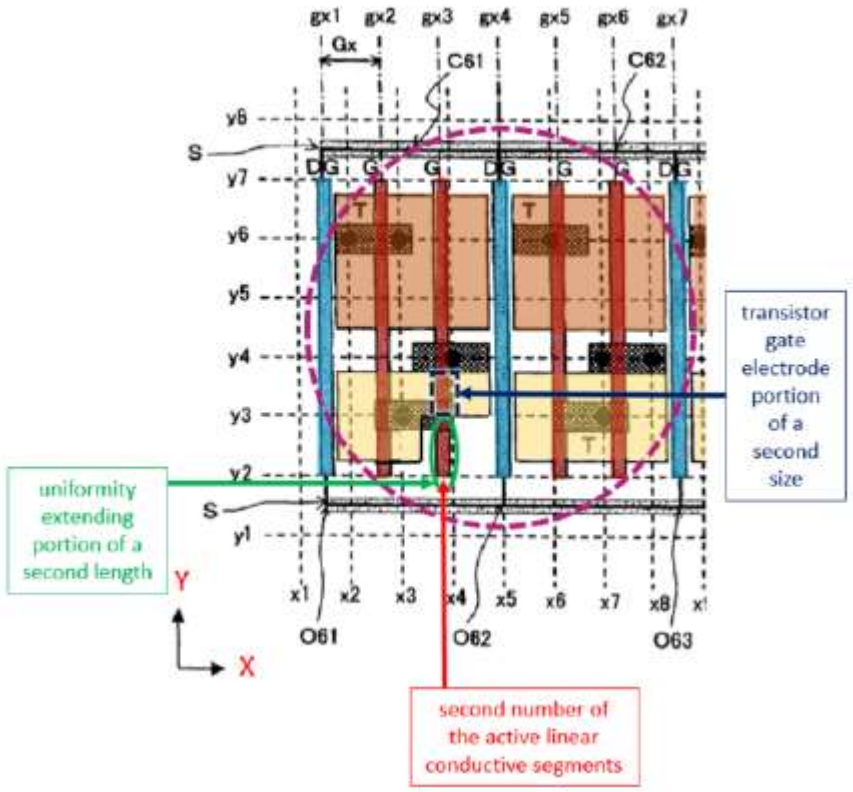
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| [12.1] wherein the uniformity extending portion of each of the second number of the active linear conductive segments has a second length as measured in the first direction, and | At least under Tela’s apparent infringement theory, Ichiryu discloses and/or renders obvious wherein the uniformity extending portion of each of the second number of the active linear conductive segments has a second length as measured in the first direction.<br><br>Ichiryu depicts transistors that have extending portions.<br><br>Modified Fig. 11M<br>  <br><br>Modified Fig. 11M<br>  <br><br>*See, e.g.*: |

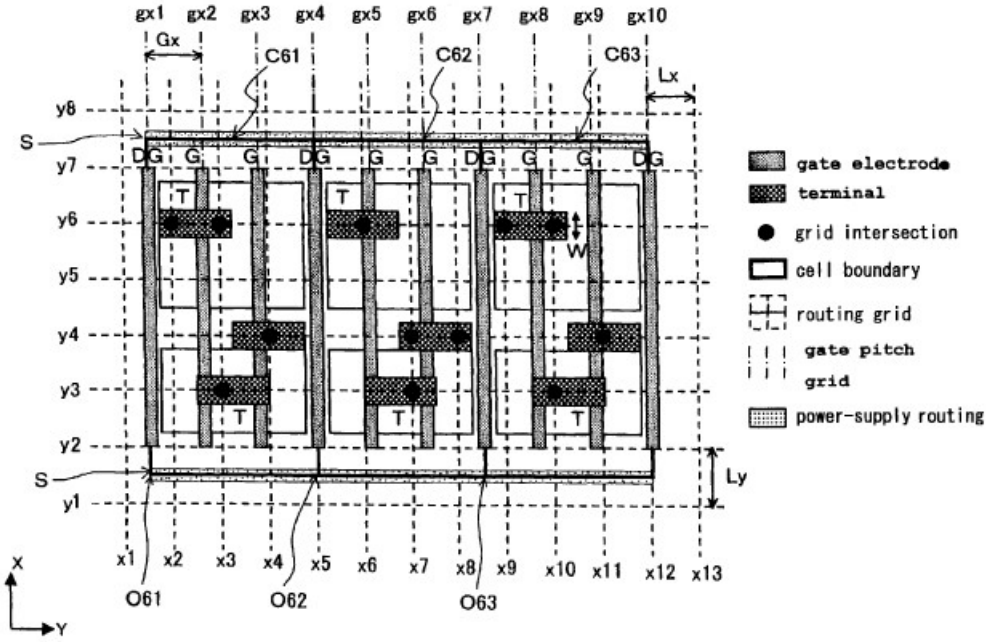
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | F I G. 11<br>  <br><br>(Ichiryu Fig. 11). As described above, the NMOS diffusion could be L-shaped, such that the uniform extending portion is a second, longer length.<br><br>*See also* Ichiryu Figs. 1, 2, 3, 8, 12, 13, 14. |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | This limitation also would have been obvious to a person of ordinary skill in the art based on (1) Ichiryu alone; and/or (2) the teachings with respect to this claim element as detailed in the cover document of Respondent’s invalidity contentions and Respondent’s other invalidity charts. |
| [12.2] wherein the second length is larger than the first length. | At least under Tela’s apparent infringement theory, Ichiryu discloses and/or renders obvious wherein the second length is larger than the first length.<br><br>Ichiryu depicts transistors that have extending portions.<br><br>Modified Fig. 11M<br>  <br><br>Modified Fig. 11M<br>  <br><br>*See, e.g.*: |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | F I G. 11<br>  <br><br>(Ichiryu Fig. 11).<br><br>*See also* Ichiryu Figs. 1, 2, 3, 8, 12, 13, 14. As described above, the NMOS diffusion could be L-shaped, such that the uniform extending portion is a second, longer length. In that case, the second length is larger than the first length. |

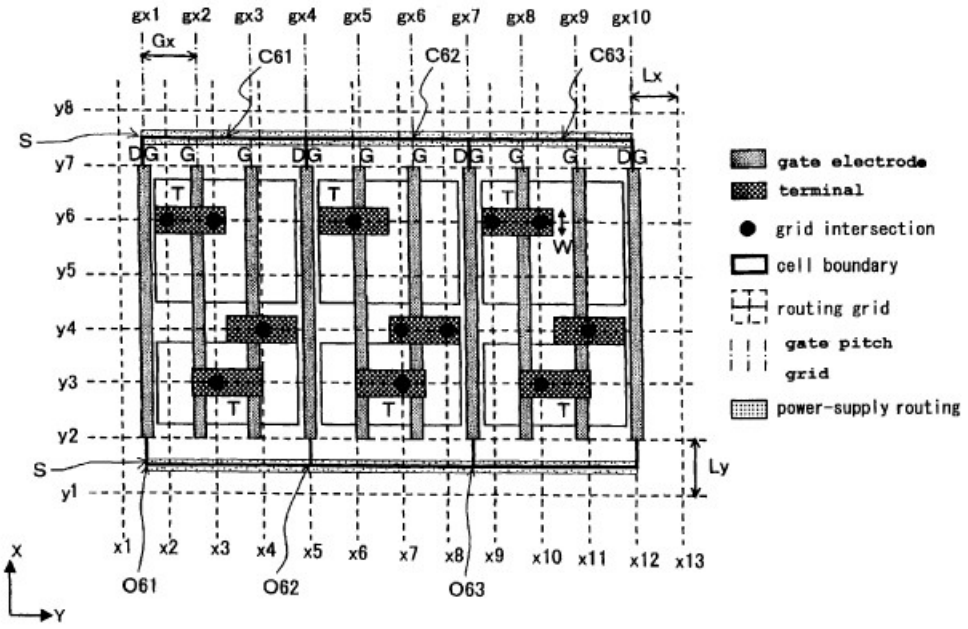
| '012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | This limitation also would have been obvious to a person of ordinary skill in the art based on (1) Ichiryu alone; and/or (2) the teachings with respect to this claim element as detailed in the cover document of Respondent's invalidity contentions and Respondent's other invalidity charts. |
| [13.0] An integrated circuit device as recited in claim 11,<br><br>wherein the uniformity extending portion of each of the second number of the active linear conductive segments has a length as measured in the first direction that is larger than the second size of the transistor gate electrode portion. | At least under Tela's apparent infringement theory, Ichiryu discloses and/or renders obvious an integrated circuit device as recited in claim 11, wherein the uniformity extending portion of each of the second number of the active linear conductive segments has a length as measured in the first direction that is larger than the second size of the transistor gate electrode portion. |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | **Modified Fig. 11M**<br>  <br><br>Ichiryu depicts transistors that have extending portions.<br>*See, e.g.*: |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | F I G. 11<br>  <br><br>(Ichiryu Fig. 11).<br><br>*See also* Ichiryu Figs. 1, 2, 3, 8, 12, 13, 14. As described above, the NMOS diffusion could be L-shaped, such that the uniform extending portion is a second, longer length. In that case, the second length could be larger than the second size of the transistor gate electrode portion. |

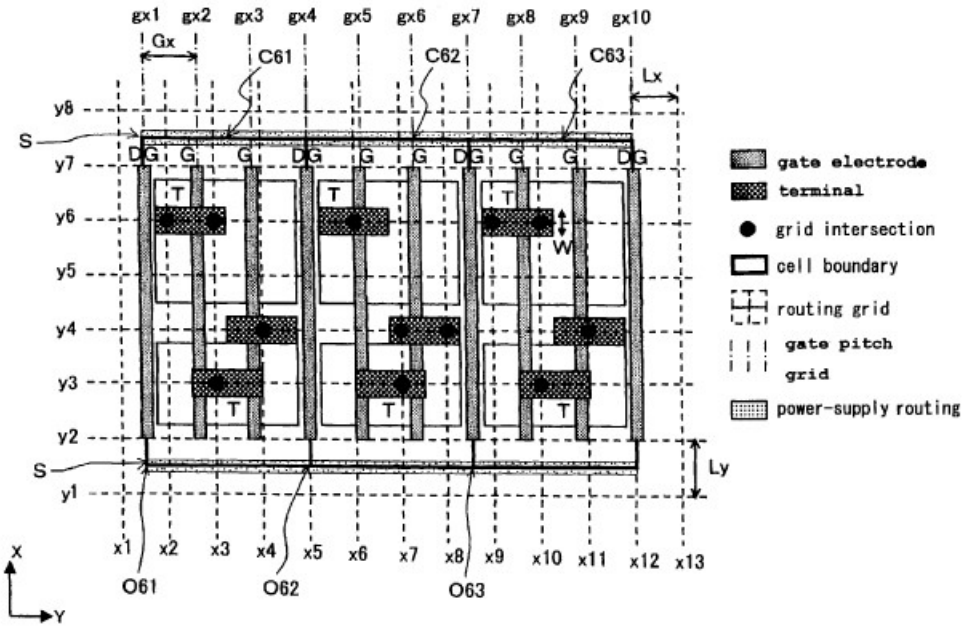
| '012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | This limitation also would have been obvious to a person of ordinary skill in the art based on (1) Ichiryu alone; and/or (2) the teachings with respect to this claim element as detailed in the cover document of Respondent's invalidity contentions and Respondent's other invalidity charts. |
| [26.0] An integrated circuit device as recited in claim 2, further comprising:<br><br>a first interconnect level region that forms part of an overall first interconnect level of the integrated circuit device, the first interconnect level region formed above and over the substrate region, wherein the first interconnect level region includes first interconnect linear conductive structures formed to extend in a linear manner in the first direction. | At least under Tela's apparent infringement theory, Ichiryu discloses and/or renders obvious an integrated circuit device as recited in claim 2, further comprising a first interconnect level region that forms part of an overall first interconnect level of the integrated circuit device, the first interconnect level region formed above and over the substrate region, wherein the first interconnect level region includes first interconnect linear) conductive structures formed to extend in a linear manner in the first direction.<br><br>Ichiryu describes and depicts terminals "T" that form interconnect / wiring layers. The first interconnect layer may be one of these wiring layers. One such of these terminals extends in a linear manner in the first (vertical) direction.<br><br>*See, e.g.*:<br><br>"When the automatic placement & routing tool is used, the wiring can be provided with a minimum wiring width on the routing grids in the X and Y directions. The routing grids for the wirings are located at the equal interval of Lx in the X direction and located at the equal interval of Ly in the Y direction. Basically, different wiring layers are respectively used for the wirings in the X direction and the wirings in the Y direction, and the different wiring layers are joined by means of an inter-layer connection." (Ichiryu at 9:43-51).<br><br>"[T]he automatic placement & routing apparatus connects the plurality of terminals T by wrings based on the circuit connection information in a tentative routing processing step S13. Because the shape of the terminal T is extended in the X direction, a degree of freedom in the tentative routing is increased, which reduces an entire wiring length. Thereafter, the automatic placement & routing apparatus automatically acknowledges a shape and a dimension of the terminal demanded to realize an effective connection, and removes any unnecessary part from the terminal T to thereby reduce the dimension of the terminal in a terminal shape processing step S14. Finally, the automatic placement |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | & routing apparatus routes the standard cells with respect to one another in an actual routing processing step S15. Because the routing resource is increased by the reduction of the terminal dimension in the terminal shape processing step S14, the standard cells are routed with respect to one another in Such manner that the increased routing resource is maximally utilized. By executing the steps S11-S15, the entire wiring length can be reduced, and the reductions of the wiring capacity and delay time and the reduction of the design TAT because of the increased routing resource can be realized.” (Ichiryu at 12:38-60).<br><br>“Referring to reference symbols in FIG. 11, x1-x13 denote routing grids for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, y1-y8 denote routing grids disposed in parallel with the X direction and adjacent to one another in the Y direction, gx1-gx10 denote grids of gate pitches for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, C61, C62 and C63 are standard cells, O61, O62 and O63 are respective origins of the standard cells C61, C62 and C63, … G denotes a gate electrode, and DG denotes a dummy gate electrode.” (Ichiryu at 14:32-44).<br><br>“The use of the automatic 1 placement & routing tool allows the wiring to be provided on the routing grids in the X and Y directions with a minimum wiring width. The routing grids are located at the equal interval of Lx different to the gate pitch Gx in the X direction, and located at the equal interval of Ly in the Y direction. Basically, different wiring layers are used for the wirings in the X direction and the wirings in the Y direction, and the different wiring layers are joined by means of the inter-layer connection.” (Ichiryu at 14:62-15:3).“A wiring constituting the terminal T has a rectangular shape horizontally extended along the X direction. A shorter-side dimension of the terminal T corresponds to a wiring width W in the automatic placement & routing. A longer-side dimension is at least (Lx+W), where Lx is the routing grid interval and W is the wiring width. In order to provide the wiring connection for the terminal T using the automatic placement & routing tool, the terminal T must include the grid intersection (a point at which the routing grids intersect with each other) (see black circles). In the embodiment 1, the terminal T has the rectangular shape horizontally extended (extended in the X direction) and is located on a routing grid yi (i=1, 2, . . . ) along the Y direction.” (Ichiryu at 15:4-15). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “Alternatively, the block area can be prevented from increasing when the routing grids [Lx, Ly] are extended to be equal to the gate pitch [Gx] of the gate array cell.” (Ichiryu at 16:7-9).<br><br>F I G. 11<br><br>  <br><br><br>(Ichiryu Fig. 11).<br><br>*See also* Ichiryu Figs. 2, 3, 8, 12, 13, 17, 18.<br><br>Ichiryu describes and depicts terminals “T” that are rectangular and extend in parallel to form interconnect / wiring layers. |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | *See, e.g.*:<br><br>“When the automatic placement & routing tool is used, the wiring can be provided with a minimum wiring width on the routing grids in the X and Y directions. The routing grids for the wirings are located at the equal interval of Lx in the X direction and located at the equal interval of Ly in the Y direction. Basically, different wiring layers are respectively used for the wirings in the X direction and the wirings in the Y direction, and the different wiring layers are joined by means of an inter-layer connection.” (Ichiryu at 9:43-51).<br><br>“[T]he automatic placement & routing apparatus connects the plurality of terminals T by wrings based on the circuit connection information in a tentative routing processing step S13. Because the shape of the terminal T is extended in the X direction, a degree of freedom in the tentative routing is increased, which reduces an entire wiring length. Thereafter, the automatic placement & routing apparatus automatically acknowledges a shape and a dimension of the terminal demanded to realize an effective connection, and removes any unnecessary part from the terminal T to thereby reduce the dimension of the terminal in a terminal shape processing step S14. Finally, the automatic placement & routing apparatus routes the standard cells with respect to one another in an actual routing processing step S15. Because the routing resource is increased by the reduction of the terminal dimension in the terminal shape processing step S14, the standard cells are routed with respect to one another in Such manner that the increased routing resource is maximally utilized. By executing the steps S11-S15, the entire wiring length can be reduced, and the reductions of the wiring capacity and delay time and the reduction of the design TAT because of the increased routing resource can be realized.” (Ichiryu at 12:38-60).<br><br>“The use of the automatic 1 placement & routing tool allows the wiring to be provided on the routing grids in the X and Y directions with a minimum wiring width. The routing grids are located at the equal interval of Lx different to the gate pitch Gx in the X direction, and located at the equal interval of Ly in the Y direction. Basically, different wiring layers are used for the wirings in the X direction and the wirings in the Y direction, and the different wiring layers are joined by means of the inter-layer connection.” (Ichiryu at 14:62-15:3). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “A wiring constituting the terminal T has a rectangular shape horizontally extended along the X direction. A shorter-side dimension of the terminal T corresponds to a wiring width W in the automatic placement & routing. A longer-side dimension is at least (Lx+W), where Lx is the routing grid interval and W is the wiring width. In order to provide the wiring connection for the terminal T using the automatic placement & routing tool, the terminal T must include the grid intersection (a point at which the routing grids intersect with each other) (see black circles). In the embodiment 1, the terminal T has the rectangular shape horizontally extended (extended in the X direction) and is located on a routing grid yi (i=1, 2, . . . ) along the Y direction.” (Ichiryu at 15:4-15).<br><br>“Alternatively, the block area can be prevented from increasing when the routing grids [Lx, Ly] are extended to be equal to the gate pitch [Gx] of the gate array cell.” (Ichiryu at 16:7-9). |

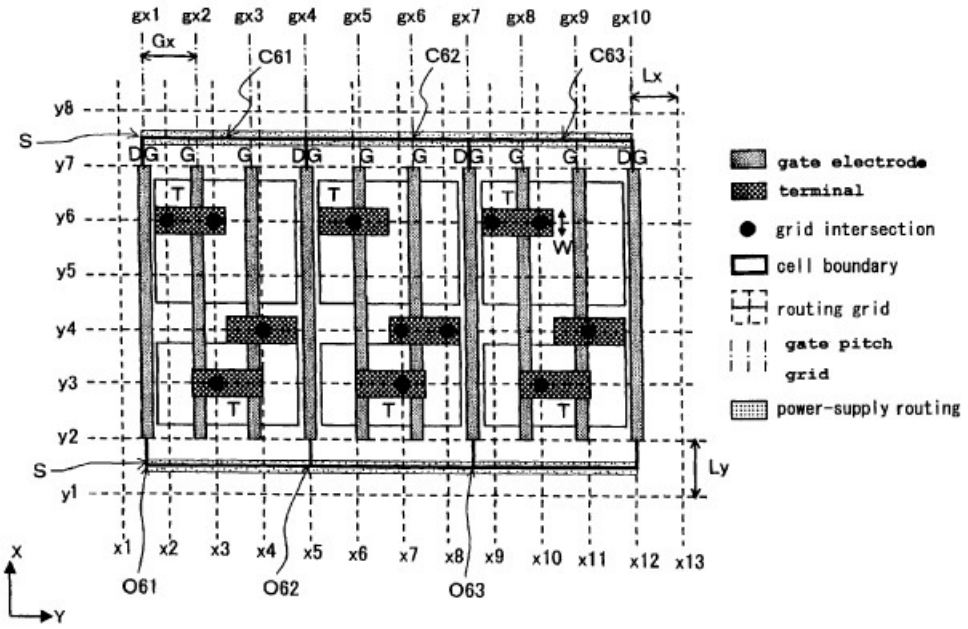
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | F I G. 11<br>  <br><br>(Ichiryu Fig. 11).<br>*See also* Ichiryu Figs. 2, 3, 8, 12, 13, 17, 18.<br>This limitation also would have been obvious to a person of ordinary skill in the art based on (1) Ichiryu alone; and/or (2) the teachings with respect to this claim element as detailed in the cover document of Respondent’s invalidity contentions and Respondent’s other invalidity charts. |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| [27.0] An integrated circuit device as recited in claim 26,<br><br>wherein the plurality of linear conductive segments within the gate electrode level region are positioned in a side-by-side manner according to a substantially equal centerline-to-centerline spacing as measured in a second direction perpendicular to the first direction, and | At least under Tela’s apparent infringement theory, Ichiryu discloses and/or renders obvious an integrated circuit device as recited in claim 26, wherein the plurality of linear conductive segments within the gate electrode level region are positioned in a side-by-side manner according to a substantially equal centerline-to-centerline spacing as measured in a second direction perpendicular to the first direction.<br><br>Ichiryu describes layout techniques for gate electrodes, including that they have equal centerline-to-centerline spacing.<br><br>*See, e.g.*:<br><br>“[A]s recited in No. H10-32253 of the Publication of the Unexamined Japanese Patent Applications, the interval and the length of the gate electrodes in each standard cell are set regular so that the OPC is processed per standard cell in the conventional technology.” (Ichiryu at 2:37-41).<br><br>“The standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes….” (Ichiryu at 6:20-21).<br><br>“A standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes, wherein gate pitches of some of the gate electrodes are set to values different to the routing grid interval set along the X direction in parallel with the power-supply wiring of the standard cell, and a cell width along the X direction in parallel with the power-supply wiring of the standard cell is set to an integral multiple of a minimum value of the gate pitches of the gate electrodes set to the values different to the routing grid interval set along the X direction.” (Ichiryu at 6:26-35).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, a precision in a finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:41-45). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “A standard cell according to the present invention comprises a plurality of gate electrodes and a plurality of dummy gate electrodes, wherein a cell width in the X direction in parallel with the power-supply wiring of the standard cell is an integral multiple of a minimum gate pitch of gate pitches of the gate electrodes and the dummy gate electrodes different to the routing grid interval along the X direction.” (Ichiryu at 6:46-52).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:58-62).<br><br>“The gate pitches of the standard cell are all preferably equal. Thereby, the pattern of the gate electrodes can impart a perfect regularity to the gate pitches, and the precision in the finished dimension of the gate electrodes can be further improved.” (Ichiryu at 6:66-7:3).<br><br>“Further, because the pattern of the gate electrodes can have the regularity, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be performed in each standard cell.” (Ichiryu at 8:21-24).<br><br>“Referring to reference symbols in FIG. 11, x1-x13 denote routing grids for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, y1-y8 denote routing grids disposed in parallel with the X direction and adjacent to one another in the Y direction, gx1-gx10 denote grids of gate pitches for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, C61, C62 and C63 are standard cells, O61, O62 and O63 are respective origins of the standard cells C61, C62 and C63, … G denotes a gate electrode, and DG denotes a dummy gate electrode.” (Ichiryu at 14:32-44).<br><br>“In the standard cells C61, C62 and C63, gate lengths and gate intervals of the gate electrode G and dummy gate electrode DG are constant, and a cell width of the standard cells C61, C62 and C63 in the X direction is an integral multiple of a minimum value of a gate pitch Gx (value of gate |

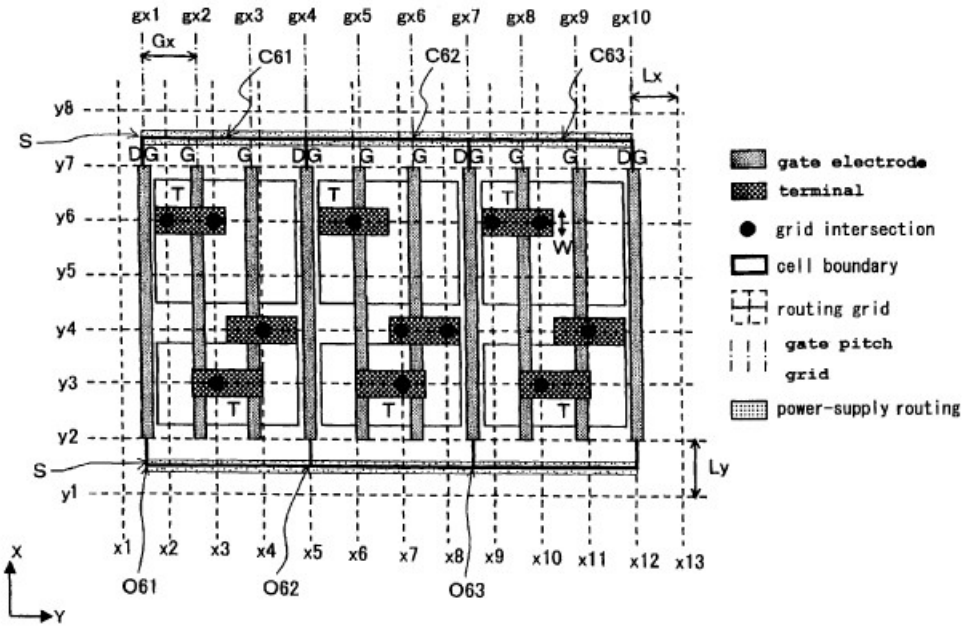
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | pitch=gate length+gate interval) (In FIG. 11, the cell width of the standard cells C61, C62 and C63 is three times as wide as Gx).” (Ichiryu at 14:45-51).<br><br>“Not only inside the respective standard cells C61, C62 and C63, but also among the standard cells C61, C62 and C63 to one another, the gate lengths and the gate intervals are equal in the patterns of the gate electrodes and the dummy gate electrodes.” (Ichiryu at 15:47-51).<br><br>“In the embodiment 5, the gate lengths are all equal in the gate electrodes and the dummy gate electrodes….” (Ichiryu at 16:10-11).<br><br>“In FIG. 14, a reference symbol C81 denotes a standard cell. The standard cell C81 comprises gate electrodes G, dummy gate electrodes DG and two gate electrodes G2 having a gate length different to those of the gate electrode G and the dummy gate electrode DG, wherein a width of the gate electrode G2 is set so that a cell width of the standard cell C81 in the X direction is an integral multiple of the gate pitch Gx. In FIG. 14, the cell width of the standard cell C81 is nine times as wide as the gate pitch Gx. The width of the gate electrode G2 is thus set because a processing speed is expected to be faster when the cell width of each cell in the X direction is the integral multiple of the gate pitch Gx than when the cell width of each cell takes an arbitrary value in the placement using the conventional automatic placement & routing tool. However, the width of the gate electrode G2 is not necessarily set in the foregoing manner.” (Ichiryu at 16:15-30).<br><br>“In the constitution, the distance from the cell boundary of each standard cell to the gate electrode in the closest vicinity and the distance from the cell boundary of another standard cell adjacent thereto to the gate electrode in the closest vicinity are constant.” (Ichiryu at 16:65-17:2).<br><br>“For example, a distance from each of the cell boundary of the standard cells C61, C62 and C63 to the gate electrode in the X direction is ‘Gx-gate length/2’ and constant even in the constitution shown in FIG. 11 where the dummy gate electrodes DG are not provided. A distance between a transistor disposed at the end of each standard cell and the gate electrode G of the adjacent standard cell is ‘2Gx-gate length’ and constant. For example, even in the case where the dummy gate electrode DG is not provided in the constitution described referring to FIG. 11, the distance from each of the cell |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | boundary of the respective standard cells C61, C62 and C63 to the gate electrode G located at the end of each of the standard cells in the X direction is constant at (Gx-gate length/2). Further, the distance from the gate electrode G located at the end of each of the standard cells to the gate electrode G located at the end of each of adjacent standard cells in the X direction is constant at (2Gx-gate length).” (Ichiryu at 17:6-22).<br><br>“Further, in the embodiment 6, the standard cells described in the embodiments 1 and 5 are used. The gate lengths and the gate intervals are thereby equal in the patterns of the gate electrodes of the placed standard cells C91, C92 and C93, which leads to the improvement of the precision in the finished dimension of the gate electrodes. The improvement of the precision in the finished dimension of the gate electrodes can be realized not only inside each of the standard cells C91, C92 and C93 but also between the standard cells.” (Ichiryu at 18:1-9).<br><br>“[W]hen the standard cells are adjacently located, the gate lengths and the gate intervals in the patterns of the gate electrodes and the dummy gate electrodes are the same as when they are located alone.” (Ichiryu at 18:10-13). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | F I G. 11<br>  <br><br>(Ichiryu Fig. 11).<br>*See also* Ichiryu at Figs. 1, 2, 3, 8, 12, 13, 14.<br>This limitation also would have been obvious to a person of ordinary skill in the art based on (1) Ichiryu alone; and/or (2) the teachings with respect to this claim element as detailed in the cover document of Respondent’s invalidity contentions and Respondent’s other invalidity charts. |

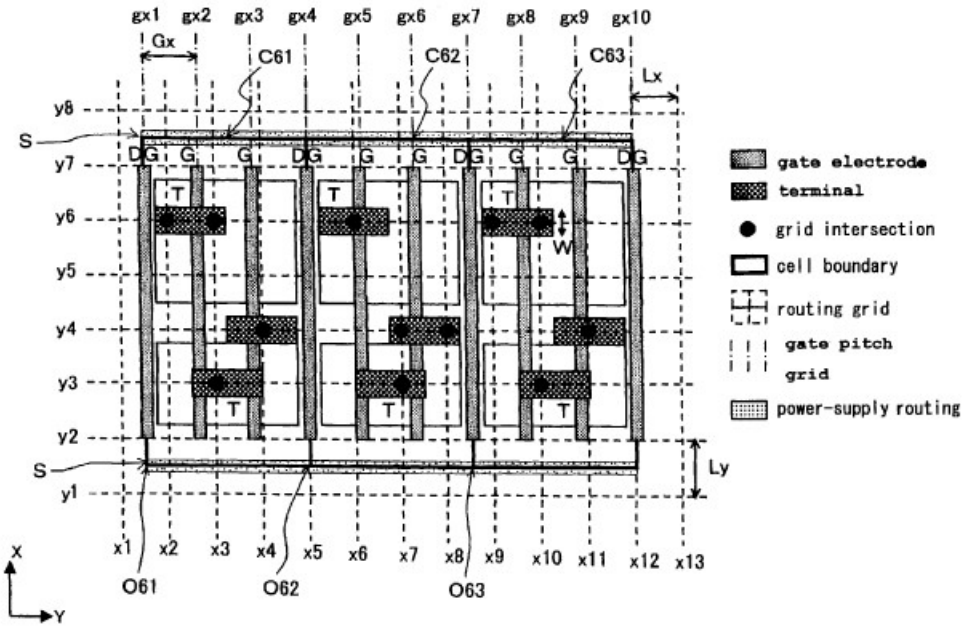
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| [27.1] wherein a centerline-to-centerline spacing as measured in the second direction between adjacently positioned first interconnect linear conductive structures is an integer multiple of the substantially equal centerline-to-centerline spacing as measured in the second direction between adjacently positioned ones of the plurality of linear conductive segments within the gate electrode level region. | At least under Tela’s apparent infringement theory, Ichiryu discloses and/or renders obvious wherein a centerline-to-centerline spacing as measured in the second direction between adjacently positioned first interconnect linear conductive structures is an integer multiple of the substantially equal centerline-to-centerline spacing as measured in the second direction between adjacently positioned ones of the plurality of linear conductive segments) within the gate electrode level region.<br><br>Ichiryu describes and depicts terminals “T” that are rectangular, regularly spaced, and extend in parallel to form interconnect / wiring layers. These terminals can have the same pitch as the gate pitch.<br><br>*See, e.g.*:<br><br>“When the automatic placement & routing tool is used, the wiring can be provided with a minimum wiring width on the routing grids in the X and Y directions. The routing grids for the wirings are located at the equal interval of Lx in the X direction and located at the equal interval of Ly in the Y direction. Basically, different wiring layers are respectively used for the wirings in the X direction and the wirings in the Y direction, and the different wiring layers are joined by means of an inter-layer connection.” (Ichiryu at 9:43-51).<br><br>“[T]he automatic placement & routing apparatus connects the plurality of terminals T by wrings based on the circuit connection information in a tentative routing processing step S13. Because the shape of the terminal T is extended in the X direction, a degree of freedom in the tentative routing is increased, which reduces an entire wiring length. Thereafter, the automatic placement & routing apparatus automatically acknowledges a shape and a dimension of the terminal demanded to realize an effective connection, and removes any unnecessary part from the terminal T to thereby reduce the dimension of the terminal in a terminal shape processing step S14. Finally, the automatic placement & routing apparatus routes the standard cells with respect to one another in an actual routing processing step S15. Because the routing resource is increased by the reduction of the terminal dimension in the terminal shape processing step S14, the standard cells are routed with respect to one another in Such manner that the increased routing resource is maximally utilized. By executing the steps S11-S15, the entire wiring length can be reduced, and the reductions of the wiring capacity and |

| '012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | delay time and the reduction of the design TAT because of the increased routing resource can be realized." (Ichiryu at 12:38-60).<br><br>"The use of the automatic 1 placement & routing tool allows the wiring to be provided on the routing grids in the X and Y directions with a minimum wiring width. The routing grids are located at the equal interval of Lx different to the gate pitch Gx in the X direction, and located at the equal interval of Ly in the Y direction. Basically, different wiring layers are used for the wirings in the X direction and the wirings in the Y direction, and the different wiring layers are joined by means of the inter-layer connection." (Ichiryu at 14:62-15:3).<br><br>"A wiring constituting the terminal T has a rectangular shape horizontally extended along the X direction. A shorter-side dimension of the terminal T corresponds to a wiring width W in the automatic placement & routing. A longer-side dimension is at least (Lx+W), where Lx is the routing grid interval and W is the wiring width. In order to provide the wiring connection for the terminal T using the automatic placement & routing tool, the terminal T must include the grid intersection (a point at which the routing grids intersect with each other) (see black circles). In the embodiment 1, the terminal T has the rectangular shape horizontally extended (extended in the X direction) and is located on a routing grid yi (i=1, 2, . . . ) along the Y direction." (Ichiryu at 15:4-15).<br><br>"Alternatively, the block area can be prevented from increasing when the routing grids [Lx, Ly] are extended to be equal to the gate pitch [Gx] of the gate array cell." (Ichiryu at 16:7-9). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | F I G. 11<br>  <br><br>(Ichiryu Fig. 11).<br>*See also* Ichiryu Figs. 2, 3, 8, 12, 13, 17, 18.<br>This limitation also would have been obvious to a person of ordinary skill in the art based on (1) Ichiryu alone; and/or (2) the teachings with respect to this claim element as detailed in the cover document of Respondent’s invalidity contentions and Respondent’s other invalidity charts. |

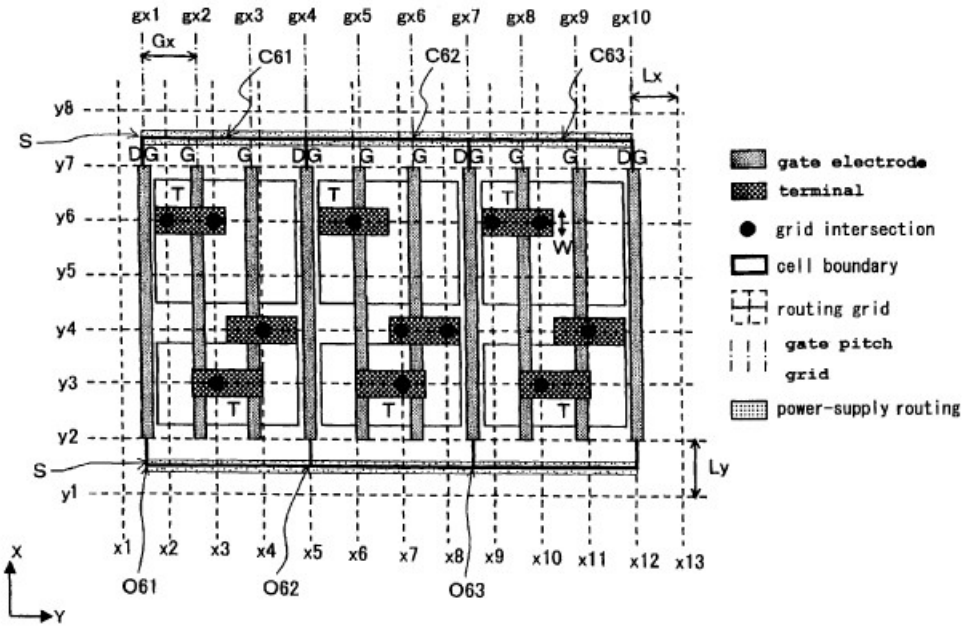
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| [28.0] An integrated circuit device as recited in claim 26, further comprising:<br><br>a second interconnect level region that forms part of an overall second interconnect level of the integrated circuit device, the second interconnect level region formed above and over the substrate region, wherein the second interconnect level region includes second interconnect linear conductive structures formed to extend in a linear manner in a second direction perpendicular to the first direction. | At least under Tela’s apparent infringement theory, Ichiryu discloses and/or renders obvious an integrated circuit device as recited in claim 26, further comprising: a second interconnect level region that forms part of an overall second interconnect level of the integrated circuit device, the second interconnect level region formed above and over the substrate region, wherein the second interconnect level region includes second interconnect linear conductive structures formed to extend in a linear manner in a second direction perpendicular to the first direction.<br><br>Ichiryu describes and depicts terminals “T” that are rectangular, regularly spaced, and extend in parallel to form interconnect / wiring layers. The second interconnect layer may be one of these wiring layers such that it is between gates and the first interconnect layer. The wiring layers can extend in the horizontal direction, which is a second direction.<br><br>*See, e.g.*:<br><br>“When the automatic placement & routing tool is used, the wiring can be provided with a minimum wiring width on the routing grids in the X and Y directions. The routing grids for the wirings are located at the equal interval of Lx in the X direction and located at the equal interval of Ly in the Y direction. Basically, different wiring layers are respectively used for the wirings in the X direction and the wirings in the Y direction, and the different wiring layers are joined by means of an inter-layer connection.” (Ichiryu at 9:43-51).<br><br>“[T]he automatic placement & routing apparatus connects the plurality of terminals T by wrings based on the circuit connection information in a tentative routing processing step S13. Because the shape of the terminal T is extended in the X direction, a degree of freedom in the tentative routing is increased, which reduces an entire wiring length. Thereafter, the automatic placement & routing apparatus automatically acknowledges a shape and a dimension of the terminal demanded to realize an effective connection, and removes any unnecessary part from the terminal T to thereby reduce the dimension of the terminal in a terminal shape processing step S14. Finally, the automatic placement & routing apparatus routes the standard cells with respect to one another in an actual routing processing step S15. Because the routing resource is increased by the reduction of the terminal dimension in the terminal shape processing step S14, the standard cells are routed with respect to one |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | another in Such manner that the increased routing resource is maximally utilized. By executing the steps S11-S15, the entire wiring length can be reduced, and the reductions of the wiring capacity and delay time and the reduction of the design TAT because of the increased routing resource can be realized.” (Ichiryu at 12:38-60).<br><br>“The use of the automatic 1 placement & routing tool allows the wiring to be provided on the routing grids in the X and Y directions with a minimum wiring width. The routing grids are located at the equal interval of Lx different to the gate pitch Gx in the X direction, and located at the equal interval of Ly in the Y direction. Basically, different wiring layers are used for the wirings in the X direction and the wirings in the Y direction, and the different wiring layers are joined by means of the inter-layer connection.” (Ichiryu at 14:62-15:3).<br><br>“A wiring constituting the terminal T has a rectangular shape horizontally extended along the X direction. A shorter-side dimension of the terminal T corresponds to a wiring width W in the automatic placement & routing. A longer-side dimension is at least (Lx+W), where Lx is the routing grid interval and W is the wiring width. In order to provide the wiring connection for the terminal T using the automatic placement & routing tool, the terminal T must include the grid intersection (a point at which the routing grids intersect with each other) (see black circles). In the embodiment 1, the terminal T has the rectangular shape horizontally extended (extended in the X direction) and is located on a routing grid yi (i=1, 2, . . . ) along the Y direction.” (Ichiryu at 15:4-15).<br><br>“Alternatively, the block area can be prevented from increasing when the routing grids [Lx, Ly] are extended to be equal to the gate pitch [Gx] of the gate array cell.” (Ichiryu at 16:7-9). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | F I G. 11<br>  <br><br>(Ichiryu Fig. 11).<br>*See also* Ichiryu Figs. 2, 3, 8, 12, 13, 17, 18.<br>Ichiryu describes and depicts terminals “T” that are rectangular, regularly spaced, and extend in parallel to form interconnect / wiring layers.<br>*See, e.g.*: |

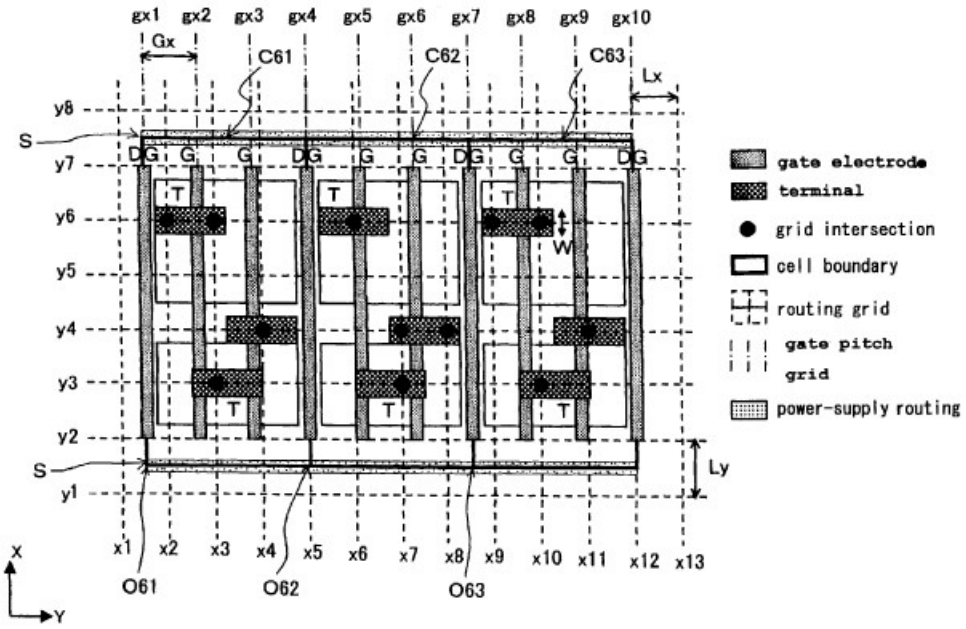
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “When the automatic placement & routing tool is used, the wiring can be provided with a minimum wiring width on the routing grids in the X and Y directions. The routing grids for the wirings are located at the equal interval of Lx in the X direction and located at the equal interval of Ly in the Y direction. Basically, different wiring layers are respectively used for the wirings in the X direction and the wirings in the Y direction, and the different wiring layers are joined by means of an inter-layer connection.” (Ichiryu at 9:43-51).<br><br>“[T]he automatic placement & routing apparatus connects the plurality of terminals T by wrings based on the circuit connection information in a tentative routing processing step S13. Because the shape of the terminal T is extended in the X direction, a degree of freedom in the tentative routing is increased, which reduces an entire wiring length. Thereafter, the automatic placement & routing apparatus automatically acknowledges a shape and a dimension of the terminal demanded to realize an effective connection, and removes any unnecessary part from the terminal T to thereby reduce the dimension of the terminal in a terminal shape processing step S14. Finally, the automatic placement & routing apparatus routes the standard cells with respect to one another in an actual routing processing step S15. Because the routing resource is increased by the reduction of the terminal dimension in the terminal shape processing step S14, the standard cells are routed with respect to one another in Such manner that the increased routing resource is maximally utilized. By executing the steps S11-S15, the entire wiring length can be reduced, and the reductions of the wiring capacity and delay time and the reduction of the design TAT because of the increased routing resource can be realized.” (Ichiryu at 12:38-60).<br><br>“The use of the automatic 1 placement & routing tool allows the wiring to be provided on the routing grids in the X and Y directions with a minimum wiring width. The routing grids are located at the equal interval of Lx different to the gate pitch Gx in the X direction, and located at the equal interval of Ly in the Y direction. Basically, different wiring layers are used for the wirings in the X direction and the wirings in the Y direction, and the different wiring layers are joined by means of the inter-layer connection.” (Ichiryu at 14:62-15:3).<br><br>“A wiring constituting the terminal T has a rectangular shape horizontally extended along the X direction. A shorter-side dimension of the terminal T corresponds to a wiring width W in the |

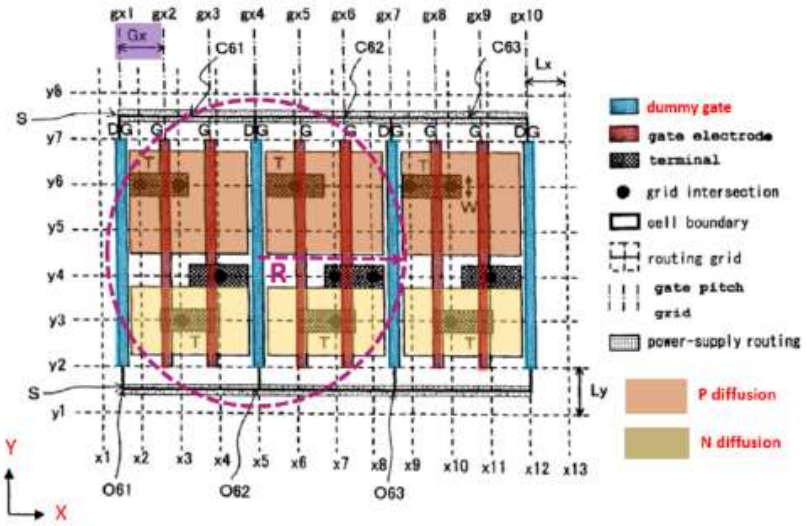
| '012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | automatic placement & routing. A longer-side dimension is at least (Lx+W), where Lx is the routing grid interval and W is the wiring width. In order to provide the wiring connection for the terminal T using the automatic placement & routing tool, the terminal T must include the grid intersection (a point at which the routing grids intersect with each other) (see black circles). In the embodiment 1, the terminal T has the rectangular shape horizontally extended (extended in the X direction) and is located on a routing grid yi (i=1, 2, . . . ) along the Y direction." (Ichiryu at 15:4-15).<br><br>"Alternatively, the block area can be prevented from increasing when the routing grids [Lx, Ly] are extended to be equal to the gate pitch [Gx] of the gate array cell." (Ichiryu at 16:7-9). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | F I G. 11<br>  <br><br>(Ichiryu Fig. 11).<br>*See also* Ichiryu Figs. 2, 3, 8, 12, 13, 17, 18.<br>This limitation also would have been obvious to a person of ordinary skill in the art based on (1) Ichiryu alone; and/or (2) the teachings with respect to this claim element as detailed in the cover document of Respondent’s invalidity contentions and Respondent’s other invalidity charts. |

| '012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| [30.0] An integrated circuit device as recited in claim 28,<br><br>wherein the second interconnect level region is positioned at a level between the substrate region and the first interconnect level region. | At least under Tela's apparent infringement theory, Ichiryu discloses and/or renders obvious an integrated circuit device as recited in claim 28, wherein the second interconnect level region is positioned at a level between the substrate region and the first interconnect level region.<br><br>Ichiryu describes and depicts terminals "T" that are rectangular, regularly spaced, and extend in parallel to form interconnect / wiring layers. The first and second interconnect layers may be chosen such that the second interconnect layer is under the first interconnect layer.<br><br>*See, e.g.*:<br><br>"When the automatic placement & routing tool is used, the wiring can be provided with a minimum wiring width on the routing grids in the X and Y directions. The routing grids for the wirings are located at the equal interval of Lx in the X direction and located at the equal interval of Ly in the Y direction. Basically, different wiring layers are respectively used for the wirings in the X direction and the wirings in the Y direction, and the different wiring layers are joined by means of an inter-layer connection." (Ichiryu at 9:43-51).<br><br>"[T]he automatic placement & routing apparatus connects the plurality of terminals T by wrings based on the circuit connection information in a tentative routing processing step S13. Because the shape of the terminal T is extended in the X direction, a degree of freedom in the tentative routing is increased, which reduces an entire wiring length. Thereafter, the automatic placement & routing apparatus automatically acknowledges a shape and a dimension of the terminal demanded to realize an effective connection, and removes any unnecessary part from the terminal T to thereby reduce the dimension of the terminal in a terminal shape processing step S14. Finally, the automatic placement & routing apparatus routes the standard cells with respect to one another in an actual routing processing step S15. Because the routing resource is increased by the reduction of the terminal dimension in the terminal shape processing step S14, the standard cells are routed with respect to one another in Such manner that the increased routing resource is maximally utilized. By executing the steps S11-S15, the entire wiring length can be reduced, and the reductions of the wiring capacity and |

| '012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | delay time and the reduction of the design TAT because of the increased routing resource can be realized." (Ichiryu at 12:38-60).<br><br>"The use of the automatic 1 placement & routing tool allows the wiring to be provided on the routing grids in the X and Y directions with a minimum wiring width. The routing grids are located at the equal interval of Lx different to the gate pitch Gx in the X direction, and located at the equal interval of Ly in the Y direction. Basically, different wiring layers are used for the wirings in the X direction and the wirings in the Y direction, and the different wiring layers are joined by means of the inter-layer connection." (Ichiryu at 14:62-15:3).<br><br>"A wiring constituting the terminal T has a rectangular shape horizontally extended along the X direction. A shorter-side dimension of the terminal T corresponds to a wiring width W in the automatic placement & routing. A longer-side dimension is at least (Lx+W), where Lx is the routing grid interval and W is the wiring width. In order to provide the wiring connection for the terminal T using the automatic placement & routing tool, the terminal T must include the grid intersection (a point at which the routing grids intersect with each other) (see black circles). In the embodiment 1, the terminal T has the rectangular shape horizontally extended (extended in the X direction) and is located on a routing grid yi (i=1, 2, . . . ) along the Y direction." (Ichiryu at 15:4-15).<br><br>"Alternatively, the block area can be prevented from increasing when the routing grids [Lx, Ly] are extended to be equal to the gate pitch [Gx] of the gate array cell." (Ichiryu at 16:7-9). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | F I G. 11<br>  <br><br>(Ichiryu Fig. 11).<br>*See also* Ichiryu Figs. 2, 3, 8, 12, 13, 17, 18.<br>This limitation also would have been obvious to a person of ordinary skill in the art based on (1) Ichiryu alone; and/or (2) the teachings with respect to this claim element as detailed in the cover document of Respondent’s invalidity contentions and Respondent’s other invalidity charts. |

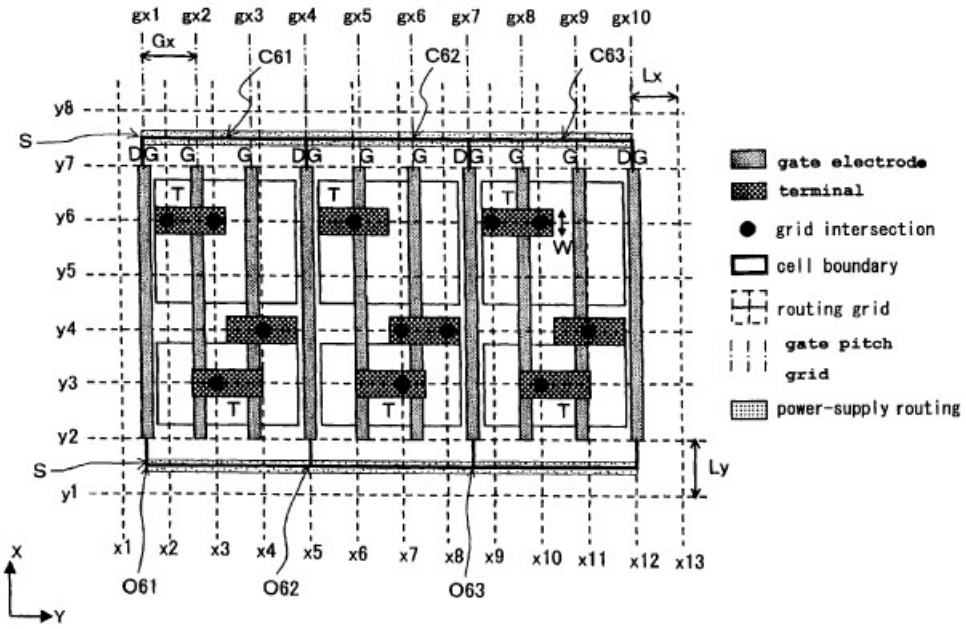
| '012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| 3. An integrated circuit device as recited in claim 2, wherein each of the plurality of linear conductive segments is defined to have a substantially equal length as measured in the first direction. | At least under Tela's apparent infringement theory, Ichiryu discloses and/or renders obvious an integrated circuit device as recited in claim 2, wherein each of the plurality of linear conductive segments is defined to have a substantially equal length as measured in the first direction.<br><br>Ichiryu describes and depicts multiple linear conductive segments, e.g. structures in the polysilicon level, that have an equal length.<br><br>F I G. 11<br>  <br><br><br>*See, e.g.*:<br><br>"[A]s the miniaturization of the process [continues], a precision in a finished dimension of the gate electrode ultimately obtained is deteriorated by an optical proximity effect when an interval between the gate electrodes and gate lengths of the gate electrodes are irregular in their patterns. When the precision in the finished dimension of the gate electrode is deteriorated, performances of respective |

| '012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | transistors of the semiconductor integrated circuit are increasingly inconstant, which leads to an increased variation in a performance of the semiconductor integrate[d] circuit." (Ichiryu at 2:23-32).<br><br>"[A]s recited in No. H10-32253 of the Publication of the Unexamined Japanese Patent Applications, the interval and the length of the gate electrodes in each standard cell are set regular so that the OPC is processed per standard cell in the conventional technology." (Ichiryu at 2:37-41).<br><br>"The standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes…." (Ichiryu at 6:20-21).<br><br>"A standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes, wherein gate pitches of some of the gate electrodes are set to values different to the routing grid interval set along the X direction in parallel with the power-supply wiring of the standard cell, and a cell width along the X direction in parallel with the power-supply wiring of the standard cell is set to an integral multiple of a minimum value of the gate pitches of the gate electrodes set to the values different to the routing grid interval set along the X direction." (Ichiryu at 6:26-35).<br><br>"[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, a precision in a finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell." (Ichiryu at 6:41-45).<br><br>"A standard cell according to the present invention comprises a plurality of gate electrodes and a plurality of dummy gate electrodes, wherein a cell width in the X direction in parallel with the power-supply wiring of the standard cell is an integral multiple of a minimum gate pitch of gate pitches of the gate electrodes and the dummy gate electrodes different to the routing grid interval along the X direction." (Ichiryu at 6:46-52). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:58-62).<br><br>“The gate pitches of the standard cell are all preferably equal. Thereby, the pattern of the gate electrodes can impart a perfect regularity to the gate pitches, and the precision in the finished dimension of the gate electrodes can be further improved.” (Ichiryu at 6:66-7:3).<br><br>“Further, because the pattern of the gate electrodes can have the regularity, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be performed in each standard cell.” (Ichiryu at 8:21-24).<br><br>“Referring to reference symbols in FIG. 11, x1-x13 denote routing grids for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, y1-y8 denote routing grids disposed in parallel with the X direction and adjacent to one another in the Y direction, gx1-gx10 denote grids of gate pitches for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, C61, C62 and C63 are standard cells, O61, O62 and O63 are respective origins of the standard cells C61, C62 and C63, … G denotes a gate electrode, and DG denotes a dummy gate electrode.” (Ichiryu at 14:32-44).<br><br>“In the standard cells C61, C62 and C63, gate lengths and gate intervals of the gate electrode G and dummy gate electrode DG are constant, and a cell width of the standard cells C61, C62 and C63 in the X direction is an integral multiple of a minimum value of a gate pitch Gx (value of gate pitch=gate length+gate interval) (In FIG. 11, the cell width of the standard cells C61, C62 and C63 is three times as wide as Gx).” (Ichiryu at 14:45-51).<br><br>“Not only inside the respective standard cells C61, C62 and C63, but also among the standard cells C61, C62 and C63 to one another, the gate lengths and the gate intervals are equal in the patterns of the gate electrodes and the dummy gate electrodes.” (Ichiryu at 15:47-51). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “In the embodiment 5, the gate lengths are all equal in the gate electrodes and the dummy gate electrodes….” (Ichiryu at 16:10-11).<br><br>“In FIG. 14, a reference symbol C81 denotes a standard cell. The standard cell C81 comprises gate electrodes G, dummy gate electrodes DG and two gate electrodes G2 having a gate length different to those of the gate electrode G and the dummy gate electrode DG, wherein a width of the gate electrode G2 is set so that a cell width of the standard cell C81 in the X direction is an integral multiple of the gate pitch Gx. In FIG. 14, the cell width of the standard cell C81 is nine times as wide as the gate pitch Gx. The width of the gate electrode G2 is thus set because a processing speed is expected to be faster when the cell width of each cell in the X direction is the integral multiple of the gate pitch Gx than when the cell width of each cell takes an arbitrary value in the placement using the conventional automatic placement & routing tool. However, the width of the gate electrode G2 is not necessarily set in the foregoing manner.” (Ichiryu at 16:15-30).<br><br>“As described, in the case of including the standard cell comprising the gate electrodes having the different gate lengths….” (Ichiryu at 16:32-34).<br><br>“In the constitution, the distance from the cell boundary of each standard cell to the gate electrode in the closest vicinity and the distance from the cell boundary of another standard cell adjacent thereto to the gate electrode in the closest vicinity are constant.” (Ichiryu at 16:65-17:2).<br><br>“For example, a distance from each of the cell boundary of the standard cells C61, C62 and C63 to the gate electrode in the X direction is ‘Gx-gate length/2’ and constant even in the constitution shown in FIG. 11 where the dummy gate electrodes DG are not provided. A distance between a transistor disposed at the end of each standard cell and the gate electrode G of the adjacent standard cell is ‘2Gx-gate length’ and constant. For example, even in the case where the dummy gate electrode DG is not provided in the constitution described referring to FIG. 11, the distance from each of the cell boundary of the respective standard cells C61, C62 and C63 to the gate electrode G located at the end of each of the standard cells in the X direction is constant at (Gx-gate length/2). Further, the distance from the gate electrode G located at the end of each of the standard cells to the gate electrode G |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | located at the end of each of adjacent standard cells in the X direction is constant at (2Gx-gate length).” (Ichiryu at 17:6-22).<br><br>“Further, in the embodiment 6, the standard cells described in the embodiments 1 and 5 are used. The gate lengths and the gate intervals are thereby equal in the patterns of the gate electrodes of the placed standard cells C91, C92 and C93, which leads to the improvement of the precision in the finished dimension of the gate electrodes. The improvement of the precision in the finished dimension of the gate electrodes can be realized not only inside each of the standard cells C91, C92 and C93 but also between the standard cells.” (Ichiryu at 18:1-9).<br><br>“[W]hen the standard cells are adjacently located, the gate lengths and the gate intervals in the patterns of the gate electrodes and the dummy gate electrodes are the same as when they are located alone.” (Ichiryu at 18:10-13). |

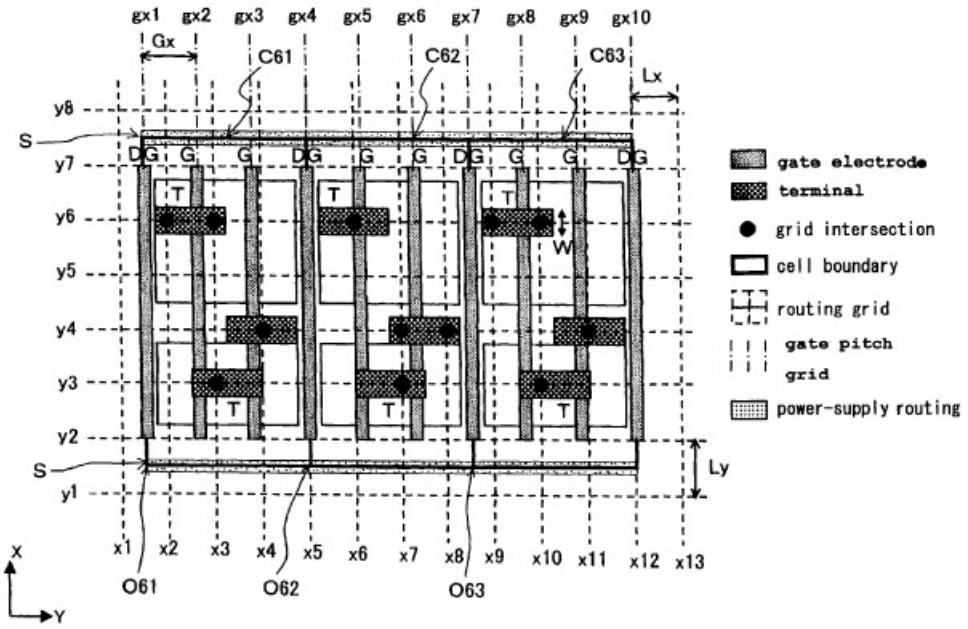
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | F I G. 11<br>  <br><br>(Ichiryu Fig. 11).<br>*See also* Ichiryu at Figs. 1, 2, 3, 8, 12, 13, 14.<br>This limitation also would have been obvious to a person of ordinary skill in the art based on (1) Ichiryu alone; and/or (2) the teachings with respect to this claim element as detailed in the cover document of Respondent’s invalidity contentions and Respondent’s other invalidity charts. |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| [7.0] An integrated circuit device as recited in claim 2, wherein the active linear conductive segments are positioned in a side-by-side manner, and | At least under Tela’s apparent infringement theory, Ichiryu discloses and/or renders obvious an integrated circuit device as recited in claim 2, wherein the active linear conductive segments are positioned in a side-by-side manner.<br><br>Ichiryu describes and depicts multiple gate electrodes that form transistors of different types and are placed on a grid having the same pitch and width, and thus equal side-to-side spacing.<br><br>*See, e.g.*:<br><br>“[A]s recited in No. H10-32253 of the Publication of the Unexamined Japanese Patent Applications, the interval and the length of the gate electrodes in each standard cell are set regular so that the OPC is processed per standard cell in the conventional technology.” (Ichiryu at 2:37-41).<br><br>“The standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes….” (Ichiryu at 6:20-21).<br><br>“A standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes, wherein gate pitches of some of the gate electrodes are set to values different to the routing grid interval set along the X direction in parallel with the power-supply wiring of the standard cell, and a cell width along the X direction in parallel with the power-supply wiring of the standard cell is set to an integral multiple of a minimum value of the gate pitches of the gate electrodes set to the values different to the routing grid interval set along the X direction.” (Ichiryu at 6:26-35).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, a precision in a finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:41-45).<br><br>“A standard cell according to the present invention comprises a plurality of gate electrodes and a plurality of dummy gate electrodes, wherein a cell width in the X direction in parallel with the power-supply wiring of the standard cell is an integral multiple of a minimum gate pitch of gate |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | pitches of the gate electrodes and the dummy gate electrodes different to the routing grid interval along the X direction.” (Ichiryu at 6:46-52).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:58-62).<br><br>“The gate pitches of the standard cell are all preferably equal. Thereby, the pattern of the gate electrodes can impart a perfect regularity to the gate pitches, and the precision in the finished dimension of the gate electrodes can be further improved.” (Ichiryu at 6:66-7:3).<br><br>“Further, because the pattern of the gate electrodes can have the regularity, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be performed in each standard cell.” (Ichiryu at 8:21-24).<br><br>“Referring to reference symbols in FIG. 11, x1-x13 denote routing grids for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, y1-y8 denote routing grids disposed in parallel with the X direction and adjacent to one another in the Y direction, gx1-gx10 denote grids of gate pitches for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, C61, C62 and C63 are standard cells, O61, O62 and O63 are respective origins of the standard cells C61, C62 and C63, … G denotes a gate electrode, and DG denotes a dummy gate electrode.” (Ichiryu at 14:32-44).<br><br>“In the standard cells C61, C62 and C63, gate lengths and gate intervals of the gate electrode G and dummy gate electrode DG are constant, and a cell width of the standard cells C61, C62 and C63 in the X direction is an integral multiple of a minimum value of a gate pitch Gx (value of gate pitch=gate length+gate interval) (In FIG. 11, the cell width of the standard cells C61, C62 and C63 is three times as wide as Gx).” (Ichiryu at 14:45-51). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “Not only inside the respective standard cells C61, C62 and C63, but also among the standard cells C61, C62 and C63 to one another, the gate lengths and the gate intervals are equal in the patterns of the gate electrodes and the dummy gate electrodes.” (Ichiryu at 15:47-51).<br><br>“In the embodiment 5, the gate lengths are all equal in the gate electrodes and the dummy gate electrodes….” (Ichiryu at 16:10-11).<br><br>“In FIG. 14, a reference symbol C81 denotes a standard cell. The standard cell C81 comprises gate electrodes G, dummy gate electrodes DG and two gate electrodes G2 having a gate length different to those of the gate electrode G and the dummy gate electrode DG, wherein a width of the gate electrode G2 is set so that a cell width of the standard cell C81 in the X direction is an integral multiple of the gate pitch Gx. In FIG. 14, the cell width of the standard cell C81 is nine times as wide as the gate pitch Gx. The width of the gate electrode G2 is thus set because a processing speed is expected to be faster when the cell width of each cell in the X direction is the integral multiple of the gate pitch Gx than when the cell width of each cell takes an arbitrary value in the placement using the conventional automatic placement & routing tool. However, the width of the gate electrode G2 is not necessarily set in the foregoing manner.” (Ichiryu at 16:15-30).<br><br>“In the constitution, the distance from the cell boundary of each standard cell to the gate electrode in the closest vicinity and the distance from the cell boundary of another standard cell adjacent thereto to the gate electrode in the closest vicinity are constant.” (Ichiryu at 16:65-17:2).<br><br>“For example, a distance from each of the cell boundary of the standard cells C61, C62 and C63 to the gate electrode in the X direction is ‘Gx-gate length/2’ and constant even in the constitution shown in FIG. 11 where the dummy gate electrodes DG are not provided. A distance between a transistor disposed at the end of each standard cell and the gate electrode G of the adjacent standard cell is ‘2Gx-gate length’ and constant. For example, even in the case where the dummy gate electrode DG is not provided in the constitution described referring to FIG. 11, the distance from each of the cell boundary of the respective standard cells C61, C62 and C63 to the gate electrode G located at the end of each of the standard cells in the X direction is constant at (Gx-gate length/2). Further, the distance from the gate electrode G located at the end of each of the standard cells to the gate electrode G |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | located at the end of each of adjacent standard cells in the X direction is constant at (2Gx-gate length).” (Ichiryu at 17:6-22).<br><br>“Further, in the embodiment 6, the standard cells described in the embodiments 1 and 5 are used. The gate lengths and the gate intervals are thereby equal in the patterns of the gate electrodes of the placed standard cells C91, C92 and C93, which leads to the improvement of the precision in the finished dimension of the gate electrodes. The improvement of the precision in the finished dimension of the gate electrodes can be realized not only inside each of the standard cells C91, C92 and C93 but also between the standard cells.” (Ichiryu at 18:1-9).<br><br>“[W]hen the standard cells are adjacently located, the gate lengths and the gate intervals in the patterns of the gate electrodes and the dummy gate electrodes are the same as when they are located alone.” (Ichiryu at 18:10-13). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | F I G. 11<br>  <br><br>(Ichiryu Fig. 11).<br>*See also* Ichiryu at Figs. 1, 2, 3, 8, 12, 13, 14.<br>This limitation also would have been obvious to a person of ordinary skill in the art based on (1) Ichiryu alone; and/or (2) the teachings with respect to this claim element as detailed in the cover document of Respondent’s invalidity contentions and Respondent’s other invalidity charts. |

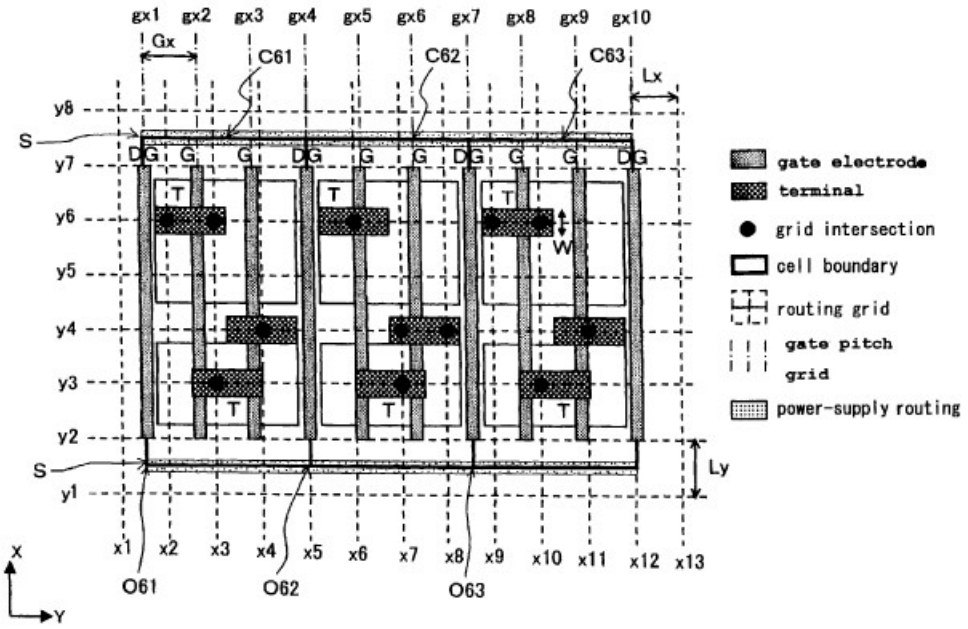
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| [7.1] wherein the non-gate linear conductive segment is positioned beside at least one of the active linear conductive segments. | At least under Tela’s apparent infringement theory, Ichiryu discloses and/or renders obvious wherein the non-gate linear conductive segment is positioned beside at least one of the active linear conductive segments.<br><br>Ichiryu describes and depicts multiple dummy gates beside linear conductive segments, e.g. “dummy gate eletrodes” or “DG.”<br><br>*See, e.g.*:<br><br>“[A]s the miniaturization of the process [continues], a precision in a finished dimension of the gate electrode ultimately obtained is deteriorated by an optical proximity effect when an interval between the gate electrodes and gate lengths of the gate electrodes are irregular in their patterns. When the precision in the finished dimension of the gate electrode is deteriorated, performances of respective transistors of the semiconductor integrated circuit are increasingly inconstant, which leads to an increased variation in a performance of the semiconductor integrate[d] circuit.” (Ichiryu at 2:23-32).<br><br>“[A]s recited in No. H10-32253 of the Publication of the Unexamined Japanese Patent Applications, the interval and the length of the gate electrodes in each standard cell are set regular so that the OPC is processed per standard cell in the conventional technology.” (Ichiryu at 2:37-41).“<br><br>Dummy gate electrodes DG are provided on cell boundaries of standard cells C41’, C4[2]’ and C43’ disposed on the upper side in FIG. 18. These dummy gate electrodes DG are shared between the adjacent standard cells. The gate electrodes G and the dummy gate electrodes DG are respectively equally spaced, and their gate [] lengths are equal.” (Ichiryu at 2:45-50).<br><br>“[W]hen the regions R1, R2 and R3 for adjusting the cell width to the integral multiple of the routing grid interval are provided, the gate electrode located on the cell boundary of the standard cell cannot be shared. There is a possibility that the dummy electrodes DG are located with less than a minimum interval allowed in a design rule therebetween, which results in an error in the design rule. In order to |

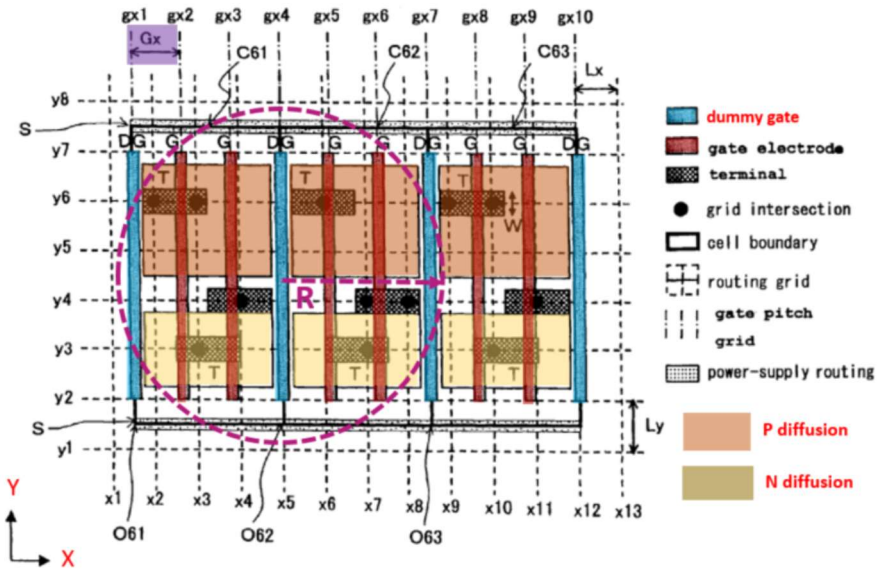
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | avoid the foregoing error in the design rule, it is necessary to enlarge the gate length, for example, in the same manner as the dummy gate DG2 disposed on the lower side in FIG. 18.” (Ichiryu at 3:7-16).<br><br>“Though the gate interval in each standard cell can be maintained at the constant level when such the gate length enlargement is executed, the gate length becomes irregular at the dummy gate electrodes DG2, which results in the imprecision of the finished dimension of the gate electrodes. Further, the OPC cannot be processed in each standard cell due to the different gate lengths in the dummy gate electrodes DG in each standard cell and the dummy gate electrodes DG2 adjacent thereto.” (Ichiryu at 3:17-25).<br><br>“The standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes….” (Ichiryu at 6:20-21).<br><br>“A standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes, wherein gate pitches of some of the gate electrodes are set to values different to the routing grid interval set along the X direction in parallel with the power-supply wiring of the standard cell, and a cell width along the X direction in parallel with the power-supply wiring of the standard cell is set to an integral multiple of a minimum value of the gate pitches of the gate electrodes set to the values different to the routing grid interval set along the X direction.” (Ichiryu at 6:26-35).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, a precision in a finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:41-45).<br><br>“A standard cell according to the present invention comprises a plurality of gate electrodes and a plurality of dummy gate electrodes, wherein a cell width in the X direction in parallel with the power-supply wiring of the standard cell is an integral multiple of a minimum gate pitch of gate pitches of the gate electrodes and the dummy gate electrodes different to the routing grid interval along the X direction.” (Ichiryu at 6:46-52). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell. As another advantage, the provision of the dummy gate electrodes can further improve the regularity of the gate length and gate interval, which largely contributes to the facilitation of the OPC process in each standard cell.” (Ichiryu at 6:58-65).<br><br>“The gate pitches of the standard cell are all preferably equal. Thereby, the pattern of the gate electrodes can impart a perfect regularity to the gate pitches, and the precision in the finished dimension of the gate electrodes can be further improved.” (Ichiryu at 6:66-7:3).<br><br>“Further, because the pattern of the gate electrodes can have the regularity, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be performed in each standard cell.” (Ichiryu at 8:21-24).<br><br>“Referring to reference symbols in FIG. 11, x1-x13 denote routing grids for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, y1-y8 denote routing grids disposed in parallel with the X direction and adjacent to one another in the Y direction, gx1-gx10 denote grids of gate pitches for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, C61, C62 and C63 are standard cells, O61, O62 and O63 are respective origins of the standard cells C61, C62 and C63, … G denotes a gate electrode, and DG denotes a dummy gate electrode.” (Ichiryu at 14:32-44).<br><br>“In the standard cells C61, C62 and C63, gate lengths and gate intervals of the gate electrode G and dummy gate electrode DG are constant, and a cell width of the standard cells C61, C62 and C63 in the X direction is an integral multiple of a minimum value of a gate pitch Gx (value of gate pitch=gate length+gate interval) (In FIG. 11, the cell width of the standard cells C61, C62 and C63 is three times as wide as Gx).” (Ichiryu at 14:45-51). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “Not only inside the respective standard cells C61, C62 and C63, but also among the standard cells C61, C62 and C63 to one another, the gate lengths and the gate intervals are equal in the patterns of the gate electrodes and the dummy gate electrodes.” (Ichiryu at 15:47-51).<br><br>“In the embodiment 5, the gate lengths are all equal in the gate electrodes and the dummy gate electrodes….” (Ichiryu at 16:10-11).<br><br>“In FIG. 14, a reference symbol C81 denotes a standard cell. The standard cell C81 comprises gate electrodes G, dummy gate electrodes DG and two gate electrodes G2 having a gate length different to those of the gate electrode G and the dummy gate electrode DG, wherein a width of the gate electrode G2 is set so that a cell width of the standard cell C81 in the X direction is an integral multiple of the gate pitch Gx. In FIG. 14, the cell width of the standard cell C81 is nine times as wide as the gate pitch Gx. The width of the gate electrode G2 is thus set because a processing speed is expected to be faster when the cell width of each cell in the X direction is the integral multiple of the gate pitch Gx than when the cell width of each cell takes an arbitrary value in the placement using the conventional automatic placement & routing tool. However, the width of the gate electrode G2 is not necessarily set in the foregoing manner.” (Ichiryu at 16:15-30).<br><br>“As described, in the case of including the standard cell comprising the gate electrodes having the different gate lengths….” (Ichiryu at 16:32-34).<br><br>“[T]he embodiment 5 can be applied in the same manner to a cell structure where the dummy gate electrodes having the different gate lengths are provided and a cell structure where the gate electrodes and the dummy gate electrodes having the different gate intervals are provided. The description of the embodiment 5 is premised on the provision of the dummy gates DG….” (Ichiryu at 16:53-59).<br><br>“In the constitution, the distance from the cell boundary of each standard cell to the gate electrode in the closest vicinity and the distance from the cell boundary of another standard cell adjacent thereto to the gate electrode in the closest vicinity are constant.” (Ichiryu at 16:65-17:2). |

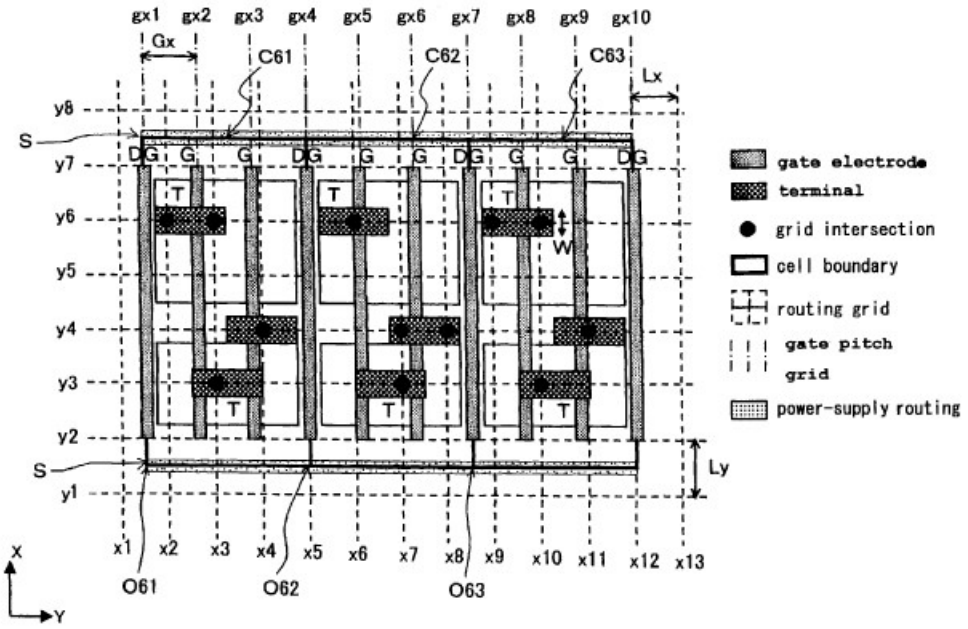
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “For example, a distance from each of the cell boundary of the standard cells C61, C62 and C63 to the gate electrode in the X direction is ‘Gx-gate length/2’ and constant even in the constitution shown in FIG. 11 where the dummy gate electrodes DG are not provided. A distance between a transistor disposed at the end of each standard cell and the gate electrode G of the adjacent standard cell is ‘2Gx-gate length’ and constant. For example, even in the case where the dummy gate electrode DG is not provided in the constitution described referring to FIG. 11, the distance from each of the cell boundary of the respective standard cells C61, C62 and C63 to the gate electrode G located at the end of each of the standard cells in the X direction is constant at (Gx-gate length/2). Further, the distance from the gate electrode G located at the end of each of the standard cells to the gate electrode G located at the end of each of adjacent standard cells in the X direction is constant at (2Gx-gate length).” (Ichiryu at 17:6-22).<br><br>“Further, in the embodiment 6, the standard cells described in the embodiments 1 and 5 are used. The gate lengths and the gate intervals are thereby equal in the patterns of the gate electrodes of the placed standard cells C91, C92 and C93, which leads to the improvement of the precision in the finished dimension of the gate electrodes. The improvement of the precision in the finished dimension of the gate electrodes can be realized not only inside each of the standard cells C91, C92 and C93 but also between the standard cells.” (Ichiryu at 18:1-9).<br><br>“[W]hen the standard cells are adjacently located, the gate lengths and the gate intervals in the patterns of the gate electrodes and the dummy gate electrodes are the same as when they are located alone.” (Ichiryu at 18:10-13). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | F I G. 11<br>  <br><br>(Ichiryu Fig. 11).<br>*See also* Ichiryu at Figs. 1, 2, 3, 8, 12, 13, 14.<br><br>This limitation also would have been obvious to a person of ordinary skill in the art based on (1) Ichiryu alone; and/or (2) the teachings with respect to this claim element as detailed in the cover document of Respondent’s invalidity contentions and Respondent’s other invalidity charts. |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| 14. An integrated circuit device as recited in claim 2, wherein at least two of the plurality of linear conductive segments are non-gate linear conductive segments, wherein each non-gate linear conductive segment does not form a gate electrode of a transistor device. | At least under Tela’s apparent infringement theory, Ichiryu discloses and/or renders obvious an integrated circuit device as recited in claim 2, wherein at least two of the plurality of linear conductive segments are non-gate linear conductive segments, wherein each non-gate linear conductive segment does not form a gate electrode of a transistor device.<br><br>Ichiryu describes and depicts multiple dummy gates, e.g. “dummy gate eletrodes” or “DG.”<br><br>F I G. 11<br>  <br><br><br>*See, e.g.*:<br><br>“Dummy gate electrodes DG are provided on cell boundaries of standard cells C41’, C4[2]’ and C43’ disposed on the upper side in FIG. 18. These dummy gate electrodes DG are shared between |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | the adjacent standard cells. The gate electrodes G and the dummy gate electrodes DG are respectively equally spaced, and their gate [] lengths are equal.” (Ichiryu at 2:45-50).<br><br>“[W]hen the regions R1, R2 and R3 for adjusting the cell width to the integral multiple of the routing grid interval are provided, the gate electrode located on the cell boundary of the standard cell cannot be shared. There is a possibility that the dummy electrodes DG are located with less than a minimum interval allowed in a design rule therebetween, which results in an error in the design rule. In order to avoid the foregoing error in the design rule, it is necessary to enlarge the gate length, for example, in the same manner as the dummy gate DG2 disposed on the lower side in FIG. 18.” (Ichiryu at 3:7-16).<br><br>“Though the gate interval in each standard cell can be maintained at the constant level when such the gate length enlargement is executed, the gate length becomes irregular at the dummy gate electrodes DG2, which results in the imprecision of the finished dimension of the gate electrodes. Further, the OPC cannot be processed in each standard cell due to the different gate lengths in the dummy gate electrodes DG in each standard cell and the dummy gate electrodes DG2 adjacent thereto.” (Ichiryu at 3:17-25).<br><br>“A standard cell according to the present invention comprises a plurality of gate electrodes and a plurality of dummy gate electrodes, wherein a cell width in the X direction in parallel with the power-supply wiring of the standard cell is an integral multiple of a minimum gate pitch of gate pitches of the gate electrodes and the dummy gate electrodes different to the routing grid interval along the X direction.” (Ichiryu at 6:46-52).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell. As another advantage, the provision of the dummy gate electrodes can further improve the regularity of the gate length and gate interval, which largely contributes to the facilitation of the OPC process in each standard cell.” (Ichiryu at 6:58-65).<br><br>“Referring to reference symbols in FIG. 11, x1-x13 denote routing grids for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, y1- |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | y8 denote routing grids disposed in parallel with the X direction and adjacent to one another in the Y direction, gx1-gx10 denote grids of gate pitches for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, C61, C62 and C63 are standard cells, O61, O62 and O63 are respective origins of the standard cells C61, C62 and C63, … G denotes a gate electrode, and DG denotes a dummy gate electrode.” (Ichiryu at 14:32-44).<br><br>“Not only inside the respective standard cells C61, C62 and C63, but also among the standard cells C61, C62 and C63 to one another, the gate lengths and the gate intervals are equal in the patterns of the gate electrodes and the dummy gate electrodes.” (Ichiryu at 15:47-51).<br><br>“In FIG. 14, a reference symbol C81 denotes a standard cell. The standard cell C81 comprises gate electrodes G, dummy gate electrodes DG and two gate electrodes G2 having a gate length different to those of the gate electrode G and the dummy gate electrode DG, wherein a width of the gate electrode G2 is set so that a cell width of the standard cell C81 in the X direction is an integral multiple of the gate pitch Gx. In FIG. 14, the cell width of the standard cell C81 is nine times as wide as the gate pitch Gx. The width of the gate electrode G2 is thus set because a processing speed is expected to be faster when the cell width of each cell in the X direction is the integral multiple of the gate pitch Gx than when the cell width of each cell takes an arbitrary value in the placement using the conventional automatic placement & routing tool. However, the width of the gate electrode G2 is not necessarily set in the foregoing manner.” (Ichiryu at 16:15-30).<br><br>“[T]he embodiment 5 can be applied in the same manner to a cell structure where the dummy gate electrodes having the different gate lengths are provided and a cell structure where the gate electrodes and the dummy gate electrodes having the different gate intervals are provided. The description of the embodiment 5 is premised on the provision of the dummy gates DG….” (Ichiryu at 16:53-59).<br><br>“[W]hen the standard cells are adjacently located, the gate lengths and the gate intervals in the patterns of the gate electrodes and the dummy gate electrodes are the same as when they are located alone.” (Ichiryu at 18:10-13). |

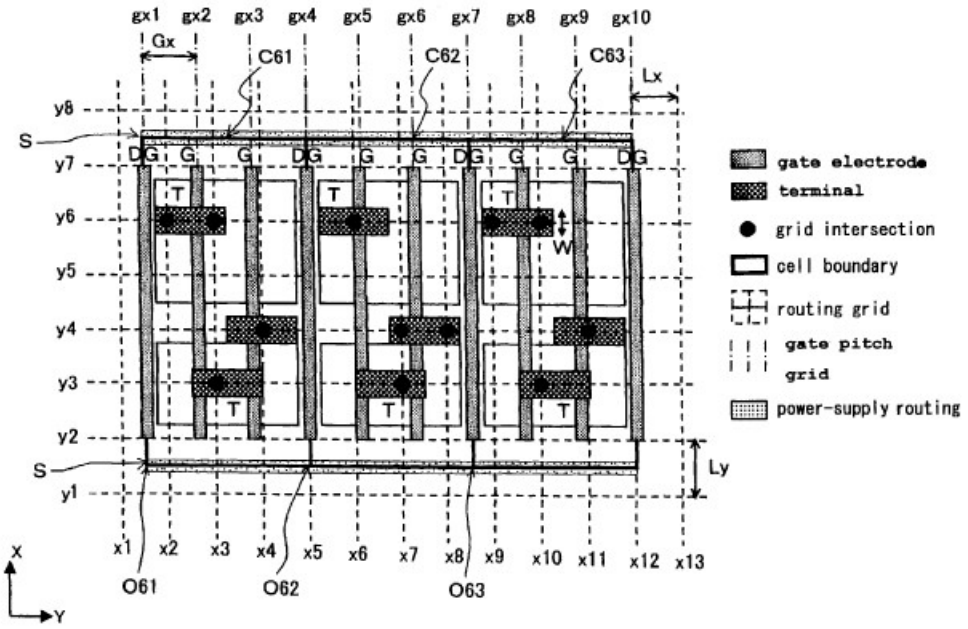
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | F I G. 11<br>  <br><br>(Ichiryu Fig. 11).<br>*See also* Ichiryu at Figs. 1, 2, 3, 8, 12, 13, 14.<br>This limitation also would have been obvious to a person of ordinary skill in the art based on (1) Ichiryu alone; and/or (2) the teachings with respect to this claim element as detailed in the cover document of Respondent’s invalidity contentions and Respondent’s other invalidity charts. |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| 15. An integrated circuit device as recited in claim 14, wherein the active linear conductive segments are positioned in a side-by-side manner so as to include a first outer positioned one of the active linear conductive segments and a second outer positioned one of the active linear conductive segments, and | At least under Tela’s apparent infringement theory, Ichiryu discloses and/or renders obvious an integrated circuit device as recited in claim 14, wherein the active linear conductive segments are positioned in a side-by-side manner so as to include a first outer positioned one of the active linear conductive segments and a second outer positioned one of the active linear conductive segments.<br><br>Ichiryu describes and depicts multiple gate electrodes that form transistors of different types and are placed on a grid having the same pitch and width, and thus equal side-to-side spacing. Ichiryu describes layout techniques for gate electrodes, which are linear conductive segments.<br><br>*See, e.g.*:<br><br>“[A]s the miniaturization of the process [continues], a precision in a finished dimension of the gate electrode ultimately obtained is deteriorated by an optical proximity effect when an interval between the gate electrodes and gate lengths of the gate electrodes are irregular in their patterns. When the precision in the finished dimension of the gate electrode is deteriorated, performances of respective transistors of the semiconductor integrated circuit are increasingly inconstant, which leads to an increased variation in a performance of the semiconductor integrate[d] circuit.” (Ichiryu at 2:23-32).<br><br>“[A]s recited in No. H10-32253 of the Publication of the Unexamined Japanese Patent Applications, the interval and the length of the gate electrodes in each standard cell are set regular so that the OPC is processed per standard cell in the conventional technology.” (Ichiryu at 2:37-41).<br><br>“The standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes….” (Ichiryu at 6:20-21).<br><br>“A standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes, wherein gate pitches of some of the gate electrodes are set to values different to the routing grid interval set along the X direction in parallel with the power-supply wiring of the standard cell, and a cell width along the X direction in parallel with the power-supply wiring of the standard cell is set to an integral multiple of a minimum value of the gate pitches of the gate |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | electrodes set to the values different to the routing grid interval set along the X direction.” (Ichiryu at 6:26-35).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, a precision in a finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:41-45).<br><br>“A standard cell according to the present invention comprises a plurality of gate electrodes and a plurality of dummy gate electrodes, wherein a cell width in the X direction in parallel with the power-supply wiring of the standard cell is an integral multiple of a minimum gate pitch of gate pitches of the gate electrodes and the dummy gate electrodes different to the routing grid interval along the X direction.” (Ichiryu at 6:46-52).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:58-62).<br><br>“The gate pitches of the standard cell are all preferably equal. Thereby, the pattern of the gate electrodes can impart a perfect regularity to the gate pitches, and the precision in the finished dimension of the gate electrodes can be further improved.” (Ichiryu at 6:66-7:3).<br><br>“Further, because the pattern of the gate electrodes can have the regularity, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be performed in each standard cell.” (Ichiryu at 8:21-24).<br><br>“Referring to reference symbols in FIG. 11, x1-x13 denote routing grids for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, y1-y8 denote routing grids disposed in parallel with the X direction and adjacent to one another in the Y direction, gx1-gx10 denote grids of gate pitches for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, C61, C62 and C63 are |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | standard cells, O61, O62 and O63 are respective origins of the standard cells C61, C62 and C63, … G denotes a gate electrode, and DG denotes a dummy gate electrode.” (Ichiryu at 14:32-44).<br><br>“In the standard cells C61, C62 and C63, gate lengths and gate intervals of the gate electrode G and dummy gate electrode DG are constant, and a cell width of the standard cells C61, C62 and C63 in the X direction is an integral multiple of a minimum value of a gate pitch Gx (value of gate pitch=gate length+gate interval) (In FIG. 11, the cell width of the standard cells C61, C62 and C63 is three times as wide as Gx).” (Ichiryu at 14:45-51).<br><br>“Not only inside the respective standard cells C61, C62 and C63, but also among the standard cells C61, C62 and C63 to one another, the gate lengths and the gate intervals are equal in the patterns of the gate electrodes and the dummy gate electrodes.” (Ichiryu at 15:47-51).<br><br>“In the embodiment 5, the gate lengths are all equal in the gate electrodes and the dummy gate electrodes….” (Ichiryu at 16:10-11).<br><br>“In FIG. 14, a reference symbol C81 denotes a standard cell. The standard cell C81 comprises gate electrodes G, dummy gate electrodes DG and two gate electrodes G2 having a gate length different to those of the gate electrode G and the dummy gate electrode DG, wherein a width of the gate electrode G2 is set so that a cell width of the standard cell C81 in the X direction is an integral multiple of the gate pitch Gx. In FIG. 14, the cell width of the standard cell C81 is nine times as wide as the gate pitch Gx. The width of the gate electrode G2 is thus set because a processing speed is expected to be faster when the cell width of each cell in the X direction is the integral multiple of the gate pitch Gx than when the cell width of each cell takes an arbitrary value in the placement using the conventional automatic placement & routing tool. However, the width of the gate electrode G2 is not necessarily set in the foregoing manner.” (Ichiryu at 16:15-30).<br><br>“As described, in the case of including the standard cell comprising the gate electrodes having the different gate lengths….” (Ichiryu at 16:32-34). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “In the constitution, the distance from the cell boundary of each standard cell to the gate electrode in the closest vicinity and the distance from the cell boundary of another standard cell adjacent thereto to the gate electrode in the closest vicinity are constant.” (Ichiryu at 16:65-17:2).<br><br>“For example, a distance from each of the cell boundary of the standard cells C61, C62 and C63 to the gate electrode in the X direction is ‘Gx-gate length/2’ and constant even in the constitution shown in FIG. 11 where the dummy gate electrodes DG are not provided. A distance between a transistor disposed at the end of each standard cell and the gate electrode G of the adjacent standard cell is ‘2Gx-gate length’ and constant. For example, even in the case where the dummy gate electrode DG is not provided in the constitution described referring to FIG. 11, the distance from each of the cell boundary of the respective standard cells C61, C62 and C63 to the gate electrode G located at the end of each of the standard cells in the X direction is constant at (Gx-gate length/2). Further, the distance from the gate electrode G located at the end of each of the standard cells to the gate electrode G located at the end of each of adjacent standard cells in the X direction is constant at (2Gx-gate length).” (Ichiryu at 17:6-22).<br><br>“Further, in the embodiment 6, the standard cells described in the embodiments 1 and 5 are used. The gate lengths and the gate intervals are thereby equal in the patterns of the gate electrodes of the placed standard cells C91, C92 and C93, which leads to the improvement of the precision in the finished dimension of the gate electrodes. The improvement of the precision in the finished dimension of the gate electrodes can be realized not only inside each of the standard cells C91, C92 and C93 but also between the standard cells.” (Ichiryu at 18:1-9).<br><br>“[W]hen the standard cells are adjacently located, the gate lengths and the gate intervals in the patterns of the gate electrodes and the dummy gate electrodes are the same as when they are located alone.” (Ichiryu at 18:10-13). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | F I G. 11<br>  <br><br>(Ichiryu Fig. 11).<br>*See also* Ichiryu at Figs. 1, 2, 3, 8, 12, 13, 14.<br>This limitation also would have been obvious to a person of ordinary skill in the art based on (1) Ichiryu alone; and/or (2) the teachings with respect to this claim element as detailed in the cover document of Respondent’s invalidity contentions and Respondent’s other invalidity charts. |

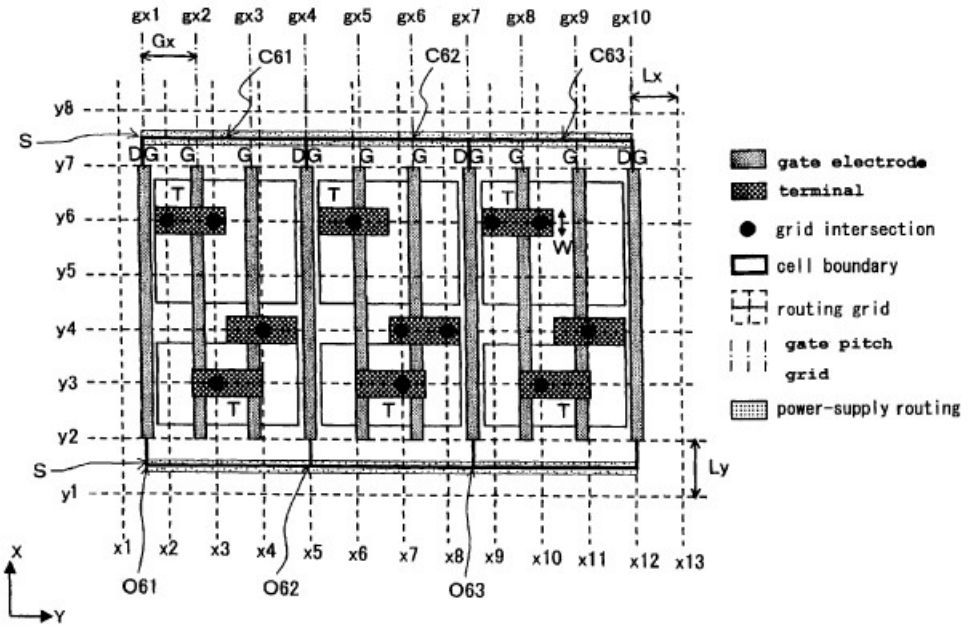
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| [15.1] wherein a first non-gate linear conductive segment is positioned beside the first outer positioned one of the active linear conductive segments, and | At least under Tela’s apparent infringement theory, Ichiryu discloses and/or renders obvious wherein a first non-gate linear conductive segment is positioned beside the first outer positioned one of the active linear conductive segments.<br><br>Ichiryu describes and depicts multiple dummy gates beside linear conductive segments, e.g. “dummy gate eletrodes” or “DG.”<br><br>*See, e.g.*:<br><br>“[A]s the miniaturization of the process [continues], a precision in a finished dimension of the gate electrode ultimately obtained is deteriorated by an optical proximity effect when an interval between the gate electrodes and gate lengths of the gate electrodes are irregular in their patterns. When the precision in the finished dimension of the gate electrode is deteriorated, performances of respective transistors of the semiconductor integrated circuit are increasingly inconstant, which leads to an increased variation in a performance of the semiconductor integrate[d] circuit.” (Ichiryu at 2:23-32).<br><br>“[A]s recited in No. H10-32253 of the Publication of the Unexamined Japanese Patent Applications, the interval and the length of the gate electrodes in each standard cell are set regular so that the OPC is processed per standard cell in the conventional technology.” (Ichiryu at 2:37-41).“<br><br>Dummy gate electrodes DG are provided on cell boundaries of standard cells C41’, C4[2]’ and C43’ disposed on the upper side in FIG. 18. These dummy gate electrodes DG are shared between the adjacent standard cells. The gate electrodes G and the dummy gate electrodes DG are respectively equally spaced, and their gate [] lengths are equal.” (Ichiryu at 2:45-50).<br><br>“[W]hen the regions R1, R2 and R3 for adjusting the cell width to the integral multiple of the routing grid interval are provided, the gate electrode located on the cell boundary of the standard cell cannot be shared. There is a possibility that the dummy electrodes DG are located with less than a minimum interval allowed in a design rule therebetween, which results in an error in the design rule. In order to |

| '012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | avoid the foregoing error in the design rule, it is necessary to enlarge the gate length, for example, in the same manner as the dummy gate DG2 disposed on the lower side in FIG. 18." (Ichiryu at 3:7-16).<br><br>"Though the gate interval in each standard cell can be maintained at the constant level when such the gate length enlargement is executed, the gate length becomes irregular at the dummy gate electrodes DG2, which results in the imprecision of the finished dimension of the gate electrodes. Further, the OPC cannot be processed in each standard cell due to the different gate lengths in the dummy gate electrodes DG in each standard cell and the dummy gate electrodes DG2 adjacent thereto." (Ichiryu at 3:17-25).<br><br>"The standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes…." (Ichiryu at 6:20-21).<br><br>"A standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes, wherein gate pitches of some of the gate electrodes are set to values different to the routing grid interval set along the X direction in parallel with the power-supply wiring of the standard cell, and a cell width along the X direction in parallel with the power-supply wiring of the standard cell is set to an integral multiple of a minimum value of the gate pitches of the gate electrodes set to the values different to the routing grid interval set along the X direction." (Ichiryu at 6:26-35).<br><br>"[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, a precision in a finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell." (Ichiryu at 6:41-45).<br><br>"A standard cell according to the present invention comprises a plurality of gate electrodes and a plurality of dummy gate electrodes, wherein a cell width in the X direction in parallel with the power-supply wiring of the standard cell is an integral multiple of a minimum gate pitch of gate pitches of the gate electrodes and the dummy gate electrodes different to the routing grid interval along the X direction." (Ichiryu at 6:46-52). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell. As another advantage, the provision of the dummy gate electrodes can further improve the regularity of the gate length and gate interval, which largely contributes to the facilitation of the OPC process in each standard cell.” (Ichiryu at 6:58-65).<br><br>“The gate pitches of the standard cell are all preferably equal. Thereby, the pattern of the gate electrodes can impart a perfect regularity to the gate pitches, and the precision in the finished dimension of the gate electrodes can be further improved.” (Ichiryu at 6:66-7:3).<br><br>“Further, because the pattern of the gate electrodes can have the regularity, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be performed in each standard cell.” (Ichiryu at 8:21-24).<br><br>“Referring to reference symbols in FIG. 11, x1-x13 denote routing grids for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, y1-y8 denote routing grids disposed in parallel with the X direction and adjacent to one another in the Y direction, gx1-gx10 denote grids of gate pitches for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, C61, C62 and C63 are standard cells, O61, O62 and O63 are respective origins of the standard cells C61, C62 and C63, … G denotes a gate electrode, and DG denotes a dummy gate electrode.” (Ichiryu at 14:32-44).<br><br>“In the standard cells C61, C62 and C63, gate lengths and gate intervals of the gate electrode G and dummy gate electrode DG are constant, and a cell width of the standard cells C61, C62 and C63 in the X direction is an integral multiple of a minimum value of a gate pitch Gx (value of gate pitch=gate length+gate interval) (In FIG. 11, the cell width of the standard cells C61, C62 and C63 is three times as wide as Gx).” (Ichiryu at 14:45-51). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “Not only inside the respective standard cells C61, C62 and C63, but also among the standard cells C61, C62 and C63 to one another, the gate lengths and the gate intervals are equal in the patterns of the gate electrodes and the dummy gate electrodes.” (Ichiryu at 15:47-51).<br><br>“In the embodiment 5, the gate lengths are all equal in the gate electrodes and the dummy gate electrodes….” (Ichiryu at 16:10-11).<br><br>“In FIG. 14, a reference symbol C81 denotes a standard cell. The standard cell C81 comprises gate electrodes G, dummy gate electrodes DG and two gate electrodes G2 having a gate length different to those of the gate electrode G and the dummy gate electrode DG, wherein a width of the gate electrode G2 is set so that a cell width of the standard cell C81 in the X direction is an integral multiple of the gate pitch Gx. In FIG. 14, the cell width of the standard cell C81 is nine times as wide as the gate pitch Gx. The width of the gate electrode G2 is thus set because a processing speed is expected to be faster when the cell width of each cell in the X direction is the integral multiple of the gate pitch Gx than when the cell width of each cell takes an arbitrary value in the placement using the conventional automatic placement & routing tool. However, the width of the gate electrode G2 is not necessarily set in the foregoing manner.” (Ichiryu at 16:15-30).<br><br>“As described, in the case of including the standard cell comprising the gate electrodes having the different gate lengths….” (Ichiryu at 16:32-34).<br><br>“[T]he embodiment 5 can be applied in the same manner to a cell structure where the dummy gate electrodes having the different gate lengths are provided and a cell structure where the gate electrodes and the dummy gate electrodes having the different gate intervals are provided. The description of the embodiment 5 is premised on the provision of the dummy gates DG….” (Ichiryu at 16:53-59).<br><br>“In the constitution, the distance from the cell boundary of each standard cell to the gate electrode in the closest vicinity and the distance from the cell boundary of another standard cell adjacent thereto to the gate electrode in the closest vicinity are constant.” (Ichiryu at 16:65-17:2). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “For example, a distance from each of the cell boundary of the standard cells C61, C62 and C63 to the gate electrode in the X direction is ‘Gx-gate length/2’ and constant even in the constitution shown in FIG. 11 where the dummy gate electrodes DG are not provided. A distance between a transistor disposed at the end of each standard cell and the gate electrode G of the adjacent standard cell is ‘2Gx-gate length’ and constant. For example, even in the case where the dummy gate electrode DG is not provided in the constitution described referring to FIG. 11, the distance from each of the cell boundary of the respective standard cells C61, C62 and C63 to the gate electrode G located at the end of each of the standard cells in the X direction is constant at (Gx-gate length/2). Further, the distance from the gate electrode G located at the end of each of the standard cells to the gate electrode G located at the end of each of adjacent standard cells in the X direction is constant at (2Gx-gate length).” (Ichiryu at 17:6-22).<br><br>“Further, in the embodiment 6, the standard cells described in the embodiments 1 and 5 are used. The gate lengths and the gate intervals are thereby equal in the patterns of the gate electrodes of the placed standard cells C91, C92 and C93, which leads to the improvement of the precision in the finished dimension of the gate electrodes. The improvement of the precision in the finished dimension of the gate electrodes can be realized not only inside each of the standard cells C91, C92 and C93 but also between the standard cells.” (Ichiryu at 18:1-9).<br><br>“[W]hen the standard cells are adjacently located, the gate lengths and the gate intervals in the patterns of the gate electrodes and the dummy gate electrodes are the same as when they are located alone.” (Ichiryu at 18:10-13). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | F I G. 11<br>  <br><br>(Ichiryu Fig. 11).<br>*See also* Ichiryu at Figs. 1, 2, 3, 8, 12, 13, 14.<br>This limitation also would have been obvious to a person of ordinary skill in the art based on (1) Ichiryu alone; and/or (2) the teachings with respect to this claim element as detailed in the cover document of Respondent’s invalidity contentions and Respondent’s other invalidity charts. |

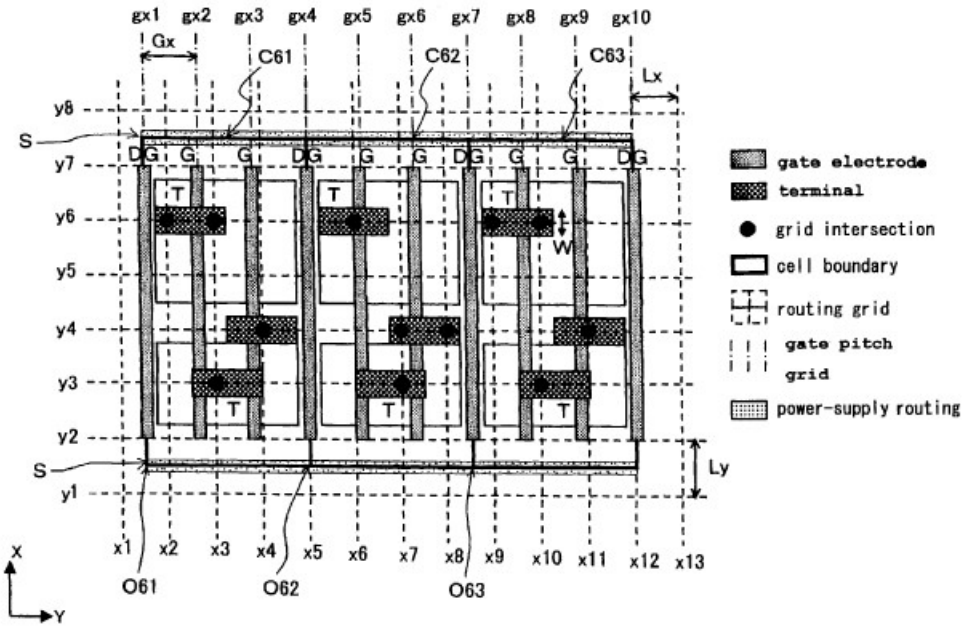
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| [15.2] wherein a second non-gate linear conductive segment is positioned beside the second outer positioned one of the active linear conductive segments. | At least under Tela’s apparent infringement theory, Ichiryu discloses and/or renders obvious wherein a second non-gate linear conductive segment is positioned beside the second outer positioned one of the active linear conductive segments.<br><br>Ichiryu describes and depicts multiple dummy gates beside linear conductive segments, e.g. “dummy gate eletrodes” or “DG.”<br><br>*See, e.g.*:<br><br>“[A]s the miniaturization of the process [continues], a precision in a finished dimension of the gate electrode ultimately obtained is deteriorated by an optical proximity effect when an interval between the gate electrodes and gate lengths of the gate electrodes are irregular in their patterns. When the precision in the finished dimension of the gate electrode is deteriorated, performances of respective transistors of the semiconductor integrated circuit are increasingly inconstant, which leads to an increased variation in a performance of the semiconductor integrate[d] circuit.” (Ichiryu at 2:23-32).<br><br>“[A]s recited in No. H10-32253 of the Publication of the Unexamined Japanese Patent Applications, the interval and the length of the gate electrodes in each standard cell are set regular so that the OPC is processed per standard cell in the conventional technology.” (Ichiryu at 2:37-41).“<br><br>Dummy gate electrodes DG are provided on cell boundaries of standard cells C41’, C4[2]’ and C43’ disposed on the upper side in FIG. 18. These dummy gate electrodes DG are shared between the adjacent standard cells. The gate electrodes G and the dummy gate electrodes DG are respectively equally spaced, and their gate [] lengths are equal.” (Ichiryu at 2:45-50).<br><br>“[W]hen the regions R1, R2 and R3 for adjusting the cell width to the integral multiple of the routing grid interval are provided, the gate electrode located on the cell boundary of the standard cell cannot be shared. There is a possibility that the dummy electrodes DG are located with less than a minimum interval allowed in a design rule therebetween, which results in an error in the design rule. In order to |

| '012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | avoid the foregoing error in the design rule, it is necessary to enlarge the gate length, for example, in the same manner as the dummy gate DG2 disposed on the lower side in FIG. 18." (Ichiryu at 3:7-16).<br><br>"Though the gate interval in each standard cell can be maintained at the constant level when such the gate length enlargement is executed, the gate length becomes irregular at the dummy gate electrodes DG2, which results in the imprecision of the finished dimension of the gate electrodes. Further, the OPC cannot be processed in each standard cell due to the different gate lengths in the dummy gate electrodes DG in each standard cell and the dummy gate electrodes DG2 adjacent thereto." (Ichiryu at 3:17-25).<br><br>"The standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes…." (Ichiryu at 6:20-21).<br><br>"A standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes, wherein gate pitches of some of the gate electrodes are set to values different to the routing grid interval set along the X direction in parallel with the power-supply wiring of the standard cell, and a cell width along the X direction in parallel with the power-supply wiring of the standard cell is set to an integral multiple of a minimum value of the gate pitches of the gate electrodes set to the values different to the routing grid interval set along the X direction." (Ichiryu at 6:26-35).<br><br>"[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, a precision in a finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell." (Ichiryu at 6:41-45).<br><br>"A standard cell according to the present invention comprises a plurality of gate electrodes and a plurality of dummy gate electrodes, wherein a cell width in the X direction in parallel with the power-supply wiring of the standard cell is an integral multiple of a minimum gate pitch of gate pitches of the gate electrodes and the dummy gate electrodes different to the routing grid interval along the X direction." (Ichiryu at 6:46-52). |

| '012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | "[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell. As another advantage, the provision of the dummy gate electrodes can further improve the regularity of the gate length and gate interval, which largely contributes to the facilitation of the OPC process in each standard cell." (Ichiryu at 6:58-65).<br><br>"The gate pitches of the standard cell are all preferably equal. Thereby, the pattern of the gate electrodes can impart a perfect regularity to the gate pitches, and the precision in the finished dimension of the gate electrodes can be further improved." (Ichiryu at 6:66-7:3).<br><br>"Further, because the pattern of the gate electrodes can have the regularity, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be performed in each standard cell." (Ichiryu at 8:21-24).<br><br>"Referring to reference symbols in FIG. 11, x1-x13 denote routing grids for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, y1-y8 denote routing grids disposed in parallel with the X direction and adjacent to one another in the Y direction, gx1-gx10 denote grids of gate pitches for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, C61, C62 and C63 are standard cells, O61, O62 and O63 are respective origins of the standard cells C61, C62 and C63, … G denotes a gate electrode, and DG denotes a dummy gate electrode." (Ichiryu at 14:32-44).<br><br>"In the standard cells C61, C62 and C63, gate lengths and gate intervals of the gate electrode G and dummy gate electrode DG are constant, and a cell width of the standard cells C61, C62 and C63 in the X direction is an integral multiple of a minimum value of a gate pitch Gx (value of gate pitch=gate length+gate interval) (In FIG. 11, the cell width of the standard cells C61, C62 and C63 is three times as wide as Gx)." (Ichiryu at 14:45-51). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “Not only inside the respective standard cells C61, C62 and C63, but also among the standard cells C61, C62 and C63 to one another, the gate lengths and the gate intervals are equal in the patterns of the gate electrodes and the dummy gate electrodes.” (Ichiryu at 15:47-51).<br><br>“In the embodiment 5, the gate lengths are all equal in the gate electrodes and the dummy gate electrodes….” (Ichiryu at 16:10-11).<br><br>“In FIG. 14, a reference symbol C81 denotes a standard cell. The standard cell C81 comprises gate electrodes G, dummy gate electrodes DG and two gate electrodes G2 having a gate length different to those of the gate electrode G and the dummy gate electrode DG, wherein a width of the gate electrode G2 is set so that a cell width of the standard cell C81 in the X direction is an integral multiple of the gate pitch Gx. In FIG. 14, the cell width of the standard cell C81 is nine times as wide as the gate pitch Gx. The width of the gate electrode G2 is thus set because a processing speed is expected to be faster when the cell width of each cell in the X direction is the integral multiple of the gate pitch Gx than when the cell width of each cell takes an arbitrary value in the placement using the conventional automatic placement & routing tool. However, the width of the gate electrode G2 is not necessarily set in the foregoing manner.” (Ichiryu at 16:15-30).<br><br>“As described, in the case of including the standard cell comprising the gate electrodes having the different gate lengths….” (Ichiryu at 16:32-34).<br><br>“[T]he embodiment 5 can be applied in the same manner to a cell structure where the dummy gate electrodes having the different gate lengths are provided and a cell structure where the gate electrodes and the dummy gate electrodes having the different gate intervals are provided. The description of the embodiment 5 is premised on the provision of the dummy gates DG….” (Ichiryu at 16:53-59).<br><br>“In the constitution, the distance from the cell boundary of each standard cell to the gate electrode in the closest vicinity and the distance from the cell boundary of another standard cell adjacent thereto to the gate electrode in the closest vicinity are constant.” (Ichiryu at 16:65-17:2). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “For example, a distance from each of the cell boundary of the standard cells C61, C62 and C63 to the gate electrode in the X direction is ‘Gx-gate length/2’ and constant even in the constitution shown in FIG. 11 where the dummy gate electrodes DG are not provided. A distance between a transistor disposed at the end of each standard cell and the gate electrode G of the adjacent standard cell is ‘2Gx-gate length’ and constant. For example, even in the case where the dummy gate electrode DG is not provided in the constitution described referring to FIG. 11, the distance from each of the cell boundary of the respective standard cells C61, C62 and C63 to the gate electrode G located at the end of each of the standard cells in the X direction is constant at (Gx-gate length/2). Further, the distance from the gate electrode G located at the end of each of the standard cells to the gate electrode G located at the end of each of adjacent standard cells in the X direction is constant at (2Gx-gate length).” (Ichiryu at 17:6-22).<br><br>“Further, in the embodiment 6, the standard cells described in the embodiments 1 and 5 are used. The gate lengths and the gate intervals are thereby equal in the patterns of the gate electrodes of the placed standard cells C91, C92 and C93, which leads to the improvement of the precision in the finished dimension of the gate electrodes. The improvement of the precision in the finished dimension of the gate electrodes can be realized not only inside each of the standard cells C91, C92 and C93 but also between the standard cells.” (Ichiryu at 18:1-9).<br><br>“[W]hen the standard cells are adjacently located, the gate lengths and the gate intervals in the patterns of the gate electrodes and the dummy gate electrodes are the same as when they are located alone.” (Ichiryu at 18:10-13). |

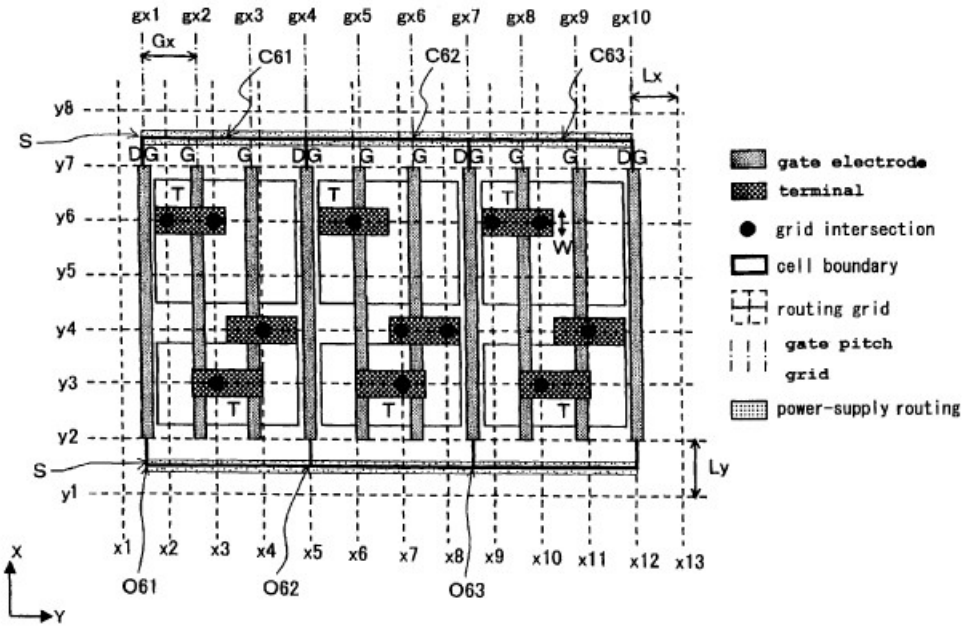
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | F I G. 11<br>  <br><br>(Ichiryu Fig. 11).<br>*See also* Ichiryu at Figs. 1, 2, 3, 8, 12, 13, 14.<br>This limitation also would have been obvious to a person of ordinary skill in the art based on (1) Ichiryu alone; and/or (2) the teachings with respect to this claim element as detailed in the cover document of Respondent’s invalidity contentions and Respondent’s other invalidity charts. |

| '012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| 16. An integrated circuit device as recited in claim 15, wherein the plurality of linear conductive segments are positioned in a side-by-side manner according to a substantially equal centerline-to-centerline spacing as measured in a second direction perpendicular to the first direction. | At least under Tela's apparent infringement theory, Ichiryu discloses and/or renders obvious an integrated circuit device as recited in claim 15, wherein the plurality of linear conductive segments are positioned in a side-by-side manner according to a substantially equal centerline-to-centerline spacing as measured in a second direction perpendicular to the first direction.<br><br>Ichiryu describes and depicts multiple gate electrodes that form transistors of different types and are placed on a grid having the same pitch and width, and thus equal side-to-side spacing.<br><br>*See, e.g.*:<br><br>"[A]s recited in No. H10-32253 of the Publication of the Unexamined Japanese Patent Applications, the interval and the length of the gate electrodes in each standard cell are set regular so that the OPC is processed per standard cell in the conventional technology." (Ichiryu at 2:37-41).<br><br>"The standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes…." (Ichiryu at 6:20-21).<br><br>"A standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes, wherein gate pitches of some of the gate electrodes are set to values different to the routing grid interval set along the X direction in parallel with the power-supply wiring of the standard cell, and a cell width along the X direction in parallel with the power-supply wiring of the standard cell is set to an integral multiple of a minimum value of the gate pitches of the gate electrodes set to the values different to the routing grid interval set along the X direction." (Ichiryu at 6:26-35).<br><br>"[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, a precision in a finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell." (Ichiryu at 6:41-45).<br><br>"A standard cell according to the present invention comprises a plurality of gate electrodes and a plurality of dummy gate electrodes, wherein a cell width in the X direction in parallel with the |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | power-supply wiring of the standard cell is an integral multiple of a minimum gate pitch of gate pitches of the gate electrodes and the dummy gate electrodes different to the routing grid interval along the X direction.” (Ichiryu at 6:46-52).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:58-62).<br><br>“The gate pitches of the standard cell are all preferably equal. Thereby, the pattern of the gate electrodes can impart a perfect regularity to the gate pitches, and the precision in the finished dimension of the gate electrodes can be further improved.” (Ichiryu at 6:66-7:3).<br><br>“Further, because the pattern of the gate electrodes can have the regularity, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be performed in each standard cell.” (Ichiryu at 8:21-24).<br><br>“Referring to reference symbols in FIG. 11, x1-x13 denote routing grids for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, y1-y8 denote routing grids disposed in parallel with the X direction and adjacent to one another in the Y direction, gx1-gx10 denote grids of gate pitches for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, C61, C62 and C63 are standard cells, O61, O62 and O63 are respective origins of the standard cells C61, C62 and C63, … G denotes a gate electrode, and DG denotes a dummy gate electrode.” (Ichiryu at 14:32-44).<br><br>“In the standard cells C61, C62 and C63, gate lengths and gate intervals of the gate electrode G and dummy gate electrode DG are constant, and a cell width of the standard cells C61, C62 and C63 in the X direction is an integral multiple of a minimum value of a gate pitch Gx (value of gate pitch=gate length+gate interval) (In FIG. 11, the cell width of the standard cells C61, C62 and C63 is three times as wide as Gx).” (Ichiryu at 14:45-51). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “Not only inside the respective standard cells C61, C62 and C63, but also among the standard cells C61, C62 and C63 to one another, the gate lengths and the gate intervals are equal in the patterns of the gate electrodes and the dummy gate electrodes.” (Ichiryu at 15:47-51).<br><br>“In the embodiment 5, the gate lengths are all equal in the gate electrodes and the dummy gate electrodes….” (Ichiryu at 16:10-11).<br><br>“In FIG. 14, a reference symbol C81 denotes a standard cell. The standard cell C81 comprises gate electrodes G, dummy gate electrodes DG and two gate electrodes G2 having a gate length different to those of the gate electrode G and the dummy gate electrode DG, wherein a width of the gate electrode G2 is set so that a cell width of the standard cell C81 in the X direction is an integral multiple of the gate pitch Gx. In FIG. 14, the cell width of the standard cell C81 is nine times as wide as the gate pitch Gx. The width of the gate electrode G2 is thus set because a processing speed is expected to be faster when the cell width of each cell in the X direction is the integral multiple of the gate pitch Gx than when the cell width of each cell takes an arbitrary value in the placement using the conventional automatic placement & routing tool. However, the width of the gate electrode G2 is not necessarily set in the foregoing manner.” (Ichiryu at 16:15-30).<br><br>“In the constitution, the distance from the cell boundary of each standard cell to the gate electrode in the closest vicinity and the distance from the cell boundary of another standard cell adjacent thereto to the gate electrode in the closest vicinity are constant.” (Ichiryu at 16:65-17:2).<br><br>“For example, a distance from each of the cell boundary of the standard cells C61, C62 and C63 to the gate electrode in the X direction is ‘Gx-gate length/2’ and constant even in the constitution shown in FIG. 11 where the dummy gate electrodes DG are not provided. A distance between a transistor disposed at the end of each standard cell and the gate electrode G of the adjacent standard cell is ‘2Gx-gate length’ and constant. For example, even in the case where the dummy gate electrode DG is not provided in the constitution described referring to FIG. 11, the distance from each of the cell boundary of the respective standard cells C61, C62 and C63 to the gate electrode G located at the end of each of the standard cells in the X direction is constant at (Gx-gate length/2). Further, the distance from the gate electrode G located at the end of each of the standard cells to the gate electrode G |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | located at the end of each of adjacent standard cells in the X direction is constant at (2Gx-gate length).” (Ichiryu at 17:6-22).<br><br>“Further, in the embodiment 6, the standard cells described in the embodiments 1 and 5 are used. The gate lengths and the gate intervals are thereby equal in the patterns of the gate electrodes of the placed standard cells C91, C92 and C93, which leads to the improvement of the precision in the finished dimension of the gate electrodes. The improvement of the precision in the finished dimension of the gate electrodes can be realized not only inside each of the standard cells C91, C92 and C93 but also between the standard cells.” (Ichiryu at 18:1-9).<br><br>“[W]hen the standard cells are adjacently located, the gate lengths and the gate intervals in the patterns of the gate electrodes and the dummy gate electrodes are the same as when they are located alone.” (Ichiryu at 18:10-13). |

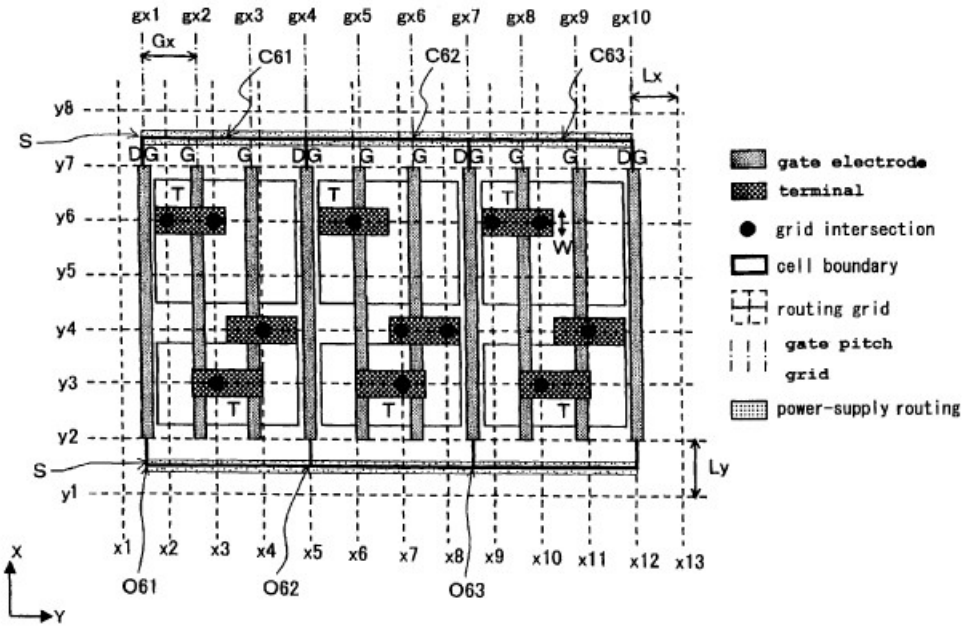
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | F I G. 11<br>  <br><br>(Ichiryu Fig. 11).<br>*See also* Ichiryu at Figs. 1, 2, 3, 8, 12, 13, 14.<br>This limitation also would have been obvious to a person of ordinary skill in the art based on (1) Ichiryu alone; and/or (2) the teachings with respect to this claim element as detailed in the cover document of Respondent’s invalidity contentions and Respondent’s other invalidity charts. |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| 17. An integrated circuit device as recited in claim 16, wherein the substantially equal centerline-to-centerline spacing as measured in the second direction is less than 360 nanometers. | At least under Tela’s apparent infringement theory, Ichiryu discloses and/or renders obvious an integrated circuit device as recited in claim 16, wherein the substantially equal centerline-to-centerline spacing as measured in the second direction is less than 360 nanometers.<br><br>Ichiryu describes layout techniques for gate electrodes, including that they have equal centerline-to-centerline spacing.<br><br>*See, e.g.*:<br><br>“[A]s recited in No. H10-32253 of the Publication of the Unexamined Japanese Patent Applications, the interval and the length of the gate electrodes in each standard cell are set regular so that the OPC is processed per standard cell in the conventional technology.” (Ichiryu at 2:37-41).<br><br>“The standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes….” (Ichiryu at 6:20-21).<br><br>“A standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes, wherein gate pitches of some of the gate electrodes are set to values different to the routing grid interval set along the X direction in parallel with the power-supply wiring of the standard cell, and a cell width along the X direction in parallel with the power-supply wiring of the standard cell is set to an integral multiple of a minimum value of the gate pitches of the gate electrodes set to the values different to the routing grid interval set along the X direction.” (Ichiryu at 6:26-35).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, a precision in a finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:41-45).<br><br>“A standard cell according to the present invention comprises a plurality of gate electrodes and a plurality of dummy gate electrodes, wherein a cell width in the X direction in parallel with the power-supply wiring of the standard cell is an integral multiple of a minimum gate pitch of gate |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | pitches of the gate electrodes and the dummy gate electrodes different to the routing grid interval along the X direction.” (Ichiryu at 6:46-52).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:58-62).<br><br>“The gate pitches of the standard cell are all preferably equal. Thereby, the pattern of the gate electrodes can impart a perfect regularity to the gate pitches, and the precision in the finished dimension of the gate electrodes can be further improved.” (Ichiryu at 6:66-7:3).<br><br>“Further, because the pattern of the gate electrodes can have the regularity, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be performed in each standard cell.” (Ichiryu at 8:21-24).<br><br>“Referring to reference symbols in FIG. 11, x1-x13 denote routing grids for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, y1-y8 denote routing grids disposed in parallel with the X direction and adjacent to one another in the Y direction, gx1-gx10 denote grids of gate pitches for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, C61, C62 and C63 are standard cells, O61, O62 and O63 are respective origins of the standard cells C61, C62 and C63, … G denotes a gate electrode, and DG denotes a dummy gate electrode.” (Ichiryu at 14:32-44).<br><br>“In the standard cells C61, C62 and C63, gate lengths and gate intervals of the gate electrode G and dummy gate electrode DG are constant, and a cell width of the standard cells C61, C62 and C63 in the X direction is an integral multiple of a minimum value of a gate pitch Gx (value of gate pitch=gate length+gate interval) (In FIG. 11, the cell width of the standard cells C61, C62 and C63 is three times as wide as Gx).” (Ichiryu at 14:45-51). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “Not only inside the respective standard cells C61, C62 and C63, but also among the standard cells C61, C62 and C63 to one another, the gate lengths and the gate intervals are equal in the patterns of the gate electrodes and the dummy gate electrodes.” (Ichiryu at 15:47-51).<br><br>“In the embodiment 5, the gate lengths are all equal in the gate electrodes and the dummy gate electrodes….” (Ichiryu at 16:10-11).<br><br>“In FIG. 14, a reference symbol C81 denotes a standard cell. The standard cell C81 comprises gate electrodes G, dummy gate electrodes DG and two gate electrodes G2 having a gate length different to those of the gate electrode G and the dummy gate electrode DG, wherein a width of the gate electrode G2 is set so that a cell width of the standard cell C81 in the X direction is an integral multiple of the gate pitch Gx. In FIG. 14, the cell width of the standard cell C81 is nine times as wide as the gate pitch Gx. The width of the gate electrode G2 is thus set because a processing speed is expected to be faster when the cell width of each cell in the X direction is the integral multiple of the gate pitch Gx than when the cell width of each cell takes an arbitrary value in the placement using the conventional automatic placement & routing tool. However, the width of the gate electrode G2 is not necessarily set in the foregoing manner.” (Ichiryu at 16:15-30).<br><br>“In the constitution, the distance from the cell boundary of each standard cell to the gate electrode in the closest vicinity and the distance from the cell boundary of another standard cell adjacent thereto to the gate electrode in the closest vicinity are constant.” (Ichiryu at 16:65-17:2).<br><br>“For example, a distance from each of the cell boundary of the standard cells C61, C62 and C63 to the gate electrode in the X direction is ‘Gx-gate length/2’ and constant even in the constitution shown in FIG. 11 where the dummy gate electrodes DG are not provided. A distance between a transistor disposed at the end of each standard cell and the gate electrode G of the adjacent standard cell is ‘2Gx-gate length’ and constant. For example, even in the case where the dummy gate electrode DG is not provided in the constitution described referring to FIG. 11, the distance from each of the cell boundary of the respective standard cells C61, C62 and C63 to the gate electrode G located at the end of each of the standard cells in the X direction is constant at (Gx-gate length/2). Further, the distance from the gate electrode G located at the end of each of the standard cells to the gate electrode G |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | located at the end of each of adjacent standard cells in the X direction is constant at (2Gx-gate length).” (Ichiryu at 17:6-22).<br><br>“Further, in the embodiment 6, the standard cells described in the embodiments 1 and 5 are used. The gate lengths and the gate intervals are thereby equal in the patterns of the gate electrodes of the placed standard cells C91, C92 and C93, which leads to the improvement of the precision in the finished dimension of the gate electrodes. The improvement of the precision in the finished dimension of the gate electrodes can be realized not only inside each of the standard cells C91, C92 and C93 but also between the standard cells.” (Ichiryu at 18:1-9).<br><br>“[W]hen the standard cells are adjacently located, the gate lengths and the gate intervals in the patterns of the gate electrodes and the dummy gate electrodes are the same as when they are located alone.” (Ichiryu at 18:10-13). |

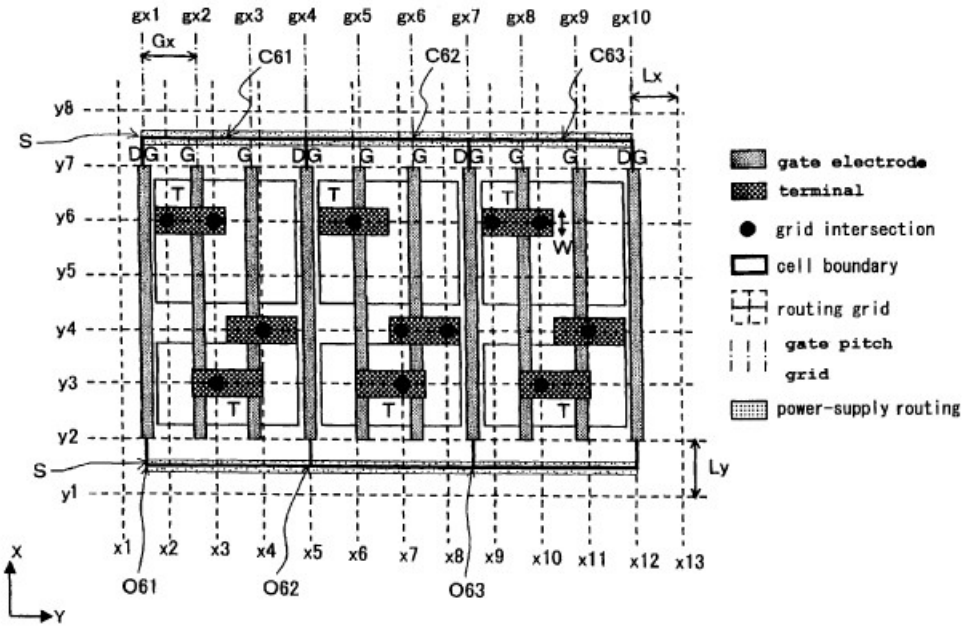
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | F I G. 11<br>  <br><br>(Ichiryu Fig. 11).<br>*See also* Ichiryu at Figs. 1, 2, 3, 8, 12, 13, 14.<br>This limitation also would have been obvious to a person of ordinary skill in the art based on (1) Ichiryu alone; and/or (2) the teachings with respect to this claim element as detailed in the cover document of Respondent’s invalidity contentions and Respondent’s other invalidity charts. |

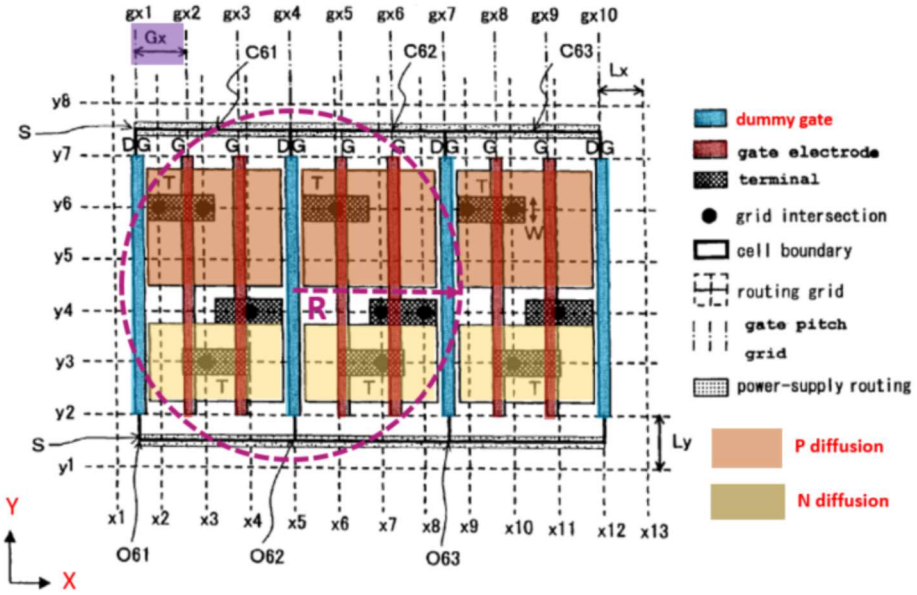
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| 18. An integrated circuit device as recited in claim 16, wherein a side-to-side spacing between each adjacently positioned pair of the plurality of linear conductive segments is less than 360 nanometers, wherein the side-to-side spacing is measured in the second direction. | At least under Tela’s apparent infringement theory, Ichiryu discloses and/or renders obvious an integrated circuit device as recited in claim 16, wherein a side-to-side spacing between each adjacently positioned pair of the plurality of linear conductive segments is less than 360 nanometers, wherein the side-to-side spacing is measured in the second direction.<br><br>Ichiryu describes and depicts multiple gate electrodes that form transistors of different types and are placed on a grid having the same pitch and width, and thus equal side-to-side spacing.<br><br>*See, e.g.*:<br><br>“[A]s recited in No. H10-32253 of the Publication of the Unexamined Japanese Patent Applications, the interval and the length of the gate electrodes in each standard cell are set regular so that the OPC is processed per standard cell in the conventional technology.” (Ichiryu at 2:37-41).<br><br>“The standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes….” (Ichiryu at 6:20-21).<br><br>“A standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes, wherein gate pitches of some of the gate electrodes are set to values different to the routing grid interval set along the X direction in parallel with the power-supply wiring of the standard cell, and a cell width along the X direction in parallel with the power-supply wiring of the standard cell is set to an integral multiple of a minimum value of the gate pitches of the gate electrodes set to the values different to the routing grid interval set along the X direction.” (Ichiryu at 6:26-35).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, a precision in a finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:41-45).<br><br>“A standard cell according to the present invention comprises a plurality of gate electrodes and a plurality of dummy gate electrodes, wherein a cell width in the X direction in parallel with the |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | power-supply wiring of the standard cell is an integral multiple of a minimum gate pitch of gate pitches of the gate electrodes and the dummy gate electrodes different to the routing grid interval along the X direction.” (Ichiryu at 6:46-52).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:58-62).<br><br>“The gate pitches of the standard cell are all preferably equal. Thereby, the pattern of the gate electrodes can impart a perfect regularity to the gate pitches, and the precision in the finished dimension of the gate electrodes can be further improved.” (Ichiryu at 6:66-7:3).<br><br>“Further, because the pattern of the gate electrodes can have the regularity, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be performed in each standard cell.” (Ichiryu at 8:21-24).<br><br>“Referring to reference symbols in FIG. 11, x1-x13 denote routing grids for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, y1-y8 denote routing grids disposed in parallel with the X direction and adjacent to one another in the Y direction, gx1-gx10 denote grids of gate pitches for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, C61, C62 and C63 are standard cells, O61, O62 and O63 are respective origins of the standard cells C61, C62 and C63, … G denotes a gate electrode, and DG denotes a dummy gate electrode.” (Ichiryu at 14:32-44).<br><br>“In the standard cells C61, C62 and C63, gate lengths and gate intervals of the gate electrode G and dummy gate electrode DG are constant, and a cell width of the standard cells C61, C62 and C63 in the X direction is an integral multiple of a minimum value of a gate pitch Gx (value of gate pitch=gate length+gate interval) (In FIG. 11, the cell width of the standard cells C61, C62 and C63 is three times as wide as Gx).” (Ichiryu at 14:45-51). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “Not only inside the respective standard cells C61, C62 and C63, but also among the standard cells C61, C62 and C63 to one another, the gate lengths and the gate intervals are equal in the patterns of the gate electrodes and the dummy gate electrodes.” (Ichiryu at 15:47-51).<br><br>“In the embodiment 5, the gate lengths are all equal in the gate electrodes and the dummy gate electrodes….” (Ichiryu at 16:10-11).<br><br>“In FIG. 14, a reference symbol C81 denotes a standard cell. The standard cell C81 comprises gate electrodes G, dummy gate electrodes DG and two gate electrodes G2 having a gate length different to those of the gate electrode G and the dummy gate electrode DG, wherein a width of the gate electrode G2 is set so that a cell width of the standard cell C81 in the X direction is an integral multiple of the gate pitch Gx. In FIG. 14, the cell width of the standard cell C81 is nine times as wide as the gate pitch Gx. The width of the gate electrode G2 is thus set because a processing speed is expected to be faster when the cell width of each cell in the X direction is the integral multiple of the gate pitch Gx than when the cell width of each cell takes an arbitrary value in the placement using the conventional automatic placement & routing tool. However, the width of the gate electrode G2 is not necessarily set in the foregoing manner.” (Ichiryu at 16:15-30).<br><br>“In the constitution, the distance from the cell boundary of each standard cell to the gate electrode in the closest vicinity and the distance from the cell boundary of another standard cell adjacent thereto to the gate electrode in the closest vicinity are constant.” (Ichiryu at 16:65-17:2).<br><br>“For example, a distance from each of the cell boundary of the standard cells C61, C62 and C63 to the gate electrode in the X direction is ‘Gx-gate length/2’ and constant even in the constitution shown in FIG. 11 where the dummy gate electrodes DG are not provided. A distance between a transistor disposed at the end of each standard cell and the gate electrode G of the adjacent standard cell is ‘2Gx-gate length’ and constant. For example, even in the case where the dummy gate electrode DG is not provided in the constitution described referring to FIG. 11, the distance from each of the cell boundary of the respective standard cells C61, C62 and C63 to the gate electrode G located at the end of each of the standard cells in the X direction is constant at (Gx-gate length/2). Further, the distance from the gate electrode G located at the end of each of the standard cells to the gate electrode G |

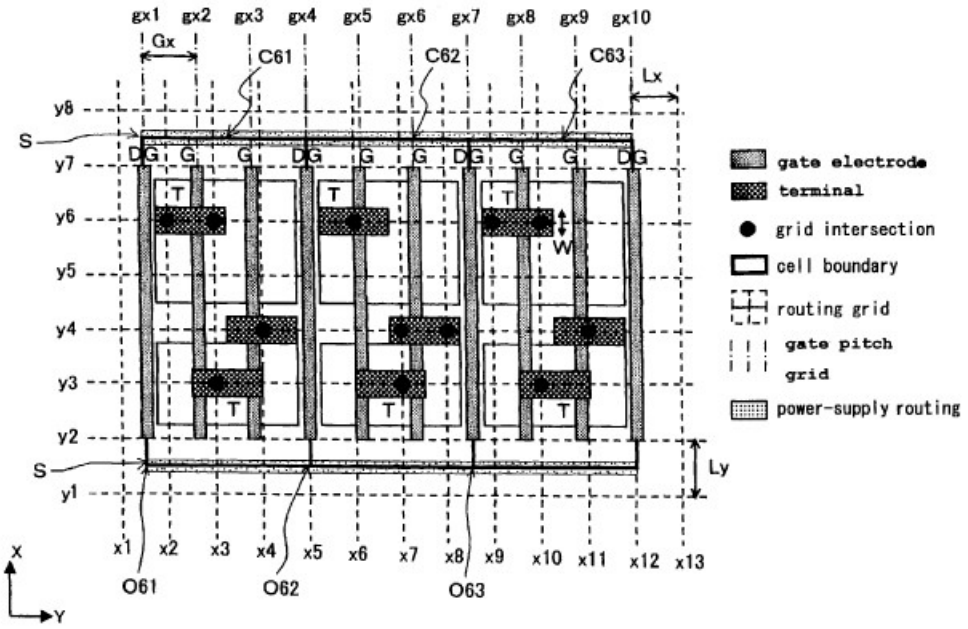
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | located at the end of each of adjacent standard cells in the X direction is constant at (2Gx-gate length).” (Ichiryu at 17:6-22).<br><br>“Further, in the embodiment 6, the standard cells described in the embodiments 1 and 5 are used. The gate lengths and the gate intervals are thereby equal in the patterns of the gate electrodes of the placed standard cells C91, C92 and C93, which leads to the improvement of the precision in the finished dimension of the gate electrodes. The improvement of the precision in the finished dimension of the gate electrodes can be realized not only inside each of the standard cells C91, C92 and C93 but also between the standard cells.” (Ichiryu at 18:1-9).<br><br>“[W]hen the standard cells are adjacently located, the gate lengths and the gate intervals in the patterns of the gate electrodes and the dummy gate electrodes are the same as when they are located alone.” (Ichiryu at 18:10-13). |

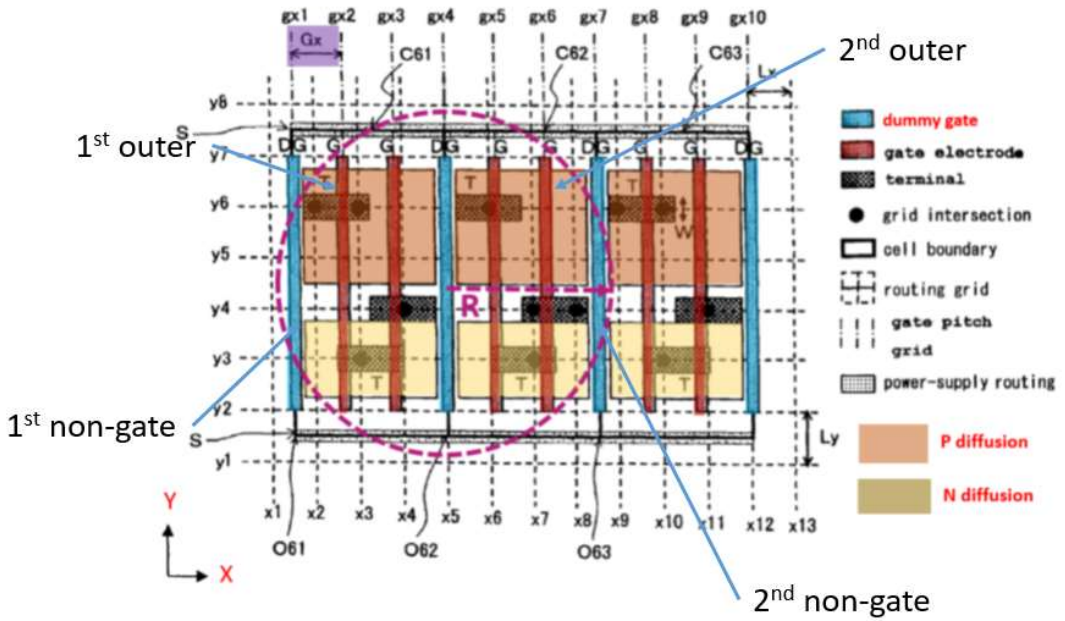
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | F I G. 11<br>  <br><br>(Ichiryu Fig. 11).<br>*See also* Ichiryu at Figs. 1, 2, 3, 8, 12, 13, 14.<br>This limitation also would have been obvious to a person of ordinary skill in the art based on (1) Ichiryu alone; and/or (2) the teachings with respect to this claim element as detailed in the cover document of Respondent’s invalidity contentions and Respondent’s other invalidity charts. |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| 19. An integrated circuit device as recited in claim 2, wherein at least three of the plurality of linear conductive segments are non-gate linear conductive segments, wherein each non-gate linear conductive segment does not form a gate electrode of a transistor device. | At least under Tela’s apparent infringement theory, Ichiryu discloses and/or renders obvious an integrated circuit device as recited in claim 2, wherein at least three of the plurality of linear conductive segments are non-gate linear conductive segments, wherein each non-gate linear conductive segment does not form a gate electrode of a transistor device.<br><br>F I G. 11<br>  <br><br><br>Ichiryu describes and depicts multiple dummy gates, e.g. “dummy gate eletrodes” or “DG.”<br><br>*See, e.g.*:<br><br>“Dummy gate electrodes DG are provided on cell boundaries of standard cells C41’, C4[2]’ and C43’ disposed on the upper side in FIG. 18. These dummy gate electrodes DG are shared between |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | the adjacent standard cells. The gate electrodes G and the dummy gate electrodes DG are respectively equally spaced, and their gate [] lengths are equal.” (Ichiryu at 2:45-50).<br><br>“[W]hen the regions R1, R2 and R3 for adjusting the cell width to the integral multiple of the routing grid interval are provided, the gate electrode located on the cell boundary of the standard cell cannot be shared. There is a possibility that the dummy electrodes DG are located with less than a minimum interval allowed in a design rule therebetween, which results in an error in the design rule. In order to avoid the foregoing error in the design rule, it is necessary to enlarge the gate length, for example, in the same manner as the dummy gate DG2 disposed on the lower side in FIG. 18.” (Ichiryu at 3:7-16).<br><br>“Though the gate interval in each standard cell can be maintained at the constant level when such the gate length enlargement is executed, the gate length becomes irregular at the dummy gate electrodes DG2, which results in the imprecision of the finished dimension of the gate electrodes. Further, the OPC cannot be processed in each standard cell due to the different gate lengths in the dummy gate electrodes DG in each standard cell and the dummy gate electrodes DG2 adjacent thereto.” (Ichiryu at 3:17-25).<br><br>“A standard cell according to the present invention comprises a plurality of gate electrodes and a plurality of dummy gate electrodes, wherein a cell width in the X direction in parallel with the power-supply wiring of the standard cell is an integral multiple of a minimum gate pitch of gate pitches of the gate electrodes and the dummy gate electrodes different to the routing grid interval along the X direction.” (Ichiryu at 6:46-52).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell. As another advantage, the provision of the dummy gate electrodes can further improve the regularity of the gate length and gate interval, which largely contributes to the facilitation of the OPC process in each standard cell.” (Ichiryu at 6:58-65).<br><br>“Referring to reference symbols in FIG. 11, x1-x13 denote routing grids for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, y1- |

| '012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | y8 denote routing grids disposed in parallel with the X direction and adjacent to one another in the Y direction, gx1-gx10 denote grids of gate pitches for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, C61, C62 and C63 are standard cells, O61, O62 and O63 are respective origins of the standard cells C61, C62 and C63, … G denotes a gate electrode, and DG denotes a dummy gate electrode." (Ichiryu at 14:32-44).<br><br>"Not only inside the respective standard cells C61, C62 and C63, but also among the standard cells C61, C62 and C63 to one another, the gate lengths and the gate intervals are equal in the patterns of the gate electrodes and the dummy gate electrodes." (Ichiryu at 15:47-51).<br><br>"In FIG. 14, a reference symbol C81 denotes a standard cell. The standard cell C81 comprises gate electrodes G, dummy gate electrodes DG and two gate electrodes G2 having a gate length different to those of the gate electrode G and the dummy gate electrode DG, wherein a width of the gate electrode G2 is set so that a cell width of the standard cell C81 in the X direction is an integral multiple of the gate pitch Gx. In FIG. 14, the cell width of the standard cell C81 is nine times as wide as the gate pitch Gx. The width of the gate electrode G2 is thus set because a processing speed is expected to be faster when the cell width of each cell in the X direction is the integral multiple of the gate pitch Gx than when the cell width of each cell takes an arbitrary value in the placement using the conventional automatic placement & routing tool. However, the width of the gate electrode G2 is not necessarily set in the foregoing manner." (Ichiryu at 16:15-30).<br><br>"[T]he embodiment 5 can be applied in the same manner to a cell structure where the dummy gate electrodes having the different gate lengths are provided and a cell structure where the gate electrodes and the dummy gate electrodes having the different gate intervals are provided. The description of the embodiment 5 is premised on the provision of the dummy gates DG…." (Ichiryu at 16:53-59).<br><br>"[W]hen the standard cells are adjacently located, the gate lengths and the gate intervals in the patterns of the gate electrodes and the dummy gate electrodes are the same as when they are located alone." (Ichiryu at 18:10-13). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | F I G. 11<br>  <br><br>(Ichiryu Fig. 11).<br>*See also* Ichiryu at Figs. 1, 2, 3, 8, 12, 13, 14.<br>This limitation also would have been obvious to a person of ordinary skill in the art based on (1) Ichiryu alone; and/or (2) the teachings with respect to this claim element as detailed in the cover document of Respondent’s invalidity contentions and Respondent’s other invalidity charts. |

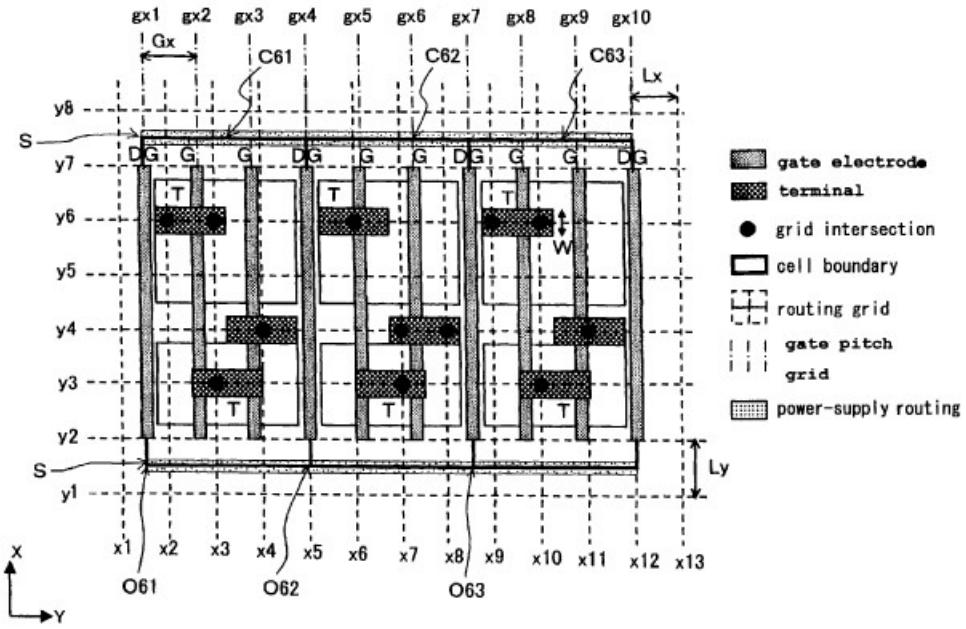
| '012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| 20. An integrated circuit device as recited in claim 19, wherein the plurality of linear conductive segments are positioned in a side-by-side manner so as to include a first outer positioned one of the active linear conductive segments and a second outer positioned one of the active linear conductive segments, and | At least under Tela's apparent infringement theory, Ichiryu discloses and/or renders obvious an integrated circuit device as recited in claim 19, wherein the plurality of linear conductive segments are positioned in a side-by-side manner so as to include a first outer positioned one of the active linear conductive segments and a second outer positioned one of the active linear conductive segments.<br><br>F I G. 11<br>  <br><br><br>*See, e.g.*:<br><br>"[A]s the miniaturization of the process [continues], a precision in a finished dimension of the gate electrode ultimately obtained is deteriorated by an optical proximity effect when an interval between the gate electrodes and gate lengths of the gate electrodes are irregular in their patterns. When the |

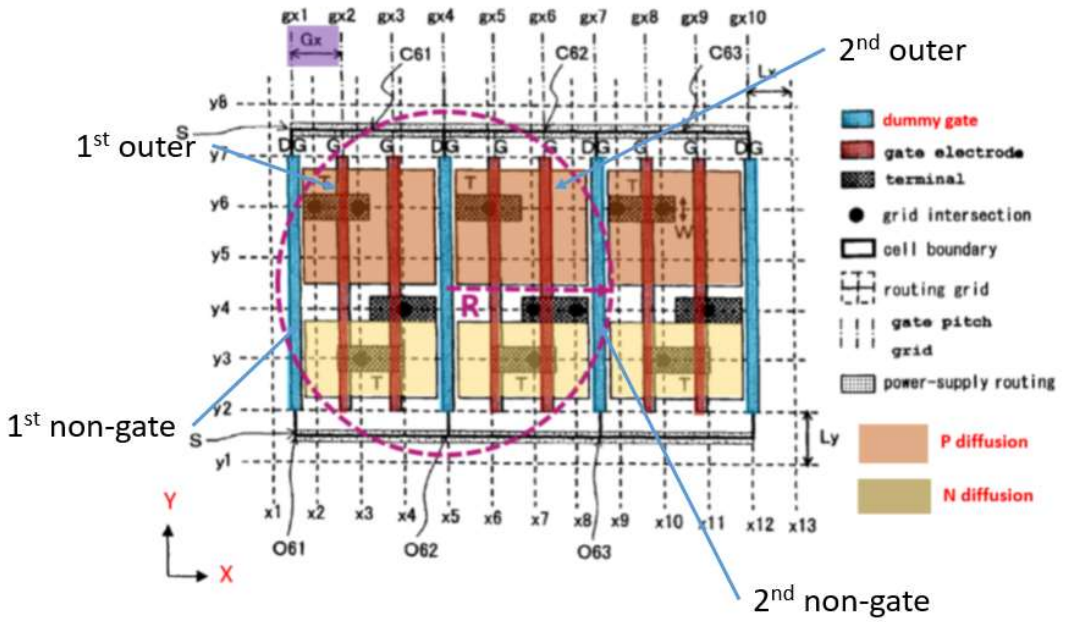
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | precision in the finished dimension of the gate electrode is deteriorated, performances of respective transistors of the semiconductor integrated circuit are increasingly inconstant, which leads to an increased variation in a performance of the semiconductor integrate[d] circuit.” (Ichiryu at 2:23-32).<br><br>“[A]s recited in No. H10-32253 of the Publication of the Unexamined Japanese Patent Applications, the interval and the length of the gate electrodes in each standard cell are set regular so that the OPC is processed per standard cell in the conventional technology.” (Ichiryu at 2:37-41).<br><br>“The standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes….” (Ichiryu at 6:20-21).<br><br>“A standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes, wherein gate pitches of some of the gate electrodes are set to values different to the routing grid interval set along the X direction in parallel with the power-supply wiring of the standard cell, and a cell width along the X direction in parallel with the power-supply wiring of the standard cell is set to an integral multiple of a minimum value of the gate pitches of the gate electrodes set to the values different to the routing grid interval set along the X direction.” (Ichiryu at 6:26-35).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, a precision in a finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:41-45).<br><br>“A standard cell according to the present invention comprises a plurality of gate electrodes and a plurality of dummy gate electrodes, wherein a cell width in the X direction in parallel with the power-supply wiring of the standard cell is an integral multiple of a minimum gate pitch of gate pitches of the gate electrodes and the dummy gate electrodes different to the routing grid interval along the X direction.” (Ichiryu at 6:46-52). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:58-62).<br><br>“The gate pitches of the standard cell are all preferably equal. Thereby, the pattern of the gate electrodes can impart a perfect regularity to the gate pitches, and the precision in the finished dimension of the gate electrodes can be further improved.” (Ichiryu at 6:66-7:3).<br><br>“Further, because the pattern of the gate electrodes can have the regularity, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be performed in each standard cell.” (Ichiryu at 8:21-24).<br><br>“Referring to reference symbols in FIG. 11, x1-x13 denote routing grids for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, y1-y8 denote routing grids disposed in parallel with the X direction and adjacent to one another in the Y direction, gx1-gx10 denote grids of gate pitches for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, C61, C62 and C63 are standard cells, O61, O62 and O63 are respective origins of the standard cells C61, C62 and C63, … G denotes a gate electrode, and DG denotes a dummy gate electrode.” (Ichiryu at 14:32-44).<br><br>“In the standard cells C61, C62 and C63, gate lengths and gate intervals of the gate electrode G and dummy gate electrode DG are constant, and a cell width of the standard cells C61, C62 and C63 in the X direction is an integral multiple of a minimum value of a gate pitch Gx (value of gate pitch=gate length+gate interval) (In FIG. 11, the cell width of the standard cells C61, C62 and C63 is three times as wide as Gx).” (Ichiryu at 14:45-51).<br><br>“Not only inside the respective standard cells C61, C62 and C63, but also among the standard cells C61, C62 and C63 to one another, the gate lengths and the gate intervals are equal in the patterns of the gate electrodes and the dummy gate electrodes.” (Ichiryu at 15:47-51). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “In the embodiment 5, the gate lengths are all equal in the gate electrodes and the dummy gate electrodes….” (Ichiryu at 16:10-11).<br><br>“In FIG. 14, a reference symbol C81 denotes a standard cell. The standard cell C81 comprises gate electrodes G, dummy gate electrodes DG and two gate electrodes G2 having a gate length different to those of the gate electrode G and the dummy gate electrode DG, wherein a width of the gate electrode G2 is set so that a cell width of the standard cell C81 in the X direction is an integral multiple of the gate pitch Gx. In FIG. 14, the cell width of the standard cell C81 is nine times as wide as the gate pitch Gx. The width of the gate electrode G2 is thus set because a processing speed is expected to be faster when the cell width of each cell in the X direction is the integral multiple of the gate pitch Gx than when the cell width of each cell takes an arbitrary value in the placement using the conventional automatic placement & routing tool. However, the width of the gate electrode G2 is not necessarily set in the foregoing manner.” (Ichiryu at 16:15-30).<br><br>“As described, in the case of including the standard cell comprising the gate electrodes having the different gate lengths….” (Ichiryu at 16:32-34).<br><br>“In the constitution, the distance from the cell boundary of each standard cell to the gate electrode in the closest vicinity and the distance from the cell boundary of another standard cell adjacent thereto to the gate electrode in the closest vicinity are constant.” (Ichiryu at 16:65-17:2).<br><br>“For example, a distance from each of the cell boundary of the standard cells C61, C62 and C63 to the gate electrode in the X direction is ‘Gx-gate length/2’ and constant even in the constitution shown in FIG. 11 where the dummy gate electrodes DG are not provided. A distance between a transistor disposed at the end of each standard cell and the gate electrode G of the adjacent standard cell is ‘2Gx-gate length’ and constant. For example, even in the case where the dummy gate electrode DG is not provided in the constitution described referring to FIG. 11, the distance from each of the cell boundary of the respective standard cells C61, C62 and C63 to the gate electrode G located at the end of each of the standard cells in the X direction is constant at (Gx-gate length/2). Further, the distance from the gate electrode G located at the end of each of the standard cells to the gate electrode G |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | located at the end of each of adjacent standard cells in the X direction is constant at (2Gx-gate length).” (Ichiryu at 17:6-22).<br><br>“Further, in the embodiment 6, the standard cells described in the embodiments 1 and 5 are used. The gate lengths and the gate intervals are thereby equal in the patterns of the gate electrodes of the placed standard cells C91, C92 and C93, which leads to the improvement of the precision in the finished dimension of the gate electrodes. The improvement of the precision in the finished dimension of the gate electrodes can be realized not only inside each of the standard cells C91, C92 and C93 but also between the standard cells.” (Ichiryu at 18:1-9).<br><br>“[W]hen the standard cells are adjacently located, the gate lengths and the gate intervals in the patterns of the gate electrodes and the dummy gate electrodes are the same as when they are located alone.” (Ichiryu at 18:10-13). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | F I G. 11<br>  <br><br>(Ichiryu Fig. 11).<br>*See also* Ichiryu at Figs. 1, 2, 3, 8, 12, 13, 14.<br>This limitation also would have been obvious to a person of ordinary skill in the art based on (1) Ichiryu alone; and/or (2) the teachings with respect to this claim element as detailed in the cover document of Respondent’s invalidity contentions and Respondent’s other invalidity charts. |

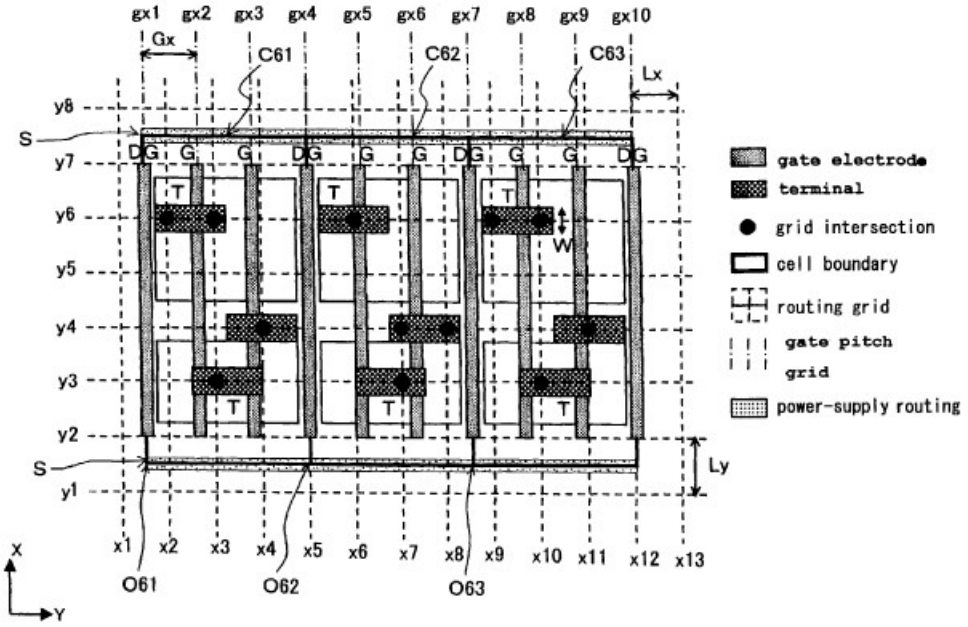
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| [20.1] wherein a first non-gate linear conductive segment is positioned beside the first outer positioned one of the active linear conductive segments, and | At least under Tela’s apparent infringement theory, Ichiryu discloses and/or renders obvious wherein a first non-gate linear conductive segment is positioned beside the first outer positioned one of the active linear conductive segments.<br><br>F I G. 11<br>  <br><br><br>*See, e.g.*:<br><br>“[A]s the miniaturization of the process [continues], a precision in a finished dimension of the gate electrode ultimately obtained is deteriorated by an optical proximity effect when an interval between the gate electrodes and gate lengths of the gate electrodes are irregular in their patterns. When the precision in the finished dimension of the gate electrode is deteriorated, performances of respective |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | transistors of the semiconductor integrated circuit are increasingly inconstant, which leads to an increased variation in a performance of the semiconductor integrate[d] circuit.” (Ichiryu at 2:23-32).<br><br>“[A]s recited in No. H10-32253 of the Publication of the Unexamined Japanese Patent Applications, the interval and the length of the gate electrodes in each standard cell are set regular so that the OPC is processed per standard cell in the conventional technology.” (Ichiryu at 2:37-41).“<br><br>Dummy gate electrodes DG are provided on cell boundaries of standard cells C41’, C4[2]’ and C43’ disposed on the upper side in FIG. 18. These dummy gate electrodes DG are shared between the adjacent standard cells. The gate electrodes G and the dummy gate electrodes DG are respectively equally spaced, and their gate [] lengths are equal.” (Ichiryu at 2:45-50).<br><br>“[W]hen the regions R1, R2 and R3 for adjusting the cell width to the integral multiple of the routing grid interval are provided, the gate electrode located on the cell boundary of the standard cell cannot be shared. There is a possibility that the dummy electrodes DG are located with less than a minimum interval allowed in a design rule therebetween, which results in an error in the design rule. In order to avoid the foregoing error in the design rule, it is necessary to enlarge the gate length, for example, in the same manner as the dummy gate DG2 disposed on the lower side in FIG. 18.” (Ichiryu at 3:7-16).<br><br>“Though the gate interval in each standard cell can be maintained at the constant level when such the gate length enlargement is executed, the gate length becomes irregular at the dummy gate electrodes DG2, which results in the imprecision of the finished dimension of the gate electrodes. Further, the OPC cannot be processed in each standard cell due to the different gate lengths in the dummy gate electrodes DG in each standard cell and the dummy gate electrodes DG2 adjacent thereto.” (Ichiryu at 3:17-25).<br><br>“The standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes….” (Ichiryu at 6:20-21).<br><br>“A standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes, wherein gate pitches of some of the gate electrodes are set to values different to the |

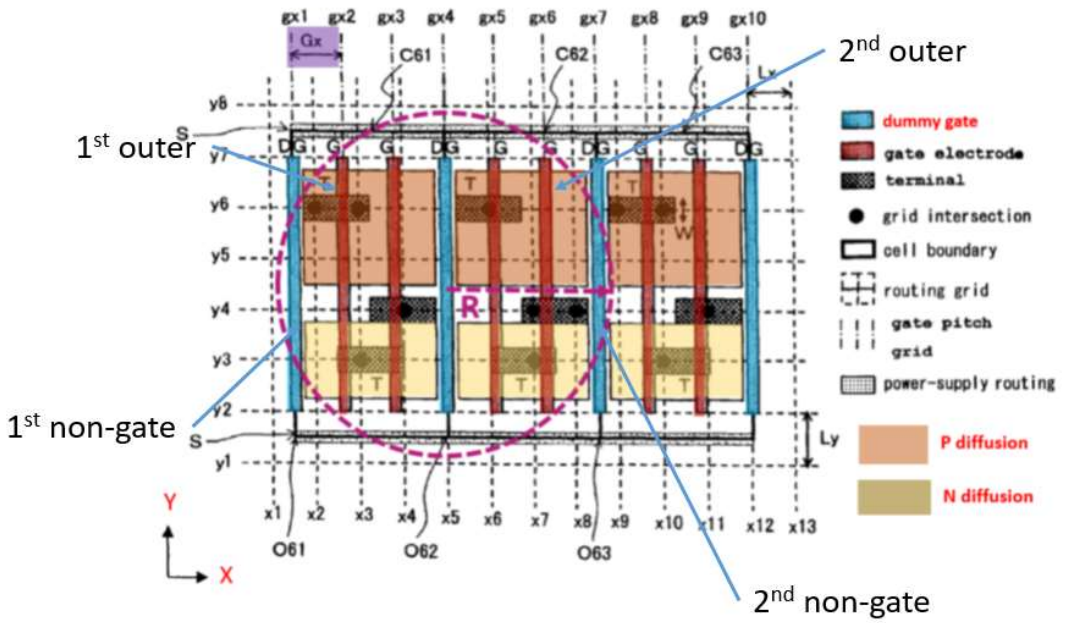
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | routing grid interval set along the X direction in parallel with the power-supply wiring of the standard cell, and a cell width along the X direction in parallel with the power-supply wiring of the standard cell is set to an integral multiple of a minimum value of the gate pitches of the gate electrodes set to the values different to the routing grid interval set along the X direction.” (Ichiryu at 6:26-35).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, a precision in a finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:41-45).<br><br>“A standard cell according to the present invention comprises a plurality of gate electrodes and a plurality of dummy gate electrodes, wherein a cell width in the X direction in parallel with the power-supply wiring of the standard cell is an integral multiple of a minimum gate pitch of gate pitches of the gate electrodes and the dummy gate electrodes different to the routing grid interval along the X direction.” (Ichiryu at 6:46-52).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell. As another advantage, the provision of the dummy gate electrodes can further improve the regularity of the gate length and gate interval, which largely contributes to the facilitation of the OPC process in each standard cell.” (Ichiryu at 6:58-65).<br><br>“The gate pitches of the standard cell are all preferably equal. Thereby, the pattern of the gate electrodes can impart a perfect regularity to the gate pitches, and the precision in the finished dimension of the gate electrodes can be further improved.” (Ichiryu at 6:66-7:3).<br><br>“Further, because the pattern of the gate electrodes can have the regularity, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be performed in each standard cell.” (Ichiryu at 8:21-24). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “Referring to reference symbols in FIG. 11, x1-x13 denote routing grids for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, y1-y8 denote routing grids disposed in parallel with the X direction and adjacent to one another in the Y direction, gx1-gx10 denote grids of gate pitches for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, C61, C62 and C63 are standard cells, O61, O62 and O63 are respective origins of the standard cells C61, C62 and C63, … G denotes a gate electrode, and DG denotes a dummy gate electrode.” (Ichiryu at 14:32-44).<br><br>“In the standard cells C61, C62 and C63, gate lengths and gate intervals of the gate electrode G and dummy gate electrode DG are constant, and a cell width of the standard cells C61, C62 and C63 in the X direction is an integral multiple of a minimum value of a gate pitch Gx (value of gate pitch=gate length+gate interval) (In FIG. 11, the cell width of the standard cells C61, C62 and C63 is three times as wide as Gx).” (Ichiryu at 14:45-51).<br><br>“Not only inside the respective standard cells C61, C62 and C63, but also among the standard cells C61, C62 and C63 to one another, the gate lengths and the gate intervals are equal in the patterns of the gate electrodes and the dummy gate electrodes.” (Ichiryu at 15:47-51).<br><br>“In the embodiment 5, the gate lengths are all equal in the gate electrodes and the dummy gate electrodes….” (Ichiryu at 16:10-11).<br><br>“In FIG. 14, a reference symbol C81 denotes a standard cell. The standard cell C81 comprises gate electrodes G, dummy gate electrodes DG and two gate electrodes G2 having a gate length different to those of the gate electrode G and the dummy gate electrode DG, wherein a width of the gate electrode G2 is set so that a cell width of the standard cell C81 in the X direction is an integral multiple of the gate pitch Gx. In FIG. 14, the cell width of the standard cell C81 is nine times as wide as the gate pitch Gx. The width of the gate electrode G2 is thus set because a processing speed is expected to be faster when the cell width of each cell in the X direction is the integral multiple of the gate pitch Gx than when the cell width of each cell takes an arbitrary value in the placement using the |

| '012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | conventional automatic placement & routing tool. However, the width of the gate electrode G2 is not necessarily set in the foregoing manner." (Ichiryu at 16:15-30).<br><br>"As described, in the case of including the standard cell comprising the gate electrodes having the different gate lengths…." (Ichiryu at 16:32-34).<br><br>"[T]he embodiment 5 can be applied in the same manner to a cell structure where the dummy gate electrodes having the different gate lengths are provided and a cell structure where the gate electrodes and the dummy gate electrodes having the different gate intervals are provided. The description of the embodiment 5 is premised on the provision of the dummy gates DG…." (Ichiryu at 16:53-59).<br><br>"In the constitution, the distance from the cell boundary of each standard cell to the gate electrode in the closest vicinity and the distance from the cell boundary of another standard cell adjacent thereto to the gate electrode in the closest vicinity are constant." (Ichiryu at 16:65-17:2).<br><br>"For example, a distance from each of the cell boundary of the standard cells C61, C62 and C63 to the gate electrode in the X direction is 'Gx-gate length/2' and constant even in the constitution shown in FIG. 11 where the dummy gate electrodes DG are not provided. A distance between a transistor disposed at the end of each standard cell and the gate electrode G of the adjacent standard cell is '2Gx-gate length' and constant. For example, even in the case where the dummy gate electrode DG is not provided in the constitution described referring to FIG. 11, the distance from each of the cell boundary of the respective standard cells C61, C62 and C63 to the gate electrode G located at the end of each of the standard cells in the X direction is constant at (Gx-gate length/2). Further, the distance from the gate electrode G located at the end of each of the standard cells to the gate electrode G located at the end of each of adjacent standard cells in the X direction is constant at (2Gx-gate length)." (Ichiryu at 17:6-22).<br><br>"Further, in the embodiment 6, the standard cells described in the embodiments 1 and 5 are used. The gate lengths and the gate intervals are thereby equal in the patterns of the gate electrodes of the placed standard cells C91, C92 and C93, which leads to the improvement of the precision in the |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | finished dimension of the gate electrodes. The improvement of the precision in the finished dimension of the gate electrodes can be realized not only inside each of the standard cells C91, C92 and C93 but also between the standard cells.” (Ichiryu at 18:1-9).<br><br>“[W]hen the standard cells are adjacently located, the gate lengths and the gate intervals in the patterns of the gate electrodes and the dummy gate electrodes are the same as when they are located alone.” (Ichiryu at 18:10-13).<br><br>F I G. 11<br>  <br> |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | (Ichiryu Fig. 11).<br><br>*See also* Ichiryu at Figs. 1, 2, 3, 8, 12, 13, 14.<br><br>This limitation also would have been obvious to a person of ordinary skill in the art based on (1) Ichiryu alone; and/or (2) the teachings with respect to this claim element as detailed in the cover document of Respondent’s invalidity contentions and Respondent’s other invalidity charts. |
| [20.2] wherein a second non-gate linear conductive segment is positioned beside the second outer positioned one of the active linear conductive segments. | At least under Tela’s apparent infringement theory, Ichiryu discloses and/or renders obvious wherein a second non-gate linear conductive segment is positioned beside the second outer positioned one of the active linear conductive segments. |

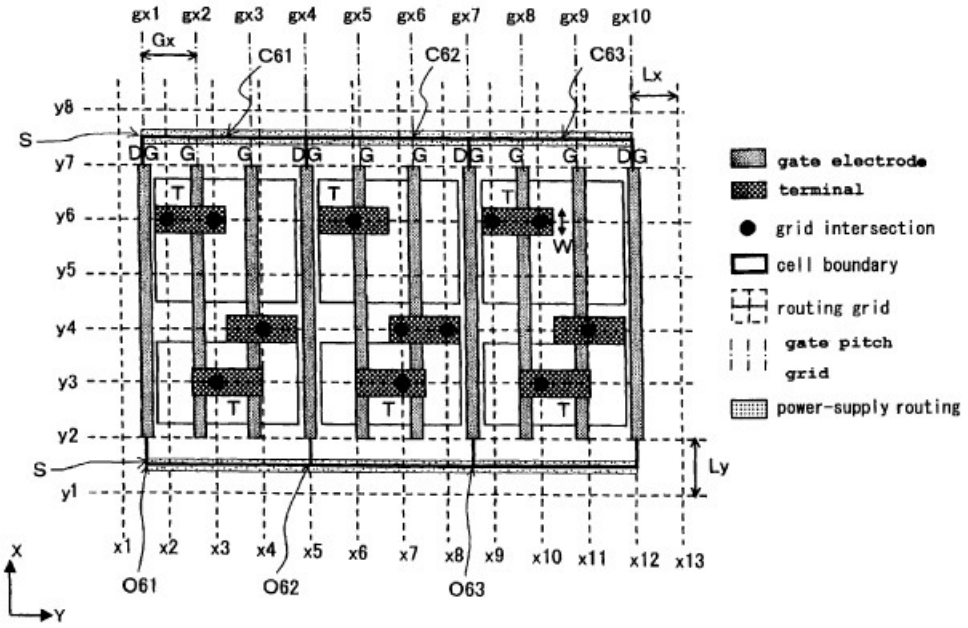
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | F I G. 11<br>  <br><br>*See, e.g.*:<br>“[A]s the miniaturization of the process [continues], a precision in a finished dimension of the gate electrode ultimately obtained is deteriorated by an optical proximity effect when an interval between the gate electrodes and gate lengths of the gate electrodes are irregular in their patterns. When the precision in the finished dimension of the gate electrode is deteriorated, performances of respective transistors of the semiconductor integrated circuit are increasingly inconstant, which leads to an increased variation in a performance of the semiconductor integrate[d] circuit.” (Ichiryu at 2:23-32). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “[A]s recited in No. H10-32253 of the Publication of the Unexamined Japanese Patent Applications, the interval and the length of the gate electrodes in each standard cell are set regular so that the OPC is processed per standard cell in the conventional technology.” (Ichiryu at 2:37-41).“<br><br>Dummy gate electrodes DG are provided on cell boundaries of standard cells C41’, C4[2]’ and C43’ disposed on the upper side in FIG. 18. These dummy gate electrodes DG are shared between the adjacent standard cells. The gate electrodes G and the dummy gate electrodes DG are respectively equally spaced, and their gate [] lengths are equal.” (Ichiryu at 2:45-50).<br><br>“[W]hen the regions R1, R2 and R3 for adjusting the cell width to the integral multiple of the routing grid interval are provided, the gate electrode located on the cell boundary of the standard cell cannot be shared. There is a possibility that the dummy electrodes DG are located with less than a minimum interval allowed in a design rule therebetween, which results in an error in the design rule. In order to avoid the foregoing error in the design rule, it is necessary to enlarge the gate length, for example, in the same manner as the dummy gate DG2 disposed on the lower side in FIG. 18.” (Ichiryu at 3:7-16).<br><br>“Though the gate interval in each standard cell can be maintained at the constant level when such the gate length enlargement is executed, the gate length becomes irregular at the dummy gate electrodes DG2, which results in the imprecision of the finished dimension of the gate electrodes. Further, the OPC cannot be processed in each standard cell due to the different gate lengths in the dummy gate electrodes DG in each standard cell and the dummy gate electrodes DG2 adjacent thereto.” (Ichiryu at 3:17-25).<br><br>“The standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes….” (Ichiryu at 6:20-21).<br><br>“A standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes, wherein gate pitches of some of the gate electrodes are set to values different to the routing grid interval set along the X direction in parallel with the power-supply wiring of the standard cell, and a cell width along the X direction in parallel with the power-supply wiring of the standard cell is set to an integral multiple of a minimum value of the gate pitches of the gate |

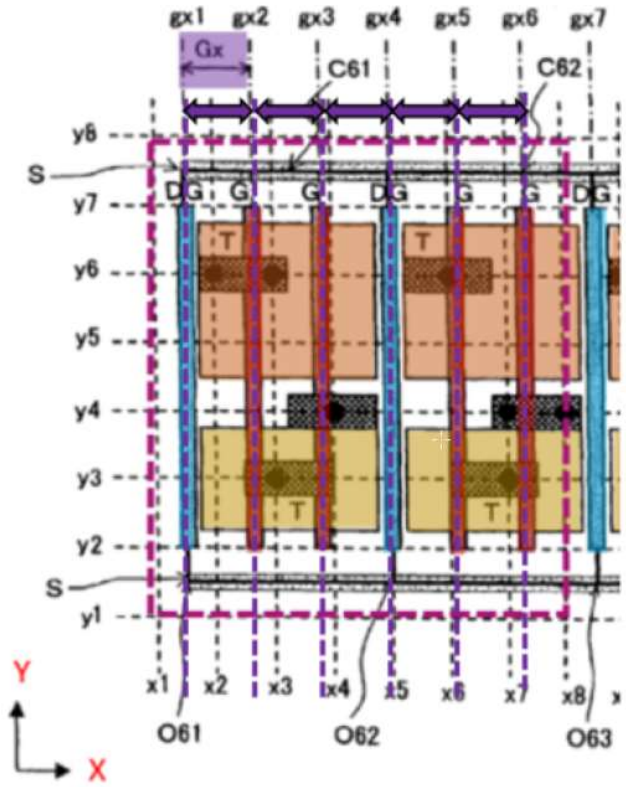
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | electrodes set to the values different to the routing grid interval set along the X direction.” (Ichiryu at 6:26-35).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, a precision in a finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:41-45).<br><br>“A standard cell according to the present invention comprises a plurality of gate electrodes and a plurality of dummy gate electrodes, wherein a cell width in the X direction in parallel with the power-supply wiring of the standard cell is an integral multiple of a minimum gate pitch of gate pitches of the gate electrodes and the dummy gate electrodes different to the routing grid interval along the X direction.” (Ichiryu at 6:46-52).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell. As another advantage, the provision of the dummy gate electrodes can further improve the regularity of the gate length and gate interval, which largely contributes to the facilitation of the OPC process in each standard cell.” (Ichiryu at 6:58-65).<br><br>“The gate pitches of the standard cell are all preferably equal. Thereby, the pattern of the gate electrodes can impart a perfect regularity to the gate pitches, and the precision in the finished dimension of the gate electrodes can be further improved.” (Ichiryu at 6:66-7:3).<br><br>“Further, because the pattern of the gate electrodes can have the regularity, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be performed in each standard cell.” (Ichiryu at 8:21-24).<br><br>“Referring to reference symbols in FIG. 11, x1-x13 denote routing grids for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, y1-y8 denote routing grids disposed in parallel with the X direction and adjacent to one another in the Y direction, gx1-gx10 denote grids of gate pitches for the automatic placement & routing disposed in |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | parallel with the Y direction and adjacent to one another in the X direction, C61, C62 and C63 are standard cells, O61, O62 and O63 are respective origins of the standard cells C61, C62 and C63, … G denotes a gate electrode, and DG denotes a dummy gate electrode.” (Ichiryu at 14:32-44).<br><br>“In the standard cells C61, C62 and C63, gate lengths and gate intervals of the gate electrode G and dummy gate electrode DG are constant, and a cell width of the standard cells C61, C62 and C63 in the X direction is an integral multiple of a minimum value of a gate pitch Gx (value of gate pitch=gate length+gate interval) (In FIG. 11, the cell width of the standard cells C61, C62 and C63 is three times as wide as Gx).” (Ichiryu at 14:45-51).<br><br>“Not only inside the respective standard cells C61, C62 and C63, but also among the standard cells C61, C62 and C63 to one another, the gate lengths and the gate intervals are equal in the patterns of the gate electrodes and the dummy gate electrodes.” (Ichiryu at 15:47-51).<br><br>“In the embodiment 5, the gate lengths are all equal in the gate electrodes and the dummy gate electrodes….” (Ichiryu at 16:10-11).<br><br>“In FIG. 14, a reference symbol C81 denotes a standard cell. The standard cell C81 comprises gate electrodes G, dummy gate electrodes DG and two gate electrodes G2 having a gate length different to those of the gate electrode G and the dummy gate electrode DG, wherein a width of the gate electrode G2 is set so that a cell width of the standard cell C81 in the X direction is an integral multiple of the gate pitch Gx. In FIG. 14, the cell width of the standard cell C81 is nine times as wide as the gate pitch Gx. The width of the gate electrode G2 is thus set because a processing speed is expected to be faster when the cell width of each cell in the X direction is the integral multiple of the gate pitch Gx than when the cell width of each cell takes an arbitrary value in the placement using the conventional automatic placement & routing tool. However, the width of the gate electrode G2 is not necessarily set in the foregoing manner.” (Ichiryu at 16:15-30).<br><br>“As described, in the case of including the standard cell comprising the gate electrodes having the different gate lengths….” (Ichiryu at 16:32-34). |

| '012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | "[T]he embodiment 5 can be applied in the same manner to a cell structure where the dummy gate electrodes having the different gate lengths are provided and a cell structure where the gate electrodes and the dummy gate electrodes having the different gate intervals are provided. The description of the embodiment 5 is premised on the provision of the dummy gates DG…." (Ichiryu at 16:53-59).<br><br>"In the constitution, the distance from the cell boundary of each standard cell to the gate electrode in the closest vicinity and the distance from the cell boundary of another standard cell adjacent thereto to the gate electrode in the closest vicinity are constant." (Ichiryu at 16:65-17:2).<br><br>"For example, a distance from each of the cell boundary of the standard cells C61, C62 and C63 to the gate electrode in the X direction is 'Gx-gate length/2' and constant even in the constitution shown in FIG. 11 where the dummy gate electrodes DG are not provided. A distance between a transistor disposed at the end of each standard cell and the gate electrode G of the adjacent standard cell is '2Gx-gate length' and constant. For example, even in the case where the dummy gate electrode DG is not provided in the constitution described referring to FIG. 11, the distance from each of the cell boundary of the respective standard cells C61, C62 and C63 to the gate electrode G located at the end of each of the standard cells in the X direction is constant at (Gx-gate length/2). Further, the distance from the gate electrode G located at the end of each of the standard cells to the gate electrode G located at the end of each of adjacent standard cells in the X direction is constant at (2Gx-gate length)." (Ichiryu at 17:6-22).<br><br>"Further, in the embodiment 6, the standard cells described in the embodiments 1 and 5 are used. The gate lengths and the gate intervals are thereby equal in the patterns of the gate electrodes of the placed standard cells C91, C92 and C93, which leads to the improvement of the precision in the finished dimension of the gate electrodes. The improvement of the precision in the finished dimension of the gate electrodes can be realized not only inside each of the standard cells C91, C92 and C93 but also between the standard cells." (Ichiryu at 18:1-9). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “[W]hen the standard cells are adjacently located, the gate lengths and the gate intervals in the patterns of the gate electrodes and the dummy gate electrodes are the same as when they are located alone.” (Ichiryu at 18:10-13).<br><br>F I G. 11<br><br>  <br><br><br>(Ichiryu Fig. 11).<br><br>*See also* Ichiryu at Figs. 1, 2, 3, 8, 12, 13, 14. |

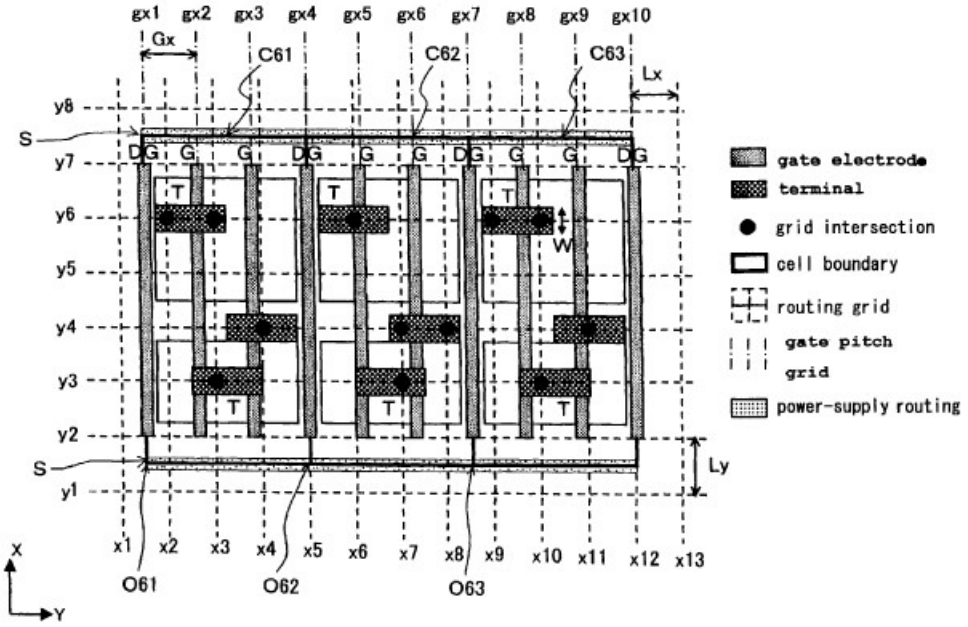
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | This limitation also would have been obvious to a person of ordinary skill in the art based on (1) Ichiryu alone; and/or (2) the teachings with respect to this claim element as detailed in the cover document of Respondent’s invalidity contentions and Respondent’s other invalidity charts. |
| 21. An integrated circuit device as recited in claim 20, wherein the plurality of linear conductive segments are positioned in the side-by-side manner according to a substantially equal centerline-to-centerline spacing as measured in a second direction perpendicular to the first direction. | At least under Tela’s apparent infringement theory, Ichiryu discloses and/or renders obvious an integrated circuit device as recited in claim 20, wherein the plurality of linear conductive segments are positioned in the side-by-side manner according to a substantially equal centerline-to-centerline spacing as measured in a second direction perpendicular to the first direction.<br><br>Ichiryu describes layout techniques for gate electrodes, including that they have equal centerline-to-centerline spacing. Ichiryu discloses that “ “[i]n the standard cells C61, C62 and C63, gate lengths and gate intervals of the gate electrode[s] G and dummy gate electrode[s] DG are constant ….” Ichiryu at 14:45-47. Gx is “gate pitch=gate length+gate interval” |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | Fig. 11 (excerpt)<br>  <br><br>*See, e.g.*: |

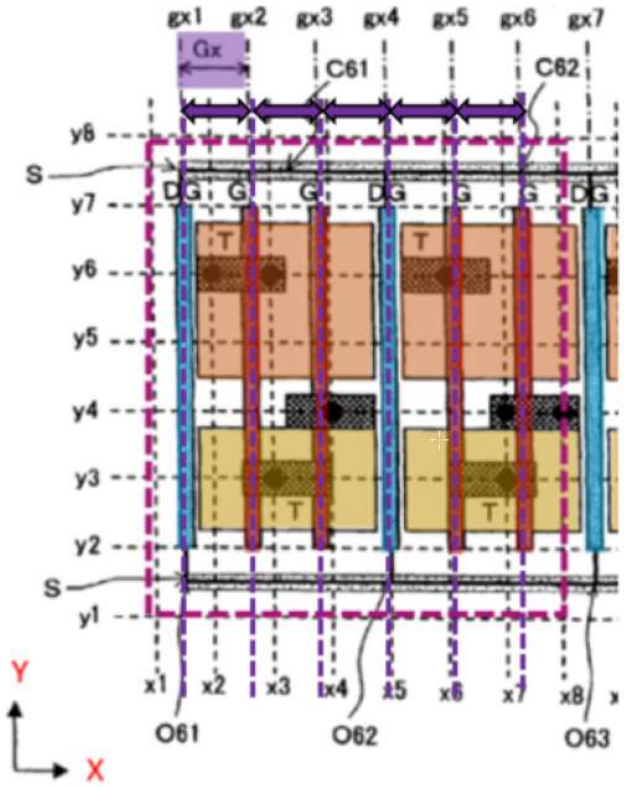
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “[A]s recited in No. H10-32253 of the Publication of the Unexamined Japanese Patent Applications, the interval and the length of the gate electrodes in each standard cell are set regular so that the OPC is processed per standard cell in the conventional technology.” (Ichiryu at 2:37-41).<br><br>“The standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes….” (Ichiryu at 6:20-21).<br><br>“A standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes, wherein gate pitches of some of the gate electrodes are set to values different to the routing grid interval set along the X direction in parallel with the power-supply wiring of the standard cell, and a cell width along the X direction in parallel with the power-supply wiring of the standard cell is set to an integral multiple of a minimum value of the gate pitches of the gate electrodes set to the values different to the routing grid interval set along the X direction.” (Ichiryu at 6:26-35).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, a precision in a finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:41-45).<br><br>“A standard cell according to the present invention comprises a plurality of gate electrodes and a plurality of dummy gate electrodes, wherein a cell width in the X direction in parallel with the power-supply wiring of the standard cell is an integral multiple of a minimum gate pitch of gate pitches of the gate electrodes and the dummy gate electrodes different to the routing grid interval along the X direction.” (Ichiryu at 6:46-52).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:58-62). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “The gate pitches of the standard cell are all preferably equal. Thereby, the pattern of the gate electrodes can impart a perfect regularity to the gate pitches, and the precision in the finished dimension of the gate electrodes can be further improved.” (Ichiryu at 6:66-7:3).<br><br>“Further, because the pattern of the gate electrodes can have the regularity, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be performed in each standard cell.” (Ichiryu at 8:21-24).<br><br>“Referring to reference symbols in FIG. 11, x1-x13 denote routing grids for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, y1-y8 denote routing grids disposed in parallel with the X direction and adjacent to one another in the Y direction, gx1-gx10 denote grids of gate pitches for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, C61, C62 and C63 are standard cells, O61, O62 and O63 are respective origins of the standard cells C61, C62 and C63, … G denotes a gate electrode, and DG denotes a dummy gate electrode.” (Ichiryu at 14:32-44).<br><br>“In the standard cells C61, C62 and C63, gate lengths and gate intervals of the gate electrode G and dummy gate electrode DG are constant, and a cell width of the standard cells C61, C62 and C63 in the X direction is an integral multiple of a minimum value of a gate pitch Gx (value of gate pitch=gate length+gate interval) (In FIG. 11, the cell width of the standard cells C61, C62 and C63 is three times as wide as Gx).” (Ichiryu at 14:45-51).<br><br>“Not only inside the respective standard cells C61, C62 and C63, but also among the standard cells C61, C62 and C63 to one another, the gate lengths and the gate intervals are equal in the patterns of the gate electrodes and the dummy gate electrodes.” (Ichiryu at 15:47-51).<br><br>“In the embodiment 5, the gate lengths are all equal in the gate electrodes and the dummy gate electrodes….” (Ichiryu at 16:10-11).<br><br>“In FIG. 14, a reference symbol C81 denotes a standard cell. The standard cell C81 comprises gate electrodes G, dummy gate electrodes DG and two gate electrodes G2 having a gate length different to |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | those of the gate electrode G and the dummy gate electrode DG, wherein a width of the gate electrode G2 is set so that a cell width of the standard cell C81 in the X direction is an integral multiple of the gate pitch Gx. In FIG. 14, the cell width of the standard cell C81 is nine times as wide as the gate pitch Gx. The width of the gate electrode G2 is thus set because a processing speed is expected to be faster when the cell width of each cell in the X direction is the integral multiple of the gate pitch Gx than when the cell width of each cell takes an arbitrary value in the placement using the conventional automatic placement & routing tool. However, the width of the gate electrode G2 is not necessarily set in the foregoing manner.” (Ichiryu at 16:15-30).<br><br>“In the constitution, the distance from the cell boundary of each standard cell to the gate electrode in the closest vicinity and the distance from the cell boundary of another standard cell adjacent thereto to the gate electrode in the closest vicinity are constant.” (Ichiryu at 16:65-17:2).<br><br>“For example, a distance from each of the cell boundary of the standard cells C61, C62 and C63 to the gate electrode in the X direction is ‘Gx-gate length/2’ and constant even in the constitution shown in FIG. 11 where the dummy gate electrodes DG are not provided. A distance between a transistor disposed at the end of each standard cell and the gate electrode G of the adjacent standard cell is ‘2Gx-gate length’ and constant. For example, even in the case where the dummy gate electrode DG is not provided in the constitution described referring to FIG. 11, the distance from each of the cell boundary of the respective standard cells C61, C62 and C63 to the gate electrode G located at the end of each of the standard cells in the X direction is constant at (Gx-gate length/2). Further, the distance from the gate electrode G located at the end of each of the standard cells to the gate electrode G located at the end of each of adjacent standard cells in the X direction is constant at (2Gx-gate length).” (Ichiryu at 17:6-22).<br><br>“Further, in the embodiment 6, the standard cells described in the embodiments 1 and 5 are used. The gate lengths and the gate intervals are thereby equal in the patterns of the gate electrodes of the placed standard cells C91, C92 and C93, which leads to the improvement of the precision in the finished dimension of the gate electrodes. The improvement of the precision in the finished |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | dimension of the gate electrodes can be realized not only inside each of the standard cells C91, C92 and C93 but also between the standard cells.” (Ichiryu at 18:1-9).<br><br>“[W]hen the standard cells are adjacently located, the gate lengths and the gate intervals in the patterns of the gate electrodes and the dummy gate electrodes are the same as when they are located alone.” (Ichiryu at 18:10-13).<br><br>F I G. 11<br><br>  <br><br><br>(Ichiryu Fig. 11). |

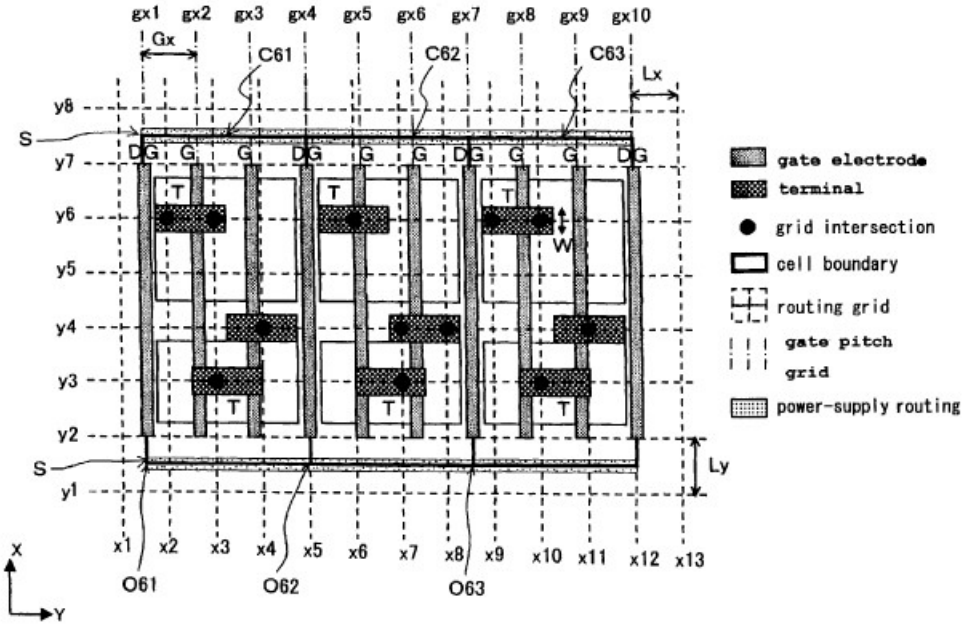
| '012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | *See also* Ichiryu at Figs. 1, 2, 3, 8, 12, 13, 14.<br><br>This limitation also would have been obvious to a person of ordinary skill in the art based on (1) Ichiryu alone; and/or (2) the teachings with respect to this claim element as detailed in the cover document of Respondent's invalidity contentions and Respondent's other invalidity charts. |
| 22. An integrated circuit device as recited in claim 21, wherein the substantially equal centerline-to-centerline spacing as measured in the second direction is less than 360 nanometers. | At least under Tela's apparent infringement theory, Ichiryu discloses and/or renders obvious an integrated circuit device as recited in claim 21, wherein the substantially equal centerline-to-centerline spacing as measured in the second direction is less than 360 nanometers.<br><br>Ichiryu describes layout techniques for gate electrodes, including that they have equal centerline-to-centerline spacing. Ichiryu discloses that " "[i]n the standard cells C61, C62 and C63, gate lengths and gate intervals of the gate electrode[s] G and dummy gate electrode[s] DG are constant …." Ichiryu at 14:45-47. Gx is "gate pitch=gate length+gate interval" |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | Fig. 11 (excerpt)<br>  <br><br>*See, e.g.*: |

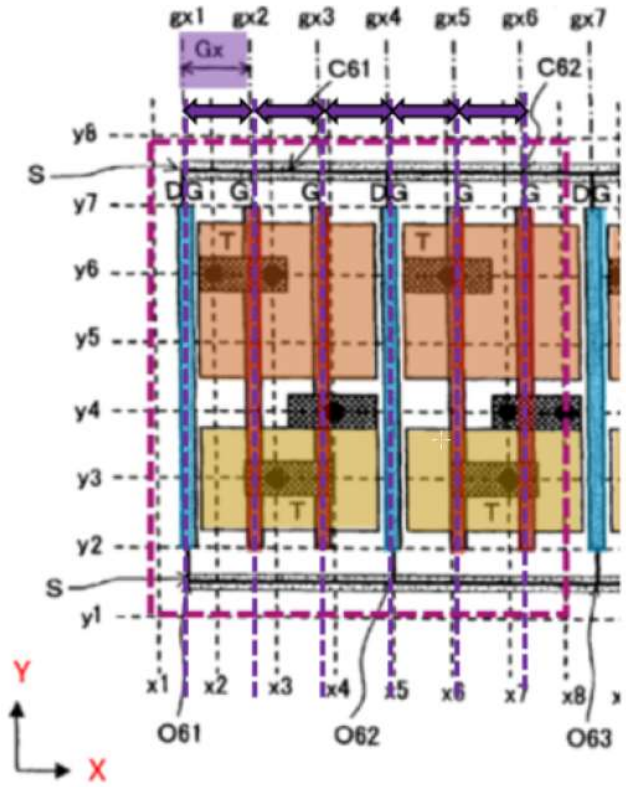
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “[A]s recited in No. H10-32253 of the Publication of the Unexamined Japanese Patent Applications, the interval and the length of the gate electrodes in each standard cell are set regular so that the OPC is processed per standard cell in the conventional technology.” (Ichiryu at 2:37-41).<br><br>“The standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes….” (Ichiryu at 6:20-21).<br><br>“A standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes, wherein gate pitches of some of the gate electrodes are set to values different to the routing grid interval set along the X direction in parallel with the power-supply wiring of the standard cell, and a cell width along the X direction in parallel with the power-supply wiring of the standard cell is set to an integral multiple of a minimum value of the gate pitches of the gate electrodes set to the values different to the routing grid interval set along the X direction.” (Ichiryu at 6:26-35).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, a precision in a finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:41-45).<br><br>“A standard cell according to the present invention comprises a plurality of gate electrodes and a plurality of dummy gate electrodes, wherein a cell width in the X direction in parallel with the power-supply wiring of the standard cell is an integral multiple of a minimum gate pitch of gate pitches of the gate electrodes and the dummy gate electrodes different to the routing grid interval along the X direction.” (Ichiryu at 6:46-52).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:58-62). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “The gate pitches of the standard cell are all preferably equal. Thereby, the pattern of the gate electrodes can impart a perfect regularity to the gate pitches, and the precision in the finished dimension of the gate electrodes can be further improved.” (Ichiryu at 6:66-7:3).<br><br>“Further, because the pattern of the gate electrodes can have the regularity, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be performed in each standard cell.” (Ichiryu at 8:21-24).<br><br>“Referring to reference symbols in FIG. 11, x1-x13 denote routing grids for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, y1-y8 denote routing grids disposed in parallel with the X direction and adjacent to one another in the Y direction, gx1-gx10 denote grids of gate pitches for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, C61, C62 and C63 are standard cells, O61, O62 and O63 are respective origins of the standard cells C61, C62 and C63, … G denotes a gate electrode, and DG denotes a dummy gate electrode.” (Ichiryu at 14:32-44).<br><br>“In the standard cells C61, C62 and C63, gate lengths and gate intervals of the gate electrode G and dummy gate electrode DG are constant, and a cell width of the standard cells C61, C62 and C63 in the X direction is an integral multiple of a minimum value of a gate pitch Gx (value of gate pitch=gate length+gate interval) (In FIG. 11, the cell width of the standard cells C61, C62 and C63 is three times as wide as Gx).” (Ichiryu at 14:45-51).<br><br>“Not only inside the respective standard cells C61, C62 and C63, but also among the standard cells C61, C62 and C63 to one another, the gate lengths and the gate intervals are equal in the patterns of the gate electrodes and the dummy gate electrodes.” (Ichiryu at 15:47-51).<br><br>“In the embodiment 5, the gate lengths are all equal in the gate electrodes and the dummy gate electrodes….” (Ichiryu at 16:10-11).<br><br>“In FIG. 14, a reference symbol C81 denotes a standard cell. The standard cell C81 comprises gate electrodes G, dummy gate electrodes DG and two gate electrodes G2 having a gate length different to |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | those of the gate electrode G and the dummy gate electrode DG, wherein a width of the gate electrode G2 is set so that a cell width of the standard cell C81 in the X direction is an integral multiple of the gate pitch Gx. In FIG. 14, the cell width of the standard cell C81 is nine times as wide as the gate pitch Gx. The width of the gate electrode G2 is thus set because a processing speed is expected to be faster when the cell width of each cell in the X direction is the integral multiple of the gate pitch Gx than when the cell width of each cell takes an arbitrary value in the placement using the conventional automatic placement & routing tool. However, the width of the gate electrode G2 is not necessarily set in the foregoing manner.” (Ichiryu at 16:15-30).<br><br>“In the constitution, the distance from the cell boundary of each standard cell to the gate electrode in the closest vicinity and the distance from the cell boundary of another standard cell adjacent thereto to the gate electrode in the closest vicinity are constant.” (Ichiryu at 16:65-17:2).<br><br>“For example, a distance from each of the cell boundary of the standard cells C61, C62 and C63 to the gate electrode in the X direction is ‘Gx-gate length/2’ and constant even in the constitution shown in FIG. 11 where the dummy gate electrodes DG are not provided. A distance between a transistor disposed at the end of each standard cell and the gate electrode G of the adjacent standard cell is ‘2Gx-gate length’ and constant. For example, even in the case where the dummy gate electrode DG is not provided in the constitution described referring to FIG. 11, the distance from each of the cell boundary of the respective standard cells C61, C62 and C63 to the gate electrode G located at the end of each of the standard cells in the X direction is constant at (Gx-gate length/2). Further, the distance from the gate electrode G located at the end of each of the standard cells to the gate electrode G located at the end of each of adjacent standard cells in the X direction is constant at (2Gx-gate length).” (Ichiryu at 17:6-22).<br><br>“Further, in the embodiment 6, the standard cells described in the embodiments 1 and 5 are used. The gate lengths and the gate intervals are thereby equal in the patterns of the gate electrodes of the placed standard cells C91, C92 and C93, which leads to the improvement of the precision in the finished dimension of the gate electrodes. The improvement of the precision in the finished |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | dimension of the gate electrodes can be realized not only inside each of the standard cells C91, C92 and C93 but also between the standard cells.” (Ichiryu at 18:1-9).<br><br>“[W]hen the standard cells are adjacently located, the gate lengths and the gate intervals in the patterns of the gate electrodes and the dummy gate electrodes are the same as when they are located alone.” (Ichiryu at 18:10-13).<br><br>F I G. 11<br>  <br><br><br>(Ichiryu Fig. 11). |

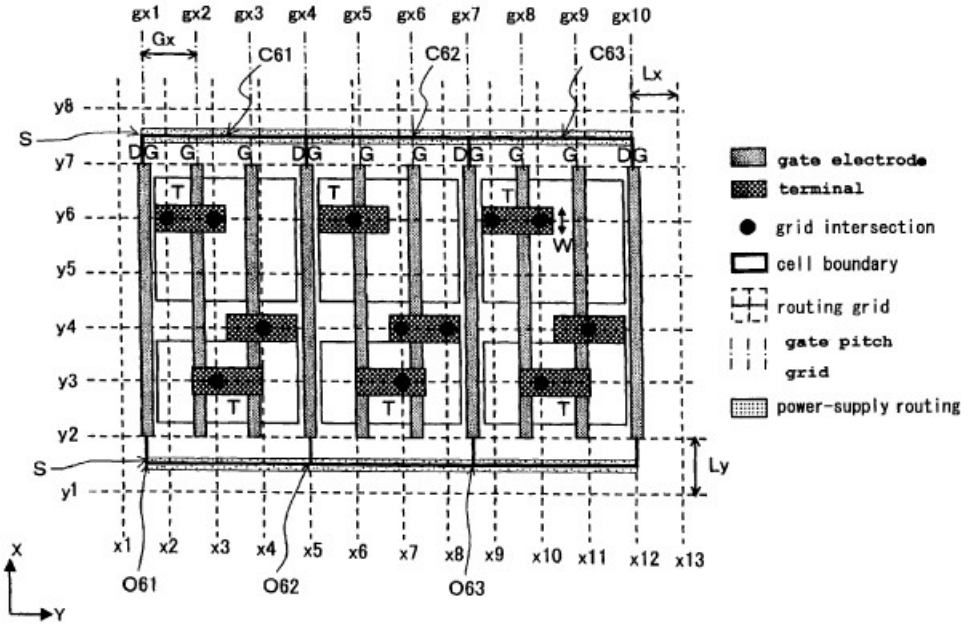
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | *See also* Ichiryu at Figs. 1, 2, 3, 8, 12, 13, 14.<br><br>This limitation also would have been obvious to a person of ordinary skill in the art based on (1) Ichiryu alone; and/or (2) the teachings with respect to this claim element as detailed in the cover document of Respondent’s invalidity contentions and Respondent’s other invalidity charts. |
| 23. An integrated circuit device as recited in claim 21, wherein a side-to-side spacing between each adjacently positioned pair of the plurality of linear conductive segments is less than 360 nanometers, wherein the side-to-side spacing is measured in the second direction. | At least under Tela’s apparent infringement theory, Ichiryu discloses and/or renders obvious an integrated circuit device as recited in claim 21, wherein a side-to-side spacing between each adjacently positioned pair of the plurality of linear conductive segments is less than 360 nanometers, wherein the side-to-side spacing is measured in the second direction.<br><br>Ichiryu describes and depicts multiple gate electrodes that form transistors of different types and are placed on a grid having the same pitch and width, and thus equal side-to-side spacing. Ichiryu discloses that “ “[i]n the standard cells C61, C62 and C63, gate lengths and gate intervals of the gate electrode[s] G and dummy gate electrode[s] DG are constant ….” Ichiryu at 14:45-47. Gx is “gate pitch=gate length+gate interval” Side-to-side spacing is less than gate pitch. |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | Fig. 11 (excerpt)<br>  <br><br>*See, e.g.*: |

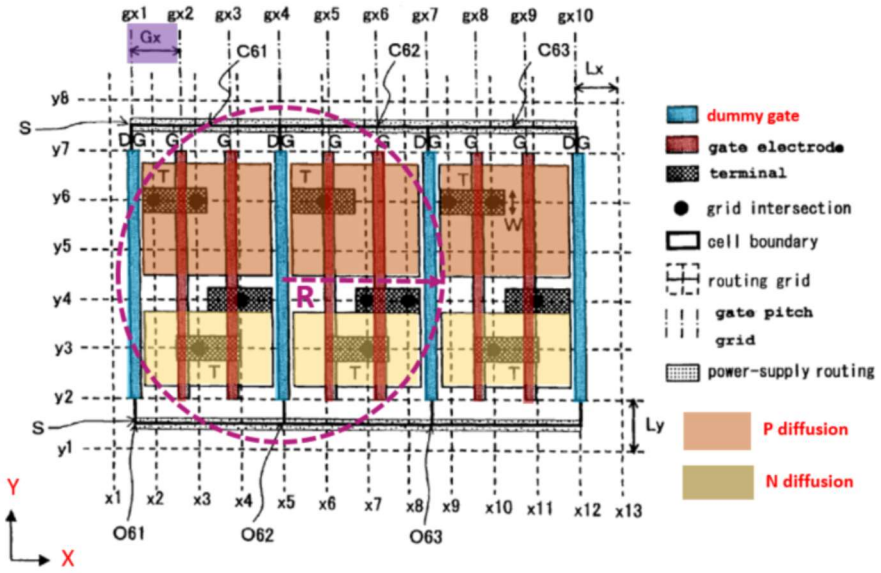
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “[A]s recited in No. H10-32253 of the Publication of the Unexamined Japanese Patent Applications, the interval and the length of the gate electrodes in each standard cell are set regular so that the OPC is processed per standard cell in the conventional technology.” (Ichiryu at 2:37-41).<br><br>“The standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes….” (Ichiryu at 6:20-21).<br><br>“A standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes, wherein gate pitches of some of the gate electrodes are set to values different to the routing grid interval set along the X direction in parallel with the power-supply wiring of the standard cell, and a cell width along the X direction in parallel with the power-supply wiring of the standard cell is set to an integral multiple of a minimum value of the gate pitches of the gate electrodes set to the values different to the routing grid interval set along the X direction.” (Ichiryu at 6:26-35).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, a precision in a finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:41-45).<br><br>“A standard cell according to the present invention comprises a plurality of gate electrodes and a plurality of dummy gate electrodes, wherein a cell width in the X direction in parallel with the power-supply wiring of the standard cell is an integral multiple of a minimum gate pitch of gate pitches of the gate electrodes and the dummy gate electrodes different to the routing grid interval along the X direction.” (Ichiryu at 6:46-52).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:58-62). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “The gate pitches of the standard cell are all preferably equal. Thereby, the pattern of the gate electrodes can impart a perfect regularity to the gate pitches, and the precision in the finished dimension of the gate electrodes can be further improved.” (Ichiryu at 6:66-7:3).<br><br>“Further, because the pattern of the gate electrodes can have the regularity, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be performed in each standard cell.” (Ichiryu at 8:21-24).<br><br>“Referring to reference symbols in FIG. 11, x1-x13 denote routing grids for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, y1-y8 denote routing grids disposed in parallel with the X direction and adjacent to one another in the Y direction, gx1-gx10 denote grids of gate pitches for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, C61, C62 and C63 are standard cells, O61, O62 and O63 are respective origins of the standard cells C61, C62 and C63, … G denotes a gate electrode, and DG denotes a dummy gate electrode.” (Ichiryu at 14:32-44).<br><br>“In the standard cells C61, C62 and C63, gate lengths and gate intervals of the gate electrode G and dummy gate electrode DG are constant, and a cell width of the standard cells C61, C62 and C63 in the X direction is an integral multiple of a minimum value of a gate pitch Gx (value of gate pitch=gate length+gate interval) (In FIG. 11, the cell width of the standard cells C61, C62 and C63 is three times as wide as Gx).” (Ichiryu at 14:45-51).<br><br>“Not only inside the respective standard cells C61, C62 and C63, but also among the standard cells C61, C62 and C63 to one another, the gate lengths and the gate intervals are equal in the patterns of the gate electrodes and the dummy gate electrodes.” (Ichiryu at 15:47-51).<br><br>“In the embodiment 5, the gate lengths are all equal in the gate electrodes and the dummy gate electrodes….” (Ichiryu at 16:10-11).<br><br>“In FIG. 14, a reference symbol C81 denotes a standard cell. The standard cell C81 comprises gate electrodes G, dummy gate electrodes DG and two gate electrodes G2 having a gate length different to |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | those of the gate electrode G and the dummy gate electrode DG, wherein a width of the gate electrode G2 is set so that a cell width of the standard cell C81 in the X direction is an integral multiple of the gate pitch Gx. In FIG. 14, the cell width of the standard cell C81 is nine times as wide as the gate pitch Gx. The width of the gate electrode G2 is thus set because a processing speed is expected to be faster when the cell width of each cell in the X direction is the integral multiple of the gate pitch Gx than when the cell width of each cell takes an arbitrary value in the placement using the conventional automatic placement & routing tool. However, the width of the gate electrode G2 is not necessarily set in the foregoing manner.” (Ichiryu at 16:15-30).<br><br>“In the constitution, the distance from the cell boundary of each standard cell to the gate electrode in the closest vicinity and the distance from the cell boundary of another standard cell adjacent thereto to the gate electrode in the closest vicinity are constant.” (Ichiryu at 16:65-17:2).<br><br>“For example, a distance from each of the cell boundary of the standard cells C61, C62 and C63 to the gate electrode in the X direction is ‘Gx-gate length/2’ and constant even in the constitution shown in FIG. 11 where the dummy gate electrodes DG are not provided. A distance between a transistor disposed at the end of each standard cell and the gate electrode G of the adjacent standard cell is ‘2Gx-gate length’ and constant. For example, even in the case where the dummy gate electrode DG is not provided in the constitution described referring to FIG. 11, the distance from each of the cell boundary of the respective standard cells C61, C62 and C63 to the gate electrode G located at the end of each of the standard cells in the X direction is constant at (Gx-gate length/2). Further, the distance from the gate electrode G located at the end of each of the standard cells to the gate electrode G located at the end of each of adjacent standard cells in the X direction is constant at (2Gx-gate length).” (Ichiryu at 17:6-22).<br><br>“Further, in the embodiment 6, the standard cells described in the embodiments 1 and 5 are used. The gate lengths and the gate intervals are thereby equal in the patterns of the gate electrodes of the placed standard cells C91, C92 and C93, which leads to the improvement of the precision in the finished dimension of the gate electrodes. The improvement of the precision in the finished |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | dimension of the gate electrodes can be realized not only inside each of the standard cells C91, C92 and C93 but also between the standard cells.” (Ichiryu at 18:1-9).<br><br>“[W]hen the standard cells are adjacently located, the gate lengths and the gate intervals in the patterns of the gate electrodes and the dummy gate electrodes are the same as when they are located alone.” (Ichiryu at 18:10-13).<br><br>F I G. 11<br>  <br><br><br>(Ichiryu Fig. 11). |

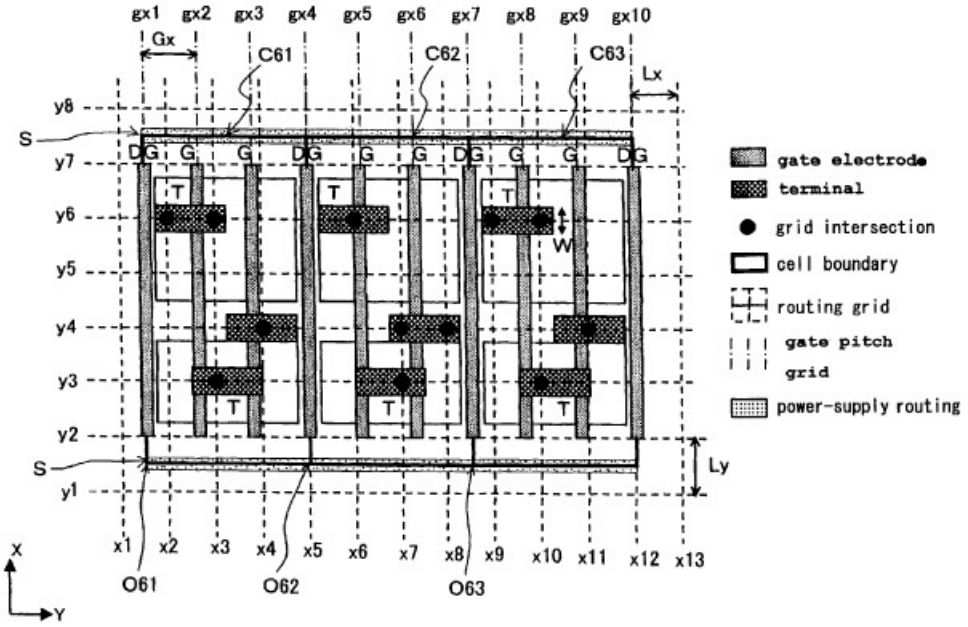
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | *See also* Ichiryu at Figs. 1, 2, 3, 8, 12, 13, 14.<br><br>This limitation also would have been obvious to a person of ordinary skill in the art based on (1) Ichiryu alone; and/or (2) the teachings with respect to this claim element as detailed in the cover document of Respondent’s invalidity contentions and Respondent’s other invalidity charts. |
| 24. An integrated circuit device as recited in claim 2, wherein each of the plurality of linear conductive segments respectively includes a first end and a second end, wherein the first ends of the plurality of linear conductive segments are substantially aligned to a first position relative to the first direction, and wherein the second ends of the plurality of linear conductive segments are substantially aligned to a second position relative to the first direction. | At least under Tela’s apparent infringement theory, Ichiryu discloses and/or renders obvious an integrated circuit device as recited in claim 2, wherein each of the plurality of linear conductive segments respectively includes a first end and a second end, wherein the first ends of the plurality of linear conductive segments are substantially aligned to a first position relative to the first direction, and wherein the second ends of the plurality of linear conductive segments are substantially aligned to a second position relative to the first direction.<br><br>Ichiryu describes layout techniques for gate electrodes, which are linear conductive segments, including placing them such that they extend in parallel and have aligned ends. The top end could be a first end and the bottom end could be a second end. |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | F I G. 11<br>  <br><br>*See, e.g.*:<br>“[A]s the miniaturization of the process [continues], a precision in a finished dimension of the gate electrode ultimately obtained is deteriorated by an optical proximity effect when an interval between the gate electrodes and gate lengths of the gate electrodes are irregular in their patterns. When the precision in the finished dimension of the gate electrode is deteriorated, performances of respective transistors of the semiconductor integrated circuit are increasingly inconstant, which leads to an increased variation in a performance of the semiconductor integrate[d] circuit.” (Ichiryu at 2:23-32). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “[A]s recited in No. H10-32253 of the Publication of the Unexamined Japanese Patent Applications, the interval and the length of the gate electrodes in each standard cell are set regular so that the OPC is processed per standard cell in the conventional technology.” (Ichiryu at 2:37-41).<br><br>“The standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes….” (Ichiryu at 6:20-21).<br><br>“A standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes, wherein gate pitches of some of the gate electrodes are set to values different to the routing grid interval set along the X direction in parallel with the power-supply wiring of the standard cell, and a cell width along the X direction in parallel with the power-supply wiring of the standard cell is set to an integral multiple of a minimum value of the gate pitches of the gate electrodes set to the values different to the routing grid interval set along the X direction.” (Ichiryu at 6:26-35).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, a precision in a finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:41-45).<br><br>“A standard cell according to the present invention comprises a plurality of gate electrodes and a plurality of dummy gate electrodes, wherein a cell width in the X direction in parallel with the power-supply wiring of the standard cell is an integral multiple of a minimum gate pitch of gate pitches of the gate electrodes and the dummy gate electrodes different to the routing grid interval along the X direction.” (Ichiryu at 6:46-52).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:58-62). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “The gate pitches of the standard cell are all preferably equal. Thereby, the pattern of the gate electrodes can impart a perfect regularity to the gate pitches, and the precision in the finished dimension of the gate electrodes can be further improved.” (Ichiryu at 6:66-7:3).<br><br>“Further, because the pattern of the gate electrodes can have the regularity, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be performed in each standard cell.” (Ichiryu at 8:21-24).<br><br>“Referring to reference symbols in FIG. 11, x1-x13 denote routing grids for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, y1-y8 denote routing grids disposed in parallel with the X direction and adjacent to one another in the Y direction, gx1-gx10 denote grids of gate pitches for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, C61, C62 and C63 are standard cells, O61, O62 and O63 are respective origins of the standard cells C61, C62 and C63, … G denotes a gate electrode, and DG denotes a dummy gate electrode.” (Ichiryu at 14:32-44).<br><br>“In the standard cells C61, C62 and C63, gate lengths and gate intervals of the gate electrode G and dummy gate electrode DG are constant, and a cell width of the standard cells C61, C62 and C63 in the X direction is an integral multiple of a minimum value of a gate pitch Gx (value of gate pitch=gate length+gate interval) (In FIG. 11, the cell width of the standard cells C61, C62 and C63 is three times as wide as Gx).” (Ichiryu at 14:45-51).<br><br>“Not only inside the respective standard cells C61, C62 and C63, but also among the standard cells C61, C62 and C63 to one another, the gate lengths and the gate intervals are equal in the patterns of the gate electrodes and the dummy gate electrodes.” (Ichiryu at 15:47-51).<br><br>“In the embodiment 5, the gate lengths are all equal in the gate electrodes and the dummy gate electrodes….” (Ichiryu at 16:10-11).<br><br>“In FIG. 14, a reference symbol C81 denotes a standard cell. The standard cell C81 comprises gate electrodes G, dummy gate electrodes DG and two gate electrodes G2 having a gate length different to |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | those of the gate electrode G and the dummy gate electrode DG, wherein a width of the gate electrode G2 is set so that a cell width of the standard cell C81 in the X direction is an integral multiple of the gate pitch Gx. In FIG. 14, the cell width of the standard cell C81 is nine times as wide as the gate pitch Gx. The width of the gate electrode G2 is thus set because a processing speed is expected to be faster when the cell width of each cell in the X direction is the integral multiple of the gate pitch Gx than when the cell width of each cell takes an arbitrary value in the placement using the conventional automatic placement & routing tool. However, the width of the gate electrode G2 is not necessarily set in the foregoing manner.” (Ichiryu at 16:15-30).<br><br>“As described, in the case of including the standard cell comprising the gate electrodes having the different gate lengths….” (Ichiryu at 16:32-34).<br><br>“In the constitution, the distance from the cell boundary of each standard cell to the gate electrode in the closest vicinity and the distance from the cell boundary of another standard cell adjacent thereto to the gate electrode in the closest vicinity are constant.” (Ichiryu at 16:65-17:2).<br><br>“For example, a distance from each of the cell boundary of the standard cells C61, C62 and C63 to the gate electrode in the X direction is ‘Gx-gate length/2’ and constant even in the constitution shown in FIG. 11 where the dummy gate electrodes DG are not provided. A distance between a transistor disposed at the end of each standard cell and the gate electrode G of the adjacent standard cell is ‘2Gx-gate length’ and constant. For example, even in the case where the dummy gate electrode DG is not provided in the constitution described referring to FIG. 11, the distance from each of the cell boundary of the respective standard cells C61, C62 and C63 to the gate electrode G located at the end of each of the standard cells in the X direction is constant at (Gx-gate length/2). Further, the distance from the gate electrode G located at the end of each of the standard cells to the gate electrode G located at the end of each of adjacent standard cells in the X direction is constant at (2Gx-gate length).” (Ichiryu at 17:6-22).<br><br>“Further, in the embodiment 6, the standard cells described in the embodiments 1 and 5 are used. The gate lengths and the gate intervals are thereby equal in the patterns of the gate electrodes of the placed standard cells C91, C92 and C93, which leads to the improvement of the precision in the |

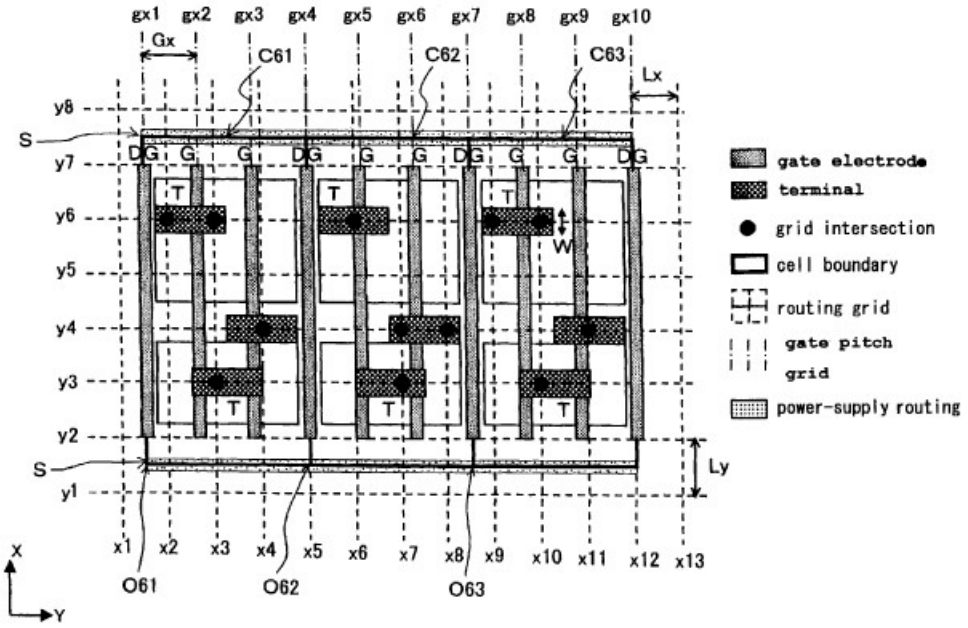
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | finished dimension of the gate electrodes. The improvement of the precision in the finished dimension of the gate electrodes can be realized not only inside each of the standard cells C91, C92 and C93 but also between the standard cells.” (Ichiryu at 18:1-9).<br><br>“[W]hen the standard cells are adjacently located, the gate lengths and the gate intervals in the patterns of the gate electrodes and the dummy gate electrodes are the same as when they are located alone.” (Ichiryu at 18:10-13).<br><br>F I G. 11<br>  <br> |

| '012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | (Ichiryu Fig. 11).<br><br>*See also* Ichiryu at Figs. 1, 2, 3, 8, 12, 13, 14.<br><br>This limitation also would have been obvious to a person of ordinary skill in the art based on (1) Ichiryu alone; and/or (2) the teachings with respect to this claim element as detailed in the cover document of Respondent's invalidity contentions and Respondent's other invalidity charts. |
| 25. An integrated circuit device as recited in claim 2, wherein each of the plurality of linear conductive segments is defined to have a substantially equal width as measured in a second direction perpendicular to the first direction. | At least under Tela's apparent infringement theory, Ichiryu discloses and/or renders obvious an integrated circuit device as recited in claim 2, wherein each of the plurality of linear conductive segments is defined to have a substantially equal width as measured in a second direction perpendicular to the first direction.<br><br>Ichiryu describes and depicts multiple linear conductive segments, e.g. structures in the polysilicon level, that have an equal width. Ichiryu discloses that " "[i]n the standard cells C61, C62 and C63, gate lengths and gate intervals of the gate electrode[s] G and dummy gate electrode[s] DG are constant …." Ichiryu at 14:45-47. What Ichiryu refers to as "gate length" is the claimed "width."<br><br>*See, e.g.*:<br><br>"[A]s the miniaturization of the process [continues], a precision in a finished dimension of the gate electrode ultimately obtained is deteriorated by an optical proximity effect when an interval between the gate electrodes and gate lengths of the gate electrodes are irregular in their patterns. When the precision in the finished dimension of the gate electrode is deteriorated, performances of respective transistors of the semiconductor integrated circuit are increasingly inconstant, which leads to an increased variation in a performance of the semiconductor integrate[d] circuit." (Ichiryu at 2:23-32).<br><br>"[A]s recited in No. H10-32253 of the Publication of the Unexamined Japanese Patent Applications, the interval and the length of the gate electrodes in each standard cell are set regular so that the OPC is processed per standard cell in the conventional technology." (Ichiryu at 2:37-41). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “The standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes….” (Ichiryu at 6:20-21).<br><br>“A standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes, wherein gate pitches of some of the gate electrodes are set to values different to the routing grid interval set along the X direction in parallel with the power-supply wiring of the standard cell, and a cell width along the X direction in parallel with the power-supply wiring of the standard cell is set to an integral multiple of a minimum value of the gate pitches of the gate electrodes set to the values different to the routing grid interval set along the X direction.” (Ichiryu at 6:26-35).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, a precision in a finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:41-45).<br><br>“A standard cell according to the present invention comprises a plurality of gate electrodes and a plurality of dummy gate electrodes, wherein a cell width in the X direction in parallel with the power-supply wiring of the standard cell is an integral multiple of a minimum gate pitch of gate pitches of the gate electrodes and the dummy gate electrodes different to the routing grid interval along the X direction.” (Ichiryu at 6:46-52).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:58-62).<br><br>“The gate pitches of the standard cell are all preferably equal. Thereby, the pattern of the gate electrodes can impart a perfect regularity to the gate pitches, and the precision in the finished dimension of the gate electrodes can be further improved.” (Ichiryu at 6:66-7:3). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “Further, because the pattern of the gate electrodes can have the regularity, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be performed in each standard cell.” (Ichiryu at 8:21-24).<br><br>“Referring to reference symbols in FIG. 11, x1-x13 denote routing grids for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, y1-y8 denote routing grids disposed in parallel with the X direction and adjacent to one another in the Y direction, gx1-gx10 denote grids of gate pitches for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, C61, C62 and C63 are standard cells, O61, O62 and O63 are respective origins of the standard cells C61, C62 and C63, … G denotes a gate electrode, and DG denotes a dummy gate electrode.” (Ichiryu at 14:32-44).<br><br>“In the standard cells C61, C62 and C63, gate lengths and gate intervals of the gate electrode G and dummy gate electrode DG are constant, and a cell width of the standard cells C61, C62 and C63 in the X direction is an integral multiple of a minimum value of a gate pitch Gx (value of gate pitch=gate length+gate interval) (In FIG. 11, the cell width of the standard cells C61, C62 and C63 is three times as wide as Gx).” (Ichiryu at 14:45-51).<br><br>“Not only inside the respective standard cells C61, C62 and C63, but also among the standard cells C61, C62 and C63 to one another, the gate lengths and the gate intervals are equal in the patterns of the gate electrodes and the dummy gate electrodes.” (Ichiryu at 15:47-51).<br><br>“In the embodiment 5, the gate lengths are all equal in the gate electrodes and the dummy gate electrodes….” (Ichiryu at 16:10-11).<br><br>“In FIG. 14, a reference symbol C81 denotes a standard cell. The standard cell C81 comprises gate electrodes G, dummy gate electrodes DG and two gate electrodes G2 having a gate length different to those of the gate electrode G and the dummy gate electrode DG, wherein a width of the gate electrode G2 is set so that a cell width of the standard cell C81 in the X direction is an integral multiple of the gate pitch Gx. In FIG. 14, the cell width of the standard cell C81 is nine times as wide as the gate pitch Gx. The width of the gate electrode G2 is thus set because a processing speed is |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | expected to be faster when the cell width of each cell in the X direction is the integral multiple of the gate pitch Gx than when the cell width of each cell takes an arbitrary value in the placement using the conventional automatic placement & routing tool. However, the width of the gate electrode G2 is not necessarily set in the foregoing manner.” (Ichiryu at 16:15-30).<br><br>“As described, in the case of including the standard cell comprising the gate electrodes having the different gate lengths….” (Ichiryu at 16:32-34).<br><br>“In the constitution, the distance from the cell boundary of each standard cell to the gate electrode in the closest vicinity and the distance from the cell boundary of another standard cell adjacent thereto to the gate electrode in the closest vicinity are constant.” (Ichiryu at 16:65-17:2).<br><br>“For example, a distance from each of the cell boundary of the standard cells C61, C62 and C63 to the gate electrode in the X direction is ‘Gx-gate length/2’ and constant even in the constitution shown in FIG. 11 where the dummy gate electrodes DG are not provided. A distance between a transistor disposed at the end of each standard cell and the gate electrode G of the adjacent standard cell is ‘2Gx-gate length’ and constant. For example, even in the case where the dummy gate electrode DG is not provided in the constitution described referring to FIG. 11, the distance from each of the cell boundary of the respective standard cells C61, C62 and C63 to the gate electrode G located at the end of each of the standard cells in the X direction is constant at (Gx-gate length/2). Further, the distance from the gate electrode G located at the end of each of the standard cells to the gate electrode G located at the end of each of adjacent standard cells in the X direction is constant at (2Gx-gate length).” (Ichiryu at 17:6-22).<br><br>“Further, in the embodiment 6, the standard cells described in the embodiments 1 and 5 are used. The gate lengths and the gate intervals are thereby equal in the patterns of the gate electrodes of the placed standard cells C91, C92 and C93, which leads to the improvement of the precision in the finished dimension of the gate electrodes. The improvement of the precision in the finished dimension of the gate electrodes can be realized not only inside each of the standard cells C91, C92 and C93 but also between the standard cells.” (Ichiryu at 18:1-9). |

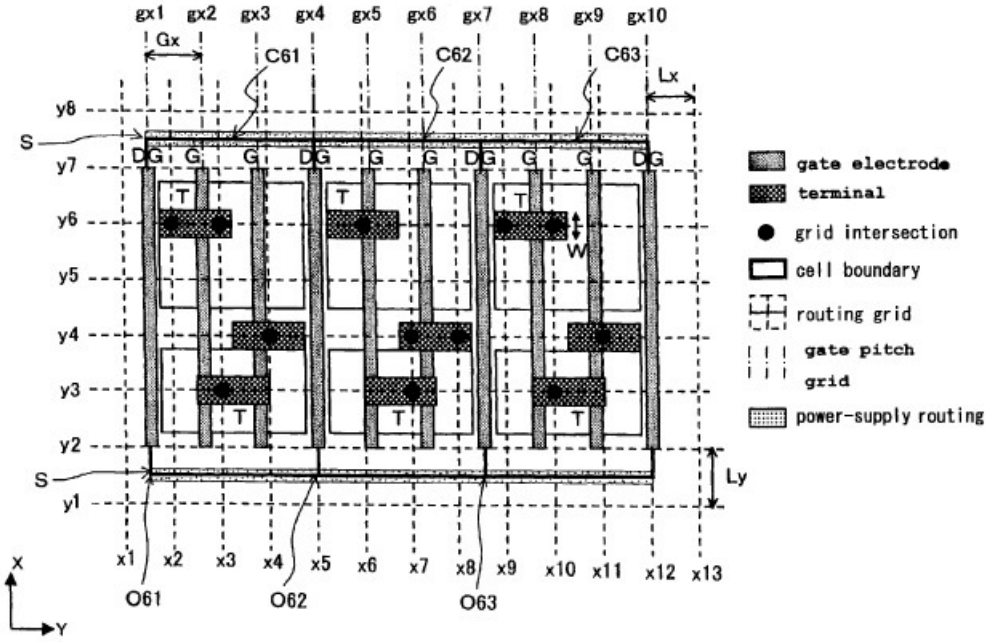
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “[W]hen the standard cells are adjacently located, the gate lengths and the gate intervals in the patterns of the gate electrodes and the dummy gate electrodes are the same as when they are located alone.” (Ichiryu at 18:10-13).<br><br>F I G. 11<br><br>  <br><br><br>(Ichiryu Fig. 11).<br><br>*See also* Ichiryu at Figs. 1, 2, 3, 8, 12, 13, 14. |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | This limitation also would have been obvious to a person of ordinary skill in the art based on (1) Ichiryu alone; and/or (2) the teachings with respect to this claim element as detailed in the cover document of Respondent’s invalidity contentions and Respondent’s other invalidity charts. |
| 31. An integrated circuit device as recited in claim 2, wherein the substrate region includes a number of diffusion regions, wherein the gate electrodes formed by the active linear conductive segments together with the diffusion regions form transistor devices. | At least under Tela’s apparent infringement theory, Ichiryu discloses and/or renders obvious an integrated circuit device as recited in claim 2, wherein the substrate region includes a number of diffusion regions, wherein the gate electrodes formed by the active linear conductive segments together with the diffusion regions form transistor devices.<br><br>Ichiryu depicts multiple rectangular diffusion regions. Ichiryu describes layout techniques for gate electrodes, which are linear conductive segments, including placing them such that they extend in parallel. Ichiryu describes layout techniques for gate electrodes in a gate electrode region.<br><br>*See, e.g.*:<br><br>“[A]s the miniaturization of the process [continues], a precision in a finished dimension of the gate electrode ultimately obtained is deteriorated by an optical proximity effect when an interval between the gate electrodes and gate lengths of the gate electrodes are irregular in their patterns. When the precision in the finished dimension of the gate electrode is deteriorated, performances of respective transistors of the semiconductor integrated circuit are increasingly inconstant, which leads to an increased variation in a performance of the semiconductor integrate[d] circuit.” (Ichiryu at 2:23-32).<br><br>“[A]s recited in No. H10-32253 of the Publication of the Unexamined Japanese Patent Applications, the interval and the length of the gate electrodes in each standard cell are set regular so that the OPC is processed per standard cell in the conventional technology.” (Ichiryu at 2:37-41).<br><br>“The standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes….” (Ichiryu at 6:20-21).<br><br>“A standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes, wherein gate pitches of some of the gate electrodes are set to values different to the |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | routing grid interval set along the X direction in parallel with the power-supply wiring of the standard cell, and a cell width along the X direction in parallel with the power-supply wiring of the standard cell is set to an integral multiple of a minimum value of the gate pitches of the gate electrodes set to the values different to the routing grid interval set along the X direction.” (Ichiryu at 6:26-35).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, a precision in a finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:41-45).<br><br>“A standard cell according to the present invention comprises a plurality of gate electrodes and a plurality of dummy gate electrodes, wherein a cell width in the X direction in parallel with the power-supply wiring of the standard cell is an integral multiple of a minimum gate pitch of gate pitches of the gate electrodes and the dummy gate electrodes different to the routing grid interval along the X direction.” (Ichiryu at 6:46-52).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:58-62).<br><br>“The gate pitches of the standard cell are all preferably equal. Thereby, the pattern of the gate electrodes can impart a perfect regularity to the gate pitches, and the precision in the finished dimension of the gate electrodes can be further improved.” (Ichiryu at 6:66-7:3).<br><br>“Further, because the pattern of the gate electrodes can have the regularity, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be performed in each standard cell.” (Ichiryu at 8:21-24).<br><br>“Referring to reference symbols in FIG. 11, x1-x13 denote routing grids for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, y1-y8 denote routing grids disposed in parallel with the X direction and adjacent to one another in the Y |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | direction, gx1-gx10 denote grids of gate pitches for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, C61, C62 and C63 are standard cells, O61, O62 and O63 are respective origins of the standard cells C61, C62 and C63, … G denotes a gate electrode, and DG denotes a dummy gate electrode.” (Ichiryu at 14:32-44).<br><br>“In the standard cells C61, C62 and C63, gate lengths and gate intervals of the gate electrode G and dummy gate electrode DG are constant, and a cell width of the standard cells C61, C62 and C63 in the X direction is an integral multiple of a minimum value of a gate pitch Gx (value of gate pitch=gate length+gate interval) (In FIG. 11, the cell width of the standard cells C61, C62 and C63 is three times as wide as Gx).” (Ichiryu at 14:45-51).<br><br>“Not only inside the respective standard cells C61, C62 and C63, but also among the standard cells C61, C62 and C63 to one another, the gate lengths and the gate intervals are equal in the patterns of the gate electrodes and the dummy gate electrodes.” (Ichiryu at 15:47-51).<br><br>“In the embodiment 5, the gate lengths are all equal in the gate electrodes and the dummy gate electrodes….” (Ichiryu at 16:10-11).<br><br>“In FIG. 14, a reference symbol C81 denotes a standard cell. The standard cell C81 comprises gate electrodes G, dummy gate electrodes DG and two gate electrodes G2 having a gate length different to those of the gate electrode G and the dummy gate electrode DG, wherein a width of the gate electrode G2 is set so that a cell width of the standard cell C81 in the X direction is an integral multiple of the gate pitch Gx. In FIG. 14, the cell width of the standard cell C81 is nine times as wide as the gate pitch Gx. The width of the gate electrode G2 is thus set because a processing speed is expected to be faster when the cell width of each cell in the X direction is the integral multiple of the gate pitch Gx than when the cell width of each cell takes an arbitrary value in the placement using the conventional automatic placement & routing tool. However, the width of the gate electrode G2 is not necessarily set in the foregoing manner.” (Ichiryu at 16:15-30). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “As described, in the case of including the standard cell comprising the gate electrodes having the different gate lengths….” (Ichiryu at 16:32-34).<br><br>“In the constitution, the distance from the cell boundary of each standard cell to the gate electrode in the closest vicinity and the distance from the cell boundary of another standard cell adjacent thereto to the gate electrode in the closest vicinity are constant.” (Ichiryu at 16:65-17:2).<br><br>“For example, a distance from each of the cell boundary of the standard cells C61, C62 and C63 to the gate electrode in the X direction is ‘Gx-gate length/2’ and constant even in the constitution shown in FIG. 11 where the dummy gate electrodes DG are not provided. A distance between a transistor disposed at the end of each standard cell and the gate electrode G of the adjacent standard cell is ‘2Gx-gate length’ and constant. For example, even in the case where the dummy gate electrode DG is not provided in the constitution described referring to FIG. 11, the distance from each of the cell boundary of the respective standard cells C61, C62 and C63 to the gate electrode G located at the end of each of the standard cells in the X direction is constant at (Gx-gate length/2). Further, the distance from the gate electrode G located at the end of each of the standard cells to the gate electrode G located at the end of each of adjacent standard cells in the X direction is constant at (2Gx-gate length).” (Ichiryu at 17:6-22).<br><br>“Further, in the embodiment 6, the standard cells described in the embodiments 1 and 5 are used. The gate lengths and the gate intervals are thereby equal in the patterns of the gate electrodes of the placed standard cells C91, C92 and C93, which leads to the improvement of the precision in the finished dimension of the gate electrodes. The improvement of the precision in the finished dimension of the gate electrodes can be realized not only inside each of the standard cells C91, C92 and C93 but also between the standard cells.” (Ichiryu at 18:1-9).<br><br>“[W]hen the standard cells are adjacently located, the gate lengths and the gate intervals in the patterns of the gate electrodes and the dummy gate electrodes are the same as when they are located alone.” (Ichiryu at 18:10-13). |

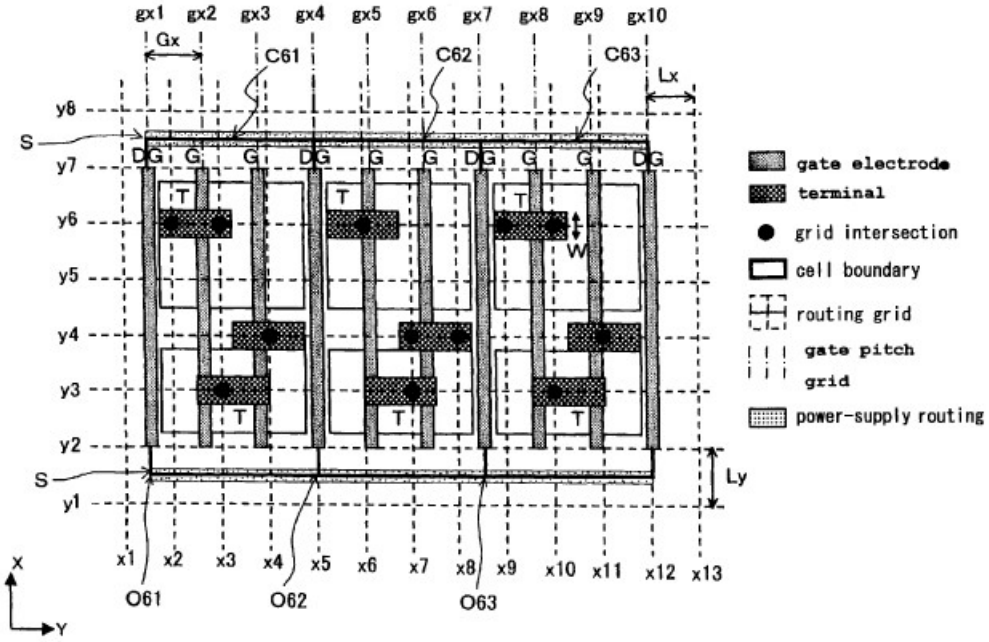
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | F I G. 11<br>  <br><br>(Ichiryu Fig. 11).<br>*See also* Ichiryu Figs. 1, 3, 8, 13, 14, 17, 18.<br>This limitation also would have been obvious to a person of ordinary skill in the art based on (1) Ichiryu alone; and/or (2) the teachings with respect to this claim element as detailed in the cover document of Respondent’s invalidity contentions and Respondent’s other invalidity charts. |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| 32. An integrated circuit device as recited in claim 31, wherein the number of diffusion regions include a diffusion region formed adjacent to each of a first active linear conductive segment and a second active linear conductive segment, | At least under Tela’s apparent infringement theory, Ichiryu discloses and/or renders obvious an integrated circuit device as recited in claim 31, wherein the number of diffusion regions include a diffusion region formed adjacent to each of a first active linear conductive segment and a second active linear conductive segment.<br><br>Ichiryu depicts multiple rectangular diffusion regions. Ichiryu describes layout techniques for gate electrodes, which are linear conductive segments, including placing them such that they extend in parallel.<br><br>*See, e.g.,:*<br><br>“[A]s the miniaturization of the process [continues], a precision in a finished dimension of the gate electrode ultimately obtained is deteriorated by an optical proximity effect when an interval between the gate electrodes and gate lengths of the gate electrodes are irregular in their patterns. When the precision in the finished dimension of the gate electrode is deteriorated, performances of respective transistors of the semiconductor integrated circuit are increasingly inconstant, which leads to an increased variation in a performance of the semiconductor integrate[d] circuit.” (Ichiryu at 2:23-32).<br><br>“[A]s recited in No. H10-32253 of the Publication of the Unexamined Japanese Patent Applications, the interval and the length of the gate electrodes in each standard cell are set regular so that the OPC is processed per standard cell in the conventional technology.” (Ichiryu at 2:37-41).<br><br>“The standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes….” (Ichiryu at 6:20-21).<br><br>“A standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes, wherein gate pitches of some of the gate electrodes are set to values different to the routing grid interval set along the X direction in parallel with the power-supply wiring of the standard cell, and a cell width along the X direction in parallel with the power-supply wiring of the standard cell is set to an integral multiple of a minimum value of the gate pitches of the gate |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | electrodes set to the values different to the routing grid interval set along the X direction.” (Ichiryu at 6:26-35).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, a precision in a finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:41-45).<br><br>“A standard cell according to the present invention comprises a plurality of gate electrodes and a plurality of dummy gate electrodes, wherein a cell width in the X direction in parallel with the power-supply wiring of the standard cell is an integral multiple of a minimum gate pitch of gate pitches of the gate electrodes and the dummy gate electrodes different to the routing grid interval along the X direction.” (Ichiryu at 6:46-52).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:58-62).<br><br>“The gate pitches of the standard cell are all preferably equal. Thereby, the pattern of the gate electrodes can impart a perfect regularity to the gate pitches, and the precision in the finished dimension of the gate electrodes can be further improved.” (Ichiryu at 6:66-7:3).<br><br>“Further, because the pattern of the gate electrodes can have the regularity, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be performed in each standard cell.” (Ichiryu at 8:21-24).<br><br>“Referring to reference symbols in FIG. 11, x1-x13 denote routing grids for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, y1-y8 denote routing grids disposed in parallel with the X direction and adjacent to one another in the Y direction, gx1-gx10 denote grids of gate pitches for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, C61, C62 and C63 are |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | standard cells, O61, O62 and O63 are respective origins of the standard cells C61, C62 and C63, … G denotes a gate electrode, and DG denotes a dummy gate electrode.” (Ichiryu at 14:32-44).<br><br>“In the standard cells C61, C62 and C63, gate lengths and gate intervals of the gate electrode G and dummy gate electrode DG are constant, and a cell width of the standard cells C61, C62 and C63 in the X direction is an integral multiple of a minimum value of a gate pitch Gx (value of gate pitch=gate length+gate interval) (In FIG. 11, the cell width of the standard cells C61, C62 and C63 is three times as wide as Gx).” (Ichiryu at 14:45-51).<br><br>“Not only inside the respective standard cells C61, C62 and C63, but also among the standard cells C61, C62 and C63 to one another, the gate lengths and the gate intervals are equal in the patterns of the gate electrodes and the dummy gate electrodes.” (Ichiryu at 15:47-51).<br><br>“In the embodiment 5, the gate lengths are all equal in the gate electrodes and the dummy gate electrodes….” (Ichiryu at 16:10-11).<br><br>“In FIG. 14, a reference symbol C81 denotes a standard cell. The standard cell C81 comprises gate electrodes G, dummy gate electrodes DG and two gate electrodes G2 having a gate length different to those of the gate electrode G and the dummy gate electrode DG, wherein a width of the gate electrode G2 is set so that a cell width of the standard cell C81 in the X direction is an integral multiple of the gate pitch Gx. In FIG. 14, the cell width of the standard cell C81 is nine times as wide as the gate pitch Gx. The width of the gate electrode G2 is thus set because a processing speed is expected to be faster when the cell width of each cell in the X direction is the integral multiple of the gate pitch Gx than when the cell width of each cell takes an arbitrary value in the placement using the conventional automatic placement & routing tool. However, the width of the gate electrode G2 is not necessarily set in the foregoing manner.” (Ichiryu at 16:15-30).<br><br>“As described, in the case of including the standard cell comprising the gate electrodes having the different gate lengths….” (Ichiryu at 16:32-34). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “In the constitution, the distance from the cell boundary of each standard cell to the gate electrode in the closest vicinity and the distance from the cell boundary of another standard cell adjacent thereto to the gate electrode in the closest vicinity are constant.” (Ichiryu at 16:65-17:2).<br><br>“For example, a distance from each of the cell boundary of the standard cells C61, C62 and C63 to the gate electrode in the X direction is ‘Gx-gate length/2’ and constant even in the constitution shown in FIG. 11 where the dummy gate electrodes DG are not provided. A distance between a transistor disposed at the end of each standard cell and the gate electrode G of the adjacent standard cell is ‘2Gx-gate length’ and constant. For example, even in the case where the dummy gate electrode DG is not provided in the constitution described referring to FIG. 11, the distance from each of the cell boundary of the respective standard cells C61, C62 and C63 to the gate electrode G located at the end of each of the standard cells in the X direction is constant at (Gx-gate length/2). Further, the distance from the gate electrode G located at the end of each of the standard cells to the gate electrode G located at the end of each of adjacent standard cells in the X direction is constant at (2Gx-gate length).” (Ichiryu at 17:6-22).<br><br>“Further, in the embodiment 6, the standard cells described in the embodiments 1 and 5 are used. The gate lengths and the gate intervals are thereby equal in the patterns of the gate electrodes of the placed standard cells C91, C92 and C93, which leads to the improvement of the precision in the finished dimension of the gate electrodes. The improvement of the precision in the finished dimension of the gate electrodes can be realized not only inside each of the standard cells C91, C92 and C93 but also between the standard cells.” (Ichiryu at 18:1-9).<br><br>“[W]hen the standard cells are adjacently located, the gate lengths and the gate intervals in the patterns of the gate electrodes and the dummy gate electrodes are the same as when they are located alone.” (Ichiryu at 18:10-13). |

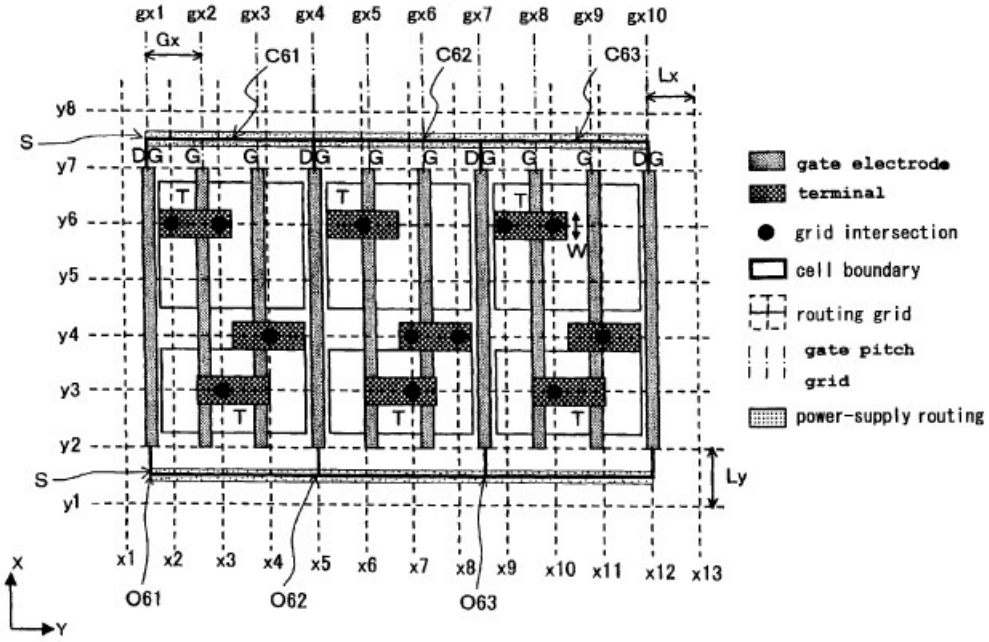
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | F I G. 11<br>  <br><br>(Ichiryu Fig. 11).<br>*See also* Ichiryu Figs. 1, 3, 8, 13, 14, 17, 18.<br>This limitation also would have been obvious to a person of ordinary skill in the art based on (1) Ichiryu alone; and/or (2) the teachings with respect to this claim element as detailed in the cover document of Respondent’s invalidity contentions and Respondent’s other invalidity charts. |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| [32.1] wherein the first active linear conductive segment includes at least one transistor gate electrode portion, and | At least under Tela’s apparent infringement theory, Ichiryu discloses and/or renders obvious wherein the first active linear conductive segment includes at least one transistor gate electrode portion.<br><br>Ichiryu describes layout techniques for gate electrodes, which are linear conductive segments, including placing them such that they extend in parallel. Ichiryu describes layout techniques for gate electrodes in a gate electrode region.<br><br>*See, e.g.*:<br><br>“[A]s the miniaturization of the process [continues], a precision in a finished dimension of the gate electrode ultimately obtained is deteriorated by an optical proximity effect when an interval between the gate electrodes and gate lengths of the gate electrodes are irregular in their patterns. When the precision in the finished dimension of the gate electrode is deteriorated, performances of respective transistors of the semiconductor integrated circuit are increasingly inconstant, which leads to an increased variation in a performance of the semiconductor integrate[d] circuit.” (Ichiryu at 2:23-32).<br><br>“[A]s recited in No. H10-32253 of the Publication of the Unexamined Japanese Patent Applications, the interval and the length of the gate electrodes in each standard cell are set regular so that the OPC is processed per standard cell in the conventional technology.” (Ichiryu at 2:37-41).<br><br>“The standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes….” (Ichiryu at 6:20-21).<br><br>“A standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes, wherein gate pitches of some of the gate electrodes are set to values different to the routing grid interval set along the X direction in parallel with the power-supply wiring of the standard cell, and a cell width along the X direction in parallel with the power-supply wiring of the standard cell is set to an integral multiple of a minimum value of the gate pitches of the gate electrodes set to the values different to the routing grid interval set along the X direction.” (Ichiryu at 6:26-35). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, a precision in a finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:41-45).<br><br>“A standard cell according to the present invention comprises a plurality of gate electrodes and a plurality of dummy gate electrodes, wherein a cell width in the X direction in parallel with the power-supply wiring of the standard cell is an integral multiple of a minimum gate pitch of gate pitches of the gate electrodes and the dummy gate electrodes different to the routing grid interval along the X direction.” (Ichiryu at 6:46-52).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:58-62).<br><br>“The gate pitches of the standard cell are all preferably equal. Thereby, the pattern of the gate electrodes can impart a perfect regularity to the gate pitches, and the precision in the finished dimension of the gate electrodes can be further improved.” (Ichiryu at 6:66-7:3).<br><br>“Further, because the pattern of the gate electrodes can have the regularity, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be performed in each standard cell.” (Ichiryu at 8:21-24).<br><br>“Referring to reference symbols in FIG. 11, x1-x13 denote routing grids for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, y1-y8 denote routing grids disposed in parallel with the X direction and adjacent to one another in the Y direction, gx1-gx10 denote grids of gate pitches for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, C61, C62 and C63 are standard cells, O61, O62 and O63 are respective origins of the standard cells C61, C62 and C63, … G denotes a gate electrode, and DG denotes a dummy gate electrode.” (Ichiryu at 14:32-44). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “In the standard cells C61, C62 and C63, gate lengths and gate intervals of the gate electrode G and dummy gate electrode DG are constant, and a cell width of the standard cells C61, C62 and C63 in the X direction is an integral multiple of a minimum value of a gate pitch Gx (value of gate pitch=gate length+gate interval) (In FIG. 11, the cell width of the standard cells C61, C62 and C63 is three times as wide as Gx).” (Ichiryu at 14:45-51).<br><br>“Not only inside the respective standard cells C61, C62 and C63, but also among the standard cells C61, C62 and C63 to one another, the gate lengths and the gate intervals are equal in the patterns of the gate electrodes and the dummy gate electrodes.” (Ichiryu at 15:47-51).<br><br>“In the embodiment 5, the gate lengths are all equal in the gate electrodes and the dummy gate electrodes….” (Ichiryu at 16:10-11).<br><br>“In FIG. 14, a reference symbol C81 denotes a standard cell. The standard cell C81 comprises gate electrodes G, dummy gate electrodes DG and two gate electrodes G2 having a gate length different to those of the gate electrode G and the dummy gate electrode DG, wherein a width of the gate electrode G2 is set so that a cell width of the standard cell C81 in the X direction is an integral multiple of the gate pitch Gx. In FIG. 14, the cell width of the standard cell C81 is nine times as wide as the gate pitch Gx. The width of the gate electrode G2 is thus set because a processing speed is expected to be faster when the cell width of each cell in the X direction is the integral multiple of the gate pitch Gx than when the cell width of each cell takes an arbitrary value in the placement using the conventional automatic placement & routing tool. However, the width of the gate electrode G2 is not necessarily set in the foregoing manner.” (Ichiryu at 16:15-30).<br><br>“As described, in the case of including the standard cell comprising the gate electrodes having the different gate lengths….” (Ichiryu at 16:32-34).<br><br>“In the constitution, the distance from the cell boundary of each standard cell to the gate electrode in the closest vicinity and the distance from the cell boundary of another standard cell adjacent thereto to the gate electrode in the closest vicinity are constant.” (Ichiryu at 16:65-17:2). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “For example, a distance from each of the cell boundary of the standard cells C61, C62 and C63 to the gate electrode in the X direction is ‘Gx-gate length/2’ and constant even in the constitution shown in FIG. 11 where the dummy gate electrodes DG are not provided. A distance between a transistor disposed at the end of each standard cell and the gate electrode G of the adjacent standard cell is ‘2Gx-gate length’ and constant. For example, even in the case where the dummy gate electrode DG is not provided in the constitution described referring to FIG. 11, the distance from each of the cell boundary of the respective standard cells C61, C62 and C63 to the gate electrode G located at the end of each of the standard cells in the X direction is constant at (Gx-gate length/2). Further, the distance from the gate electrode G located at the end of each of the standard cells to the gate electrode G located at the end of each of adjacent standard cells in the X direction is constant at (2Gx-gate length).” (Ichiryu at 17:6-22).<br><br>“Further, in the embodiment 6, the standard cells described in the embodiments 1 and 5 are used. The gate lengths and the gate intervals are thereby equal in the patterns of the gate electrodes of the placed standard cells C91, C92 and C93, which leads to the improvement of the precision in the finished dimension of the gate electrodes. The improvement of the precision in the finished dimension of the gate electrodes can be realized not only inside each of the standard cells C91, C92 and C93 but also between the standard cells.” (Ichiryu at 18:1-9).<br><br>“[W]hen the standard cells are adjacently located, the gate lengths and the gate intervals in the patterns of the gate electrodes and the dummy gate electrodes are the same as when they are located alone.” (Ichiryu at 18:10-13). |

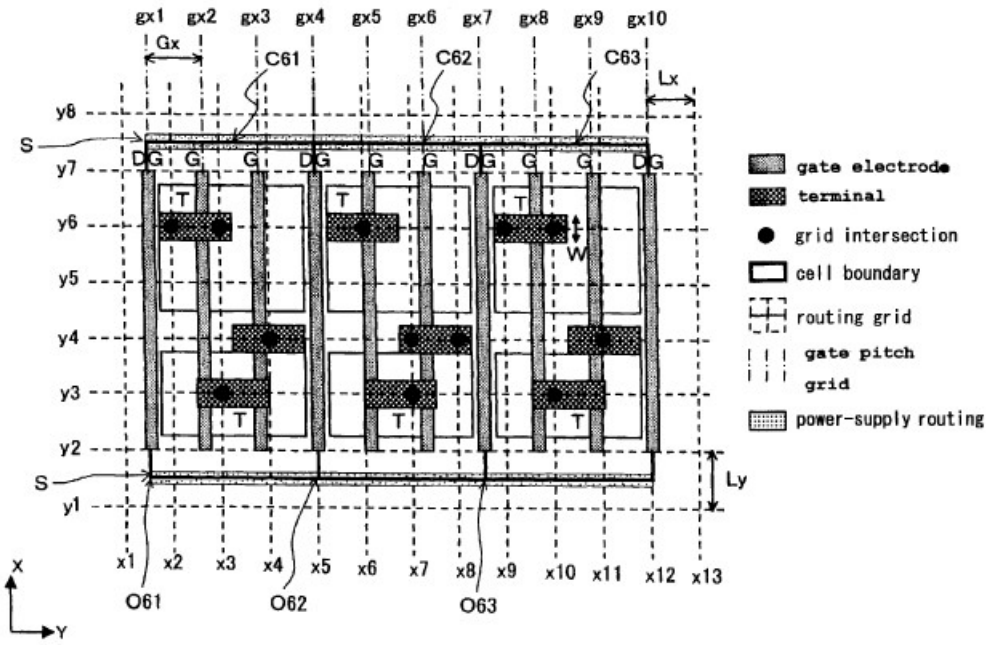
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | F I G. 11<br>  <br><br>(Ichiryu Fig. 11).<br>*See also* Ichiryu Figs. 1, 3, 8, 13, 14, 17, 18.<br>This limitation also would have been obvious to a person of ordinary skill in the art based on (1) Ichiryu alone; and/or (2) the teachings with respect to this claim element as detailed in the cover document of Respondent’s invalidity contentions and Respondent’s other invalidity charts. |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| [32.2] wherein the second active linear conductive segment includes at least one transistor gate electrode portion. | At least under Tela’s apparent infringement theory, Ichiryu discloses and/or renders obvious wherein the second active linear conductive segment includes at least one transistor gate electrode portion.<br><br>Ichiryu describes layout techniques for gate electrodes in a gate electrode region. Ichiryu describes layout techniques for gate electrodes, which are linear conductive segments, including placing them such that they extend in parallel.<br><br>*See, e.g.*:<br><br>“[A]s the miniaturization of the process [continues], a precision in a finished dimension of the gate electrode ultimately obtained is deteriorated by an optical proximity effect when an interval between the gate electrodes and gate lengths of the gate electrodes are irregular in their patterns. When the precision in the finished dimension of the gate electrode is deteriorated, performances of respective transistors of the semiconductor integrated circuit are increasingly inconstant, which leads to an increased variation in a performance of the semiconductor integrate[d] circuit.” (Ichiryu at 2:23-32).<br><br>“[A]s recited in No. H10-32253 of the Publication of the Unexamined Japanese Patent Applications, the interval and the length of the gate electrodes in each standard cell are set regular so that the OPC is processed per standard cell in the conventional technology.” (Ichiryu at 2:37-41).<br><br>“The standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes….” (Ichiryu at 6:20-21).<br><br>“A standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes, wherein gate pitches of some of the gate electrodes are set to values different to the routing grid interval set along the X direction in parallel with the power-supply wiring of the standard cell, and a cell width along the X direction in parallel with the power-supply wiring of the standard cell is set to an integral multiple of a minimum value of the gate pitches of the gate electrodes set to the values different to the routing grid interval set along the X direction.” (Ichiryu at 6:26-35). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, a precision in a finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:41-45).<br><br>“A standard cell according to the present invention comprises a plurality of gate electrodes and a plurality of dummy gate electrodes, wherein a cell width in the X direction in parallel with the power-supply wiring of the standard cell is an integral multiple of a minimum gate pitch of gate pitches of the gate electrodes and the dummy gate electrodes different to the routing grid interval along the X direction.” (Ichiryu at 6:46-52).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:58-62).<br><br>“The gate pitches of the standard cell are all preferably equal. Thereby, the pattern of the gate electrodes can impart a perfect regularity to the gate pitches, and the precision in the finished dimension of the gate electrodes can be further improved.” (Ichiryu at 6:66-7:3).<br><br>“Further, because the pattern of the gate electrodes can have the regularity, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be performed in each standard cell.” (Ichiryu at 8:21-24).<br><br>“Referring to reference symbols in FIG. 11, x1-x13 denote routing grids for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, y1-y8 denote routing grids disposed in parallel with the X direction and adjacent to one another in the Y direction, gx1-gx10 denote grids of gate pitches for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, C61, C62 and C63 are standard cells, O61, O62 and O63 are respective origins of the standard cells C61, C62 and C63, … G denotes a gate electrode, and DG denotes a dummy gate electrode.” (Ichiryu at 14:32-44). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “In the standard cells C61, C62 and C63, gate lengths and gate intervals of the gate electrode G and dummy gate electrode DG are constant, and a cell width of the standard cells C61, C62 and C63 in the X direction is an integral multiple of a minimum value of a gate pitch Gx (value of gate pitch=gate length+gate interval) (In FIG. 11, the cell width of the standard cells C61, C62 and C63 is three times as wide as Gx).” (Ichiryu at 14:45-51).<br><br>“Not only inside the respective standard cells C61, C62 and C63, but also among the standard cells C61, C62 and C63 to one another, the gate lengths and the gate intervals are equal in the patterns of the gate electrodes and the dummy gate electrodes.” (Ichiryu at 15:47-51).<br><br>“In the embodiment 5, the gate lengths are all equal in the gate electrodes and the dummy gate electrodes….” (Ichiryu at 16:10-11).<br><br>“In FIG. 14, a reference symbol C81 denotes a standard cell. The standard cell C81 comprises gate electrodes G, dummy gate electrodes DG and two gate electrodes G2 having a gate length different to those of the gate electrode G and the dummy gate electrode DG, wherein a width of the gate electrode G2 is set so that a cell width of the standard cell C81 in the X direction is an integral multiple of the gate pitch Gx. In FIG. 14, the cell width of the standard cell C81 is nine times as wide as the gate pitch Gx. The width of the gate electrode G2 is thus set because a processing speed is expected to be faster when the cell width of each cell in the X direction is the integral multiple of the gate pitch Gx than when the cell width of each cell takes an arbitrary value in the placement using the conventional automatic placement & routing tool. However, the width of the gate electrode G2 is not necessarily set in the foregoing manner.” (Ichiryu at 16:15-30).<br><br>“As described, in the case of including the standard cell comprising the gate electrodes having the different gate lengths….” (Ichiryu at 16:32-34).<br><br>“In the constitution, the distance from the cell boundary of each standard cell to the gate electrode in the closest vicinity and the distance from the cell boundary of another standard cell adjacent thereto to the gate electrode in the closest vicinity are constant.” (Ichiryu at 16:65-17:2). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “For example, a distance from each of the cell boundary of the standard cells C61, C62 and C63 to the gate electrode in the X direction is ‘Gx-gate length/2’ and constant even in the constitution shown in FIG. 11 where the dummy gate electrodes DG are not provided. A distance between a transistor disposed at the end of each standard cell and the gate electrode G of the adjacent standard cell is ‘2Gx-gate length’ and constant. For example, even in the case where the dummy gate electrode DG is not provided in the constitution described referring to FIG. 11, the distance from each of the cell boundary of the respective standard cells C61, C62 and C63 to the gate electrode G located at the end of each of the standard cells in the X direction is constant at (Gx-gate length/2). Further, the distance from the gate electrode G located at the end of each of the standard cells to the gate electrode G located at the end of each of adjacent standard cells in the X direction is constant at (2Gx-gate length).” (Ichiryu at 17:6-22).<br><br>“Further, in the embodiment 6, the standard cells described in the embodiments 1 and 5 are used. The gate lengths and the gate intervals are thereby equal in the patterns of the gate electrodes of the placed standard cells C91, C92 and C93, which leads to the improvement of the precision in the finished dimension of the gate electrodes. The improvement of the precision in the finished dimension of the gate electrodes can be realized not only inside each of the standard cells C91, C92 and C93 but also between the standard cells.” (Ichiryu at 18:1-9).<br><br>“[W]hen the standard cells are adjacently located, the gate lengths and the gate intervals in the patterns of the gate electrodes and the dummy gate electrodes are the same as when they are located alone.” (Ichiryu at 18:10-13). |

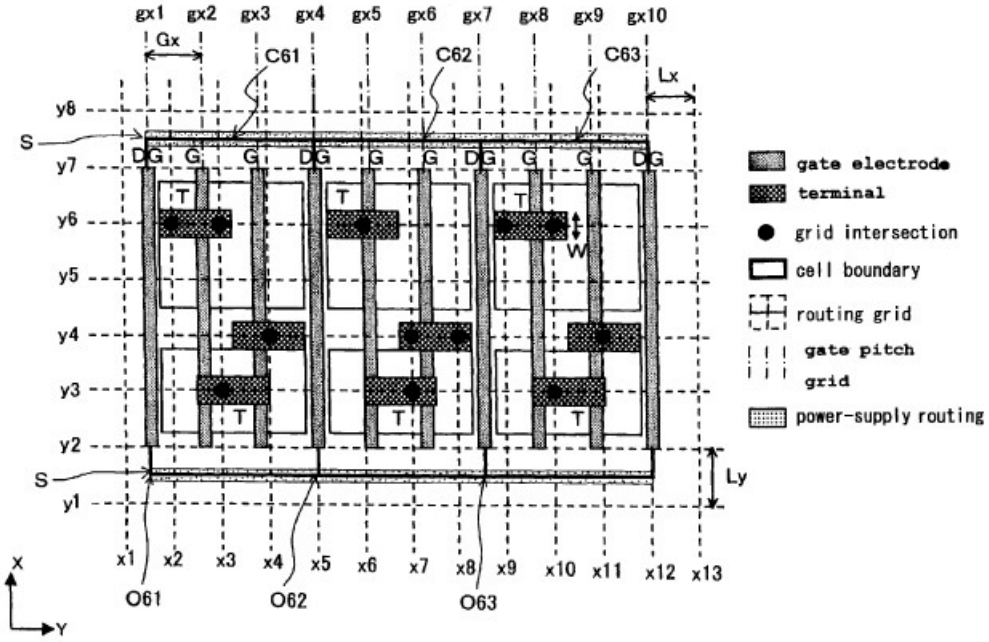
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | F I G. 11<br>  <br><br>(Ichiryu Fig. 11).<br>*See also* Ichiryu Figs. 1, 3, 8, 13, 14, 17, 18.<br>This limitation also would have been obvious to a person of ordinary skill in the art based on (1) Ichiryu alone; and/or (2) the teachings with respect to this claim element as detailed in the cover document of Respondent’s invalidity contentions and Respondent’s other invalidity charts. |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| 33. An integrated circuit device as recited in claim 32, wherein the diffusion region is formed along a first length of the first active linear conductive segment as measured in the first direction, | At least under Tela’s apparent infringement theory, Ichiryu discloses and/or renders obvious an integrated circuit device as recited in claim 32, wherein the diffusion region is formed along a first length of the first active linear conductive segment as measured in the first direction.<br><br>Ichiryu describes layout techniques for gate electrodes in a gate electrode region. Ichiryu describes layout techniques for gate electrodes, which are linear conductive segments, including placing them such that they extend in parallel. Ichiryu discloses transistors in the larger diffusion regions in Figures 1, 2, 3, 8, 12, 13, and 14 are PMOS transistors, and the transistors in the smaller diffusion regions in those figures are NMOS transistors, and the length of the NMOS transistor gates are different than the length of the PMOS transistor gates.<br><br>*See, e.g.*:<br><br>“[A]s the miniaturization of the process [continues], a precision in a finished dimension of the gate electrode ultimately obtained is deteriorated by an optical proximity effect when an interval between the gate electrodes and gate lengths of the gate electrodes are irregular in their patterns. When the precision in the finished dimension of the gate electrode is deteriorated, performances of respective transistors of the semiconductor integrated circuit are increasingly inconstant, which leads to an increased variation in a performance of the semiconductor integrate[d] circuit.” (Ichiryu at 2:23-32).<br><br>“[A]s recited in No. H10-32253 of the Publication of the Unexamined Japanese Patent Applications, the interval and the length of the gate electrodes in each standard cell are set regular so that the OPC is processed per standard cell in the conventional technology.” (Ichiryu at 2:37-41).<br><br>“The standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes….” (Ichiryu at 6:20-21).<br><br>“A standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes, wherein gate pitches of some of the gate electrodes are set to values different to the routing grid interval set along the X direction in parallel with the power-supply wiring of the standard cell, and a cell width along the X direction in parallel with the power-supply wiring of the |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | standard cell is set to an integral multiple of a minimum value of the gate pitches of the gate electrodes set to the values different to the routing grid interval set along the X direction.” (Ichiryu at 6:26-35).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, a precision in a finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:41-45).<br><br>“A standard cell according to the present invention comprises a plurality of gate electrodes and a plurality of dummy gate electrodes, wherein a cell width in the X direction in parallel with the power-supply wiring of the standard cell is an integral multiple of a minimum gate pitch of gate pitches of the gate electrodes and the dummy gate electrodes different to the routing grid interval along the X direction.” (Ichiryu at 6:46-52).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:58-62).<br><br>“The gate pitches of the standard cell are all preferably equal. Thereby, the pattern of the gate electrodes can impart a perfect regularity to the gate pitches, and the precision in the finished dimension of the gate electrodes can be further improved.” (Ichiryu at 6:66-7:3).<br><br>“Further, because the pattern of the gate electrodes can have the regularity, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be performed in each standard cell.” (Ichiryu at 8:21-24).<br><br>“Referring to reference symbols in FIG. 11, x1-x13 denote routing grids for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, y1-y8 denote routing grids disposed in parallel with the X direction and adjacent to one another in the Y direction, gx1-gx10 denote grids of gate pitches for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, C61, C62 and C63 are |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | standard cells, O61, O62 and O63 are respective origins of the standard cells C61, C62 and C63, … G denotes a gate electrode, and DG denotes a dummy gate electrode.” (Ichiryu at 14:32-44).<br><br>“In the standard cells C61, C62 and C63, gate lengths and gate intervals of the gate electrode G and dummy gate electrode DG are constant, and a cell width of the standard cells C61, C62 and C63 in the X direction is an integral multiple of a minimum value of a gate pitch Gx (value of gate pitch=gate length+gate interval) (In FIG. 11, the cell width of the standard cells C61, C62 and C63 is three times as wide as Gx).” (Ichiryu at 14:45-51).<br><br>“Not only inside the respective standard cells C61, C62 and C63, but also among the standard cells C61, C62 and C63 to one another, the gate lengths and the gate intervals are equal in the patterns of the gate electrodes and the dummy gate electrodes.” (Ichiryu at 15:47-51).<br><br>“In the embodiment 5, the gate lengths are all equal in the gate electrodes and the dummy gate electrodes….” (Ichiryu at 16:10-11).<br><br>“In FIG. 14, a reference symbol C81 denotes a standard cell. The standard cell C81 comprises gate electrodes G, dummy gate electrodes DG and two gate electrodes G2 having a gate length different to those of the gate electrode G and the dummy gate electrode DG, wherein a width of the gate electrode G2 is set so that a cell width of the standard cell C81 in the X direction is an integral multiple of the gate pitch Gx. In FIG. 14, the cell width of the standard cell C81 is nine times as wide as the gate pitch Gx. The width of the gate electrode G2 is thus set because a processing speed is expected to be faster when the cell width of each cell in the X direction is the integral multiple of the gate pitch Gx than when the cell width of each cell takes an arbitrary value in the placement using the conventional automatic placement & routing tool. However, the width of the gate electrode G2 is not necessarily set in the foregoing manner.” (Ichiryu at 16:15-30).<br><br>“As described, in the case of including the standard cell comprising the gate electrodes having the different gate lengths….” (Ichiryu at 16:32-34). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “In the constitution, the distance from the cell boundary of each standard cell to the gate electrode in the closest vicinity and the distance from the cell boundary of another standard cell adjacent thereto to the gate electrode in the closest vicinity are constant.” (Ichiryu at 16:65-17:2).<br><br>“For example, a distance from each of the cell boundary of the standard cells C61, C62 and C63 to the gate electrode in the X direction is ‘Gx-gate length/2’ and constant even in the constitution shown in FIG. 11 where the dummy gate electrodes DG are not provided. A distance between a transistor disposed at the end of each standard cell and the gate electrode G of the adjacent standard cell is ‘2Gx-gate length’ and constant. For example, even in the case where the dummy gate electrode DG is not provided in the constitution described referring to FIG. 11, the distance from each of the cell boundary of the respective standard cells C61, C62 and C63 to the gate electrode G located at the end of each of the standard cells in the X direction is constant at (Gx-gate length/2). Further, the distance from the gate electrode G located at the end of each of the standard cells to the gate electrode G located at the end of each of adjacent standard cells in the X direction is constant at (2Gx-gate length).” (Ichiryu at 17:6-22).<br><br>“Further, in the embodiment 6, the standard cells described in the embodiments 1 and 5 are used. The gate lengths and the gate intervals are thereby equal in the patterns of the gate electrodes of the placed standard cells C91, C92 and C93, which leads to the improvement of the precision in the finished dimension of the gate electrodes. The improvement of the precision in the finished dimension of the gate electrodes can be realized not only inside each of the standard cells C91, C92 and C93 but also between the standard cells.” (Ichiryu at 18:1-9).<br><br>“[W]hen the standard cells are adjacently located, the gate lengths and the gate intervals in the patterns of the gate electrodes and the dummy gate electrodes are the same as when they are located alone.” (Ichiryu at 18:10-13). |

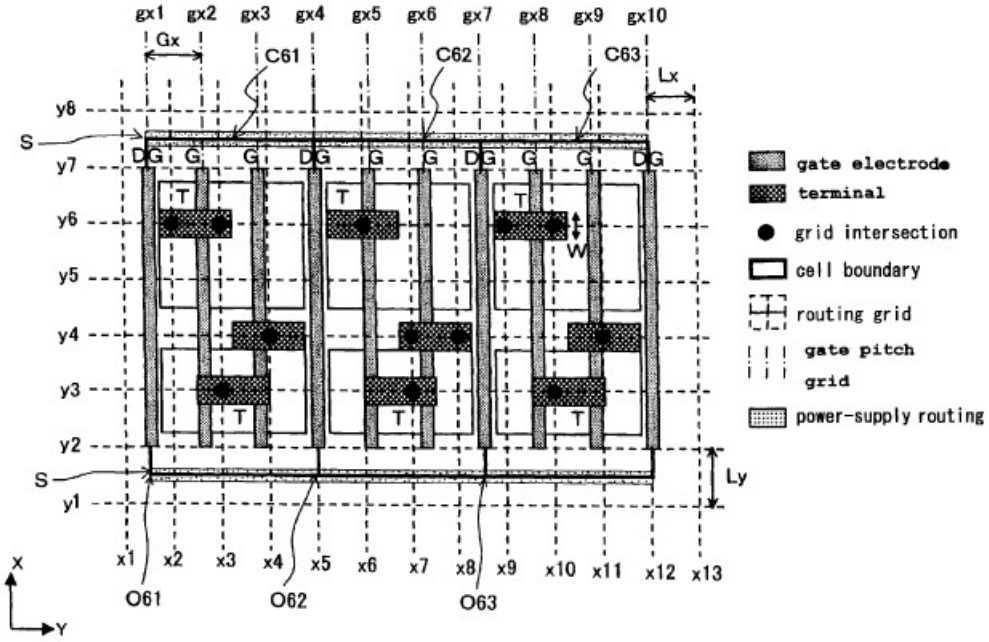
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | F I G. 11<br>  <br><br>(Ichiryu Fig. 11).<br>*See also* Ichiryu Figs. 1, 3, 8, 13, 14, 17, 18.<br>This limitation also would have been obvious to a person of ordinary skill in the art based on (1) Ichiryu alone; and/or (2) the teachings with respect to this claim element as detailed in the cover document of Respondent’s invalidity contentions and Respondent’s other invalidity charts. |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| [33.1] wherein the diffusion region is also formed along a second length of the second active linear conductive segment as measured in the first direction, and | At least under Tela’s apparent infringement theory, Ichiryu discloses and/or renders obvious wherein the diffusion region is also formed along a second length of the second active linear conductive segment as measured in the first direction.<br><br>Ichiryu describes layout techniques for gate electrodes in a gate electrode region. Ichiryu describes layout techniques for gate electrodes, which are linear conductive segments, including placing them such that they extend in parallel. Ichiryu discloses transistors in the larger diffusion regions in Figures 1, 2, 3, 8, 12, 13, and 14 are PMOS transistors, and the transistors in the smaller diffusion regions in those figures are NMOS transistors, and the length of the NMOS transistor gates are different than the length of the PMOS transistor gates.<br><br>*See, e.g.*:<br><br>“[A]s the miniaturization of the process [continues], a precision in a finished dimension of the gate electrode ultimately obtained is deteriorated by an optical proximity effect when an interval between the gate electrodes and gate lengths of the gate electrodes are irregular in their patterns. When the precision in the finished dimension of the gate electrode is deteriorated, performances of respective transistors of the semiconductor integrated circuit are increasingly inconstant, which leads to an increased variation in a performance of the semiconductor integrate[d] circuit.” (Ichiryu at 2:23-32).<br><br>“[A]s recited in No. H10-32253 of the Publication of the Unexamined Japanese Patent Applications, the interval and the length of the gate electrodes in each standard cell are set regular so that the OPC is processed per standard cell in the conventional technology.” (Ichiryu at 2:37-41).<br><br>“The standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes….” (Ichiryu at 6:20-21).<br><br>“A standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes, wherein gate pitches of some of the gate electrodes are set to values different to the routing grid interval set along the X direction in parallel with the power-supply wiring of the standard cell, and a cell width along the X direction in parallel with the power-supply wiring of the |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | standard cell is set to an integral multiple of a minimum value of the gate pitches of the gate electrodes set to the values different to the routing grid interval set along the X direction.” (Ichiryu at 6:26-35).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, a precision in a finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:41-45).<br><br>“A standard cell according to the present invention comprises a plurality of gate electrodes and a plurality of dummy gate electrodes, wherein a cell width in the X direction in parallel with the power-supply wiring of the standard cell is an integral multiple of a minimum gate pitch of gate pitches of the gate electrodes and the dummy gate electrodes different to the routing grid interval along the X direction.” (Ichiryu at 6:46-52).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:58-62).<br><br>“The gate pitches of the standard cell are all preferably equal. Thereby, the pattern of the gate electrodes can impart a perfect regularity to the gate pitches, and the precision in the finished dimension of the gate electrodes can be further improved.” (Ichiryu at 6:66-7:3).<br><br>“Further, because the pattern of the gate electrodes can have the regularity, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be performed in each standard cell.” (Ichiryu at 8:21-24).<br><br>“Referring to reference symbols in FIG. 11, x1-x13 denote routing grids for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, y1-y8 denote routing grids disposed in parallel with the X direction and adjacent to one another in the Y direction, gx1-gx10 denote grids of gate pitches for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, C61, C62 and C63 are |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | standard cells, O61, O62 and O63 are respective origins of the standard cells C61, C62 and C63, … G denotes a gate electrode, and DG denotes a dummy gate electrode.” (Ichiryu at 14:32-44).<br><br>“In the standard cells C61, C62 and C63, gate lengths and gate intervals of the gate electrode G and dummy gate electrode DG are constant, and a cell width of the standard cells C61, C62 and C63 in the X direction is an integral multiple of a minimum value of a gate pitch Gx (value of gate pitch=gate length+gate interval) (In FIG. 11, the cell width of the standard cells C61, C62 and C63 is three times as wide as Gx).” (Ichiryu at 14:45-51).<br><br>“Not only inside the respective standard cells C61, C62 and C63, but also among the standard cells C61, C62 and C63 to one another, the gate lengths and the gate intervals are equal in the patterns of the gate electrodes and the dummy gate electrodes.” (Ichiryu at 15:47-51).<br><br>“In the embodiment 5, the gate lengths are all equal in the gate electrodes and the dummy gate electrodes….” (Ichiryu at 16:10-11).<br><br>“In FIG. 14, a reference symbol C81 denotes a standard cell. The standard cell C81 comprises gate electrodes G, dummy gate electrodes DG and two gate electrodes G2 having a gate length different to those of the gate electrode G and the dummy gate electrode DG, wherein a width of the gate electrode G2 is set so that a cell width of the standard cell C81 in the X direction is an integral multiple of the gate pitch Gx. In FIG. 14, the cell width of the standard cell C81 is nine times as wide as the gate pitch Gx. The width of the gate electrode G2 is thus set because a processing speed is expected to be faster when the cell width of each cell in the X direction is the integral multiple of the gate pitch Gx than when the cell width of each cell takes an arbitrary value in the placement using the conventional automatic placement & routing tool. However, the width of the gate electrode G2 is not necessarily set in the foregoing manner.” (Ichiryu at 16:15-30).<br><br>“As described, in the case of including the standard cell comprising the gate electrodes having the different gate lengths….” (Ichiryu at 16:32-34). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “In the constitution, the distance from the cell boundary of each standard cell to the gate electrode in the closest vicinity and the distance from the cell boundary of another standard cell adjacent thereto to the gate electrode in the closest vicinity are constant.” (Ichiryu at 16:65-17:2).<br><br>“For example, a distance from each of the cell boundary of the standard cells C61, C62 and C63 to the gate electrode in the X direction is ‘Gx-gate length/2’ and constant even in the constitution shown in FIG. 11 where the dummy gate electrodes DG are not provided. A distance between a transistor disposed at the end of each standard cell and the gate electrode G of the adjacent standard cell is ‘2Gx-gate length’ and constant. For example, even in the case where the dummy gate electrode DG is not provided in the constitution described referring to FIG. 11, the distance from each of the cell boundary of the respective standard cells C61, C62 and C63 to the gate electrode G located at the end of each of the standard cells in the X direction is constant at (Gx-gate length/2). Further, the distance from the gate electrode G located at the end of each of the standard cells to the gate electrode G located at the end of each of adjacent standard cells in the X direction is constant at (2Gx-gate length).” (Ichiryu at 17:6-22).<br><br>“Further, in the embodiment 6, the standard cells described in the embodiments 1 and 5 are used. The gate lengths and the gate intervals are thereby equal in the patterns of the gate electrodes of the placed standard cells C91, C92 and C93, which leads to the improvement of the precision in the finished dimension of the gate electrodes. The improvement of the precision in the finished dimension of the gate electrodes can be realized not only inside each of the standard cells C91, C92 and C93 but also between the standard cells.” (Ichiryu at 18:1-9).<br><br>“[W]hen the standard cells are adjacently located, the gate lengths and the gate intervals in the patterns of the gate electrodes and the dummy gate electrodes are the same as when they are located alone.” (Ichiryu at 18:10-13). |

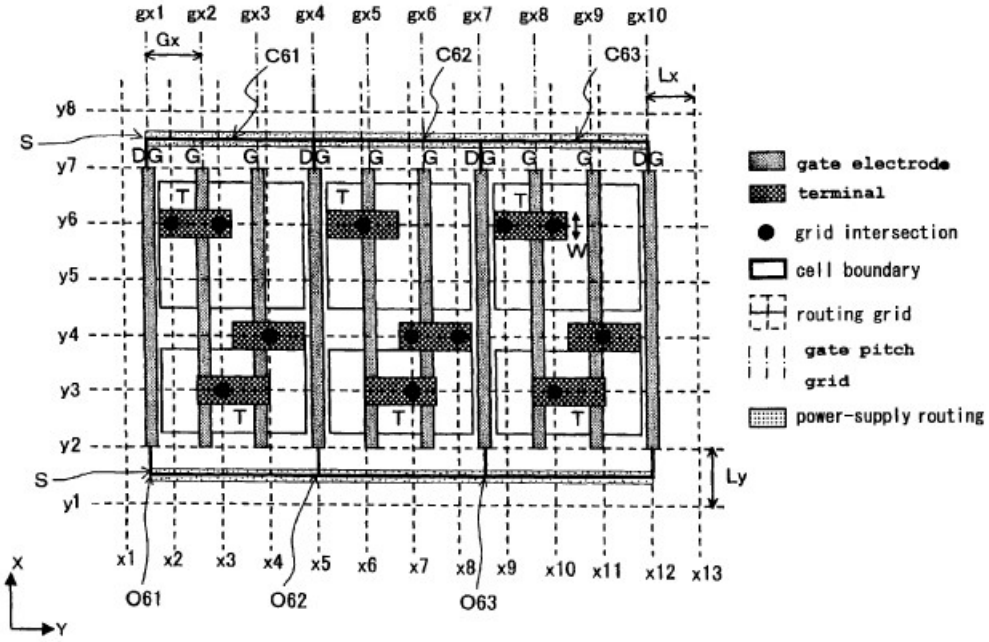
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | F I G. 11<br>  <br><br>(Ichiryu Fig. 11).<br>*See also* Ichiryu Figs. 1, 3, 8, 13, 14, 17, 18.<br>This limitation also would have been obvious to a person of ordinary skill in the art based on (1) Ichiryu alone; and/or (2) the teachings with respect to this claim element as detailed in the cover document of Respondent’s invalidity contentions and Respondent’s other invalidity charts. |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| [33.2] wherein the first length of the first active linear conductive segment is different than the second length of the second active linear conductive segment. | At least under Tela’s apparent infringement theory, Ichiryu discloses and/or renders obvious wherein the first length of the first active linear conductive segment is different than the second length of the second active linear conductive segment.<br><br>Ichiryu discloses transistors in the larger diffusion regions in Figures 1, 2, 3, 8, 12, 13, and 14 are PMOS transistors, and the transistors in the smaller diffusion regions in those figures are NMOS transistors, and the length of the NMOS transistor gates are different than the length of the PMOS transistor gates.<br><br>*See, e.g.*:<br><br>“[A]s the miniaturization of the process [continues], a precision in a finished dimension of the gate electrode ultimately obtained is deteriorated by an optical proximity effect when an interval between the gate electrodes and gate lengths of the gate electrodes are irregular in their patterns. When the precision in the finished dimension of the gate electrode is deteriorated, performances of respective transistors of the semiconductor integrated circuit are increasingly inconstant, which leads to an increased variation in a performance of the semiconductor integrate[d] circuit.” (Ichiryu at 2:23-32).<br><br>“[A]s recited in No. H10-32253 of the Publication of the Unexamined Japanese Patent Applications, the interval and the length of the gate electrodes in each standard cell are set regular so that the OPC is processed per standard cell in the conventional technology.” (Ichiryu at 2:37-41).<br><br>“The standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes….” (Ichiryu at 6:20-21).<br><br>“A standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes, wherein gate pitches of some of the gate electrodes are set to values different to the routing grid interval set along the X direction in parallel with the power-supply wiring of the standard cell, and a cell width along the X direction in parallel with the power-supply wiring of the standard cell is set to an integral multiple of a minimum value of the gate pitches of the gate |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | electrodes set to the values different to the routing grid interval set along the X direction.” (Ichiryu at 6:26-35).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, a precision in a finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:41-45).<br><br>“A standard cell according to the present invention comprises a plurality of gate electrodes and a plurality of dummy gate electrodes, wherein a cell width in the X direction in parallel with the power-supply wiring of the standard cell is an integral multiple of a minimum gate pitch of gate pitches of the gate electrodes and the dummy gate electrodes different to the routing grid interval along the X direction.” (Ichiryu at 6:46-52).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:58-62).<br><br>“The gate pitches of the standard cell are all preferably equal. Thereby, the pattern of the gate electrodes can impart a perfect regularity to the gate pitches, and the precision in the finished dimension of the gate electrodes can be further improved.” (Ichiryu at 6:66-7:3).<br><br>“Further, because the pattern of the gate electrodes can have the regularity, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be performed in each standard cell.” (Ichiryu at 8:21-24).<br><br>“Referring to reference symbols in FIG. 11, x1-x13 denote routing grids for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, y1-y8 denote routing grids disposed in parallel with the X direction and adjacent to one another in the Y direction, gx1-gx10 denote grids of gate pitches for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, C61, C62 and C63 are |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | standard cells, O61, O62 and O63 are respective origins of the standard cells C61, C62 and C63, … G denotes a gate electrode, and DG denotes a dummy gate electrode.” (Ichiryu at 14:32-44).<br><br>“In the standard cells C61, C62 and C63, gate lengths and gate intervals of the gate electrode G and dummy gate electrode DG are constant, and a cell width of the standard cells C61, C62 and C63 in the X direction is an integral multiple of a minimum value of a gate pitch Gx (value of gate pitch=gate length+gate interval) (In FIG. 11, the cell width of the standard cells C61, C62 and C63 is three times as wide as Gx).” (Ichiryu at 14:45-51).<br><br>“Not only inside the respective standard cells C61, C62 and C63, but also among the standard cells C61, C62 and C63 to one another, the gate lengths and the gate intervals are equal in the patterns of the gate electrodes and the dummy gate electrodes.” (Ichiryu at 15:47-51).<br><br>“In the embodiment 5, the gate lengths are all equal in the gate electrodes and the dummy gate electrodes….” (Ichiryu at 16:10-11).<br><br>“In FIG. 14, a reference symbol C81 denotes a standard cell. The standard cell C81 comprises gate electrodes G, dummy gate electrodes DG and two gate electrodes G2 having a gate length different to those of the gate electrode G and the dummy gate electrode DG, wherein a width of the gate electrode G2 is set so that a cell width of the standard cell C81 in the X direction is an integral multiple of the gate pitch Gx. In FIG. 14, the cell width of the standard cell C81 is nine times as wide as the gate pitch Gx. The width of the gate electrode G2 is thus set because a processing speed is expected to be faster when the cell width of each cell in the X direction is the integral multiple of the gate pitch Gx than when the cell width of each cell takes an arbitrary value in the placement using the conventional automatic placement & routing tool. However, the width of the gate electrode G2 is not necessarily set in the foregoing manner.” (Ichiryu at 16:15-30).<br><br>“As described, in the case of including the standard cell comprising the gate electrodes having the different gate lengths….” (Ichiryu at 16:32-34). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “In the constitution, the distance from the cell boundary of each standard cell to the gate electrode in the closest vicinity and the distance from the cell boundary of another standard cell adjacent thereto to the gate electrode in the closest vicinity are constant.” (Ichiryu at 16:65-17:2).<br><br>“For example, a distance from each of the cell boundary of the standard cells C61, C62 and C63 to the gate electrode in the X direction is ‘Gx-gate length/2’ and constant even in the constitution shown in FIG. 11 where the dummy gate electrodes DG are not provided. A distance between a transistor disposed at the end of each standard cell and the gate electrode G of the adjacent standard cell is ‘2Gx-gate length’ and constant. For example, even in the case where the dummy gate electrode DG is not provided in the constitution described referring to FIG. 11, the distance from each of the cell boundary of the respective standard cells C61, C62 and C63 to the gate electrode G located at the end of each of the standard cells in the X direction is constant at (Gx-gate length/2). Further, the distance from the gate electrode G located at the end of each of the standard cells to the gate electrode G located at the end of each of adjacent standard cells in the X direction is constant at (2Gx-gate length).” (Ichiryu at 17:6-22).<br><br>“Further, in the embodiment 6, the standard cells described in the embodiments 1 and 5 are used. The gate lengths and the gate intervals are thereby equal in the patterns of the gate electrodes of the placed standard cells C91, C92 and C93, which leads to the improvement of the precision in the finished dimension of the gate electrodes. The improvement of the precision in the finished dimension of the gate electrodes can be realized not only inside each of the standard cells C91, C92 and C93 but also between the standard cells.” (Ichiryu at 18:1-9).<br><br>“[W]hen the standard cells are adjacently located, the gate lengths and the gate intervals in the patterns of the gate electrodes and the dummy gate electrodes are the same as when they are located alone.” (Ichiryu at 18:10-13). |

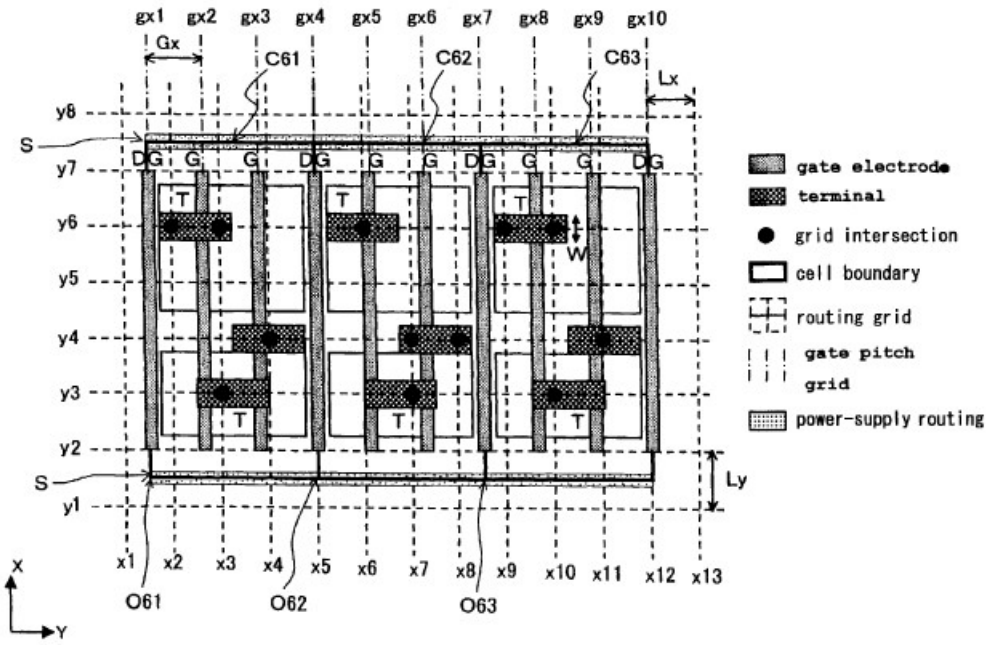
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | F I G. 11<br>  <br><br>(Ichiryu Fig. 11).<br>*See also* Ichiryu Figs. 1, 3, 8, 13, 14, 17, 18.<br>This limitation also would have been obvious to a person of ordinary skill in the art based on (1) Ichiryu alone; and/or (2) the teachings with respect to this claim element as detailed in the cover document of Respondent’s invalidity contentions and Respondent’s other invalidity charts. |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| 34. An integrated circuit device as recited in claim 33, wherein the first and second lengths extend in the first direction from a common position relative to the first direction. | At least under Tela’s apparent infringement theory, Ichiryu discloses and/or renders obvious an integrated circuit device as recited in claim 33, wherein the first and second lengths extend in the first direction from a common position relative to the first direction.<br><br>Ichiryu discloses transistors in the larger diffusion regions in Figures 1, 2, 3, 8, 12, 13, and 14 are PMOS transistors, and the transistors in the smaller diffusion regions in those figures are NMOS transistors, and the length of the NMOS transistor gates are different than the length of the PMOS transistor gates.<br><br>*See, e.g.*:<br><br>“[A]s the miniaturization of the process [continues], a precision in a finished dimension of the gate electrode ultimately obtained is deteriorated by an optical proximity effect when an interval between the gate electrodes and gate lengths of the gate electrodes are irregular in their patterns. When the precision in the finished dimension of the gate electrode is deteriorated, performances of respective transistors of the semiconductor integrated circuit are increasingly inconstant, which leads to an increased variation in a performance of the semiconductor integrate[d] circuit.” (Ichiryu at 2:23-32).<br><br>“[A]s recited in No. H10-32253 of the Publication of the Unexamined Japanese Patent Applications, the interval and the length of the gate electrodes in each standard cell are set regular so that the OPC is processed per standard cell in the conventional technology.” (Ichiryu at 2:37-41).<br><br>“The standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes….” (Ichiryu at 6:20-21).<br><br>“A standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes, wherein gate pitches of some of the gate electrodes are set to values different to the routing grid interval set along the X direction in parallel with the power-supply wiring of the standard cell, and a cell width along the X direction in parallel with the power-supply wiring of the standard cell is set to an integral multiple of a minimum value of the gate pitches of the gate |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | electrodes set to the values different to the routing grid interval set along the X direction.” (Ichiryu at 6:26-35).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, a precision in a finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:41-45).<br><br>“A standard cell according to the present invention comprises a plurality of gate electrodes and a plurality of dummy gate electrodes, wherein a cell width in the X direction in parallel with the power-supply wiring of the standard cell is an integral multiple of a minimum gate pitch of gate pitches of the gate electrodes and the dummy gate electrodes different to the routing grid interval along the X direction.” (Ichiryu at 6:46-52).<br><br>“[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell.” (Ichiryu at 6:58-62).<br><br>“The gate pitches of the standard cell are all preferably equal. Thereby, the pattern of the gate electrodes can impart a perfect regularity to the gate pitches, and the precision in the finished dimension of the gate electrodes can be further improved.” (Ichiryu at 6:66-7:3).<br><br>“Further, because the pattern of the gate electrodes can have the regularity, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be performed in each standard cell.” (Ichiryu at 8:21-24).<br><br>“Referring to reference symbols in FIG. 11, x1-x13 denote routing grids for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, y1-y8 denote routing grids disposed in parallel with the X direction and adjacent to one another in the Y direction, gx1-gx10 denote grids of gate pitches for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, C61, C62 and C63 are |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | standard cells, O61, O62 and O63 are respective origins of the standard cells C61, C62 and C63, … G denotes a gate electrode, and DG denotes a dummy gate electrode.” (Ichiryu at 14:32-44).<br><br>“In the standard cells C61, C62 and C63, gate lengths and gate intervals of the gate electrode G and dummy gate electrode DG are constant, and a cell width of the standard cells C61, C62 and C63 in the X direction is an integral multiple of a minimum value of a gate pitch Gx (value of gate pitch=gate length+gate interval) (In FIG. 11, the cell width of the standard cells C61, C62 and C63 is three times as wide as Gx).” (Ichiryu at 14:45-51).<br><br>“Not only inside the respective standard cells C61, C62 and C63, but also among the standard cells C61, C62 and C63 to one another, the gate lengths and the gate intervals are equal in the patterns of the gate electrodes and the dummy gate electrodes.” (Ichiryu at 15:47-51).<br><br>“In the embodiment 5, the gate lengths are all equal in the gate electrodes and the dummy gate electrodes….” (Ichiryu at 16:10-11).<br><br>“In FIG. 14, a reference symbol C81 denotes a standard cell. The standard cell C81 comprises gate electrodes G, dummy gate electrodes DG and two gate electrodes G2 having a gate length different to those of the gate electrode G and the dummy gate electrode DG, wherein a width of the gate electrode G2 is set so that a cell width of the standard cell C81 in the X direction is an integral multiple of the gate pitch Gx. In FIG. 14, the cell width of the standard cell C81 is nine times as wide as the gate pitch Gx. The width of the gate electrode G2 is thus set because a processing speed is expected to be faster when the cell width of each cell in the X direction is the integral multiple of the gate pitch Gx than when the cell width of each cell takes an arbitrary value in the placement using the conventional automatic placement & routing tool. However, the width of the gate electrode G2 is not necessarily set in the foregoing manner.” (Ichiryu at 16:15-30).<br><br>“As described, in the case of including the standard cell comprising the gate electrodes having the different gate lengths….” (Ichiryu at 16:32-34). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “In the constitution, the distance from the cell boundary of each standard cell to the gate electrode in the closest vicinity and the distance from the cell boundary of another standard cell adjacent thereto to the gate electrode in the closest vicinity are constant.” (Ichiryu at 16:65-17:2).<br><br>“For example, a distance from each of the cell boundary of the standard cells C61, C62 and C63 to the gate electrode in the X direction is ‘Gx-gate length/2’ and constant even in the constitution shown in FIG. 11 where the dummy gate electrodes DG are not provided. A distance between a transistor disposed at the end of each standard cell and the gate electrode G of the adjacent standard cell is ‘2Gx-gate length’ and constant. For example, even in the case where the dummy gate electrode DG is not provided in the constitution described referring to FIG. 11, the distance from each of the cell boundary of the respective standard cells C61, C62 and C63 to the gate electrode G located at the end of each of the standard cells in the X direction is constant at (Gx-gate length/2). Further, the distance from the gate electrode G located at the end of each of the standard cells to the gate electrode G located at the end of each of adjacent standard cells in the X direction is constant at (2Gx-gate length).” (Ichiryu at 17:6-22).<br><br>“Further, in the embodiment 6, the standard cells described in the embodiments 1 and 5 are used. The gate lengths and the gate intervals are thereby equal in the patterns of the gate electrodes of the placed standard cells C91, C92 and C93, which leads to the improvement of the precision in the finished dimension of the gate electrodes. The improvement of the precision in the finished dimension of the gate electrodes can be realized not only inside each of the standard cells C91, C92 and C93 but also between the standard cells.” (Ichiryu at 18:1-9).<br><br>“[W]hen the standard cells are adjacently located, the gate lengths and the gate intervals in the patterns of the gate electrodes and the dummy gate electrodes are the same as when they are located alone.” (Ichiryu at 18:10-13). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | F I G. 11<br>  <br><br>(Ichiryu Fig. 11).<br>*See also* Ichiryu Figs. 1, 3, 8, 13, 14, 17, 18.<br>This limitation also would have been obvious to a person of ordinary skill in the art based on (1) Ichiryu alone; and/or (2) the teachings with respect to this claim element as detailed in the cover document of Respondent’s invalidity contentions and Respondent’s other invalidity charts. |

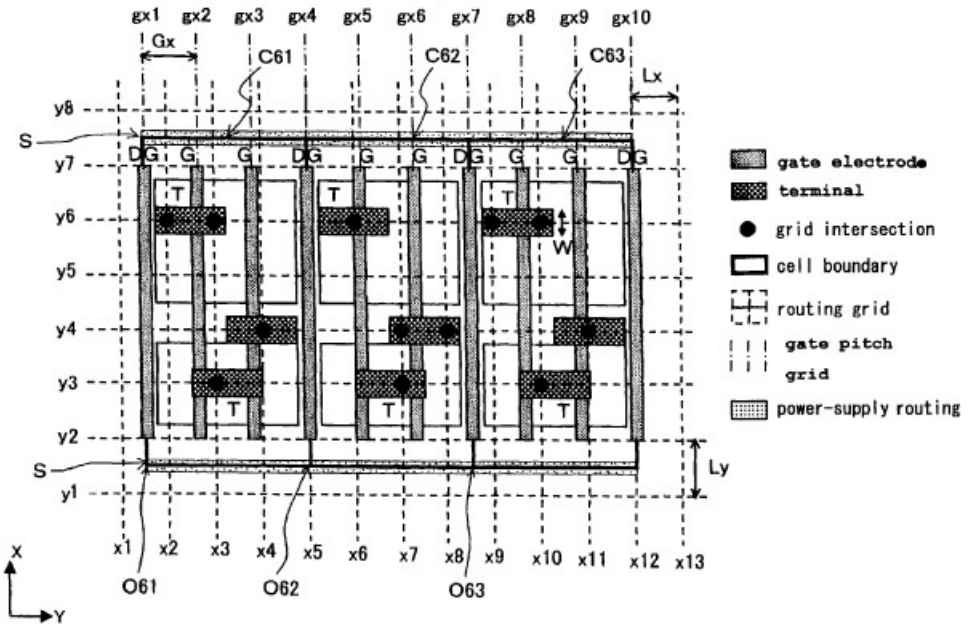
| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| 35. An integrated circuit device as recited in claim 2, wherein the non-gate linear conductive segment is positioned between two active linear conductive segments. | At least under Tela’s apparent infringement theory, Ichiryu discloses and/or renders obvious an integrated circuit device as recited in claim 2, wherein the non-gate linear conductive segment is positioned between two active linear conductive segments.<br><br>Ichiryu describes and depicts multiple dummy gates between linear conductive segments, e.g. “dummy gate eletrodes” or “DG.”<br><br>*See, e.g.*:<br><br>“[A]s the miniaturization of the process [continues], a precision in a finished dimension of the gate electrode ultimately obtained is deteriorated by an optical proximity effect when an interval between the gate electrodes and gate lengths of the gate electrodes are irregular in their patterns. When the precision in the finished dimension of the gate electrode is deteriorated, performances of respective transistors of the semiconductor integrated circuit are increasingly inconstant, which leads to an increased variation in a performance of the semiconductor integrate[d] circuit.” (Ichiryu at 2:23-32).<br><br>“[A]s recited in No. H10-32253 of the Publication of the Unexamined Japanese Patent Applications, the interval and the length of the gate electrodes in each standard cell are set regular so that the OPC is processed per standard cell in the conventional technology.” (Ichiryu at 2:37-41).“<br><br>Dummy gate electrodes DG are provided on cell boundaries of standard cells C41’, C4[2]’ and C43’ disposed on the upper side in FIG. 18. These dummy gate electrodes DG are shared between the adjacent standard cells. The gate electrodes G and the dummy gate electrodes DG are respectively equally spaced, and their gate [] lengths are equal.” (Ichiryu at 2:45-50).<br><br>“[W]hen the regions R1, R2 and R3 for adjusting the cell width to the integral multiple of the routing grid interval are provided, the gate electrode located on the cell boundary of the standard cell cannot be shared. There is a possibility that the dummy electrodes DG are located with less than a minimum interval allowed in a design rule therebetween, which results in an error in the design rule. In order to |

| '012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | avoid the foregoing error in the design rule, it is necessary to enlarge the gate length, for example, in the same manner as the dummy gate DG2 disposed on the lower side in FIG. 18." (Ichiryu at 3:7-16).<br><br>"Though the gate interval in each standard cell can be maintained at the constant level when such the gate length enlargement is executed, the gate length becomes irregular at the dummy gate electrodes DG2, which results in the imprecision of the finished dimension of the gate electrodes. Further, the OPC cannot be processed in each standard cell due to the different gate lengths in the dummy gate electrodes DG in each standard cell and the dummy gate electrodes DG2 adjacent thereto." (Ichiryu at 3:17-25).<br><br>"The standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes…." (Ichiryu at 6:20-21).<br><br>"A standard cell according to the present invention is a standard cell comprising a plurality of gate electrodes, wherein gate pitches of some of the gate electrodes are set to values different to the routing grid interval set along the X direction in parallel with the power-supply wiring of the standard cell, and a cell width along the X direction in parallel with the power-supply wiring of the standard cell is set to an integral multiple of a minimum value of the gate pitches of the gate electrodes set to the values different to the routing grid interval set along the X direction." (Ichiryu at 6:26-35).<br><br>"[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, a precision in a finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell." (Ichiryu at 6:41-45).<br><br>"A standard cell according to the present invention comprises a plurality of gate electrodes and a plurality of dummy gate electrodes, wherein a cell width in the X direction in parallel with the power-supply wiring of the standard cell is an integral multiple of a minimum gate pitch of gate pitches of the gate electrodes and the dummy gate electrodes different to the routing grid interval along the X direction." (Ichiryu at 6:46-52). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “[T]he gate electrode pattern including a gate length and a gate interval can be regular. Then, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be processed in each standard cell. As another advantage, the provision of the dummy gate electrodes can further improve the regularity of the gate length and gate interval, which largely contributes to the facilitation of the OPC process in each standard cell.” (Ichiryu at 6:58-65).<br><br>“The gate pitches of the standard cell are all preferably equal. Thereby, the pattern of the gate electrodes can impart a perfect regularity to the gate pitches, and the precision in the finished dimension of the gate electrodes can be further improved.” (Ichiryu at 6:66-7:3).<br><br>“Further, because the pattern of the gate electrodes can have the regularity, the precision in the finished dimension of the gate electrodes can be improved, and the OPC can be performed in each standard cell.” (Ichiryu at 8:21-24).<br><br>“Referring to reference symbols in FIG. 11, x1-x13 denote routing grids for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, y1-y8 denote routing grids disposed in parallel with the X direction and adjacent to one another in the Y direction, gx1-gx10 denote grids of gate pitches for the automatic placement & routing disposed in parallel with the Y direction and adjacent to one another in the X direction, C61, C62 and C63 are standard cells, O61, O62 and O63 are respective origins of the standard cells C61, C62 and C63, … G denotes a gate electrode, and DG denotes a dummy gate electrode.” (Ichiryu at 14:32-44).<br><br>“In the standard cells C61, C62 and C63, gate lengths and gate intervals of the gate electrode G and dummy gate electrode DG are constant, and a cell width of the standard cells C61, C62 and C63 in the X direction is an integral multiple of a minimum value of a gate pitch Gx (value of gate pitch=gate length+gate interval) (In FIG. 11, the cell width of the standard cells C61, C62 and C63 is three times as wide as Gx).” (Ichiryu at 14:45-51). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “Not only inside the respective standard cells C61, C62 and C63, but also among the standard cells C61, C62 and C63 to one another, the gate lengths and the gate intervals are equal in the patterns of the gate electrodes and the dummy gate electrodes.” (Ichiryu at 15:47-51).<br><br>“In the embodiment 5, the gate lengths are all equal in the gate electrodes and the dummy gate electrodes….” (Ichiryu at 16:10-11).<br><br>“In FIG. 14, a reference symbol C81 denotes a standard cell. The standard cell C81 comprises gate electrodes G, dummy gate electrodes DG and two gate electrodes G2 having a gate length different to those of the gate electrode G and the dummy gate electrode DG, wherein a width of the gate electrode G2 is set so that a cell width of the standard cell C81 in the X direction is an integral multiple of the gate pitch Gx. In FIG. 14, the cell width of the standard cell C81 is nine times as wide as the gate pitch Gx. The width of the gate electrode G2 is thus set because a processing speed is expected to be faster when the cell width of each cell in the X direction is the integral multiple of the gate pitch Gx than when the cell width of each cell takes an arbitrary value in the placement using the conventional automatic placement & routing tool. However, the width of the gate electrode G2 is not necessarily set in the foregoing manner.” (Ichiryu at 16:15-30).<br><br>“As described, in the case of including the standard cell comprising the gate electrodes having the different gate lengths….” (Ichiryu at 16:32-34).<br><br>“[T]he embodiment 5 can be applied in the same manner to a cell structure where the dummy gate electrodes having the different gate lengths are provided and a cell structure where the gate electrodes and the dummy gate electrodes having the different gate intervals are provided. The description of the embodiment 5 is premised on the provision of the dummy gates DG….” (Ichiryu at 16:53-59).<br><br>“In the constitution, the distance from the cell boundary of each standard cell to the gate electrode in the closest vicinity and the distance from the cell boundary of another standard cell adjacent thereto to the gate electrode in the closest vicinity are constant.” (Ichiryu at 16:65-17:2). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | “For example, a distance from each of the cell boundary of the standard cells C61, C62 and C63 to the gate electrode in the X direction is ‘Gx-gate length/2’ and constant even in the constitution shown in FIG. 11 where the dummy gate electrodes DG are not provided. A distance between a transistor disposed at the end of each standard cell and the gate electrode G of the adjacent standard cell is ‘2Gx-gate length’ and constant. For example, even in the case where the dummy gate electrode DG is not provided in the constitution described referring to FIG. 11, the distance from each of the cell boundary of the respective standard cells C61, C62 and C63 to the gate electrode G located at the end of each of the standard cells in the X direction is constant at (Gx-gate length/2). Further, the distance from the gate electrode G located at the end of each of the standard cells to the gate electrode G located at the end of each of adjacent standard cells in the X direction is constant at (2Gx-gate length).” (Ichiryu at 17:6-22).<br><br>“Further, in the embodiment 6, the standard cells described in the embodiments 1 and 5 are used. The gate lengths and the gate intervals are thereby equal in the patterns of the gate electrodes of the placed standard cells C91, C92 and C93, which leads to the improvement of the precision in the finished dimension of the gate electrodes. The improvement of the precision in the finished dimension of the gate electrodes can be realized not only inside each of the standard cells C91, C92 and C93 but also between the standard cells.” (Ichiryu at 18:1-9).<br><br>“[W]hen the standard cells are adjacently located, the gate lengths and the gate intervals in the patterns of the gate electrodes and the dummy gate electrodes are the same as when they are located alone.” (Ichiryu at 18:10-13). |

| ’012 Patent Claim Limitation | U.S. Patent No. 7,503,026 to Ichiryu |
|---|---|
| | F I G. 11<br>  <br><br>(Ichiryu Fig. 11).<br>*See also* Ichiryu at Figs. 1, 2, 3, 8, 12, 13, 14.<br>This limitation also would have been obvious to a person of ordinary skill in the art based on (1) Ichiryu alone; and/or (2) the teachings with respect to this claim element as detailed in the cover document of Respondent’s invalidity contentions and Respondent’s other invalidity charts. |