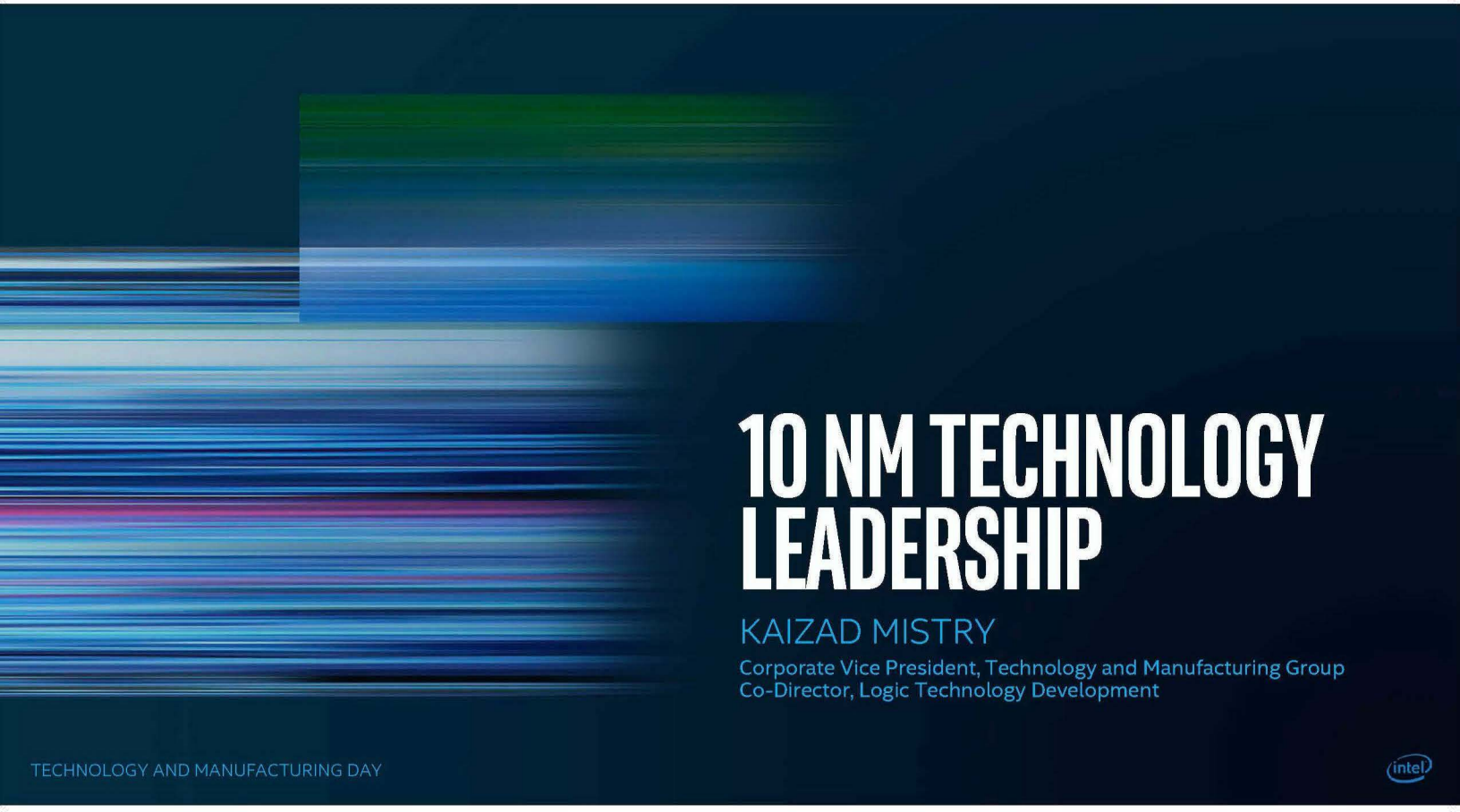

10 NM TECHNOLOGY LEADERSHIP
KAIZAD MISTRY
Corporate Vice President, Technology and Manufacturing Group
Co-Director, Logic Technology Development
TECHNOLOGY AND MANUFACTURING DAY
intel

DISCLOSURES

Intel Technology and Manufacturing Day 2017 occurs during Intel's "Quiet Period," before Intel announces its 2017 first quarter financial and operating results. Therefore, presenters will not be addressing first quarter information during this year's program.

Statements in this presentation that refer to forecasts, future plans and expectations are forward-looking statements that involve a number of risks and uncertainties. Words such as "anticipates," "expects," "intends," "goals," "plans," "believes," "seeks," "estimates," "continues," "may," "will," "would," "should," "could," and variations of such words and similar expressions are intended to identify such forward-looking statements. Statements that refer to or are based on projections, uncertain events or assumptions also identify forward-looking statements. Such statements are based on management's expectations as of March 28, 2017, and involve many risks and uncertainties that could cause actual results to differ materially from those expressed or implied in these forward-looking statements. Important factors that could cause actual results to differ materially from the company's expectations are set forth in Intel's earnings release dated January 26, 2017, which is included as an exhibit to Intel's Form 8-K furnished to the SEC on such date. Additional information regarding these and other factors that could affect Intel's results is included in Intel's SEC filings, including the company's most recent reports on Forms 10-K, 10-Q and 8-K reports may be obtained by visiting our Investor Relations website at www.intc.com or the SEC's website at www.sec.gov.

KEY MESSAGES

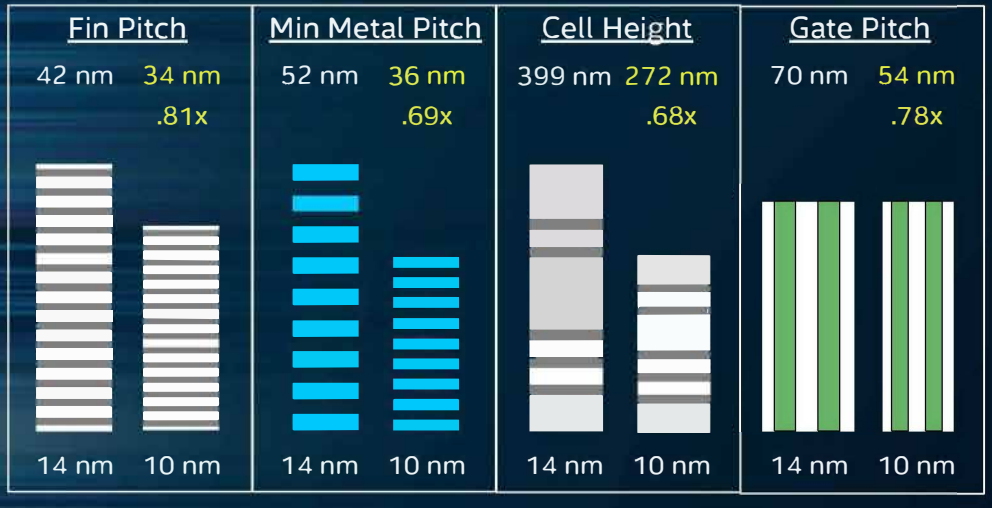
- Intel's 10 nm process technology has the world's tightest transistor & metal pitches along with hyper scaling features for leadership density
- Intel's 10 nm technology is a full generation ahead of other "10 nm" technologies
- Enhanced versions of Intel 10 nm provide improved power/performance within the 10 nm process family
- Hyper scaling extracts the full value of multi-patterning schemes and allows Intel to continue the benefits of Moore's Law economics

Source: Amalgamation of analyst data and Intel analysis, based upon current expectations and available information

AGENDA

- Intel 10 nm Features
- Intel 10 nm Hyper Scaling
- Enhanced Versions of Intel 10 nm
- Hyper Scaling Redux

10 NM HYPER SCALING

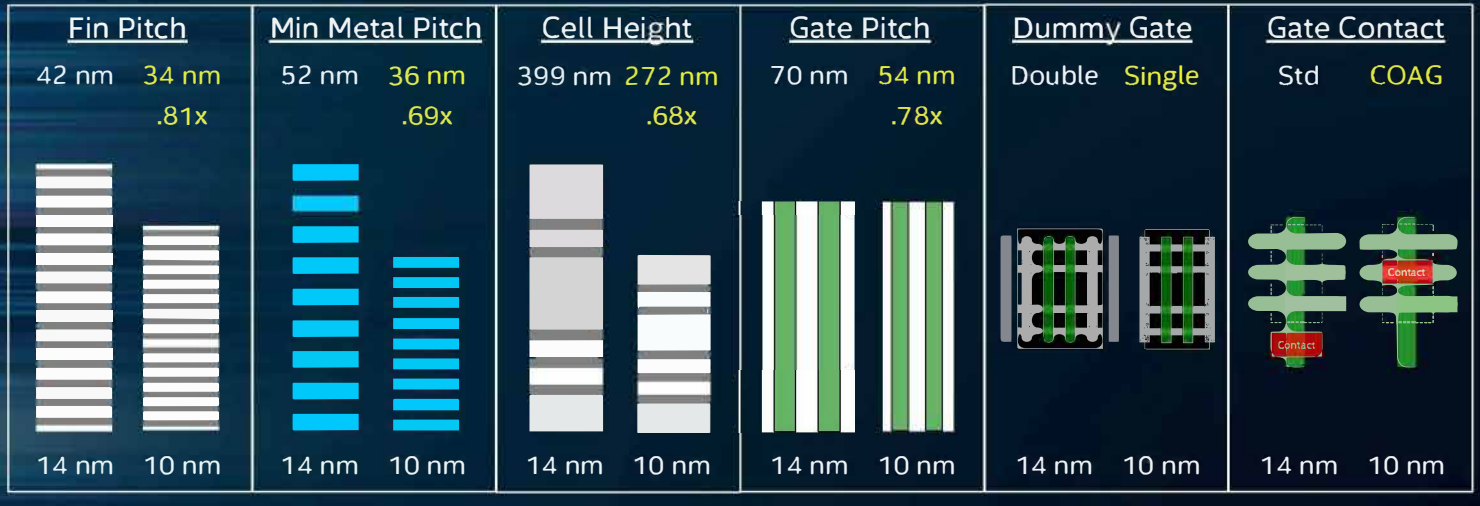


10 nm features aggressive pitch scaling - world's first Self-Aligned Quad Patterning

TECHNOLOGY AND MANUFACTURING DAY

Source: Intel

10 NM HYPER SCALING

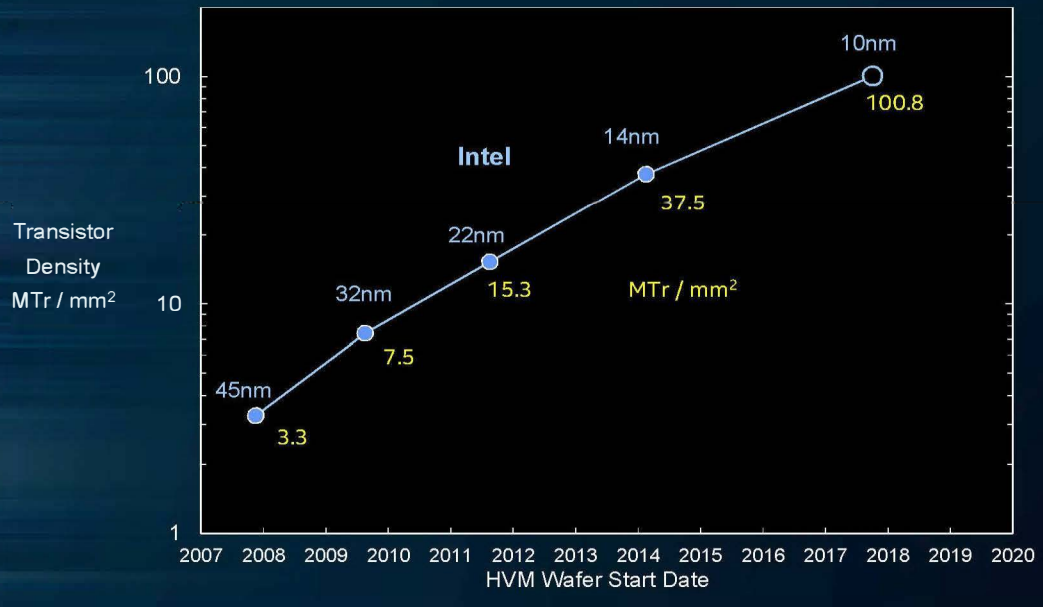


10 nm aggressive scaling & new features deliver 2.7x transistor density improvement

TECHNOLOGY AND MANUFACTURING DAY

Source: Intel

LOGIC TRANSISTOR DENSITY

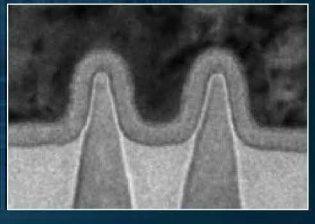


Intel 10 nm hyper scaling features result in Transistor Density above 100MTr/mm²

Source: Intel. 2017-2020 are estimates based upon current expectations and available information.

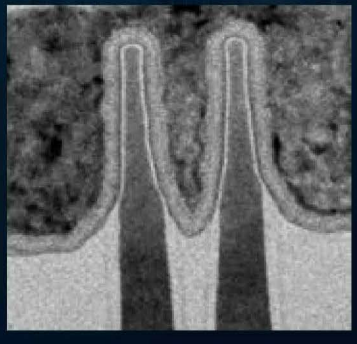
3RD GENERATION FINFETS

22 NM



14 NM

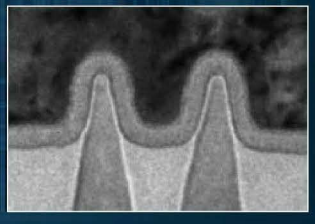
10 NM



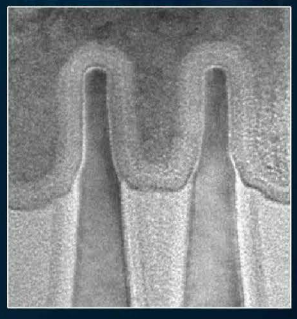
10 nm Fins are ~25% taller and ~25% more closely spaced than 14 nm

3RD GENERATION FINFETS

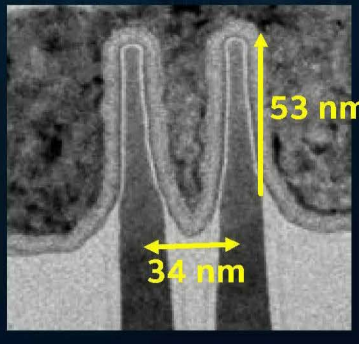
22 NM



14 NM

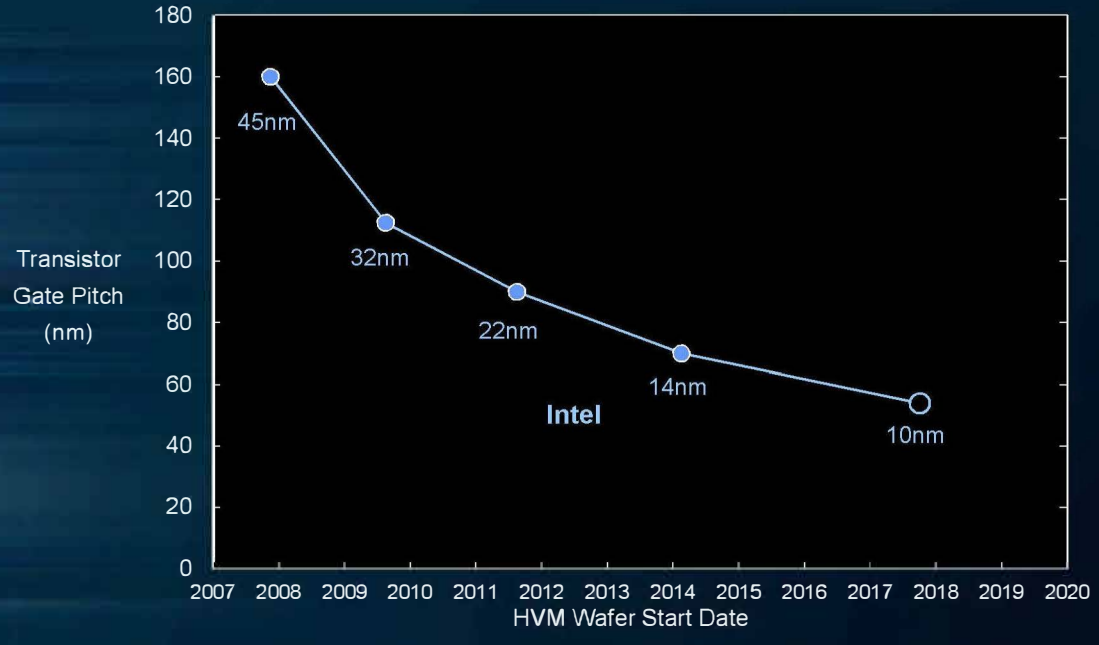


10 NM



Intel's 10 nm technology features a Fin Pitch of 34 nm, Fin Height of 53 nm

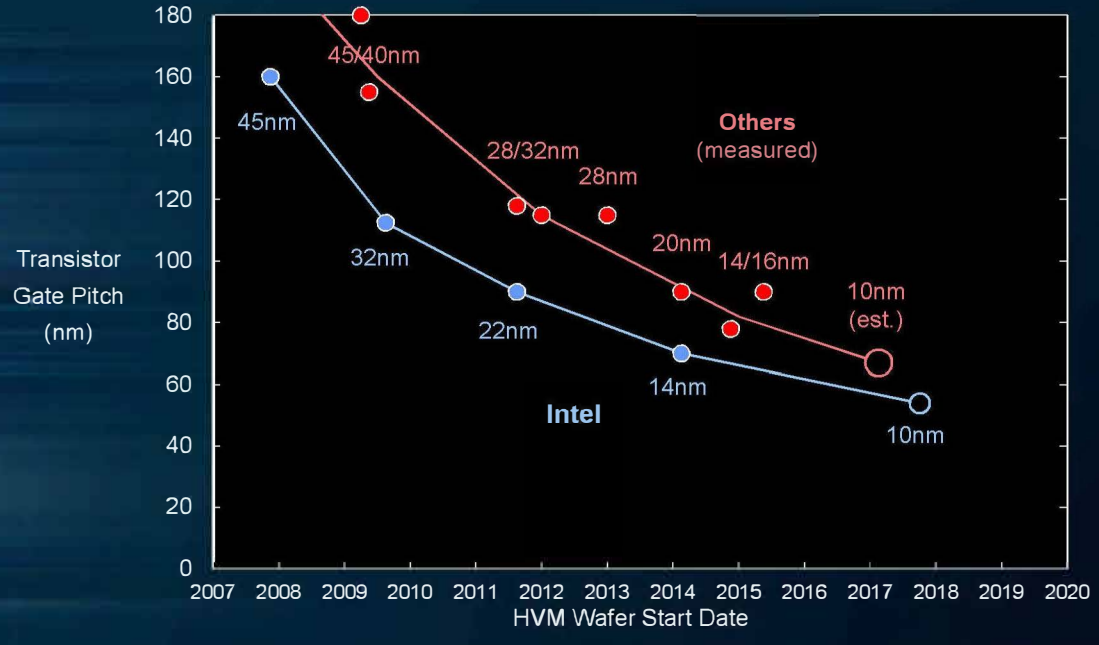
TRANSISTOR GATE PITCH SCALING



Intel's 10 nm technology features 54 nm gate pitch

Source: Intel. 2017-2020 are estimates based upon current expectations and available information.

TRANSISTOR GATE PITCH TREND

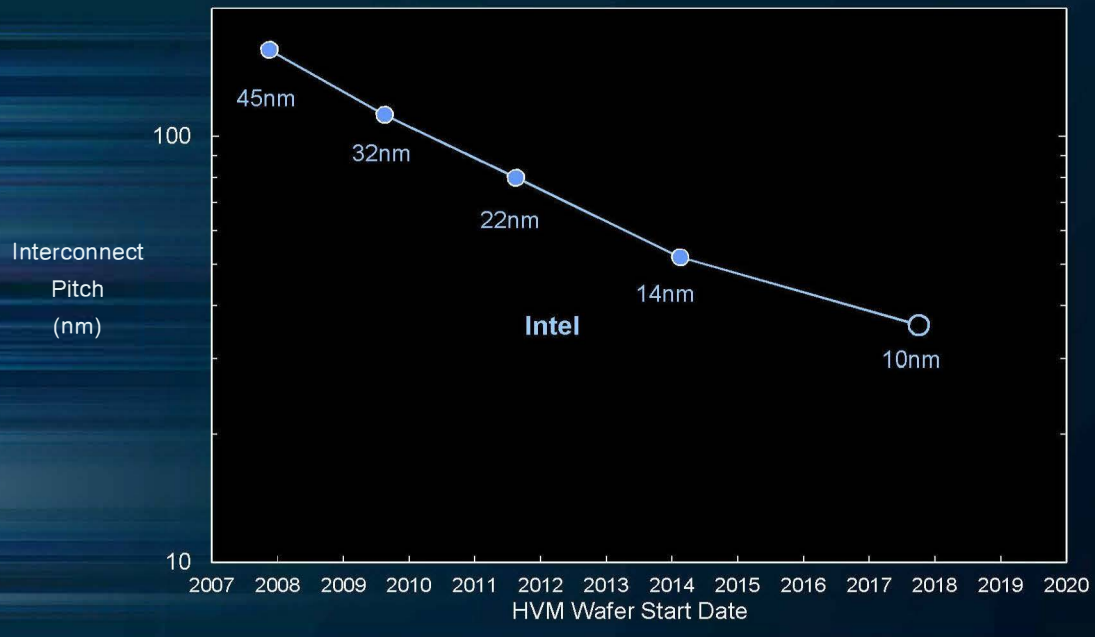


Intel 10 nm Gate Pitch is the tightest in the industry

TECHNOLOGY AND MANUFACTURING DAY

Source: Amalgamation of analyst data and Intel analysis. 2017-2020 are estimates based upon current expectations and available information.

METAL PITCH SCALING



Intel 10 nm technology features a minimum metal pitch of 36 nm
World's first Self-Aligned Quad Patterning

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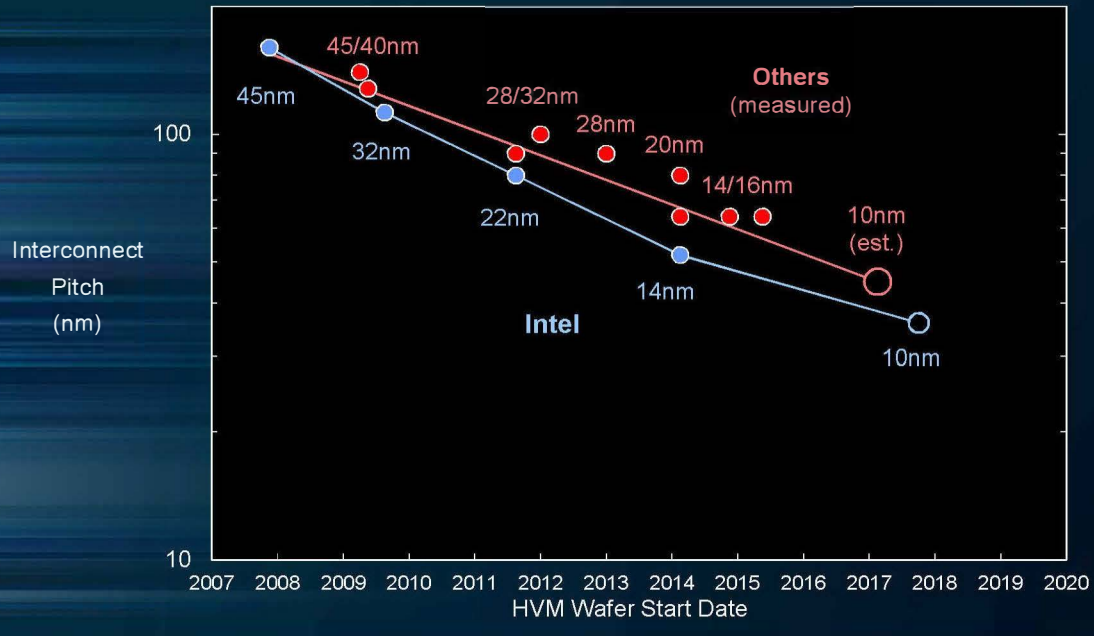
Source: Intel. 2017-2020 are estimates based upon current expectations and available information.

METAL PITCH SCALING TREND



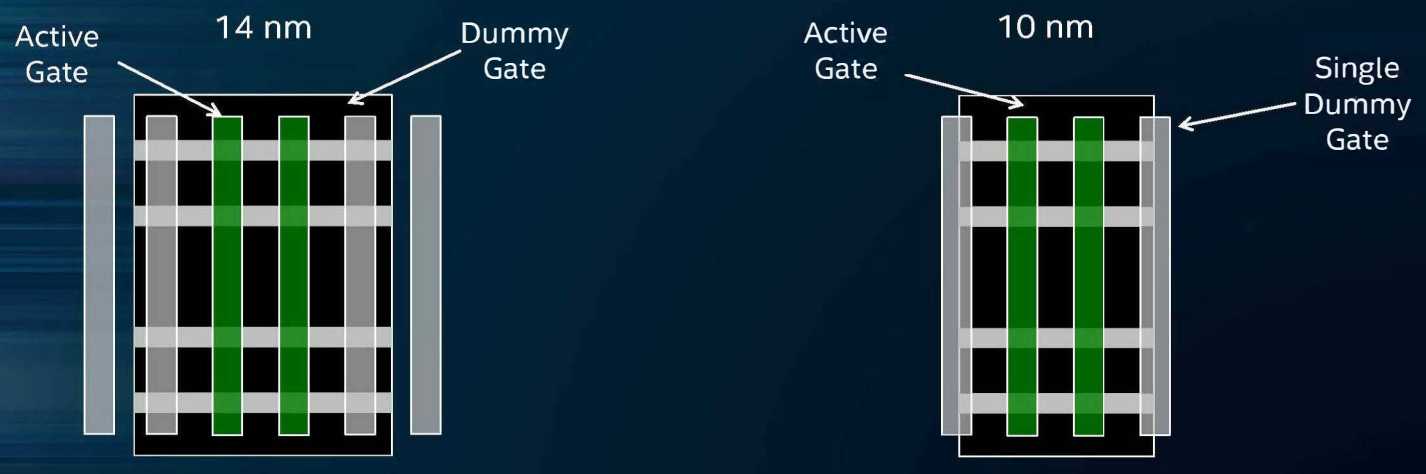
Intel 10 nm technology has the tightest minimum metal pitch in the industry

Source: Intel. 2017-2020 are estimates based upon current expectations and available information.

CONTACT OVER ACTIVE GATE

Contact over active gate is a revolutionary feature for another ~10% area scaling

SINGLE DUMMY GATE

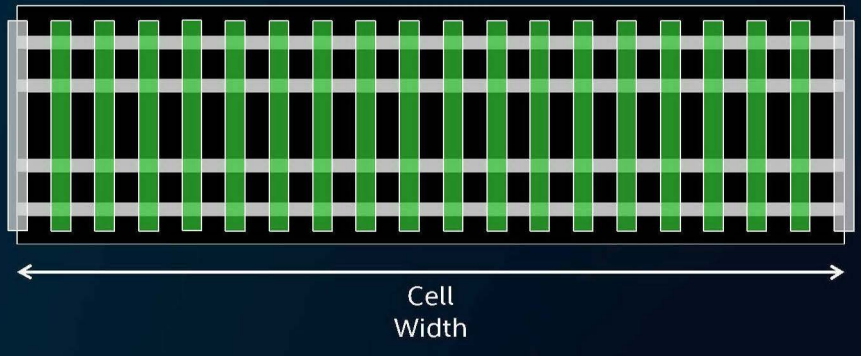


Process innovations enable denser single dummy gate at cell borders

SINGLE DUMMY GATE

2-Input NAND Cell

Complex Scan Flip-Flop Logic Cell



Single dummy gate at cell borders provides ~20% effective area scaling benefit

AGENDA

- Intel 10 nm Features
- Intel 10 nm Hyper Scaling
- Enhanced Versions of Intel 10 nm
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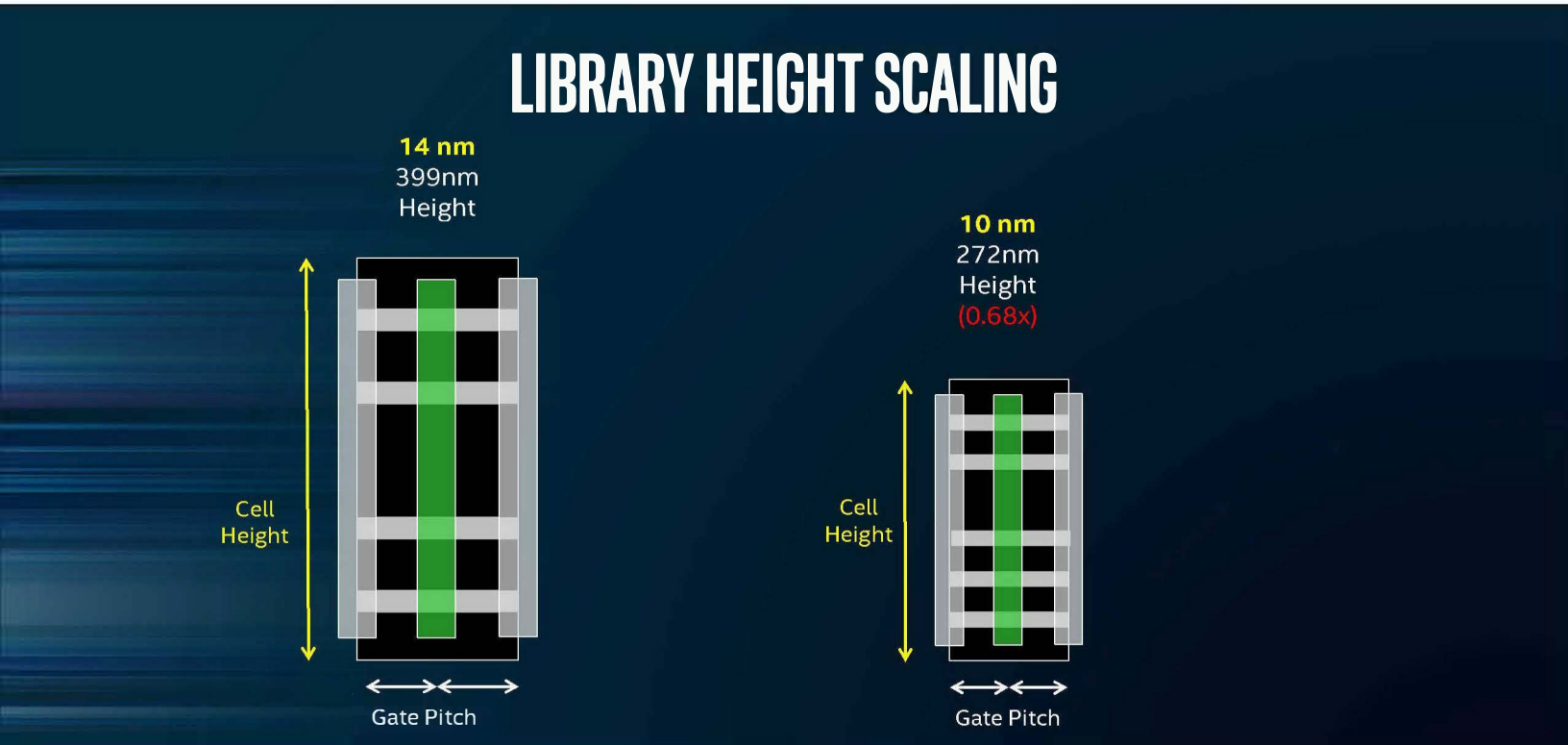
LIBRARY HEIGHT SCALING

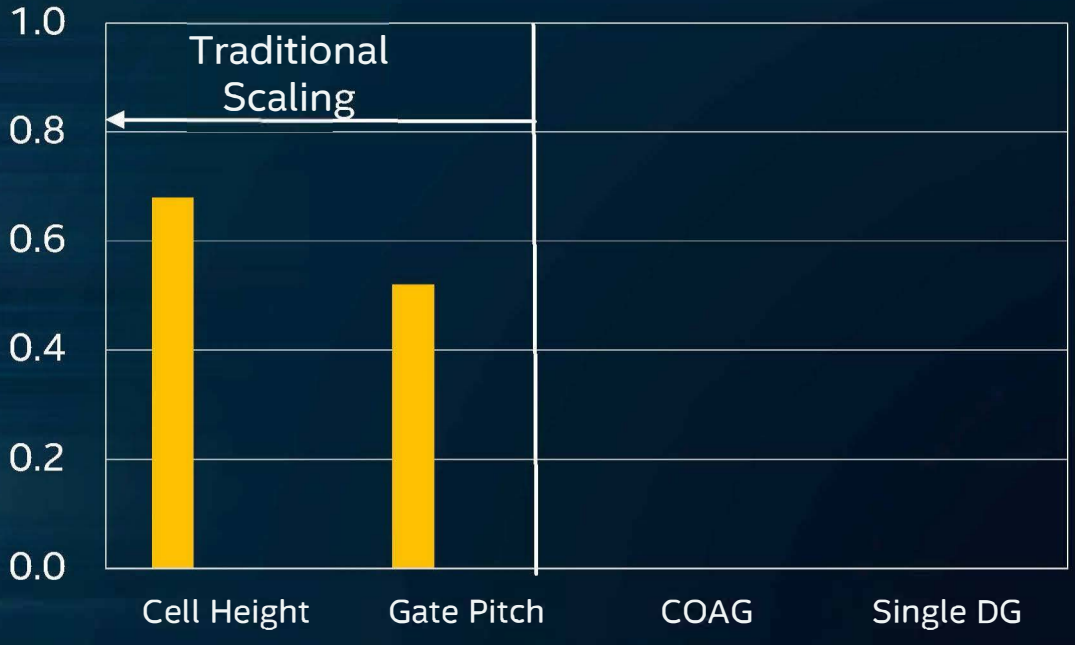


Fin pitch and metal pitch scaling allow cell height to scale 0.68x from 14 nm

TECHNOLOGY AND MANUFACTURING DAY

Source: Intel

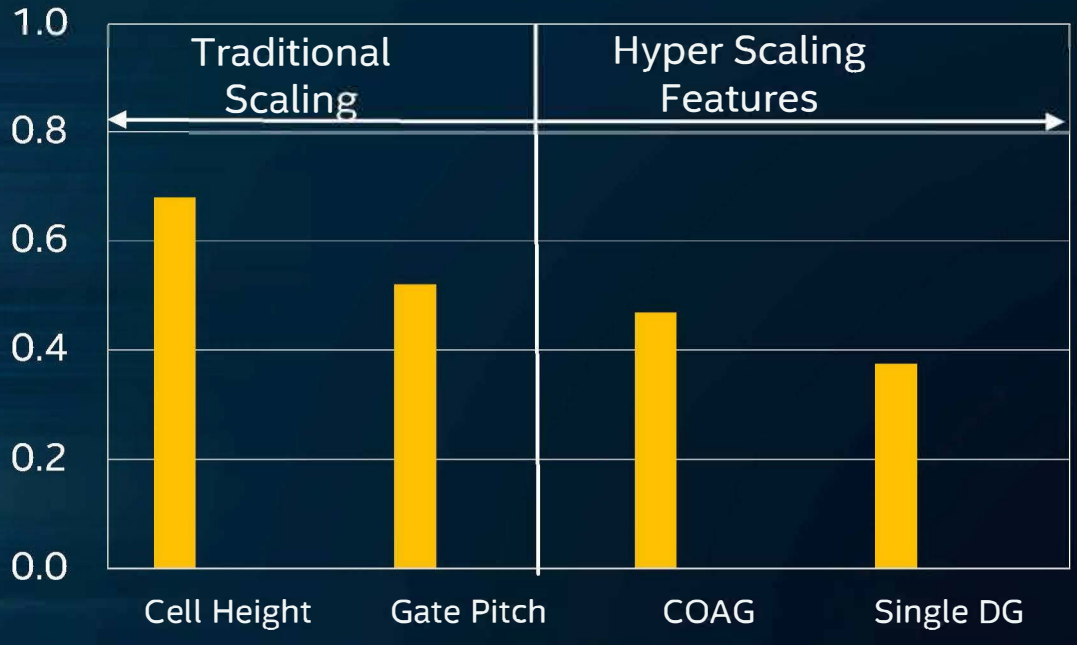
INTEL 10 NM LOGIC DENSITY SCALING



Cell height and gate pitch scaling provides traditional area reduction of ~0.5x

Source: Intel

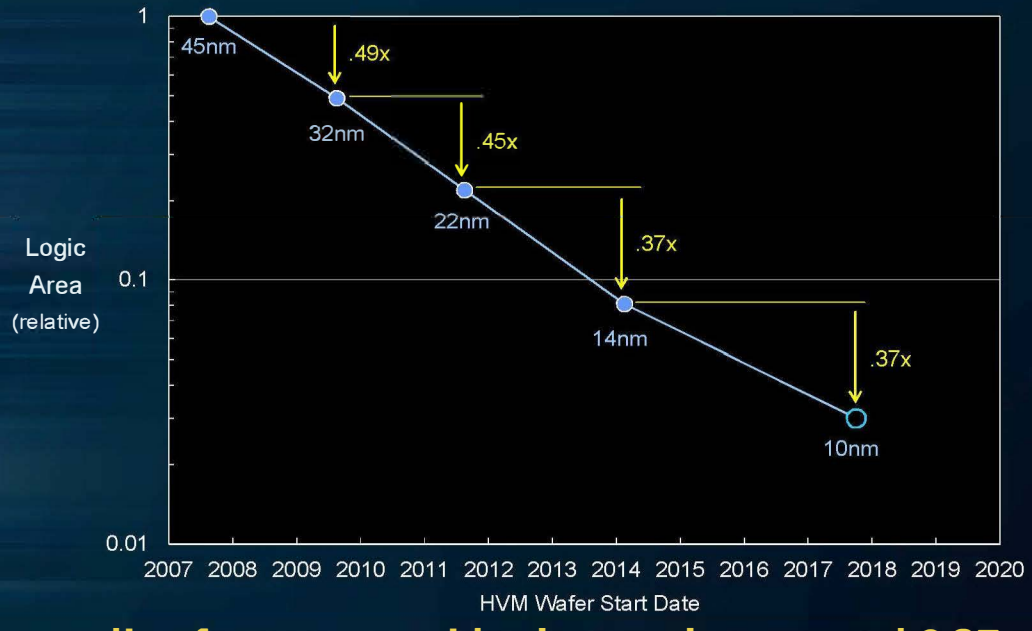
INTEL 10 NM LOGIC DENSITY SCALING



Intel 10 nm hyper scaling features further improve area scaling to 0.37x

Source: Intel

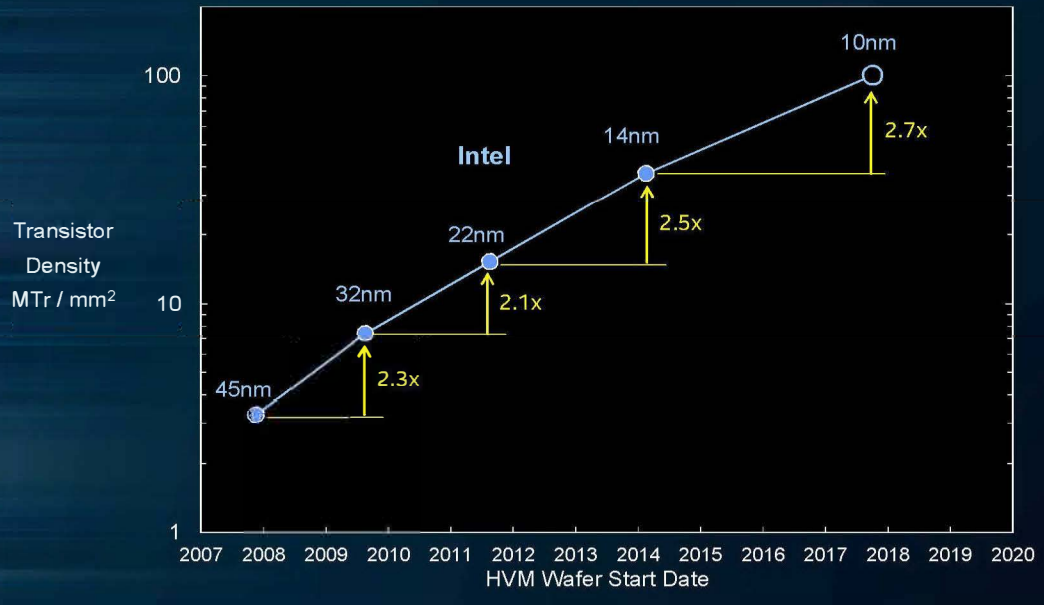
LOGIC AREA SCALING



10 nm hyper scaling features provides better-than-normal 0.37x logic area scaling

Source: Intel. 2017-2020 are estimates based upon current expectations and available information.

LOGIC TRANSISTOR DENSITY

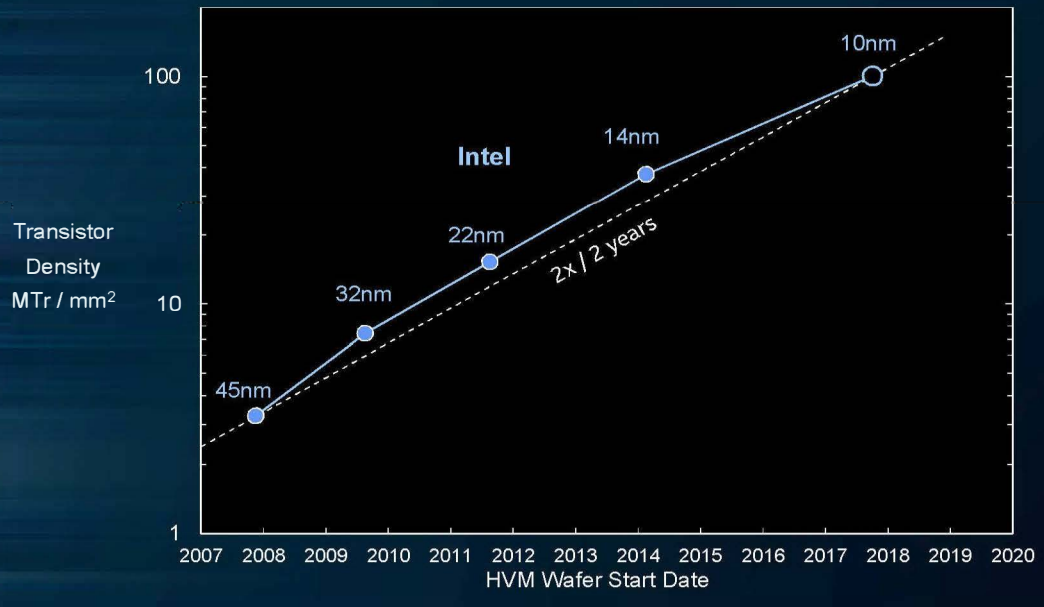


Intel 10 nm hyper scaling features provide ~2.7x transistor density improvement

TECHNOLOGY AND MANUFACTURING DAY

Source: Intel. 2017-2020 are estimates based upon current expectations and available information

LOGIC TRANSISTOR DENSITY

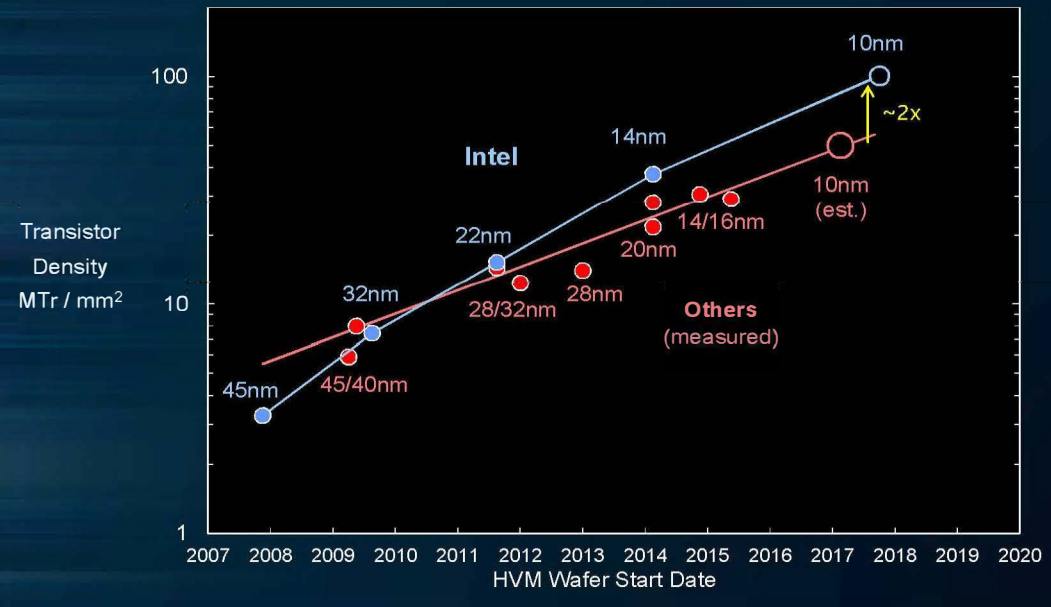


Hyper scaling maintains the rate of Moore's Law density scaling

TECHNOLOGY AND MANUFACTURING DAY

Source: Intel. 2017-2020 are estimates based upon current expectations and available information.

LOGIC TRANSISTOR DENSITY

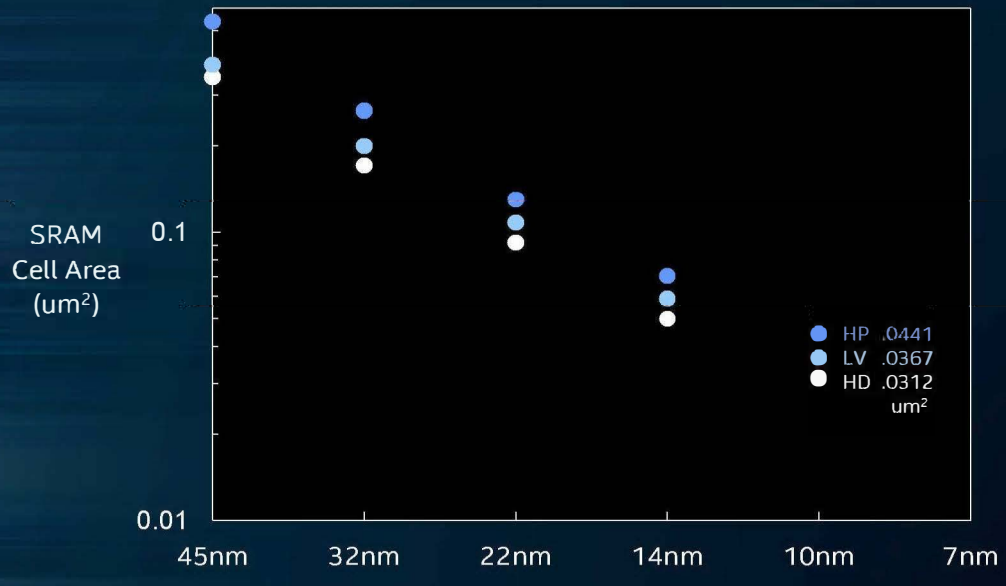


Intel 10 nm is a full generation ahead of other "10 nm" technologies

TECHNOLOGY AND MANUFACTURING DAY

Source: Amalgamation of analyst data and Intel analysis. 2017-2020 are estimates based upon current expectations and available information.

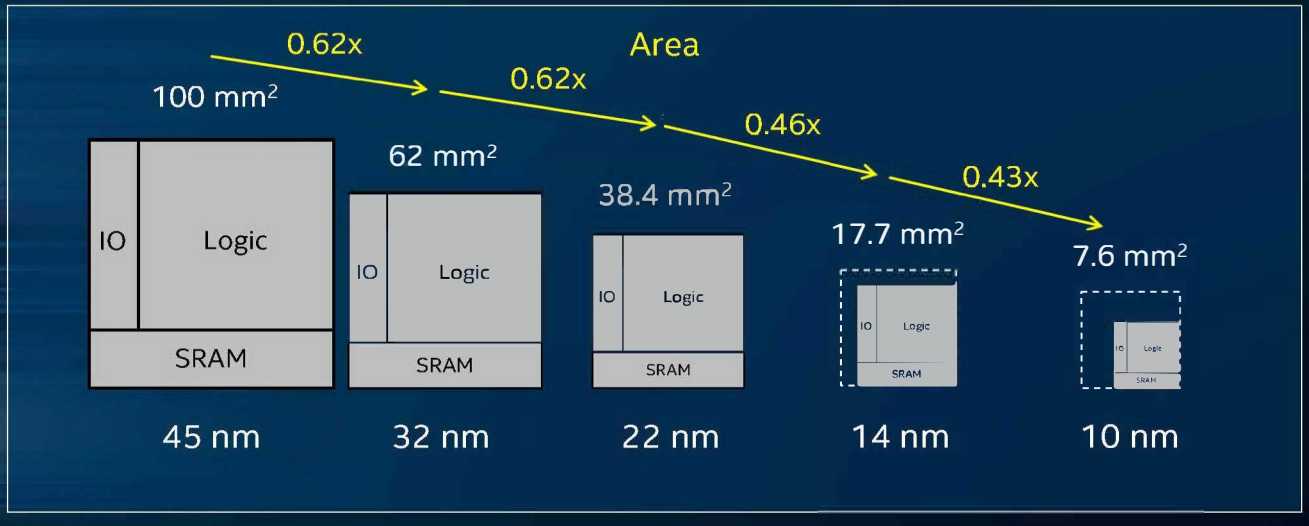
SRAM AREA SCALING



10 nm offers a range of SRAM cells for density and power/performance
SRAM cell area scaled ~0.6x from 14 nm

Source: Intel

MICROPROCESSOR DIE AREA SCALING



Hyper scaling delivers better microprocessor die area scaling than the normal trend

TECHNOLOGY AND MANUFACTURING DAY

Source: Intel

AGENDA

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- Enhanced Versions of Intel 10 nm
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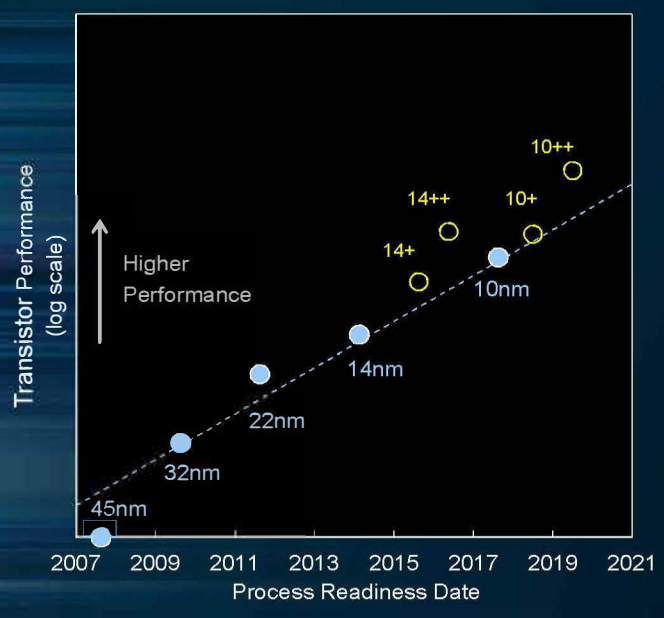
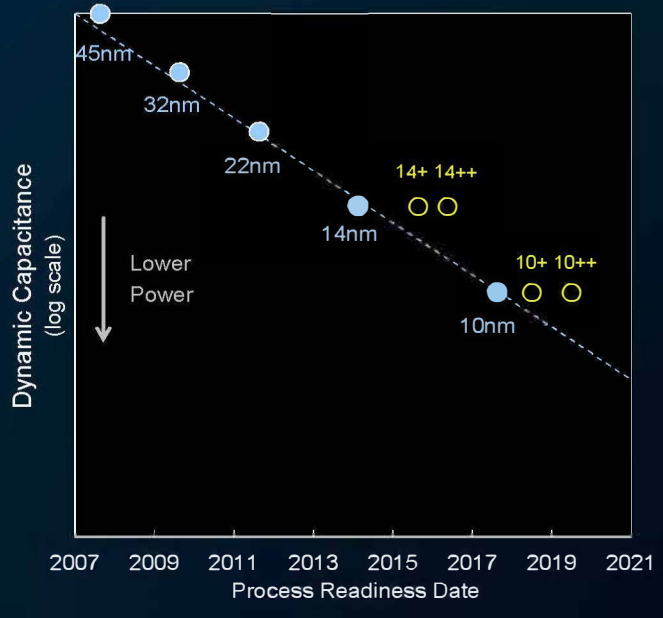
TECHNOLOGY ENHANCEMENTS

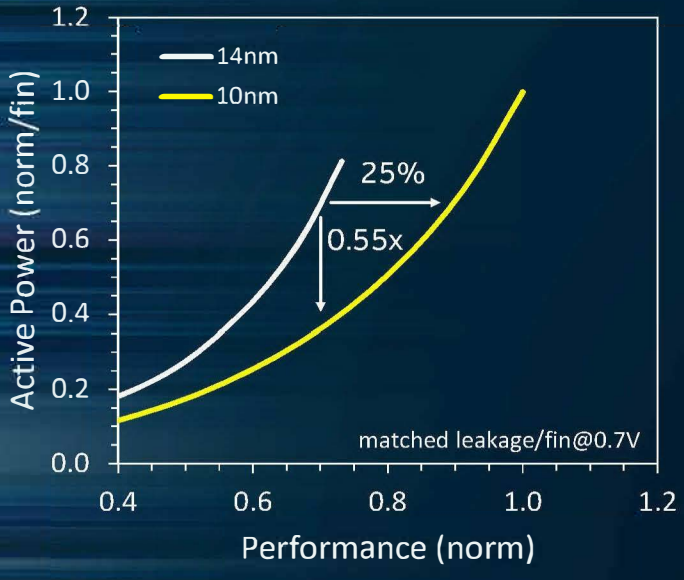




10 nm enhancements improve performance and extend technology life

Source: Intel. 2017-2021 are estimates based upon current expectations and available information.

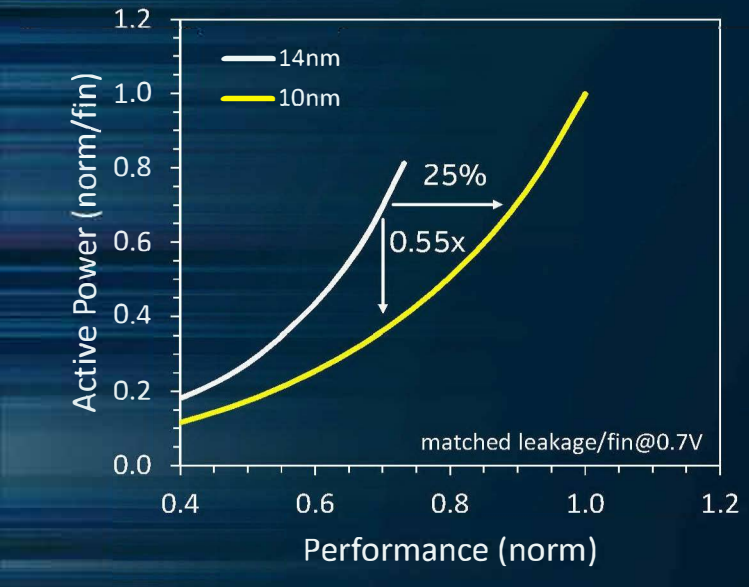
TECHNOLOGY ENHANCEMENTS

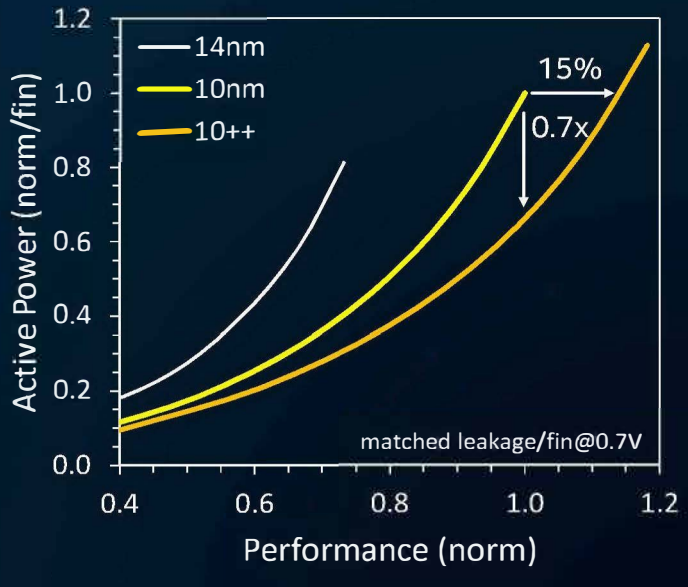


10 nm technology continues trend of power/performance improvements

Source: Intel estimates based upon current expectations and available information.

TECHNOLOGY ENHANCEMENTS

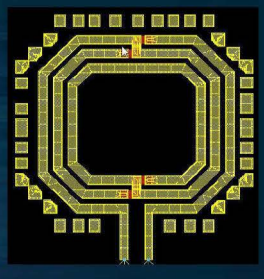




10++ enhancements offer improved power/performance within 10 nm generation

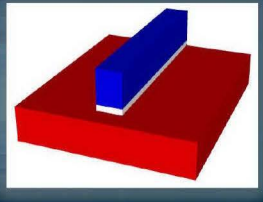
Source: Intel estimates based upon current expectations and available information.

TECHNOLOGY ENHANCEMENTS

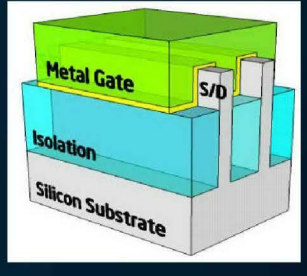


High Q Inductors

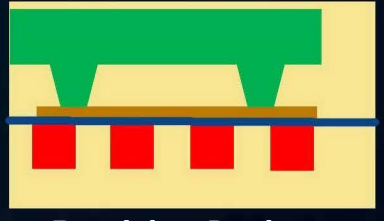
Interconnect Options



High Res Substrates



High Voltage FinFETs



Precision Resistors

Intel's 10 nm technology family has features for a broad range of products

Source: Intel

AGENDA

- Intel 10 nm Features
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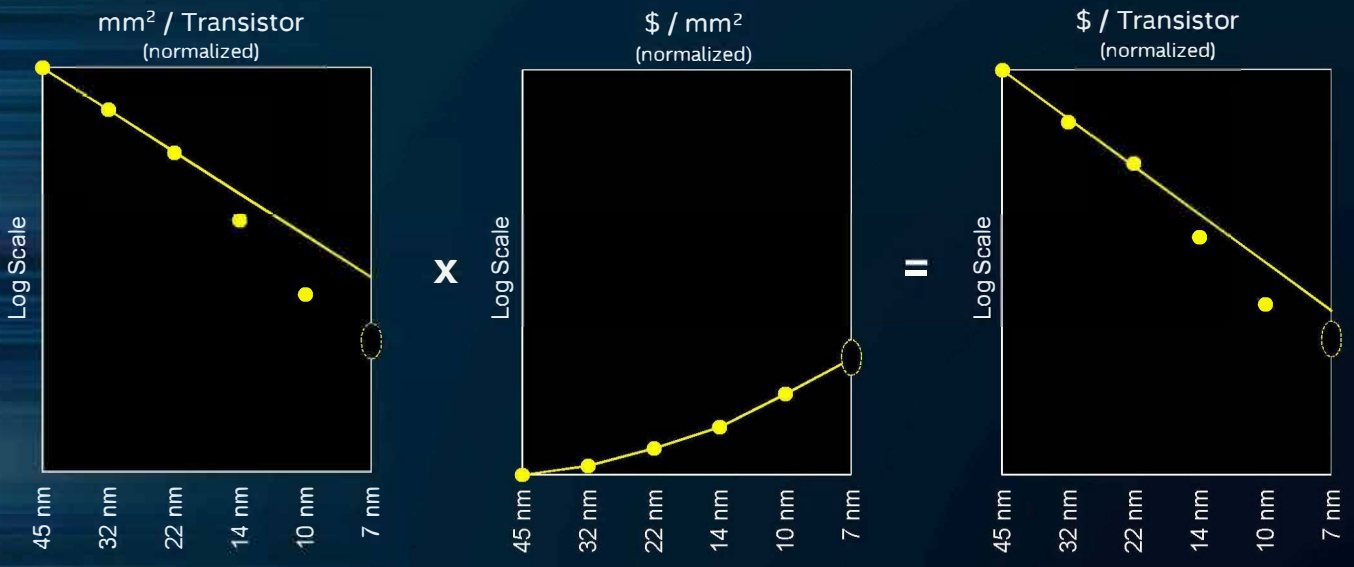
HYPER SCALING

- Hyper scaling allows Intel to continue the economics of Moore's Law
  - More than 2X logic transistor density increase but with longer than 2 year cadence
  - Same rate of transistor density increase as traditional Moore's Law scaling
  - Same rate of Cost per Transistor improvement as traditional Moore's Law scaling
  - Power/performance enhancements within each process node

- Why hyper scaling?
  - Multi-pass patterning adds to the cost of lithography
  - Hyper scaling extracts the full cost per transistor benefit of advanced patterning schemes

- Hyper scaling would not be possible without Self-Aligned Dual and Self-Aligned Quad Patterning along with other 10 nm hyper scaling innovations

COST PER TRANSISTOR



Hyper scaling allows the economics of Moore's Law to continue

Source: Intel estimates based upon current expectations and available information.

CONCLUSIONS

- Intel's 10 nm process technology has the world's tightest transistor & metal pitches along with hyper scaling features for leadership density
- Intel's 10 nm technology is a full generation ahead of other "10 nm" technologies
- Enhanced versions of Intel 10 nm provide improved power/performance within the 10 nm process family
- Intel's 10nm process technology is on track to commence manufacturing in 2H'17
- Hyper scaling extracts the full value of multi-patterning schemes and allows Intel to continue the economic benefits of Moore's Law

Source: Amalgamation of analyst data and Intel analysis, based upon current expectations and available information.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LEADING AT THE EDGE
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