UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SEMICONDUCTOR COMPONENTS INDUSTRIES, LLC d/b/a
ON SEMICONDUCTOR
Petitioner

v.

POWER INTEGRATIONS, INC.
Patent Owner

Case No. Unassigned
Patent 8,773,871

DECLARATION OF R. JACOB BAKER, P.H.D., P.E.

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Declaration of R. Jacob Baker, Ph.D., P.E.

I, R. Jacob Baker, declare as follows:

1. I make this declaration based upon my own personal knowledge and, if called upon to testify, would testify competently to the matters contained herein.

2. I have been asked to provide technical assistance in the *inter partes* review of U.S. Patent No. 8,733,871 ("the '871 Patent").

3. This declaration is a statement of my opinions on issues related to the unpatentability of claims 1-3, 6, 8, 11, 12, 14, and 15 of the '871 Patent.

I. Background and Qualifications

4. In formulating my opinions, I have relied upon my knowledge, training, and experience in the relevant art. My qualifications are stated more fully in my curriculum vitae. Ex. 1003. Here I provide a brief summary of my qualifications.

5. I have been teaching Electrical Engineering for 27 years. From 1991-1992, I was an adjunct faculty member in the Electrical Engineering department of the University of Nevada, Las Vegas ("UNLV"). From 1993 to 2000, I served on the faculty at the University of Idaho as an Assistant Professor and then as an Associate Professor of Electrical Engineering. In 2000, I joined a new Electrical and Computer Engineering program at Boise State University ("BSU") where I served as department chair from 2004 to 2007. At BSU, I helped establish graduate

programs in Electrical and Computer Engineering including, in 2006, the university's second Ph.D. degree. In 2012, I re-joined the faculty at UNLV where I am currently a Professor of Electrical and Computer Engineering. Over the course of my career as a professor, I have advised over 75 graduate students.

6. I have been recognized for my contributions as an educator in the field. While at Boise State University, I received the President's Research and Scholarship Award (2005), Honored Faculty Member recognition (2003), and Outstanding Department of Electrical Engineering Faculty recognition (2001). In 2007, I received the Frederick Emmons Terman Award (the "Father of Silicon Valley"). The Terman Award is bestowed annually upon an outstanding young electrical/computer engineering educator in recognition of the educator's contributions to the profession. In 2011, I received the IEEE Circuits and Systems Education Award. I have also received the Tau Beta Pi Outstanding Electrical and Computer Engineering Professor Award while at UNLV.

7. I received a B.S. degree and a M.S. degree in electrical engineering from the University of Nevada, Las Vegas ("UNLV") in 1986 and 1988, respectively. I received my Ph.D. in Electrical Engineering from the University of Nevada, Reno, in 1993.

8. My doctoral research, culminating in the award of a Ph.D. in Electrical Engineering in 1993, investigated the use of power MOSFETs (metal

oxide semiconductor field effect transistors) in the design of very high peak power, and high-speed, instrumentation. I developed techniques to reliably stack power MOSFETs to switch higher voltages, that is, greater than 1,000 V and near 100 Amps of current with nanosecond switching times. This work was reported in the paper entitled "Transformerless Capacitive Coupling of Gate Signals for Series Operation of Power MOSFET Devices," published in the IEEE Transactions on Power Electronics. The paper received the 2000 Best Paper Award from the Power Electronics Society. In addition, I have published several other papers in this area, and hold a patent, Patent No. 5,874,830, in the area of power supply design, titled, "Adaptively biased voltage regulator and operating method," which was issued on February 23, 1999. Further, I have designed dozens of linear and switching power supplies for commercial products and scientific instrumentation.

9. I am a licensed Professional Engineer and have extensive industry experience, including extensive experience in circuit design and manufacture of power supplies and circuitry related to the control of power supplies.

10. From 1985 to 1993, I worked for EG&G Energy Measurements and the Lawrence Livermore National Laboratory designing nuclear diagnostic instrumentation for underground weapon tests at the Nevada test site. During this time, I designed and oversaw the fabrication of over 30 electronic and electro-optic instruments including high-speed cable and fiber-optic receiver/transmitters, PLLs,

frame and bit-syncs, data converters, streak-camera sweep circuits, Pockel's cell drivers, micro-channel plate gating circuits, and analog oscilloscope electronics.

11. I also have more extensive experience doing research and development in the area of electrical instrumentation in a multitude of areas including diagnostic electrical and electro-optic instrumentation for scientific research; integrated electrical/biological circuits and systems, array (memory, imagers, and displays) circuit design; CMOS analog and digital circuit design; CAD tool development and online tutorials; low-power interconnect and packaging techniques; design of communication/interface circuits; circuit design for the use and storage of renewable energy; and power electronics.

12. I have also performed technical and expert witness consulting for over 100 companies and laboratories. I have worked as a consultant at companies designing memory chips and modules, including Sun Microsystems, Oracle Corporation, Micron Technology, and Contour Semiconductor. I have worked at companies designing CISs, including Aerius Photonics, Lockheed Martin, Freedom Photonics, Aptina, and OmniVision Technologies.

13. I have given more than 50 invited talks at conferences, companies, and Universities in the areas of integrated circuit design, including: AMD; Arizona State University; Beijing Jiaotong University; Carleton University; Carnegie Mellon; Columbia University; Dublin City University (Ireland); École

Polytechnique de Montréal; Georgia Tech; Gonzaga University; Hong Kong University of Science and Technology; Indian Institute of Science (Bangalore, India); Instituto de Informatica (Brazil); Instituto Tecnológico y de Estudios Superiores de Monterrey; ITESM (Mexico); Iowa State University; Laval University; Lehigh University; Princeton University; Temple University; University of Alabama; University of Arkansas; University of Buenos Aires (Argentina); University of Illinois, Urbana-Champaign; Utah State University; University of Nevada, Las Vegas; University of Houston; University of Idaho; University of Nevada, Reno; University of Macau; University of Toronto; University of Utah; Yonsei University (Seoul, Korea); University of Maryland; IEEE Electron Devices Conference (NVMTS); IEEE Workshop on Microelectronics and Electron Devices (WMED); the Franklin Institute; National Semiconductor; AMI semiconductor; Micron Technology; Rendition; Saintgits College (Kerala, India); Southern Methodist University; Sun Microsystems; Stanford University; ST Microelectronics (Delhi, India); Tower (Israel); Foveon; ICySSS keynote; and Xilinx Publications and Patents.

14. I have authored several books and papers in the electrical and computer engineering area. My published books include CMOS Circuit Design, Layout, and Simulation (Baker, R.J., Wiley-IEEE, ISBN: 978-0470881323 (3rd ed., 2010)) and CMOS Mixed-Signal Circuit Design (Baker, R.J., Wiley-IEEE,

ISBN: 978-0470290262 (2nd ed., 2009) and ISBN: 978-0471227540 (1st ed., 2002)). I have also co-authored DRAM Circuit Design: Fundamental and High-Speed Topics (Keeth, B., Baker, R.J., Johnson, B., and Lin, F., Wiley-IEEE, ISBN: 978-0-470-18475-2 (2008)), DRAM Circuit Design: A Tutorial (Keeth, B. and Baker, R.J., Wiley-IEEE, ISBN: 0-7803-6014-1 (2001)), and CMOS Circuit Design, Layout and Simulation (Baker, R.J., Li, H.W., and Boyce, D.E., Wiley-IEEE, ISBN: 978-0780334168 (1998)). I have also contributed as an editor and co-author on several other books on CMOS circuit design and VLSI.

15. I am the author and co-author of more than 100 papers and presentations in the areas of electrical and computer engineering design, fabrication and packaging.

16. I am a named inventor on 148 U.S. patents in integrated circuit design including Flash memory, DRAM, and CMOS image sensors.

17. I currently serve, or have served, on: the IEEE Press Editorial Board (1999-2004); as editor for the Wiley-IEEE Press Book Series on Microelectronic Systems (2010-present); as the Technical Program Chair of the 2015 IEEE 58th International Midwest Symposium on Circuits and Systems (MWSCAS 2015); on the IEEE Solid-State Circuits Society (SSCS) Administrative Committee (2011-2016); as a Distinguished Lecturer for the SSCS (2012-2015); and as the Technology Editor (2012-2014) and Editor-in-Chief (2015-present) for the IEEE

Solid-State Circuits Magazine. These meetings, groups, and publications are intended to allow researchers to share and coordinate research. My active participation in these meetings, groups, and publications allowed me to see what other researchers in the field have been doing.

18. In addition to the above, I am an IEEE Fellow for contributions to memory circuit design and a member of the honor societies Eta Kappa Nu and Tau Beta Pi.

19. I am being compensated by ON Semiconductor at the rate of $615 per hour for my work in this case, including time spent testifying. This rate is my standard hourly rate for engagements of this nature. I am also being reimbursed for reasonable fees and expenses, including hotel and travel expenses, incurred as a result of my work in this case. My compensation does not depend on the outcome of the case, and the fact that I am being compensated has not altered the opinions that I have or will give in this case.

II. Legal Understanding

20. My opinions are also informed by my understanding of the relevant law. I understand that the patentability analysis is conducted on a claim-by-claim and element-by-element basis, and that there are several possible reasons that a patent claim may be found to be unpatentable.

21. I understand that earlier publications and patents may act to render a patent unpatentable for one of two reasons: (1) anticipation and (2) obviousness.

A. Anticipation

22. First, I understand that a single prior art reference, article, patent or publication "anticipates" a claim if each and every element of the claim is disclosed in that prior art reference. I further understand that, where a claim element is not explicitly disclosed in a prior art reference, the reference may nonetheless anticipate a claim if the missing claim element is necessarily present in the apparatus or a natural result of the method disclosed—i.e., the missing element is "inherent."

B. Obviousness

23. Second, I understand that the prior art may render a patent claim "obvious." I understand that two or more prior art references (e.g., prior art articles, patents, or publications) that each disclose fewer than all elements of a patent claim may nevertheless be combined to render a patent claim obvious if the combination of the prior art collectively discloses all elements of the claim and one of ordinary skill in the art at the time would have been motivated to combine the prior art in such a way. I understand that this motivation to combine need not be explicit in any of the prior art, but may be inferred from the knowledge of one of ordinary skill in the art at the time the patent was filed. I also understand that one

of ordinary skill in the art is not an automaton, but is a person having ordinary creativity. I further understand that one or more prior art references, articles, patents or publications that disclose fewer than all of the elements of a patent claim may render a patent claim obvious if including the missing element would have been obvious to one of skill in the art (e.g., the missing element represents only an insubstantial difference over the prior art or a reconfiguration of a known system).

24. Under the doctrine of obviousness, a claim may be invalid if the differences between the invention and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains.

25. I understand that obviousness is based on the scope and content of the prior art, the differences between the prior art and the claim, the level of ordinary skill in the art, and secondary indicia of obviousness and non-obviousness to the extent they exist.

26. I understand that any evidence of secondary indicia of non-obviousness should be considered when evaluating whether a claimed invention would have been obvious to one of ordinary skill at the time of invention. These secondary indicia of non-obviousness may include, for example:

- a long felt but unmet need in the prior art that was satisfied by the claimed invention;

- commercial success of processes claimed by the patent;
- unexpected results achieved by the invention;
- praise of the invention by others skilled in the art;
- the taking of licenses under the patent by others; and
- deliberate copying of the invention.

27. I understand that there must be a relationship between any such secondary indicia and the claimed invention.

28. It is also my understanding that there are additional considerations that may be used as further guidance as to when the above factors will result in a finding that a claim is obvious, including the following:

> the claimed invention is simply a combination of prior art elements according to known methods to yield predictable results;
>
> the claimed invention is a simple substitution of one known element for another to obtain predictable results;
>
> the claimed invention uses known techniques to improve similar devices or methods in the same way;
>
> the claimed invention applies a known technique to a known device or method that is ready for improvement to yield predictable results;
>
> the claimed invention would have been "obvious to try" choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;

there is known work in one field of endeavor that may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations would have been predictable to one of ordinary skill in the art;

there existed at the time of invention a known problem for which there was an obvious solution encompassed by the patent's claims; and

there is some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

29. Finally, I understand that a claim may be deemed invalid for obviousness in light of a single prior art reference, without the need to combine references, if the elements of the claim that are not found in the reference can be supplied by the knowledge or common sense of one of ordinary skill in the relevant art.

C. Level of Ordinary Skill in the Art

30. I understand that the person having ordinary skill in the art ("POSITA") is a hypothetical person who is presumed to know the relevant prior art. I understand that the actual inventor's skill is not determinative of the level of ordinary skill. I further understand that factors that may be considered in determining level of skill include: type of problems encountered in art; prior art solutions to those problems; rapidity with which innovations are made; sophistication of the technology; and educational level of active workers in the field. I understand that not all such factors may be present in every case, and one or

more of them may predominate. In a given case, every factor may not be present, and one or more factors may predominate.

31. A POSITA at the time of invention of the ’871 Patent would have an M.S. in Electrical Engineering or related field or a B.S. with at least two years of experience in designing power electronics. At the time of invention, I was familiar with this level of skill because at the time of the ’871 Patent, I taught post-graduate engineering students at Boise State University with this level of skill.

III. Overview of the ’871 Patent

32. I have reviewed the ’871 Patent, which is entitled “Method and Apparatus for Sensing Multiple Voltage Values From a Single Terminal of a Power Converter Controller.” Ex. 1001. I understand the ’871 Patent was filed on February 26, 2013 and issued on July 8, 2014. *Id.* I understand that the ’871 Patent claims a priority date based on Provisional Application No. 60/922,133, filed on April 6, 2007. *Id.*

A. Background of the Technology

33. The ’871 Patent relates to switching power converters. Ex. 1001, Abstract. Such devices convert a first voltage (e.g., from a wall socket) to a second voltage to power an electronic device. *Id.*, 1:28-38. The ’871 Patent describes and claims a class of switching power converters that use the auxiliary winding of a transformer to detect information relevant to the control of the converter. But, as

described by the background materials below, use of an auxiliary winding in switching power converters was well-known prior to the '871 Patent. In the paragraphs below, I will describe the basic operation of a flyback-type switching power converter, as well as the characteristics of an auxiliary winding in an flyback-type switching power converter.

34. One example in the prior art of a switching power converter that uses an auxiliary winding is the flyback-type power converter disclosed by U.S. Patent 7,016,204 to Ta-Yung Yang et al. ("Yang").[1] Ex. 1006.

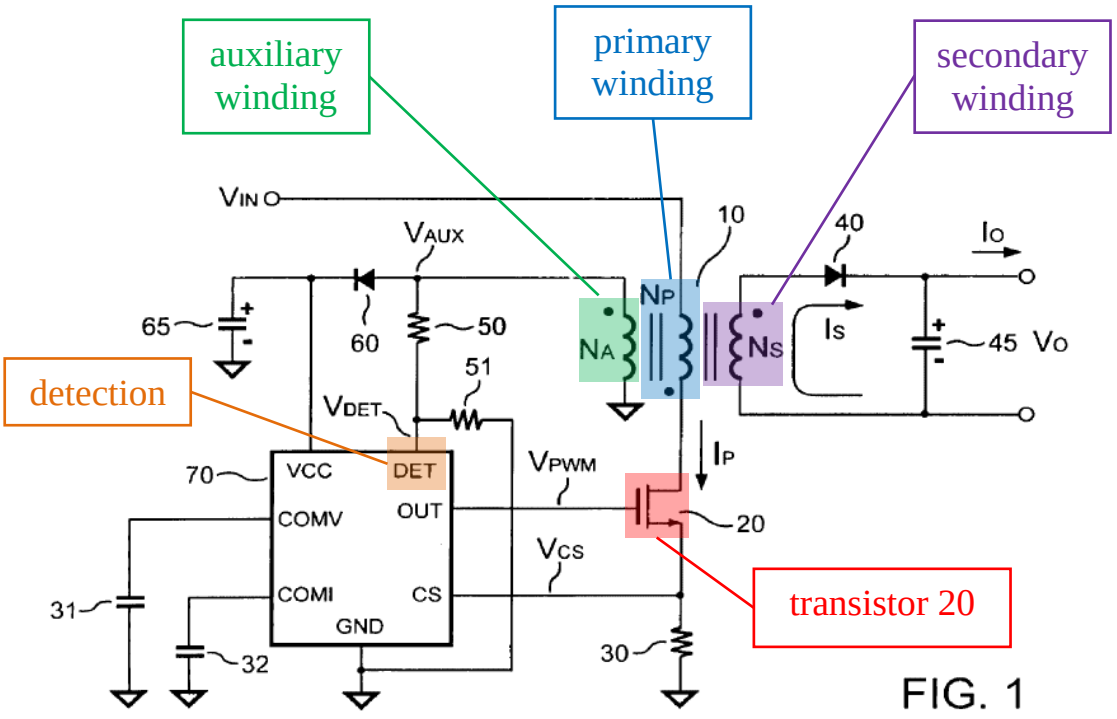


FIG. 1

Ex. 1006, Fig. 1 (annotations added).

[1] Yang was filed on August 12, 2004, and issued on March 21, 2006. Ex. 1006. Thus, I understand Yang to pre-date the claimed priority date of the '871 Patent.

35. I will first explain how energy is transferred from the input to the output of the converter via the first and second windings of the converter, and then later how the auxiliary winding responds to the activity at the first and second windings.

36. Yang's power converter includes transistor 20 coupled to transformer 10. Ex. 1006, Fig. 1. The transistor is turned on and off by a switching signal "V_{PWM}" to regulate how much energy is transferred from the input (V_{IN}) to the output (V_O) of the power converter. *Id.*, 2:34:40, Fig. 1. When V_{PWM} goes high to turn on transistor 20, a current (I_P) flows from V_{IN}, through the primary winding N_P of transformer 10, and through transistor 20 and resistor 30 to ground. *Id.*, 2:41-43, Figs. 1-2. As the primary-side current I_P flows, the magnetic energy stored in transformer 10 builds. Then, when V_{PWM} goes low to turn off transistor 20, the magnetic energy stored in transformer 10 induces a secondary-side current I_S through the secondary winding N_S. Ex. 1006, 2:54-59, Figs. 1-2. The magnetic energy stored in transformer 10 is therefore transferred to the output by the secondary-side current I_S. In sum, the magnetic energy in the transformer is built up via primary winding N_P during the on-time of transistor 20 and transferred to the output of the power converter via secondary winding N_S during the off-time of transistor 20.

37. As shown in Figure 1 of Yang, transformer 10 also includes auxiliary winding N_A, which is magnetically coupled to both primary winding N_P and secondary winding N_S. Because auxiliary winding N_A is magnetically coupled to the primary winding N_P and secondary winding N_S, auxiliary winding N_A "reflects" activity on the primary and secondary windings. For example, when the secondary-side current I_S flows in the secondary side during the off-time of the primary-side switch, the auxiliary winding reflects the voltage present at the secondary winding.[2] Ex. 1006, 3:4-15. This voltage at the secondary winding is equal to the output voltage (V_O) plus the forward voltage drop (V_F) of rectifier 40.

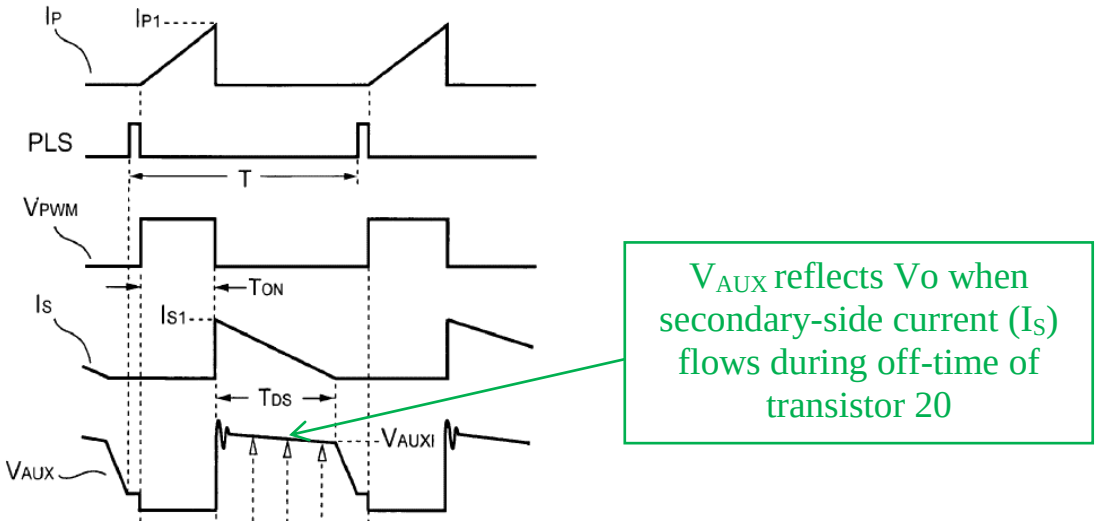
[2] The auxiliary winding reflects the voltage present at the secondary winding only during the portion of the off-time that current is flowing in the secondary side. *See* Ex. 1006, Fig. 2. For example, as shown in Figure 2, voltage of the auxiliary winding (V_{AUX}) reflects the voltage at the secondary winding during the portion of the off-time (i.e., when V_{PWM} is low) when the secondary side current (I_S) is above zero. *Id.* For the remainder of the off-time (i.e., when V_{PWM} is low and the secondary side current is zero), V_{AUX} does not reflect the voltage at the secondary winding. Thus, when discussing herein the auxiliary winding's reflection of the voltage during the off-time of the power switch, I am referring to the portion of the off-time during which current flows through the secondary winding, not the portion of the off-time where the secondary-side current is zero.

38. The reflection by the auxiliary winding of the voltage at the secondary winding is due to the magnetic coupling between the windings. The reflected voltage of the auxiliary winding will therefore account for the windings ratio between the secondary and auxiliary windings. Thus, as explained in Yang, the reflected voltage produced by the auxiliary winding equals the output voltage (V_O) plus the forward voltage drop (V_F) of rectifier 40, multiplied by the winding ratio of the auxiliary and secondary windings:

$$V_{AUX} = \frac{T_{NA}}{T_{NS}} \times (V_O + V_F)$$

Ex. 1006, 3:10 (Equation 3).

39. Figure 2 of Yang illustrates this reflected voltage (V_{AUX}) produced on the auxiliary winding when the secondary-side current (I_S) flows:



Ex. 1006, Fig. 2 (excerpt) (annotations added).

40. The auxiliary winding's reflected voltage can be used for multiple purposes. As shown in Figure 1 of Yang, V_{AUX} charges capacitor 65 via rectifier 60 to supply power for the internal circuitry of controller 70. Ex. 1006, 3:51-52, Fig. 1. In addition, V_{AUX} feeds information regarding output voltage V_O back to controller 70 via the DET pin. *See id.*, 3:36-50, 4:5-8. In turn, controller 70 uses the feedback information to determine the pulse width of switching signal V_{PWM}, thereby controlling the flow of energy from the input V_{IN} to the output V_O of the converter. *See id.*, 4:5-38.

41. Prior to the claimed priority date of the '871 Patent, it was well known in the art that different types of functions could be performed based on the reflected voltage present at the auxiliary winding of a flyback-type switching converter. As described directly above for Yang, it was known that the reflection of the output voltage on the auxiliary winding could be used as feedback for controlling the output voltage. Ex. 1006, 3:4-50, 4:5-8. And as described directly below, it was also widely recognized that the reflection of the output voltage on the auxiliary winding could be used to detect various fault conditions at the output of the power converter.

42. Examples of fault conditions at the output of a switching power converter include output over voltage fault conditions and output short circuit fault conditions. An output over voltage fault condition is a condition whereby the

output voltage rises to an overly high level that may damage either components of the power supply itself, or other electrical devices connected to the output of the power supply. Another fault condition is an output short circuit condition, whereby the output is shorted, for example, to ground. Both of these fault conditions may be detected by monitoring the output voltage itself. And as recognized in the prior art, such output voltage information could be obtained by sensing a voltage on the auxiliary winding during the off-time of the switch that represents the output voltage.

43. For example, U.S. Patent 6,061,257[3] ("Spampinato") uses the reflection of the output voltage on the auxiliary winding during the off-time of the power switch to detect an output short circuit condition. *See* Ex. 1015, 3:21-29, 5:47-57. When such a fault is detected, the fault detector disables switching to prevent damage to the power supply that would otherwise result from the short circuit condition. *Id.*, 5:47-57. Similarly, U.S. Patent 4,447,841[4] ("Kent") uses the output voltage information sensed via an auxiliary winding to recognize "a short circuit or an overload in an output circuit" of the power supply. Ex. 1016,

[3] Spampinato issued on May 9, 2000. Ex. 1015. Thus, I understand Spampinato to pre-date the claimed priority date of the '871 Patent.

[4] Kent issued on May 8, 1984. Ex. 1016. Thus, I understand Kent to pre-date the claimed priority date of the '871 Patent.

Abstract, 3:15-51, Fig. 1. When such a fault condition is detected, switching is disabled to prevent damage to the power supply that would otherwise result from the short circuit condition. *Id.*, 3:39-44.

44. As another example, U.S. Patent Application Publication 2005/0254268 ("Reinhard")[5] uses the reflection of the output voltage on the auxiliary winding during the off-time of the power switch to detect an output over voltage condition. *See* Ex. 1007, 5:11-19. Reinhard includes an "over-voltage protection comparator" that was "supplied with the voltage that is induced at the auxiliary winding" of the switching power converter. *Id.*, 5:11-15, Fig. 1. "The OVP comparator 107 detects positive voltages above the control region, switches off the driver 106 for the duration of a gating time and thus prevents the occurring of over-voltages." *Id.*, 5:16-19.

B. Subject Matter of the '871 Patent

45. Figure 1 of the '871 Patent illustrates a flyback-type switching power converter:

[5] Reinhard was filed on February 11, 2005 and published on November 17, 2005. Ex. 1007. Thus, I understand Kent to pre-date the claimed priority date of the '871 Patent.

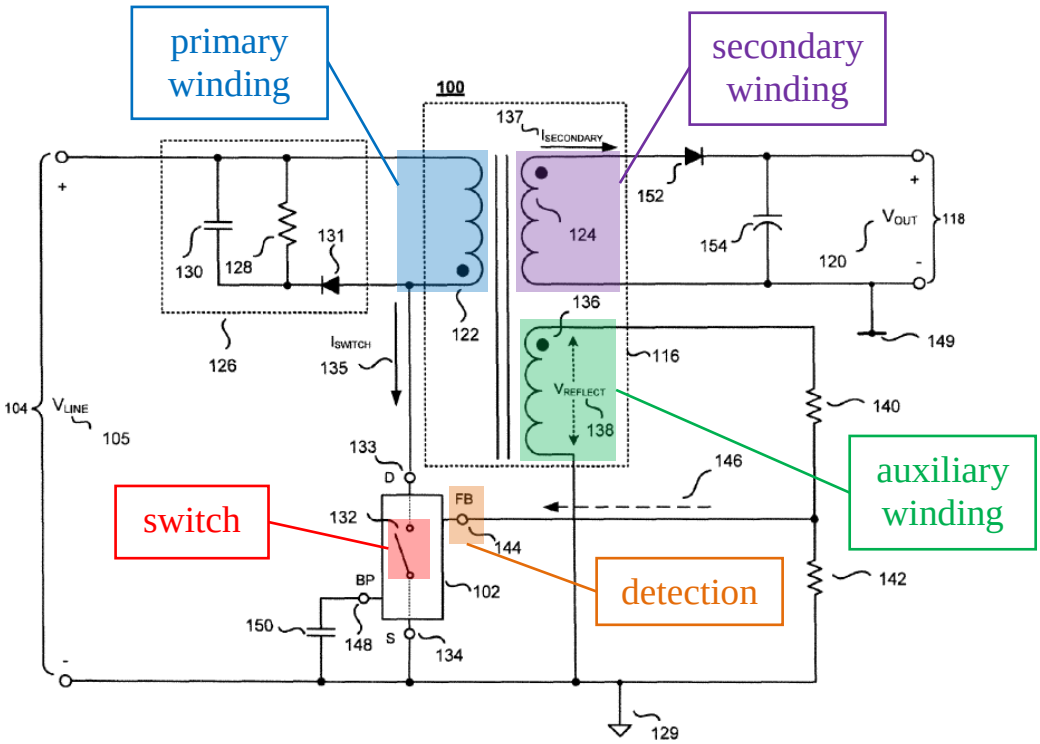
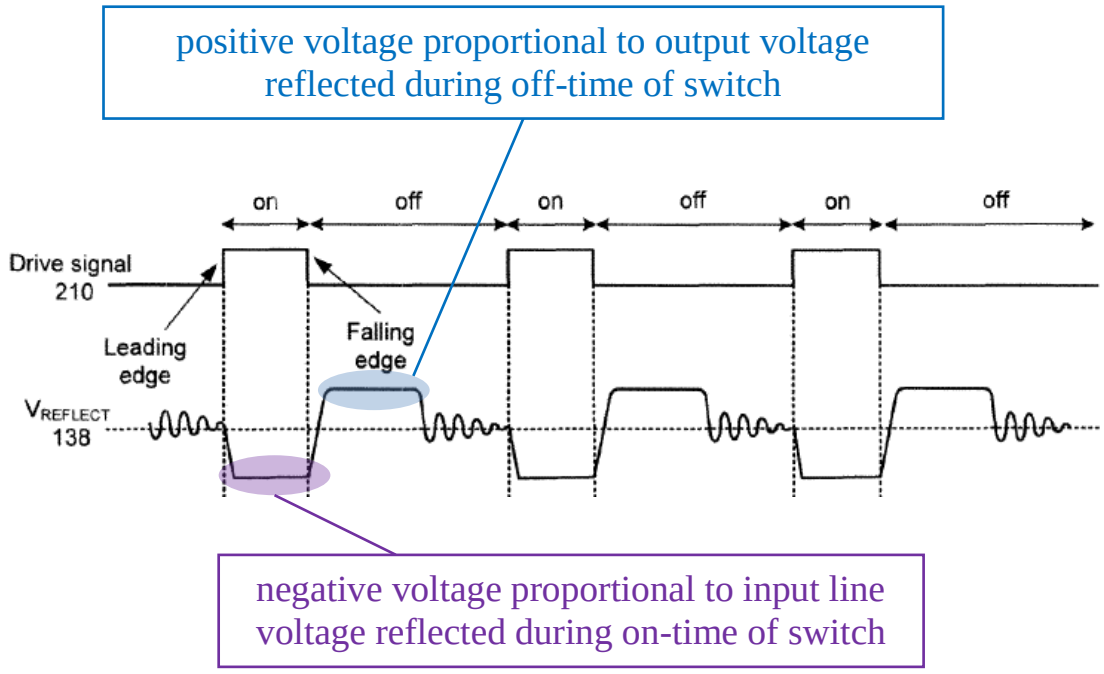


FIG. 1

Ex. 1001, Fig. 1 (annotations added); *see also id.*, 3:5-10. The general operation of the flyback-type converter in the '871 Patent is the same as described above for Yang. Power switch 132 is coupled to input winding 122 (also referred to as the primary winding) of a transformer. When power switch 132 is on, switch current 135 flows through the primary winding and magnetic energy is built up in transformer 100. Ex. 1001, 3:24-32, Fig. 1. And when power switch 132 turns off, the magnetic energy stored in transformer 100 is transferred to the output of the converter via the secondary current 137 produced by the secondary winding. *Id.*, 3:47-53, 4:7-13, Fig. 1.

46. The ’871 Patent purports to improve upon known switching power converters by using the auxiliary winding to detect the input voltage (also referred to as the “line” voltage) in addition to the output voltage. Ex. 1001, 2:54-58, 3:47-58. The ’871 Patent explains that the “reflected voltage $V_{REFLECT}$” at the auxiliary winding is “representative of output voltage V_{OUT} 120 during at least a portion of the time when the power switch 132 is off.” *Id.*, 3:53-58. The ’871 Patent further explains that the “reflected voltage $V_{REFLECT}$” is also “representative of an input line voltage V_{LINE} 105 during at least a portion of the time of when the power switch 132 is on.” *Id.*; *see also id.*, 3:58-4:7. The reflection of both output voltage V_{OUT} and input line voltage V_{LINE} at different times of the switching cycle is shown in Figure 4:



Ex. 1001, Fig. 4 (excerpt) (annotations added).

47. As shown in Figure 4, the auxiliary winding produces a *positive* voltage representative of the output voltage during a portion of the off-time of the power switch, and produces a *negative* voltage representative of the line input voltage during the on-time of the power switch. The polarity of the positive and negative voltages is due to the orientation of auxiliary winding relative to the primary winding and the secondary winding. Referring to Figure 1 of the '871 Patent, the opposing orientation of the primary and auxiliary winding is shown by the dot on the lower end of the primary winding versus the dot on the upper end of the auxiliary winding. Ex. 1001, Fig. 1. Thus, the auxiliary winding reflects negative positive voltage when current flows through the primary winding during the on-time of the switch. In contrast, the auxiliary winding has the same orientation as the secondary winding, with the dot shown on the upper end of the respective windings. *Id.* Thus, the auxiliary winding reflects a positive voltage when current flows through the secondary winding during a portion of the off-time of the switch. Because the respective orientations of the primary, secondary, and auxiliary windings are the same for any flyback-type converter with an auxiliary winding (*see, e.g.*, Ex. 1004, Fig. 7; Ex. 1016, Fig. 4), the reflection of a negative voltage (representing the line input voltage) during the on-time of the switch and a positive voltage (representing the output voltage) during the off-time of the switch

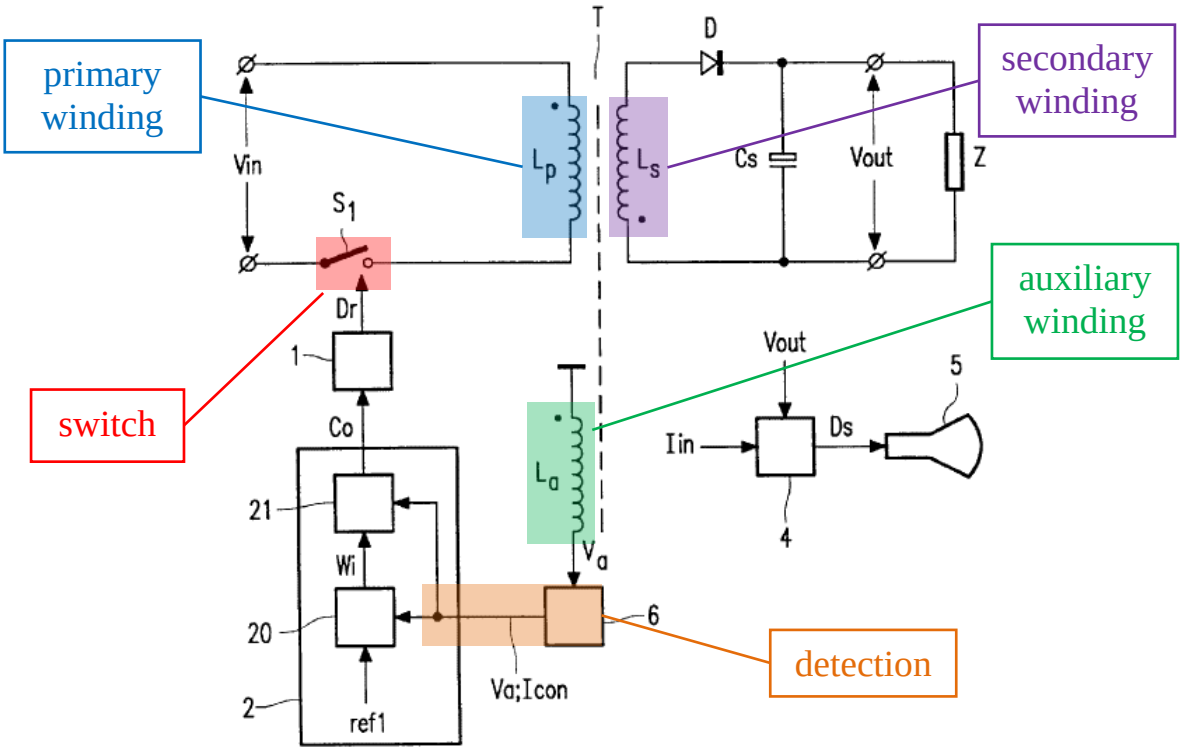
is a common feature of all flyback-type switching power converters with an auxiliary winding (*see* Ex. 1004, 5:5-10, 5:50-55, Fig. 7; Ex. 1016, Figs. 4, 6B).

48. The reflection of both the output voltage and the input line voltage on the auxiliary winding at different times during the switching cycle is merely the result of the magnetic coupling between the different windings of the transformer. In other words, it is the magnetic coupling of the auxiliary winding in the flyback architecture that ***dictates*** the voltage that is reflected by the auxiliary winding during the on-time and off-time of the power switch. *See* Ex. 1001, 3:62-4:34; Ex. 1004, 4:13-28, 4:52-5:5; Ex. 1006, 3:4-15 (each showing that the equation for the reflected voltage is based on the windings ratio of the auxiliary winding to the primary and/or secondary windings). As explained above, the auxiliary winding reflects the voltage present on the secondary winding (i.e., V_{OUT} plus the voltage drop of the rectifier) when current flows through the secondary side (i.e., during off-time of the switch). *See* Ex. 1006, 3:4-15. The auxiliary winding likewise reflects the voltage present on the primary winding (i.e., the input line voltage) when current flows through the primary side (i.e., during the on-time of the switch). *See* Ex. 1004, 5:5-10, 5:50-55. And because the input line voltage is applied to the primary winding during the on-time of the switch, the voltage reflected by the auxiliary winding during this time is proportional to the line voltage. Ex. 1004, 4:52-65, 5:5-10, 5:50-55; Ex. 1008, 7:31-50.

49. Thus, in my opinion, the purported invention of the ’871 Patent is based on nothing more than the recognition of how an auxiliary winding naturally responds during the on-time and off-time of the switch due to the physical relationship (i.e., the magnetic coupling) between the auxiliary winding and the other windings, which exists in every flyback-type power converter with an auxiliary winding.

C. Characteristics of Auxiliary Windings in Flyback Converters Were Well Known in the Art Prior to the Claimed Priority Date of the ’871 Patent

50. Multiple prior art references recognize and describe the relationship between the auxiliary winding and the primary and secondary windings. For example, U.S. Patent 5,831,839 (“Pansier”) issued on November 3, 1998, over eight years prior to the claimed priority date of the ’871 Patent. Ex. 1008. Like the ’871 Patent, Pansier discloses a flyback-type switching power converter with an auxiliary winding:

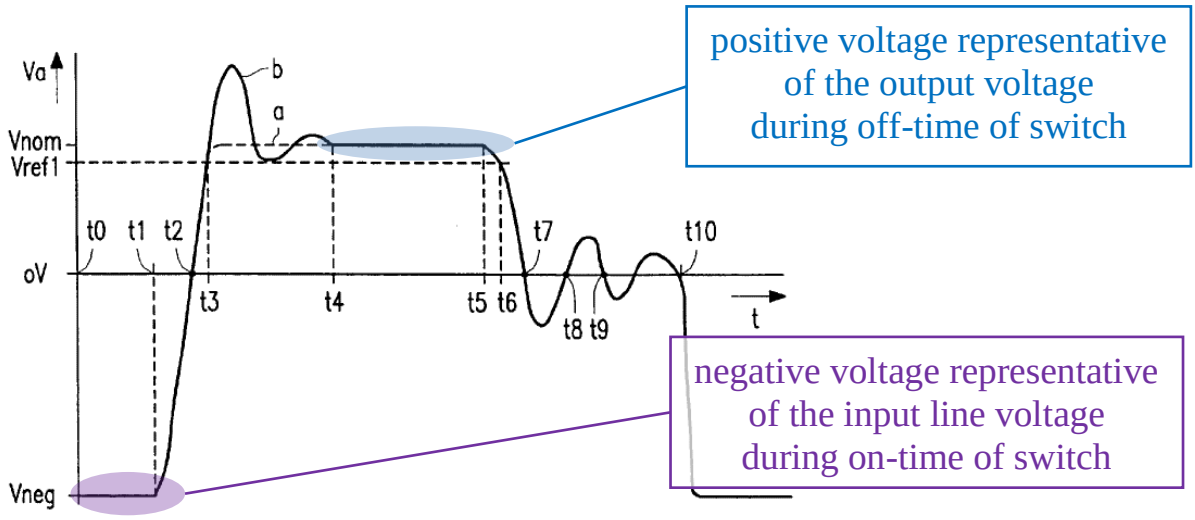


Ex. 1008, Fig. 1 (annotations added).

51. Pansier explains that, during the off-time of the switch, the auxiliary winding voltage Va "is equal to the DC output voltage Vout multiplied by the transformation ratio between the auxiliary winding La and the secondary winding Ls." Ex. 1008, 7:45-50, Fig. 3.[6] On the other hand, "auxiliary winding voltage Va has a negative value Vneg" during the on-time of the switch, "which equals the input voltage Vi multiplied by the transformation ratio between the auxiliary winding La and the primary winding Lp." *Id.*, 7:31-37.

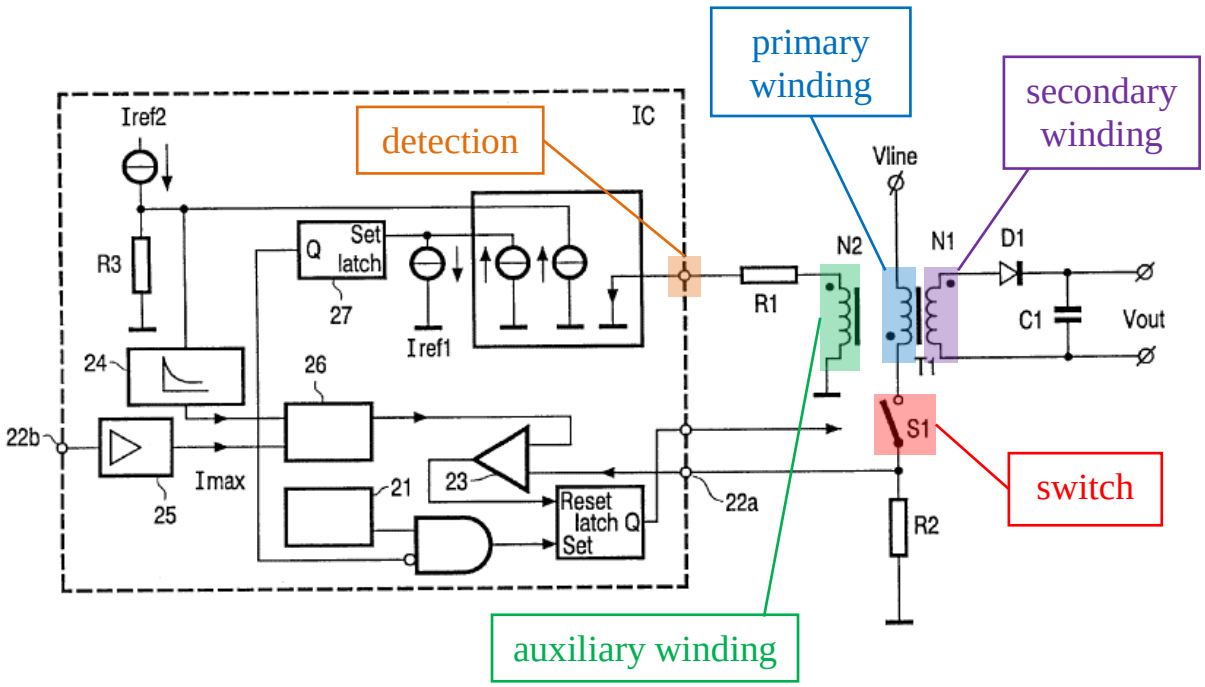
[6] *See also* Ex. 1008, 7:45-64 (explaining temporary overshoot of Va before settling to value representing output voltage).

52. Like Figure 4 of the ’871 Patent, Figure 3 of Pansier illustrates the reflection at the auxiliary winding of both the output voltage (Vout) and input line voltage (Vi) at different times of the switching cycle:



Ex. 1008, Fig. 3 (annotations added).

53. Another example is U.S. Patent 6,542,386 (“Mobers”), which issued on April 1, 2003, over four years before the claimed priority date of the ’871 Patent. Ex. 1004. Like Pansier, Mobers discloses a switching power converter with an auxiliary winding:



Ex. 1004, Fig. 7 (annotations added). Mobers explains that by monitoring the auxiliary winding in a time-phased way, "not only V_{out} can be monitored …, but also V_{line} can be monitored." Ex. 1004, 5:5-10. Specifically, "information relating to the output voltage V_{out} will be present" on the auxiliary winding during the off-time of the switch, whereas "information relating to V_{line} will be present" on the auxiliary winding during the on-time of the switch. *Id.*, 5:50-53.

54. As I explain in detail below in Section IV, Mobers not only describes how the auxiliary winding reflects both the input line voltage and the output voltage during different portions of the switching cycle, but also how its control circuit uses this information to implement different protection functions.

D. Examination History

55. The ’871 Patent is a continuation of U.S. Patent No. 8,406,013, which is a continuation of U.S. Patent No. 8,077,483. I have reviewed the examination history of the ’871 Patent and the ’483 Patent. I understand that during prosecution of the ’483 Patent, Applicants distinguished the purported invention by arguing that the prior art “fails to disclose ‘*a sensor coupled to receive a signal from* ***a single terminal*** *of the controller’ where the signal represents both* ***a line input voltage*** during the on time and ***an output voltage*** during the off time of a power converter.” Ex. 1010, 31 (bold and italics emphases in original). For example, Patent Owner argued that the Yamada and Uruno references received the line input voltage information and the output voltage information from separate terminals, not a single terminal. *Id.*, 30-31. Patent Owner also distinguished the Balakrishnan ’161 reference because a diode in the path of the identified terminal blocked that terminal from receiving a signal representing the line input voltage during the on time. *Id.*, 13.

56. Thus, Patent Owner emphasized that the distinguishing feature of the ’483 Patent (and by association the ’871 Patent) was the single terminal coupled to receive a signal representative of both the input and output voltage. But as I described above in Section III.C, it is the magnetic coupling of the auxiliary winding in the flyback architecture that ***dictates*** the voltage that is reflected by the

auxiliary winding during the on-time and off-time of the power switch. *See* Ex. 1001, 3:62-4:34; Ex. 1004, 4:13-28, 4:52-5:5; Ex. 1006, 3:4-15 (each showing that the equation for the reflected voltage is based on the windings ratio of the auxiliary winding to the primary and/or secondary windings). Thus, an auxiliary winding of a flyback switching power converter naturally reflects both the input and output voltage at different times during the switching cycle due to the physical properties of the transformer. *See, e.g.*, Ex. 1008, 7:31-43, Fig. 3; Ex. 1004, 5:11-14, 5:50-53. Thus, in the absence of a diode that blocks either the positive swing (representing the output voltage) or the negative swing (representing the input line voltage) of the signal from the auxiliary winding, a signal received from an auxiliary winding via a single terminal of the controller will represent both the input and the output voltage.

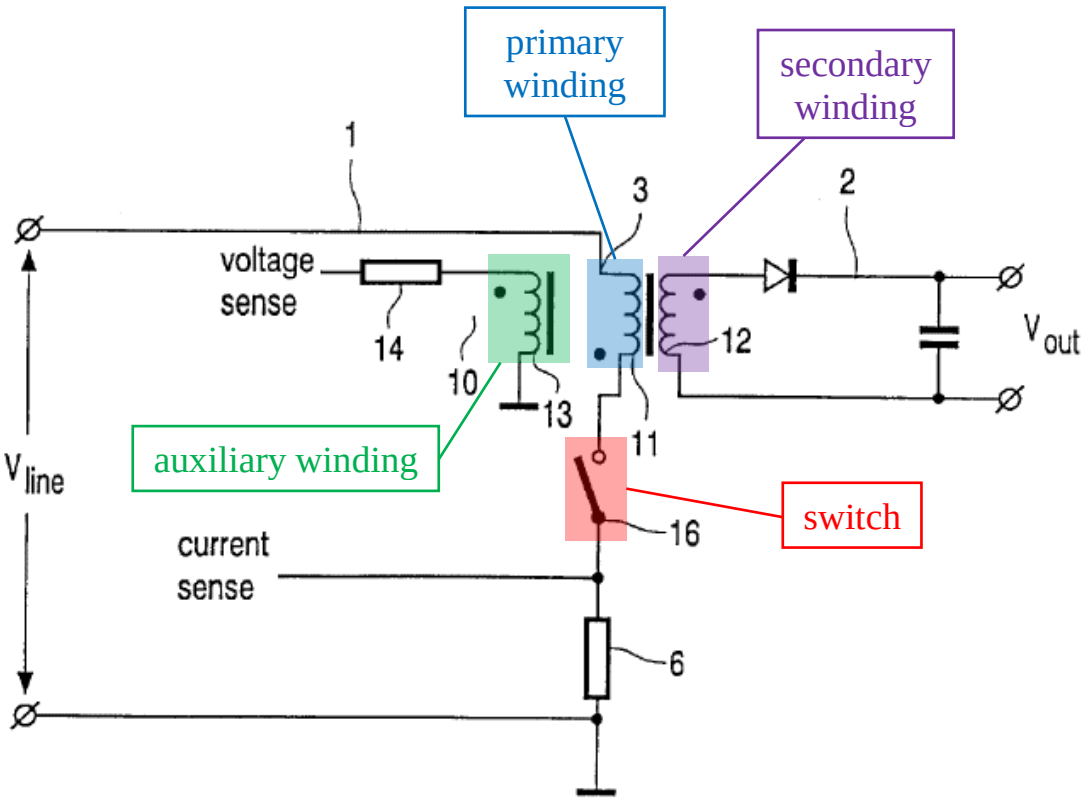
IV. SUMMARY OF PRIOR ART

A. Mobers

57. U.S. Patent 6,542,386 to Mobers et al. ("Mobers") was filed on October 12, 2001 and issued on April 1, 2003. Ex. 1004. The '871 Patent was filed on February 26, 2013 and claims priority to a provisional application filed on April 6, 2007. Ex. 1001. Mobers therefore pre-dates the '871 Patent.

58. Mobers discloses a switching power converter that utilizes a transformer with an auxiliary winding, which is referred to by Mobers as a "control

winding." Ex. 1004, 4:1-28, Fig. 6. Figure 6 illustrates certain components of the switching power converter:



Ex. 1004, Fig. 6 (annotations added). For flyback-type switching power converters like the one shown in Figure 6 of Mobers, the current through the primary winding builds up when the switch is turned on. *See id.*, 1:45-48. This rising current through the primary winding during the on-time of the switch is shown, for example, by the plot of "Ip" in Figure 3 of Mobers. *See id.*, Fig. 3. As the primary-side current builds, the magnetic energy stored in the transformer also builds. When the switch is turned off, the magnetic energy stored in the transformer is transferred to the output via a current produced by the transformer's

secondary winding. Ex. 1004, 1:58-64. This current through the secondary side during the off-time of the switch is in turn shown by the plot of "Is" in Figure 3 of Mobers. *See id.*, Fig. 3.

59. As I described above in Section III.A-C, the auxiliary winding in a flyback-type switching power converter (i) reflects the voltage across the primary winding (indicative of input line voltage) when current flows through the primary side, and (ii) reflects the voltage across the secondary winding (indicative of the output voltage) when current flows through the secondary side. Mobers recognizes this relationship and, with reference to Figure 6, explains: "When a current flows in either of windings 11 or 12, a current will also be induced in regulation circuit 10. The voltage generated across control winding 13 is related to V_{line} or V_{out} … ." Ex. 1004, 4:52-55; *see also id.*, 5:50-53 ("[T]he information relating to V_{line} will be present on the control winding N2 during the primary stroke, whereas information relating to the output voltage V_{out} will be present during the secondary stroke.").

60. Mobers also discloses a technique for how to detect the V_{line} or V_{out} information provided by control winding 13 in Figure 6. Specifically, Mobers clamps the voltage on the left side of resistor 14 in Figure 6 to a fixed potential. Ex. 1004, 4:29-36. When a voltage (indicative of either V_{line} or V_{out}) is generated on the other side of resistor 14 by the control winding, the voltage potential across

the resistor causes a current to flow. *Id.* During the on-time of the switch, the current through the resistor is:

$$I_r = \frac{kV_{line}}{R},$$

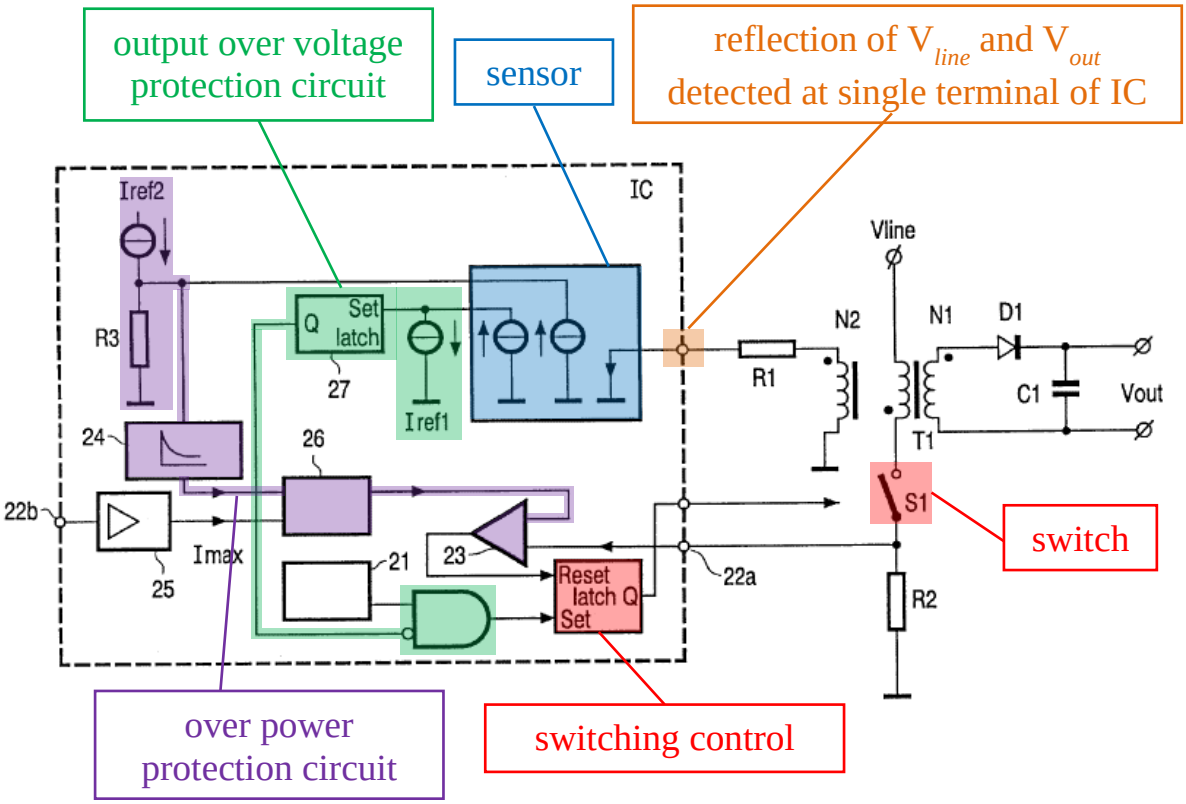
where *R* equals the resistor value and *k* is the winding ratio of the control winding to the primary winding. *Id.*, 4:54-65 (equation 2); *see also id.*, 4:12-20. And during the off-time of the switch, the current through the resistor is:

$$I_r = \frac{mV_{out}}{R}.$$

where *R* equals the resistor value and *m* is the winding ratio of the control winding to the secondary winding. *Id.*, 4:66-5:5 (equation 3); *see also id.*, 4:21-28.

61. During the on-time of the switch, the control winding reflects a negative voltage indicative of V_{line}. Thus, the current through resistor 14 in Figure 6 during the on-time of the switch is a "negative" current, i.e., a current flowing toward the control winding. Ex. 1004, 5:14-19. On the other hand, the control winding reflects a positive voltage indicative of V_{out} during off-time of the switch. Thus, the current through resistor 14 in Figure 6 during the off-time of the switch is a "positive" current, i.e., a current flowing away from the control winding. Ex. 1004, 5:14-19.

62. Building on the explanation of the control winding shown in Figure 6, Mobers illustrates in Figure 7 how an integrated circuit (IC) controller utilizes the V_{line} and V_{out} information provided by control winding N2. Ex. 1004, Fig. 7.



Ex. 1004, Fig. 7 (annotations added).

63. For example, Mobers utilizes the output voltage information to implement output over voltage protection. Ex. 1004, 5:56-62. As shown in Figure 7, the sensor monitors the current from resistor R1, which represents either V_{out} or V_{line}. The sensor reproduces the current representative of V_{out} for comparison to a reference "Iref1." Ex. 1004, Fig. 7. If the current signal representing V_{out} exceeds "Iref1," then an output over voltage condition is detected

and latch 27 is set. *See id.* In turn, the output of latch 27 causes a logic gate to block pulses from oscillator 21 to the switching control latch, which blocks the switching control latch from turning on the switch. *See id.*, Fig. 7, 5:57-62 ("If it is determined that V_{out} comes above a predetermined level a latch is set in circuit 27. This latch prevents switch S1 from switching on again so as to shut down the switched-mode power supply in case of an over voltage being present on the output terminals.").[7]

64. Mobers also utilizes the input line voltage information to implement an over power protection. Ex. 1004, 3:60-62, 5:26-45. The over power protection scheme limits the on-time of the switch when the input line voltage V_{line} is high to prevent too much power from being transferred from the input to the output. Figure 7 of Mobers illustrates that a pulse from oscillator 21 sets the switching control latch to turn on switch S1 during each switching cycle (assuming no output over voltage fault condition). Ex. 1004, 5:27-28, Fig. 7. Comparator 23 resets the switching control latch to turn off switch S1 when the voltage across resistor R2

[7] The logic gate in Figure 7 is an AND gate. The circle at the input of the AND gate indicates that the lower input of the AND gate is inverted. Ex. 1014, 28, 33. Thus, when latch 27 provides a high signal, the inverted input of the AND gate will go low, and any pulses from oscillator 21 to the switching control latch will be blocked.

(which represents the current through switch S1 and resistor R2) exceeds a threshold. *See id.*, 5:28-33, Fig. 7. The threshold for comparator 23 is set by minimum circuit 26. *Id.*, 5:48-50, Fig. 7. During normal conditions, minimum circuit 26 passes the feedback signal from error amplifier 25 to comparator 23. *See id.*, 5:46-50, Fig. 7. The switch is turned off during each cycle when the current through the power switch reaches a threshold that is based on feedback from the output voltage. *See id.*, Fig. 7.

65. The control scheme described in Mobers and shown in Figure 7 is a common scheme that is known in the art as current-mode control or current-programmed control. *See* Ex. 1013, 17; Ex. 1016, 4:49-60. Such current mode control is described, for example, in the Erickson textbook that is geared toward undergraduate and graduate-level course. Ex. 1013, 12, 16-18. At its most basic level, current-mode control operates by turning the power switch off on a cycle-by-cycle basis when the current through the switch reaches a threshold (i.e., a peak current set point) that is determined based on feedback information from the output voltage of the power converter. *See* Ex. 1013, 17-18; Ex. 1015, 4:49-60.

66. Mobers uses such current mode control (*see* Ex. 1004, Fig. 7), and also discloses an over power protection system that limits the maximum power input into the converter by intervening with the current mode control. When the input line voltage is high, the over power protection system intervenes by limiting

the peak current set point as a function of the input line voltage. Minimum circuit 26 passes the smaller of the two thresholds provided by error amplifier 25 and curve circuit 24. *See* Ex. 1004, 5:46-48, Fig. 7. As depicted by the curve inside curve circuit 24 in Figure 7, curve circuit 24 outputs a lower threshold value at higher input line voltages. *Id.*, 5:38-45, Fig. 7. When the signal from curve circuit 24 is less than the feedback signal from error amplifier 25, minimum circuit 26 passes the threshold from curve circuit 24 to comparator 23. *See id.*, 5:46-50, Fig. 7. This limits the peak current allowed through switch S1 as a function of the input line voltage, thereby preventing the amount of power passed to the output from exceeding a maximum safe level. *Id.*, 5:46-50, Fig. 7; *see also id.*, Abstract, 1:5-13, 2:50-53, 3:60-62.

67. Notably, Mobers explains that the "advantage" of its detection scheme is that both V_{out} and V_{line} are detected "via the same existing pin on the integrated circuit." *Id.*, 5:20-25; *see also id.*, 2:56-61, 3:14-20. The advantages of detecting both the output voltage and the input line voltage via a single terminal of an IC coupled to an auxiliary winding of a flyback-type switching power converter were therefore known in the prior art before the claimed priority date of the '871 Patent.

V. CLAIM CONSTRUCTION

68. I understand that the '871 Patent is at issue in a District Court proceeding entitled *ON Semiconductor Corp., et al. v. Power Integrations, Inc.*,

No. 17-cv-247-LPS-CJB (D. Del.) ("Delaware Litigation"). Ex. 1009. I also understand that neither Petitioner nor Patent Owner raised a claim construction issue involving the '871 Patent for the District Court to resolve in the Delaware Litigation. Ex. 1011.

69. I understand that the words of the claim are given their plain and ordinary meaning unless inconsistent with the specification. I provide my opinion below with respect to what I consider the plain and ordinary meaning of certain terms of the '871 Patent, consistent with the specification.

A. "switching control" elements (Claim 1)

70. Claim element 1[c] requires "a switching control to be coupled to switch the power switch to regulate the output of the power converter in response to the sensor." Ex. 1001, 8:59-61. Part of claim element 1[d] then recites "wherein the switching control is further coupled to switch the power switch to regulate the output of the power converter in response to the power limit signal."[8] *Id.*, Col. 8:64-67. The phrase "further coupled to switch the power switch to regulate the output of the power converter in response to the power limit signal" further defines the coupling of the switching control to specify that regulation of the output is specifically in response to the power limit signal from the sensor. In

[8] Like Claim 1, Claim 8 and its dependent Claim 14 together recite the "coupled to" language (Claim 8) and the "further coupled to" language (Claim 14).

my opinion, the plain meaning of this language does not, however, require a separate coupling between the sensor and the switching control, or between the switching control and the power switch, as compared to the coupling required by claim element 1[c].

71. In addition to the '871 Patent itself, I have reviewed Patent Owner's infringement contentions for the '871 Patent in the Delaware Litigation. Ex. 1012. I note that Patent Owner appears to have applied a similarly broad view of the plain and ordinary meaning of the switching control elements. For example, with respect to the alleged infringing device, Patent Owner pointed to the over power protection ("OPP") and the over voltage protection ("OVP") as mapping to claim element 1[c][9] (which includes the "coupled to" language). Ex. 1012, pp. 5-7 ("The NCP1250 implements over power protection ('OPP') that reduces the peak current set point of the switching control in response to sensing the signal representative of the input voltage at the OPP/Latch pin. ... The NCP1250 also implements a latching output over-voltage protection ('OVP') that will stop the switching of the power switch when an output over voltage is detected.").

[9] The claim elements labeled 1[c] and 1[d] herein are respectively labeled 1[d] and 1[e] in Patent Owner's infringement contentions. *See* Ex. 1012, 5-7, 8-9.

72. Patent Owner then pointed to the over power protection circuit again as mapping to claim element 1[d][10] (which includes the "further coupled to" language). Ex. 1012, pp. 8-9 ("The NCP1250 implements over power protection ('OPP') that reduces the peak current set point of the switching control in response to sensing the signal representative of the input voltage at the OPP/Latch pin."). Thus, as applied by Patent Owner, the "further coupled to" language in claim element 1[d] would not require a separate or additional coupling for the switching control as compared to what is already identified in claim element 1[c].

VI. THE CHALLENGED CLAIMS ARE UNPATENTABLE

A. Ground 1: Mobers Anticipates Claims 1-3, 6, 8, 12, 14, and 15

73. In my opinion, Mobers discloses each element of claims 1, 2, 3, 6, 8, 12, 14, and 15, and thus anticipates each of these claims.

(i) Claim 1

a) 1[pre]: "A controller for use in a power converter, comprising:"

74. Mobers discloses a controller for use in a power converter. "The switched-mode power supply … may … comprise a control circuit for controlling the controllable current switching means. The control circuit may comprise a

[10] The claim elements labeled 1[c] and 1[d] herein are respectively labeled 1[d] and 1[e] in Patent Owner's infringement contentions. *See* Ex. 1012, 5-7, 8-9.

PWM-circuit operating the switch at a frequency between 25-250 kHz." Ex. 1004, 3:6-11 (emphasis added). The PWM control circuit is specifically shown in Fig. 7:

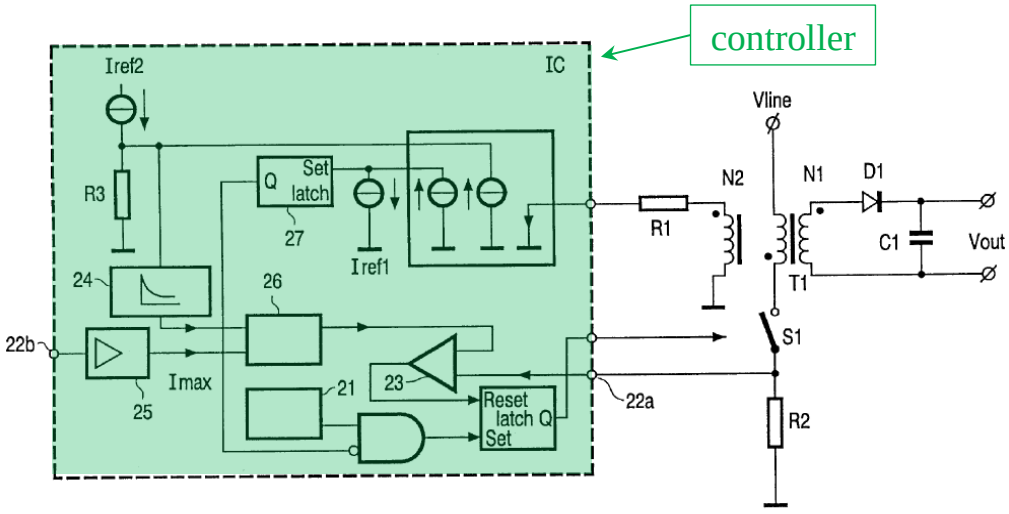


FIG. 7

Ex. 1004, Fig. 7; *see also id.*, 5:26-33. Accordingly, Mobers discloses each element of the preamble of Claim 1.[11]

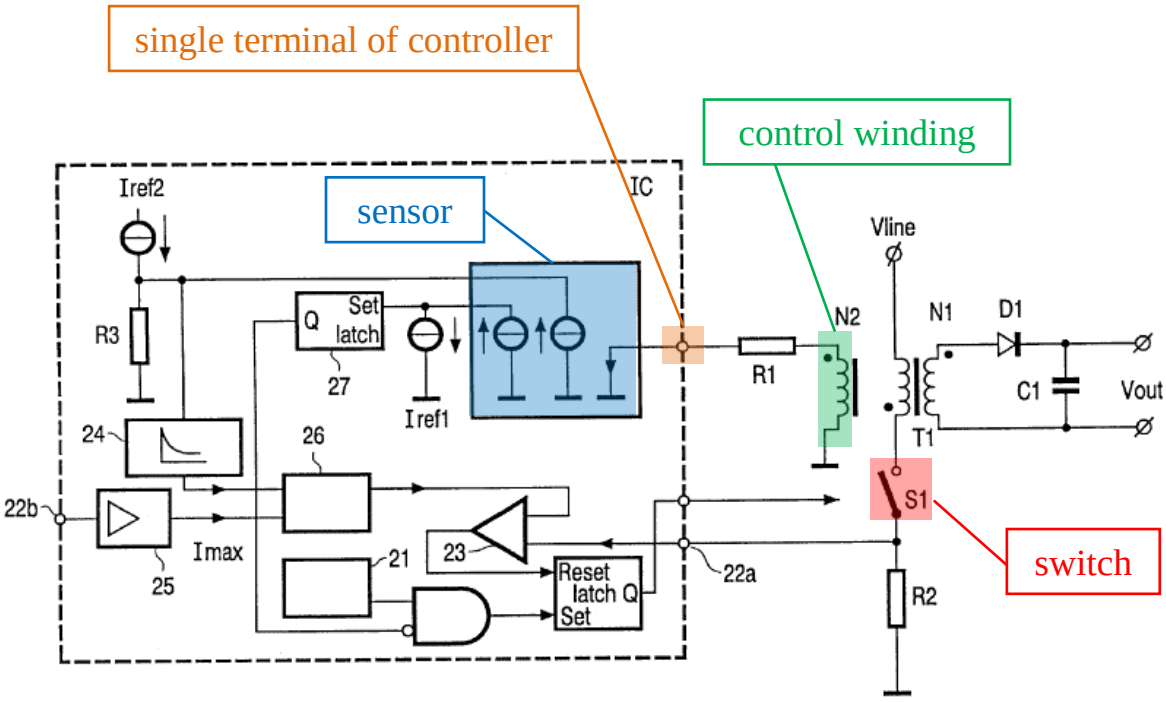
1[pre]. A controller for use in a power converter, comprising:	Ex. 1004, 3:6-12: "The switched-mode power supply according to the first aspect of the present invention may further comprise a control circuit for controlling the controllable current switching means. The control circuit may comprise a PWM-circuit operating the switch at a frequency between 25-250 kHz. The control circuit typically response to a control signal from the third winding." Ex. 1004, 5:26-33: "Referring now to FIG. 7, the switch S1 is controlled by a PWM signal from a PWM circuit. The switch is switched on by the set signal from the oscillator 21. The switch is switched off if a certain peak current through S1 is sensed. As previously mentioned, the peak current through S1 is sensed by sensing the voltage generated across R2. This sensed voltage is

[11] The preamble is not limiting in my opinion, but is nonetheless disclosed by Mobers.

	provided through pin 22a. As soon as the comparator 23 trips, S1 is switched off." *See also* Ex. 1004, 5:20-25, 5:34-62, 5:63-6:3; Figs. 6-8, Claims 1, 3, 5, 6.

b) 1[a]: "a sensor coupled to receive a signal from a single terminal of the controller,"

75. As shown in Figure 7, Mobers discloses a sensor coupled to receive a signal from a single terminal of the controller:



Ex. 1004, Fig. 7 (annotations added). Mobers explains that the controller typically responds "to a control signal from the third winding" (i.e., control winding N2). *Id.*, 3:11-12. "Preferably, the control signal relates to the input voltage to the power supply in the first period of time. In the second period of time the control signal relates to the output voltage of the power supply." *Id.*, 3:14-17. And

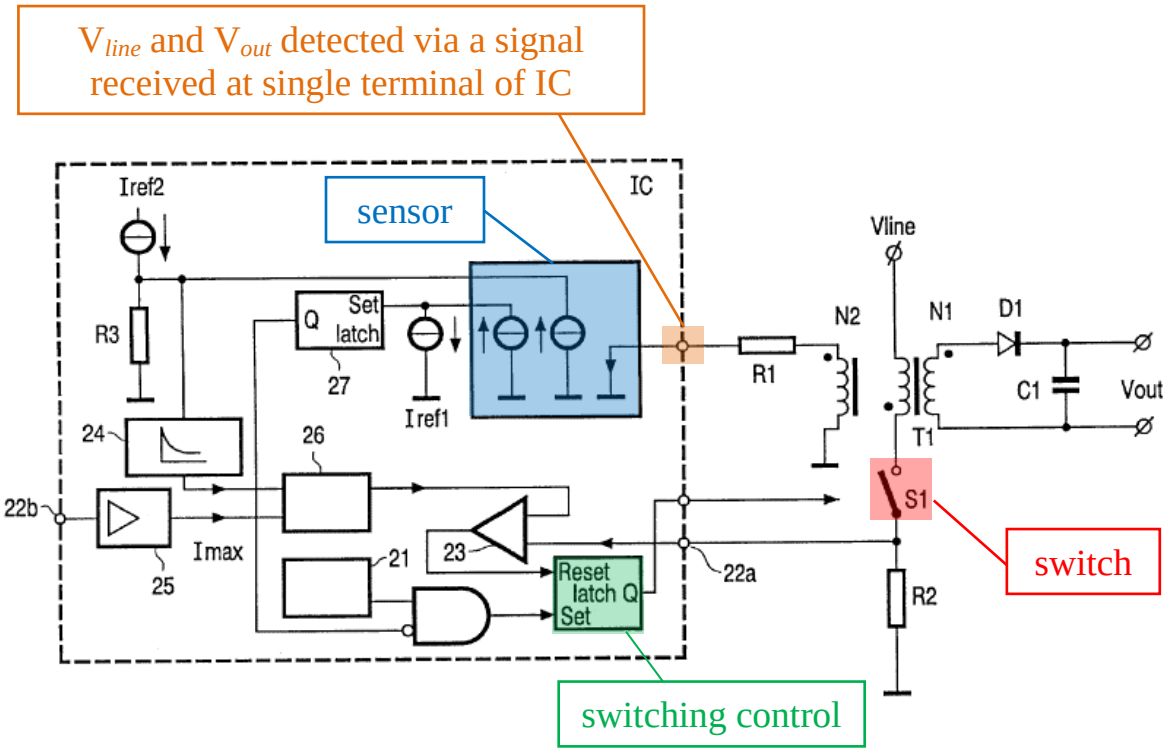
because "a plurality of information is provided via the same control signal the control circuit may receive that information via a *single input pin*." *Id.*, 3:18-20 (emphasis added).

76. Accordingly, Mobers discloses each limitation of claim element 1[a].

[1a] a sensor coupled to receive a signal from a single terminal of the controller,	Ex. 1004, 5:50-55: "As previously mentioned the information relating to V_{line} will be present on the control winding N2 during the primary stroke, whereas information relating to the output voltage V_{out} will be present during the secondary stroke. Therefore, the very same pin on the IC can be used for obtaining both types of information." (emphasis added). Ex. 1004, 3:18-20: "Since a plurality of information is provided via the same control signal the control circuit may receive that information via a single input pin." (emphasis added). Ex. 1004, 5:20-25: "It is an advantage of the present invention that the information obtained during the primary and secondary strokes are provided via the same existing pin on the integrated circuit receiving and processing the information thereby avoiding the additional external components as suggested in the prior art." (emphasis added). Ex. 1004, Claim 5: "A switched-mode power regulator according to claim 3, wherein the control signal from the monitoring means is received by the control circuit via a single input pin." (emphasis added). *See also* Ex. 1004, Abstract, 1:5-13, 2:56-61, 3:1-17, 4:29-36, 4:52-5:4, 5:6-19, 5:63-6:3, Claims 1, 3, 4, 6, 10, Figures 6-8.

c) 1[b]: "the signal from the single terminal to represent an output voltage of the power converter during at least a portion of an off time of a power switch and the signal from the single terminal to represent a line input voltage during a portion of an on time of the power switch,"

77. As shown in Figure 7 of Mobers, the sensor is coupled to receive, from a single terminal of the "IC," the signal that is generated by control winding N2 and resistor R1:



Id., Fig. 7 (annotations added).

78. The signal received by the sensor from resistor R1, via the single terminal of the controller, represents (i) the input line voltage (V_{line}) of the power converter during the on time of switch S1, and (ii) the output voltage (V_{out}) of the

power converter during at least a portion of the off-time of switch S1. *See* Ex. 1004, 5:50-55.

79. Mobers discloses how V_{line} and V_{out} are represented by the signal that the sensor receives from the resistor (e.g., resistor R1 in Figure 7) coupled to the control winding. Specifically, Mobers clamps the voltage on the left side of the resistor to a fixed potential. Ex. 1004, 4:29-36, Figs. 6-7; *see also id.*, 5:63-6:3, Fig. 8. When a voltage is generated by the control winding (indicative of either V_{line} or V_{out}) on the other side of the resistor, the voltage potential across the resistor causes a current to flow. *Id.* During the on-time of the switch (i.e., when V_{line} is reflected on the control winding), the current through the resistor is:

$$I_r = \frac{kV_{line}}{R},$$

where *R* equals the resistor value and *k* is the winding ratio of the control winding to the primary winding. *Id.*, 4:54-65 (equation 2); *see also id.*, 4:12-20. And during the off-time of the switch (i.e., when V_{out} is reflected on the control winding), the current through the resistor is:

$$I_r = \frac{mV_{out}}{R}.$$

where *R* equals the resistor value and *m* is the winding ratio of the control winding to the secondary winding. *Id.*, 4:66-5:5 (equation 3); *see also id.*, 4:21-28.

80. Because the control winding reflects a negative voltage indicative of V_{line} during the on-time of the switch (*see supra* Sections III.B-C), the current through resistor 14 in Figure 6 during the on-time of the switch is a "negative" current, i.e., a current flowing toward the control winding (Ex. 1004, 5:14-19). On the other hand, because the control winding reflects a positive voltage indicative of V_{out} during off-time of the switch (*see supra* Sections III.B-C), the current through resistor 14 in Figure 6 during the off-time of the switch is a "positive" current, i.e., a current flowing away from the control winding (Ex. 1004, 5:14-19).

81. In sum, the signal received by the sensor represents both the input line voltage V_{line} and the output voltage V_{out} during different times of the switching cycle as required by claim element 1[b]. Accordingly, Mobers discloses each limitation of claim element 1[b].

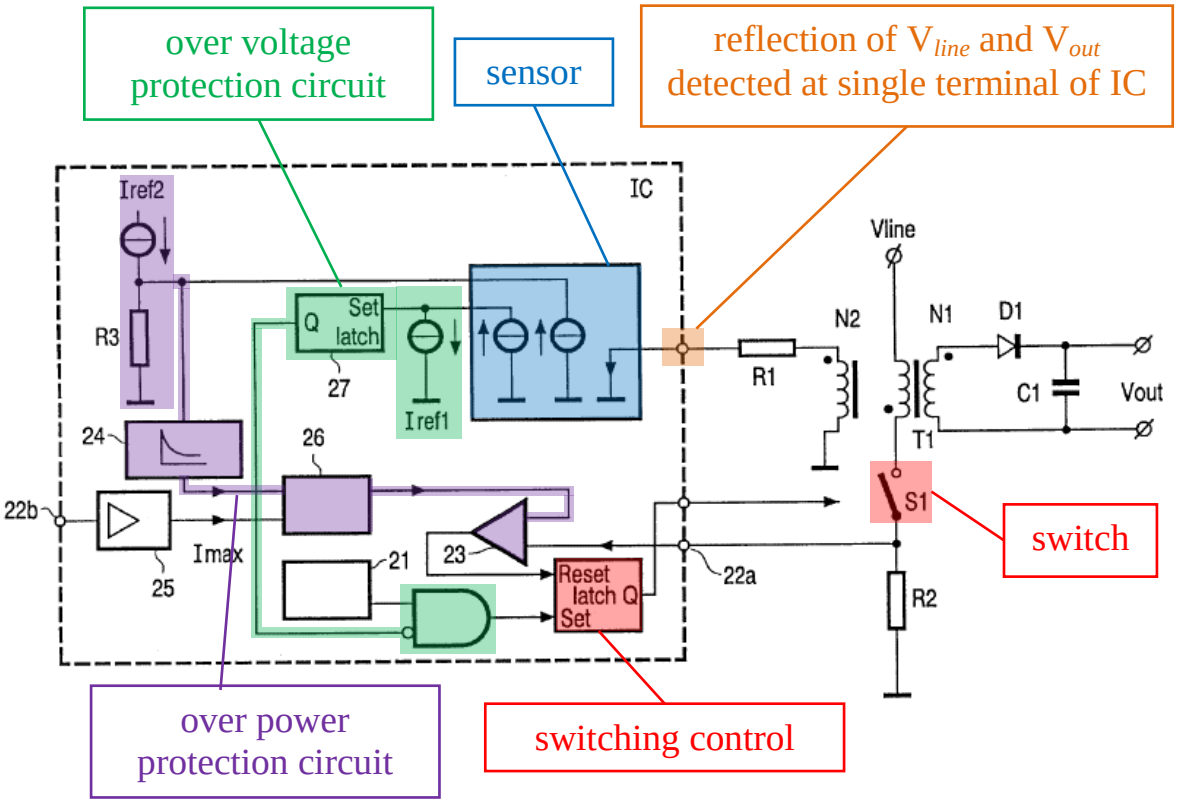
[1b] the signal from the single terminal to represent an output voltage of the power converter during at least a portion of an off time of the power switch, the signal from the single terminal to represent a line input voltage	*See* citations for claim element 1[a]. Ex. 1004, 3:11-17: "The control circuit typically response to a control signal from the third winding. This control signal may comprise a [sic] information relating to the performance or status of the switched mode power supply. Preferably, the control signal relates to the input voltage to the power supply in the first period of time. In the second period of time the control signal relates to the output voltage of the power supply." (emphasis added). Ex. 1004, 5:50-53: "As previously mentioned the information relating to V_{line} will be present on the control winding N2 during the primary stroke, whereas information relating to the output voltage V_{out} will be present during the secondary stroke. Therefore, the very same pin on the IC can be used for obtaining both types of information."

during a portion of an on time of the power switch,	Ex. 1004, 4:29-36: "One end of the control winding 13 is connected to ground whereas the other and of the control winding is connected to resistor 14. By clamping the left side of resistor 14 to a fixed potential a current will flow through resistor 14 when this potential is different from the voltage generated across control winding 13. By measuring the current flowing through resistor 14 the voltage generated across the control winding 13 can be determined." Ex. 1004, 4:52-5:5: "When a current flows in either of windings 11 or 12, a current will also be induced in regulation circuit 10. The voltage generated across control winding 13 is related to V_{line} or V_{out} according to ratios k and m, respectively. A sensing circuit (not shown) measures the current flowing through resistor 14. Thus, knowing the value of resistor 14, V_{line} and V_{out} can be monitored. If the resistor 14 has resistance R, the current in the regulation circuit 10, I_r, is related to Vl_{ine} during t_{on} in the following way $$I_r = \frac{kV_{line}}{R}, \quad (2)$$ whereas, during t_{off}, the current is related to Vout in the following way $$I_r = \frac{mV_{out}}{R}. \quad (3)$$ " Ex. 1004, 5:5-10: "Hence by monitoring the voltage in control winding 13 in a time phased way, not only V_{out} can be monitored in order to provide over voltage protection in the secondary circuit 2, but also V_{line} can be monitored in order to provide over power protection by operating the gate driving circuit in an appropriate way." Ex. 1004, Claim 6: "A switched mode power regulator according to claim 1, further comprising an integrated circuit (IC) having a single pin for receiving both information relating to an input voltage to the primary circuit in a first period of time in which energy is stored in the energy storing device (3) and information relating to an output voltage from the secondary circuit in a second period of time in which energy is

	released from the energy device (3)." Ex. 1004, Claim 10: "A method according to claim 9, wherein the monitoring circuit provides a control signal in response a measured level of the input and output voltages, said control signal relating to the input voltage in the first period of time, and said control signal relating to the output voltage in the second period of time." *See* citations to Mobers in Section IV.A. *See also* Ex. 1004, Abstract, 1:5-13, 3:60-67, 5:14-19, 5:20-25, 5:56-57.

d) 1[c]: "a switching control to be coupled to switch the power switch to regulate an output of the power converter in response to the sensor; and"

82. Mobers discloses a latch (i.e., a switching control) that controls switch S1 (i.e., the power switch) to regulate V_{out} (i.e., an output of the power converter). As explained with reference to Figure 6, the output voltage (V_{out}) of the switched power supply is controlled by regulating the conduction time of the switch, and thereby the amount of energy that is transferred from the primary side to the secondary side of the converter. Ex. 1004, 4:37-51; *see also id.*, 1:36-54. In turn, Figure 7 illustrates the switching control latch inside the controller circuit that turns the power switch on and off:



Id., Fig. 7 (annotations added). Mobers discloses:

> [T]he switch S1 is controlled by a PWM signal from a PWM circuit. The switch is switched on by the set signal from the oscillator 21. The switch is switched off if a certain peak current through S1 is sensed. As previously mentioned, the peak current through S1 is sensed by sensing the voltage generated across R2. This sensed voltage is provided through pin 22a. As soon as the comparator 23 trips, S1 is switched off.

Id., 5:26-33.

83. The switching control latch shown in Figure 7 controls switch S1 to regulate the output voltage. *See* Ex. 1004, 5:26-62. And as shown in the above

annotation of Figure 7, the switching control latch is responsive to the sensor via both the over power protection circuit and the output over voltage protection circuit.

84. During operation, the switch is turned on when a set signal from oscillator 21 sets the switching control latch. *See id.*, 5:27-28, Fig. 7. However, if the level of V_{out} detected by the sensor during the off time of the switch exceeds a predetermined level, the over voltage protection latch sends a fault signal to the logic gate located between oscillator 21 and the switching control latch. *See id.*, 5:57-62, Fig. 7. When the fault signal is asserted, the logic gate[12] blocks set signals that would otherwise be transmitted from oscillator 21 to the switching control latch, thereby preventing switch S1 from being turned on during subsequent switching cycles. Ex. 1004, 5:59-62.

85. In addition, the output power protection circuit may determine when switching control latch turns off switch S1 during a given switching cycle based on V_{line} information from the sensor. As shown in Figure 7, the current through

[12] The logic gate in Figure 7 is an AND gate. The circle at the input of the AND gate indicates that the lower input of the AND gate is inverted. Ex. 1014, 28, 33. Thus, when latch 27 provides a high signal, the inverted input of the AND gate will go low, and any pulses from oscillator 21 to the switching control latch will be blocked.

switch S1 is monitored by comparator 23, which is coupled to sense resistor R2. Ex. 1004, 5:30-31, Fig. 7. Comparator 23 resets the switching control latch to turn off switch S1 when the voltage across sense resistor R2 (which represents the current through switch S1 and resistor R2) exceeds a threshold. *See id.*, 5:28-33, Fig. 7. And, as described in Mobers, the over power protection circuit adjusts the peak current threshold provided by minimum circuit 21 based on information from the sensor relating to V_{line}. *Id.*, 5:34-50, Fig. 7.

86. Specifically, curve circuit 24 processes the input line voltage information from the sensor and passes a threshold level to minimum circuit 26. Ex. 1004, 5:34-45. When the signal from curve circuit 24 is less than the feedback signal from error amplifier 25, minimum circuit 26 passes the threshold from curve circuit 24 to comparator 23. *See id.*, 5:46-50, Fig. 7. This limits the peak current through switch S1 during the on time of a given switching cycle as a function of the input line voltage, thereby preventing the amount of power passed to the output from exceeding a maximum safe level. *Id.*, 5:46-50, Fig. 7; *see also id.*, Abstract, 1:5-13, 2:50-53, 3:60-62. Accordingly, the switching control in Mobers is coupled to switch the power switch to regulate the output voltage V_{out} in response to the sensor via both the output over voltage protection circuit and the over power protection circuit. Mobers therefore discloses each limitation of claim element 1[c].

87. I have reviewed Patent Owner's infringement contentions for the '871 Patent in the Delaware Litigation. *See* Ex. 1012. I note that the mapping of claim element 1[c] to the Mobers prior art is analogous to Patent Owner's mapping of this element[13] in its infringement contentions. *See* Ex. 1012, 5-7. As discussed above in Section V.A, Patent Owner's infringement contentions identify both the over power protection circuit and the output over voltage protection circuit in the accused product as inputs to the switching control coupled to switch the power switch to regulate the output voltage. Ex. 1012, 5-7. Thus, Mobers discloses claim element 1[c] in the same manner as compared to Patent Owner's alleged mapping of the products accused in the Delaware Litigation.

[1c] a switching control to be coupled to switch the power switch to regulate an output of the power converter in response to the sensor; and	*See* citations for claim elements 1[a]. Ex. 1004, 3:6-17: "The switched-mode power supply according to the first aspect of the present invention may further comprise a control circuit for controlling the controllable current switching means. The control circuit may comprise a PWM-circuit operating the switch at a frequency between 25-250 kHz. The control circuit typically response [sic] to a control signal from the third winding. This control signal may comprise a information relating to the performance or status of the switched mode power supply. Preferably, the control signal relates to the input voltage to the power supply in the first period of time. In the second period of time the control signal relates to the output voltage of the power supply." (emphasis added). Ex. 1004, 5:5-10: "Hence by monitoring the voltage in

[13] The claim element labeled 1[c] herein is labeled as claim element 1[d] in Patent Owner's infringement contentions. *See* Ex. 1012, 5-7.

	control winding 13 in a time phased way, not only V_{out} can be monitored in order to provide over voltage protection in the secondary circuit 2, but also V_{line} can be monitored in order to provide over power protection by operating the gate driving circuit in an appropriate way." (emphasis added). Ex. 1004, 3:60-67: "This control winding forms part of an over power protection system by providing information relating to the line voltage V_{line}. Additionally, the control winding forms part of an over voltage protection system by monitoring the output voltage V_{out} of the switched-mode power supply. As it will be explained in further details below, the sensing of V_{line} and the monitoring of V_{out} is performed in a time phased way." Ex. 1004, 5:26-62: "Referring now to FIG. 7, the switch S1 is controlled by a PWM signal from a PWM circuit. The switch is switched on by the set signal from the oscillator 21. The switch is switched off if a certain peak current through S1 is sensed. As previously mentioned, the peak current through S1 is sensed by sensing the voltage generated across R2. This sensed voltage is provided through pin 22a. As soon as the comparator 23 trips, S1 is switched off. Besides the input signal from 22a, also a signal from the over power protection circuit is used to determine the peak current through S1 and R2. For this purpose the information relating to V_{line} is used. This information is retrieved from the control winding N2 of the transformer. The V_{line} information is processed in the 'curve' circuit 24. The processor is a multiplier that transforms the input signal into the square root of the signal. The square root is taken, because for this system the optimum compensation will be made. Alternatively, a linear function will also do, but then the maximum output power still has quite some V_{line} dependence. The information from the over power protection circuit can reduce the peak current if the output signal is lower than the signal from the error amplifier 25 on pin 22b. The magnitude of both signals is sensed by the minimum (min.)

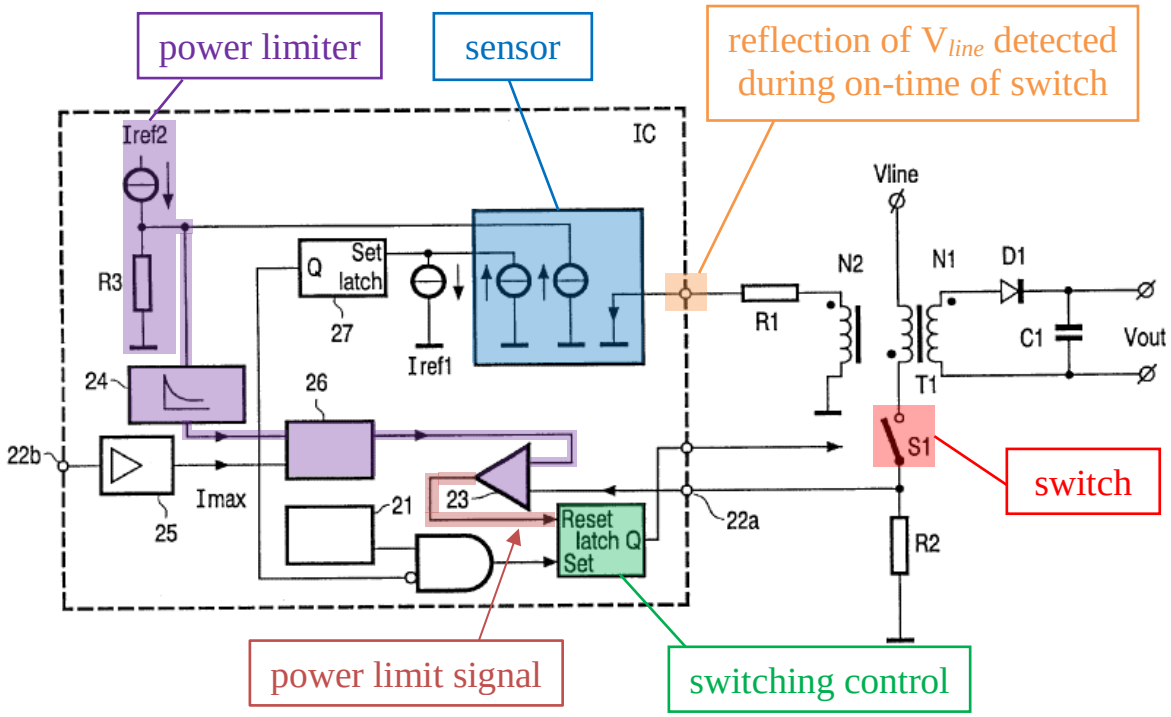
	circuit 26. As previously mentioned the information relating to V_{line} will be present on the control winding N2 during the primary stroke, whereas information relating to the output voltage V_{out} will be present during the secondary stroke. Therefore, the very same pin on the IC can be used for obtaining both types of information. As previously mentioned, information relating to V_{out} is available during the secondary stroke. If it is determined that V_{out} comes above a predetermined level a latch is set in circuit 27. This latch prevents switch S1 from switching on again so as to shut down the switched-mode power supply in case of an over voltage being present on the output terminals." Ex. 1004, 4:37-51: "The output voltage of the switched power supply, V_{out}, is controlled by controlling the current in the primary circuit I_p. I_p is controlled by operating switch 16 in a time phased way using a driving circuit (not shown [in Fig. 6]). I_p is sensed by measuring the voltage generated across resistor 5. The measured voltage is used as a control signal to the gate driving circuit (not shown [in Fig. 6]), which—in response the control signal—controls the conduction time of switch 16. Upon switching switch 16 on I_p starts to build up in the primary circuit 1. When I_p reaches a predetermined level, switch 16 is turned off. After switching switch 16 off the energy stored in transformer 3 is transferred to the secondary circuit 2. This energy transfer induces a current Is in the secondary circuit 2." Ex. 1004, 1:36-65: "The level of V_{out} is controlled by controlling the current in the primary circuit, I_p, using the controllable switch 4. I_p is determined by measuring a voltage drop across resistor 5. The measured voltage drop—which represents I_p—is provided as a control signal to a Pulse Width Modulator (PWM) circuit. The PWM-circuit adjusts the conduction time of the controllable switch 4 so as to obtain a predetermined current value. Typically, the controllable switch 4 is a transistor. The primary winding of the transformer has the inductance L. When the PWM-

	circuit switches the transistor on, I_p starts to build up in the primary circuit. The increase of I_p during t_{on} (t_{on} is the conduction time of the transistor) is illustrated in FIG. 2. FIG. 2 also illustrates the voltage across the controllable switch 4 and the current in the secondary circuit, I_s. The dashed line shows V_{line}. The controllable switch is switched off when I_p has reached a predetermined value. Thus, the conduction time is dependent on the predetermined level of the I_p—i.e. increasing the level of I_p increases the conduction time. For obvious reasons the conduction time is also dependent on the level of the input voltage and the inductance, L, of the primary winding of the transformer. When the predetermined level of I_p has been reached the controllable switch 4 is turned off, and the magnetically stored energy in the transformer 3 is transformed to the secondary circuit 2. The transformation of energy to the secondary circuit induces a current, Is, in the secondary circuit. I_s is rectified using e.g. the diode based rectifier and the capacitor 7 in combination." *See also* Ex. 1004, Abstract, 1:5-13, 2:51-55, 3:6-32, 4:37-44, 5:20-25, 5:34-6:3; Figs. 1-4 and 6-8; Claims 1, 3, 8-11.

e) 1[d]: "a power limiter coupled to the sensor to output a power limit signal to the switching control in response to the line input voltage of the power converter, wherein the switching control is further coupled to switch the power switch to regulate the output of the power converter in response to the power limit signal"

88. As described above for claim element 1[b], the signal received by the sensor from resistor R1 represents the input line voltage (V_{line}) of the power converter during the on time of switch S1. *See* Ex. 1004, 5:50-55. Mobers utilizes this input line voltage information to implement over power protection. Ex. 1004,

3:60-62, 5:26-45. The over power protection circuitry limits the on-time of the switch when the input line voltage V_{line} is high to prevent too much power from being transferred from the input to the output.



Ex. 1004, Fig. 7 (annotations added).

89. Figure 7 of Mobers illustrates that a pulse from oscillator 21 sets the switching control latch to turn on switch S1 during each switching cycle (assuming no output over voltage fault condition). Ex. 1004, 5:27-28, Fig. 7. Comparator 23 resets the switching control latch to turn off switch S1 when the voltage across resistor R2 (which represents the current through switch S1 and resistor R2) exceeds a threshold. *See id.*, 5:28-33, Fig. 7. The threshold for comparator 23 is set by minimum circuit 26. *Id.*, 5:48-50, Fig. 7. During normal conditions,

minimum circuit 26 passes the feedback signal from error amplifier 25 to comparator 23. *See id.*, 5:46-50, Fig. 7. This forms what is known in the art as a current mode control loop, whereby the switch is turned off during each cycle when the current through the power switch reaches a threshold that is based on feedback from the output voltage. *See* Ex. 1013, 16-18; Ex. 1016, 4:49-60.

90. However, when the input line voltage is high, the over power protection system intervenes by limiting the peak current set point as a function of the input line voltage. Based on the line voltage information from the sensor, curve circuit 24 passes a threshold level to minimum circuit 26. Ex. 1004, 5:34-45. As depicted by the curve inside curve circuit 24 in Figure 7, curve circuit 24 provides lower threshold values to minimum circuit 26 at higher input line voltages. *Id.*, Fig. 7, 5:38-45. When the threshold value from curve circuit 24 is less than the feedback signal from error amplifier 25, minimum circuit 26 passes the threshold value from curve circuit 24 to comparator 23. *See* Ex. 1004, 5:46-50, Fig. 7. Based on a comparison of switch current and the threshold from curve circuit 24, comparator 23 outputs a power limit signal that determines when to reset the switching control latch to turn off switch S1. *Id.*, 5:26-33, 5:46-50, Fig. 7.

91. Power is equal to voltage times current. Thus, by limiting the input current through switch S1 as a function of the input line voltage, Mobers limits the

amount of power passed from the input to the output of the converter. *Id.*, 5:34-50, Fig. 7; *see also id.*, Abstract.

92. Accordingly, Mobers discloses each limitation of claim element 1[d].

93. I have reviewed Patent Owner's infringement contentions for the '871 Patent in the Delaware Litigation. *See* Ex. 1012. I note that the mapping of claim element 1[d] to the Mobers prior art is analogous to Patent Owner's mapping in its infringement contentions for the Delaware Litigation.[14] *See* Ex. 1012, 8-9. Specifically, Patent Owner alleged that the accused product "includes a power limiter that implements over power protection ('OPP') that reduces the peak current set point of the switching control in response to sensing the signal representative of the input voltage … ." *Id.*, 8. Moreover, Patent Owner alleged that the accused device includes a "power limit signal" at the output of a comparator, which is similarly situated to comparator 23 in Mobers to reset a PWM latch. *Id.*, 9. Thus, Mobers discloses claim element 1[d] in the same manner as compared to Patent Owner's alleged mapping of the products accused in the Delaware Litigation.

[1d] a power limiter coupled to the sensor to	*See* citations for claim elements 1[b]-[c]. Ex. 1004, Abstract: "The present invention relates to a switched-mode power supply comprising a transformer (T1)

[14] The claim element labeled 1[d] herein is labeled as claim element 1[e] in Patent Owner's infringement contentions. Ex. 1012, 8-9.

output a power limit signal to the switching control in response to the line input voltage of the power converter, wherein the switching control is further coupled to switch the power switch to regulate the output of the power converter in response to the power limit signal.	having an additional control winding (N2). This control winding (N2) forms part of an over power protection system by providing information relating to the line voltage V_{line}." Ex. 1004, 3:60-62: "This control winding forms part of an over power protection system by providing information relating to the line voltage V_{line}." Ex. 1004, 5:5-10: "Hence by monitoring the voltage in control winding 13 in a time phased way, not only V_{out} can be monitored in order to provide over voltage protection in the secondary circuit 2, but also V_{line} can be monitored in order to provide over power protection by operating the gate driving circuit in an appropriate way." Ex. 1004, 5:26-33: "Referring now to FIG. 7, the switch S1 is controlled by a PWM signal from a PWM circuit. The switch is switched on by the set signal from the oscillator 21. The switch is switched off if a certain peak current through S1 is sensed. As previously mentioned, the peak current through S1 is sensed by sensing the voltage generated across R2. This sensed voltage is provided through pin 22a. As soon as the comparator 23 trips, S1 is switched off." Ex. 1004, 5:46-55: "The information from the over power protection circuit can reduce the peak current if the output signal is lower than the signal from the error amplifier 25 on pin 22 b. The magnitude of both signals is sensed by the minimum (min.) circuit 26. As previously mentioned the information relating to V_{line} will be present on the control winding N2 during the primary stroke, whereas information relating to the output voltage V_{out} will be present during the secondary stroke. Therefore, the very same pin on the IC can be used for obtaining both types of information." Ex. 1004, 3:6-17: "The switched-mode power supply according to the first aspect of the present invention may further comprise a control circuit for controlling the controllable current switching means. The control circuit may comprise a PWM-circuit operating the switch at a frequency between 25-250 kHz. The control circuit typically response to a control signal from the third winding. This control signal may comprise a information relating to the

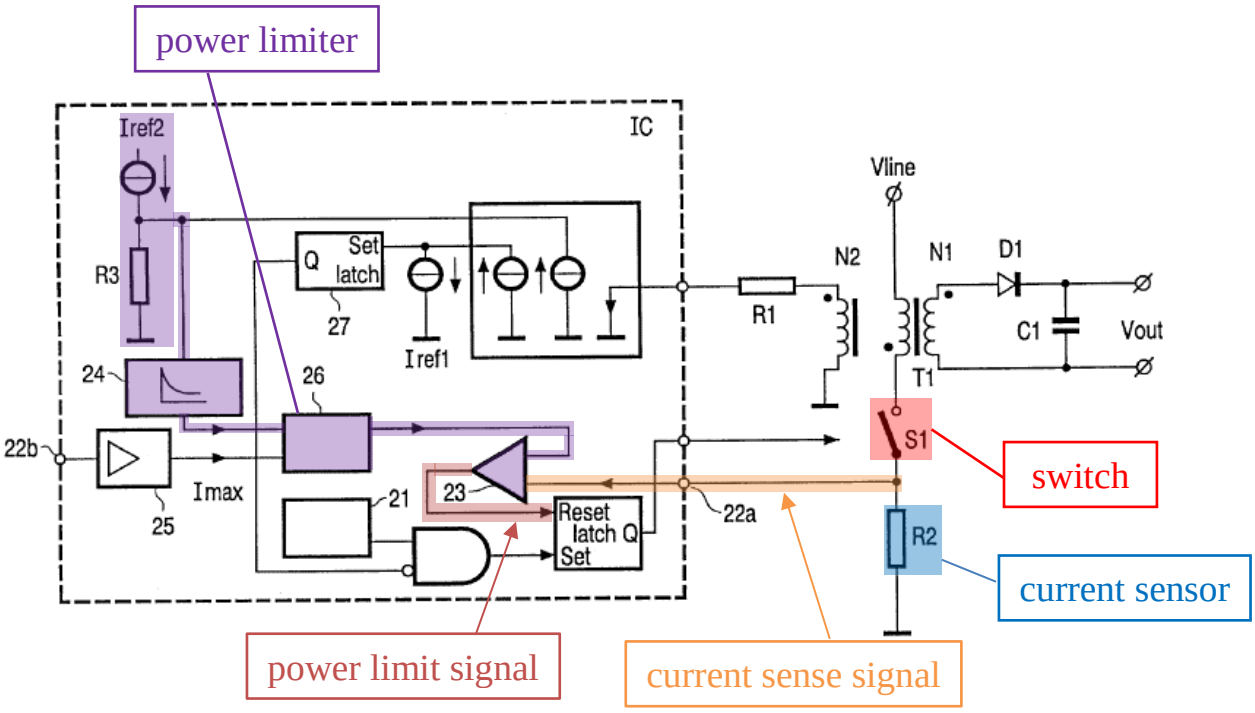
	performance or status of the switched mode power supply. Preferably, the control signal relates to the input voltage to the power supply in the first period of time. In the second period of time the control signal relates to the output voltage of the power supply." Ex. 1004, 4:37-44: "The output voltage of the switched power supply, V_{out}, is controlled by controlling the current in the primary circuit I_p. I_p is controlled by operating switch 16 in a time phased way using a driving circuit (not shown). I_p is sensed by measuring the voltage generated across resistor 5. The measured voltage is used as a control signal to the gate driving circuit (not shown), which—in response the control signal—controls the conduction time of switch 16." *See* citations to Mobers in Section IV.A. *See also* Ex. 1004, Abstract, 2:51-61, 3:58-62, 5:5-10, 5:34-55; 5:63-6:3; Figs. 6-8; Claims 1, 3, 9-11.

(ii) Claim 2

a) 2[a]: "The controller of claim 1, wherein the power limiter is further coupled to receive a current sense signal from a current sensor, wherein the current sense signal is generated in response to a switch current in the power switch,"

94. Mobers discloses that the over power protection circuit (i.e., the power limiter) is further coupled to receive a current sense signal from resistor R2 (i.e., the current sensor), as shown in Figure 7. Ex. 1004, 5:34-45, Fig. 7. Because resistor R2 (i.e., the current sensor) is coupled in series with switch S1 (i.e., the power switch), the voltage generated across resistor R2 is indicative of the switch current, and therefore serves as a current sense signal. *Id.*, 5:26-33, Fig. 7. Indeed, "the peak current through S1 is sensed by sensing the voltage across R2. This

sensed voltage is provided through pin 22a. As soon as the comparator 23 trips, S1 is switched off." *Id.*, 5:30-33.



Ex. 1004, Fig. 7 (annotations added).

95. As described directly above, resistor R2 (i.e., the current sensor) in Mobers is coupled in series with switch S1, and thus generates voltage that is indicative of the current through switch S1. This is similar to the description of a switch current sensor in the '871 Patent itself: "Any of the many know (sic) ways to measure switch current I_{SWITCH} 135, such as for example a current transformer, or the ***voltage across a discrete resistor***, or the voltage across a transistor when the transistor is conducting, may be implemented with current sensor 224." Ex. 1001, 5:52-56 (emphasis added).

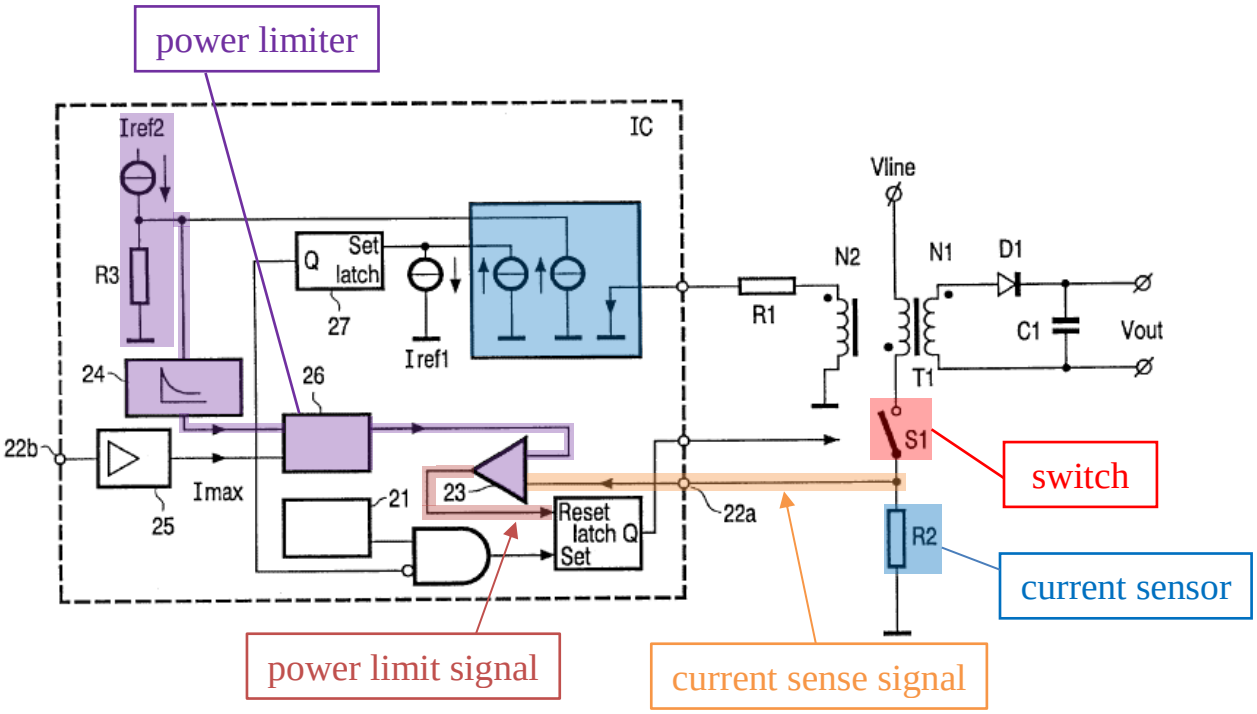
96. Accordingly, Mobers discloses each limitation of claim element 2[a].

2[a]. The controller of claim 1, wherein the power limiter is further coupled to receive a current sense signal from a current sensor, wherein the current sense signal is generated in response to a switch current in the power switch,	*See* citations for Claim 1. Ex. 1004, 3:26-32: "Preferably, the controllable current switching means is connected in series with the primary winding of the transformer. In order to determine the current flowing in this circuit a resistor is included within the circuit so that the current may be determined by measuring the voltage generated across this resistor." Ex. 1004, 4:37-44: "The output voltage of the switched power supply, V_{out}, is controlled by controlling the current in the primary circuit I_p. I_p is controlled by operating switch 16 in a time phased way using a driving circuit (not shown [in FIG. 6]). I_p, is sensed by measuring the voltage generated across resistor 5. The measured voltage is used as a control signal to the gate driving circuit (not shown [in FIG. 6]), which—in response the control signal—controls the conduction time of switch 16." Ex. 1004, 5:26-33: "Referring now to FIG. 7, the switch S1 is controlled by a PWM signal from a PWM circuit. The switch is switched on by the set signal from the oscillator 21. The switch is switched off if a certain peak current through S1 is sensed. As previously mentioned, the peak current through S1 is sensed by sensing the voltage generated across R2. This sensed voltage is provided through pin 22a. As soon as the comparator 23 trips, S1 is switched off." *See also* Ex. 1004, 3:21-25, 4:52-5:4, Figs. 6-8.

b) 2[b]: "wherein the power limiter is further coupled to output the power limit signal in response to the current sense signal."

97. Mobers discloses that the power limiter is further coupled to output the power limit signal in response to the current sense signal. As described with reference to Figure 7, "the peak current through S1 is sensed by sensing the voltage

across R2. This sensed voltage is provided through pin 22a. As soon as the comparator 23 trips, S1 is switched off." Ex. 1004, 5:30-33.



Ex. 1004, Fig. 7 (annotations added). As shown in Figure 7, comparator 23 compares the current sense signal detected across R2. If the current sense signal exceeds the peak current determined by the power limiter, comparator 23 sends the power limit signal to the switching control to turn off switch S1.

98. Accordingly, Mobers discloses each limitation of claim element 2[b].

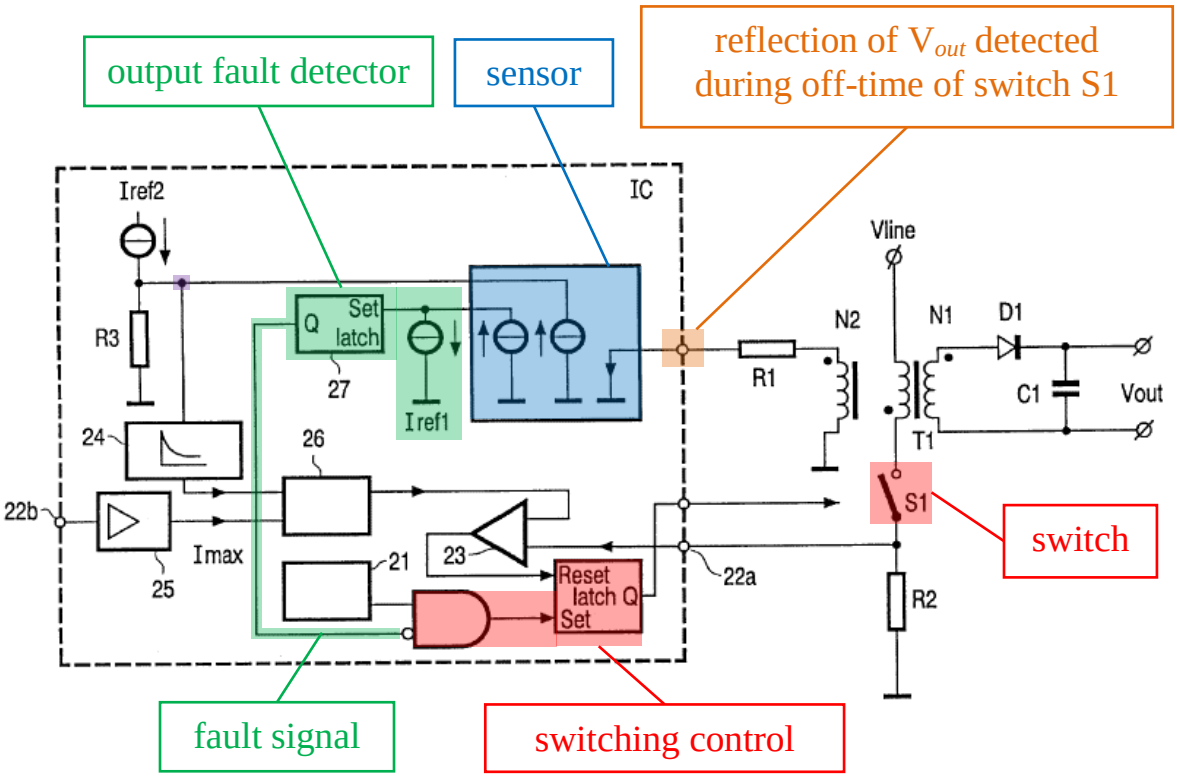
[2b] wherein the power limiter is further coupled to output the power limit signal in response to the current sense signal.	*See* citations for Claim 1. Ex. 1004, 5:26-33: "Referring now to FIG. 7, the switch S1 is controlled by a PWM signal from a PWM circuit. The switch is switched on by the set signal from the oscillator 21. The switch is switched off if a certain peak current through S1 is sensed. As previously mentioned, the peak current through S1 is sensed by sensing the voltage

	generated across R2. This sensed voltage is provided through pin 22a. As soon as the comparator 23 trips, S1 is switched off." (emphasis added). Ex. 1004, 5:34-52: "Besides the input signal from 22a, also a signal from the over power protection circuit is used to determine the peak current through S1 and R2. For this purpose the information relating to V_{line} is used. This information is retrieved from the control winding N2 of the transformer. The V_{line} information is processed in the 'curve' circuit 24. The processor is a multiplier that transforms the input signal into the square root of the signal. The square root is taken, because for this system the optimum compensation will be made. Alternatively, a linear function will also do, but then the maximum output power still has quite some Vline dependence. The information from the over power protection circuit can reduce the peak current if the output signal is lower than the signal from the error amplifier 25 on pin 22b. The magnitude of both signals is sensed by the minimum (min.) circuit 26. As previously mentioned the information relating to V_{line} will be present on the control winding N2 during the primary stroke … ." *See* citations for claim element 2[a]. *See also* Ex. 1004, 3:14-17, 3:26-32, 4:37-44, 5:34-45, 5:63-6:3, Figs. 6-8.

(iii) Claim 3

a) "3. The controller of claim 1 further comprising an output fault detector coupled between the sensor and the switching control, wherein the output fault detector is coupled to detect a fault condition in response to the signal representative of the output voltage of the power converter and to output a fault signal to the switching control in response to the detection of the fault condition."

99. Mobers discloses an over voltage protection circuit (i.e., an output fault detector) coupled between the sensor and the switching control latch:



Id., Fig. 7 (annotations added); *see also id.*, Ex. 1004, 4:52-5:5, 5:56-62.

100. As shown in Figure 7, the sensor monitors the current from resistor R1, which represents V_{out} during at least a portion of the off-time of the switch.

Ex. 1004, 5:50-53. The sensor reproduces the current representative of V_{out} for comparison to a reference "Iref1." Ex. 1004, Fig. 7. If the current signal representing V_{out} exceeds "Iref1," then an output over voltage condition is detected and latch 27 is set. *See id.* The reference "Iref1" and latch 27 thus serve as an output fault detector. If an over voltage condition is detected, latch 27 sends a signal (i.e., a fault signal) to the logic gate shown in Figure 7 between oscillator 21 and the switching control latch. *See* Ex. 1004, Fig. 7. In turn, the logic gate[15] (which is also part of the switching control) blocks pulses from oscillator 21 to the switching control latch, thereby preventing the switching control latch from turning on switch S1 when an output over voltage fault condition is detected. *See id.*, Fig. 7, 5:57-62 ("If it is determined that V_{out} comes above a predetermined level a latch is set in circuit 27. This latch prevents switch S1 from switching on again so as to shut down the switched-mode power supply in case of an over voltage being present on the output terminals.").

101. Accordingly, Mobers discloses each limitation of Claim 3.

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[15] The logic gate in Figure 7 is an AND gate. The circle at the input of the AND gate indicates that the lower input of the AND gate is inverted. Ex. 1014, 28, 33. Thus, when latch 27 provides a high signal, the inverted input of the AND gate will go low, and any pulses from oscillator 21 to the switching control latch will be blocked.

3. The controller of claim 1 further comprising an output fault detector coupled between the sensor and the switching control, wherein the output fault detector is coupled to detect a fault condition in response to the signal representative of the output voltage of the power converter and to output a fault signal to the switching control in response to the detection of the fault condition.	*See* citations for Claim 1. Ex. 1004, 2:51-53: "Advantageously, an integrated circuit is provided with an integrated over voltage and over power protection circuit without the use of additional die demanding external components." Ex. 1004, 3:58-67: "In its simplest form, the present invention provides a switched-mode power supply comprising a transformer having a control winding. This control winding forms part of an over power protection system by providing information relating to the line voltage V_{line}. Additionally, the control winding forms part of an over voltage protection system by monitoring the output voltage V_{out} of the switched-mode power supply. As it will be explained in further details 65 below, the sensing of V_{line}, and the monitoring of V_{out} is performed in a time phased way." Ex. 1004, 5:56-62: "As previously mentioned, information relating to V_{out} is available during the secondary stroke. If it is determined that V_{out} comes above a predetermined level a latch is set in circuit 27. This latch prevents switch S1 from switching on again so as to shut down the switched-mode power supply in case of an over voltage being present on the output terminals." Ex. 1004, 5:63-6:3: "An implementation of the switched power supply according to the present invention is shown in FIG. 8. The over voltage protection circuit is block 17 whereas block 15 and 18 in combination forms the over power protection circuit. Terminal 28 is to be connected to the left leg of resistor R1 in FIG. 7. It will be evident for the skilled person in the art that there are several ways of implementing the over voltage protection circuit and the over power protection circuit." *See also* Ex. 1004, Abstract, 2:51-53, 5:50-55, Figs. 6-8.

(iv) Claim 6

a) "6. The controller of claim 3 wherein the output fault detector is coupled to detect an output over voltage fault condition in response to the signal representative of the output voltage of the power converter."

102. As described above for Claim 3, the fault condition that the output fault detector in Mobers is coupled to detect is an output over voltage fault condition. *See supra* Section VI.A.iii, Claim 3; *see also* Ex. 1004, 5:56-62, 3:62-65. Accordingly, Mobers discloses each limitation of Claim 6.

6. The controller of claim 3 wherein the output fault detector is coupled to detect an output over voltage fault condition in response to the signal representative of the output voltage of the power converter.	*See* citations for Claims 1 and 3. Ex. 1004, 5:56-62: "As previously mentioned, information relating to V_{out}. is available during the secondary stroke. If it is determined that V_{out} comes above a predetermined level a latch is set in circuit 27. This latch prevents switch S1 from switching on again so as to shut down the switched-mode power supply in case of an over voltage being present on the output terminals." Ex. 1004, 3:58-67: "[T]he present invention provides a switched-mode power supply comprising a transformer having a control winding. … [T]he control winding forms part of an over voltage protection system by monitoring the output voltage V_{out} of the switched-mode power supply. As it will be explained in further details 65 below, the sensing of V_{line}, and the monitoring of V_{out}. is performed in a time phased way." (emphasis added). Ex. 1004, 5:63-6:3: "An implementation of the switched power supply according to the present invention is shown in FIG. 8. The over voltage protection circuit is block 17 whereas block 15 and 18 in combination forms the over power protection circuit. Terminal 28 is to be connected to the left leg of resistor R1 in FIG. 7. It will be evident for the skilled person in the art that there are several ways of implementing the over voltage protection circuit and the over

	power protection circuit." Ex. 1004, 2:51-53: "Advantageously, an integrated circuit is provided with an integrated over voltage and over power protection circuit without the use of additional die demanding external components." *See also* Ex. 1004, Abstract, 2:51-53, 5:50-55, Figs. 6-8.

(v) Claims 8, 12, 14, and 15

103. Claims 8, 12, 14, and 15 collectively include similar subject matter as recited in Claims 1, 2, 3, and 6 (albeit with a different ordering of the elements). Thus, according to the following mapping, Claims 8, 12, 14, and 15 are disclosed in the same manner as I described above for Claims 1, 2, 3, and 6.

104. Claim elements 8[pre],[16] [a], and [c] are identical to claim elements 1[pre], [a], and [c]. Further, claim element 8[b] is identical to claim element 1[b], aside from the addition of "at least" prior to the common phrase "a portion of an on time of the power switch." In my opinion, this slight difference does not narrow the scope of claim element 8[b] relative to claim element 1[b]. In addition, claim element 8[d] recites the same subject matter as Claim 3. Thus, Claim 8 is disclosed by Mobers in the same manner as described above for Claims 1 and 3.

105. Moreover, dependent Claims 12, 14, and 15 recite the same subject matter as Claim 6, claim element 1[d], and Claim 2, respectively. Thus, dependent

[16] The preamble is not limiting in my opinion, but is nonetheless disclosed by Mobers.

Claims 12, 14, and 15 are disclosed by Mobers in the same manner as described above.

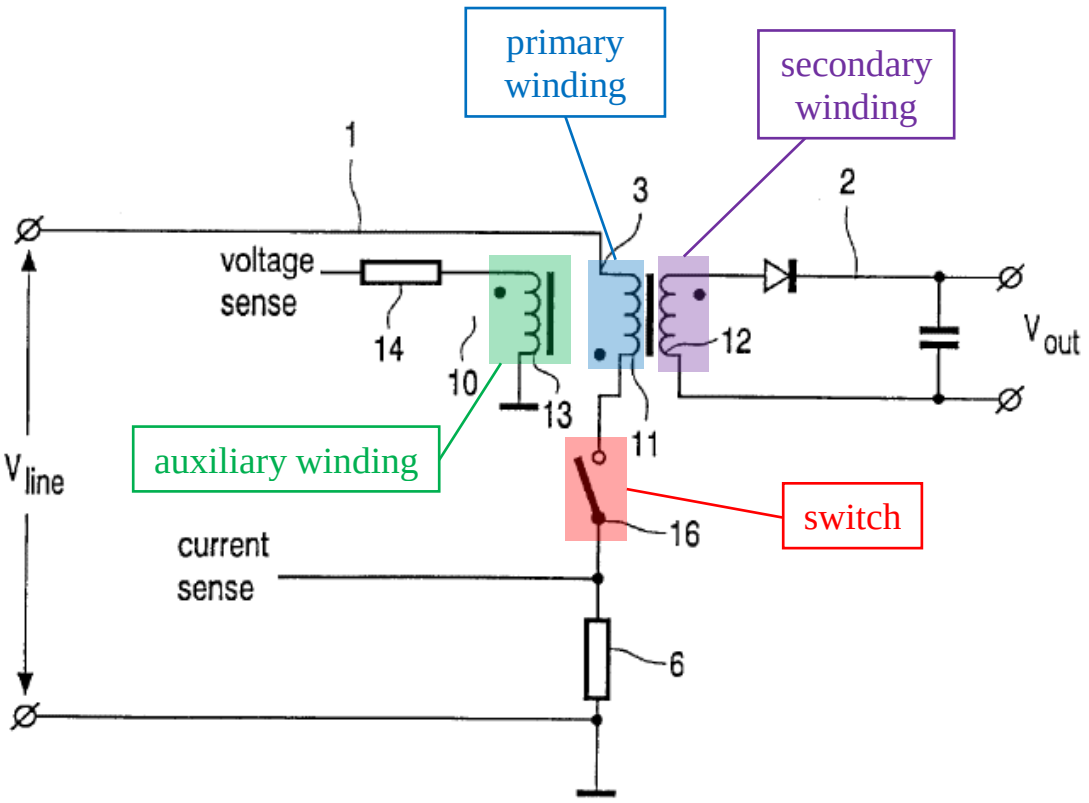
8[pre]. A controller for use in a power converter, comprising:	*See* Section VI.A.i, Claim 1[pre].
[8a] a sensor coupled to receive a signal from a single terminal of the controller,	*See* Section VI.A.i, Claim 1[a].
[8b] the signal from the single terminal to represent an output voltage of the power converter during at least a portion of an off time of the power switch, the signal from the single terminal to represent a line input voltage during at least a portion of an on time of the power switch,	*See* Section VI.A.i, Claim 1[b].
[8c] a switching control to be coupled to switch the power switch to regulate an output of the power converter in response to the sensor; and	*See* Section V.A.i, Claim 1[c].
[8d] an output fault detector coupled between the sensor and the switching control, wherein the output fault detector is coupled to detect a fault condition in response to the signal representative of the output voltage of the power converter and to output a fault signal to the switching control in response to the detection of the fault condition.	*See* Section VI.A.iii, Claim 3.
12. The controller of claim 8 wherein the output fault detector is coupled to detect an output over voltage fault condition in response to the signal representative of the output voltage of the power converter.	*See* Section VI.A.iv, Claim 6.
14. The controller of claim 8 further comprising a power limiter coupled between the sensor and the switching control, the power limiter coupled to output a power limit signal to the switching control in response to the signal representative of line input voltage of the power converter, wherein the a switching control is further coupled to switch the power switch to regulate the output of the power converter in response to the power limit signal.	*See* Section VI.A.i, Claim 1[d].

15. The controller of claim 14, wherein the power limiter is further coupled to receive a current sense signal from a current sensor, wherein the current sense signal is generated in response to a switch current in the power switch, wherein the power limiter is further coupled to output the power limit signal in response to the current sense signal.	*See* Section VI.A.ii, Claim 2.

B. Ground 2: Mobers Renders Claims 1-3, 6, 8, 12, 14, and 15 Obvious

106. Mobers, combined with the knowledge of a POSITA, discloses and suggests each element of Claims 1-3, 6, 8, 12, 14, and 15, and thus renders Claims 1-3, 6, 8, 12, 14, and 15 obvious.

107. Mobers discloses a flyback-type switching power converter that utilizes a transformer with an auxiliary winding, which is referred to by Mobers as a "control winding." Ex. 1004, 4:1-28, Fig. 6. Figure 6 illustrates certain components of the switching power converter:



Ex. 1004, Fig. 6 (annotations added).

108. In one section, Mobers states that "the control voltage generated across the control winding 13 is related to V_{line} during the conduction time (primary stroke)" (i.e., the on-time of switch 16), and is "related to V_{line} during the non-conduction time (secondary stroke)" (i.e., the off-time of switch 16). Ex. 1004, 5:10-13 (bold emphasis added). This snippet of text refers to "V_{line}" twice. However, the second instance of "V_{line}" in column 5, lines 10-13 appears to be a typographical error that should instead be "V_{out}."

109. As explained in Sections III.A-C, a POSITA would understand that an auxiliary winding in a flyback switching power converter naturally reflects the

voltage present on the secondary winding (i.e., Vout plus the voltage drop of the rectifier) when current flows through the secondary side (i.e., during off-time of the switch). Ex. 1006, 3:4-15; Ex. 1008, 7:31-43. Moreover, other portions of Mobers clarify that "the information relating to V_{line} will be present on the control winding N2 during the primary stroke, whereas information relating to the output voltage V_{out} will be present during the secondary stroke." Ex. 1004, 5:50-53; *see also id.*, 4:52-5:5.

110. Thus, in my opinion, regardless of the misstatement in Mobers column 5, lines 10-13, a POSITA would understand that Mobers discloses and suggests the sensing of both the output voltage and the line input voltage via a single terminal of a controller IC at different times during the switching cycle. *See* Ex. 1004, 5:50-53, Figs. 6-7. Moreover, Mobers discloses and suggests every other limitation of Claims 1-3, 6, 8, 12, 14, and 15 of the '871 Patent according to the mapping provided in Sections VI.A. Therefore, Mobers renders Claims 1-3, 6, 8, 12, 14, and 15 obvious to a person of ordinary skill in the art.

C. Ground 3: Mobers Renders Claim 11 Obvious

111. Mobers, combined with the knowledge of a POSITA, discloses and suggests each element of Claim 11, and thus renders Claim 11 obvious.

(i) Claim 11

a) "11. The controller of claim 8 wherein the output fault detector is coupled to detect an open loop condition fault condition in response to the signal representative of the output voltage of the power converter."

112. Claim 11 depends from Claim 8[17] and further recites: "wherein the output fault detector is coupled to detect an open loop condition fault condition in response to the signal representative of the output voltage of the power converter." Ex 1001, Claim 11 (emphasis added). As noted above, I have reviewed the '871 Patent in detail. The '871 specification does not define what is meant by an "open loop condition fault condition," or provide any examples of and open loop fault condition. However, a POSITA would understand that an open loop fault condition occurs when the feedback path from the output of the power supply to the control circuitry is broken. In other words, the normal closed-loop control is "opened" by a break in the feedback from the output of the power converter to the control circuitry. *See, e.g.,* Ex. 1020, 10 ("[T]he output of the switcher will go high if the ***feedback loop is opened***." (emphasis added)).

113. Because the feedback loop is broken, the control circuitry falsely detects that no voltage is present on the output of the power supply. The control circuitry therefore attempts to provide more power to the output of the power

[17] As discussed above in Section VI.A.v (which in turn points to Sections VI.A.i and VI.A.iii), Mobers discloses each limitation of Claim 8.

supply. This additional power, in turn, causes an over voltage fault condition on the output. Ex. 1020, 10 ("[T]he output of the switcher will go high if the feedback loop is opened."); Ex. 1017, 4:53-62 (describing "conventional open loop protection circuit" configured "to prevent any overvoltage" if feedback line is broken); Ex. 1018, 1:16-19 (referring to "an over-high output voltage during the period of feedback open loop"); Ex. 1019, 1:26-31 (describing a regulator circuit that responds to an "open loop condition on the feedback" by "delivering maximum power" to the output).

114. In other words, an output over voltage fault condition may be a symptom of an open loop fault condition. Indeed, the background of Mobers itself refers to an output over voltage condition caused by broken feedback loop. Ex. 1004, 2:41-44 ("In case such a loop is broken no information relating to the output voltage is available, and thus, no protection against damages due to over voltage on the secondary circuit is available."). Thus, as would be readily recognized by a POSITA, a circuit for detecting an output over voltage fault condition also detects the open loop condition that causes the output over voltage in the first place.

115. Mobers discloses terminal 22b coupled to error amplifier 25, which in turn is coupled to comparator 23 via minimum circuit 26. Ex. 1004, 5:26-33, 5:46-48, Fig. 7. Error amplifier 25 is configured to receive a feedback signal from the output of the power supply. *Id.*, Fig. 7, 5:26-55. When the error signal is lower

than the output curve circuit 24 in the over power protection circuitry, minimum circuit 26 uses the error signal generated by error amplifier 25 to set the threshold for comparator 23, and thereby the peak current through switch S1. Ex. 1004, 5:26-33, 5:46-48, Fig. 7. Thus, the feedback from pin 22b and error amplifier 25 forms what is commonly known in the art as a current-mode feedback control loop. Ex. 1013, 16-18; *see also* Ex. 1015, 4:49-60.

116. And as described above, a POSITA would understand that an output over voltage fault condition may occur in response to an open loop fault condition in the feedback path. For example, if an open loop condition occurred at feedback pin 22b, the error amplifier 25 would falsely detect a lack of output voltage and cause the control circuitry to provide additional power to the output of the power supply. *See* Ex. 1004, Fig. 7; *see also* Ex. 1020, 10 ("[T]he output of the switcher will go high if the ***feedback loop is opened***." (emphasis added)). This additional power, in turn, would cause an output over voltage condition.

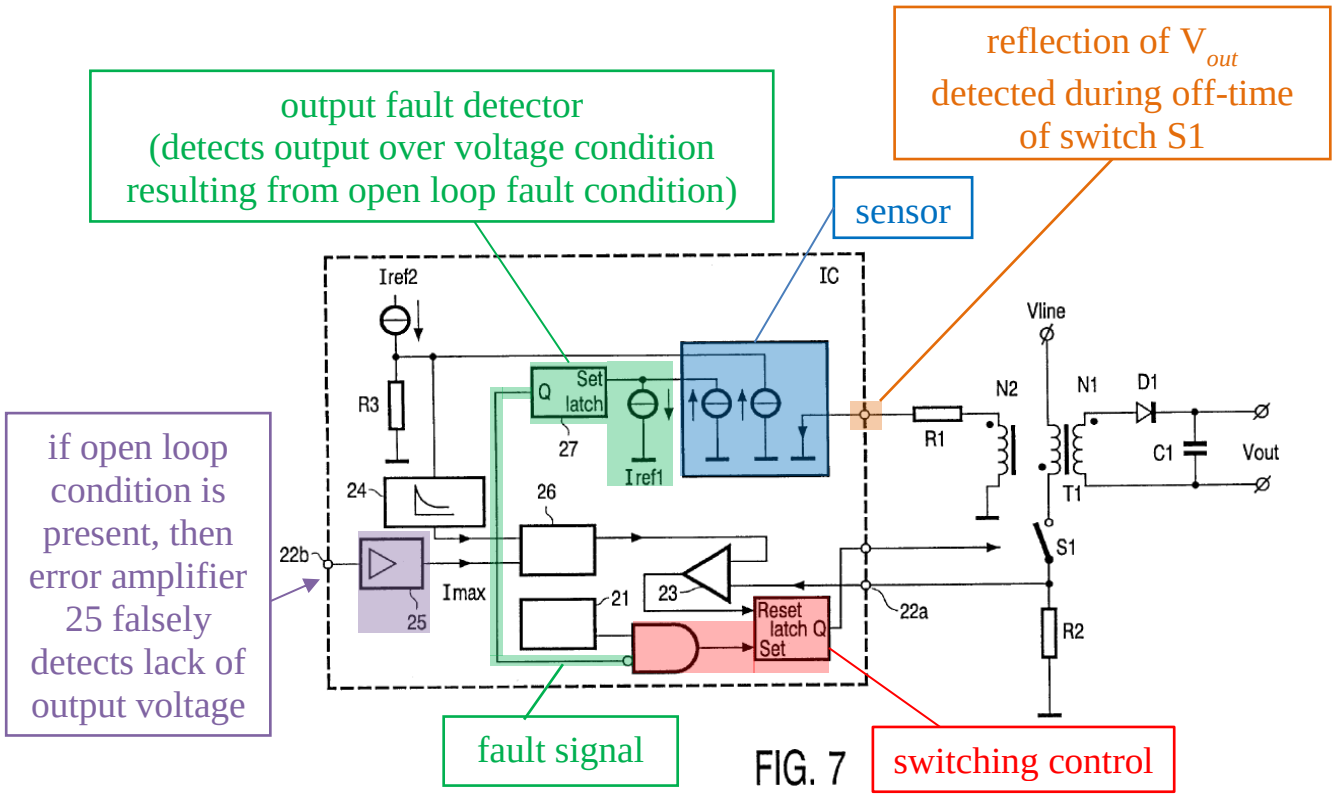


FIG. 7

Ex. 1004, Fig. 7 (annotations added).

117. As described above for Claim 12, Mobers discloses that the output fault detector is coupled to detect an output over voltage fault condition via the control winding N2. *See supra* Section VI.A.v (which in turn points to Section VI.A.iv, Claim 6). Thus, a POSITA would recognize that in the event of an open loop condition (in the feedback path including error amplifier 25), Mobers's output fault detector would detect the open loop condition by detecting the resulting over voltage condition via the control winding.[18]

[18] Notably, the over power protection system in Mobers would *not* prevent the control circuitry from providing additional power to the output of the power supply

Accordingly, the circuitry disclosed by Mobers, combined with the knowledge of a POSITA, discloses and suggests each limitation of Claim 11.

11. The controller of claim 8 wherein the output fault detector is coupled to detect an open loop condition fault condition in response to the signal representative of the output voltage of the power converter.	*See* citations in Section VI.A.v, Claim 12 (citing Section VI.A.iv, Claim 6). Ex. 1004, 2:38-44: "It is a further disadvantage of the prior art power supplies shown in FIGS. 1 and 5 that in order to obtain information relating to the output voltage a separate feedback loop/control loop must be implemented. In case such a loop is broken no information relating to the output voltage is available, and thus, no protection against damages due to over voltage on the secondary circuit is available." Ex. 1004, 5:56-62: "As previously mentioned, information relating to V_{out}. is available during the secondary stroke. If it is determined that V_{out} comes above a predetermined level a latch is set in circuit 27. This latch prevents switch S1 from switching on again so as to shut down the switched-mode power supply in case of an over voltage being present on the output

and thereby causing an output over voltage fault in response to the open loop fault condition. First, the over power protection scheme in Mobers keys off the line voltage information. Ex. 1004, 3:58-62. Thus, if the open loop fault condition occurred when the input line voltage was in the moderate or low range, the over power protection scheme in Mobers would not limit the controller from providing additional power to the output of the power supply. Moreover, an output over voltage may occur when the amount of power provided to the output exceeds the power drawn by the load. Thus, even a moderate amount of power delivered to the output could cause an output over voltage condition if the amount of power drawn from the output by the load is light.

	terminals." Ex. 1004, 3:58-67: "[T]he present invention provides a switched-mode power supply comprising a transformer having a control winding. … [T]he control winding forms part of an over voltage protection system by monitoring the output voltage V_{out} of the switched-mode power supply. As it will be explained in further details 65 below, the sensing of V_{line}, and the monitoring of V_{out}. is performed in a time phased way." (emphasis added).

VII. CONCLUSION

118. All statements made herein of my own knowledge are true, and all statements made on information and belief are believed to be true. I further understand that willful false statements and the like are punishable by fine or imprisonment, or both under Section 1001 of Title 18 of the United States Code. I declare under penalty of perjury that the foregoing is true and correct.

Executed on September 28, 2018.

R. Jacob Baker, Ph.D., P.E.