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Paper 26
Date: January 3, 2020

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE INC.,
Petitioner,

v.

QUALCOMM INCORPORATED,
Patent Owner.

IPR2018-01315
IPR2018-01316
Patent 8,063,674 B2

Before TREVOR M. JEFFERSON, DANIEL J. GALLIGAN, and SCOTT B. HOWARD, *Administrative Patent Judges*.

HOWARD, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

INTRODUCTION

In these *inter* partes reviews, instituted pursuant to 35 U.S.C. § 314, Apple Inc. ("Petitioner") challenges claims 1, 2, 5–9, 12, 13, and 16–22 ("the challenged claims") of U.S. Patent No. 8,063,674 B2 (Ex. 1001, "the '674 patent"), owned by Qualcomm Incorporated ("Patent Owner").

As explained in detail below, the references applied against the challenged claims are identical in each of the cases. A joint hearing was held for these cases. The parties rely on the same declarants submitting identical declarations in each case for testimonial evidence. Under these circumstances, we determine that a combined Final Decision will promote a just, speedy, and inexpensive resolution of these proceedings.

The Board has jurisdiction under 35 U.S.C. § 6(b). This Final Written Decision issues pursuant to 35 U.S.C. § 318(a). For the reasons that follow, we determine that Petitioner has shown by a preponderance of the evidence that the challenged claims are unpatentable.

A. IPR2018-01315 Procedural History

Petitioner filed a Petition to institute an *inter partes* review of claims 1, 2, and 5–7 of the '674 patent pursuant to 35 U.S.C. §§ 311–319. Paper 2[1] ("Petition" or "Pet."). Patent Owner filed a Preliminary Response. Paper 6. We instituted an *inter partes* review of claims 1, 2, and 5–7 on all grounds of unpatentability alleged in the Petition. Paper 7 ("Institution Decision" or "Inst. Dec.").

[1] Unless otherwise noted, all citations are to IPR2018-01315. We note that identical exhibits were filed in each of the proceedings.

After institution of trial, Patent Owner filed a Response (Paper 12, "PO Resp."), Petitioner filed a Reply (Paper 16, "Pet. Reply"), and Patent Owner filed a Sur-reply (Paper 19, "PO Sur-reply").

A joint hearing for IPR2018-01315 and IPR2018-01316 was held on October 11, 2019. Paper 25 ("Tr.").

B. IPR2018-01316 Procedural History

Petitioner filed a Petition to institute an *inter partes* review of claims 8, 9, 12, 13, and 16–22 of the '674 patent pursuant to 35 U.S.C. §§ 311–319. IPR2018-01316, Paper 2 ("1316 Pet."). Patent Owner filed a Patent Owner Preliminary Response. IPR2018-01316, Paper 6. We instituted an *inter partes* review of claims 8, 9, 12, 13, and 16–22 on all grounds of unpatentability alleged in the Petition. IPR2018-01318, Paper 7 ("1316 Inst. Dec.").

After institution of trial, Patent Owner filed a Response (IPR2018-01316, Paper 12, "1316 PO Resp."), Petitioner filed a Reply (IPR2018-01316, Paper 16, "1316 Pet. Reply"), and Patent Owner filed a Sur-reply (IPR2018-01316, Paper 19, "1316 PO Sur-reply").

A joint hearing for IPR2018-01315 and IPR2018-01316 was held on October 11, 2019. IPR2018-01316, Paper 25 ("Tr.").

C. Real Party in Interest

Petitioner identified Apple, Inc. as the real party in interest. Pet. 64.

Patent Owner identified Qualcomm Incorporated as the real party in interest. Patent Owner's Mandatory Notices, Paper 3, 2; IPR2018-01315 Patent Owner's Mandatory Notices, Paper 3, 2.

D. Related Proceedings

The parties identified the following patent litigation proceedings in which the '674 patent was asserted: *In re Certain Mobile Electronic Devices and Radio Frequency and Processing Components Thereof* (ITC Inv. No. 337-TA-1093) and *Qualcomm Inc. v. Apple Inc*., Case No. 3:17-cv-02398 (S.D. Cal.). *Id.* at 64–65; Patent Owner's Mandatory Notices, Paper 3, 2.[2]

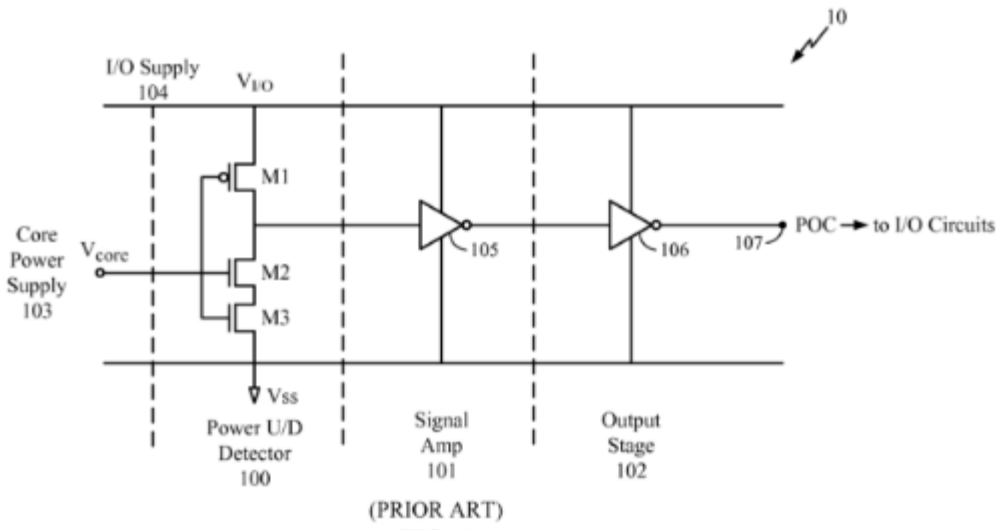
E. The '674 Patent

The '674 patent is titled "Multiple Supply-Voltage Power-Up/Down Detectors." Ex. 1001, code (54). According to the '674 patent, "many newer integrated circuit devices include dual power supplies: one lower-voltage power supply for the internally operating or core applications, and a second higher-voltage power supply for the I/O circuits and devices." *Id*. at 1:22–25.

The '674 patent further states that "[i]n order to facilitate communication between the core and I/O devices, level shifters are employed." *Id*. at 1:28–29. "Because the I/O devices are connected to the core devices through level shifters, problems may occur when the core devices are powered-down." *Id*. at 1:29–32. An example of such a problem described in the '674 patent is how stray currents while the core is powering down can cause the level shifters to "send a signal to the I/O devices for transmission" resulting in the I/O devices "transmit[ting] the erroneous signal into the external environment." *Id*. at 1:34–40.

[2] According to Petitioner, the district court proceeding and the ITC investigation have been dismissed. Petitioner's Updated Mandatory Notices, Paper 15, 1.

One prior art solution identified in the '674 patent is the use of "power-up/down detectors to generate a power-on/off-control (POC) signal internally [which] instructs the I/O devices when the core devices are shut down." Ex. 1001, 1:55–58. Figure 1 of the '674 patent is reproduced below.



(PRIOR ART)
FIG. 1

Figure 1 "is a circuit diagram illustrating a conventional POC system for multiple supply voltage devices" which is identified as being prior art. *Id*. at 4:18–19, Fig. 1.

The '674 patent identifies a number of issues associated with the Figure 1 design. For example, when I/O power supply 104 is on and core power supply 103 is off, powering on the core power supply results in "a period in which all three transistors within power up/down detector 100 are on," resulting in a virtual short "to ground causing a significant amount of current to flow from I/O power supply 104 to ground." Ex. 1001, 2:21–29. "This 'glitch' current consumes unnecessary power." *Id*. at 2:29–30. Although the glitch current can be reduced by reducing the size of transistors M1-M3, such a reduction limits "the actual amount of current that can pass through the transistors" and reduces their switching speeds, which

"translates into less sensitivity in detecting power-up/down of core supply voltage 103 or longer processing time for power-up/down events." *Id*. at 2:31–39; *see also id*. at 2:63–3:11.

According to the '674 patent, these problems can be solved by using "one or more feedback circuits coupled to the up/down detector" that "are configured to provide feedback signals to adjust a current capacity of said up/down detector." Ex. 1001, 3:31–34. An example of such a feedback circuit is shown in Figure 4, reproduced below:

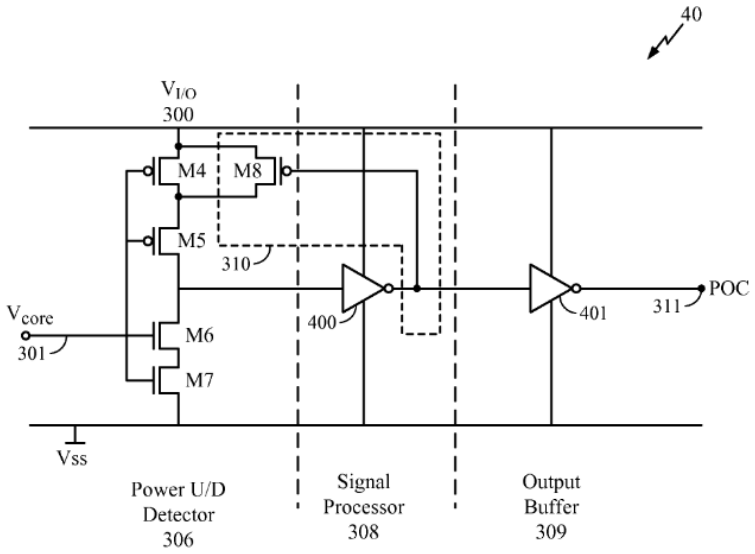


Figure 4 "is a circuit diagram illustrating another POC network configured according to the teachings of the present disclosure." *Id*. at 4:28–30. The '674 patent describes the operation of the feedback circuit in Figure 4 as follows:

> The feedback network 310 comprises a transistor M8 connected in parallel to the transistor M4. The transistor M8 is also configured as a p-type transistor, such that when the feedback signal from the inverting amplifier 400 is high, the transistor M8 is switched off, and when the feedback signal is low, the transistor M8 is switched on. Thus, when the V_{core} 301 is off, producing a high detection signal, the inverting amplifier

> 400 inverts that signal to a logic low which causes the transistor M8 to switch on. As the V_{core} 301 is powered-on, the detection signal changes to a logic low, which changes the feedback signal from the inverting amplifier 400 to a logic high, which, in turn, turns the transistor M8 off. While the transistor M8 is off, the power up/down detector 306 has a decreased current capacity, i.e., smaller current will flow through the transistor M8 because of the amplified low signal. The voltage level caused by the V_{core} 301 on the gate terminals of M4 and M5 could in some glitch or stray signal situations, cause leakage through M4 and M5. Because the feedback signal for the transistor M8 is received from the inverting amplifier 400, when the V_{core} 301 powers-down, the feedback signal will switch quickly from a logic high to a logic low, which will then switch the transistor M8 on. Thus, in the circuit configuration depicted in FIG. 4, the power up/down detector 40 will detect the V_{core} 301 powering down more quickly than the existing POC networks.

Id. at 6:4–28.

F. Illustrative Claim

Petitioner challenges claims 1, 2, and 5–9, 12, 13, and 16–22 of the '674 patent. Pet. 1; 1316 Pet. 1. Claim 1 is independent, is illustrative of the subject matter of the challenged claims, and reads as follows:

> 1. A multiple supply voltage device comprising:
>
> a core network operative at a first supply voltage; and
>
> a control network coupled to said core network wherein said control network is configured to transmit a control signal, said control network comprising: an up/down (up/down) detector configured to detect a power state of said core network; processing circuitry coupled to said up/down detector and configured to generate said control signal based on said power state;
>
> one or more feedback circuits coupled to said up/down detector, said one or more feedback circuits configured to

> provide feedback signals to adjust a current capacity of said up/down detector;
>
> at least one first transistor coupled to a second supply voltage, the at least one more first transistor being configured to switch on when said first supply voltage is powered down and to switch off when said first supply voltage is powered on;
>
> at least one second transistor coupled in series with the at least one first transistor and coupled to said first supply voltage, the at least one second transistor being configured to switch on when said first supply voltage is powered on and to switch off when said first supply voltage is powered down;
>
> at least one third transistor coupled in series between the at least one first transistor and the at least one second transistor.

Ex. 1001, 8:44–9:3 (the '674 patent).

G. Prior Art and Asserted Grounds

Petitioner asserts that claims 1, 2, and 5–9, 12, 13, and 16–22 are unpatentable on the following grounds:

Claims Challenged	35 U.S.C. §	References/Basis
1, 2, 5–9, 12, 13, 16–22	103(a)[3]	Steinacker,[4] Doyle,[5] and Park[6]

[3] The Leahy-Smith America Invents Act ("AIA") included revisions to 35 U.S.C. §§ 102, 103 that became effective on March 16, 2013. Because the '674 patent issued from an application filed before March 16, 2013, we apply the pre-AIA versions of the statutory bases for unpatentability.

[4] Steinacker, US 7,279,943 B2, issued Oct. 9, 2007 (Ex. 1005).

[5] Doyle, US 4,717,836, issued Jan. 5, 1988 (Ex. 1006).

[6] Park, J. C. & Mooney, V. J. (Nov. 2006). Sleepy Stack Leakage Reduction. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 14*(11), 1250–1263 (Ex. 1007).

Claims Challenged	35 U.S.C. §	References/Basis
1, 2, 5, 6, 8, 9, 12, 13, 17–21	103(a)	AAPA,[7] Majcherczak
7, 16, 22	103(a)	AAPA, Majcherczak, Matthews[8]

ANALYSIS

A. Legal Principles

In *Graham v. John Deere Co. of Kansas City*, 383 U.S. 1 (1966), the Supreme Court set out a framework for assessing obviousness under 35 U.S.C. § 103 that requires consideration of four factors: (1) the "level of ordinary skill in the pertinent art," (2) the "scope and content of the prior art," (3) the "differences between the prior art and the claims at issue," and (4) "secondary considerations" of non-obviousness such as "commercial success, long-felt but unsolved needs, failure of others, etc." *Id.* at 17–18. "While the sequence of these questions might be reordered in any particular case," *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 407 (2007), the Federal Circuit has "repeatedly emphasized that an obviousness inquiry requires examination of all four *Graham* factors and that an obviousness determination can be made only after consideration of each factor." *Nike, Inc. v. Adidas AG*, 812 F.3d 1326, 1335 (Fed. Cir. 2016), *overruled on other grounds by Aqua Products, Inc. v. Matal*, 872 F.3d 1290 (Fed. Cir. 2017) (en banc). We note that, with respect to the fourth Graham factor, the parties have not presented argument or evidence directed to secondary

[7] Petitioner identifies Figure 1 and the text at column 1, line 22 through column 2, line 39 of the '674 patent as Applicant Admitted Prior Art. *See* Pet. 37, 43, 46.

[8] Matthews, US 6,646,844 B1, issued Nov. 11, 2003 (Ex. 1009).

considerations of nonobviousness. The analysis below addresses the first three *Graham* factors.

B. Level of Ordinary Skill in the Art

The level of ordinary skill in the art is "a prism or lens" through which we view the prior art and the claimed invention. *Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001). Factors pertinent to a determination of the "level of ordinary skill in the art include (1) educational level of the inventor; (2) type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology; and (6) educational level of workers active in the field." *Envtl. Designs, Ltd. v. Union Oil Co. of Cal.*, 713 F.2d 693, 696–697 (Fed. Cir. 1983) (citing *Orthopedic Equip. Co. v. All Orthopedic Appliances, Inc.*, 707 F.2d 1376, 1381–82 (Fed. Cir. 1983)). Not all such factors may be present in every case, and one or more of these or other factors may predominate in a particular case. *Id.* Moreover, "[t]hese factors are not exhaustive but are merely a guide to determining the level of ordinary skill in the art." *Daiichi Sankyo Co. Ltd, Inc. v. Apotex, Inc.*, 501 F.3d 1254, 1256 (Fed. Cir. 2007).

Dr. Horst testifies that a person having ordinary skill in the art would have had "at least an undergraduate degree in electrical engineering, or a related field, and three years of experience in circuit and system design." Ex. 1003 ¶ 33. Additionally, Dr. Horst testifies that "a person of ordinary skill with less than the amount of experience noted above could have had a correspondingly greater amount of educational training such a graduate degree in a related field." *Id.*

In our Institution Decision, "we adopt[ed] Dr. Horst's definition of the level of ordinary skill in the art, with the exception of the language 'at least' . . . ." Inst. Dec. 13; 1316 Inst. Dec. 13. Patent Owner agrees with our formulation, *see* PO Resp. 9; 1316 PO Resp. 9, and Petitioner did not address it in its Reply. *See generally* Pet. Reply; 1316 Pet. Reply.

Accordingly, we find on the record as a whole that a person of ordinary skill in the art would have an undergraduate degree in electrical engineering, or a related field, and three years of experience in circuit and system design. Additionally, a person of ordinary skill with less than the amount of experience noted above could have had a correspondingly greater amount of educational training such a graduate degree in a related field.

C. Claim Construction

In this *inter partes* review, we construe claim terms in an unexpired patent according to their broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b) (2018).[9] "Under a broadest reasonable interpretation, words of the claim must be given their plain meaning, unless such meaning is inconsistent with the specification and prosecution history." *Trivascular, Inc. v. Samuels*, 812 F.3d 1056, 1062 (Fed. Cir. 2016). In addition, the Board may not "construe claims during [an *inter partes* review] so broadly that its constructions are unreasonable under general claim construction principles." *Microsoft Corp.*

[9] We apply the district court claim construction standard to petitions filed on or after November 13, 2018. *See Changes to the Claim Construction Standard for Interpreting Claims in Trial Proceedings Before the Patent Trial and Appeal Board*, 83 Fed. Reg. 51340 (Oct. 11, 2018) (to be codified at 37 C.F.R. pt. 42). Because Petitioner filed its petitions before November 13, 2018 (*see* Pet.; 1316 Pet.), we apply the BRI standard.

v. Proxyconn, Inc., 789 F.3d 1292, 1298 (Fed. Cir. 2015) (emphasis omitted), *overruled on other grounds by Aqua Products, Inc. v. Matal*, 872 F.3d 1290 (Fed. Cir. 2017) (en banc). An inventor may provide a meaning for a term that is different from its ordinary meaning by defining the term in the specification with reasonable clarity, deliberateness, and precision. *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994).

Use of the word *means* in a claim gives rise to a rebuttable presumption that 35 U.S.C. § 112, sixth paragraph, analysis applies to interpret the claim. *Williamson v. Citrix Online, LLC,* 792 F.3d 1339, 1348 (Fed. Cir. 2015). Construing a means-plus-function claim term is a two-step process, wherein we first identify the claimed function and then determine what structure, if any, disclosed in the specification corresponds to the claimed function. *Id.* at 1348–51. Our rules specifically require that a petition for *inter partes* review identify how each challenged claim is to be construed, including identification of the corresponding structure for means-plus-function limitations. *See* 37 C.F.R. § 42.104(b)(3) (2017) ("Where the claim to be construed contains a means-plus-function . . . limitation as permitted under 35 U.S.C. 112[(6)], the construction of the claim must identify the specific portions of the specification that describe the structure, material, or acts corresponding to each claimed function.").[10] "[S]tructure disclosed in the specification is 'corresponding' structure only if the specification or prosecution history clearly links or associates that structure

[10] 37 C.F.R. § 42.104(b)(3) refers to § 112(f). Section 4(c) of the AIA redesignated 35 U.S.C. § 112, sixth paragraph as 35 U.S.C. § 112(f). Because the '674 patent has a filing date before the effective date of this provision of the AIA, we use the citation § 112, sixth paragraph.

to the function recited in the claim." *Med. Instrumentation & Diagnostics Corp. v. Elekta AB*, 344 F.3d 1205, 1210 (Fed. Cir. 2003) (quoting *B. Braun Med. Inc. v. Abbott Labs.*, 124 F.3d 1419, 1424 (Fed. Cir. 1997)).

Petitioner proposes a claim construction for "processing circuitry." Pet. 10; 1316 Pet. 5. Petitioner also contends that the claims contain several means-plus-function limitations. 1316 Pet. 6–9.

Patent Owner does not believe the term "processing circuitry" or the means-plus-function limitations need to be construed. PO Resp. 8; 1316 PO Resp. 8–9.

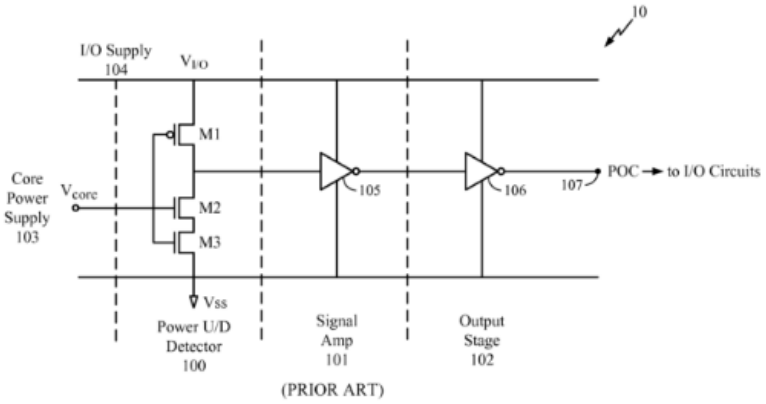
Having considered the evidence presented, we conclude that, with the exception of the means-plus-function limitations, no express claim construction of any term is necessary. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (stating that "we need only construe those claim limitations 'that are in controversy, and only to the extent necessary to resolve the controversy'" (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

With regard to the means-plus-function limitations, we are persuaded by Petitioner's identification of both the function set forth in the claim and the structure in the written description that is linked to the function, and adopt them as our own. *See* 1316 Pet. 6–9.

D. Obviousness over AAPA in View of Majcherczak

1. Overview of AAPA

The '674 patent describes a prior art "power-up/down detector[] to generate a power-on/off-control (POC) signal internally." Ex. 1001, 1:55–57, Fig. 1. The prior art design is shown in Figure 1, reproduced below.



(PRIOR ART)
FIG. 1

Id. at Fig. 1. "FIG. 1 is a circuit diagram illustrating a conventional POC system for multiple supply voltage devices" and is identified as prior art. *Id*. at 4:18–19, Fig. 1. According to the '674 patent, the POC "is made up of three functional blocks: power-up/down detector 100, signal amplifier 101, and output stage 102. Power-up/down detector 100 has PMOS transistor M1 and NMOS transistors M2-M3." *Id*. at 1:60–63.

2. Overview of Majcherczak

Majcherczak is titled "Power Supply Detection Device" and relates "to a power supply detection device for an integrated circuit using at least two power supply voltages." Ex. 1008, code (54), ¶ 1. Majcherczak describes a voltage detection device that detects when the core voltage is powered down or there is an excessively slow build-up of the voltage. Ex. 1008, code (57), ¶¶ 8–11.

Figure 2 of Majcherczak is shown below.

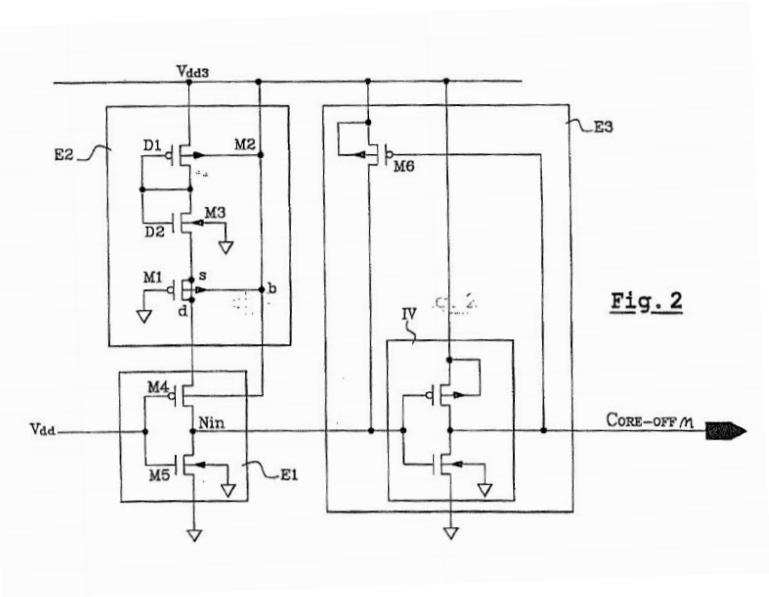


Figure 2 shows a detection device "compris[ing] an output stage E3 following the input stage E1, to obtain the desired output levels for the inverse detection signal $C_{ORE\text{-}OFFn}$." Ex. 1008, ¶¶ 35–37.

3. Using Applicant Admitted Prior Art During an Inter Partes *Review*

a. Patent Owner's Arguments

Patent Owner argues that the grounds based on AAPA "are improper because the America Invents Act (AIA) does not permit *inter partes* review based on so-called [AAPA]." PO Resp. 17; *see also id.* at 17–20; PO Sur-reply 1–2.[11] Specifically, Patent Owner argues that "that *inter partes* review be available 'only on the basis of prior art consisting of patents or printed publications'" and that "[p]ortions of the patent under review – which the Petitioner has characterized as the AAPA – cannot be considered 'prior art consisting of patents or printed publications' within the plain meaning of the

[11] Although we only cite to IPR2018-01315 in this section, the same arguments were made by the parties in IPR2018-01316.

statute." PO Resp. 17–18 (quoting 35 U.S.C. § 311(b)). Patent Owner further argues that "the regulations governing inter partes review require that the petition 'specify where each element of the claim is found in the prior art patents or printed publications relied upon.'" *Id.* at 18 (quoting 37 C.F.R. § 42.104(b)(4)). According to Patent Owner, an admission in "the patent under review cannot reasonably be considered a '*prior art* patent or printed publication' because the patent is not prior art to itself." PO Resp. 18.

Patent Owner also argues that the Board erred in the Institution Decision by "fail[ing] . . . to recognize other PTAB decisions that have correctly held that AAPA does *not* qualify as prior art under Section 311(b)." *Id.* at 18–19 (citing *LG Electronics, Inc. v. Core Wireless Licensing S.A.R.L.*, IPR2015-01987, Paper 7 at 18 (PTAB Mar. 24, 2016) (Institution Decision); *Sony Corp. v. Collabo Innovations, Inc.*, IPR2016-00940, Paper 7 at 30 (PTAB Oct. 24, 2016) (Institution Decision)).

Additionally, Patent Owner argues that "counsel for Petitioner agrees that AAPA is *not* eligible for *inter partes* review, as evidenced by arguments recently made by Petitioner's counsel in IPR2017-00126." PO Resp. 19 (citing Ex. 2004 (Patent Owner's Request for Rehearing in IPR2017-00126)); Ex. 2005 (Patent Owner's Response in IPR2017-00126)). Moreover, Patent Owner argues that Petitioner's Reply "does not disagree that AAPA is not proper prior art for IPR proceedings" and "never makes the affirmative statement that AAPA should be considered prior art in IPRs." PO Sur-reply 1 (citing Paper 16, 1–2).

Patent Owner further argues that *One World*, cited by Petitioner in the Reply, is distinguishable from the facts of this case. PO Sur-reply 1 n.1. Specifically, Patent Owner argues in *One World* "AAPA was relied on as a

secondary reference in an obviousness ground" but, "in the present case, Petitioner attempts to rely on AAPA as a primary reference." *Id.* (citing *One World Techs., Inc. v. Chamberlain Group, Inc.*, IPR2017-00126, Paper 56, 6 (PTAB Oct. 24, 2018) (Final Written Decision Public Version)).[12]

b. Petitioner's Arguments

In the Petition, Petitioner did not address whether an *inter partes* review can be based on applicant admitted prior art. *See generally* Pet. In its Reply, Petitioner argues that "Patent Owner provides no basis upon which the Board should revisit the position expressed in the Institution Decision ('ID') that AAPA is an eligible ground for an IPR." Pet. Reply 1 (citing Inst. Dec. 21–22); *see also id.* at 1–2. According to Petitioner, "the Board diligently followed the logic articulated by the panel in IPR2017-

[12] Additionally, Patent Owner argues that "this issue should be elevated for Precedential Opinion Panel review should the Board continue its improper consideration of the alleged AAPA." PO Resp. 19; *see also* Tr. 46:7–11. Patent Owner further argues that allowing a petitioner to rely on AAPA is unsound policy because "it dissuades patent applicants from including a background section in their patent applications." PO Sur-reply 2 n.2.

We do not address Patent Owner's argument that allowing *inter partes* review to consider applicant admitted prior art will dissuade patent applicants from including a background section in their patent applications. *See* PO Sur-reply 2 n.1. Such policy arguments regarding the impact of our decision on what patent applicants will do are beyond our purview. *See* 35 U.S.C. § 3(a)(2)(A) ("The Director shall be responsible for providing policy direction . . . for the Office . . . ."). If Patent Owner wishes the Precedential Opinion Panel to address the policy argument or any alleged inconsistency between PTAB panels, Patent Owner should follow the procedure set forth in Standard Operating Procedure 2, which can be found here: https://www.uspto.gov/sites/default/files/documents/SOP2%20R10%20FINAL.pdf.

00126 [(*One World*)] regarding the availability of AAPA." Pet. Reply 1. Petitioner further argues that "the exact same language used in 35 U.S.C. § 311(b) to define eligible prior art has been previously held by the Federal Circuit [in the context of pre-AIA reexamination proceedings] to encompass AAPA." *Id.* at 1–2 (citation omitted). Therefore, according to Petitioner, "[b]ecause Patent Owner fails to advance any new arguments that were not otherwise addressed by the ID or by the panel's decisions in IPR2017-00126, Patent Owner's arguments regarding the availability of AAPA in IPRs should be dismissed." *Id.* at 2.

During the Oral Hearing, counsel for Petitioner explicitly stated that it is Petitioner's position that AAPA can be used in an *inter partes* review. Tr. 19:23–20:2.

c. Our Analysis

We agree with Petitioner that an admission in the patent that is the subject to an *inter partes* review—that is, applicant admitted prior art—can be used to challenge claims in an *inter partes* review.

We begin our analysis with the statute. 35 U.S.C. § 311(b) provides that "[a] petitioner in an inter partes review may request to cancel as unpatentable 1 or more claims of a patent only on a ground that could be raised under section 102 or 103 and *only on the basis of prior art consisting of patents or printed publications*." (emphasis added). Our regulations provide substantially the same limitation. *See* 37 C.F.R. § 42.104(b)(2) (2019) (requiring the petition to "identify . . . the *patents or printed publications* relied upon for each ground" (emphasis added)). The only requirement is that the "prior art consist[] of patents or printed publications."

Because AAPA is admitted to be prior art and is found in the '674 patent, it can be used to challenge the claims in an *inter partes* review.

This is consistent with prior use of identical statutory language. Prior to enactment of the Leahy-Smith America Invents Act ("AIA"), Congress used the phrase "prior art consisting of patents or printed publications" to exclusively identify the prior art that could be relied upon in reexamination proceedings. *See* 35 U.S.C. § 302 (1980) ("Any person . . . may file a request for reexamination . . . on the basis of any prior art cited under the provisions of section 301."); 35 U.S.C. § 301 (1980) (identifying "prior art consisting of patents or printed publications" as the only prior art that could be cited in reexamination proceedings). The Federal Circuit found that applicant admitted prior art could be cited and relied upon to support the Board's findings in such proceedings. *See In re NTP, Inc.*, 654 F.3d 1279, 1304 (Fed. Cir. 2011). By finding that applicant admitted prior art could be used in combination with another reference in a pre-AIA reexamination proceeding in which only "prior art consisting of patents or printed publications" could be cited, the Federal Circuit has found, as we do above, that "prior art consisting of patents or publications" includes applicant admitted prior art. *See NTP*, 654 F.3d at 1304;[13] *see also In re Nomiya*, 509 F.2d 566, 570–71 (CCPA 1975) (holding that applicant admitted prior art may "be considered as prior art in determining obviousness of their

[13] As Patent Owner pointed out during the Oral Hearing, the patent owner in *NTP* did not appeal the Board's decision to rely on the applicant admitted prior art. Tr. 41:8–12; *see also NTP*, 654 F.3d 1279. However, the Federal Circuit's decision is still, at a minimum, persuasive authority for the proposition that application admitted prior art is "prior art consisting of patents . . ."

improvement"). Because Congress used the same language—"prior art consisting of patents or printed publications"—in both the pre-AIA reexamination statute and the *inter partes* review statute, we give the same phrase the same meaning. *See also One World*, Paper 56 at 35–41 (holding that applicant admitted prior art can be used to challenge the claims in an *inter partes* review).

We do not agree with Patent Owner that, based on our rules, an admission in "the patent under review cannot reasonably be considered a '*prior art* patent or printed publication' because the patent is not prior art to itself." PO Resp. 18 (emphasis in original); *see also id.* ("Likewise, the regulations governing *inter partes* review require that the petition "specify where each element of the claim is found in the *prior art patents* or printed publications relied upon." (quoting 37 C.F.R. § 42.104(b)(4)) (emphasis in original)). However, the language in Rule 42.104(b)(4) cannot be read in isolation, as Patent Owner has done, to contradict the related statutory and regulatory provisions. Instead, it must be read in the context of the entire rule and the governing statute.

The quoted language in 42.104(b)(4) refers back to § 42.104(b)(2): The petition must state "[h]ow the construed claim is unpatentable under the *statutory grounds identified in paragraph (b)(2)* of this section." 37 C.F.R. § 42.104(b)(4) (2017) (emphasis added). According to § 42.104(b)(2), the petitioner must state the "*statutory grounds* under 35 U.S.C. 102 or 103 on which the challenge to the claim is based and *the patents or printed publications* relied upon for each ground." 37 C.F.R. § 42.104(b)(2) (2019) (emphases added). Thus, 42.104(b)(2) refers back to the statutory language which requires a challenge to be based "only on a ground that could be

raised under section 102 or 103 and only on the basis of *prior art consisting of patents or printed publications*." 35 U.S.C. § 311(b) (emphasis added). Therefore, considered as a whole, our rules simply reflect the limitations of the governing statute and do not impose any additional limitations that would exclude applicant admitted prior art.

We are not persuaded by the cases cited by Patent Owner—*LG Electronics* and *Sony*—that it is improper in this case for us to consider AAPA in combination with Majcherczak, a prior art patent. First, both *LG Electronics* and *Sony* are routine decisions. Accordingly, they are not binding on us. *See* Standard Operating Procedure 2 (Revision 10), 3, *available at* https://www.uspto.gov/sites/default/files/documents/SOP2%20R10%20FINAL.pdf ("Every decision other than a precedential decision by the Precedential Opinion Panel is, by default, a routine decision. A routine decision is binding in the case in which it is made, even if it is not designated as precedential or informative, but it is not otherwise binding authority.").

Second, because they do not address the Federal Circuit's *Nomiya* and *NTP* decisions, we do not find the reasoning of *LG Electronics* and *Sony* sufficiently persuasive. *See LG Elecs.*, Paper 7 at 18; *Sony*, Paper 7 at 30. In contrast, we find the reasoning in *One World* persuasive. The analysis in *One World* spans seven pages, discusses relevant case law—such as *Nomiya* and *NTP*—and addresses the statutory and regulatory language in depth. *One World*, Paper 56 at 35–41.[14]

[14] We note that in *One World* the patent owner sought Precedential Opinion Panel review on whether applicant admitted prior art can be used to

Nor do we agree with Patent Owner that *One World* is distinguishable because the applicant admitted prior art was a secondary reference in that case but the primary reference in this proceeding. *See* PO Sur-reply 1 n.1. First, none of the reasoning in *One World* depended on whether the applicant admitted prior art was a primary or secondary reference. If applicant admitted prior art may be considered in an *inter partes* review, then it makes no difference if it is the primary reference or the secondary reference.

Second, Patent Owner has not cited any authority for the proposition that the order of references makes any difference in analyzing the patentability of a claim. In other contexts, a reviewing court has found changes to the order of references from A in view of B to B in view of A to be "of little consequence, and that basing arguments on them was 'attempting to make a mountain out of a mole-hill.'" *In re Bush*, 296 F.2d 491, 496 (CCPA 1961) (quoting *In re Cowles*, 156 F.2d 551, 554 (CCPA 1946)).

Accordingly, Petitioner can challenge the patentability of the claims in this *inter partes* review based on the combination of AAPA and Majcherczak.

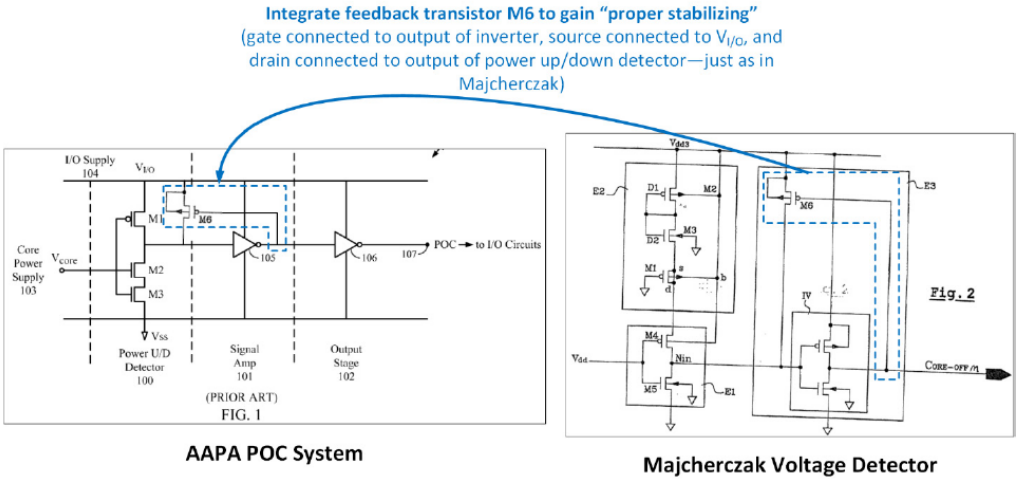
4. Claim 1

a. Undisputed Limitations

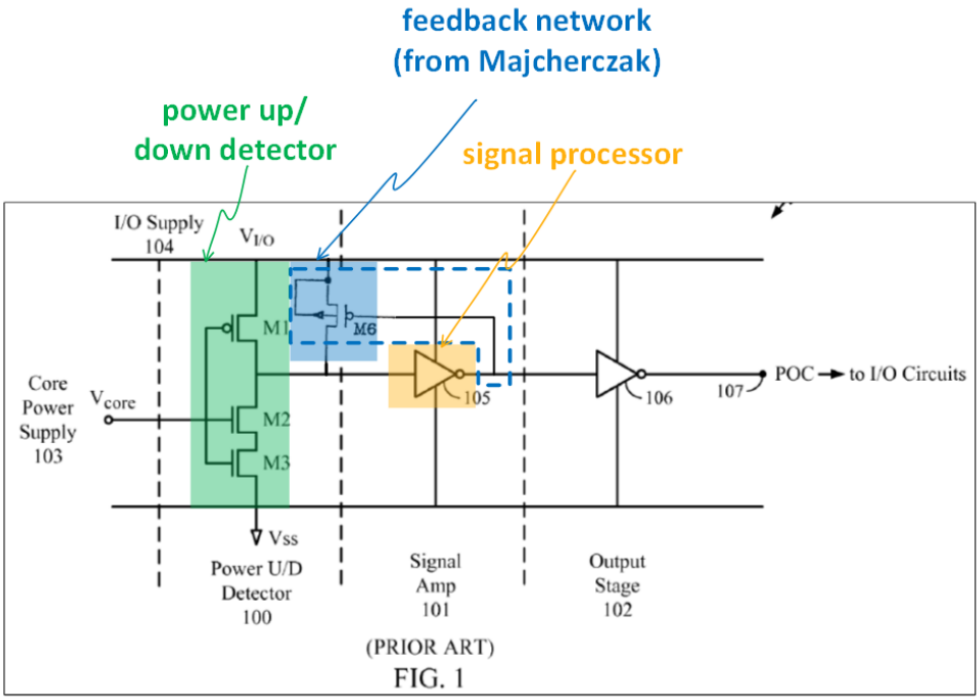
Petitioner argues that the combination of AAPA and Majcherczak teaches all of the limitations recited in claim 1. *See* Pet. 37–56. Specifically, Petitioner argues a person of ordinary skill in the art would

challenge claims in an *inter partes* review. *See One World*, Paper 61; *One World*, Ex. 3005. That request was denied. *One World*, Paper 63.

have combined the feedback circuit of Majcherczak with the POC described in AAPA as shown in the annotated figure reproduced below.



Pet. 44. The figure reproduced above shows Majcherczak's Figure 2 annotated by Petitioner (right) and a version of Figure 1 of the '674 patent (AAPA) modified by Petitioner to integrate the feedback transistor M6 from Majcherczak's Figure 2 (left). *Id*. Petitioner also provides a differently annotated version of its proposed combination as reproduced below.



AAPA + Majcherczak POC System

Pet. 50. The figure above shows what Petitioner contends is the combination of the feedback network of Majcherczak with the POC of AAPA. *Id*. Petitioner's annotations show what Petitioner argues is the power up/down detector in green, the signal processor in yellow, and the feedback network from Majcherczak in blue. *Id*.

Petitioner argues that AAPA in combination with Majcherczak teaches "[a] multiple supply voltage device" as recited in claim 1. Pet. 46. According to Petitioner, "AAPA describes that the prior art POC system 10 is useful in 'newer integrated circuit devices include dual power supplies: one lower-voltage power supply for the internally operating or core applications, and a second higher-voltage power supply for the I/O circuits and devices.'" *Id*. (quoting Ex. 1001, 1:22–25).

Petitioner also argues that AAPA in combination with Majcherczak teaches "a core network operative at a first supply voltage" as recited in claim 1. Pet. 46–47. Specifically, Petitioner argues AAPA includes power up/down detector 100 which is connected to the core power supply, which is a "lower-voltage power supply for the internally operating or core applications." *Id*. (citing Ex. 1001, 1:22–25, 1:60–64).

Petitioner further argues that AAPA in combination with Majcherczak teaches "a control network coupled to said core network wherein said control network is configured to transmit a control signal" as recited in claim 1. Pet. 47. Specifically, Petitioner argues "[t]he prior art power-on/off-control (POC) system 10 is a control network coupled to said core network (via core power supply V_{core}), and the POC system 10 is configured to transmit a power-on/off-control (POC) signal 107." *Id*. (citing Ex. 1001, 1:55–58, 1:65–2:13).

Petitioner also argues that AAPA in combination with Majcherczak teaches "said control network comprising: an up/down (up/down) detector configured to detect a power state of said core network; processing circuitry coupled to said up/down detector and configured to generate said control signal based on said power state" as recited in claim 1. *Id.* at 48–49. Specifically, Petitioner directs us to a comparison of Figure 4 of the '674 patent and the combination of AAPA and Majcherczak, both of which show a power/up down detector and a signal amplifier portion. Pet. 48. Petitioner further argues that "[t]he signal amplifier 101 and output stage 102 are processing circuitry coupled to said up/down detector and configured to generate the power-on/off-control (POC) signal 107 based on said power state." *Id.* at 49.

Petitioner argues the combination of AAPA and Majcherczak teaches "one or more feedback circuits coupled to said up/down detector, said one or more feedback circuits configured to provide feedback signals to adjust a current capacity of said up/ down detector" as recited in claim 1. *See* Pet. 49–52. Specifically, Petitioner argues that, when the teachings of AAPA and Majcherczak are combined as shown in the figure reproduced above, "the feedback transistor M6 is a feedback circuit coupled to the up/down detector 100 via its output." Pet. 51 (citing Ex. 1003 ¶ 141); *see also* Pet. 51–52 (citing Ex. 1003 ¶¶ 142–143). That is, according to Petitioner, "when both transistors M1 and M6 are 'on' (i.e., V_{core} is off), the transistor M6 increases the current capacity of the power up/down detector 100" but "when both transistors M1 and M6 are 'off' (i.e., V_{core} is on), the transistor M6 decreases the current capacity of the power up/down detector 100." Pet. 51–52 (citing Ex. 1003 ¶¶ 142–143).

Petitioner also argues that AAPA in combination with Majcherczak teaches "at least one first transistor coupled to a second supply voltage, the at least one more first transistor being configured to switch on when said first supply voltage is powered down and to switch off when said first supply voltage is powered on" as recited in claim 1. *See* Pet. 52–53. More specifically, Petitioner argues M1—a first transistor—is coupled to $V_{I/O}$—the I/O power supply or second supply voltage. *Id*. (citing Ex. 1003 ¶ 141; Ex. 1001, 1:62–2:1, 2:8–9). Petitioner further argues that "AAPA explains that the transistor M1 is configured to switch on when said first supply voltage is powered down and to switch off when said first supply voltage is powered on." Pet. 53 (citing Ex. 1001, 1:65–67, 2:8–9).

Petitioner further argues that AAPA in combination with Majcherczak teaches "at least one second transistor coupled in series with the at least one first transistor and coupled to said first supply voltage, the at least one second transistor being configured to switch on when said first supply voltage is powered on and to switch off when said first supply voltage is powered down" as recited in claim 1. *See* Pet. 54–55. More specifically, Petitioner argues transistor M3 is a second transistor and "AAPA explains that the transistor M3 is configured to switch on when said first supply voltage is powered down and to switch off when said first supply voltage is powered on." *Id*. (citing Ex. 1003 ¶¶ 141, 144–147; Ex. 1001, 1:65–67, 2:8–9).

Petitioner also argues that AAPA in combination with Majcherczak teaches "at least one third transistor coupled in series between the at least one first transistor and the at least one second transistor" as recited in claim 1. Pet. 55–56. Specifically, Petitioner points to transistor M2,[15] which, according to Petitioner, "is coupled in series between transistor M1 (i.e., the first transistor) and transistor M3 (i.e., the second transistor)." Pet. 56 (citing Ex. 1003 ¶ 144).

Patent Owner does not dispute Petitioner's contention that the combination of AAPA and Majcherczak teaches each of the limitations recited in claim 1. *See generally* PO Resp. 20–31; *see also* Pet. Reply 2

[15] The Petition interchangeably refers to transistor M2 and M3 as the third transistor. Pet. 56. However, the Petition specifically refers to the transistor highlighted in brown, which is transistor M2. We stated in the Institution Decision that we would "treat the reference to transistor M3 as a typographical error." Inst. Dec. 19 n.10. Neither party addressed this point in any subsequent briefing. *See generally* PO Resp.; Pet. Reply.

("Beyond this procedural issue [on whether applicant admitted prior art could be considered], Patent Owner's only substantive argument challenging Ground 2 is a purported lack of motivation to combine."); PO Sur-reply 2–19 (not disputing Petitioner's characterization of Patent Owner's argument).

We previously instructed Patent Owner that "any arguments for patentability not raised in the [Patent Owner Response] may be deemed waived." Scheduling Order, Paper 8, 5; *see also In re NuVasive, Inc.*, 842 F.3d 1376, 1380–81 (Fed. Cir. 2016) (determining Patent Owner waived arguments made only in its Preliminary Response but not raised in the Patent Owner Response after institution).

Based on the undisputed evidence before us and the reasons set forth in the Petition, Pet. 37–56, we find that the combination of AAPA and Majcherczak teaches all of the limitations recited in claim 1.

b. Whether a Person of Ordinary Skill in the Art Would Have Combined AAPA and Majcherczak

(1) Petitioner's Arguments

Petitioner argues that a person of ordinary skill in the art "would have been motivated to integrate the feedback transistor M6 from Majcherczak's voltage detector into the POC system 10 of AAPA in order to 'enable[] the proper stabilizing of the detection device.'" Pet. 45 (quoting Ex. 1008 ¶ 37) (citing Ex. 1003 ¶ 150). According to Petitioner, the "combination would result in AAPA's POC system 10 observing the 'hysteresis detection' described by Majcherczak, facilitating controlled operation of the I/O devices instructed by the POC signal on communications from the core devices when the core supply voltage is stably on." *Id*. (citing Ex. 1003 ¶ 150); *see also* Pet. Reply 2–5.

Petitioner further argues that "[i]t is undisputed in the [Patent Owner's Reponse] or by Dr. Pedram that adding Majcherczak's feedback transistor M6 to the AAPA as described in the Petition achieves the advantageous hysteresis described in Majcherczak." Pet. Reply 5 (citing PO Resp. 20–31; Ex. 2002 ¶¶ 67–85). According to Petitioner, "Dr. Pedram admits that it was possible to add hysteresis to the AAPA circuit shown in FIG. 1 of the '674 [p]atent, and that such an addition could help improve noise immunity of the circuit." *Id.* (citing Ex. 1017, 46:22–47:10).

Petitioner further argues that "it is irrelevant whether the prior art's explicit motivation to integrate Majcherczak's feedback transistor M6 into the AAPA matches the problem statement of the '674 [p]atent." Pet. Reply 6 (citing *Cross Med. Prods., Inc. v. Medtronic Sofamor Danek, Inc.*, 424 F.3d 1293, 1323 (Fed. Cir. 2005)). According to Petitioner, "[i]t is not necessary that the prior art suggest the combination to achieve the same advantage or result purportedly discovered by the Patent Owner." *Id.* (citing *In re Kahn*, 441 F.3d 977, 987 (Fed. Cir. 2006); *Cross*, 424 F.3d at 1323).

Moreover, according to Petitioner, a person of ordinary skill in the art would have a reasonable expectation of success:

> A POSITA would have perceived a reasonable expectation of success in making this modification to the POC system 10 of AAPA, because the POC system 10 and Majcherczak's voltage detector share many functionally commensurate elements, operate in a corresponding manner, and are used in the similar types of multiple supply voltage devices. [Ex. 1003] ¶ 151. Indeed, the integration of the feedback transistor M6 from Majcherczak's voltage detector would have simply been the use of a known technique (a feedback transistor to improve hysteresis) to improve similar devices (detection circuits in multiple supply voltage devices) in the same way. *Id.*

Pet. 45.

Petitioner also argues that any potential disadvantages with the modification identified by Patent Owner and Dr. Pedram—additional leakage current compared to AAPA or Majcherczak, glitch current, and DC fighting condition (*see* PO Resp. 21–31)—"fail to demonstrate the absence of motivation." Pet. Reply 8; *see also id.* at 7–12. Specifically, Petitioner argues that "[i]t is well understood that 'a given course of action often has simultaneous advantages and disadvantages, and this does not necessarily obviate motivation to combine.'" *Id.* at 8 (citing *Medichem, S.A. v. Rolabo, S.L.*, 437 F.3d 1157, 1165 (Fed. Cir. 2006)). According to Petitioner, in this case, "the explicit benefit articulated in Majcherczak is not undone or outweighed by the vague and unsupported disadvantages described in the [Patent Owner's Response] and by Dr. Pedram." *Id.*

Petitioner also argues that there is no evidentiary support for any of the potential disadvantages articulated by Patent Owner and Dr. Pedram. Pet. Reply 7–12. Specifically, Petitioner argues neither Patent Owner nor Dr. Pedram cite to any references to support the list of disadvantages and Dr. Pedram admitted that the list is hypothetical and "that he never simulated any of the prior art or proposed combinations to determine what, if any, performance issues would arise from the proposed combination." *Id.* at 7–8 (citing Ex. 1017, 40:15–41:13, 45:9–15, 59:4–8, 61:4–10, 65:7–14, 167:20–23, 170:13–171, 171:20–172:1, 180:6–16, 187:25–188:9) (footnote omitted). Petitioner further argues that "[w]ithout corroborating evidence to contradict the explicit motivating teaching of Majcherczak, Dr. Pedram's statements are unsupported, exposing them as insufficient to establish substantial evidence addressing or confronting the affirmative proof offered by

Petitioner." *Id.* at 8 (citing *Ericsson Inc. v. Intellectual Ventures I LLC*, 890 F. 3d 1336, 1346 (Fed. Cir. 2018)).

Petitioner further argues that the problems of the asserted combination alleged by Patent Owner are "not inherent in the proposed architectural combination. Rather, such issues would only potentially arise due to an improper selection of design characteristics such as the transistor sizes, threshold voltages, and values of $V_{I/O}$ and V_{core}." Pet. Reply 9 (citing Ex. 1018 ¶¶ 7–9, 74–77); *see also id.* at 12 ("Even assuming a POSITA would have considered these as potential disadvantages in implementing the proposed combination, the POSITA would nevertheless have been motivated for reasons cited within Majcherczak to make the combination, as the POR's alleged disadvantages and their potential adverse impacts either would not have been observed or a POSITA would have been able to minimize them." (citing Ex. 1018 ¶¶ 50–64)).

With regard to additional leakage current (PO Resp. 21–27), Petitioner argues that "Dr. Pedram acknowledged that it is the unclaimed design details—transistor sizes, threshold voltages, and values of $V_{I/O}$ and V_{core}—that will determine the amount of leakage present in the proposed combination." Pet. Reply 10 (citing Ex. 1017, 63:22-65:20). Petitioner further argues that "Dr. Horst shows through simulation of these designs" that the proper selection of design details result in "mitigat[ing] any potentially problematic increase in leakage current, leaving the power consumption due to leakage current to be relatively the same or even better than either the AAPA or Majcherczak alone." *Id.* (citing Ex. 1018 ¶¶ 50–64, 68–73).

With regard to glitch current (PO Resp. 27–30), Petitioner argues that because the '674 patent acknowledges that glitch current was an issue with AAPA, "the addition of Majcherczak's feedback transistor would not have created a new problem in the circuit." Pet. Reply 10 (citing Ex. 1001, 2:25–30; Ex. 1018 ¶¶ 31, 56, 57, 75–77). Petitioner further argues that Dr. Horst's simulation shows that the glitch current can be mitigated by a proper selection of threshold voltages. *Id.* at 11 (citing Ex. 1018 ¶¶ 21–31, 50–64).[16]

With regard to the DC fighting condition (PO Resp. 27–30), Petitioner argues that Dr. Pedram states that this "'could happen' only on 'rare occasions,' making any assessment of a hypothetical DC fighting condition a 'complicated task.'" Pet. Reply 11 (quoting Ex. 1017, 181:10–24). Petitioner further argues that "[t]he condition is so complicated and rare, in fact, that Dr. Pedram believes that a POSITA would not even see or be aware of this disadvantage when analyzing the proposed combinations." *Id.* (citing Ex. 1017, 175:11–15). According to Petitioner, a person of ordinary skill in the art "cannot have been dissuaded by a potential 'rare' problem he/she would not have even been aware of." *Id.* Petitioner further argue that the condition is dependent on the selection of design details and "this alleged problem did not arise in Dr. Horst's simulations." *Id.* at 11–12 (citing Ex. 1017, 172:10–173:16, 178:9–181:24; Ex. 1018 ¶¶ 30, 32, 33).

[16] Petitioner's Reply cites to Exhibit 2018. Based on the context of the sentence, this appears to be a typographical error and that Petitioner intended to cite Exhibit 1018.

(2) Patent Owner's Arguments

Patent Owner argues that, because "Petitioner's proposed combination results in a circuit with numerous operational flaws" that "would operate significantly worse than either the AAPA or Majcherczak had they been left unmodified," a person of ordinary skill in the art would "have had no reason to combine the alleged AAPA and Majcherczak as Petitioner proposes." PO Resp. 21; *see also id.* at 21–31; PO Sur-reply 2–19.

First, Patent Owner argues that "Petitioner's proposed addition of Majcherczak's transistor M6 to Fig. 1 of the '674 Patent (the alleged AAPA) results in *increased* leakage current, and the POSA would not be motivated to make Petitioner's proposed combination for at least this reason." PO Resp. 22 (citing Ex. 2002 ¶ 70); *see also id.* at 21–25; PO Sur-reply 4–5. Specifically, Patent Owner argues when the core power supply voltage (V_{core}) is on, "PMOS transistor M1 and feedback transistor M6 will be 'off,' and NMOS transistors M2 and M3 will be 'on' providing a path between the output of the power U/D detector 100 and ground." PO Resp. 23–24. Patent Owner further argues that "[b]ecause [V_{core}] is less then $V_{I/O}$, however, PMOS transistor M1 will be quite leaky, providing a high leakage path from $V_{I/O}$ to the output terminal of the power U/D detector 100." *Id.* at 24 (citing Ex. 2002 ¶ 72). Patent Owner further argues that "NMOS transistors N2 and M3 will be 'on,' providing a very low resistance path from the output terminal to Vss." *Id.* According to Patent Owner, as a consequence, "a high leakage DC path will exist between $V_{I/O}$ and Vss," which will result in more leakage current than would be present in the unmodified AAPA. *Id.* (citing Ex. 2002 ¶¶ 72–73).

Second, Patent Owner argues that the modified design "would also operate less effectively than Majcherczak alone." PO Resp. 25; *see also id.* at 25–27. Specifically, Patent Owner argues that "a [person having ordinary skill in the art] would have recognized that Majcherczak's power supply stage (E2) operates to reduce leakage current through the pull-up PMOS transistor (M4) in the input stage (E1) and thus helps to offset any additional leakage current introduced by the feedback transistor (M6)." *Id.* at 26 (citing Ex. 2002 ¶¶ 76–78). According to Patent Owner, because Petitioner does not suggest incorporating Majcherczak's power supply stage (E2) into the AAPA, "[t]he power detection circuit depicted in Fig. 2 of Majcherczak would thus operate with significantly less leakage current than Petitioner's proposed combination." *Id.* at 26–27 (citing Ex. 2002 ¶¶ 76–79).

Third, Patent Owner argues that Petitioner's proposed combination "would also introduce substantial operational problems during the process of powering on the core voltage supply (Vcore), causing increased glitch (i.e., crowbar) current and circuit instability." PO Resp. 27; *see also id.* at 27–30. More specifically, Patent Owner argues that "switching delays of the power up/down detector 100 and inverter 105 . . . will cause the feedback transistor M6 . . . to remain on for at least some delay period after the core power supply voltage (Vcore) turns on." *Id.* at 28 (citing Ex. 2002 ¶¶ 81–82). Patent Owner further argues that this can cause an unstable DC fighting condition during the inverter delay period. *Id.* (citing Ex. 2002 ¶ 83). According to Patent Owner, the DC fighting condition "can cause a downstream ripple effect such that Inverter 105 . . . becomes unstable, causing further instability in the 'feedback network' . . ., and potentially

resulting in a complete circuit breakdown" or, at the very least, worsen the glitch current. *Id.* at 28–30 (citing Ex. 2002 ¶¶ 83–84).

Patent Owner further argues that, contrary to Petitioner's arguments, a person of ordinary skill in the art would not seek to add hysteresis. PO Sur-reply 2–4. According to Patent Owner, a person having ordinary skill in the art would, instead, focus on how to solve the problems articulated in AAPA—high leakage current and slow switching times. *Id.* More specifically, Patent Owner argues that (1) a person having ordinary skill in the art would have avoided adding hysteresis because it would make the problems identified in the '674 patent worse, (2) in light of the switching-speed problem articulated in the AAPA, the addition of hysteresis involves impermissible hindsight, and (3) AAPA does not suggest that stability is a problem in AAPA's circuit. *Id.* at 4–6.

Patent Owner further argues that Petitioner's argument (Pet. Reply 7) that Dr. Pedram does not cite to any references to support his list of disadvantages is misplaced. PO Sur-reply 7. According Patent Owner, no references are needed because the disadvantages "are all well-known phenomena that would be immediately apparent to the [person having ordinary skill in the art] upon considering the proposed combination" and "Petitioner sets forth no argument that the disadvantages described by Dr. Pedram are obscure or not generally understood, and such an assertion would be wrong." *Id.* Patent Owner further argues that "the reply cites no statute, rule, or caselaw to support the proposition that an expert's opinion must be corroborated by independent references." *Id.*

Patent Owner also argue that Petitioner's citation to "*Medichem, S.A. v. Rolabo, S.L.* that 'a given course of action often has simultaneous

advantages and disadvantages, and this does not necessarily obviate motivation to combine'" is misplaced because "the purported advantage of Majcherczak is no advantage at all." PO Sur-reply 7–8.

Finally, Patent Owner presents six arguments explaining why Dr. Horst's simulations do not prove that a person of ordinary skill in the art would have been motivated to combine AAPA and Majcherczak. *See* PO Sur-reply 8–18.

First, Patent Owner argues that "Petitioner's argument misunderstands the proper inquiry for obviousness." *Id.* at 8. According to Patent Owner, "[t]he relevant question is whether the [person of ordinary skill in the art] would be motivated to combine the alleged AAPA and Majcherczak to reach the claimed invention," not whether the person of ordinary skill in the art would combine the references and then use a simulation to determine a set of parameters that would avoid the problems identified by Dr. Pedram. *Id.* at 8–9.

Second, Patent Owner argues that the simulations are unreliable because Dr. Horst's supplemental declaration contained numerous errors. *See* PO Sur-reply 9–11. For example, Patent Owner points out how the results in the simulation of two different circuits were identical. *Id.* at 9 (comparing Ex. 1018 ¶ 12 with Ex. 1018 ¶ 23). Patent Owner points out that a corrective declaration with a new set of graphs intended to replace page 15 of the supplemental declaration introduced a new error in the results of Figure 4. *Id.* at 9–11 (citing Ex. 2007).

Third, Patent Owner argues that Dr. Horst selected unrealistic parameter values that the person of ordinary skill in the art would never use in the proposed combination of AAPA and Majcherczak. *See* PO Sur-

reply 11–16. Specifically, Patent Owner argues Dr. Horst selected a high FET threshold voltage that results in the problem of slow switching speed discussed in the '674 patent, the selected channel length and width parameters were selected from the Voss reference (Exhibit 1022) that is not from the field related to the technology of AAPA, and that the values are divorced from real world considerations. *Id.*

Fourth, Patent Owner argues Dr. Horst "cherry picked" parameter values without providing a sufficient rationale for their selection. PO Sur-reply 16–17. Specifically, Patent Owner criticizes Dr. Horst for using the values of the Voss reference for most transistors but provides no explanation for why the Voss reference was not used for all transistors. *Id.* Patent Owner further argues that Dr. Horst explained at his deposition that he changed the width of the feedback transistor from that given in Voss because if the Voss parameters were used consistently, the simulation would fail. *Id.* at 17 (citing Ex. 2006, 101:24–102:17).

Fifth, Patent Owner argues that Dr. Horst's simulation does not show that the combination of AAPA and Majcherczak does not result in increased leakage current. PO Sur-reply 17–18. Specifically, Patent Owner argues that ramping the V_{core} to max value and then immediately pulling back—as done in the simulation—is not an accurate way of measuring leakage current. *Id* at 18. Patent Owner argues that leakage power is primarily a problem when V_{core} is high and, if the simulation was addressing leakage, it should have left V_{core} voltage at 3.3V for at least some time. *Id.* at 18.

Sixth, Patent Owner argues that a single simulation is not sufficient. PO Sur-reply 18–19. More specifically, Patent Owner argues that a typical engineer will perform thousands of computer simulations and that "a single

simulation result cannot provide an accurate indication of whether a circuit would operate correctly under realistic, real-world conditions." *Id.* at 19. Patent Owner further argues that, although Dr. Horst's testimony discusses a single simulation, Dr. Horst executed many more simulations, but did not save the results of those simulations. *Id.* at 18–19.

(3) Our Analysis

A conclusion of unpatentability based on obviousness must be supported by "some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *Kahn*, 441 F.3d at 988 (citations omitted), *cited with approval in KSR*, 550 U.S. at 418. The requirement for a reason to combine the reference acts as a check on the potential for the improper use of hindsight. *Plantronics, Inc. v. Aliph, Inc.*, 724 F.3d 1343, 1354 (Fed. Cir. 2013) (holding that an articulated reasoning "is especially important to guard against the dangers of hindsight bias").

Based on the entirety of the record, we find Petitioner has shown sufficiently articulated reasoning with rational underpinning to support the legal conclusion of obviousness. Petitioner provides detailed analysis of the prior art and explains why, based on the teachings of the references, a person of ordinary skill in the art would have combined the references. *See* Pet. 37–45; Pet. Reply 3–6.

It is undisputed that Majcherczak identifies a problem with circuits with multiple supply voltage devices when the core voltage is powered down or slow to power up. *See* Ex. 1008 ¶¶ 7–8; *see also* Pet. 39. Specifically, Majcherczak states that

> [w]hen the core supply voltage disappears, the two logic voltages DATA and /DATA fall to zero. The two control transistors are then off. The voltage at an output of the

> translator becomes uncontrollable and dependent on the leakage currents in the transistors of the translator, or on a contradiction between two logic signals.

Ex. 1008 ¶ 7.

Majcherczak teaches using an output stage E3 which includes a "transistor M6 for pulling the output node Nin of the inverter of the input stage to the interface [I/O] power supply voltage Vdd3." Ex. 1008 ¶ 37. Majcherczak describes that "transistor M6 enables the proper stabilizing of the detection device. It maintains the node Nin at Vdd3, by feedback." *Id.* Majcherczak further describes how this allows for a hysteresis detection:

> With the output stage E3, a hysteresis detection is obtained with a low threshold of switching from a state of the presence of a core power supply to a state of the absence of a core power supply, and a high threshold of switching of the detection circuit from a state of absence of the core supply to a state of presence of the core supply. In particular, if the output node Nin of the input stage is at Vdd3, then the signal IN applied to its input rises sufficiently to force the output node Nin downwards, and consequently, cut off the pull-down transistor M6. In a practical example, for integrated circuits using 0.18 μ technology with a core supply voltage of 1.8 volts, the high threshold may thus be equal to 0.98 volts and the low threshold may be equal to 0.33 volts.

Id. ¶ 38. "[H]ysteresis detection is useful for ensuring that the level shifters only operate to facilitate communications between the core network and the I/O network when the core supply voltage is stably on." Ex. 1003 ¶ 138 (Horst Decl.).

We are persuaded by the evidence in the record that a person having ordinary skill in the art would have "integrate[d] feedback transistor M6 from Majcherczak's voltage detector into the POC system 10 of the AAPA in order to 'enable[] the proper stabilizing of the detection device.'"

Ex. 1003 ¶ 150 (Horst Decl.) (quoting Ex. 1008 ¶ 37). The person having ordinary skill of the art would have made such a modification to add hysteresis detection to AAPA's POC system 10, thereby "ensuring that the I/O devices instructed by the POC signal only operate on communications from the core devices when the core supply voltage is stably on." *Id.*

It is inapposite that the reason for the modification is different from the problem being addressed in the '674 patent. In *KSR*, the Supreme Court rejected the application of rigid rules, such as considering only the problem the patentee was trying to solve:

> The first error of the Court of Appeals in this case was to foreclose this reasoning by holding that courts and patent examiners should look only to the problem the patentee was trying to solve. *The Court of Appeals failed to recognize that the problem motivating the patentee may be only one of many addressed by the patent's subject matter*. The question is not whether the combination was obvious to the patentee but whether the combination was obvious to a person with ordinary skill in the art. *Under the correct analysis, any need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed*.

KSR, 550 U.S. at 420 (emphases added, citations omitted). Instead, the Supreme Court applied a flexible approach, holding that "if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill." *Id.* at 417; *see also id.* ("When a patent simply arranges old elements with each performing the same function it had been known to perform and yields no more than one would expect from such an

arrangement, the combination is obvious.") (internal quotation and citation omitted).

Consistent with the Supreme Court's *KSR* holding, the Federal Circuit has similarly rejected arguments based on a reason to combine that were different from the one identified by the patentee. For example, in *Samsung Electronics Co. v. UUSI, LLC*, the Federal Circuit reversed a PTAB decision that required the reason to combine the references to be directed to the same problem as identified in the challenged patent:

> UUSI next argues that the Board was correct in finding that Gerpheide was addressed to a different problem, referring us to its expert's testimony regarding the fact that Gerpheide and the '183 patent were directed to different problems and solved those problems in different ways. **Samsung argues that under *KSR International Co. v. Teleflex Inc.*, 550 U.S. 398, 127 S.Ct. 1727, 167 L.Ed.2d 705 (2007), the Board's decision was legally erroneous because it required the proffered motivation to combine Gerpheide with Ingraham/Caldwell to be the same as the one that animated the patentee in arriving at the claimed invention. We agree with Samsung**. The Board's categorical rejection of the teachings from a single input device to those of a multi input device is not supportable. "[I]f a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill." *Id.* at 417, 127 S.Ct. 1727.

Samsung Electronics Co. v. UUSI, LLC, 775 F. App'x 692, 695 (Fed. Cir. 2019) (emphasis added); *see also In re Conrad*, 759 F. App'x 982, 985 (Fed. Cir. 2019) ("The Supreme Court and this court, however, have repeatedly held that the motivation that a person of ordinary skill in the art would have had to combine prior art references need not be the same motivation that inspired the patent owner." (citation omitted)); *In re Beattie*, 974 F.2d 1309,

1312 (Fed. Cir. 1992) ("As long as some motivation or suggestion to combine the references is provided by the prior art taken as a whole, the law does not required that the references be combined for the reasons contemplated by the inventor.").

Furthermore, the evidence shows that a person having ordinary skill in the art would have had a reasonable expectation of success. *See* Ex. 1003 ¶ 151 (Horst Decl.). Specifically we are persuaded by Dr. Horst's testimony that "the integration of feedback transistor M6 from Majcherczak's voltage detector would have simply been the use of a known technique (a feedback transistor to provide hysteresis) to improve similar devices (detection circuits in multiple supply voltage devices) in the same way." *Id.*

We disagree with Patent Owner's arguments, discussed below.

Explicit Motivation: As a preliminary matter, "for the reasons discussed above with regard to reason to combine, we are not persuaded by Patent Owner's argument that an explicit motivation to combine the references is required for obviousness." *See* PO Sur-reply 2–6. Moreover, Patent Owner's argument that Majcherczak's hysteresis detection does not provide an explicit motivation to combine the references is not timely and waived. *See* PO Sur-reply 2–6. Petitioner made its hysteresis argument in the Petition and Patent Owner did not address the arguments in its Response. *Compare* Pet. 45 (relying on hysteresis detection for the reason to combine the references), *with* PO Resp. 20–31 (not discussing hysteresis); *see also* Tr. 74:13–18 (acknowledging the argument was not raised in the Patent Owner's Response). Although Patent Owner addresses this argument in its Sur-reply, "arguments for patentability not raised in the response may be deemed waived." Scheduling Order, Paper 8, 5; *see also Nuvasive*, 842 F.3d

at 1380–81 (holding that an argument not presented in Patent Owner's response is waived); *Dell Inc. v. Acceleron, LLC*, 884 F.3d 1364, 1369 (Fed. Cir. 2018) (holding that the Board was not obligated to consider an "untimely argument"). Because Patent Owner did not address Petitioner's argument regarding an explicit motivation in the Patent Owner's Response, that argument is waived.

Potential Issues: We do not agree with Patent Owner that a person having ordinary skill in the art would not have combined AAPA with Majcherczak because of the following potential issues identified by Dr. Pedram: additional leakage current compared to AAPA, glitch current, and a DC fighting condition. *See* PO Resp. 21–25, 27–31. Patent Owner's argument relies exclusively on Dr. Pedram's testimony as support for why a person having ordinary skill in the art would not make the proposed modification due to the identified "problems." *See id.* (citing Ex. 2002 ¶¶ 70–74, 81–85). However, Dr. Pedram does not cite to any evidence to support his opinions. *See* Ex. 2002 ¶¶ 70–74, 81–85. That is, Dr. Pedram does not cite to any tests, references, or simulations that support his opinion. *Id.*; Ex. 1017, 41:6–13, 171:20–171:3 (Pedram Dep.).

This stands in marked contrast to Dr. Horst's testimony. In response to Dr. Pedram's argument that the combination of AAPA and Majcherczak would result in increased leakage current, glitch current, or a DC fighting condition, Dr. Horst conducted a computer simulation to demonstrate that, with the appropriate selection of design details, those potential problems

could be managed. *See* Ex. 1018 ¶¶ 21–33 (Horst Supp. Decl.); Ex. 2007 (Horst Corrective Decl.).[17]

Our rules provide that "[e]xpert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight." 37 C.F.R. 42.65(a). In light of the failure to provide any corroboration, such as a simulation, we give Dr. Pedram's conclusory, unsupported testimony little weight. *See In re Am. Acad. of Sci. Tech Ctr.*, 367 F.3d 1359, 1368 (Fed. Cir. 2004) ("[T]he Board is entitled to weigh the declarations and conclude that the lack of factual corroboration warrants discounting the opinions expressed in the declarations."); *Verlander v. Garner*, 348 F.3d 1359, 1371 (Fed. Cir. 2003) (noting that the Board has discretion to accord little weight to broad conclusory statements from expert witness); *Ashland Oil, Inc. v. Delta Resins & Refractories, Inc.*, 776 F.2d 281, 294 (Fed. Cir. 1985) (noting that the "[l]ack of factual support" for an expert opinion "may render the testimony of little probative value").

In contrast to the potential issues discussed in the preceding paragraphs, Dr. Pedram provides some factual support for his testimony that the proposed modification would result in an increased leakage current compared to Majcherczak alone. *See* Ex. 2002 ¶¶ 75–80 (citing Ex. 1008). However, although Dr. Pedram may have established that "[t]he power detection circuit depicted in Fig. 2 of Majcherczak would thus operate with significantly less leakage current than Petitioner's proposed combination, which omits the power supply stage (E2) of Majcherczak," (Ex. 2002 ¶ 79), that is not the relevant issue. Instead, the issue is whether a person of

[17] We address Patent Owner's arguments regarding Dr. Horst's simulation *infra*.

ordinary skill in the art would have improved AAPA by "integrat[ing] feedback transistor M6 from Majcherczak's voltage detector into the POC system 10 of the AAPA in order to 'enable[] the proper stabilizing of the detection device.'" Ex. 1003 ¶ 150 (Horst Decl.) (quoting Ex. 1008 ¶ 37).

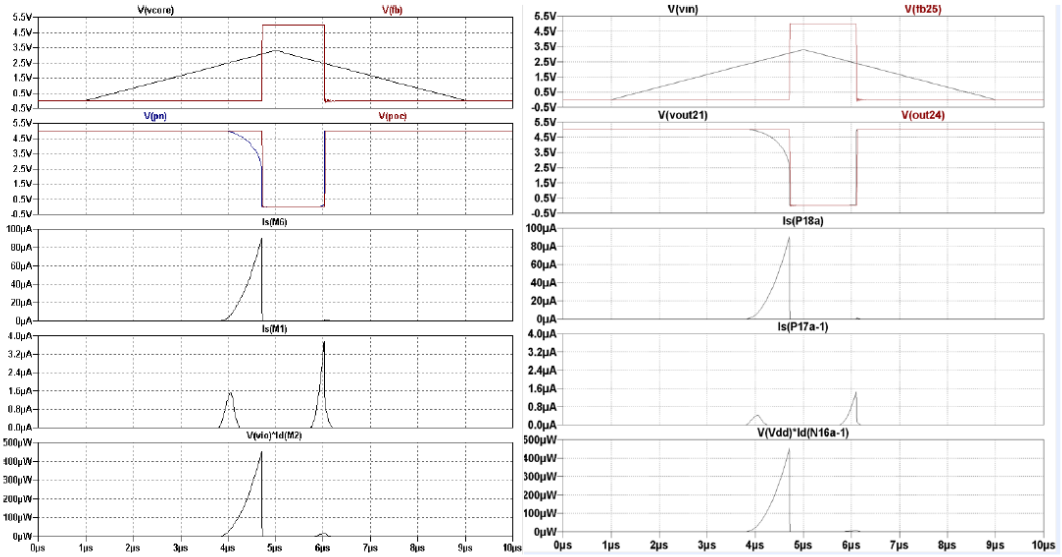
Moreover, merely identifying potential problems that could arise with a combination of references is not, by itself, enough to demonstrate that the combination would not have been obvious. Rather, "a given course of action often has simultaneous advantages and disadvantages, and this does not necessarily obviate motivation to combine." *Medichem, S.A. v. Rolabo, S.L.*, 437 F.3d 1157, 1165 (Fed. Cir. 2006) (citing *Winner Int'l Royalty Corp. v. Wang*, 202 F.3d 1340, 1349 n. 8 (Fed. Cir. 2000)). Accordingly, "[t]he fact that the motivating benefit comes at the expense of another benefit, however, should not nullify its use as a basis to modify the disclosure of one reference with the teachings of another. Instead, the benefits, both lost and gained, should be weighed against one another." *Winner*, 202 F.3d at 1349 n.8. Although Patent Owner and Dr. Pedram identify potential problems with the combination of AAPA and Majcherczak, they do not weigh the relative advantages and disadvantages. Considering only one half of the analysis is not sufficient. This is especially true in light of (1) the explicit benefit discussed in Majcherczak and (2) the unsupported identification of potential issues in the Patent Owner's Response and Dr. Pedram's testimony.

Additionally, we are persuaded by Dr. Horst's testimony that any potential problems in the combination would have been addressed by the person having ordinary skill in the art by the selection of appropriate design characteristics such as the transistor sizes, threshold voltages, and values of

$V_{I/O}$ and V_{core}. *See* Ex. 1018 ¶¶ 74–77; *see also id.* ¶¶ 50–73. That is, the simulation performed by Dr. Horst shows that, under at least one set of design characteristics, the problems identified by Dr. Pedram do not exist. *Id.* ¶¶ 21–31 (Horst Supp. Decl.); Ex. 2007 ¶¶ 2–4 (Horst Corrective Decl.). Although the evidence does not show that every permutation of design characteristics will work, the evidence does show that it would have been within the ability of a person having ordinary skill in the art to determine appropriate design values to minimize or eliminate the potential problems identified by Dr. Pedram.

Reliability of Dr. Horst's Simulations: We do not agree with Patent Owner that Dr. Horst's simulation is unreliable because the results for two different circuits are identical. *See* PO Sur-reply 9 (citing Ex. 1018, ¶¶ 12, 23). As Patent Owner concedes, prior to his deposition, Dr. Horst prepared a corrective declaration pointing out the mistake and replacing the erroneous charts from page 15. *Id.* at 9–10; *see also* Ex. 2007 (Horst Corrective Decl). In light of Dr. Horst's recognition that he "inserted the wrong set of graphs when preparing [his] supplemental report" and timely provided a correction prior to cross examination, *see* Ex. 2007, ¶ 2, we do not find that the original mistake renders the simulation unreliable. To the contrary, we credit Dr. Horst for recognizing his mistake and providing the correct graphs.

Nor are we persuaded that the introduction of a second mistake in the corrective declaration renders the simulation unreliable. *See* PO Sur-reply 9–11. A comparison of the results of Dr. Horst's simulation relating to Figure 4 of the '674 patent and the combination of AAPA and Majcherczak from his Supplemental Declaration—the original simulation report—is reproduced below.



Simulations of the '674 Figure 4 circuit (left) and AAPA+ Majcherczak (right). Waveforms are nearly identical.

Ex. 1018 ¶ 23 (Horst Supp. Decl.). The figure above shows the results of Dr. Horst's simulation of the circuit of Figure 4 of the '674 patent (left) and the circuit that is the result of the combination of AAPA and Majcherczak (right). *Id.* Relevant to our analysis, the third graph for the Figure 4 circuit is labeled Is(M6). Patent Owner has not alleged any error in the labeling of this chart. *See generally* PO Sur-reply.

However, in the replacement graph of the Corrective Declaration, that graph is relabeled as Is(M2). Ex. 2007, ¶ 2 (Horst Corrective Decl.); *see also* PO Sur-reply. As Patent Owner points out in the Sur-reply, there is no transistor M2 in the Figure 4 embodiment. *See* Ex. 1018 ¶ 22. Because the labeling was correct in the original version and the correction focused on the graphs on the right side, not the left, this appears to be no more than a typographical error. As such, it does not have a substantial impact on Dr. Horst's credibility.

In conclusion, we have considered Patent Owner's arguments. However, based on the entirety of the record, we find Dr. Horst's simulations and Dr. Horst's discussion of those simulations reliable.

Selection of Simulation Values: Additionally, we are not persuaded by Patent Owner's argument that the values selected by Dr. Horst are divorced from real world considerations. First, Patent Owner argues that "Dr. Horst conceded, however, that his simulations enabled him to choose any desired threshold voltage, even if that voltage was inconsistent with the transistor's minimum feature size and the supply voltage." PO Sur-reply 15–16 (citing Ex. 2006, 93:3–13). However, Patent Owner's characterization is not consistent with Dr. Horst's testimony. Instead, during the cited cross-examination, Dr. Horst simply testified that "you can directly set the threshold value . . . not dependent on the – on that minimum feature size parameter"; he never stated that it was inconsistent with the minimum feature size, as argued by Patent Owner. Ex. 2006, 93:3–13.

Second, although Patent Owner argues that "when asked whether his selected threshold voltage of 2.3V would be typical for transistors having a 5V supply voltage and a minimum feature size of 0.8 μm, Dr. Horst conceded that he chose the 2.3V value simply because it 'gave good results,'" that is also not supported by the actual testimony. *See* PO Sur-reply 16 (citing Ex. 2006, 94:5–13). Dr. Horst was not asked whether the value was typical but instead stated that he made the selection because it gave expected results for the '674 patent Figure 4—the patented design. Ex. 2006, 94:5–13. Although the results may have been unreliable had Dr. Horst selected values designed to make AAPA/Majcherczak circuit provide good results, Patent Owner has not sufficiently explained why it is improper

to pick design parameters that would make the reference circuit (Figure 4 of the ’674 patent) work in the manner described in the ’674 patent. For the same reason, we are unpersuaded by Patent Owner’s argument that Dr. Horst “cherry picked” design parameters so that the circuit would work; rather, Dr. Horst simply testified that he adjusted the parameters to make reference ’674 patent Figure 4 circuit work. *Compare* PO Sur-reply 17, *with* Ex. 2006, 101:24–102:17.

Third, Patent Owner’s arguments that Dr. Horst used unrealistic parameter values, that the simulation fails to show that the combination does not result in increased leakage current, or that the simulation consisted of only a single simulation are not sufficient to rebut Petitioner’s persuasive evidence on why a person having ordinary skill in the art would have combined AAPA and Majcherczak. *See* PO Sur-reply 11–15, 17–19. Petitioner did not offer the simulation and testimony to demonstrate that a person having ordinary skill in the art would combine the references. Instead, Petitioner offered the simulation and Dr. Horst’s accompanying testimony to rebut Dr. Pedram’s testimony regarding potential problems with the circuit. *See* Pet. Reply 10–12. Because we are not persuaded by Dr. Pedram’s testimony regarding the potential problems, even if we accepted Patent Owner’s criticisms and discounted Dr. Horst’s simulation and accompanying testimony, Dr. Horst’s original testimony regarding the benefits of hysteresis detection is sufficient to demonstrate why a person having ordinary skill in the art would have been motivated to combine Majcherczak and AAPA.

Accordingly, for the reasons discussed above, Petitioner provided "some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *See Kahn*, 441 F.3d at 988.

c. Conclusion

We have considered the entirety of the evidence submitted by the parties, both for and against obviousness, and determine that Petitioner has shown by a preponderance of the evidence that claim 1 of the '674 patent would have been obvious over the combined teachings of AAPA and Majcherczak.

5. Claims 2, 5, and 6

Petitioner presents persuasive arguments and evidence regarding claims 2, 5, and 6, each of which depends from claim 1. *See* Pet. 57–62.

Claim 2 recites "wherein said one or more feedback circuits comprise: one or more first feedback transistors coupled in parallel with said one or more first transistors and coupled to receive feedback from said processing circuitry, wherein said one or more first feedback transistors are configured to switch off when said processing circuitry indicates that said first supply voltage is powered on." Ex. 1001, 9:4–11. Petitioner argues that the combination of AAPA and Majcherczak teaches the additional limitation recited in claim 2. Pet. 57–59; *see also* Ex. 1003 ¶¶ 141, 146 (Horst Decl.).

Claim 5 recites "further comprising: an input/output (I/O) network operative at a second supply voltage, wherein said I/O network is coupled to said core network and said control network, and wherein said I/O network is configured to receive said control signal." Ex. 1001, 9:34–39. Petitioner argues that the combination of AAPA and Majcherczak teaches the

additional limitation recited in claim 5. Pet. 59–60; *see also* Ex. 1003 ¶¶ 148–149 (Horst Decl.).

Claim 6 recites that "the device is integrated into a semiconductor die." Ex. 1001, 9:40–41. Petitioner argues that the combination of AAPA and Majcherczak teaches the additional limitation recited in claim 6. Pet. 61–62; *see also* Ex. 1003 ¶¶ 124, 125 (Horst Decl.).

Patent Owner does not separately address the additional limitations recited in claims 2, 5, and 6. *See generally* PO Resp.

Having considered the entirety of the evidence submitted by both parties, we determine that Petitioner has demonstrated by a preponderance of the evidence that claims 2, 5, and 6 of the '674 patent would have been obvious to a person of ordinary skill in the art based on the combined teachings of AAPA and Majcherczak.

6. Claims 8 and 17

Claims 8 and 17 are independent claims. Ex. 1001, 9:48–10:3, 11:14–12:5. Petitioner relies on the same combination of AAPA and Majcherczak discussed above in subsection 4(a)(1), and makes similar arguments regarding the limitations of claims 8 and 17. *Compare* Pet. 43–44, 46–56, *with* 1316 Pet. 51–52, 54–63. That is, Petitioner relies on the same combination of AAPA and Majcherczak and maps the limitations recited in method claim 8 and system claim 17 to the operation of the circuit. *See* 1316 Pet. 51–52, 54–63.

Patent Owner does not dispute that the combination of AAPA and Majcherczak teaches each of the limitations recited in claims 8 and 17. *See generally* 1316 PO Resp. 20–31; *see also* 1316 Pet. Reply 2 ("Beyond this procedural issue [on whether applicant admitted prior art could be

considered], Patent Owner's only substantive argument challenging Ground 2 is a purported lack of motivation to combine."); 1316 PO Sur-reply 2–19 (not disputing Petitioner's characterization of Patent Owner's argument).

We previously instructed Patent Owner that "any arguments for patentability not raised in the [Patent Owner Response] may be deemed waived." 1316 Paper 8, 5 (Scheduling Order); *see also NuVasive*, 842 F.3d at 1380–81 (determining Patent Owner waived arguments made only in its Preliminary Response but not raised in the Patent Owner Response after institution).

Based on the undisputed evidence before us and the reasons set forth in the Petition (Pet. 45–63), we find that the combination of AAPA and Majcherczak teaches all of the limitations recited in claims 8 and 17.

Petitioner and Patent Owner rely on the same arguments and evidence discussed above in subsections D(4)(b)(1) and (2) as to whether a person having ordinary skill in the art would have combined AAPA and Majcherczak. *Compare* Pet. 45; PO Resp. 20–31; Pet. Reply 2–12; PO Sur-reply 2–19, *with* 1316 Pet. 53; 1316 PO Resp. 20–31; 1316 Pet. Reply 2–12; 1316 PO Sur-reply 2–19.

For the reasons discussed above in subsection D(4)(b)(3), Petitioner provided "some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *See Kahn*, 441 F.3d at 988.

Accordingly, having considered the entirety of the evidence submitted by the parties, both for and against obviousness, we determine that Petitioner has shown by a preponderance of the evidence that claims 8 and 17 of the '674 patent would have been obvious over the combined teachings of AAPA and Majcherczak.

7. Claims 9, 12, 13, 16, and 18–21

Claims 9, 12, 13, and 18–21 depend, directly or indirectly, from claim 8 or 17. Ex. 1001, 10:4–10, 10:34–52, 11:7–13. 12:6–30.

Claims 9 and 13 recite "wherein said [decreasing/increasing] said current capacity comprises: receiving a first feedback signal from said signal processor at one or more first feedback transistors coupled in parallel with said one or more first transistors; and switching [off/on] said one or more first feedback transistors in response to said first feedback signal." Ex. 1001, 10:4–10, 10:45–51. Petitioner argues that the combination of AAPA and Majcherczak teaches the additional limitation recited in claims 9 and 13. 1316 Pet. 63–65; *see also* Ex. 1003 ¶¶ 142, 145 (Horst Decl.).

Claim 12 recites

> wherein said detecting said power-down comprises:
>
> > receiving a logic-low signal at said control gate of said one or more first and second transistors, wherein said one or more first transistors are configured to switch on in response to said logic-low signal, and wherein said one or more second transistors are configured to switch off in response to said logic-low signal; and
> >
> > transmitting a detection signal to a signal processor from said one or more first transistors based on said received logic-low signal.

Ex. 1001, 10:33–44. Petitioner argues that the combination of AAPA and Majcherczak teaches the additional limitations recited in claim 12. 1316 Pet. 66–68; *see also* Ex. 1003 ¶¶ 141, 144–146 (Horst Decl.).

Claim 18 recites a "means for providing a feedback signal associated with at least one of: said detected power-on or said detected power-down, wherein said feedback signal is used in said means for decreasing and said means for increasing." Ex. 1001, 12:6–10. Petitioner argues that the

combination of AAPA and Majcherczak teaches the additional limitation recited in claim 18. 1316 Pet. 68–70; *see also* Ex. 1003 ¶¶ 141, 145, 146 (Horst Decl.).

Claims 19 and 20 recite "wherein said means for [decreasing/increasing] said current capacity comprises: means, responsive to said feedback signal, for switching [off/on] one or more transistors of a plurality of transistors, wherein said plurality of transistors define said current capacity of said power on/off detector." Ex. 1001, 12:11–22. Petitioner argues that the combination of AAPA and Majcherczak teaches the additional limitation recited in claims 19 and 20. 1316 Pet. 70–72; *see* Ex. 1003 ¶¶ 141–143, 145, 146 (Horst Decl.).

Claim 21 recites that "the device is integrated into a semiconductor die." Ex. 1001, 12:23–24. Petitioner argues that the combination of AAPA and Majcherczak teaches the additional limitation recited in claim 21. 1316 Pet. 73; *see also* Ex. 1003 ¶¶ 124, 125 (Horst Decl.).

Patent Owner does not separately address the additional limitations recited in claims 9, 12, 13, 16, and 18–21. *See generally* 1316 PO Resp.

Having considered the entirety of the evidence submitted by both parties, we determine that Petitioner has demonstrated by a preponderance of the evidence that claims 9, 12, 13, 16, and 18–21 of the '674 patent would have been obvious to a person having ordinary skill in the art based on the combined teachings of AAPA and Majcherczak.

E. Obviousness over AAPA, Majcherczak, and Matthews

1. Overview of Matthews

Matthews is titled "Apparatus for Power-on Disable in a Multiple Power Supply System and a Method Therefor" and is directed "to a system

such as an embedded system that has multiple power supplies that are synchronized during initialization of the system." Ex. 1009, code (54), 1:9–12. More specifically, Matthews teaches an apparatus "for disabling portions of a system, circuit, etc. having multiple power supplies," which provides the advantages of disabling "certain portions of a system" "during system power-on or other times when power supply voltage levels may be changing," in order to prevent those portions "from generating erroneous data." *Id*. at 1:63–2:10.

2. Claim 7, 16 and 22

Claim 7 depends from claim 6 and recites that "the semiconductor die is incorporated in a device selected from a group consisting of a mobile phone, personal data assistant (PDA), navigation device, fixed location data unit, set-top box, music player, video player, entertainment unit, and computer." Ex. 1001, 9:42–47. Claims 16 and 22 recite a substantially similar limitation. *See id.* at 11:7–13, 12:25–30.

Petitioner argues Matthews teaches the additional limitation recited in claims 7, 16, and 22. *See* Pet. 62–64; 1316 Pet. 74–76; *see also* Ex. 1003 ¶¶ 152–155. Specifically, Petitioner argues Matthews teaches that the system in which its "power-on disable module is integrated 'may be a wireless communication device [e.g., a mobile phone] or a system board or component thereof, or a computer system, a system board or peripheral device thereof." Pet. 63 (quoting Ex. 1009, 5:35–37); 1316 Pet. 75 (quoting Ex. 1009, 5:35–37) (emphasis in original). Petitioner further argues that a person having ordinary skill in the art "would have found it obvious to utilize the POC system 10 described in the AAPA to be used in 'wireless communication device [e.g., a mobile phone] or a system board or

component thereof, or a computer system, a system board or peripheral device thereof.'" Pet. at 63–64 (quoting Ex. 1003 ¶ 155); 1316 Pet. 76 (quoting Ex. 1003 ¶ 155).

Patent Owner does not separately address the additional limitations recited in claims 7, 16, and 22. *See generally* PO Resp.; 1316 PO Resp. Instead, Patent Owner argues that "the addition of Matthews does not remedy any of the deficiencies noted above for the combination of the alleged AAPA and Majcherczak (Ground 2a), and Petitioner's obviousness argument as to claim 7 fails for the same reasons that its arguments for claims 1, 2, 5, and 6 fail." PO Resp. 31; *see also* 1316 PO Resp. 32 (for claims 16 and 22).

Patent Owner's arguments about AAPA and Majcherczak are not persuasive for the reasons given above. We are persuaded by Petitioner's analysis of the evidence cited in the Petition and find Petitioner has shown that the combination of AAPA, Majcherczak, and Matthews teaches the additional limitation recited in claims 7, 16, and 22. Additionally, for the reasons given in the Petition, we are also persuaded by Petitioner's arguments that a person having ordinary skill in the art would have combined the teachings of Matthews with the teachings of AAPA and Majcherczak and that there would have been a reasonable expectation of success.

Having considered the entirety of the evidence submitted by both parties, we determine that Petitioner has demonstrated by a preponderance of the evidence that claims 7, 16, and 22 of the '674 patent would have been obvious to a person of ordinary skill in the art based on the combined teachings of AAPA, Majcherczak, and Matthews.

F. Obviousness over Steinacker, Doyle, and Park

1. Overview of Steinacker

Steinacker is titled "Circuit Arrangement Receiving Different Supply Voltages" and is directed to a circuit arrangement including a first circuit block operating at a first supply voltage and second circuit block operating at a second supply voltage. Ex. 1005, codes (54), (57). According to Steinacker, such an arrangement is frequently used in mobile radio technology. *Id*. at 1:18–29.

2. Overview of Doyle

Doyle is titled "CMOS Input Level Shifting Circuit with Temperature-Compensating N-Channel Field Effect Transistor Structure" and is directed "to temperature-compensated field effect transistor circuits and to inverting CMOS circuits having trip points or switching points that are compensated for variations in temperature and are relatively independent of certain manufacturing process parameter variations." Ex. 1006, code (54), 1:7–13. Doyle's Figure 2 is reproduced below.

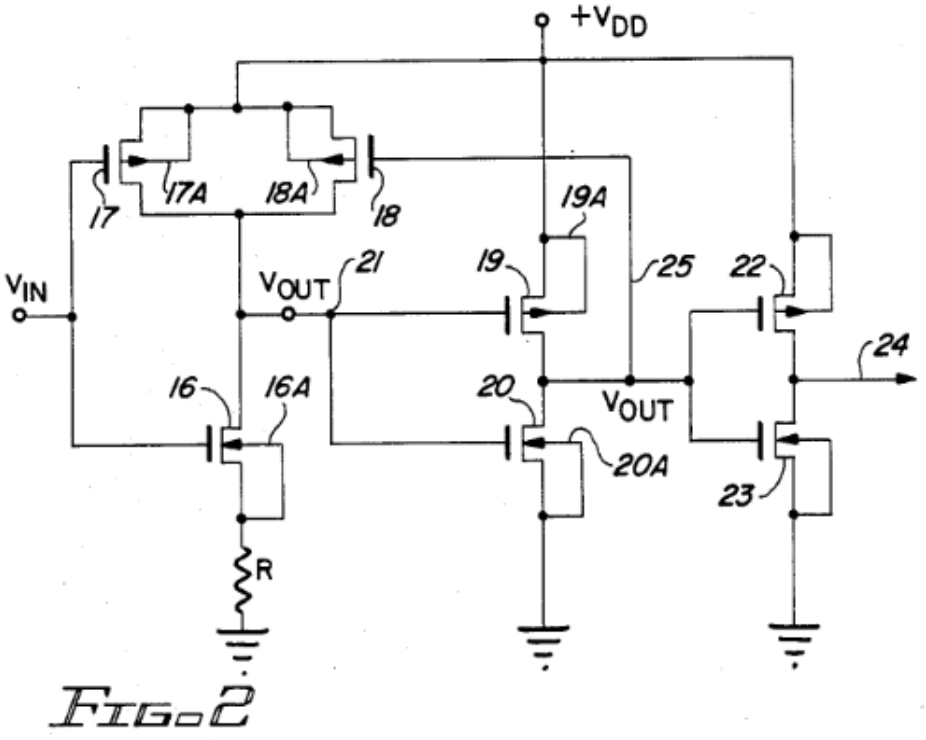


FIG-2

Id. at Fig. 2. Figure 2 "is a schematic circuit diagram of a self adjusting TTL [(transistor-transistor logic)] compatible input circuit according to the present invention." *Id*. at 3:35–37. According to Doyle, an "object of the invention [is] to provide a MOSFET circuit structure that, in effect, produces a MOSFET drain current having a predetermined amount or range of variation with respect to temperature and/or certain MOS processing parameters." *Id*. at 2:32–36.

3. Overview of Park

Park is titled "Sleepy Stack Leakage Reduction" and is directed to an "ultra-low leakage CMOS circuit structure" that "can retain logic state during sleep mode while achieving ultra-low leakage power consumption." Ex. 1007, 1. According to Park, "[a]lthough the sleepy stack incurs some delay and area overhead, the sleepy stack technique achieves the lowest leakage power consumption among known state-saving leakage reduction

techniques, thus, providing circuit designers with new choices to handle the leakage power problem." *Id*.

Park briefly mentions the forced stack technique, an older technique "to reduce leakage power." Ex. 1007, 2. According to Park, the "sleepy stack structure can achieve more power savings than the forced stack technique and the self-controlled stacked transistors" and "can save exact logic state unlike gated-V_{dd} and gated-Gnd techniques (conventional sleep transistor technique) and the zigzag technique." *Id*.

4. Claims 1, 2, 5–9, 12, 13, and 16–22

a. Combination of Steinacker and Doyle

(1) Petitioner's Arguments

Petitioner argues that the combination of Steinacker, Doyle, and Park teaches all of the limitations of claims 1, 2, 5–9, 12, 13, and 16–22. Pet. 11–37; 1316 Pet. 10–44. Specifically, Petitioner argues that a person having ordinary skill in the art "would have found it obvious that the voltage detector 5 of Steinacker's circuit arrangement 1 to be implemented as shown in the following reproduction of Doyle's FIG. 2 in which black annotations describing how the inverter would be connected in the circuit arrangement have been added." Pet. 18; 1316 Pet. 17.

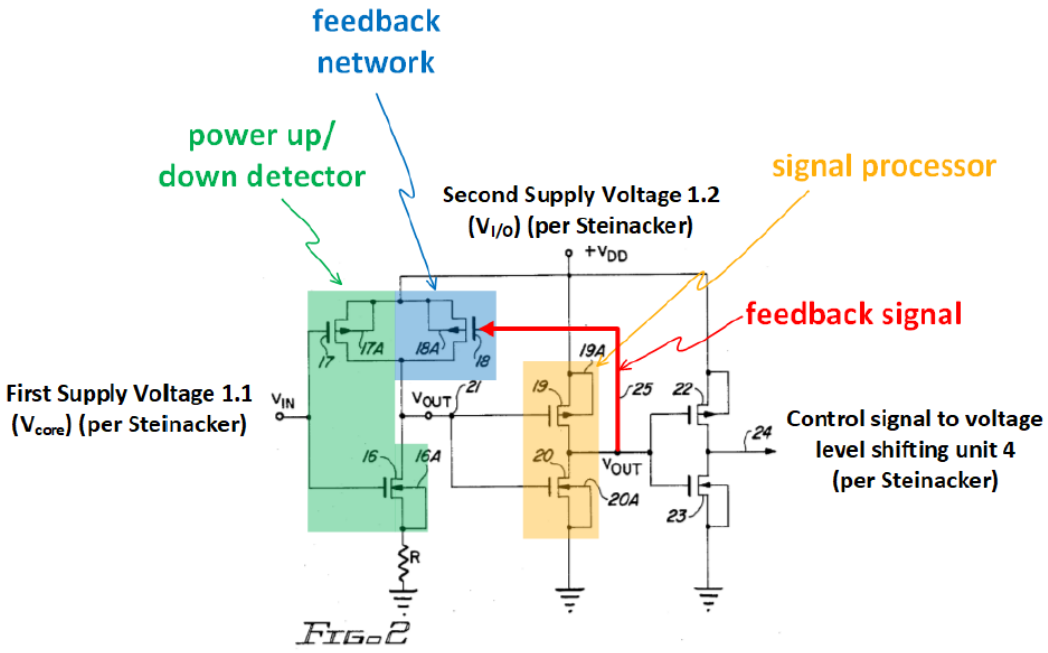


Fig. 2

Pet. 19; 1316 Pet. 18. According to Petitioner, the figure above shows the combination of the teachings of Steinacker—the first supply voltage, the second supply voltage, and the control signal to voltage shifting unit 4—with the Figure 2 embodiment of Doyle. Pet. 18–19; 1316 Pet. 17–18. Additionally, the figure has been annotated by Petitioner to identify what components Petitioner argues teach various claim limitations, such as the power up/down detector, the feedback network, the signal processor, and the feedback signal. Pet. 19; 1316 Pet. 18.

Petitioner further argues that "Steinacker describes that the voltage level detector 5 of circuit arrangement 1 can take the form of an inverter, but leaves selection of an appropriate inverter to a POSITA." Pet. 21 (citing Ex. 1003 ¶¶ 93, 103; Ex. 1005 4:49–55); 1316 Pet. 20 (citing same). Petitioner further argues that because "Doyle describes that its inverter 'has a trip point that is relatively stable with respect to temperature and/or to certain CMOS manufacturing process parameters,' particularly as compared to the basic

well-known CMOS inverter shown in FIG. 2A," a person of ordinary skill in the art would have used the inverter shown in Doyle's Figure 2 with Steinacker. Pet. 21 (citing Ex. 1003 ¶ 108; Ex. 1006, 2:37–40, 5:60–61); 1316 Pet. 20 (citing same); *see also* Pet. Reply 20 ("The additional benefit of Doyle's inverter as being 'very independent of temperature' (realized via resistor R) is also relevant to Steinacker, because Steinacker intended its circuit arrangement 1 to be used in mobile communication devices (see [Ex. 1005], 1:18-20, 3:19-22) and it was well known that '[m]obile phone is subjected to very harsh environmental conditions compared to many commercial products" including "temperature and or humidity extremes and dusty conditions.'" (citing Ex. 1018 ¶ 42)); 1316 Pet. Reply 20 (same); Ex. 1019, 2, 5 (Perera article). Petitioner further argues that the combination "would have been simple substitution of one known element (basic well-known CMOS inverter) for another (Doyle's improved inverter) to obtain predictable results." Pet. 21 (citing Ex. 1003 ¶ 108); 1316 Pet. 20 (same).

In its Reply, Petitioner argues that a person of ordinary skill in the art would have selected the improved inverter of Doyle's Figure 2 because it

> includes a "second P-channel pullup MOSFET . . . provided in parallel with the first, and has its gate coupled to a feedback signal produced by a second CMOS inverting stage in order to provide a 'polarized' hysteresis characteristic of the MOS level shifting circuit, making the trip point or switching point of the MOS level shifting circuit relatively independent of the power supply voltage applied across the CMOS level shifting circuit."

Pet. Reply 18 (quoting Ex. 1006, 3:7–14) (emphasis in original); 1316 Pet. 18 (same). According to Petitioner, "[t]he feedback transistor 18 in FIG. 2 is the source of the hysteresis effect, and provides Doyle's advantage of a 'stable trip point or switching point.'" Pet. Reply 19 (quoting Ex. 1006,

3:17–14) (citing Ex. 1018 ¶ 40); 1316 Pet. Reply 19 (same). According to Petitioner, a person having ordinary skill in the art "would have had additional motivation to select Doyle's improved inverter when implementing Steinacker's voltage detector 5, because Doyle described its improved inverter as providing 'relatively high noise immunity' and Steinacker wanted its circuit arrangement 1 to remain reset until the input voltage is reliably above the higher threshold." Pet. Reply 19–20 (citing Ex. 1006, 2:14–26; Ex. 1005, 1:57–2:10, 3:9–14; Ex. 1018 ¶ 41); 1316 Pet. Reply 19–20 (same).

(2) Patent Owner's Arguments

First, Patent Owner argues that Petitioner's reasons for combining Doyle and Steinacker are based on impermissible hindsight. PO Resp. 32–36, 40–42; 1316 PO Resp. 33–37, 41–43. Specifically, Patent Owner argues that "[t]he best evidence of the use of impermissible hindsight reconstruction in the petition is Petitioner's own diagram" (shown in the previous section) which shows a circuit that "does not include a single component from [the primary reference] Steinacker." PO Resp. 33–34; 1316 PO Resp. 33–34. Patent Owner further argues that "[a]bsent hindsight reconstruction, there is no conceivable reason why the [person having ordinary skill in the art] would have looked to a 1986 CMOS-TTL interface for use in a multiple supply voltage up/down detector." PO Resp. 35; 1316 PO Resp. 36; *see also* Ex. 2002 ¶ 95 (Pedram Decl.) (discussing differences in Steinacker and Doyle). Patent Owner also argues that the impermissible hindsight reproduction is demonstrated by Petitioner's improper use of the '674 patent as a guide. PO Resp. at 37–41; 1316 PO Resp. 38–42.

Second, Patent Owner argues that the reasons given in the Petition for combining Steinacker and Doyle are generic statements divorced from the prior art elements. PO Resp. 42–44; 1316 PO Resp. 43–45. Specifically, Patent Owner argues Petitioner's rationale for the combination—"to achieve a stable trip point"—"is not tailored to the references under consideration and provides no explanation of why a stable trip point would be desirable in Steinacker." PO Resp. 42 (citing Pet. 17; Ex. 2002 ¶ 106); 1316 PO Resp. 43 (same). Patent Owner further argues that Petitioner does not "explain why the POSA would look to a CMOS-TTL interface, much less one aimed at compensating for changes in temperature, to provide an inverter in Steinacker's system that includes no TTL components." PO Resp. 42; 1316 PO Resp. 43. Patent Owner also argues that Petitioner does not address the disadvantages associated with making the modification. PO Resp. 43–44; 1316 PO Resp. 44–45.

Third, Patent Owner argues that because the reason given for the modification in Petitioner's Reply—using a level detector with hysteresis—is not set forth in the Petition, it is improper and should not be considered. PO Sur-reply 19–21; 1316 PO Sur-reply 19–21; *see also* PO Sur-reply 20 ("But a reply is too late to submit this kind of extensive new evidence and argument. *See* Office Patent Trial Practice Guide, August 2018 Update at 14 ('Petitioner may not submit new evidence or argument in reply that it could have presented earlier, *e.g.* to make out a prima facie case of unpatentability.'); *Intelligent Bio-Systems, Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1369 (Fed. Cir. 2016)."); 1316 PO Sur-reply 20 (same). Moreover, according to Patent Owner, Petitioner's new argument is wrong. *See* PO Sur-reply 21–23; 1316 PO Sur-reply 21–23.

(3) Our Analysis

(a) Whether Petitioner Raises a New Theory in Petitioner's Reply

In an *inter partes* review, "Petitioner may not submit new evidence or argument in reply that it could have presented earlier, *e.g.* to make out a prima facie case of unpatentability." Trial Practice Guide Update (August 2018), 14, *available at* https://www.uspto.gov/sites/default/files/documents/2018_Revised_Trial_Practice_Guide.pdf. As the Federal Circuit has explained,

> [i]t is of the utmost importance that petitioners in the IPR proceedings adhere to the requirement that the initial petition identify "with particularity" the "evidence that supports the grounds for the challenge to each claim." 35 U.S.C. § 312(a)(3). "All arguments for the relief requested in a motion must be made in the motion. A reply may only respond to arguments raised in the corresponding opposition or patent owner response." 37 C.F.R. § 42.23(b). Once the Board identifies new issues presented for the first time in reply, neither this court nor the Board must parse the reply brief to determine which, if any, parts of that brief are responsive and which are improper. As the Board noted, "it will not attempt to sort proper from improper portions of the reply." Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756, 48,767 (Aug. 14, 2012).

Intelligent Bio-Sys., 821 F.3d at 1369 (Fed. Cir. 2016); *see also Acceleration Bay, LLC v. Activision Blizzard Inc.*, 908 F.3d 765, 775 (Fed. Cir. 2018) (quoting same). Based on those standards, the Federal Circuit found the PTAB properly refused to consider a new theory raised for the first time in a reply brief:

> Unlike district court litigation—where parties have greater freedom to revise and develop their arguments over time and in response to newly discovered material— the expedited nature

> of IPRs bring with it an obligation for petitioners to make their case in their petition to institute. While the Board's requirements are strict ones, they are requirements of which petitioners are aware when they seek to institute an IPR.
>
> . . . .
>
> . . . In these circumstances, we find that the Board did not err in refusing the reply brief as improper under 37 C.F.R. § 42.23(b) because [the petitioner] relied on an entirely new rationale to explain why one of skill in the art would have been motivated to combine Tsien or Ju with a modification of Zavgorodny.

Intelligent Bio-Sys., 821 F.3d at 1369–70.

The Petition contains a single paragraph discussing why a person having ordinary skill in the art would combine Steinacker and Doyle. *See* Pet. 21. Specifically, Petitioner argues that a person of ordinary skill in the art

> seeking to implement [Steinacker's] voltage level detector 5 of circuit arrangement 1 would have been motivated to utilize the inverter shown in FIG. 2 of Doyle, because Steinacker is without details regarding the implementation of an inverter and Doyle describes that its inverter "has a trip point that is relatively stable with respect to temperature and/or to certain CMOS manufacturing process parameters," particularly as compared to the basic well-known CMOS inverter shown in FIG. 2A.

Id. (citing Ex. 1006, 2:37–40, 5:60–61; Ex. 1003 ¶ 108). The Petition did not discuss hysteresis in the reason to combine. *See id.*

In the Institution Decision, we noted "concerns regarding whether Petitioner's arguments and evidence are based on impermissible hindsight." Inst. Dec. 38; 1316 Inst. Dec. 38. Specifically, with regard to Petitioner's proposed combination of Doyle and Steinacker we stated that

> Petitioner provides generic reasons for combining the various limitations. That is, although Petitioner argues that person of ordinary skill in the art would select the inverter from Doyle to be incorporated into Steinacker because it "has a trip point that is relatively stable with respect to temperature and/or to certain CMOS manufacturing process parameters," (Pet. 21 (quoting Ex. 1006, 2:37–40)), Petitioner does not explain persuasively why a person of ordinary skill in the art at the time of the invention would have considered those factors important. Nor does Petitioner explain why a person of ordinary skill in the art in 2009 (the filing date of the '674 patent) would turn to a 1986 reference (Doyle) to select an inverter to be used in a circuit from 2005 (U.S. filing date of Steinacker). Although the evidence shows that a person of ordinary skill in the art *could* have used the Doyle inverter, we have concerns whether the evidence is sufficient to demonstrate why a person of ordinary skill in the art *would* have done so. *See Personal Web Techs., LLC v. Apple, Inc.*, 848 F.3d 987, 993–94 (Fed. Cir. 2017) ("But that reasoning seems to say no more than that a skilled artisan, once presented with the two references, would have understood that they could be combined. And that is not enough: it does not imply a motivation to pick out those two references and combine them to arrive at the claimed invention.").

Inst. Dec. 38–39; 1316 Inst. Decl. 38–39. In light of that concern, we requested that the parties brief the issue during trial and to focus on the following issues:

> (1) whether impermissible hindsight was used in the selection and combination of the prior art, (2) *whether the reasons given in the Petition are generic statements divorced from the prior art elements or focus on the specific references used*, and (3) whether a person of ordinary skill in the art would have selected the forced stack technique over the sleepy stack technique.

Inst. Dec. 40 (emphasis added); 1316 Inst. Dec. 40. Although we requested further briefing on Petitioner's reason to combine Steinacker and Doyle, we did not authorize Petitioner to develop a new theory. *See id.* at 39–40.

On the one hand, in the Petitioner's Reply, Petitioner presented additional evidence which Petitioner argues supports the statement in the Petition regarding to need for an inverter that was stable with respect to temperature. *See* Pet. Reply 20; 1316 Pet. Reply 20. Specifically, the first full paragraph on page 20 of Petitioner's Reply states:

> Far from being "generic statements divorced from the prior art elements," a POSITA would have understood that the Doyle's description of its improved inverter exactly satisfies the specifications of Steinacker voltage level detector 5. [Ex. 1018] ¶¶40-42. The additional benefit of Doyle's inverter as being "very independent of temperature" (realized via resistor R) is also relevant to Steinacker, because Steinacker intended its circuit arrangement 1 to be used in mobile communication devices (*see* [Ex. 1005], 1:18-20, 3:19-22) and it was well known that "[m]obile phone is subjected to very harsh environmental conditions compared to many commercial products" including "temperature and or humidity extremes and dusty conditions." [Ex. 1018] ¶42 (citing [Ex. 1019], 2, 5).

Pet. Reply 20; 1316 Pet. Reply 20. Because this paragraph and the cited evidence merely provides reply evidence and argument related to a theory presented in the Petition, that evidence and argument will be considered. *Compare* Pet. 21 (arguing "Doyle describes that its inverter 'has a trip point that is relatively stable with respect to temperature . . . .'" (citation omitted)); 1316 Pet. 20 (same), *with* Pet. Reply 20 (arguing Doyle as "very independent of temperature" and that is an important feature for mobile phones (citations omitted)); 1316 Pet. Reply 20 (same)).

On the other hand, Petitioner focuses much of its argument and evidence relating to the reason to combine Steinacker and Doyle on hysteresis. *See* Pet. Reply 14–20; 1316 Pet. Reply 14–20; Ex. 1018 ¶¶ 38–42 (Horst Supp. Decl.) (section titled "Motivation to utilize Doyle's inverter

with hysteresis as Steinacker's voltage detector 5"). However, Petitioner did not argue in the Petition that a person having ordinary skill in the art would combine Steinacker with Doyle in order to provide a hysteresis. *See* Pet. 21; 1316 Pet. 20; Ex. 1003 ¶ 108 (Horst Decl.). That is, although hysteresis was mentioned at various points in the Petition and Dr. Horst's testimony, it was not relied upon as the reason to combine the Steinacker and Doyle. *See* Pet. 21.

During the Oral Hearing, Petitioner argued that Dr. Horst testified in his original declaration that Steinacker recognizes the advantage of introducing hysteresis in voltage detection circuits. Tr. 26:4–18 (citing Ex. 1003 ¶ 53). Merely citing evidence without identifying its use in the Petition is not sufficient. Petitioner should not expect the Board to search the record and piece together the evidence that may support Petitioner's arguments. *See* 37 C.F.R. § 42.22(a)(2) (2019) (the "petition . . . must include . . . [a] full statement of the reasons for the relief requested"); *DeSilva v. DiLeonardi*, 181 F.3d 865, 866–67 (7th Cir. 1999) ("A brief must make all arguments accessible to the judges, rather than ask them to play archeologist with the record."). By statute, a petition is required to identify "with particularity[] the grounds on which the challenge to each claim is based, and the evidence that supports the grounds for the challenge." 35 U.S.C. § 312(a)(3) (2012). The petition shall also include a "full statement" with "a detailed explanation of the significance of the evidence, including material facts." 37 C.F.R. § 42.22(a)(2) (2019). In that regard, our rules require a petition to include both an adequate explanation of how the claims should be construed, as well as information sufficient to show how and why the properly construed claims are unpatentable over the asserted prior art. 37

C.F.R. § 42.104(b)(3), (b)(4) (2019). A petition should also "explain why a person of ordinary skill in the art would have combined elements from specific references in the way the claimed invention does." *ActiveVideo Networks, Inc. v. Verizon Comm'ns, Inc.*, 694 F.3d 1312, 1328 (Fed. Cir. 2012). The fact that a potential reason to combine references is hidden in the evidentiary record does not persuade us that Petitioner did not raise a new argument in the Petitioner's Reply. Accordingly, we do not consider that new theory.[18]

(b) Whether the Petition Established a Sufficient Reason to Combine Steinacker and Doyle

It is Petitioner's "burden to demonstrate both that a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention, and that the skilled artisan would have had a reasonable expectation of success in doing so." *In re Magnum Oil Tools Int'l, Ltd.*, 829 F.3d 1364, 1381 (Fed. Cir. 2016) (quotations omitted); *see also KSR*, 550 U.S. at 418. Moreover, a petitioner cannot satisfy this burden by "employ[ing] mere conclusory statements" and "must instead articulate specific reasoning, based on evidence of record" to support an obviousness determination. *Magnum Oil*, 829 F.3d at 1380. Stated differently, there must be "articulated reasoning with some rational

[18] Although our Trial Practice Guides states that we "will not attempt to sort proper from improper portions of the reply" (Office Patent Trial Practice Guide, 77 Fed.Reg. 48,756, 48,767 (Aug. 14, 2012), in the interests of justice, we will only not consider the new theory. *See* 37 C.F.R. § 42.5(a), (b) (2019)

underpinning to support the legal conclusion of obviousness." *KSR*, 550 U.S. at 418 (quoting *Kahn*, 441 F.3d at 988).

The "factual inquiry" into the reasons for "combin[ing] references must be thorough and searching, and the need for specificity pervades . . . ." *In re Nuvasive, Inc.*, 842 F.3d 1376, 1381–82 (Fed. Cir. 2016) (quotations omitted). The reason cannot focus on generic statements divorced from the prior art elements, such as the generic desire to "build something better" or to make it "more efficient, cheaper, or . . . more attractive to [one's] customers." *ActiveVideo*, 694 F.3d. at 1328; *see also Nuvasive*, 842 F.3d at 1382–85 (holding that an obviousness determination cannot be reached where there is no "articulat[ion of] a *reason why* a [person having ordinary skill in the art] would combine" and "modify" the prior art teachings). This required explanation as to why the references would be combined avoids an impermissible "hindsight reconstruction," using "the patent in suit as a guide through the maze of prior art references, combining the right references in the right way so as to achieve the result of the claims in suit." *NTP*, 654 F.3d at 1299 (quoting *Grain Processing Corp. v. American-Maize Prods. Co.*, 702 F.2d 1005, 1012 (Fed. Cir. 1983)).

Having reviewed the record, Petitioner has not shown by a preponderance of the evidence that a person of ordinary skill in the art at the time of the invention would have combined the teachings of Steinacker and Doyle in the manner argued in the Petition. For example, although Petitioner argues that person of ordinary skill in the art would select the inverter from Doyle to be incorporated into Steinacker because it "has a trip point that is relatively stable with respect to temperature and/or to certain CMOS manufacturing process parameters," Petitioner does not explain

persuasively why a person of ordinary skill in the art at the time of the invention would have considered those factors important. *See* Pet. 21 (quoting Ex. 1006, 2:37–40); 1316 Pet. 20 (same)

First, with regard to CMOS manufacturing process parameters, Petitioner does not provide any evidence why a person of ordinary skill in the art at the time of the invention would have been concerned about having a trip point that is relatively stable with respect to certain CMOS manufacturing process parameters. *See* Ex. 1003 ¶ 108 (Horst Decl.); Ex. 1018 ¶ 42 (Horst Supp. Decl.). Although Dr. Horst provided some testimony regarding temperature, discussed below, he does not offer any persuasive evidence regarding manufacturing process parameters. *See* Ex. 1003 ¶ 108 (Horst Decl.); Ex. 1018 ¶ 42 (Horst Supp. Decl.); Ex. 2002 ¶¶ 106–107 (Pedram Decl.).

Second, we are not persuaded that the new evidence submitted with Petitioner's Reply sufficiently shows that a person having ordinary skill in the art would have been concerned with a trip point that is relatively stable with respect to temperature. *See* Pet. Reply 20; 1316 Pet. Reply 20. Although Petitioner and Dr. Horst rely on a 1995 article regarding, i*nter alia*, environmental factors, including temperature, that a mobile phone may be subject to, Petitioner has not cited to any evidence establishing that temperature concerns were still an issue at the time of the invention of the '674 patent. That is, a 1995 article does not sufficiently show that a person of ordinary skill in the art in 2009 (the filing/invention date of the '674 patent) would turn to a 1986 reference (Doyle) to select an inverter to be used in a circuit from 2005 (U.S. filing date of Steinacker).

Third, Petitioner has not shown that the portions of Doyle Petitioner is relying on provided the benefit of a stable trip point. Indeed, Petitioner has not provided any evidence linking the entire structure from Doyle it is incorporating into Steinacker to the supposed benefit of a stable trip point. Doyle refers to the trip point as the point in which V_{in} is equal to V_{out}. Ex. 1006, 4:35–38. Petitioner does not identify what portions of Doyle's Figure 2—if any—provide the benefit of the relatively stable trip point. *See, e.g.*, *id.* at 7:17–24 (stating that "the resistance of resistor R can be selected to cause trip points 8 and 8A (FIGS. 3A and 3B, respectively), to be very independent of temperature and certain processing parameter variations"); *see also* Ex. 2002, ¶ 106 n.1 (Pedram Decl.) (testifying that "[Petitioner] does not make any use of Doyle's solution to the trip point stability problem, which is to connect both source and bulk terminals of the bottom NMOS transistor in his inverter circuit to a resistor, resulting in a 'self-compensating MOSFET' arrangement." (citing Ex. 1006, 7:17–24)). Because Petitioner does not link the portions of Doyle's circuit that it is relying on to temperature stability—the benefit Petition seeks to add to Steinacker—Petitioner's argument is not sufficient.

At most, the evidence shows that a person of ordinary skill in the art *could* have used the Doyle inverter. However, Petitioner has not shown why a person of ordinary skill in the art *would* have had reason to do so. *See Personal Web Techs., LLC v. Apple, Inc.*, 848 F.3d 987, 993–94 (Fed. Cir. 2017) ("But that reasoning seems to say no more than that a skilled artisan, once presented with the two references, would have understood that they could be combined. And that is not enough: it does not imply a motivation

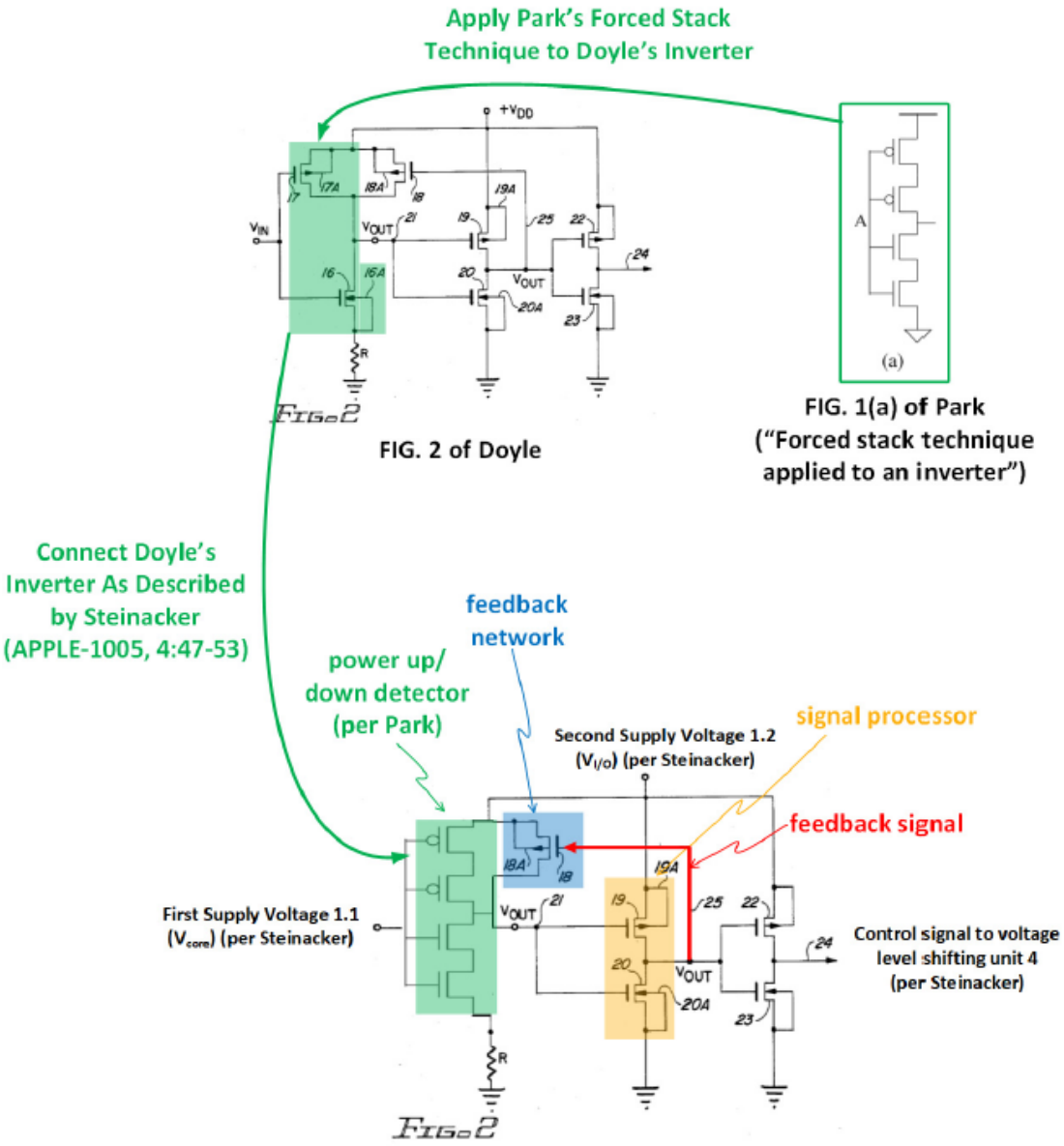
to pick out those two references and combine them to arrive at the claimed invention.").

Because Petitioner's argument requires elements from both Steinacker and Doyle, Petitioner's failure to identify a sufficient rationale for combining the references is fatal to its argument that claims 1, 2, and 5–9, 12, 13, and 16–22 are unpatentable over Steinacker in view of Doyle and Park.

b. Combination of Steinacker, Doyle and Park

(1) The Parties' Arguments

Petitioner argues that a person of ordinary skill in the art would have employed "Park's forced stacking technique in the inverter taught by Doyle" so "that the P channel MOSFET 17 of Doyle's inverter could be replaced by two P channel MOSFETs having half the size and the N channel MOSFET 16 of Doyle's inverter could be replaced by two N channel MOSFETs having half the size." Pet. 19; 1316 Pet. 18. The figure reproduced below illustrates Petitioner's combination.



Pet. 20; 1316 Pet. 19. According to Petitioner, the figure reproduced above shows Park's Figure 1(a), which shows the forced stack technique applied to an inverter, Doyle's Figure 2, and a modified version of Doyle's Figure 2 showing the application of the forced stack technique applied to transistors 17 and 18. Pet. 20; 1316 Pet. 19.

Petitioner further argues that "Park describes several techniques for reducing power consumption of an inverter, including a previously known 'forced stack' technique shown in FIG. 1a and a new proposed 'sleepy stack' technique shown in FIG. 2." Pet. Reply 22 (citing Ex. 1007, 2–3); 1316 Pet. Reply 22 (same). Petitioner argues that a person of ordinary skill in the art would have used the forced stack technique of Park with the Doyle inverter in order to reduce the subthreshold leakage current. Pet. 21–22 (citing Ex. 1003 ¶ 112); Pet. Reply 22; 1316 Pet. 20–21 (citing Ex. 1003 ¶ 112); 1316 Reply Pet. 22. Petitioner further argues that "using Park's forced stack technique would have been simple substitution of one known element (a two-transistor inverter) for another (a four-transistor inverter) to obtain predictable results (improve leakage current)." Pet. 22 (citing Ex. 1003 ¶ 112); 1316 Pet. 21 (same).

Petitioner further argues that a person of ordinary skill would have chosen the forced stack technique over sleepy stack technique. Pet. Reply 22–23; 1316 Pet. Reply 22–23. Specifically, Petitioner argues that the forced stack technique only requires four transistors while the sleepy stack technique requires six, two of which are driven by sleep signals. Pet. Reply 22–23 (citations omitted); 1316 Pet. Reply 22–23 (same). According to Petitioner, neither Steinacker nor Doyle have a sleep signal. Reply Pet. 23 (citations omitted); 1316 Reply Pet. 23. Petitioner also argues that "the forced stack technique offers several potential benefits over the sleep stack technique" and the sleep stack technique is only advantageous for certain applications. Reply Pet. 23 (citations omitted); 1316 Reply Pet. 23.

Patent Owner raises several arguments challenging the combination.

First, Patent Owner argues neither Doyle nor Steinacker discuss any problem relating to current leakage. PO. Resp. 36 (citing Ex. 2002 ¶¶ 97–98); 1316 PO Resp. 37 (same). Therefore, according to Patent Owner, there would have been no reason for a person of ordinary skill in the art to look to Park. PO Resp. 36, 41–42; 1316 PO Resp. 37, 42–43. Additionally, Patent Owner argues that current leakage is generic rationale that would apply to every circuit with a FET and "falls short of the articulated reasoning with rational underpinning required by *KSR*." PO Resp. 42; 1316 PO Resp. 43.

Second, Patent Owner argues if a person of ordinary skill in the art would have considered using Park's teaching of reducing current leakage, the person "would not have done so using the forced stack circuit from Park. Rather, the [person having ordinary skill in the art] would have used the superior 'sleepy stack' technique that is the focus of Park." PO Resp. 44 (citing Ex. 1007; Ex. 2002 ¶ 110); 1316 PO Resp. 45 (citing same); *see also* PO Resp. 45 ("As explained by Dr. Pedram, even if the [person having ordinary skill in the art] sought to reduce leakage current in Doyle using the teachings of Park, the [person having ordinary skill in the art] would have selected Park's sleepy stack technique over the older forced stack technique." (citing Ex. 2002, ¶¶ 110–113)); 1316 PO Resp. 46 (same). Specifically, Patent Owner argues that "Park explains that the sleepy stack technique provides up to two orders of magnitude more leakage power reduction compared to the forced stack technique at the cost of some additional delay and area overhead." PO Resp. 45 (citing Ex. 1007, 1250; Ex. 2002 ¶ 112); 1316 PO Resp. 46 (citing same). Patent Owner also argues that the additional logic circuitry or connection needed to generate the sleep signal for the sleepy stack would have been within the capability of the

person having ordinary skill of the art. PO Sur-reply 24; 1316 PO Sur-reply 24.

Third, Patent Owner argues Petitioner's rationale is deficient because it is only partially applied. *See* PO Resp. 41–42. 1316 PO Resp. 42–43; PO Sur-reply 24; 1316 PO Sur-reply 24. That is, Patent Owner argues that Petitioner's argument to apply Park to some, but not all, transistors without an explanation demonstrates that Petitioner did not provide a sufficient rationale.

Fourth, Patent Owner argues that Petitioner introduced a new argument in the Petitioner's Reply. PO Sur-reply 23; 1316 PO Sur-reply 23. Specifically, Patent Owner argues the Petitioner's argument that a person of ordinary skill "would be motivated to combine Park with Steinacker because Steinacker may be used for mobile applications, and the [person having ordinary skill in the art] would therefore be motivated to apply Park's techniques for lowering leakage current" is a new argument that was not made in the Petition. PO Sur-reply 23 (citations omitted); 1316 PO Sur-reply 23 (same).

(2) Our Analysis

We do not decide whether Petitioner raised a new rationale for using Park in its Reply. Whether reduced power consumption (the reason provided in the Reply) is the same as reduced leakage current (the reason provided in the Petition), neither reasoning is sufficient to provide a reason to combine the references in the manner suggested by the Petitions.

The Federal Circuit has held the reason for combining references cannot focus on generic statements divorced from the prior art elements, such as the generic desire to "build something better" or to make it "more

efficient, cheaper, or . . . more attractive." *ActiveVideo*, 694 F.3d. at 1328. Reduced leakage current and power consumption in Petitioner's arguments are no more than generic concerns that exist in many, if not all, electronic devices. Accordingly, they are, individually or combined, nothing more than a generic reason to make something better. Because Petitioner has not sufficiently linked the concerns to the prior are elements, neither reason is an "articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *See KSR*, 550 U.S. at 418 (quoting *Kahn*, 441 F.3d at 88).

Moreover, even if a person of ordinary skill in the art would have been concerned about current leakage or power consumption, Petitioner has not sufficiently or persuasively shown why a person having ordinary skill in the art would use the forced stack technique over the sleepy stack technique. Although Park briefly discusses the forced stack technique, the focus of Park—as demonstrated by the title and abstract—is on the newly developed, superior sleepy stack structure. *See* Ex. 1007. Park states that the "sleepy stack structure can achieve more power savings than the forced stack technique and the self-controlled stacked transistors (e.g., 100x compared with 10x for the forced stack transistor or the self-controlled stacked transistors)." *Id*. at 2; *see also id.* at 1 ("Although the sleepy stack incurs some delay and area overhead, the sleepy stack technique achieves the lowest leakage power consumption among known state-saving leakage reduction techniques, thus, providing circuit designers with new choices to handle the leakage power problem."), 1 ("[U]nlike the forced stack technique, the sleepy stack technique can utilize high-V_{th} to achieve up to two orders of magnitude leakage power reduction compared to the forced

stack."), 13 ("For systems spending a large percentage of time in sleep mode yet requiring ultra-fast wakeup through maintenance of precise logic state, sleepy stack may provide the best solution currently known in VLSI design, typically resulting in approximately two orders of magnitude less leakage power over the best of all prior known state-saving VLSI design approaches."). Although a person of ordinary skill in the art *could* have selected the less effective forced stack over the sleepy stack, Petitioner has not sufficiently demonstrated why a person of ordinary skill in the art *would* have selected forced stack transistors. Without such an explanation, we infer that the forced stack was selected using impermissible hindsight because it could be used to modify Doyle to make a circuit claimed in the '674 patent.

We are not persuaded by Petitioner's evidence that a person having ordinary skill in the art would have used the inferior forced stack technique over the sleepy stack technique. Although Petitioner argues that the sleepy stack technique would require using a sleep signal, Petitioner does not argue or provide evidence establishing that a person of ordinary skill in the art would not have known how to implement the sleep signal. *See* Pet. Reply 23; 1316 Pet. Reply 23; Ex. 1018 ¶ 47 (Horst Supp. Decl.). Although Petitioner argues that "it is unclear how Patent Owner proposes that a [person having ordinary skill in the art] would have implemented Park's sleepy stack technique in the combination of Steinacker and Doyle" (Pet. Reply 23; 1316 Pet. Reply 23), that is an improper attempt to shift the burden of persuasion. It is Petitioner's burden to show that a person of ordinary skill in the art would have made Petitioner's proposed combination; it is not Patent Owner's burden to prove the opposite. *See Magnum Oil*, 829 F.3d at 1381 (It is Petitioner's "burden to demonstrate both that a skilled

artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention, and that the skilled artisan would have had a reasonable expectation of success in doing so." (quotations omitted)).

Finally, we are not persuaded by Petitioner's argument that, depending on the application, the forced stack technique is superior to the sleepy stack technique. *See* Tr. 33:14–35:5. We agree with Petitioner that "proposing an improvement to the prior art does not suddenly render the prior art non-obvious and thus patentable." Pet. Reply 23. However, in the obviousness inquiry, we must also consider whether "a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant." *In re Gurley*, 27 F.3d 551, 553 (Fed Cir. 1994). A reference "does not teach away. . . [if] it merely expresses a general preference for an alternative invention but does not 'criticize, discredit, or otherwise discourage' investigation into the invention claimed." *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 567 F.3d 1314, 1327 (Fed. Cir. 2009) (quoting *In re Fulton*, 391 F.3d 1195, 1201 (Fed. Cir. 2004)). However, "even if a reference is not found to teach away, its statements regarding preferences are relevant to a finding regarding whether a skilled artisan would be motivated to combine that reference with another reference." *Polaris Indus. v. Arctic Cat, Inc.*, 882 F.3d 1056, 1069 (Fed. Cir. 2018) (citing *Apple Inc. v. Samsung Elecs. Co.*, 839 F.3d 1034, 1051 n.15 (Fed. Cir. 2016) (en banc)).

In light of the clear teachings in Park that the sleepy stack technique is superior, Petitioner's conclusory argument that the forced stack technique

may be superior in some cases without identifying those cases is not sufficient. *See* Ex. 1007 1, 2, 13 (Park). That is, without evidence that the forced stack technique would have been superior when applied to Steinacker and Doyle, the evidence does not demonstrate that a person of ordinary skill in the art would have been motivated to use that technique. Instead, in the absence of evidence relating to the specific application, the evidence suggests that the person of ordinary skill in the art would have applied the sleepy stack technique with its tenfold increase in power savings. *See* Ex. 1007, 2 (Park) ("Our sleepy stack structure can achieve more power savings than the forced stack technique and the self-controlled stacked transistors (e.g., 100x compared with 10x for the forced stack transistor or the self-controlled stacked transistors).").

Because Petitioner's argument requires elements applying the forced stack technique to the combination of Steinacker and Doyle, Petitioner's failure to identify a sufficient rationale for combining the references is fatal to its argument that a claims 1, 2, 5–9, 12, 13, and 16–22 are unpatentable over Steinacker in view of Doyle and Park.[19]

We have considered the entirety of the evidence submitted by the parties, both for and against obviousness, and determine that Petitioner has not shown by a preponderance of the evidence that claims 1, 2, 5–9, 12, 13, and 16–22 of the '674 patent are unpatentable over Steinacker in view of Doyle and Park.

[19] Because we find Petitioner's arguments for the reason to combine insufficient, we do not need to address the remainder of Patent Owner's arguments, including the potential disadvantages of the combination and the separate argument directed to claim 5.

CONCLUSION[20]

For the foregoing reasons, we conclude that Petitioner has demonstrated by a preponderance of the evidence the unpatentability of claims 1, 2, 5–9, 12, 13, and 16–22 of the '674 patent. Specifically, Petitioner has demonstrated by a preponderance of the evidence that (1) claims 1, 2, 5, 6, 8, 9, 12, 13, and 17–21 would have been obvious under 35 U.S.C. § 103 in light of AAPA and Majcherczak and (2) claims 7, 16, and 22 would have been obvious under 35 U.S.C. § 103 in light of AAPA, Majcherczak, and Matthews. Petitioner has not demonstrated by a preponderance of the evidence that (1) claims 1, 2, and 5–9, 12, 13, and 16–22 would have been obvious under 35 U.S.C. § 103 in light of Steinacker, Doyle, and Park.

ORDER

In consideration of the foregoing, it is hereby:

ORDERED that claims 1, 2, 5–9, 12, 13, and 16–22 of the '674 patent are held unpatentable; and

FURTHER ORDERED that because this Decision is final, a party to the proceeding *see*king judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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[20] Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. *See* 84 Fed. Reg. 16654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

In summary:

Claims	**35 U.S.C. §**	**References**	**Claims Shown Unpatentable**	**Claims Not shown Unpatentable**
1, 2, 5–9, 12, 13, 16–22	103(a)	Steinacker, Doyle, Park		1, 2, 5–9, 12, 13, 16–22
1, 2, 5, 6, 8, 9, 12, 13, 17–21	103(a)	AAPA, Majcherczak	1, 2, 5, 6, 8, 9, 12, 13, 17–21	
7, 16, 22	103(a)	AAPA, Majcherczak, Matthews	7, 16, 22	
Overall Outcome			1, 2, 5–9, 12, 13, 16–22	

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