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CMOS Video Cameras

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Abstract

A single chip CMOS video camera is presented, along with design technique and characterization results. The chip comprises a 312×287 pixel photodiode array together with all the necessary sensing, addressing and amplifying circuitry, as well as a 1,000 gate logic processor, which implements synchronization timing to deliver a fully-formatted composite video signal and a further 1,000 gate logic processor, which implements automatic exposure control over a wide range. There are also simple solutions for γ correction and test.

1. Introduction

We introduce a new capability that extends the CMOS ASIC marketplace in a sector of high growth rates. This market sector is that of image sensing and processing, covering applications from electronic cameras to 'smart' vision systems.

Camera and vision systems addressed by today's CCD technology appear cumbersome, power-hungry and expensive. The experimental work reported here demonstrates that high-quality image sensors can be implemented entirely in commodity ASIC CMOS technology, operating from single 5v supplies.

The reported chip is a highly-integrated CMOS VLSI camera, shown in Figure 1. Most of the core area is a 312×287 pixel image sensor array, together with the necessary sensing, addressing and amplifying circuitry. The output signal can be either linear or γ corrected. γ correction is achieved by a simple solution which uses the nonlinear I_D-V_{GS} characteristic of an MOS transistor. The layout of the sensor is custom designed to make it as compact as possible.

At the top (Figure 1) is the 2,000 gate logic processor, laid out using a semi-custom standard-cell compiler. Half of these gates generate synchronization timing, including line-sync and frame-sync signals to format a 625line/50Hz standard composite video output. The other half of the gates are included to electronically control exposure over a wide range (40,000:1), enabling the use of a single fixed-aperture lens. The chip measures 7.58*mm* ×7.56*mm* , using 1.5 μm, 2 level metal CMOS technology.

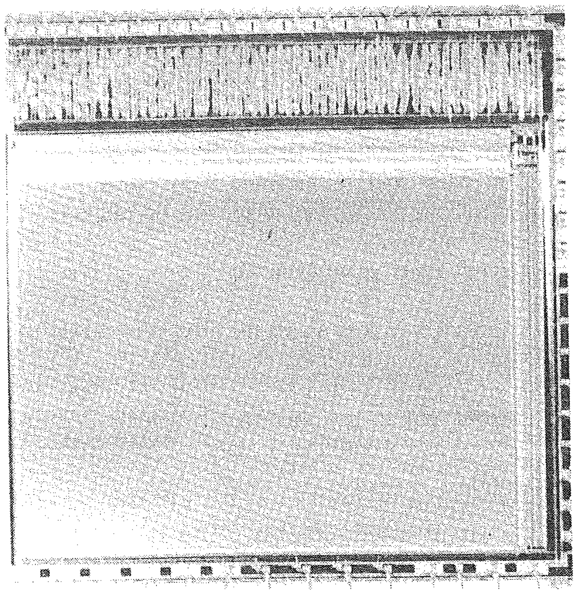
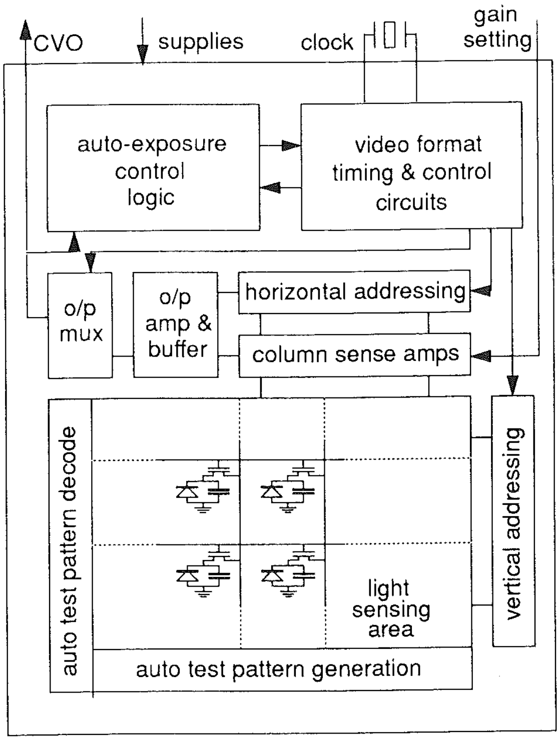


Figure 1. Photo-micrograph of single chip video camera

A video camera has been built using this chip along with a 6 MHz clock source, a 5 volt power supply, plus one bipolar transistor and a small number of resistors and capacitors required to match the line impedance to the monitor and decouple the power supply. The picture quality is subjectively excellent, and compares well with commercially available cameras.

2. Image Sensor Block

The architecture of the image sensor is shown in Figure 2. The light sensing area consists of a 312×287 diode array matrix, schematically indicated by the columns and rows of individual photodiodes. The pixel size is $19.6\mu m \times 16\mu m$, giving a light sensing area of $6.12mm \times 4.59mm$. This corresponds to the standard 1/2" format.



* CVO -- composite video output

Figure 2. Architecture of the image sensor

The photodiodes are accessed on the basis of sequential selection of each row through a vertical shift register. At the top of each column is a sense amplifier. The sensed information is read out sequentially along the x-direction under control of a horizontal shift register. At the end of the path there is an output amplifier [1,2].

The sense amplifier is a single-ended differential charge integrator. Its performance demands an accurate capacitor, formed by metal1/metal2 and metal1/poly. However, commodity ASIC CMOS technology sometimes can not guarantee the resulting capacitance values. We designed a gain-controllable integrator, shown in Figure. 3, which allows wide range of programmable variation of the capacitance value.

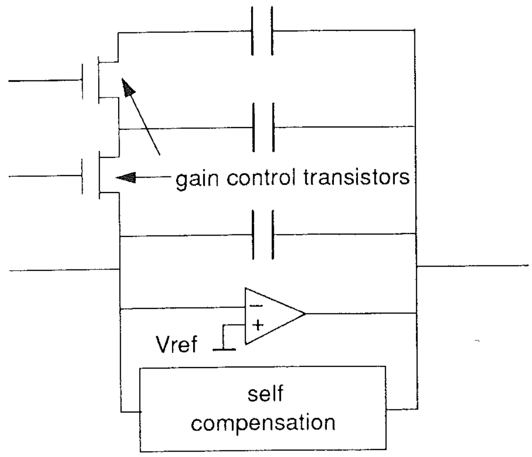


Figure 3. Integrator with programmable gain and self compensation

The main concern in the output stage design is the read-out speed required to achieve high resolution. A 6 MHz clock was chosen for this design; this gives a horizontal resolution of 312 pixels. The resultant picture quality is assured by a two stage output buffer with sample and hold function.

3. Automatic Exposure Control

The device automatically controls its exposure over a range of 40,000:1. Control is achieved by varying the integration time prior to reading each row of pixels. The integration time can be as long as one field, or as short as three cycles of the pixel clock(about 500ns).

The exposure is set by monitoring the video stream and estimating the fractions of each picture which are very white and very black. On the basis of this information, the device decides whether the picture contrast is acceptable, or too white, or too dark. If necessary, the exposure time is then changed, in the appropriate direction.

4. Generation of the Video Format Signal

Figure 4 shows a block diagram for the generation of the video formatted signal. The γ corrected image data is multiplexed with the sync-level and blanking-level, controlled by timing control signals, which are provided from the video timing block. A bipolar transistor (emitter follower) is needed to provide a low impedance output.

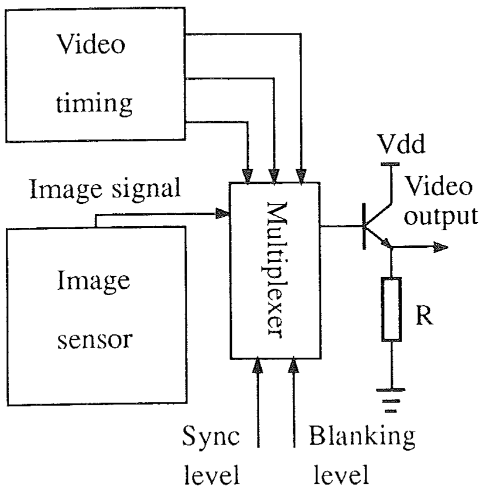


Figure 4. Generation of the video output

5. Simple Solution for γ Correction

The analogue image data needs to be γ corrected, to compensate for the nonlinearity of monitor tubes [3]. This is usually implemented using discrete components e.g. a ladder-network of diodes, resistors and reference voltages. Unfortunately, this is not suitable for integration. In this design γ correction is achieved by a simple solution which uses the nonlinear I_D-V_{GS} characteristic of an MOS FET, as shown in Figure 5.

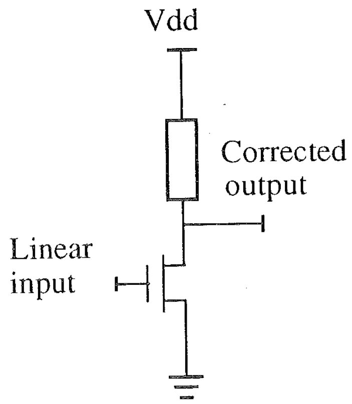


Figure 5. Gamma corrector

SPICE simulation was carried out and a simulation result is shown in Figure 6. A theoretical curve of ideal γ correction (γ =0.45) is also shown in Figure 6.

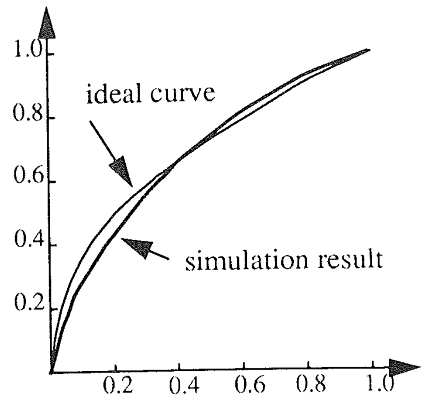


Figure 6. Gamma correction curves

6. Simple Solution for Test

Special consideration has been given to make it possible to carry out digital wafer test which is as complete as possible. The analogue parts are also tested by making them produce digital outputs, so avoiding a requirement for full analogue test. The test includes bit-line tests and word-line tests. Only a 0.78% increase in chip area was required to implement the on chip hardware necessary for this form of testing (Figure 2). The individual photo pixels may be tested if a sufficiently long vector set is allowable.

The chip can also self-generate a checkerboard pattern which may be displayed on a monitor screen, or captured by a frame grabber. This pattern can be used not only to find defective pixels, but also to check analogue performance parameters, such as read out speed and uniformity.

7. Eliminating Noise

Complete guard rings are put around all analogue parts to minimize interference from the digital parts. Routing is arranged with priority to analogue output and analogue power supplies. Analogue power supplies and digital supplies are separated, and supplies to different analogue parts are divided where necessary.

There are two sources of fixed pattern noise: threshold variation in the MOS pixel access transistors causing speckles, and mismatches between the column sense amplifiers causing vertical stripes. The solution to the pixel threshold variation is to reduce the pixel reset voltage below (Vdd-Vt) so that the reset voltage is insensitive to the variation of the threshold Vt.

Column fixed pattern noise arises mostly from offset mismatches in the column sense amplifiers. We have successfully eliminated this problem by automatically compensating each amplifier to give zero offset during each line synchronization interval.

8. Characterization

An optical test measurement set-up was used to characterize the camera. The following table summarize the measured results of the performance characterization experiments. The parameters of typical monochrome CCD cameras are also given for comparison.

parameter	CMOS	CCD
operating voltage for camera	5v	12v
power dissipation for chip	50mW	
power dissipation for camera	200mW	1W
s.n.r.	51dB	52dB
exposure range	40,000:1	300:1
saturation level	20lux	20lux
antiblooming factor	100x	100x
dark current*	0.0004	0.005

* as fraction of saturation at room temperature, 20msec integration time

9. Conclusions

We have developed several design techniques to achieve a single chip camera, in unmodified CMOS technology, which matches the performance of CCD cameras. The design has proven that three technical barriers which most greatly influence new product development; cost, power consumption and size, are all dramatically reduced over today's solid-state camera technologies.

10. Acknowledgements

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